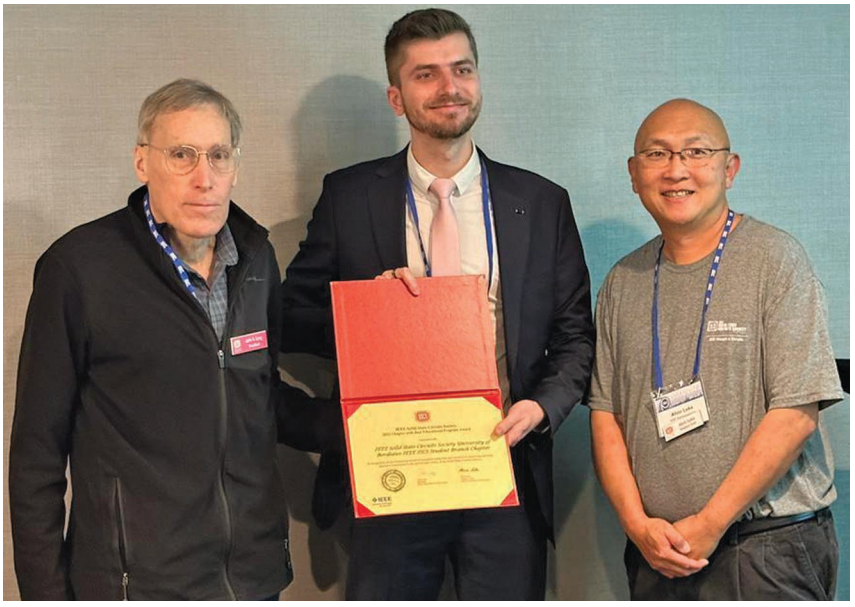
and its breathtaking photos captured by radar technology.

On 24 March 2023, the Chapter invited Prof. Makoto Ikeda, SSCS Distinguished Lecturer, University of Tokyo, Japan, for a special talk to celebrate the 75th anniversary of the transistor. Ikeda delivered a captivating presentation that delved into the fascinating history of the transistor, followed by an in-depth exploration of public key encryption basics and the optimization design of elliptic curve-based encryption algorithms, highlighting the importance of security measures in this field. During the coffee break, the audience was treated to a unique pastry specialty of Bordeaux, called a "canelé," shaped as the logo of the 75th anniversary of the transistor.

The three events attracted over 100 people, including local IEEE Members. The audience, composed of students and researchers, was impressed by every presentation.



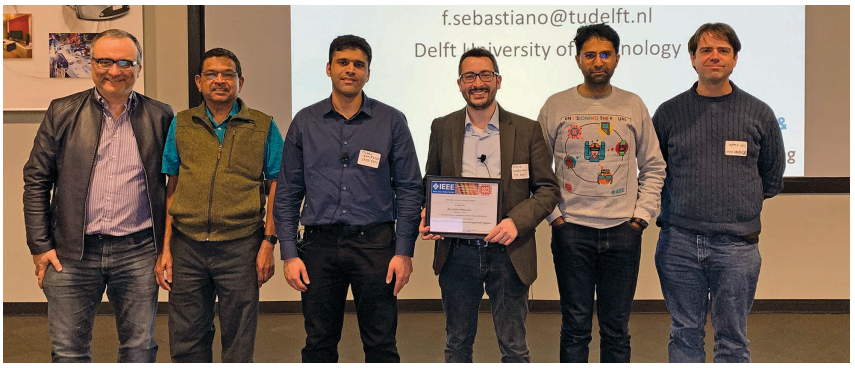
SSCS President John R. Long and SSC Chapters Chair Alvin Loke present the Best Educational Program Award to the Bordeaux University SBC.

The SSCS Bordeaux University SBC also received the Best Educational Program Award during the 2023 International Solid-State Circuits Conference, in San Francisco, CA, USA.

—Maxandre Fellmann

Recent IEEE SSCS Silicon Valley Chapter News: Seminars, Workshops, Distinguished Lectures, and Silicon Valley Engineering Hall of Fame Awards Ceremony Honoring Dr. Bill Dally, Nvidia and Stanford

The IEEE Solid-State Circuits Society (SSCS) Santa Clara Valley (SCV) Chapter held several well-attended seminars, webinars, workshops, and Distinguished Lecturer (DL) talks over the past three years, throughout the pandemic, and recently attended the Silicon Valley Engineering Council (SVEC) Engineers Week Banquet and Hall of Fame Awards Ceremony, in February 2023, honoring Dr. Bill Dally, chief scientist, Nvidia, and adjunct professor, Stanford University, who is also well known in our SSCS community. This article highlights the wide variety of events covering topics from mixed-signal and analog circuits, high-speed links, machine learning acceleration, and the semiconductor industry. The speakers included professors and postdoctoral scholars from academia as well as start-up founders, technology



Prof. Sebastiano (center) poses with the SSCS Silicon Valley Chapter committee members.

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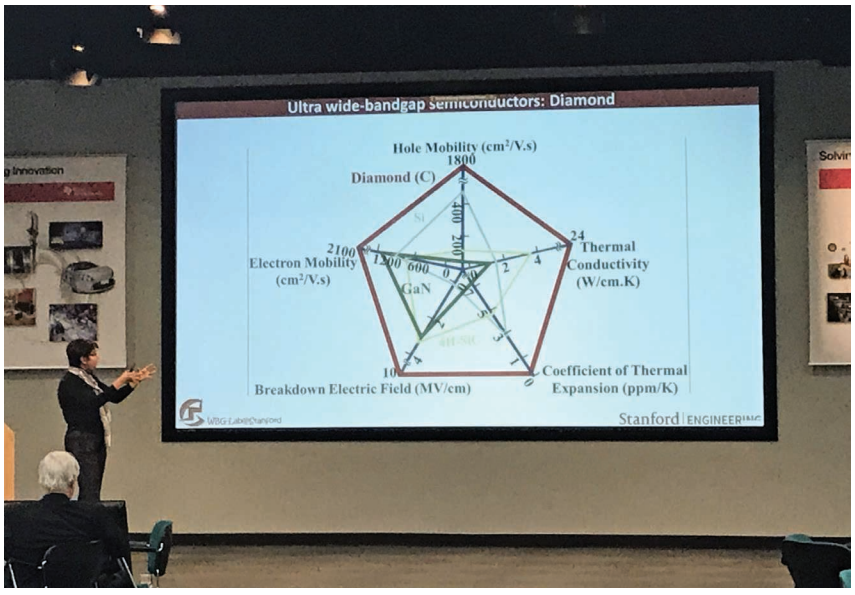
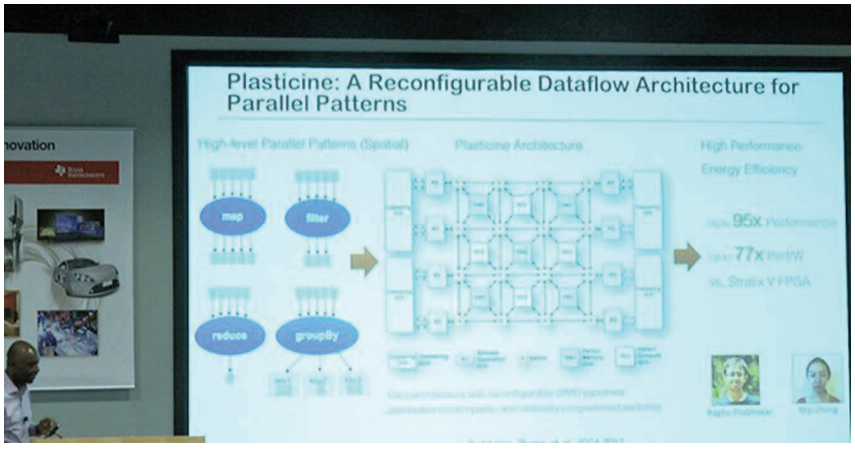
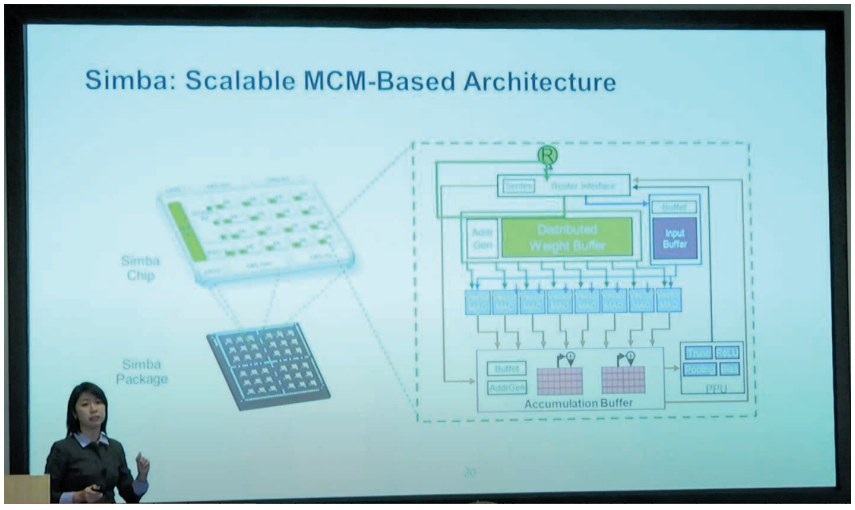


Prof. Chowdhury explains the ultra-WBG semiconductor diamond.



Prof. Olukotun delivers "Plasticine: A Reconfigurable Dataflow Architecture for Software 2.0" at the SSCS-SCV event.



Prof. Shao explains machine learning accelerators.

leaders, and executives from industry. Please contact us if you are interested in presenting at our meetings, would like to attend Chapter events, or wish to volunteer. Full information on Chapter activities and upcoming seminars is available on the Chapter website: https://r6.ieee.org/scv-sscs/.

21 February 2019: "Cryogenic CMOS Interfaces for Large-Scale Quantum Computers," DL Fabio Sebastiano, TU Delft

In his talk, Prof. Fabio Sebastiano addressed the challenges of building scalable cryogenic CMOS interfaces for large-scale quantum computers, enabling the readout of thousands to millions of qubits. He highlighted the need for accurate cryogenic device models and quantum-electronic system codesign and presented results on an experimental interface operating at temperatures down to 4 K.

5 December 2019: "Enabling Circuits and Technologies for Addressing Some of the 21st Century's Hard Energy Challenges With Wide Bandgap Semiconductors and Devices," Srabanti Chowdhury, Stanford University

In her seminar, Prof. Srabanti Chowdhury covered a range of topics, including how wide-bandgap semiconductor (WBG) devices, namely, GaN and diamond, can enable more efficient power conversion and higher power density to meet the demands of future electronic systems.

11 August 2021: "The Analog Designer's Toolbox (ADT): Towards a New Paradigm for Analog IC Design," Hesham Omran, Ain Shams University and Master Micro

Prof. Hesham Omran examined how to rethink analog IC design methodology with the Analog Designer's Toolbox (ADT), a new design methodology and automation tool to systematically explore the analog design space using g_m/I_D design methodology and precomputed lookup tables.

18 April 2019: "Plasticine: A Reconfigurable Dataflow Architecture for Software 2.0," Kunle Olukotun, Stanford University and SambaNova Systems

In his talk, Prof. Kunle Olukotun discussed how to create the performant and reconfigurable hardware platform needed to enable Software 2.0. He introduced Plasticine, a new spatially reconfigurable architecture designed to efficiently execute applications composed of parallel patterns, which laid the groundwork for SambaNova Systems' solutions.

24 July 2019: "Squeezing Down the Computing Requirements of Deep Neural Networks," Forrest Iandola, DeepScale

Forrest Iandola covered several techniques to squeeze deep neural networks (DNNs) into smaller computing footprints, including better DNN design, DNN quantization, better implementations of DNNs, and better utilization of specialized computing hardware. With a particular emphasis on computer vision, Iandola showed how neural architecture search technologies have begun to make significant progress in automating the process of designing "squeezed" DNNs.

16 January 2020: "Scalable and Productive: Holistic Hardware Optimizations for Machine Learning Acceleration," Sophia Shao, University of California, Berkeley

In her talk, Prof. Sophia Shao described her recent work on building scalable and efficient machine learning systems that deliver real-time and robust performance across diverse deployment scenarios through joint hardware-software optimizations.

Mixed-Signal Circuit Design Seminars

19 November 2020: "Low-Spur PLL Architectures and Techniques," Mike Chen, University of Southern California

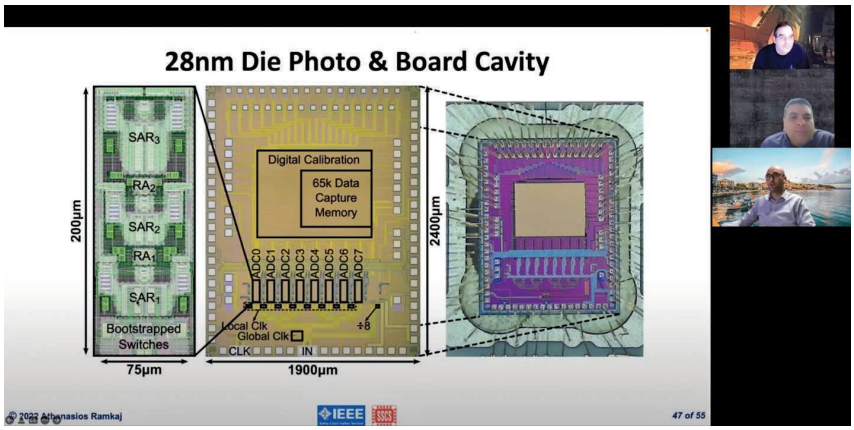
Prof. Mike Chen examined the sources of spurious tone generation in different PLL architectures and operation modes, providing an overview of design techniques to mitigate spurious tones and diving into several real PLL design examples with low-spur performance.

15 September 2021: "Automatic Generation of SystemVerilog Models From Analog/Mixed-Signal Circuits: A Pipelined ADC Example," Jaeha Kim, Seoul National University

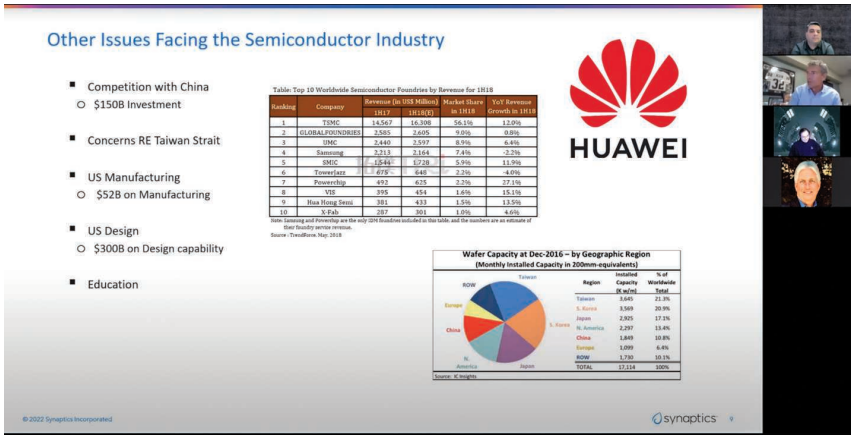
In his webinar, Prof. Jaeha Kim discussed his cutting-edge research in analog and mixed-signal circuit functional modeling using SystemVerilog, with a pipelined ADC as the primary example. This seminar was broadcast live online.

26 January 2022: "Design Considerations Towards Optimal High-Resolution Wide-Bandwidth Time-Interleaved ADCs," Athanasios Ramkaj, Stanford University

In his talk, given in a webinar format, Dr. Athanasios Ramkaj, a postdoctoral scholar in the Murmann Mixed-Signal Group at Stanford University and now with AMD, discussed his



Hurlston (right, middle pane) presents his perspectives on the semiconductor industry.



Dr. Ramkaj (right, bottom pane) showcases his 5-GS/s 8× interleaved ADC in 28 nm during his talk at the virtual SSCS-SCV event.

SVEC

Dr. Dally (right) is inducted into the Silicon Valley Engineering Hall of Fame.

SVEC

Silicon Valley Hall of Fame inductee Dr. Dally gives his acceptance speech to a crowd of local engineers at the CHM.

SVEC

Dr. Shen delivers the keynote speech at the SVEC Hall of Fame Awards Ceremony.

SVEC

Outstanding students in STEM are awarded SVEC scholarships by SVEC President and SSCS Silicon Valley Chapter Past Chair Zadeh (right).

state-of-the-art research toward achieving optimal high-speed high-resolution time-interleaved ADCs.

Wireline Seminars

8 September 2021: "Communication Link Modeling Using PyBERT," David Banas, Luminous Computing

In his talk, David Banas covered a range of topics, including serial communications link modeling and equalization optimization, using the public domain open source tool PyBERT.

1 June 2022: "Global Architectural Optimization of 100+ Gb/s Wireline Transceivers," Tony Chan Carusone, Alphawave IP, University of Toronto

Prof. Tony Chan Carusone discussed how to identify optimal architectural tradeoffs in high-speed links at bleeding-edge data rates above 100 Gb/s, where subtle interactions between the analog front end and digital equalization, timing recovery, and forward error correction impact the BER, and, thus, the transceiver design, significantly.

Executive Seminars

9 February 2022: "The Semiconductor Shortage—Cause and Effect," Michael Hurlston, President and Chief Executive Officer, Synaptics

In this executive series webinar, Michael Hurlston, president and chief executive officer, Synaptics, discussed the causes and effects of the semiconductor supply chain shortage.

SSCS Silicon Valley Chapter Attends SVEC Engineers Week and Silicon Valley Engineering Hall of Fame Awards Ceremony Honoring Dally

Every year during Engineers' Week, in February, the SVEC (www.svec.org) holds an awards ceremony and banquet to honor outstanding individuals for their contributions by inducting them into the Silicon Valley Engineering Hall of Fame. The awards ceremony also features a distinguished keynote speech and awards several scholarships to students for academic excellence. The Hall of Fame ceremony recognizes engineers and academics for their outstanding professional achievements and significant contributions to the community. The SSCS Silicon Valley Chapter, along with other engineering societies in the San Francisco Bay, CA, USA, area, attends the event and supports

SVEC scholarships for outstanding students at local colleges in science, technology, engineering, and mathematics (STEM). SSCS Silicon Valley Chapter Past Chair Sharif Zadeh has served on the SVEC board over the past few years and is currently the SVEC president.

This year, the 32nd annual National Engineers Week Banquet and Hall of Fame Awards Ceremony was held on 24 February 2023 at the Computer History Museum (CHM), in Mountain View, CA, USA. The keynote speaker was Dr. Kang Shen, director, Wu Tsai Neuroscience Institute, Stanford University. The 2023 Hall of Fame inductee was Dally, chief scientist and senior vice president, research, Nvidia, and adjunct professor, Stanford, who is also well known in our SSCS community.

Dally was inducted into the Silicon Valley Engineering Hall of Fame for contributions to GPU computing, as a professor of computer science, and as chief scientist at Nvidia, which led to the world's fastest most energy-efficient supercomputers and enabled the current revolution in artificial intelligence.

—Luke Sammarone,
SSCS Silicon Valley Chapter

IEEE SSCS University of Science and Technology of China Student Branch Chapter Wins Outstanding Chapter of the Year and Holds Numerous Events

The IEEE Solid-State Circuits Society (SSCS) University of Science and Technology of China (USTC) Student Branch Chapter (SBC) won the SSCS Student Branch Chapter of the Year award. The award was received by Chapter Advisor Prof. Fujiang Lin during the Chapter Chair Luncheon at the International Solid-State Circuits Conference, on 21 February 2023.

The SSCS USTC SBC, in collaboration with the School of Microelectronics, is working to educate student members and enhance their life by organizing lectures and outdoor activities. Lectures have been conducted in person as well as virtually. These events were an excellent opportunity for SBC members to connect and network.

On 9 November 2022, the SSCS USTC SBC organized a talk by Dr. Mingqiang Huang, associate researcher, Shenzhen Advanced Technology Research Institute, Chinese Academy of Sciences. The lecture was held at the fusion building, north campus, School of Microelectronics. He talked about intelligent computing with high performance and low power

The SSCS USTC SBC wins the 2022 SSCS Student Branch Chapter of the Year award.

The lecture speakers: (top row, left to right) Dr. Huang, Prof. Li, Dr. Zhao, and Prof. Hu as well as (bottom row, left to right) Prof. Yu, Prof. Zheng, Dr. Tang, and Prof. Su.

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