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Wide band gap circuit optimisation and performance comparison

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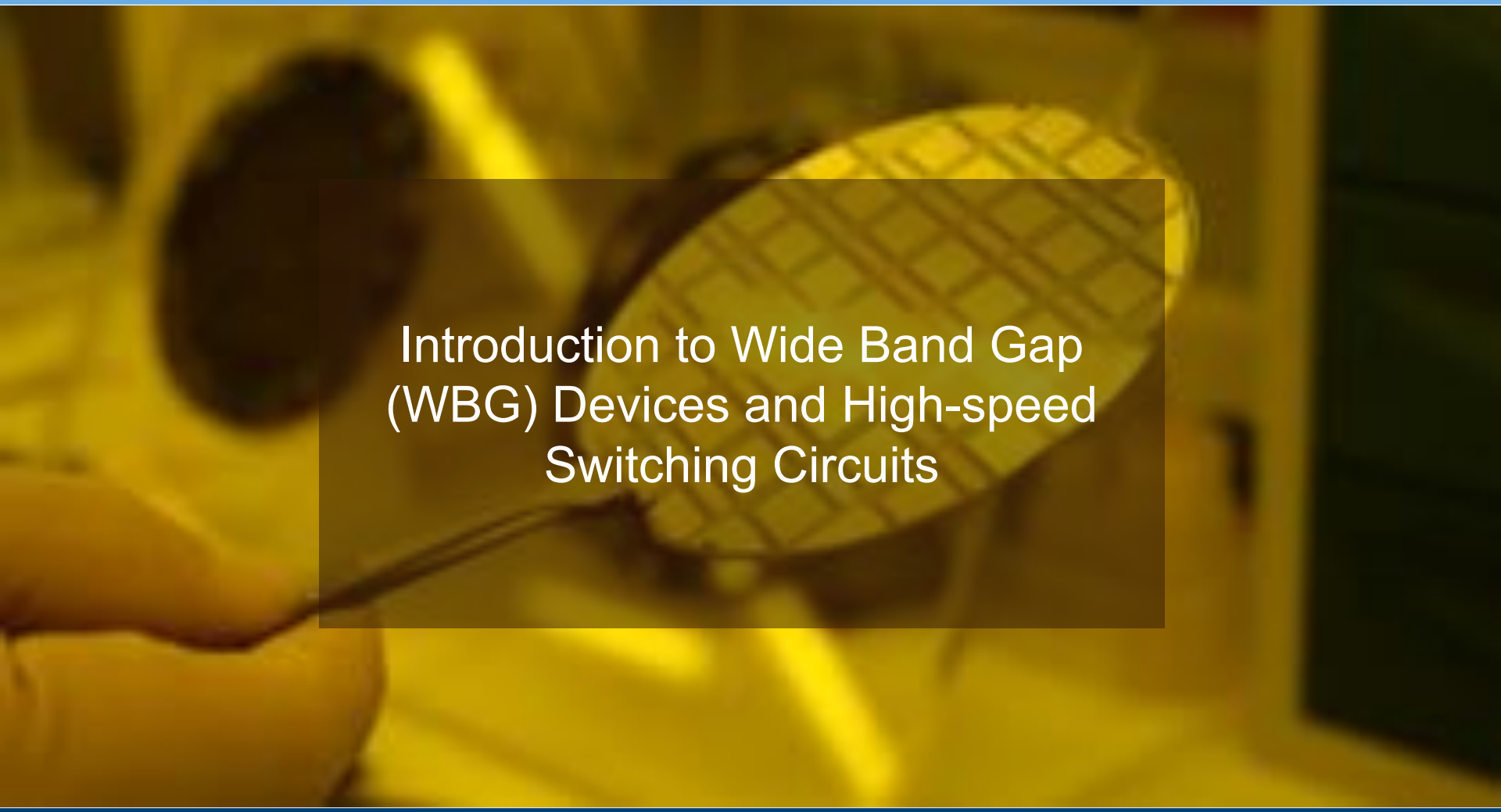
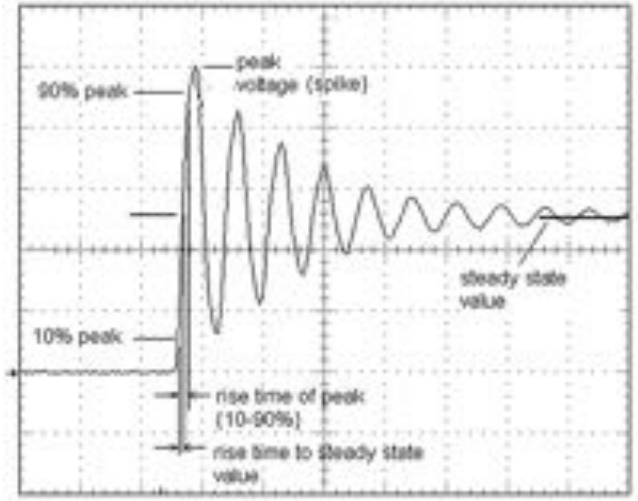
Section 1



Introduction to Wide Band Gap (WBG) Devices and High-speed Switching Circuits

WBG Power Transistor Switching Circuits

- WBG power devices are inherently fast switching, and should be used in this way to get maximum cost / benefit out of them.
- This fast switching brings new challenges to power electronics engineers, as they now have to deal with very fast voltage and current slew rates.
- Typical voltage and current traces after the switch point show significant ringing oscillation that is poorly damped.
- This can have significant power dissipation and EMC implications.
- At switch-off, excessive voltage over-shoot can cause device failure.



Three Parasitic Inductances

The main parasitic inductive elements are:

1.Common source inductance: Shared between gate-drive and power circuit, inside device package and external connectivity on PCB.

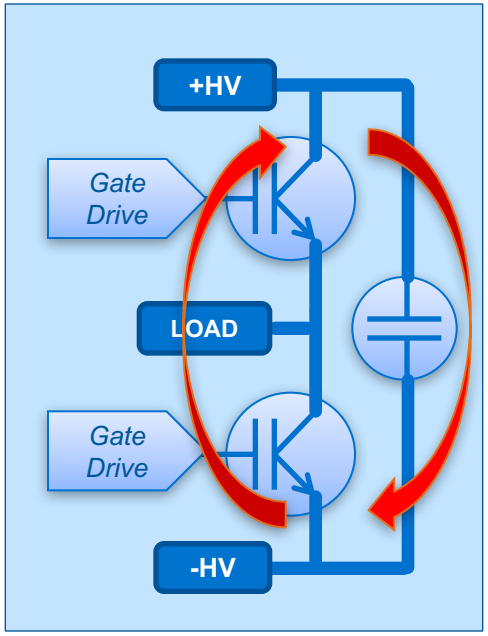
2.Gate loop inductance: Due to area enclosed by gate-drive current path to the switching die and the return path from the source connection back to the gate-drive 0V.

3.Switched current commutation loop inductance: Caused by magnetic field generated when switching the load current from the top device to bottom device (or vice-versa) in a half-bridge switching topology.

Reduced by careful PCB layout giving consideration to cancellation of the loop magnetic field.

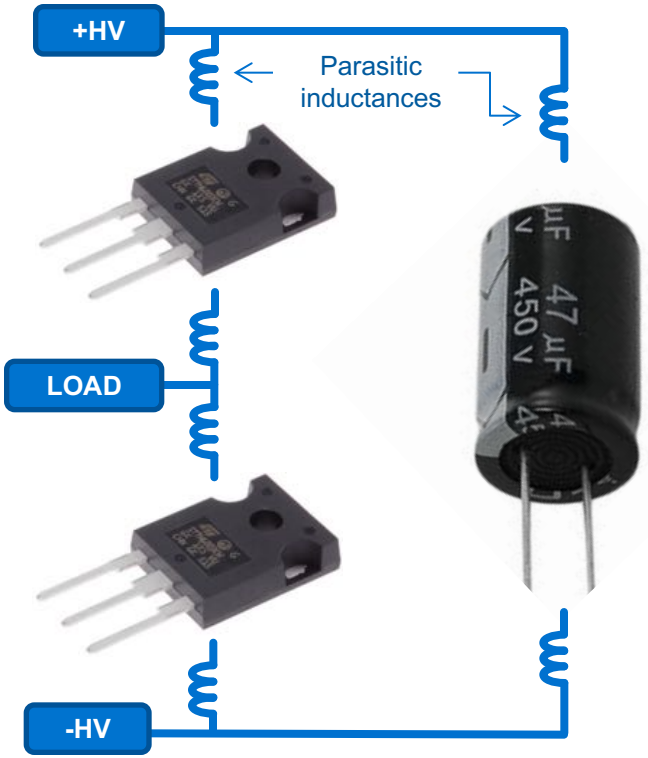
Switch Current Commutation Loop Inductance

Half-bridge schematic



Commutation loop inductance: Loop around two switching transistors and DC-bus de-coupling capacitors.

Switched loop commutation inductance

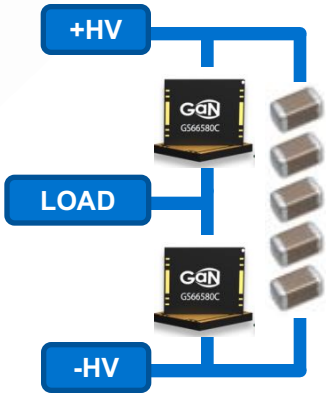


⇦ High commutation loop inductance:

- TO247 packages.
- Simple PCB layout.

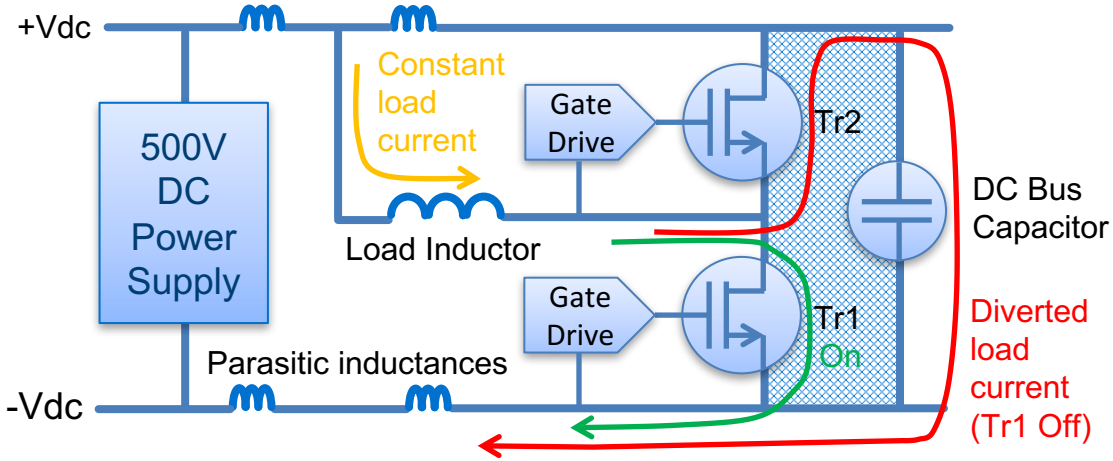
⇩ Low commutation loop inductance:

- SMD packages.
- Multi-layer PCB.

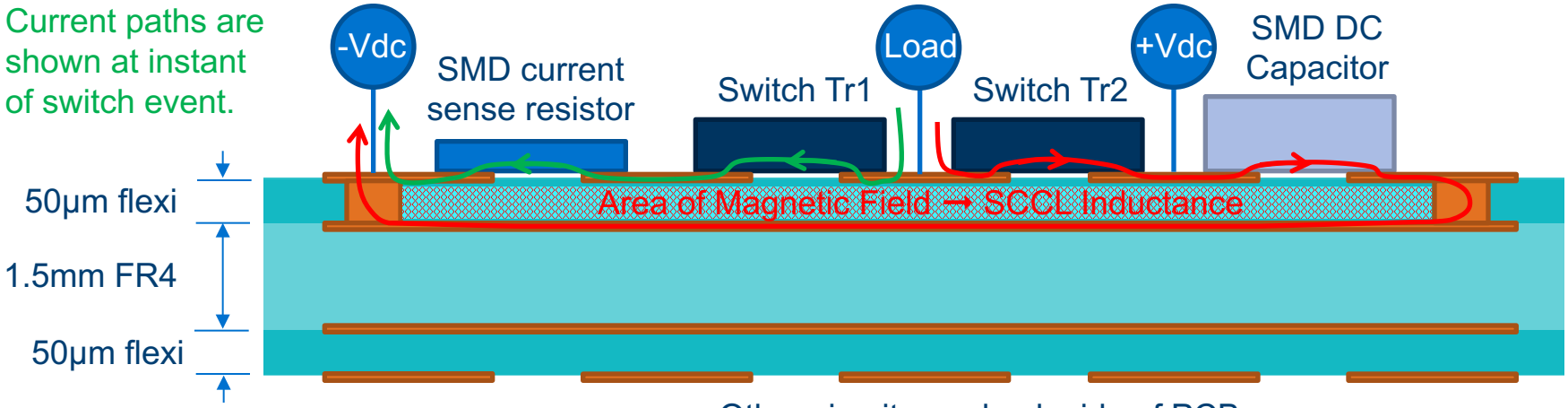


Low Inductance PCB Layout

- PCB construction to minimise **Switched current commutation loop inductance.**
- Multilayer FR4 and flexi polyamide with heavy copper weight tracks.
- Reduce inductance by minimising area of switched current loop.



Current paths are shown at instant of switch event.

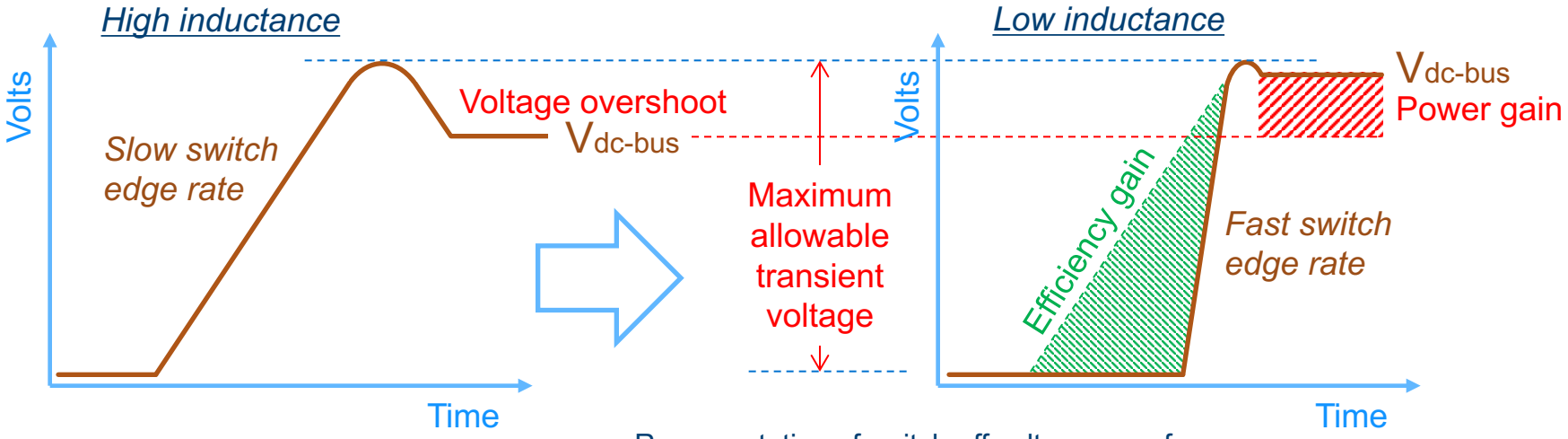


Benefits of Low Inductance Switching

- Fast edge-rate reduces switching losses, increasing efficiency at high PWM freq.
- Low voltage overshoot:
  - Maximise power throughput and device utilization.
  - Maximize efficiency with lowest Rds(on) transistors.

Low switch commutation loop inductance achieved with:

- SMD transistor packages.
- SMD local DC-bus decoupling capacitors.
- Multi-layer PCB with magnetic field cancelling layout.



Representation of switch-off voltage waveform

Device packaging inductance chart

	 IGBT Module	 TO247	 SMD
Achievable Power Circuit Loop Inductance (typical)	100nH	20nH	<1nH
Typical Current Rating	500A	100A	50A
Interconnect type	Bus bars	Standard PCB	Flexi PCB
Overshoot @ 1A / nsec	100V	20V	2V
Overshoot @ 10A / nsec	1kV	200V	20V

- Conventional packaging demonstrates unacceptable voltage overshoot at high di/dt.
- This problem can be overcome with SMD packaging and correct circuit layout.

Section 2

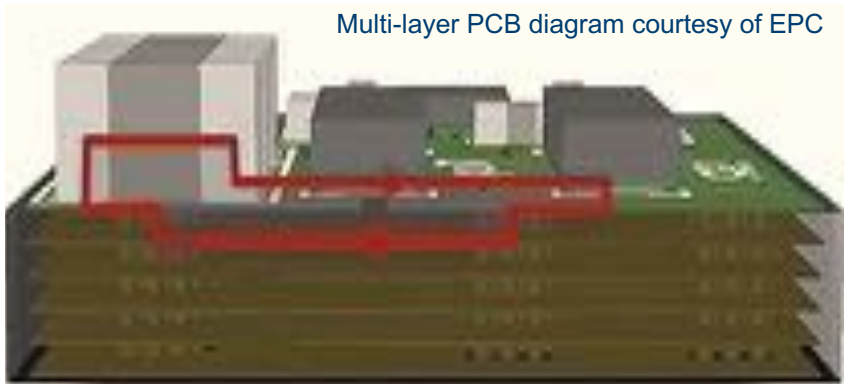
GaN Development Platform: Design and Test Results

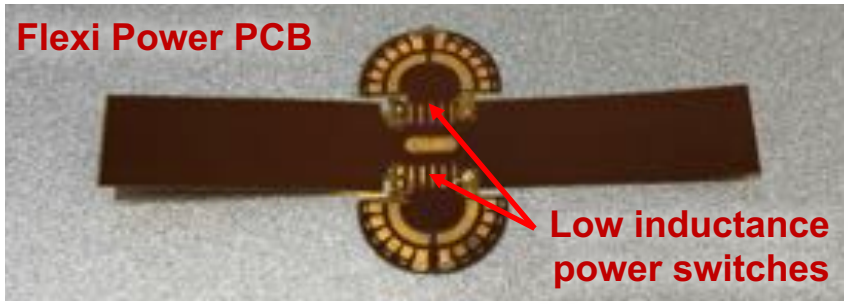
GaN Development Platform: Overview

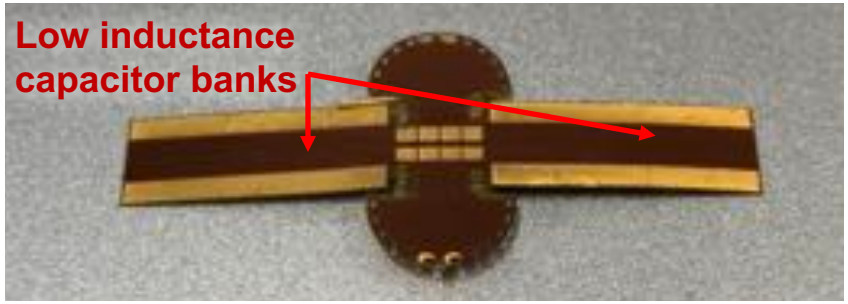
- Test platform to establish fundamental operating principles and limitations of GaN power switching devices.
- Integrated linear current gate-drive and high-bandwidth measurement circuits.
- Low inductance gate-drive and switched power commutation loop (on 25um thick polyamide flexi-circuit to minimise magnetic field).
- Designed around 200V, 22A, EPC GaN HEMT 'FET' in a chip-scale package.
- Circuit is designed for highest performance.

EPC GaN Die (underside)

Multi-layer PCB diagram courtesy of EPC





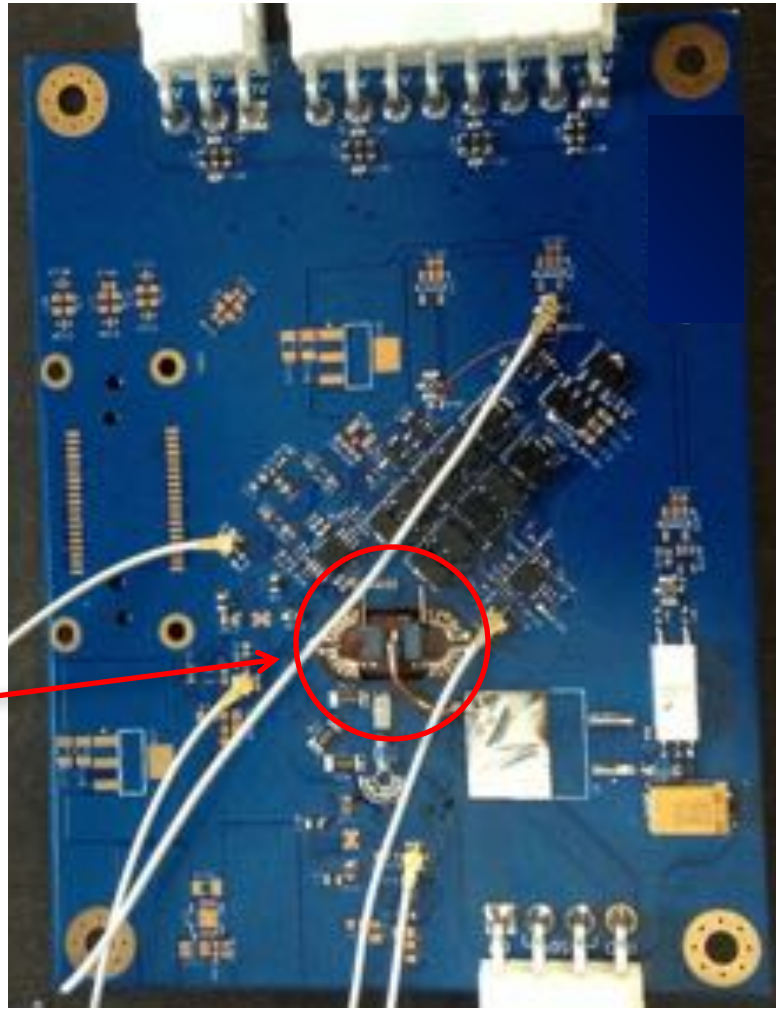


GaN Development Platform: Introduction

- Half-bridge demo circuit, using two EPC GaN eHEMT power devices.
- Local DC-bus capacitors and 25um thick flexi-pcb gives very low switch commutation loop inductance.
- Current-source gate drive on lower switch device. Top switch device configured in diode mode.
- Embedded measurement circuits looking at four parameters:

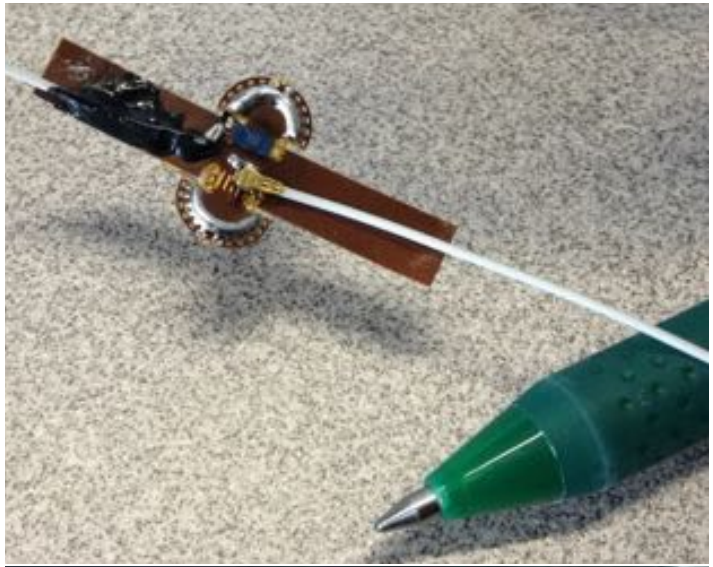
  Vds, Is, Vgs, Ig

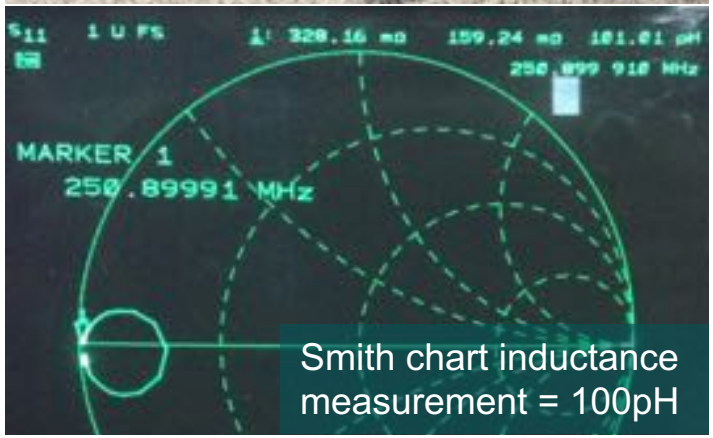
- Embedded current measurement has very low insertion resistance and inductance.



Switched Current Commutation Loop Inductance

- Low inductance switch commutation loop achieved with power circuit on flexi-pcb sub-circuit (25um thick flexi-pcb polyamide core thickness with 2oz copper tracks / planes).
- Half-bridge configuration with integrated DC-bus capacitors (contained on flexi-sub-circuit).
- With current measurement, total loop inductance = 750pH (worst case at 600MHz).
- Without current measurement, loop inductance = 500pH (worst case at 600MHz).
- VNA test results show 100pH (at 250MHz) loop inductance of bare-flexi-pcb and one GaN transistor in circuit.

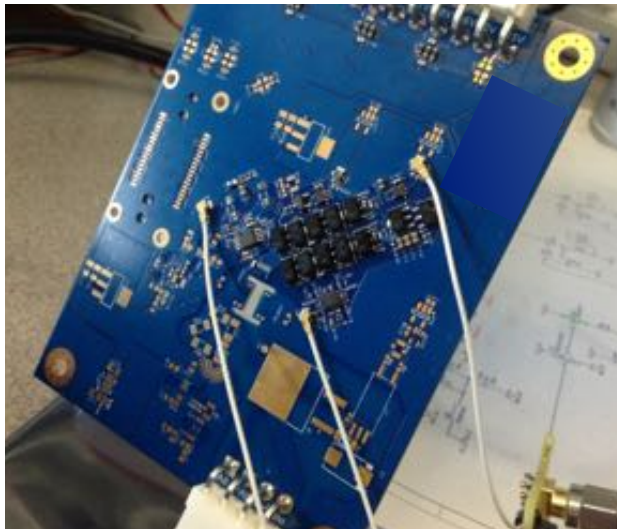


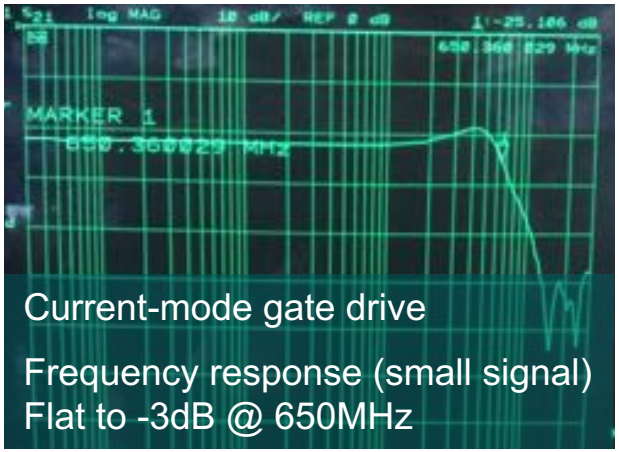


Smith chart inductance measurement = 100pH

Current-source Gate-drive

- Current-source gate-drive (linear voltage-to-current amplifier driving into a capacitive gate load).
- 650MHz bandwidth (with integrator transfer function).
- 1n sec propagation delay (for stable closed-loop control applications).
- Gate voltage: +6V to -1V (specifically for driving eHEMT GaN) with +/- 400mA drive capability.
- Low power: Gate-drive amplifier is enabled only during switch event, with MOS clamps to supply rails during constant on/off period.
- Discrete implementation at present: Simple ASIC development possible for size and cost reduction.



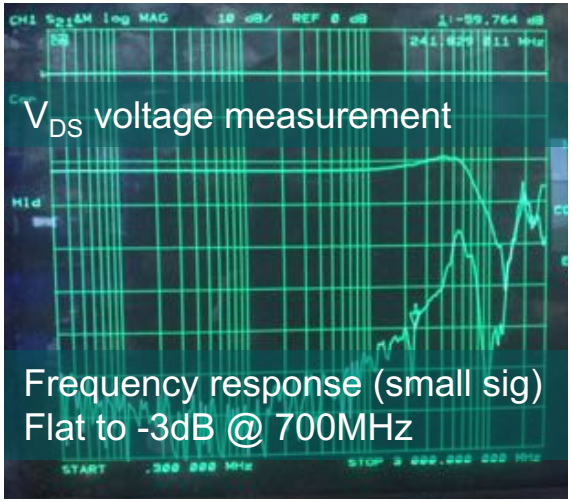


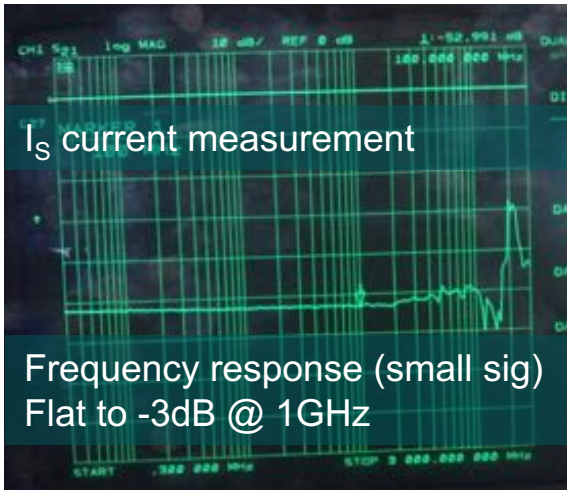
Current-mode gate drive

Frequency response (small signal)
Flat to -3dB @ 650MHz

In-circuit Embedded Measurement

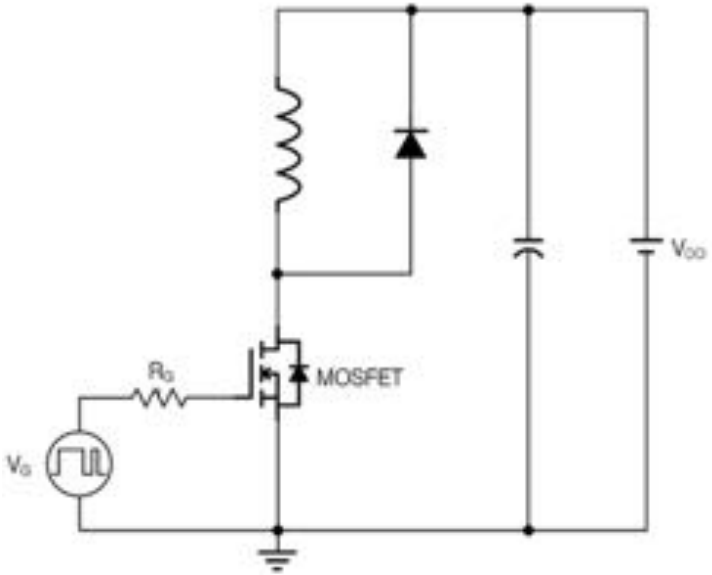
- High bandwidth current and voltage measurements are needed to properly test GaN switching circuits. This is not possible with conventional scope probes.
- High-voltage measurement probes act as un-terminated transmission line, giving spurious results.
- 700MHz high voltage measurement using RC potential divider chain. Scaleable to 3kV and beyond. Buffered 50 ohm output to scope.
- Current measurement probes add unacceptable loop inductance, degrading performance of circuit.
- 1GHz current measurement using 10 mOhm resistive shunt (approx. 100mV at 10A), with inductance compensation. Buffered 50 ohm output to scope.
- Gate-voltage and gate-current measurement circuits have similar performance.

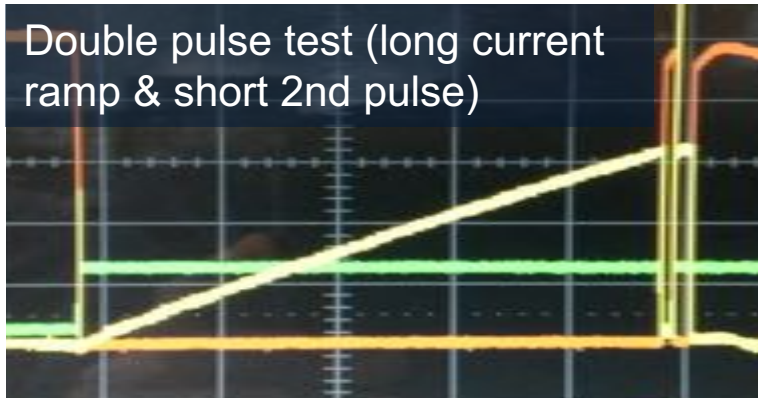




Test Configuration – Double Pulse Test

- Half-bridge configuration with eHEMT GaN switch devices (EPC chip-scale parts rated at 200V / 12A).
- 100Vdc-bus, 10A from inductive load.
- Lower device has gate-drive, top device acting as catch-diode.
- Double-pulse test at 10Hz, so no significant power dissipation.
- Four channels of waveforms, all with embedded measurement and 50 ohm connections to 4Gsps LeCroy oscilloscope.
- Double pulse drive signal from arbitrary waveform generator. Electrical power from bench-top PSUs.

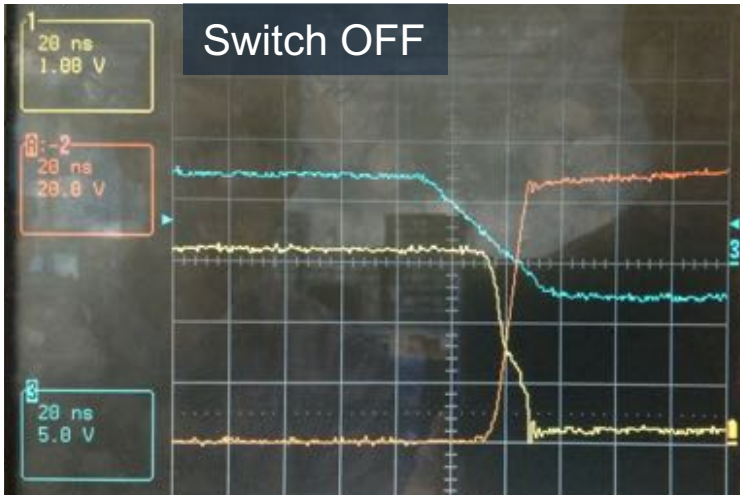


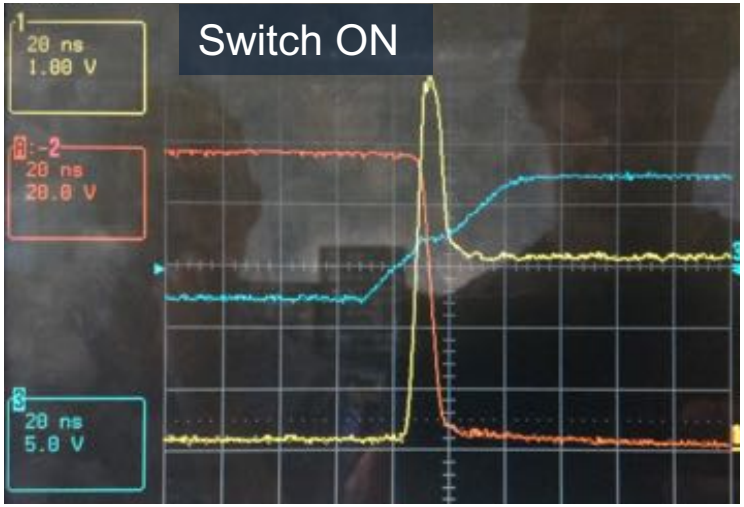


GaN Development Platform: Test Results

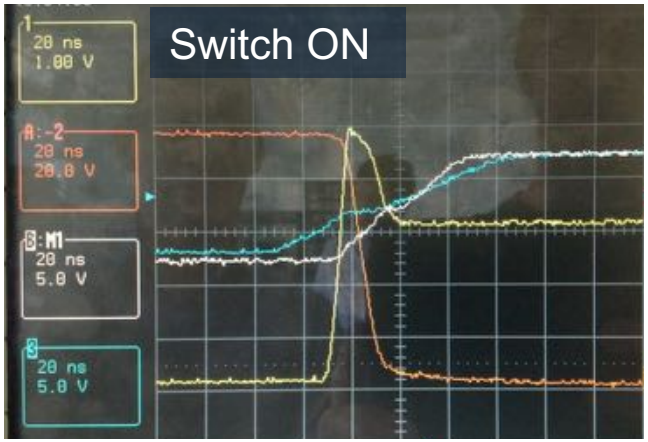
- Medium gate-drive current level (200mA)
- At turn-OFF:
  - No voltage over-shoot.!!
  - dI/dt 'hesitation' due to switch device capacitance (charged by load current).
- At turn-ON:
  - dI/dt = 10A in 4nsec.
  - dV/dt = 100V in 10nsec.
  - Current spike during dV/dt due to output capacitance of GaN switch devices (normally masked by ringing).
- Scope traces:

  Red = Vds Yellow = Is Blue = Vgs



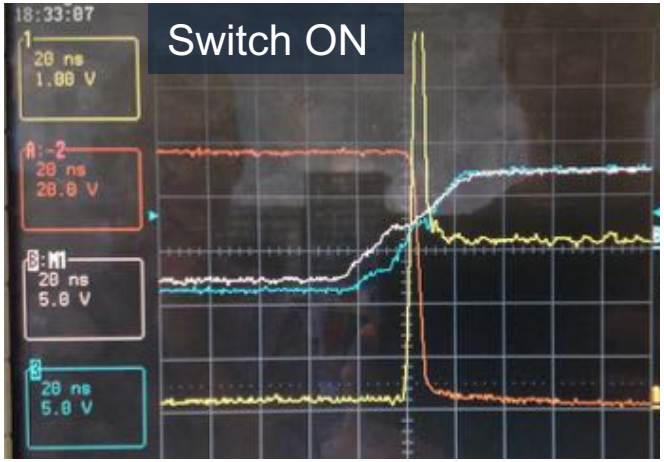


GaN Development Platform: dV/dt Comparison



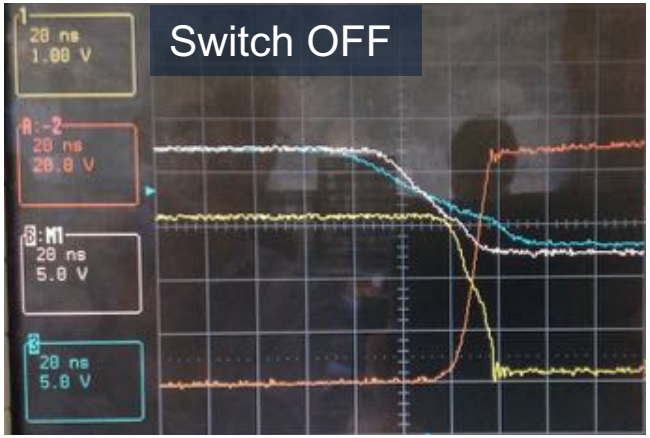
Left scope waveforms:

- Slow dV/dt with 100mA gate drive current.
- 10 V/nsec.



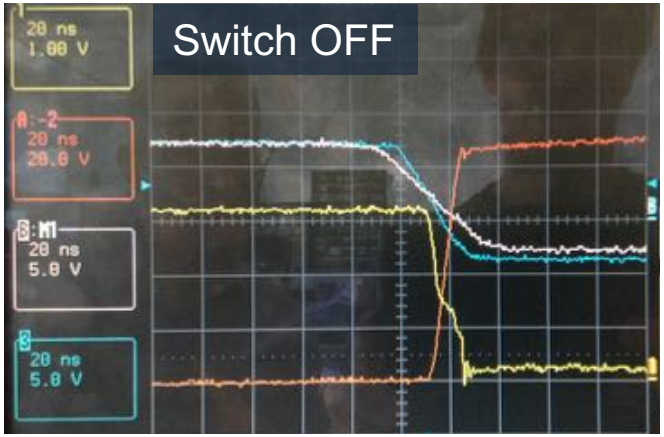
Right scope waveforms:

- Fast dV/dt with 400mA gate drive current.
- 5 V/nSec.



dV/dt was found to be:

- Invariant of load current*
- A linear function of gate drive current.



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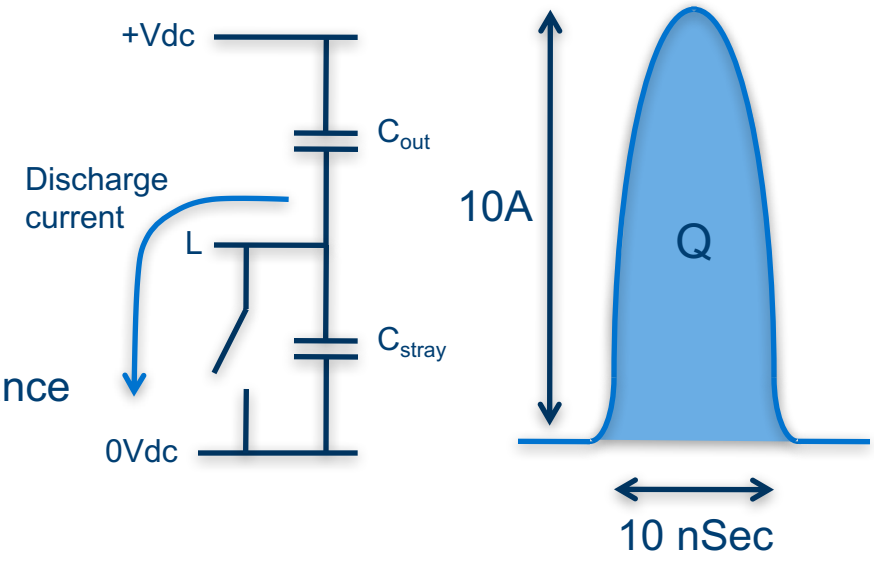
* Turn-off at light loads dependent on load current to charge output capacitances so will see extended slew times.

GaN Development Platform: C_{out} Discharge Spike

EPC2010C GaN power transistor:

- 200V, 25mOhm, 22A rated
- C_{out} = 240pF (datasheet)
- C_{stray} = 20pF (measured)



With 100Vdc-bus, stored charge output capacitance of top transistor and stray node capacitance,

$Q = V \times (C_{out} + C_{stray}) = 100V \times 260\times10^{-12}pF$

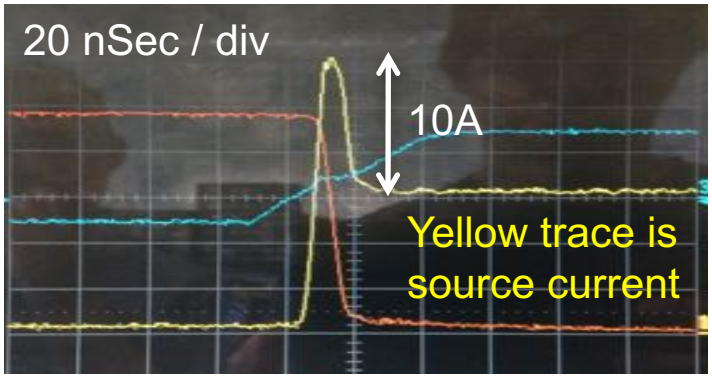
$= 2.6\times10^{-8}$ Coulombs

With 10A discharge current, area under current spike,

$Q = 0.5 \times I \times t = 0.5 \times 10 \times 10\times10^{-9}$ (approximately)

$= 2.5\times10^{-8}$ Coulombs!

This demonstrates that the current spike in switch-on waveform is caused by the output capacitance.



Section 3

WBG Development Platform: Design and Methodology

WBG Development Platform: Overview

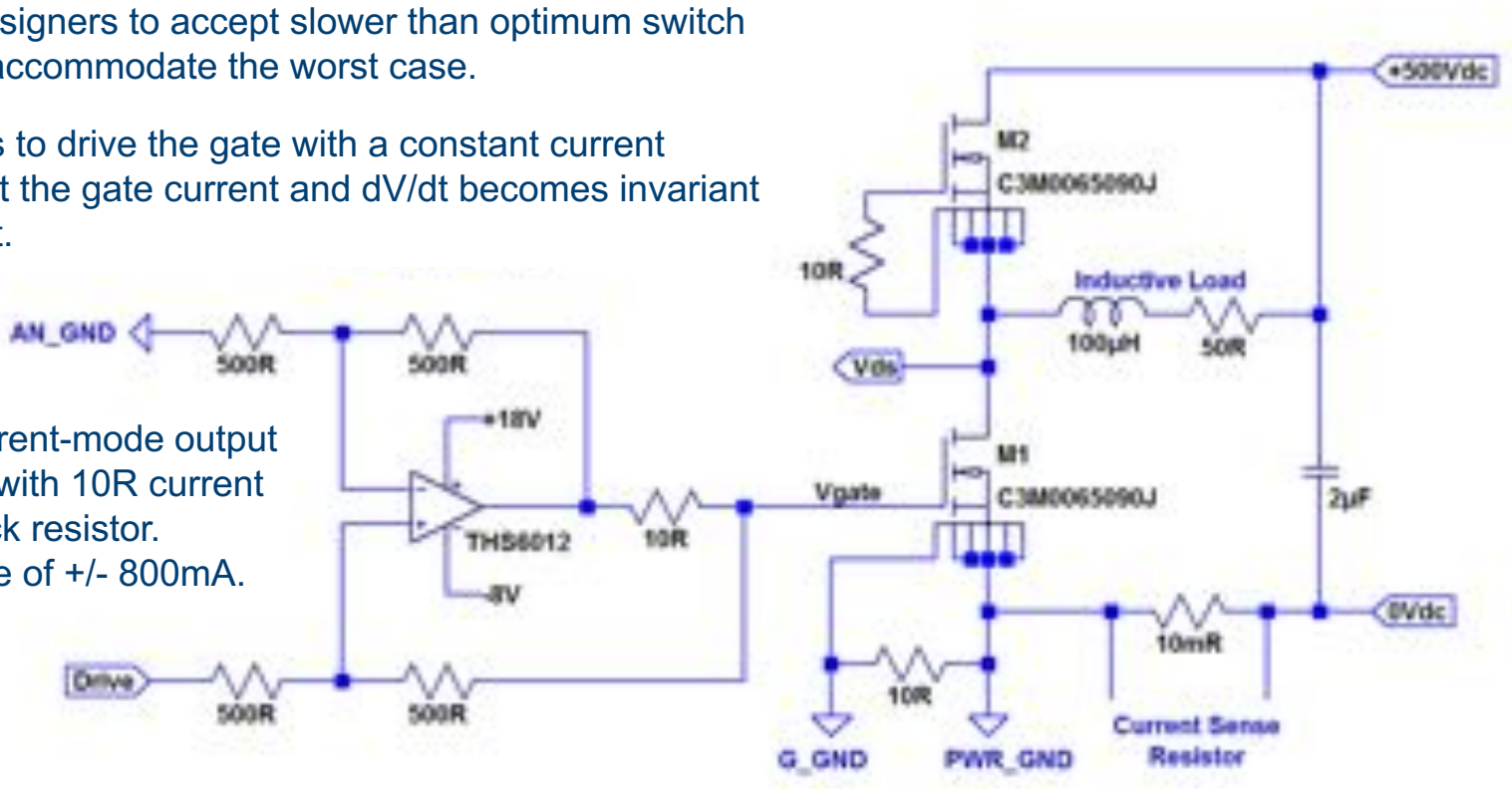
- Double-pulse test circuit, using a single WBG switch device and SiC Schottky ‘catch’ diode.
- 1200V 25A switching capability.
- Can accommodate various devices and package outlines.
- A conventional PCB construction, with local SMD DC-bus decoupling capacitors.
- Controlled current-source gate drive can provide different current waveform profiles.
- Embedded measurement circuits looking at three parameters:

  Vds, Is, Vgs

  Embedded current measurement has low insertion resistance and inductance.

Gate-drive Circuit

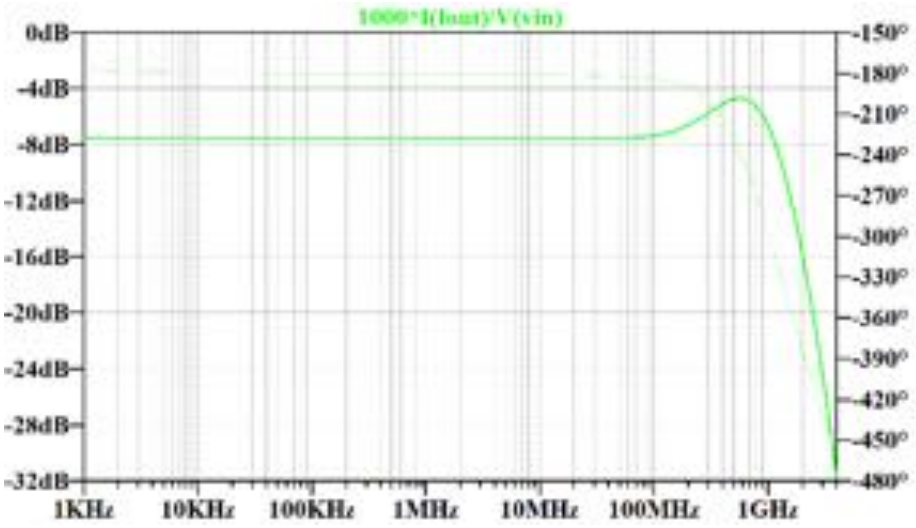
- Conventional resistive gate drive: ‘Miller plateau’ Vg varies with load current, so gate current and therefore dV/dt is dependent on load.
- This forces designers to accept slower than optimum switch slew rates to accommodate the worst case.
- The solution is to drive the gate with a constant current source, so that the gate current and dV/dt becomes invariant of load current.
- Op-amp in current-mode output configuration, with 10R current sense feedback resistor. Output capable of +/- 800mA.



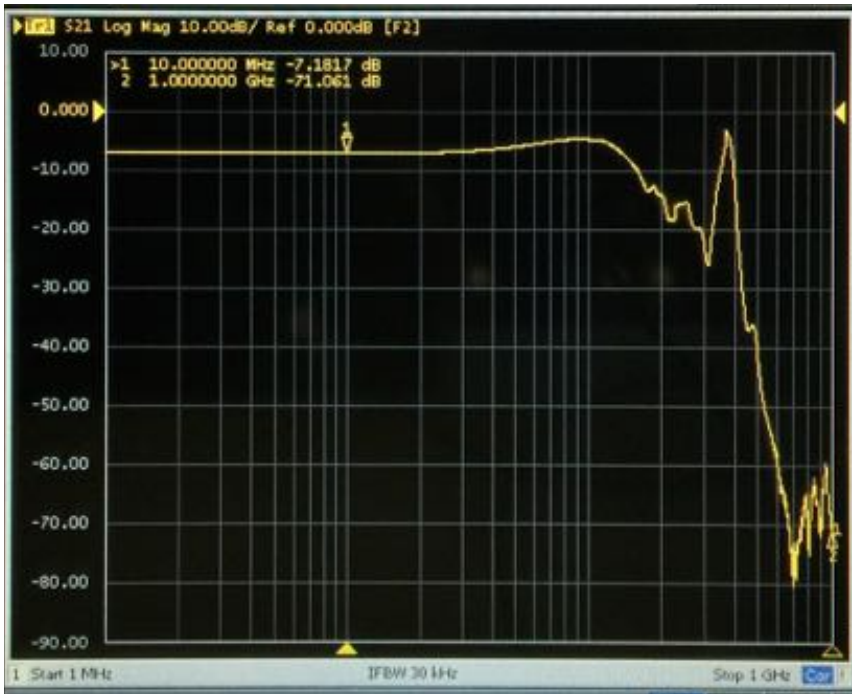
Gate-drive Circuit

- Gate drive test results demonstrate a 200MHz bandwidth and therefore a fast response.
- This will enable profiled current gate driving and feedback control for future experiments.

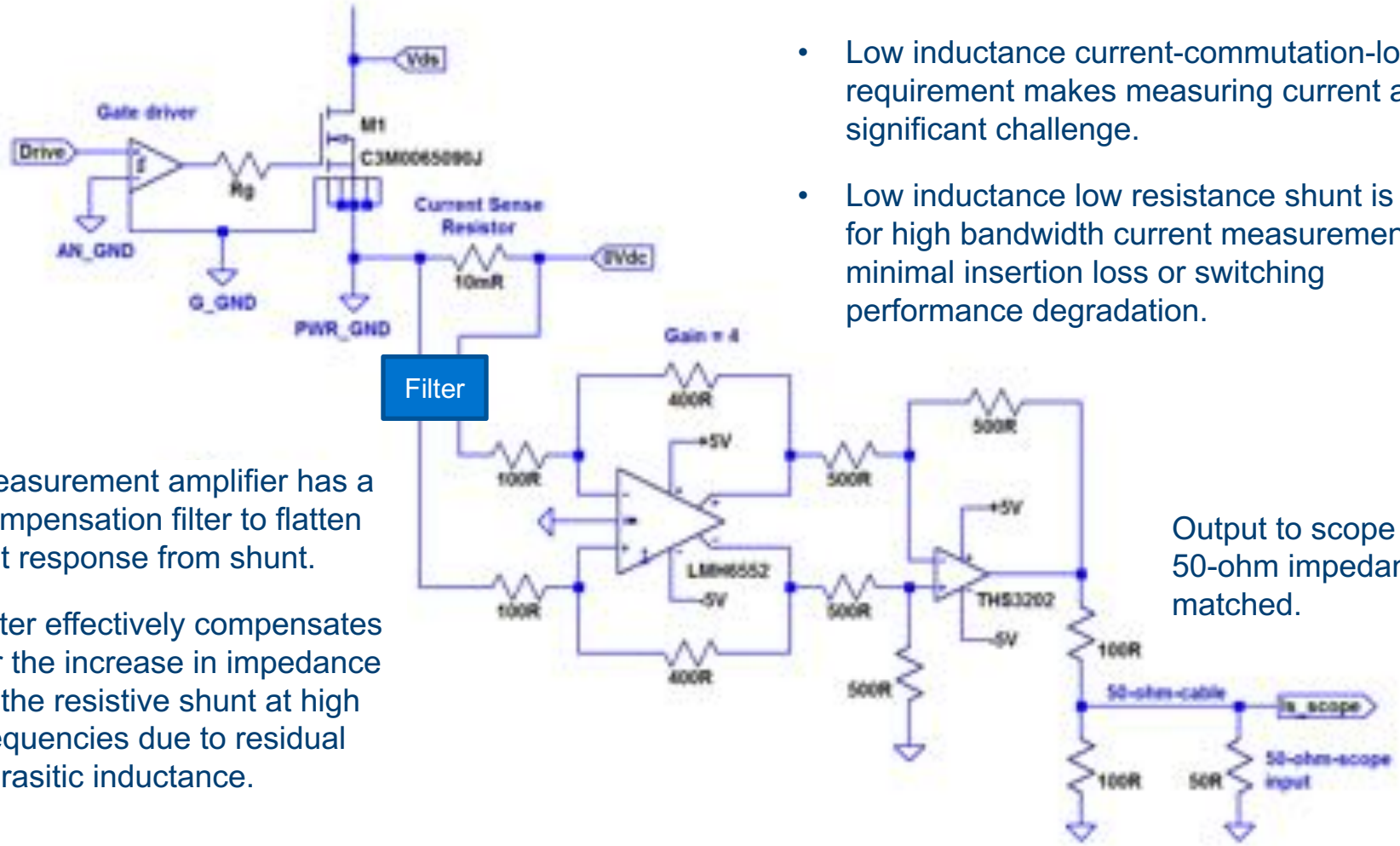
Simulation result of gate-drive circuit



Gate-drive test with VNA 1MHz-1GHz



Current Measurement Circuit



- Low inductance current-commutation-loop requirement makes measuring current a significant challenge.
- Low inductance low resistance shunt is used for high bandwidth current measurement, with minimal insertion loss or switching performance degradation.

- Measurement amplifier has a compensation filter to flatten out response from shunt.
- Filter effectively compensates for the increase in impedance of the resistive shunt at high frequencies due to residual parasitic inductance.

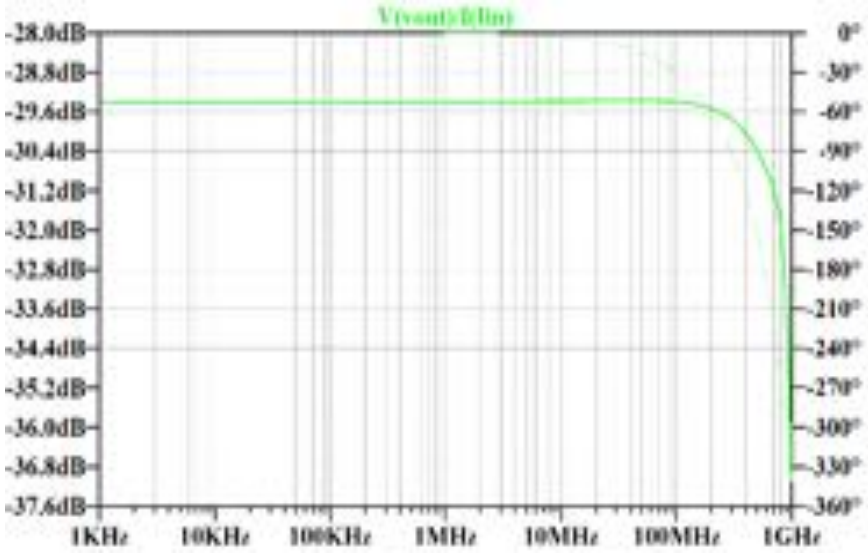
Output to scope is 50-ohm impedance matched.

Current Measurement Circuit

- Network analyzer (small signal) test results demonstrate a 200MHz bandwidth.
- This gives accurate current measurement for fast switching power circuits with high di/dt.

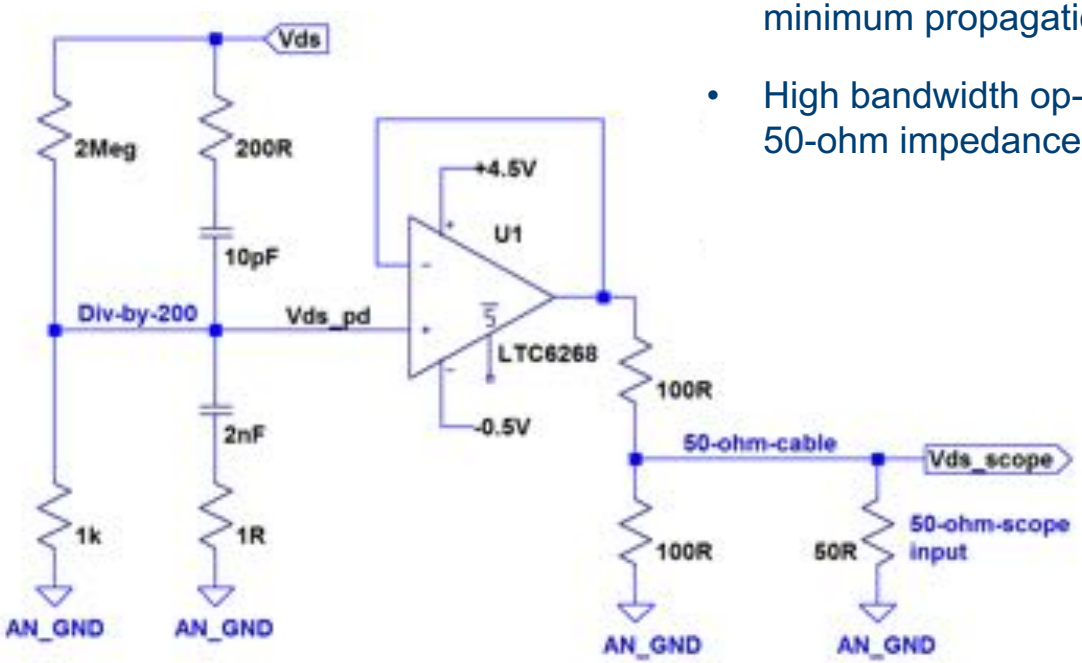
High bandwidth for feedback control in current limit circuit, to be tested in a future experiment.

LT Spice simulation result of I_S measurement



I_S test on VNA 1MHz-1GHz

V_{DS} Measurement Circuit

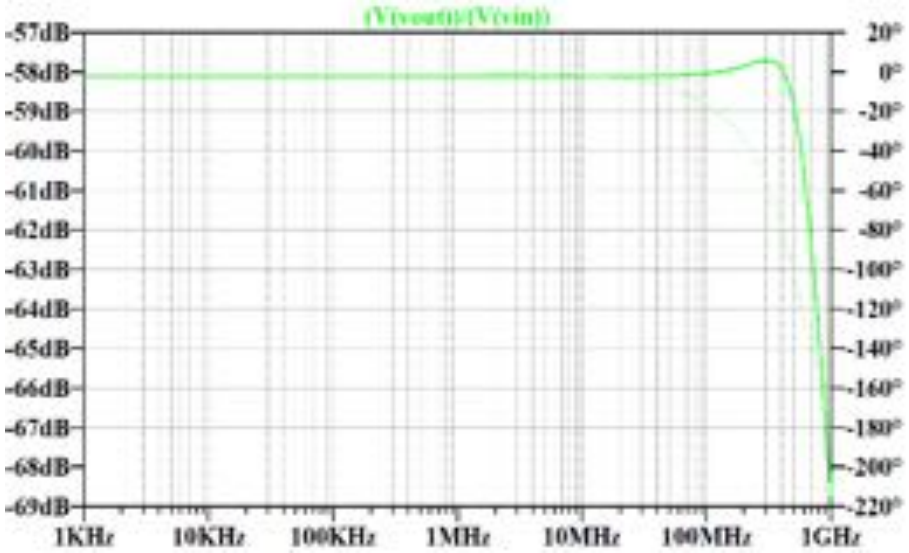


- High bandwidth necessary to capture fast slew rates and high-frequency overshoot ringing.
- Vds measurement uses resistor-capacitor array to achieve high bandwidth and high precision with minimum propagation delay and low EMI pick up.
- High bandwidth op-amp buffers signal and provides 50-ohm impedance-matched output to scope.

V_{DS} Measurement Circuit

- Test results on network analyser (right) show minimal out-of-band peaking and agrees well with Spice simulation results (left).
- Checked using a precision high voltage scope probe.

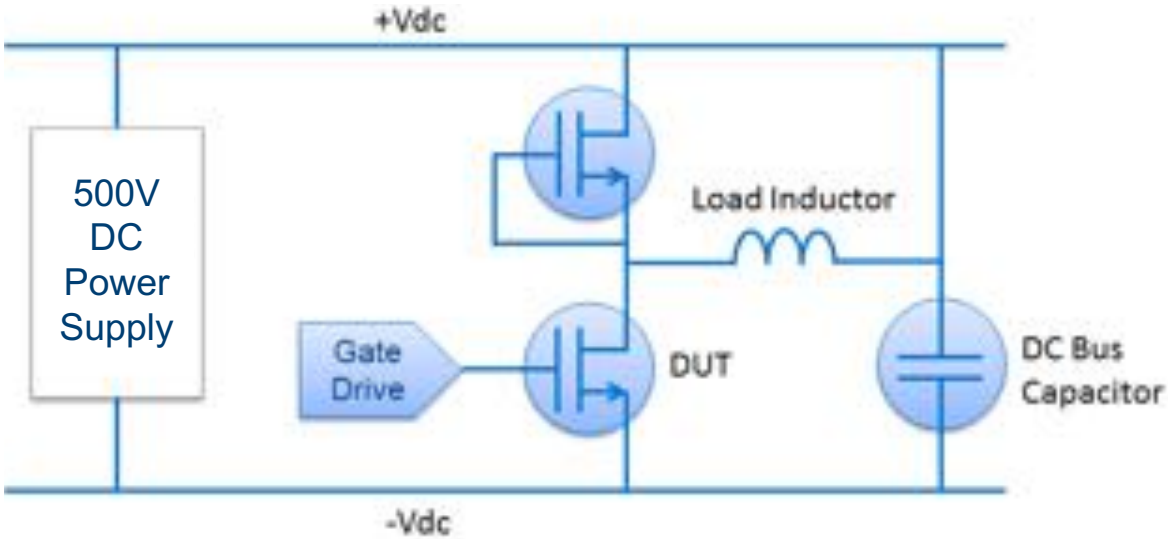
Simulation result of V_{DS} measurement

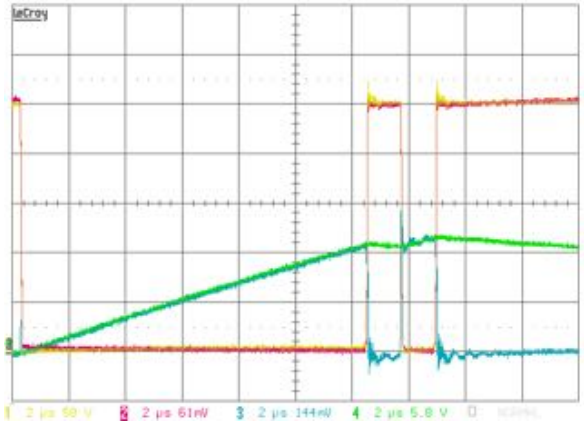


High bandwidth for feedback control in voltage clamping circuit, to be tested in a future experiment.

V_{DS} test with VNA 1MHz-1GHz

Double pulse test setup

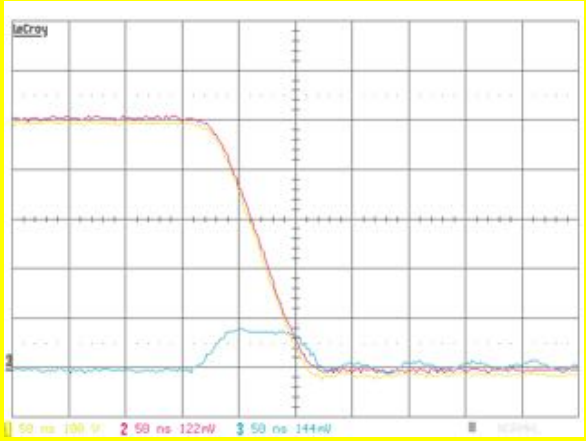




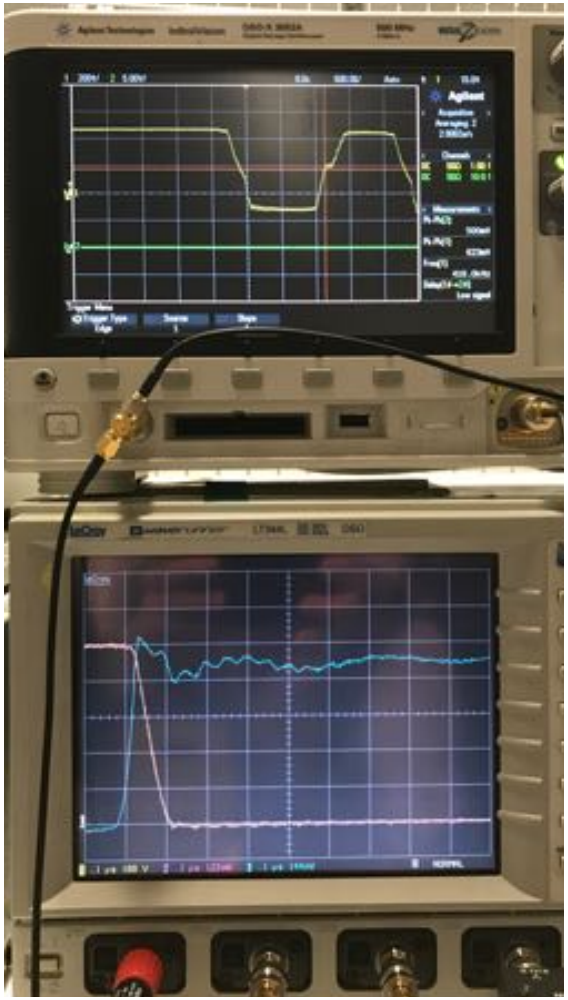
Double pulse test cycle, showing initial current ramp followed by rapid on/off pulse to test DUT switching under full current conditions.
Calibration of on-board current measurement circuit (Ch.3 blue) against an Agilent hall-effect current probe (Ch.4 green).

Cout Discharge Spike

Switching at zero load current: Ch.3 (blue) shows switch node capacitance discharge current during dV/dt region at switch-ON.



Switching Results



Top traces (left and right)

Yellow: Gate voltage on lower FET.

Bottom left traces

Switch-ON waveform.

Red: Embedded V_{ds} measurement.

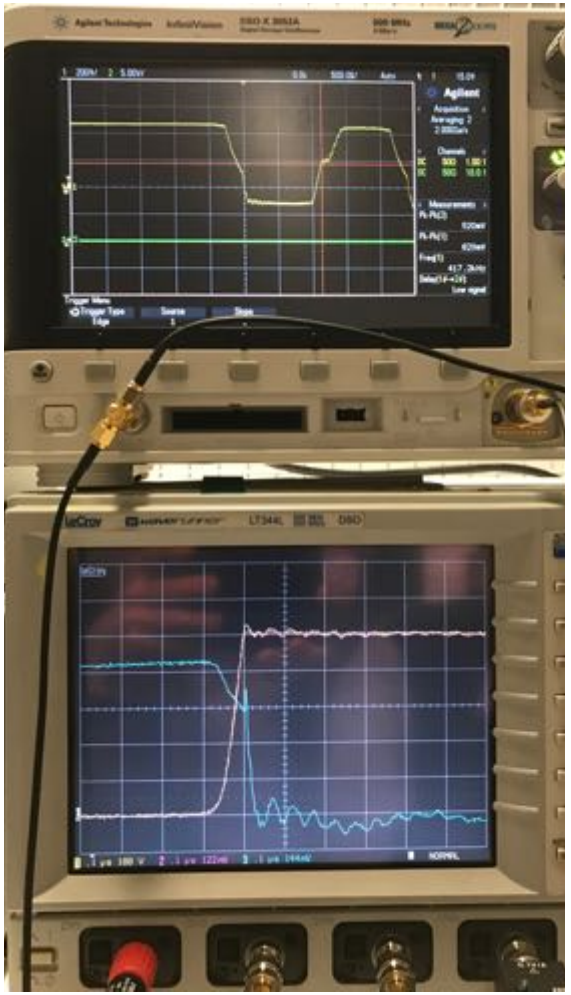
Yellow: Probe V_{ds} measurement.

Blue: Embedded I_e measurement.

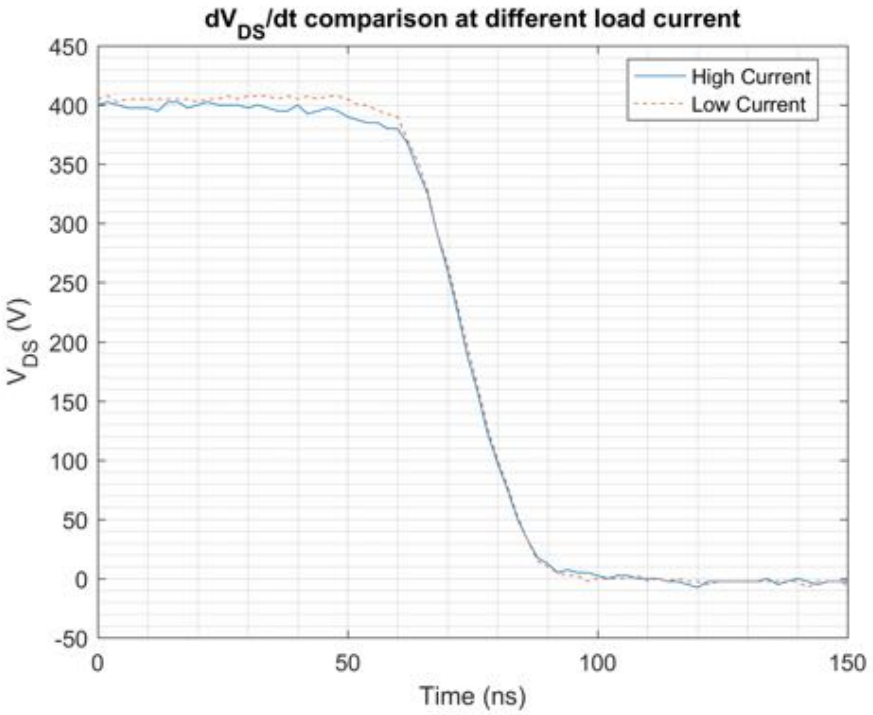
Bottom right traces

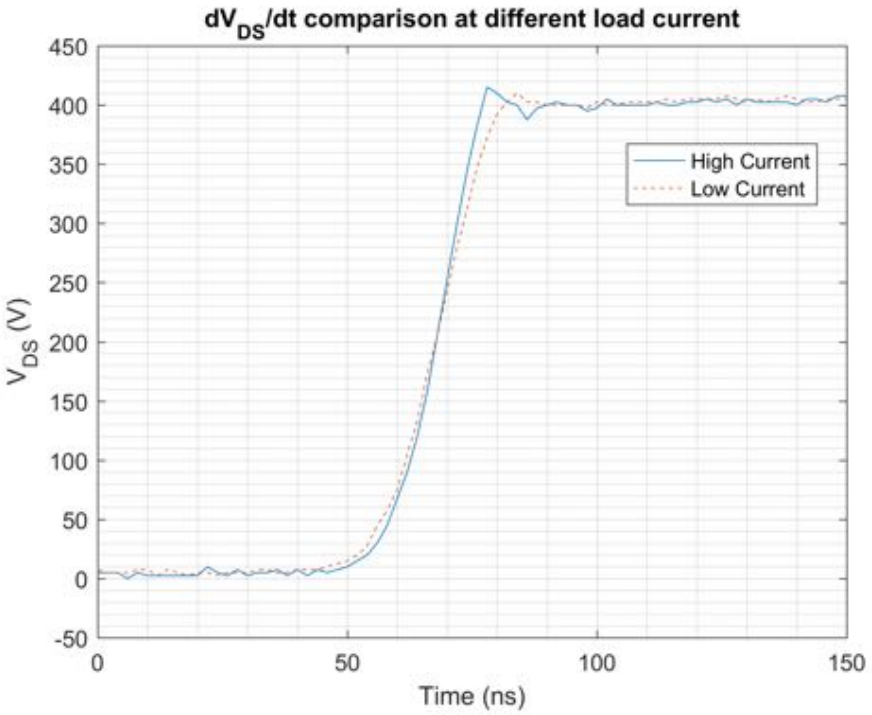
Switch-OFF waveform.

- Trace colours as before.
- Probe & embedded V_{ds} coincide.



Variation in dV/dt with Load Current





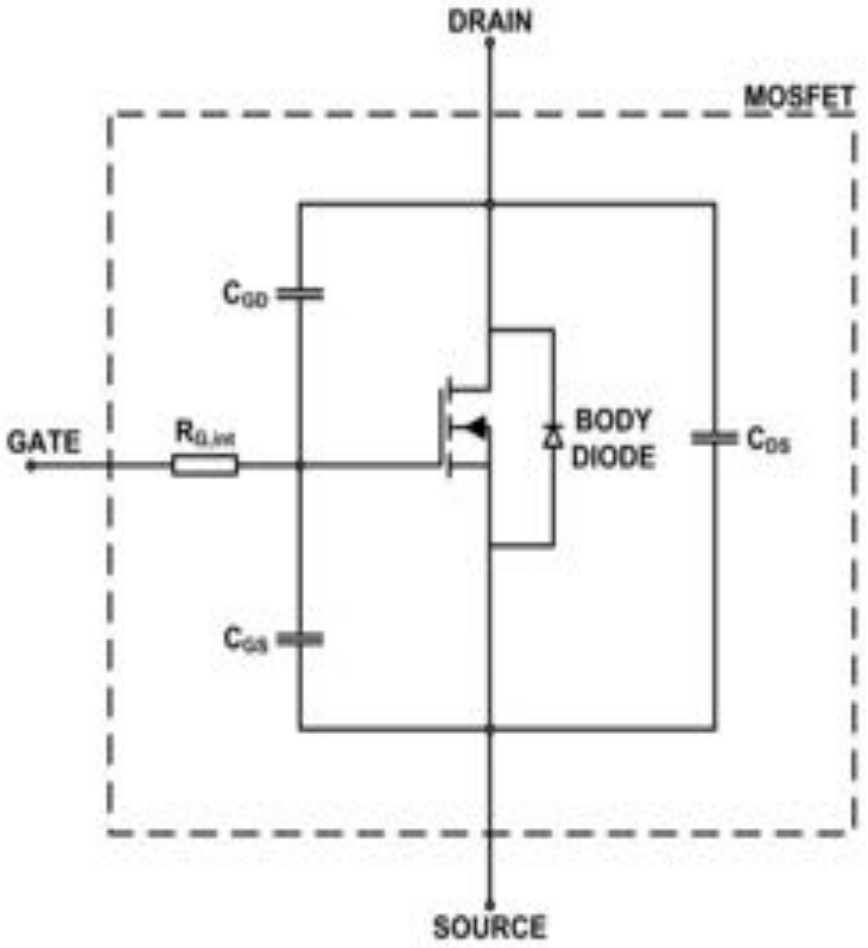
- Measure of dV/dt at constant gate drive current but at two different load currents.
- High current is 18 Amps, Low current is 9 Amps.
- dV/dt found to be invariant of load current with current-mode gate drive.

Section 4

Four-way Showdown:
GaN vs. SiC vs. CoolMOS vs. IGBT

Switching MOSFETs and IGBTs

- MOSFETs and IGBTs have internal capacitances related to their structure.
- These play an important part in the internal switching mechanism.
- IGBTs also have a charge plasma to set up and remove as a result of their bipolar structure.
- Packaging and circuit board layout parasitic inductances also play an important role in determining switching characteristics.
- Conventional MOSFETs and IGBTs have been used for 20+ years and this experience is embodied in typical circuit designs.



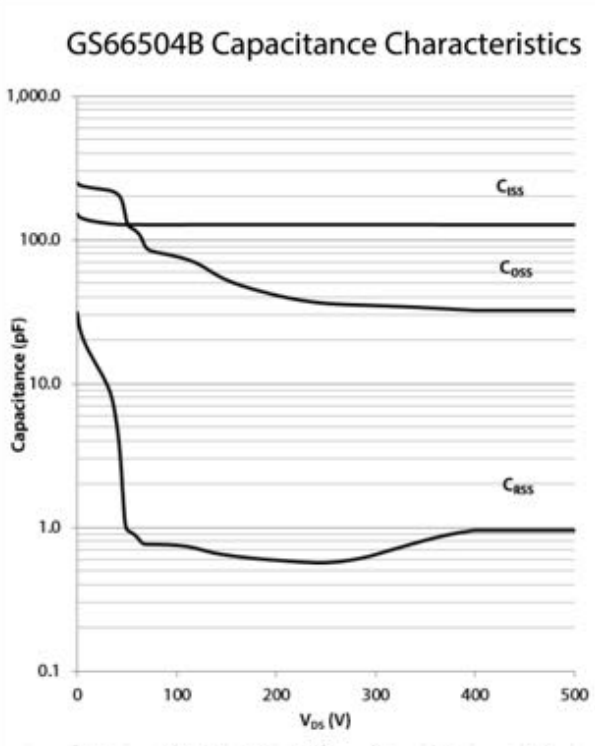
Comparison of Switching Devices

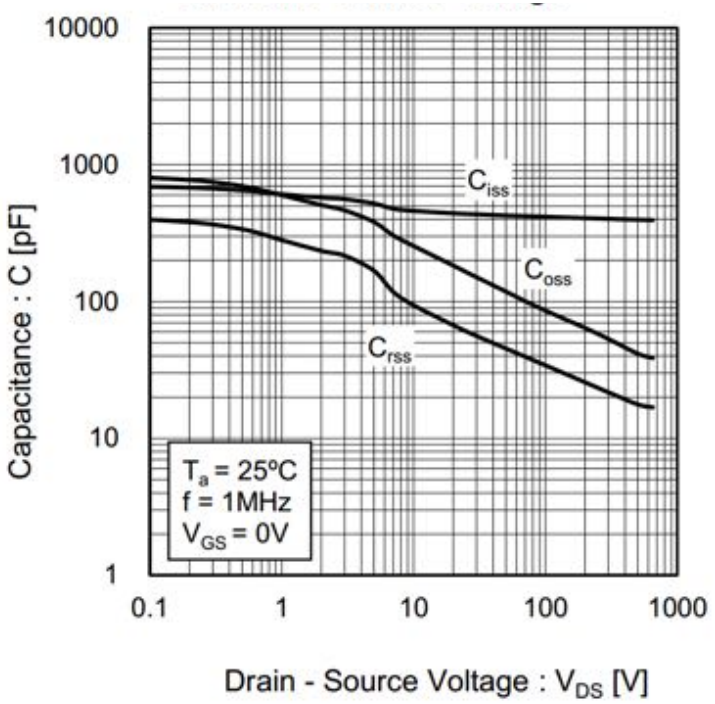
GAN TRANSISTORS VERSUS SIC MOSFET VERSUS SI SUPERJUNCTION MOSFET AND IGBT (T_C=25°C UNLESS SPECIFIED OTHERWISE)					
Type	GaN Transistors		SiC MOSFET	Si SJ MOSFET	Si IGBT
Brand	Panasonic	GaN Systems	Rohm	Infineon	Infineon
Part	PGA26C09	GS66504B	SCT3120AL	IPW65R125C7	IKP08N65F5
Voltage	600V	650V	650V	700V	650V
Current	15A	15A	21A	18A	18A
$R_{DS(on)}$	100mΩ	120mΩ	120mΩ	111mΩ	133mΩ *
Gate Voltage	+4.5V, -10V	+7V, -10V	+22V, -4V	+20V, -20V	+20V, -20V
Transconductance	-	12S *	2.7S	14S *	17S
Input Capacitance	272pF [a]	130pF	460pF [a]	1670pF	500pF [a]
Output Capacitance (Effective)	80pF [a]	44pF	70pF [a]	53pF	Large
Reverse Transfer Capacitance	32pF [a]	1pF	16pF [a]	52pF *	3pF [a]
Gate Drain Charge	5.5nC	0.84nC	13nC	11nC	-
Test	400V	400V	300V, R_G=0Ω	400V, R_G=10Ω,	400V, R_G=48Ω

* Estimated from the datasheet, [a] Under different test conditions

Capacitance Curves: GaN HEMT and SiC MOSFET

Similar behaviour between GaN and SiC, but the capacitance magnitudes are vastly different.

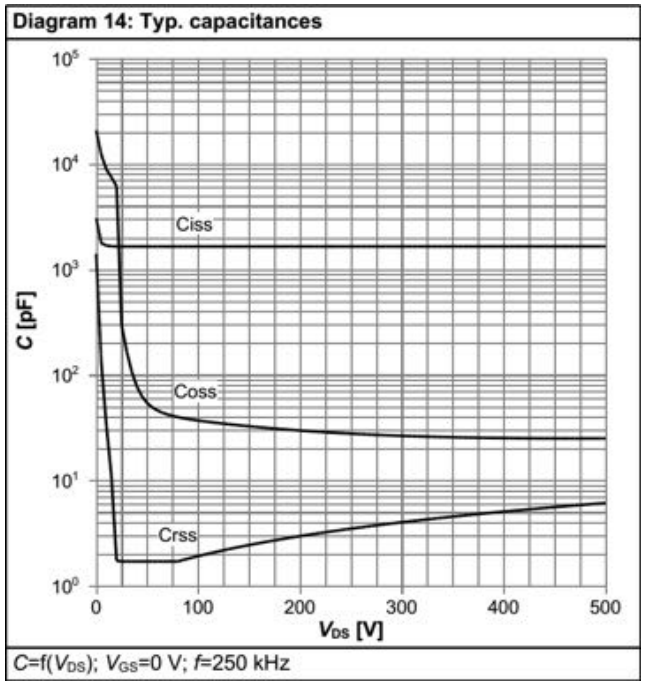




The SiC MOSFET capacitances can contribute to significant ringing.

Capacitance Curves Si SJ MOSFET and Si IGBT

Very rapid drop off with voltage



The SJ MOSFET has 2D fields in the bulk.

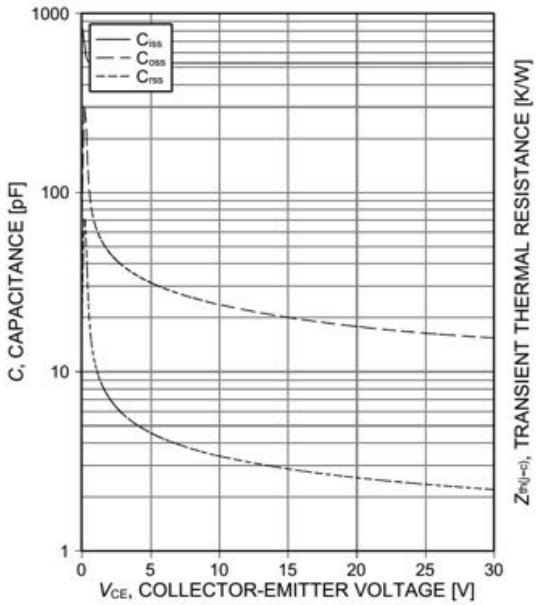


Figure 17. **Typical capacitance as a function of collector-emitter voltage** (V_{GE}=0V, f=1MHz)

The IGBT also has stored charge increasing the output and Miller capacitances at turn off.

Comparison of Switching Devices

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$R_{DS(on)}$	100mΩ	100mΩ	120mΩ	111mΩ	133mΩ *
Gate Voltage	+4.5V, -10V	+7V, -10V	+22V, -4V	+20V, -20V	+20V, -20V
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Input Capacitance	272pF [a]	130pF	460pF [a]	1670pF	500pF [a]
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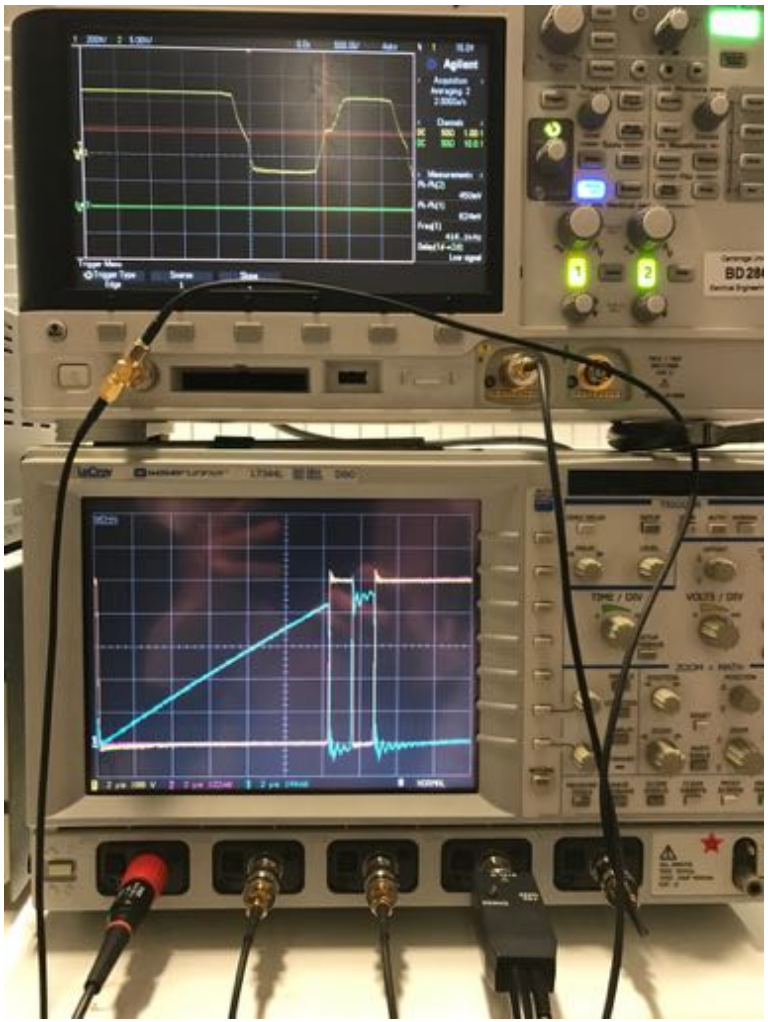
Gate Drain Charge	5.5nC	**0.84nC**	13nC	11nC	-
Test	400V	400V	300V, R_G=0Ω	400V, R_G=10Ω,	400V, R_G=48Ω

* Estimated from the datasheet, [a] Under different test conditions

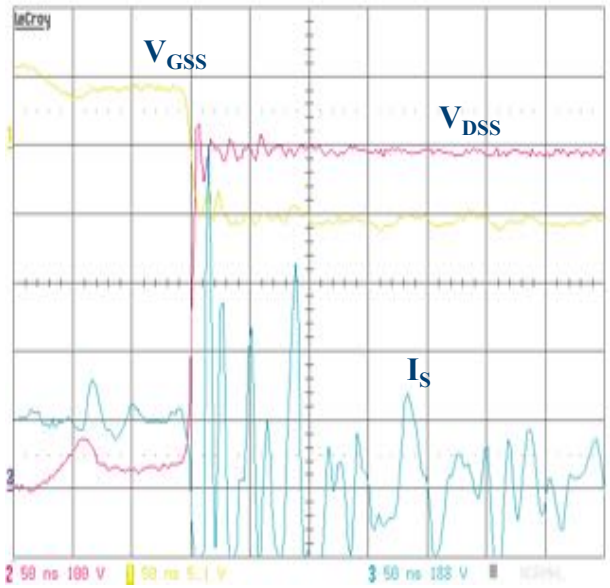
WBG Development Platform: Switching Tests

- Half-bridge switched inductive load topology.
- Gate drive on lower device, with SiC catch diode.
- Double-pulse switch test at 400Vdc.
- Peak switched load current of 10A.

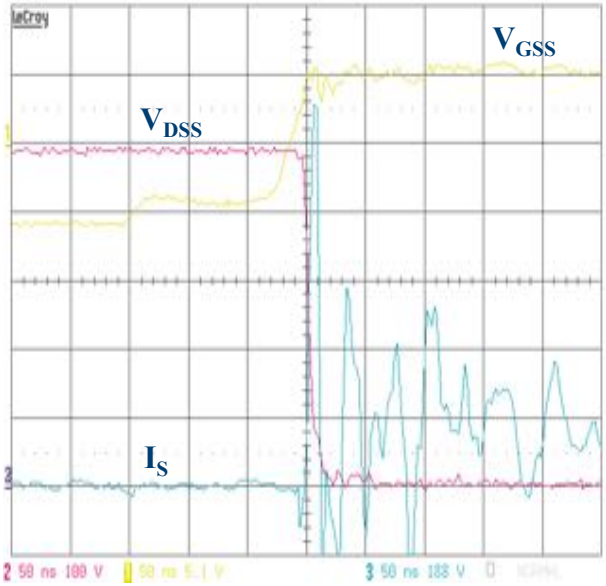


GaN Systems GS66504B Switching 500mA Gate Drive

GaN HEMT Turn-off with I_G=500mA



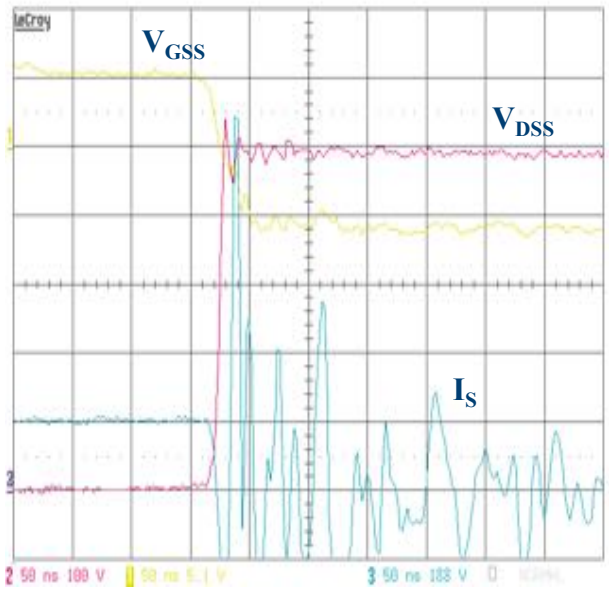
GaN HEMT Turn-on with I_G=500mA



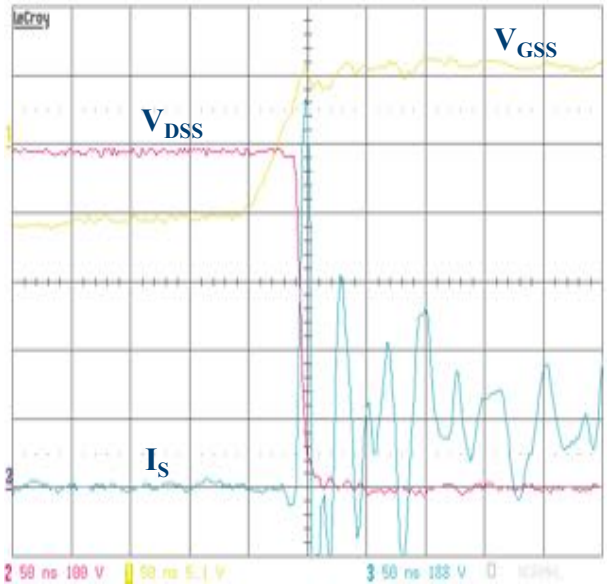
The dV/dt is around 50,000V/us, virtually no overshoot.
Current waveform contains significant ringing: For further investigation.

GaN Systems GS66504B Switching 200mA Gate Drive

GaN HEMT Turn-off with I_G=200mA



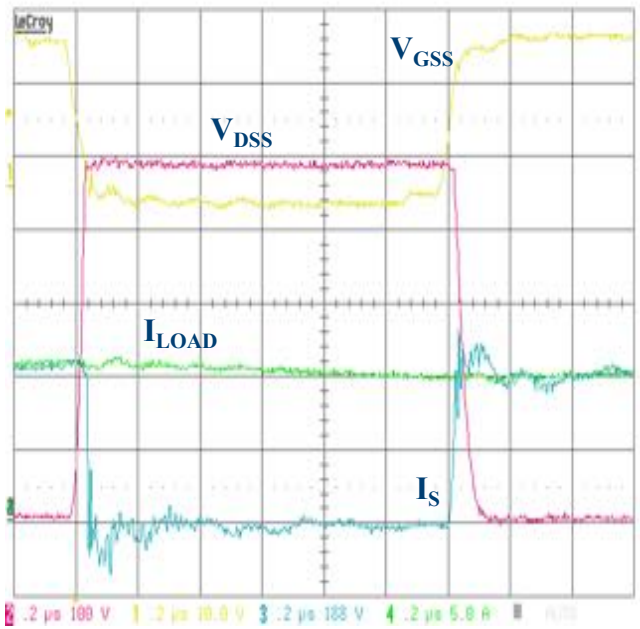
GaN HEMT Turn-on with I_G=200mA



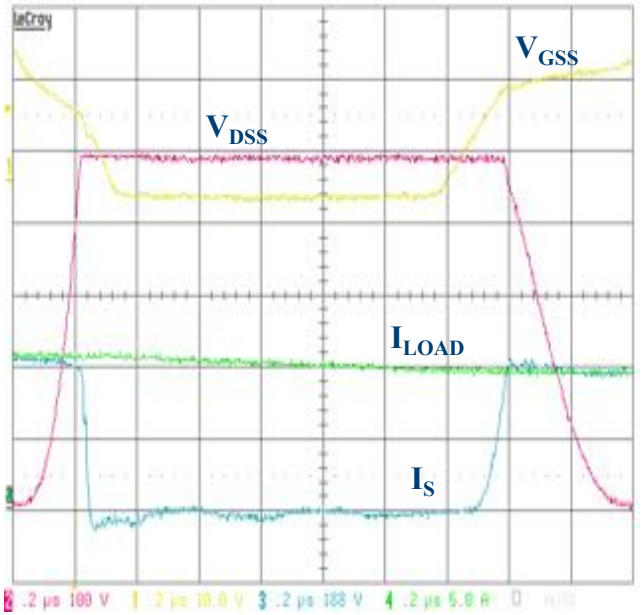
The dV/dt is a little slower and the waveforms are quite clean. Some parasitic current oscillation.

ROHM SCT3120AL SiC MOSFET

SiC MOSFET Switching
with I_G=500mA



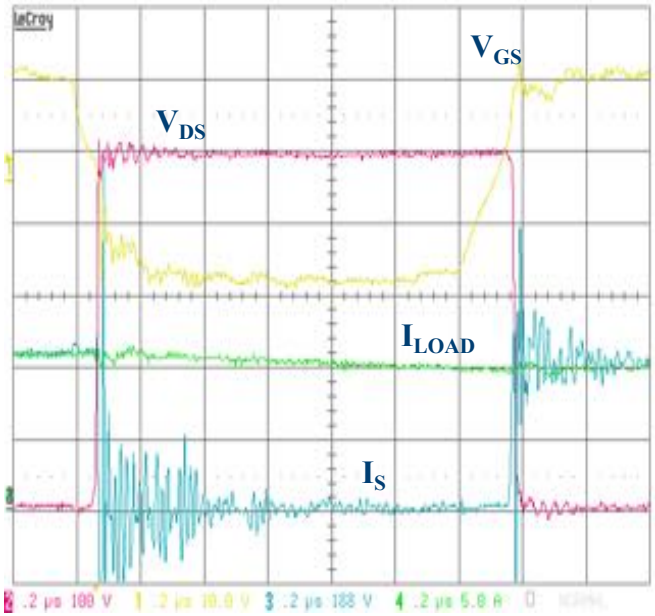
SiC MOSFET Switching
with I_G=100mA



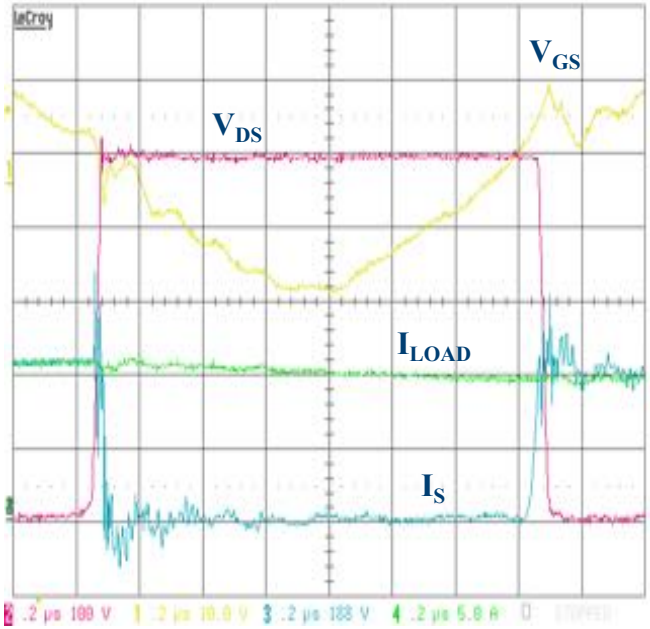
The dV/dt is around 10,000 V/us (turn-off); no overshoot, clean current.
Current measurement looking good!

Infineon IPW65R125C7 Si SJ MOSFET

Si SJ MOSFET Switching with I_G=500mA



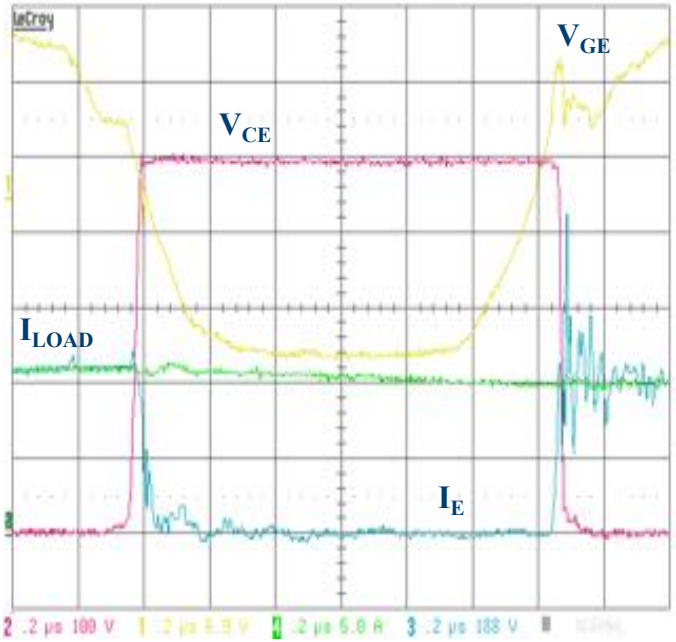
Si SJ MOSFET Switching with I_G=100mA



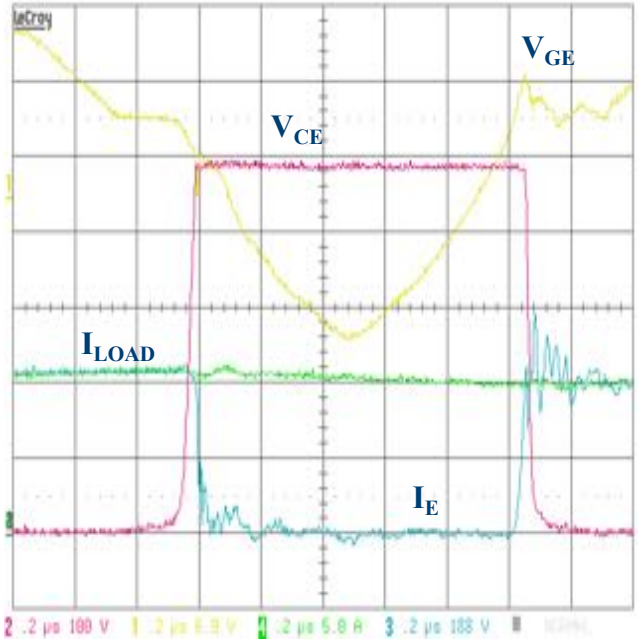
The dV/dt is around 32,000 V/us; no overshoot, clean current.
Gate current drive working hard to deliver to large Qgs required.

Infineon IKP08N65F5 Si IGBT

Si IGBT Switching with I_G=500mA

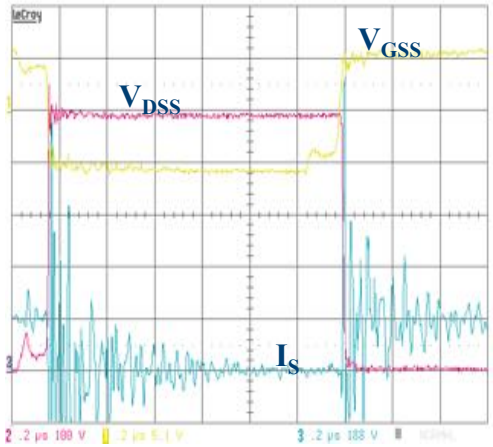


Si IGBT Switching with I_G=200mA

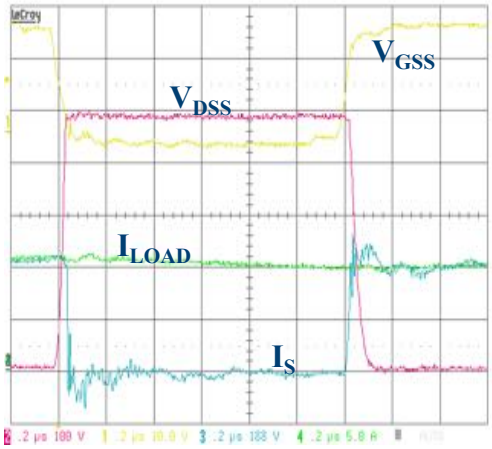


The dV/dt is around 12,000 V/us (at turn-off); no overshoot, clean current.
Gate drive working hard!

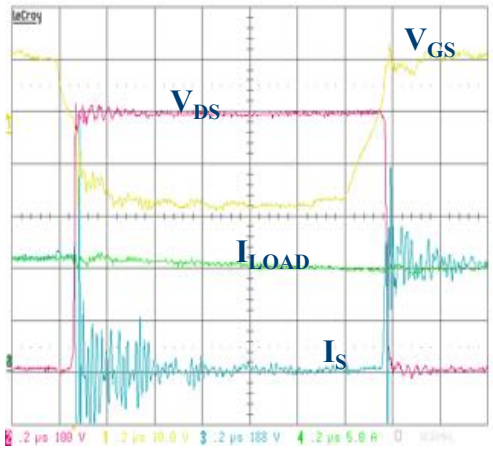
Show Down: Switching with 500mA Gate Drive



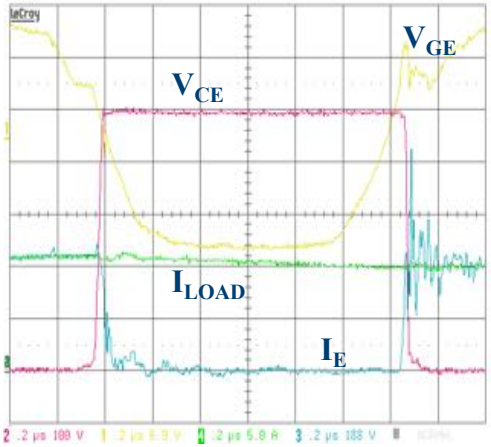
GaN HEMT



SiC MOSFET

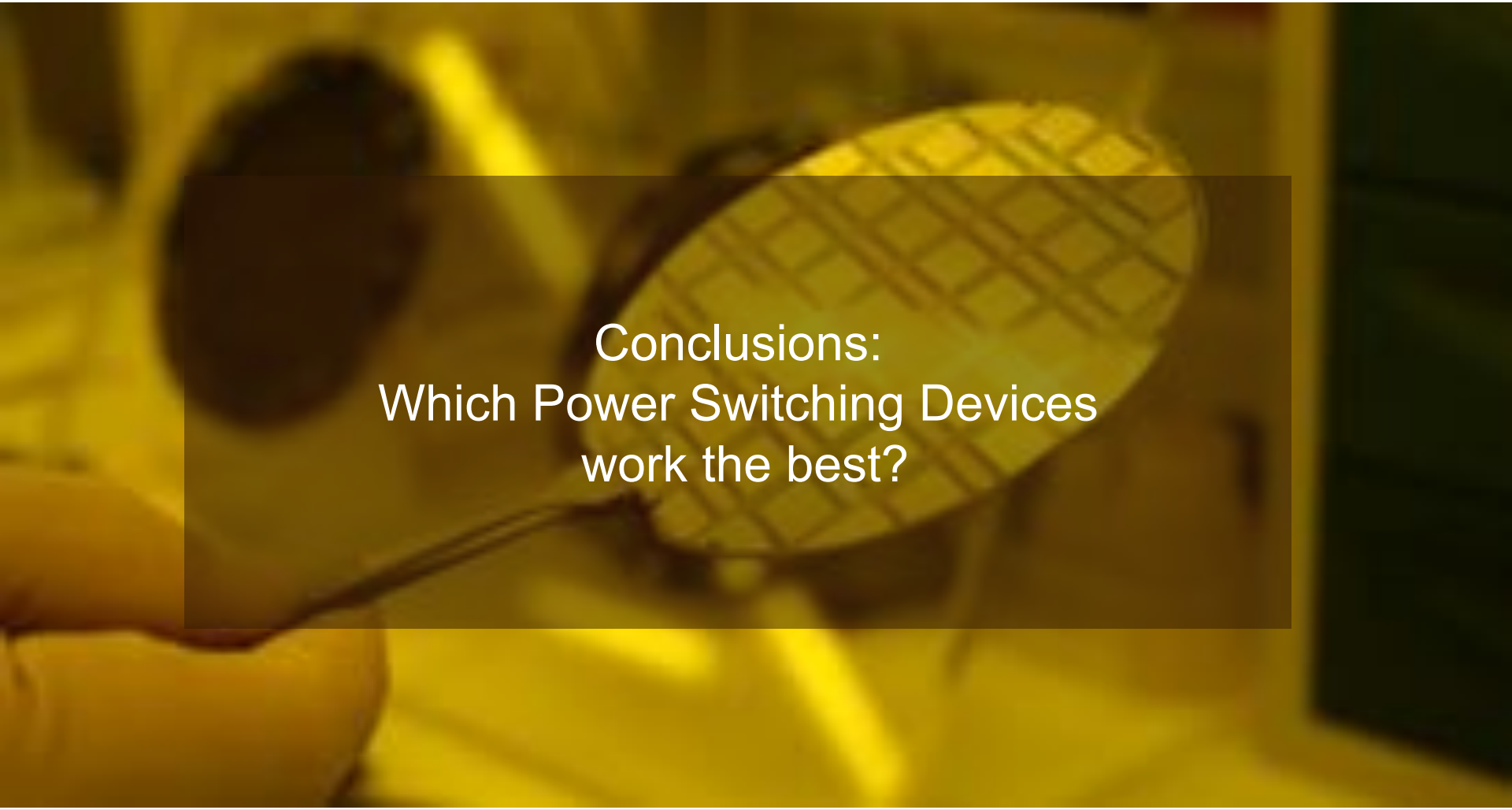


Si SJ MOSFET



Si IGBT

Section 5



Conclusions:
Which Power Switching Devices work the best?

Section 5: Conclusions

So, which switching devices offer the best performance?

- New GaN and SiC WBG devices offer a great opportunity to get low conduction losses and low switching losses in a very small footprint.
- GaN 'FET's look very attractive when compared to SiC MOSFETs at the 400V level and below: Low capacitances, low drive voltages, high gain, highly controllable.
- There are various other contenders in traditional Silicon that still offer impressive switching, such as some new IGBTs and CoolMOS devices, but they also require careful circuit design to achieve reliable circuit operation.
- However, the GaN and SiC devices do not suffer the tail current or diode reverse recovery issues of their Silicon IGBT and CoolMOS counterparts.
- Circuit behaviour can be predicted and designed for, but there are significant design, test and qualification challenges.

The final verdict: For fast switching applications below 400V, GaN is hard to beat.!!

The End

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- Jin Zhang (PhD Student)

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