Extreme Power Density Converters - Fundamental Techniques and Selected Applications

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University of Illinois Urbana-Champaign

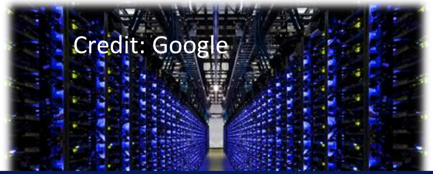
PELS Bay Area Chapter Seminar

July 13th, 2017

Acknowledgment

The Goals of Power Electronics


Credit: EWEA


Credit: Google


Credit: Samsung

Credit: Tesla

High Power Density | High Efficiency

High Performance Power Converters

High Reliability | Low Cost

Credit: AES


Credit: CAT

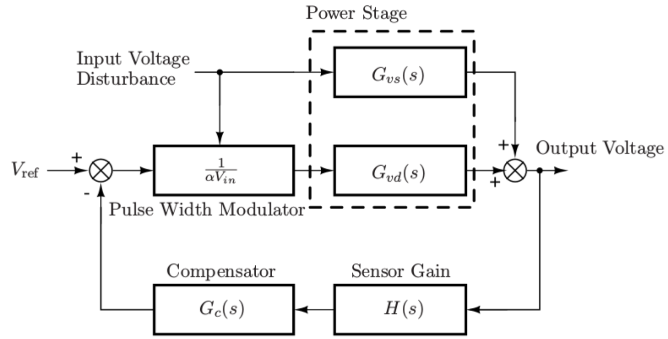
Integration of power electronics in systems for overall performance improvements

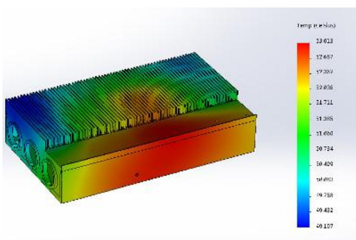

Credit: ABB

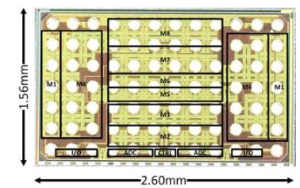

Credit: Tesla Motors

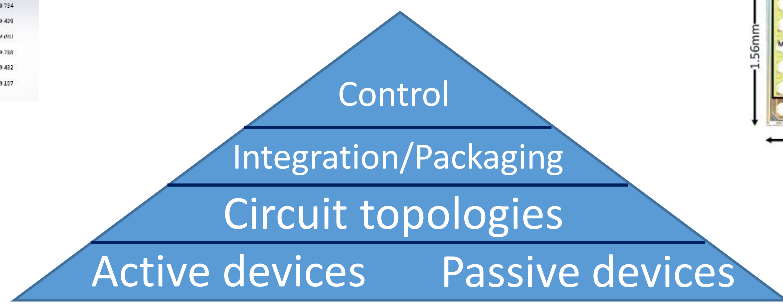

Credit: NASA/MIT/Aurora Flight Sciences

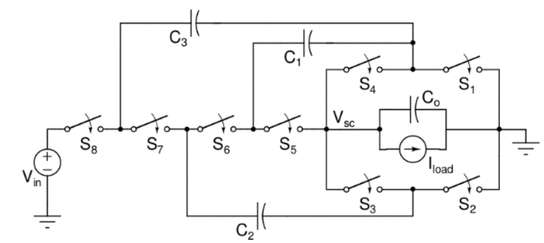
The Tools of Power Electronics

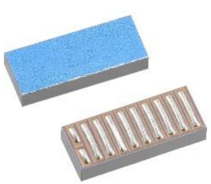




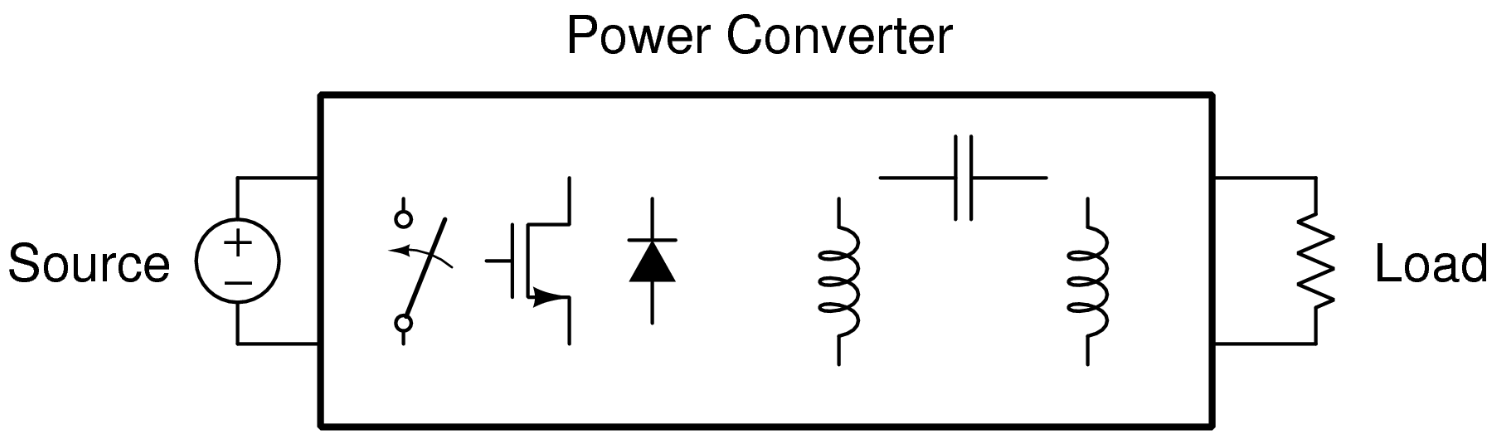


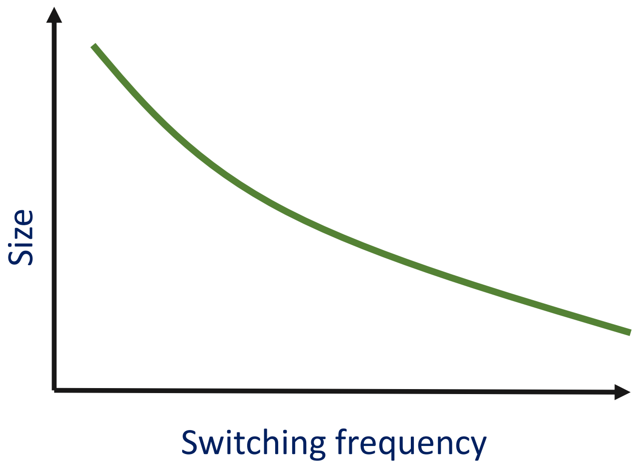


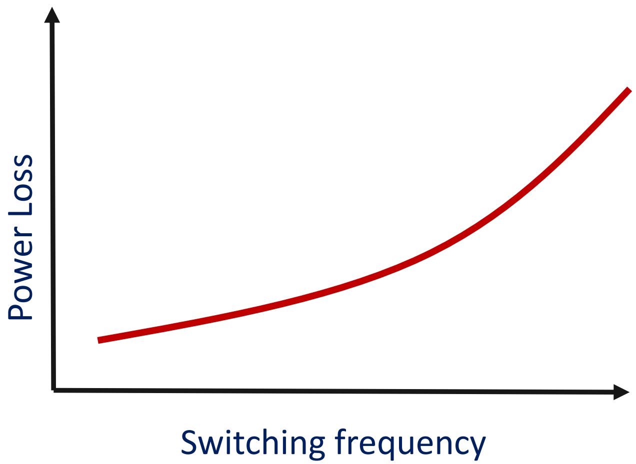




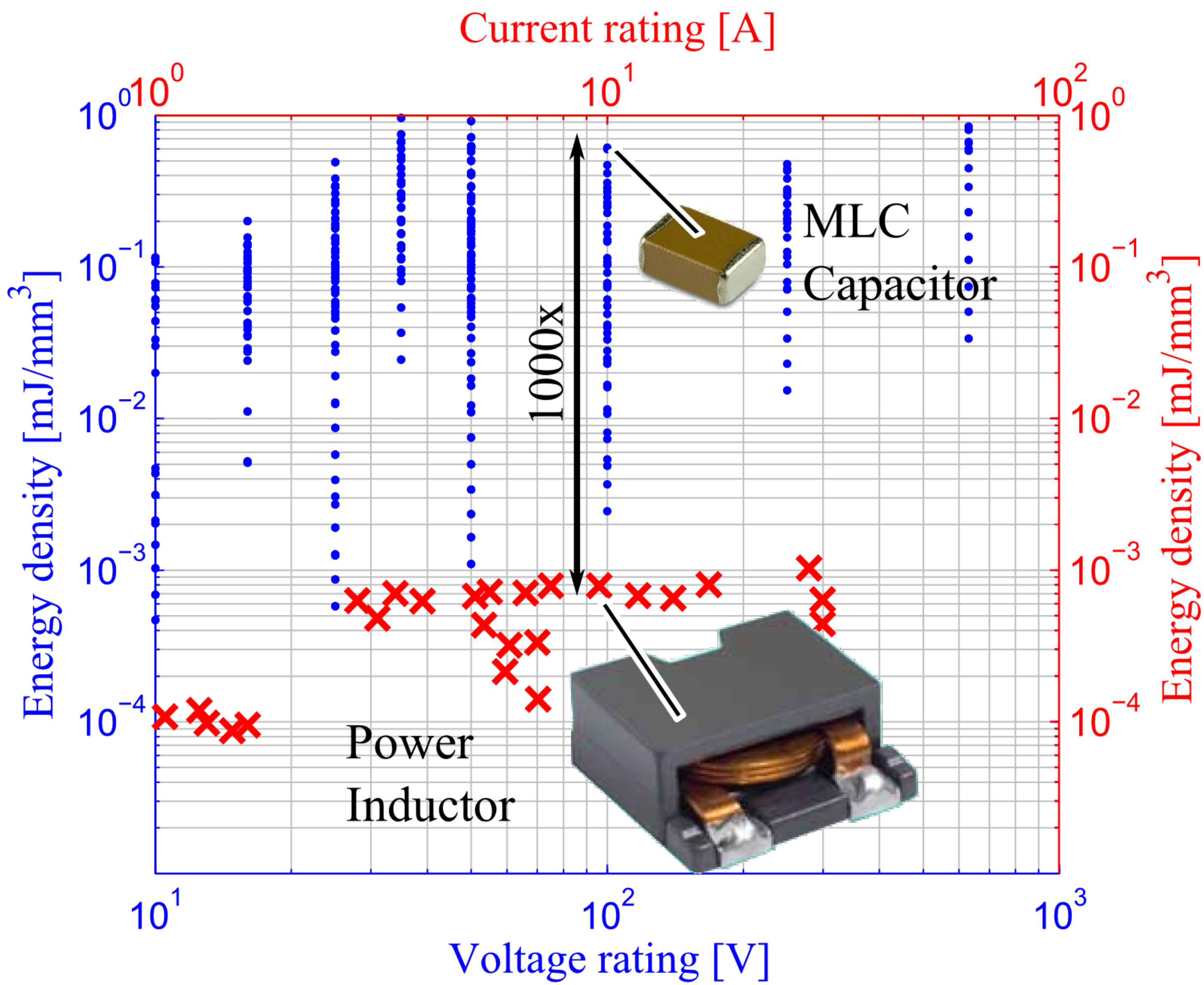
Conventional Path to High Power Density



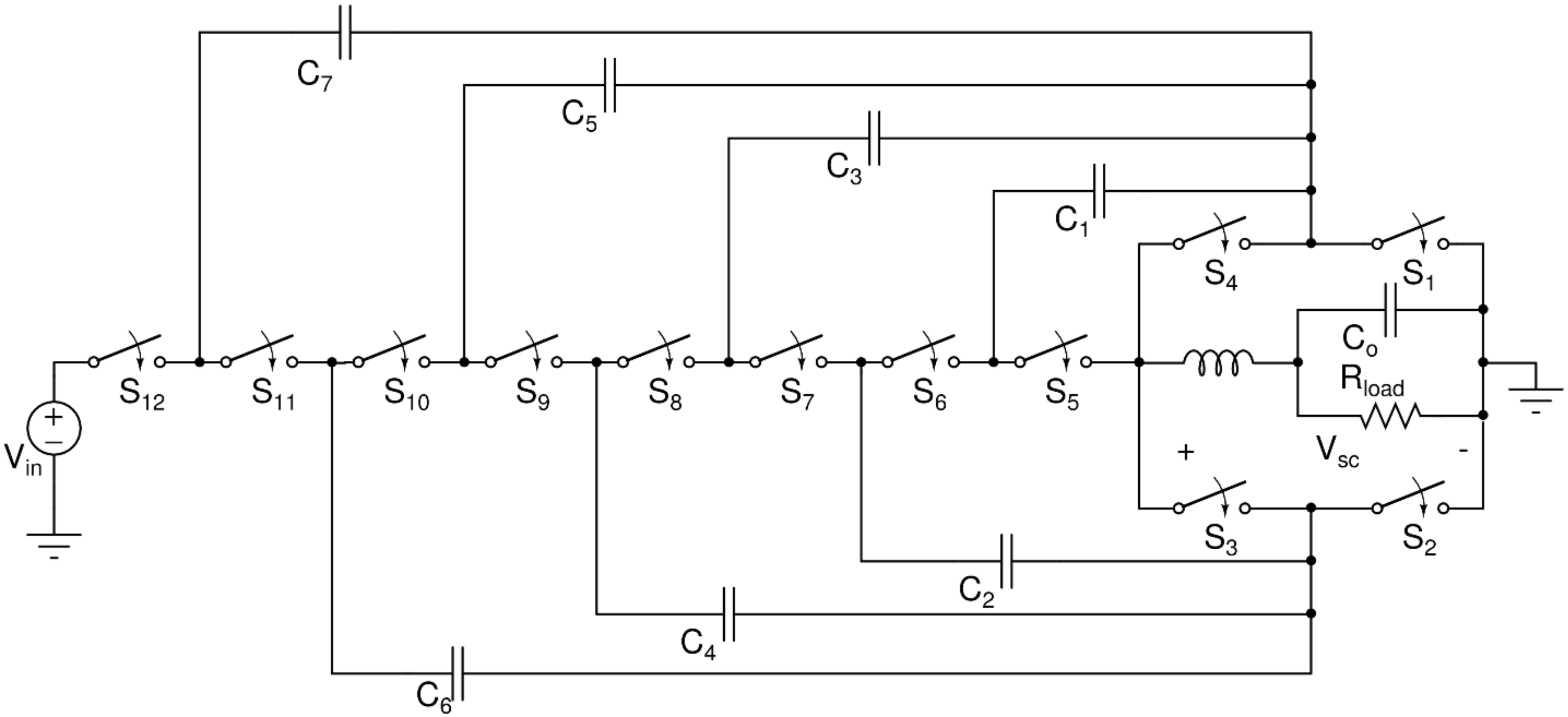




Component Choices



Hybrid Switched-Capacitor Converters

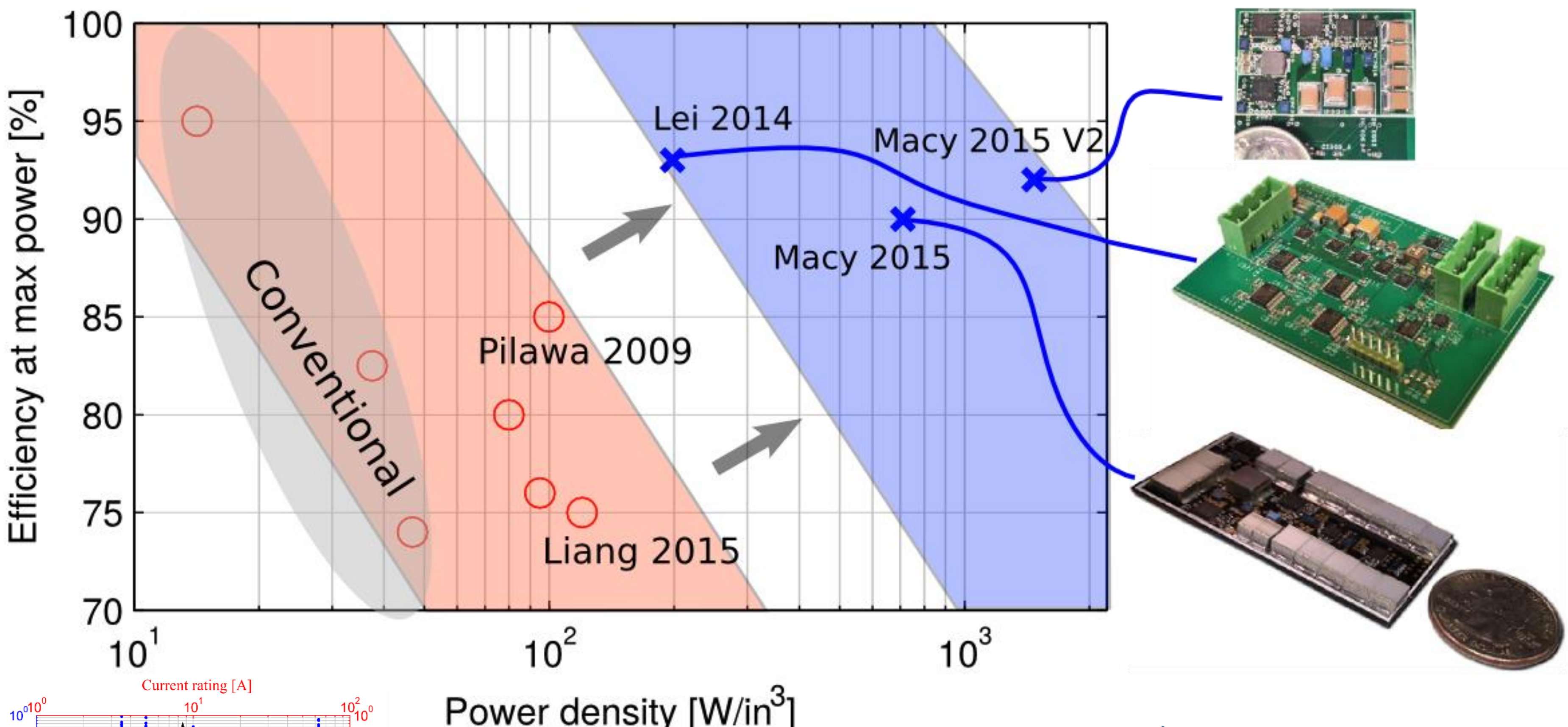


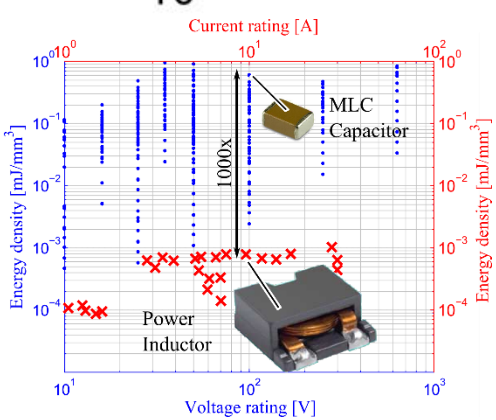
R.C.N. Pilawa-Podgurski, D.J. Perreault, “Merged Two-Stage Power Converter with Soft Charging Switched-Capacitor Stage in 180 nm CMOS,” IEEE Journal of Solid-State Circuits, Vol. 47, No 7, pp. 1557-1567, 2012

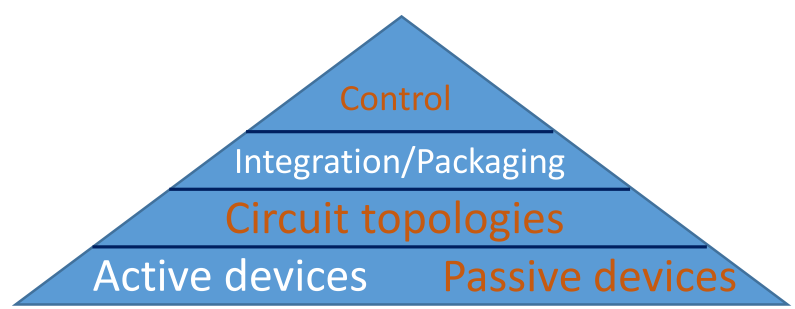
Y. Lei, R.C.N. Pilawa-Podgurski “A General Method for Analyzing Resonant and Soft-charging Operation of Switched-Capacitor Converters,” IEEE Transactions on Power Electronics, Vol. 30, No. 10, pp. 5650-5664, October 2015

Y. Lei, R. May, R.C.N. Pilawa-Podgurski, “Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter,” IEEE Transactions on Power Electronics, Vol. 31, No. 1, pp. 770-782, January 2016

Hybrid Switched-Capacitor Converters







DC-AC and AC-DC Power Conversion

The Importance of DC/AC and AC/DC

Grid Integration of Renewables and Storage

Credit: Tesla

Credit: Nissan

Power Electronics:
DC/AC & AC/DC

Credit: iStockphoto

Electric Transportation

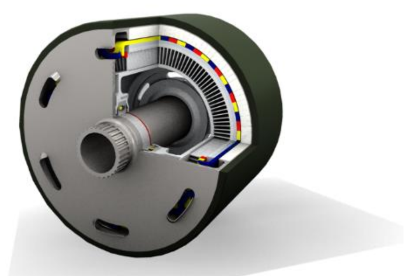
Credit: CAT

Credit: GM

Credit: NASA

Credit: Nissan

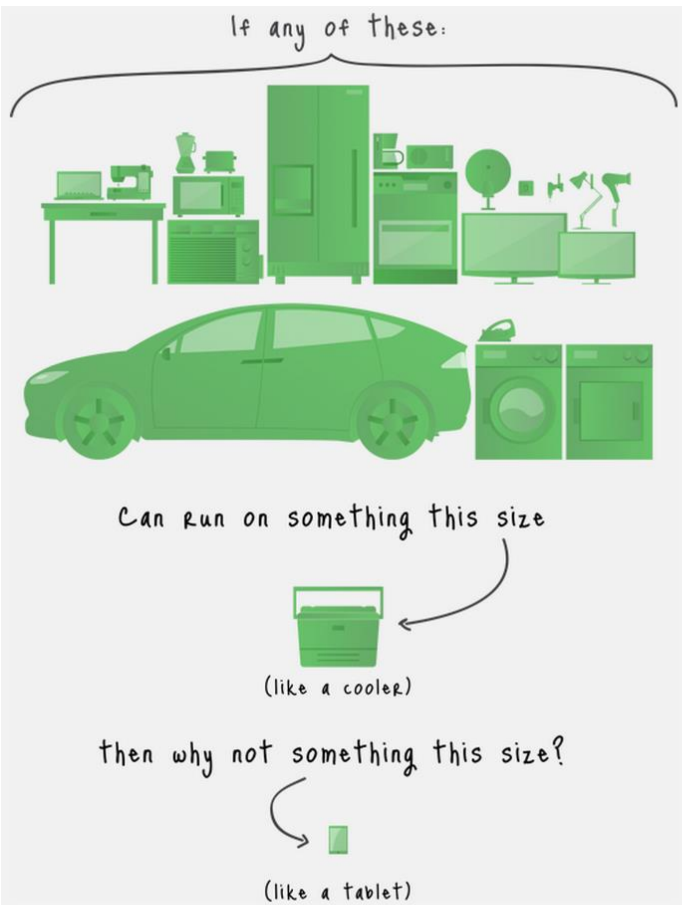
Power Electronics:
DC/AC & AC/DC



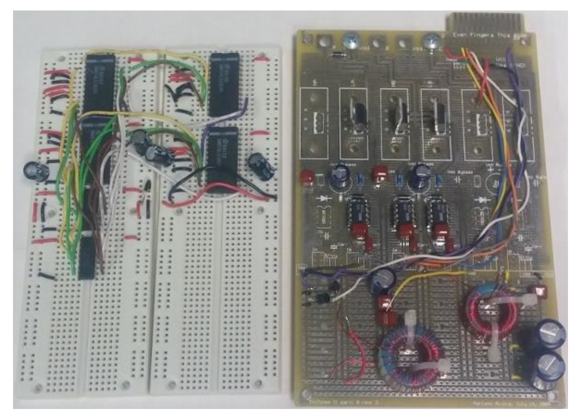
Google/IEEE $1M Little Box Challenge

LITTLE BOX CHALLENGE

Google | IEEE



- 2 kW, single-phase 240 V, 60 Hz AC
- Example usage: solar inverter, electric car charger, grid storage integration
- Current state-of-the-art: 95% efficiency, 400 in^3.
- Target goal: >95% efficiency, 10x smaller (40 in^3)
- $1M prize to winning entry

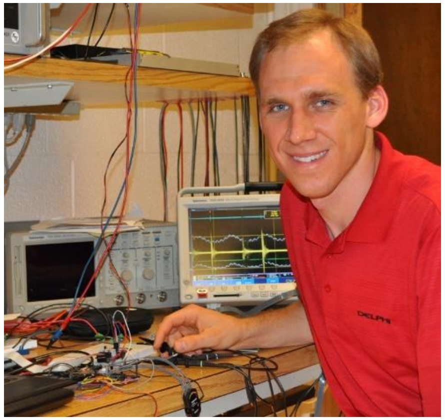


Prior (lack of!) experience

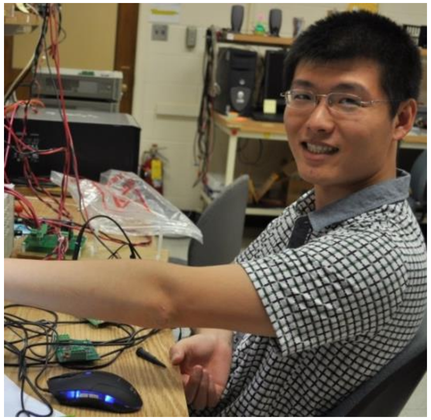
Our Goal

Develop a radically different solution – make significant research contribution to the field of power electronics. May not win competition, but will have long-term impact

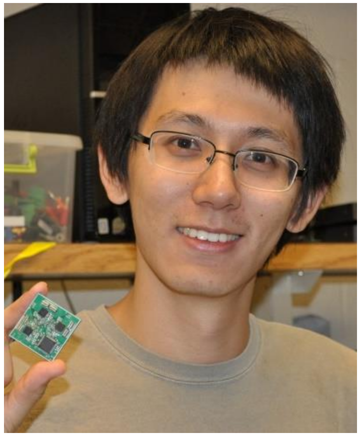
Original Team



- Chris Barth
  - Integration
  - Mechanical
  - Thermal
  - Capacitor evaluation



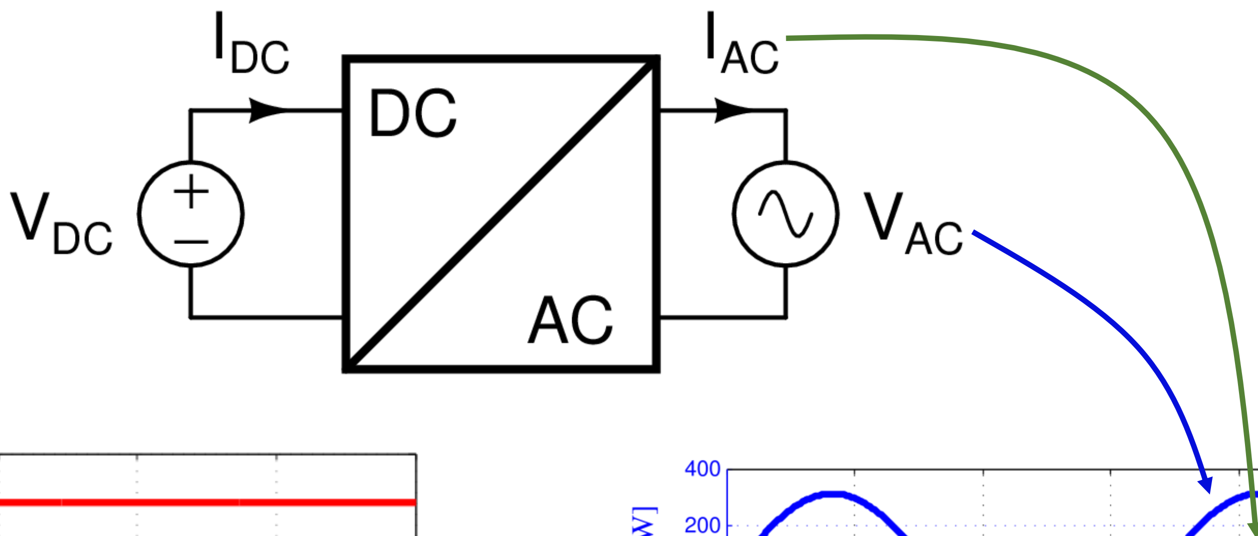
- Yutian Lei
  - Inverter design
  - Inverter control

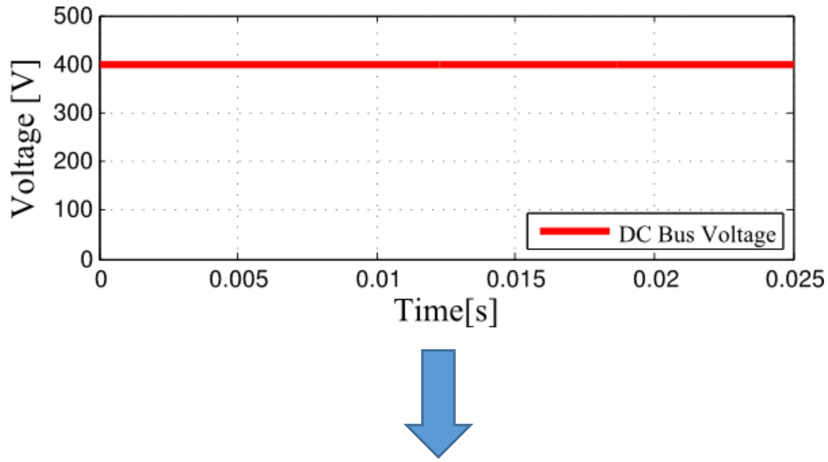


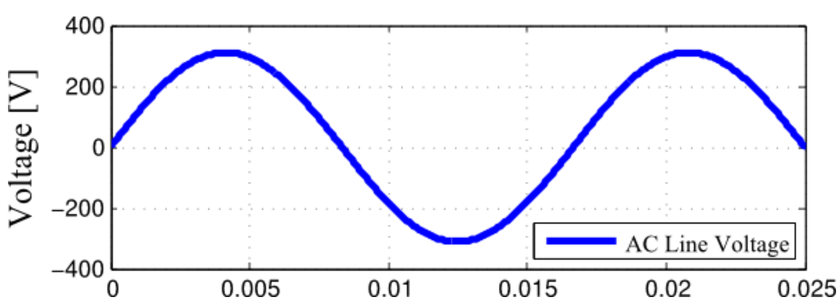
- Shibin Qin
  - Twice-line-frequency buffering
  - System control

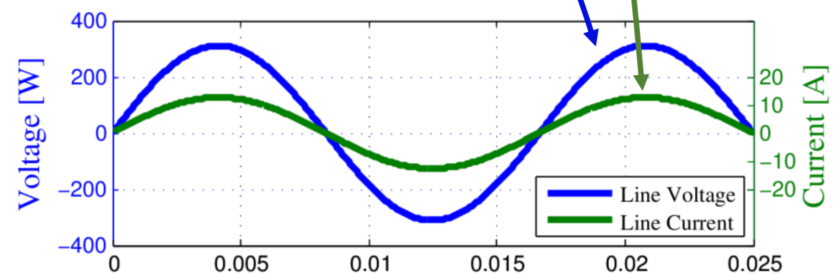
$30k funding through Google Academic Grant

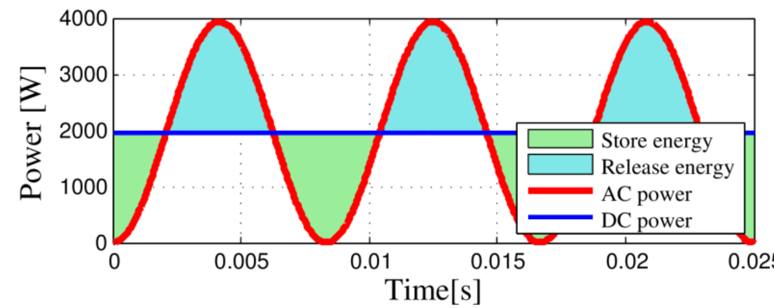
Key Technical Challenges





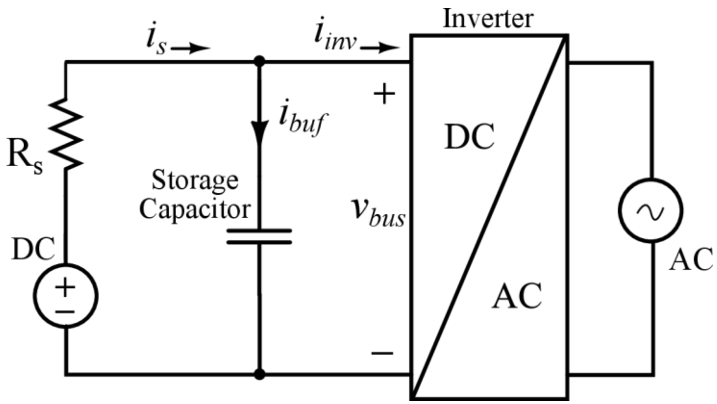




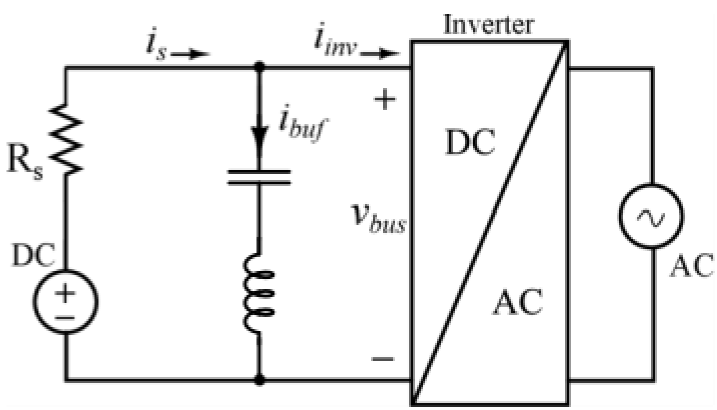


$$E_{store} = \frac{P_{dc}}{2\pi f_{line}}$$

Buffer Solutions



Passive: dc-link capacitor bank

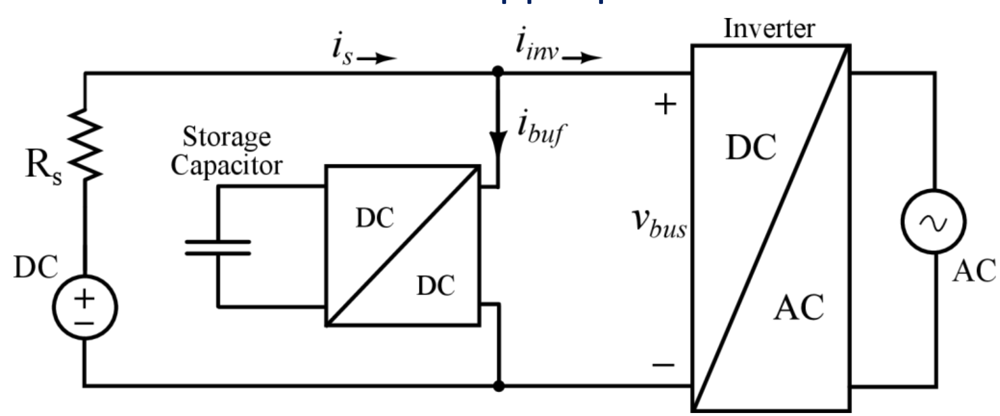


Passive: series resonant LC

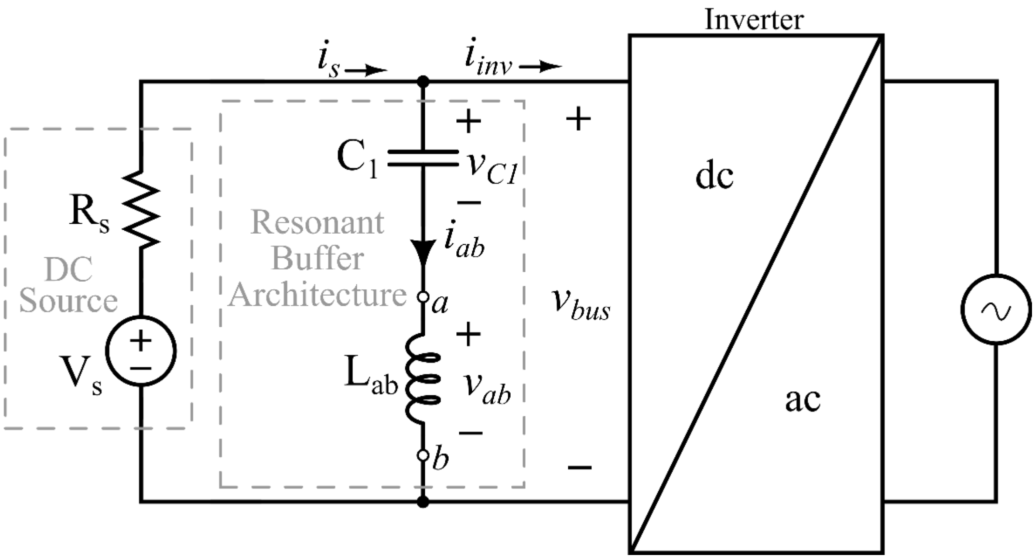
Twice-line frequency power decoupling solutions

- Passive buffering
  - Large volume = poor system power density
  - Poor lifetime
- Active buffering
  - Low efficiency
  - Increased system complexity
  - Higher cost

Active: full-ripple port



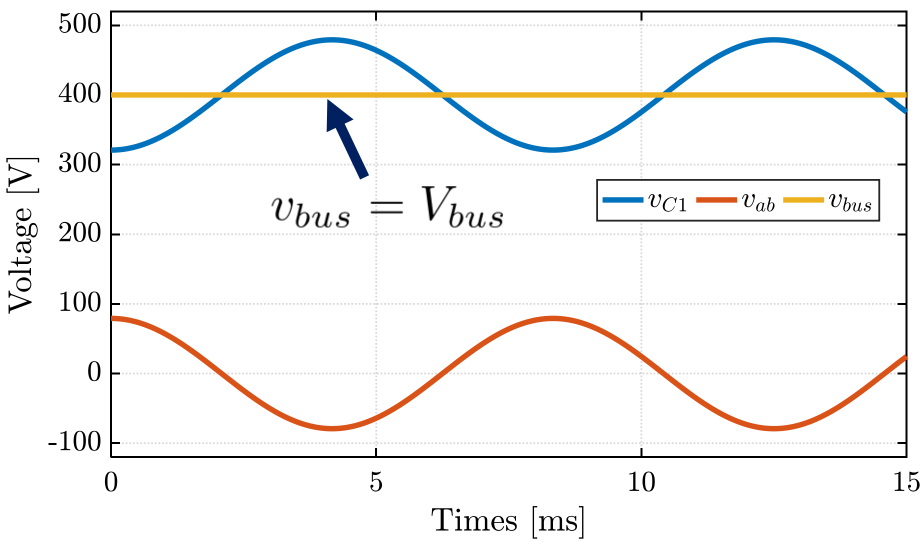
Passive Series Resonant LC Buffer

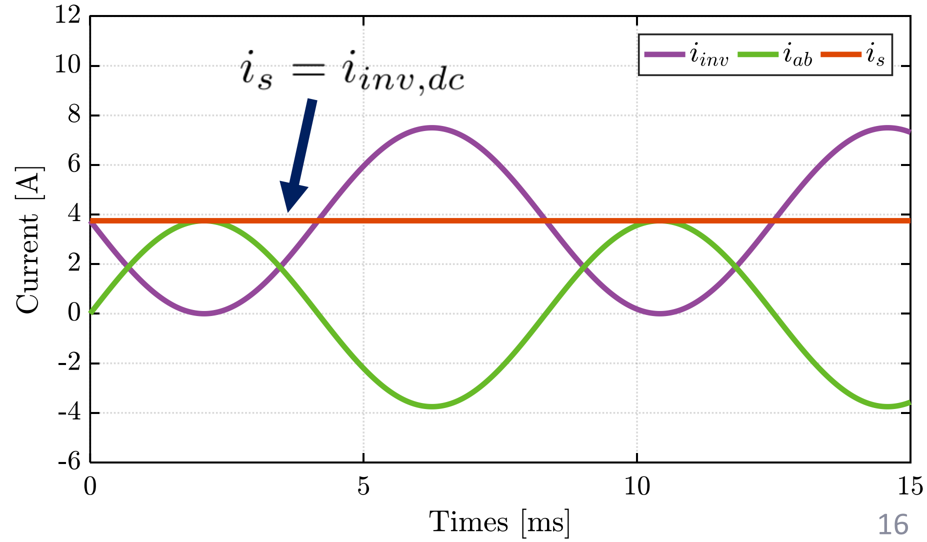


At resonant frequency:

$$2\omega_L = \frac{1}{\sqrt{L_{ab}C_1}}$$

$$Z_{buf} = 0$$

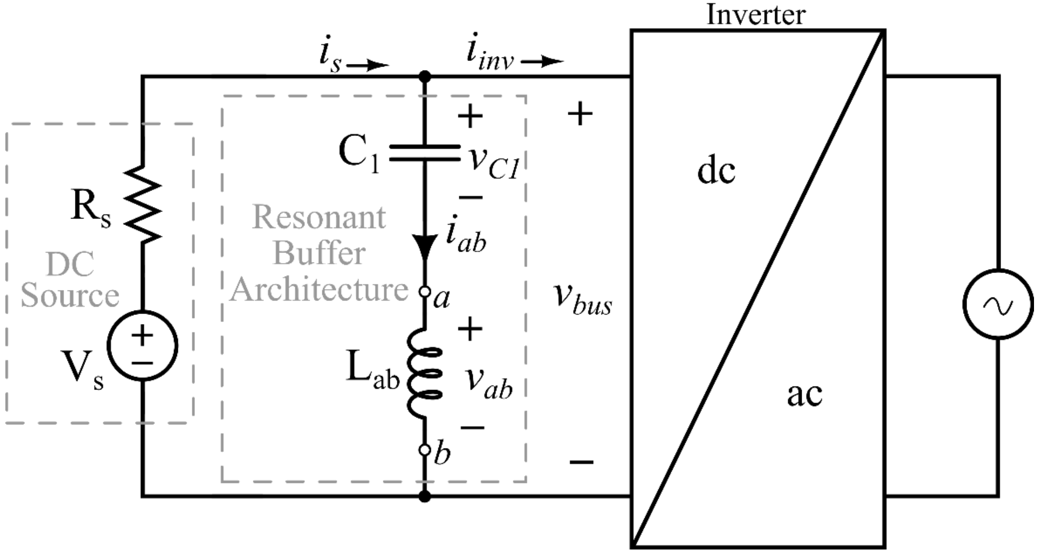




Passive Series Resonant LC Buffer

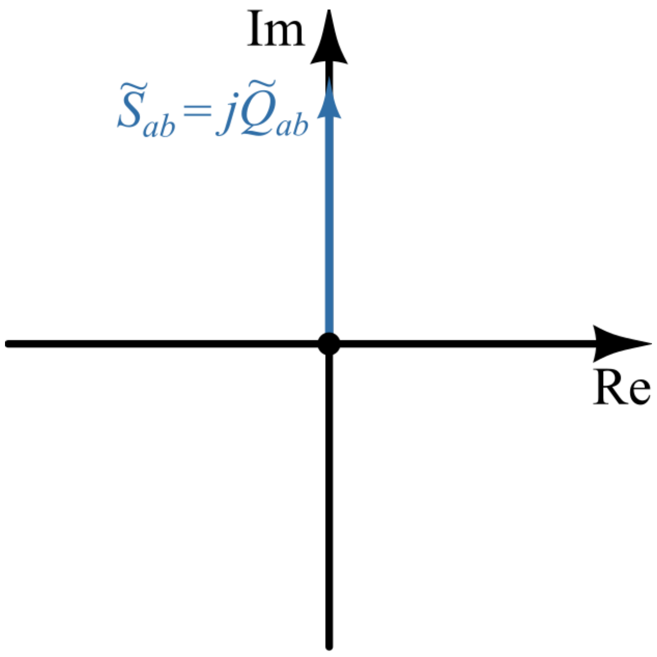
Express the $2\omega_L$ voltage and current components in phasor representation:

$$\widetilde{I}_{ab} = i_{ab,ac} = I_{ab} sin(2\omega_L t)$$



purely reactive power

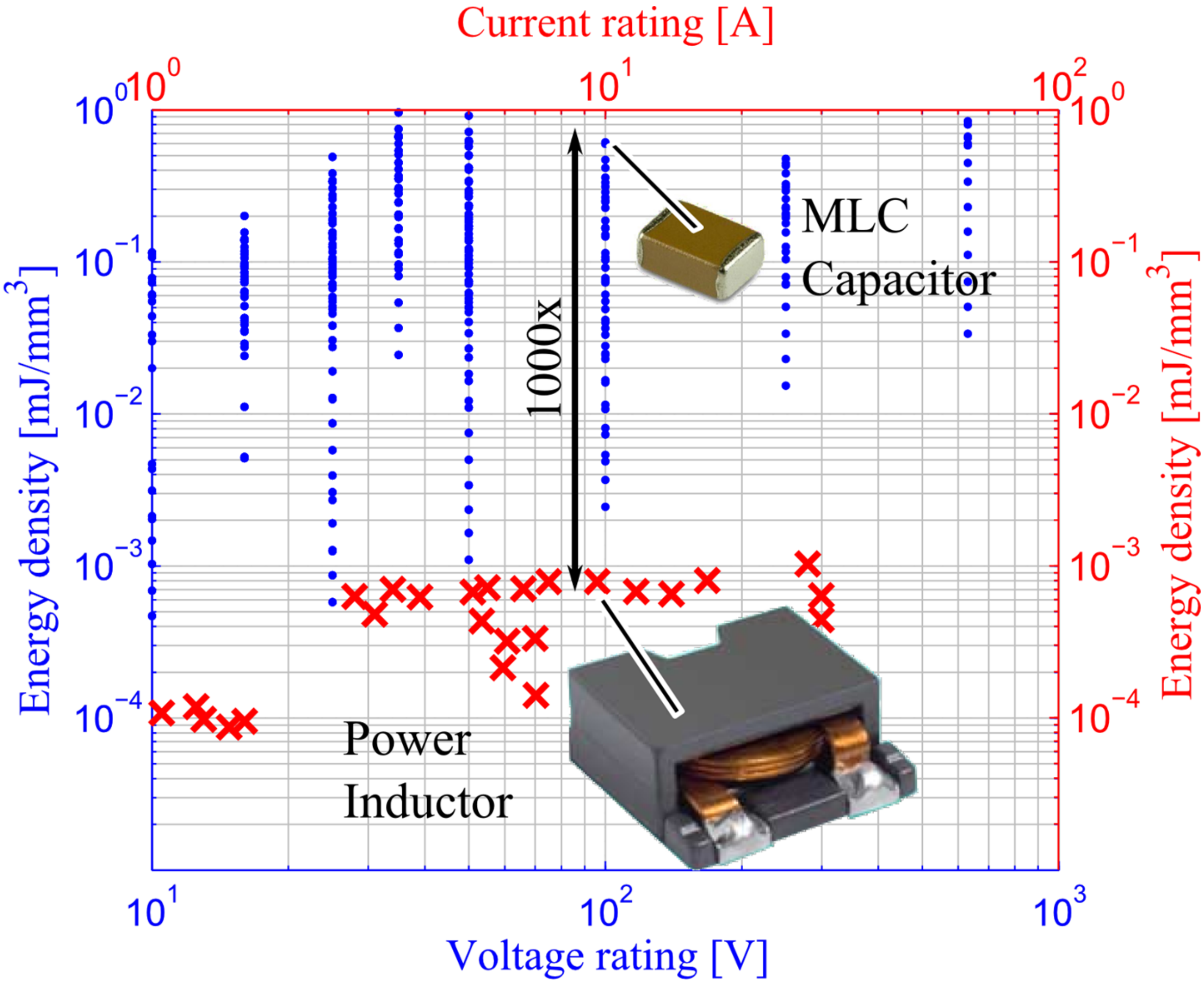
$$\widetilde{S}_{ab} = \widetilde{V}_{ab}\widetilde{I}^{*}_{ab} = j\widetilde{Q}_{ab}$$



Example: If C = 100 uF then L = 18mH for resonance at 120 Hz

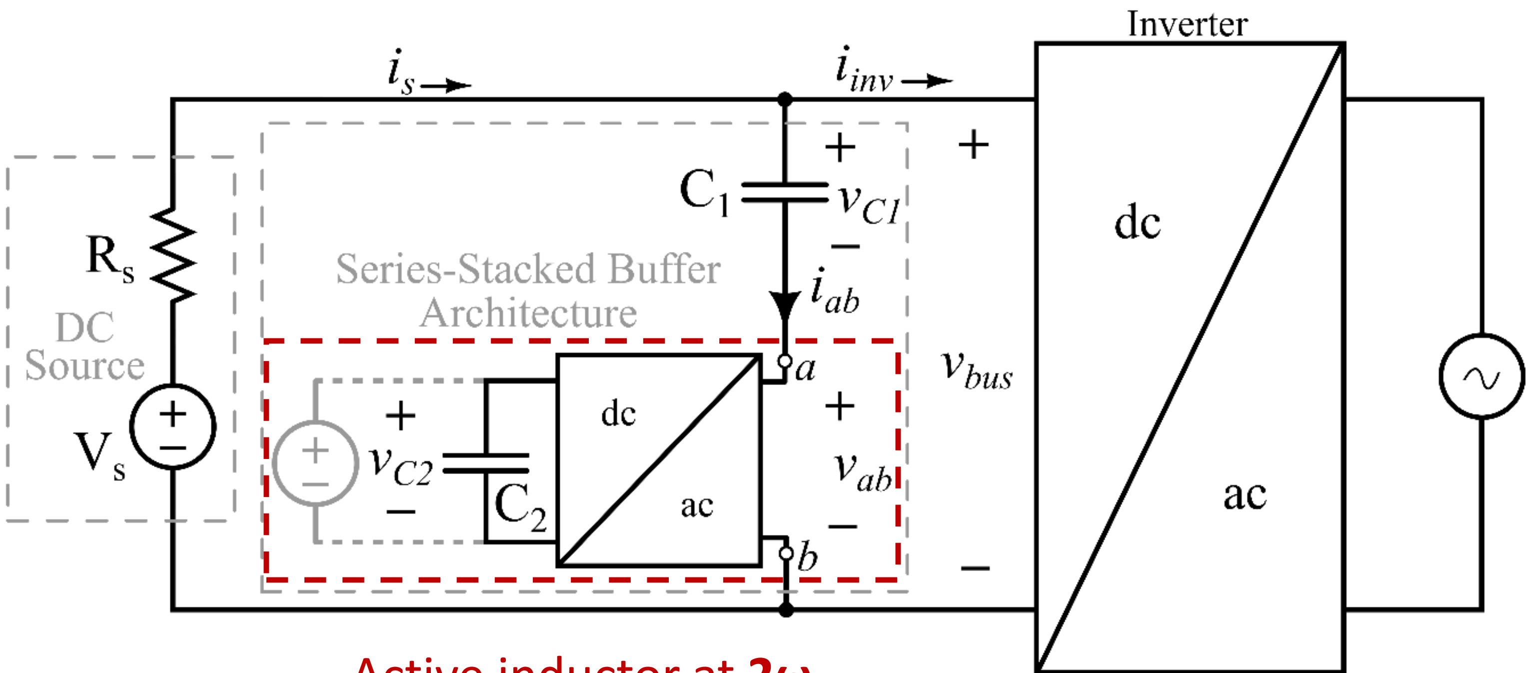
Can we implement the resonant buffer without such a large physical inductor?

Passive Component Density



Active Series Resonant LC Buffer

- Use a dc-ac converter with capacitive load to emulate an active inductor
  - Vastly improve power density of passive resonant solution
  - Implement resonant impedance behavior with proper control
  - Series-stacked buffer (SSB) architecture



Active inductor at $\mathbf{2\omega_L}$

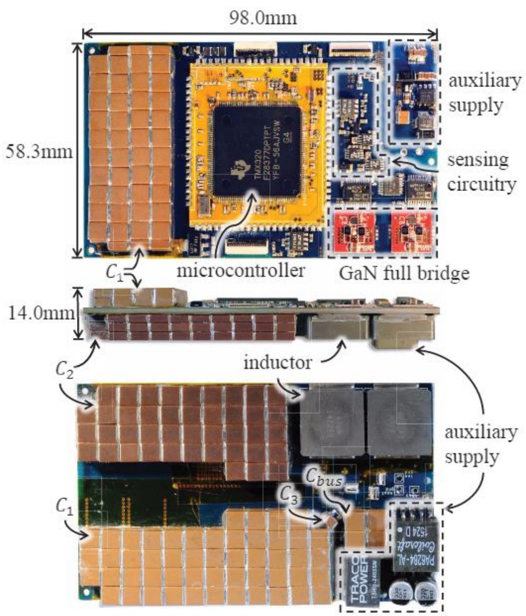
Buffer Solutions – Series-Stacked Buffer

Benefits:

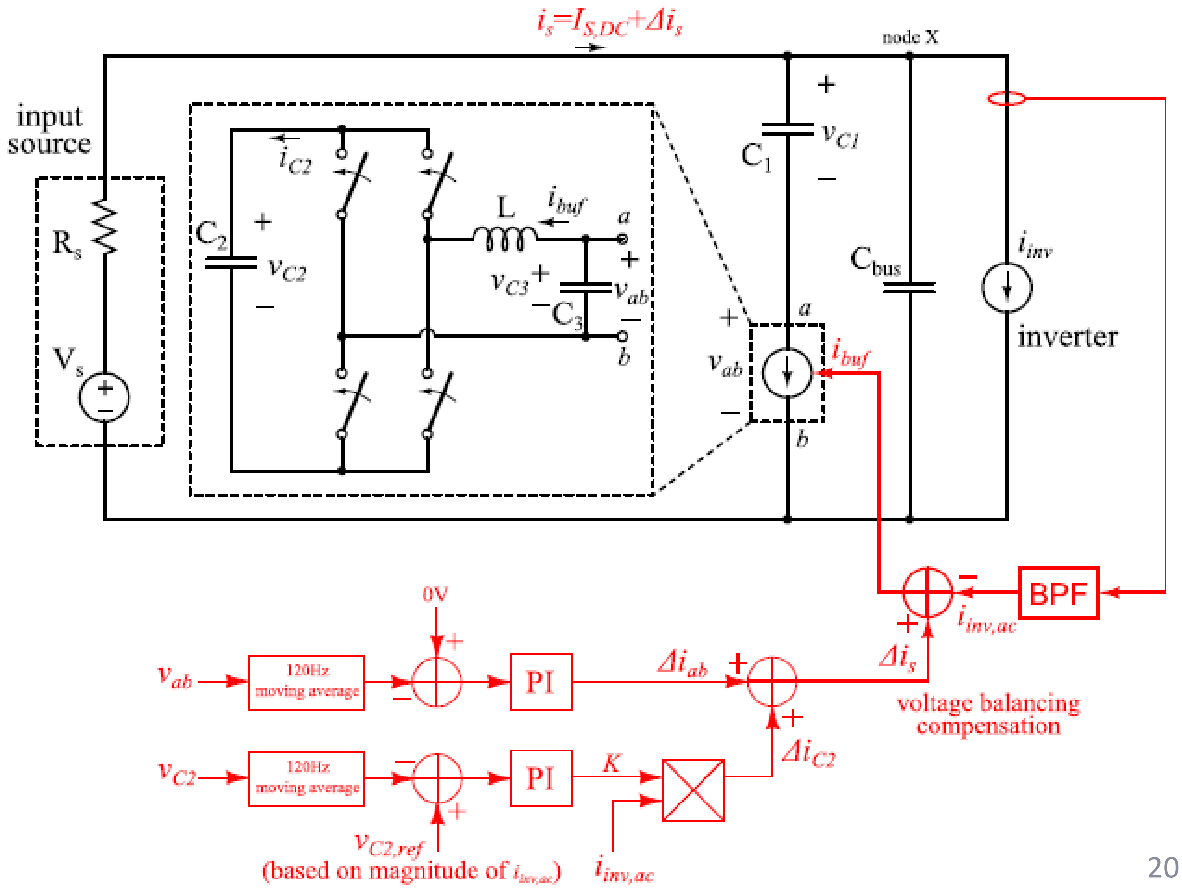
- High efficiency
  - Partial power processing
- High power density

Shortcomings:

- Complex non-intuitive control
- Current sensing and control
  - Not a two-terminal device



2 kW SSB, Google Little Box[1],[2]

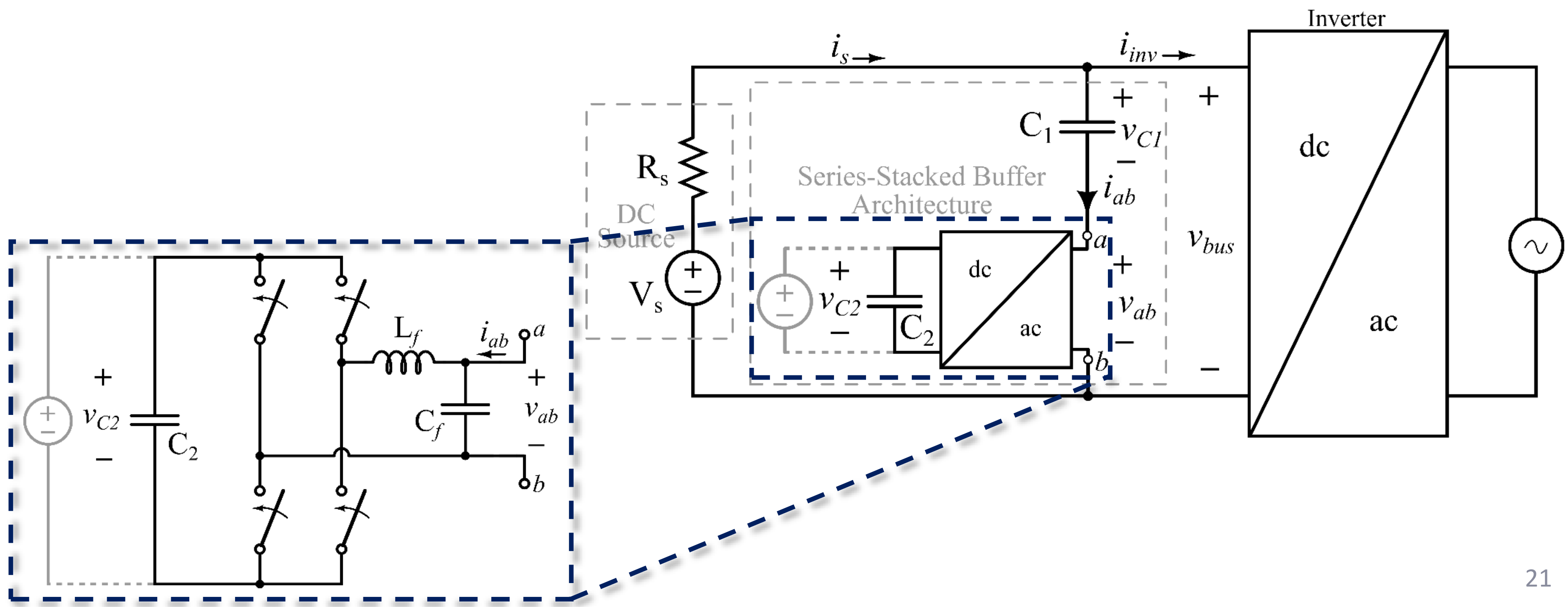


[1] S. Qin. TPEL, 2017.
[2] Y. Lei. APEC, 2016.

Active Series Resonant LC Buffer

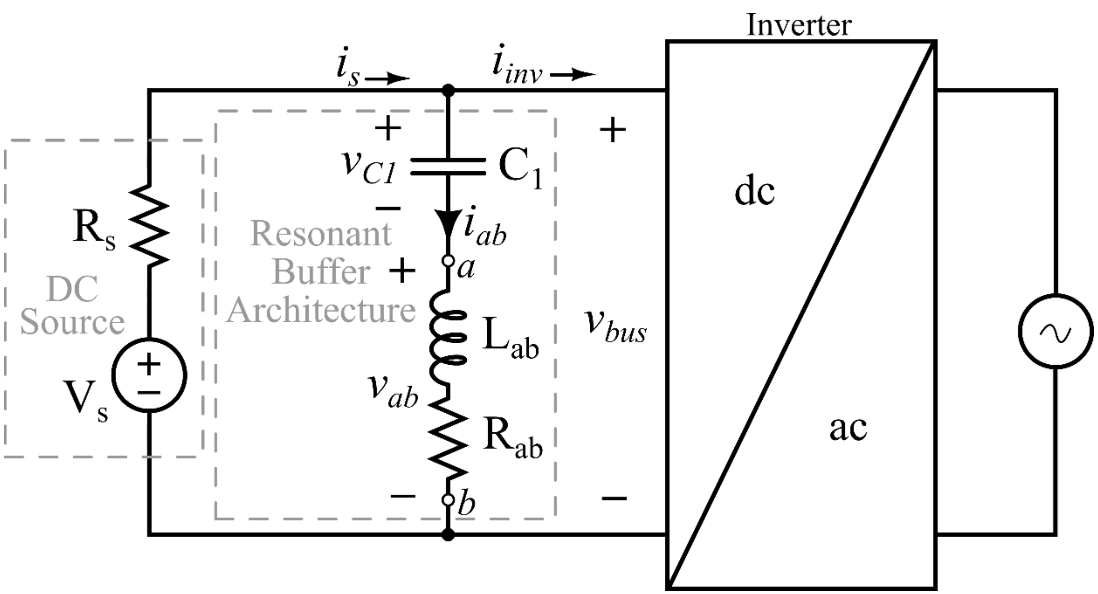
- Dc-ac buffer converter: full-bridge buck
- Practical buffer converter is lossy
  - V_{C2} will gradually decay

$$\widetilde{S}_{ab} = \widetilde{V}_{ab}\widetilde{I}^*_{ab} = j\widetilde{Q}_{ab} + \widetilde{P}_{ab}$$ ← additional real power term



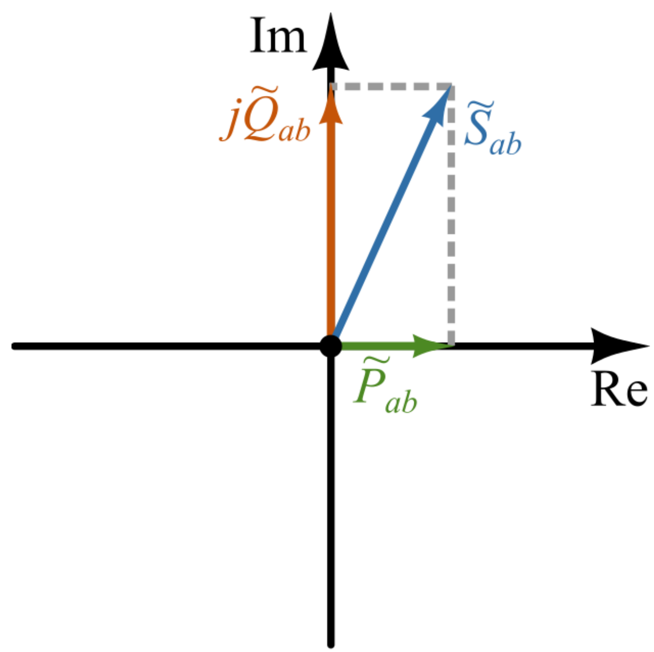
Passive Series Resonant LC Buffer with Loss

Incorporate practical buffer converter loss with a series resistance, R_{ab}, in the equivalent impedance model



real power = power loss

$$\widetilde{S}_{ab} = \widetilde{V}_{ab}\widetilde{I}^*_{ab} = j\widetilde{Q}_{ab} + \widetilde{P}_{ab}$$



Control Architecture with Loss

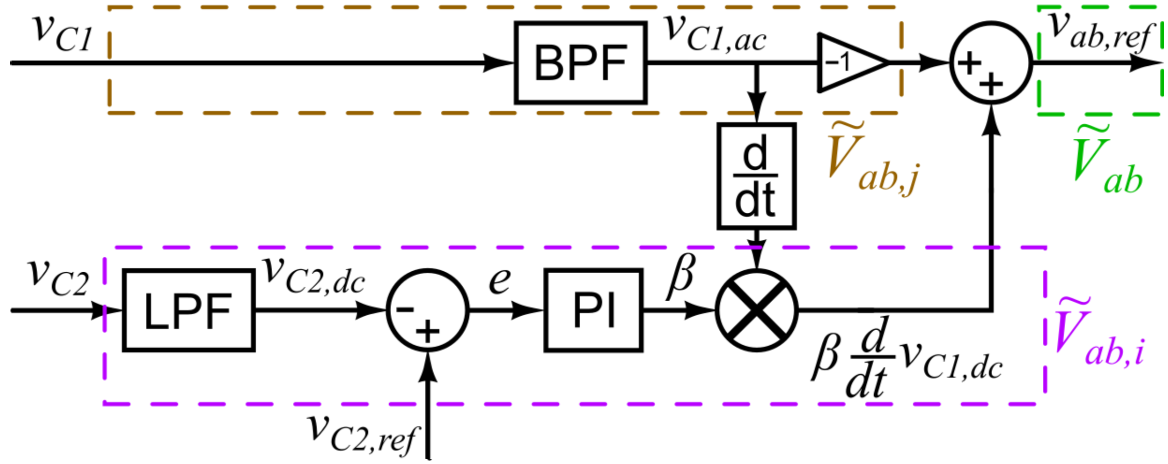
Characteristic equations:

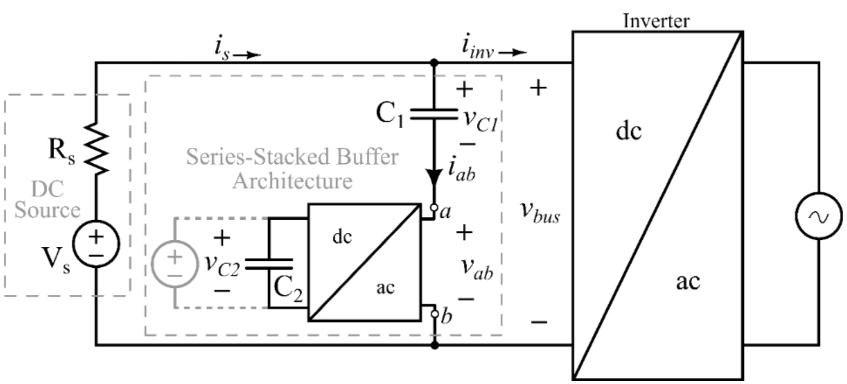
$$\widetilde{V}_{ab,j} = -\widetilde{V}_{C1}$$

$$\widetilde{V}_{ab,i} = R_{ab}\widetilde{I}_{ab} = R_{ab}\widetilde{I}_{C1} = R_{ab}C_1\frac{d}{dt}\widetilde{V}_{C1} = \beta\frac{d}{dt}\widetilde{V}_{C1}$$

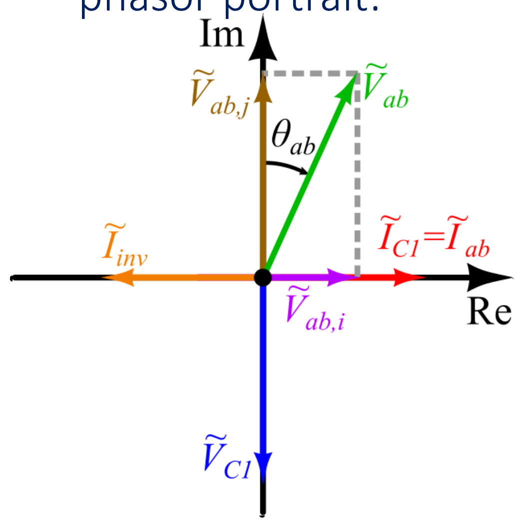
$$\widetilde{V}_{ab} = \widetilde{V}_{ab,i} + \widetilde{V}_{ab,j}$$

Control architecture:

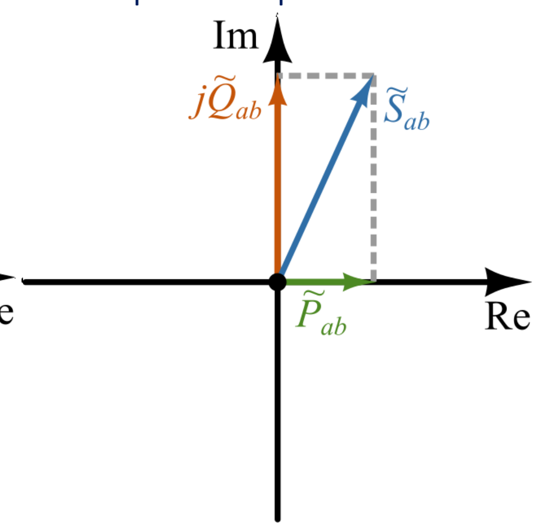




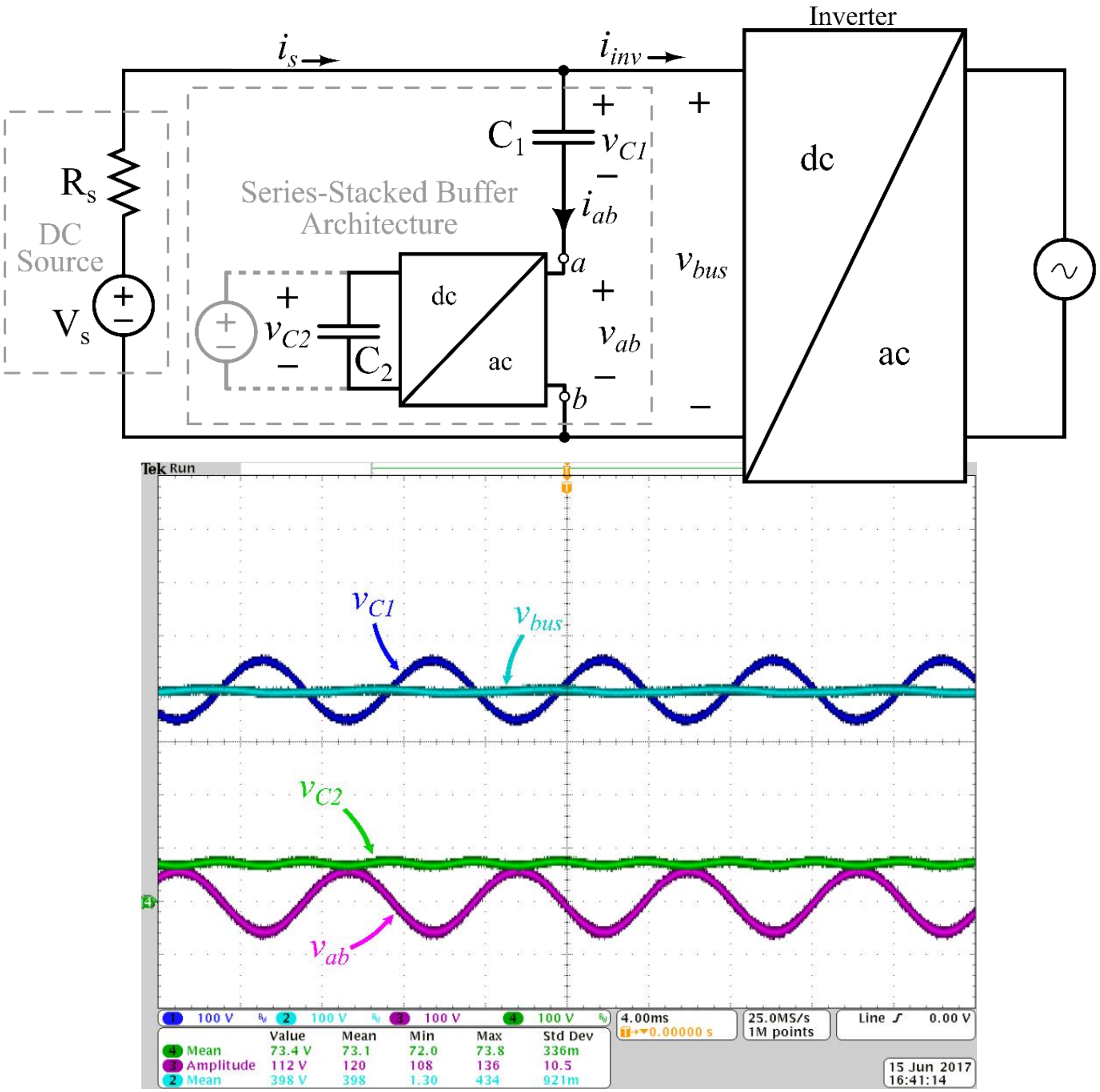
Voltage/current phasor portrait:



Power phasor portrait:



Experimental Results

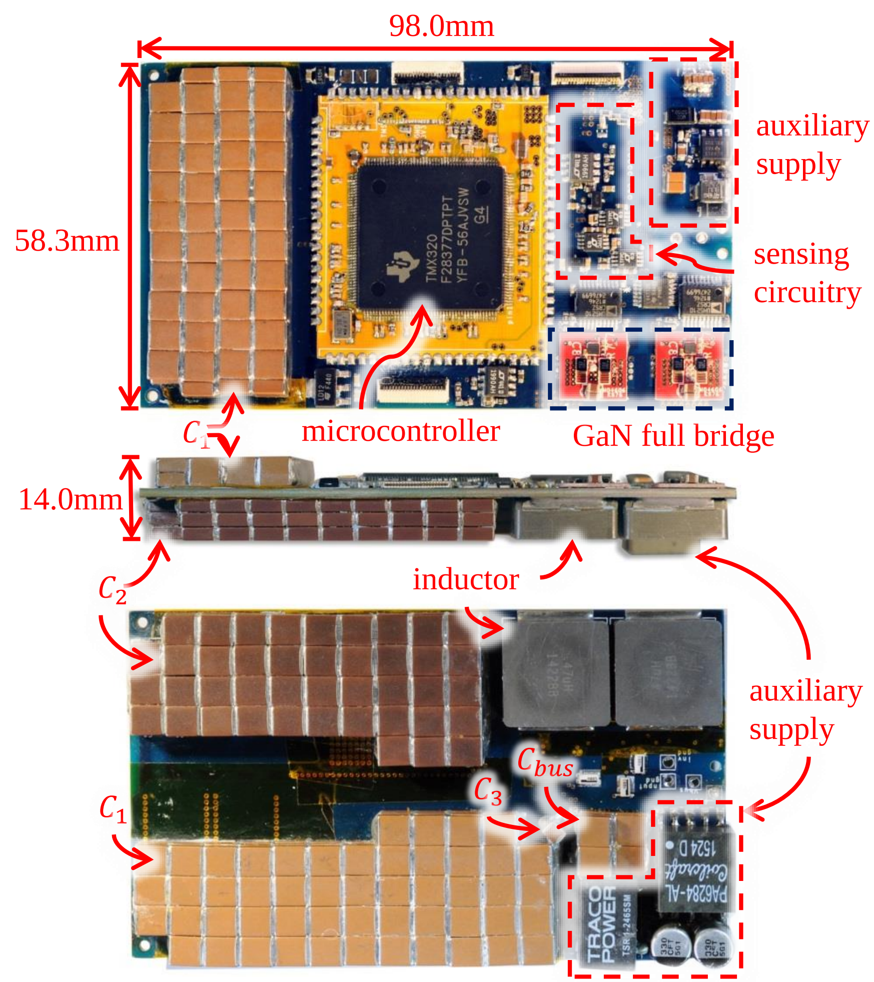


N. Brooks, S. Qin, R.C.N. Pilawa-Podurski “Design of an Active Power Pulsation Buffer Using an Equivalent Series-Resonant Impedance Model”, COMPEL 2017 [Best Paper Award]

Hardware Prototype – Energy Density

Design requirement:
- 2 kVA (PF = 0.7~1)
- 400 V ~ 450V bus voltage,
- 10 A peak to peak current

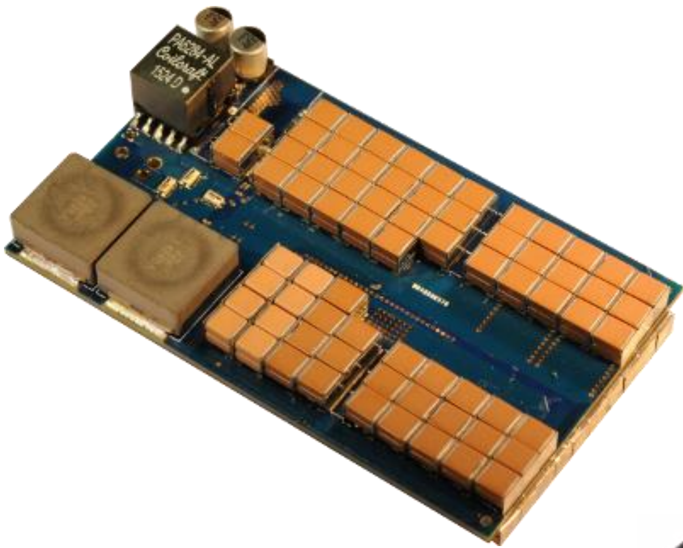
Way of measurement	Volume	Power density
Rectangular box	4.88 inch^3	410 W/inch^3
passive component	2.01 inch^3	995 W/inch^3



The highest prior active filtering power density reported was 79.4W/inch^3 by component volume, by Chen et al, TPELS 2013 (120 W, metal film capacitors)

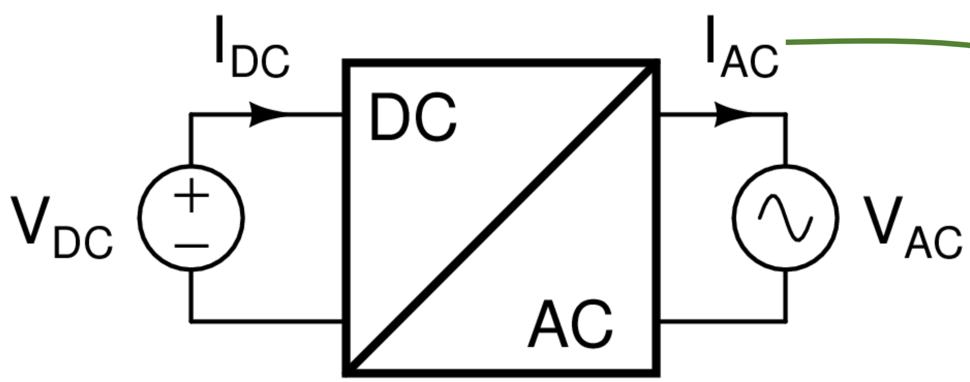
> 99% efficiency across load range

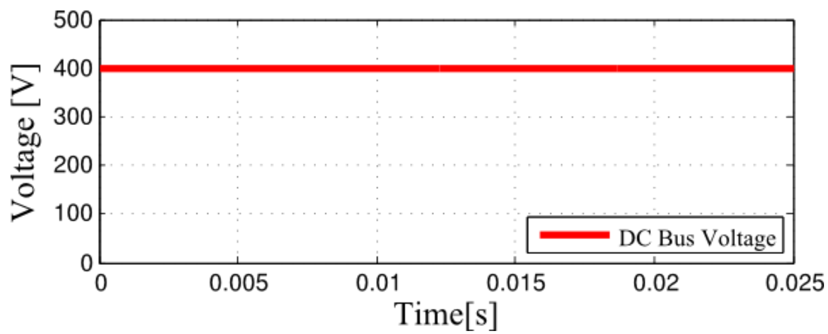
Overall Size Reduction

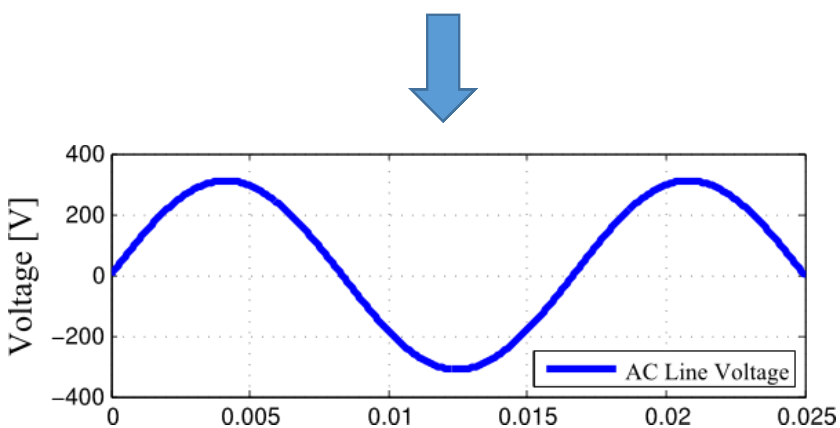


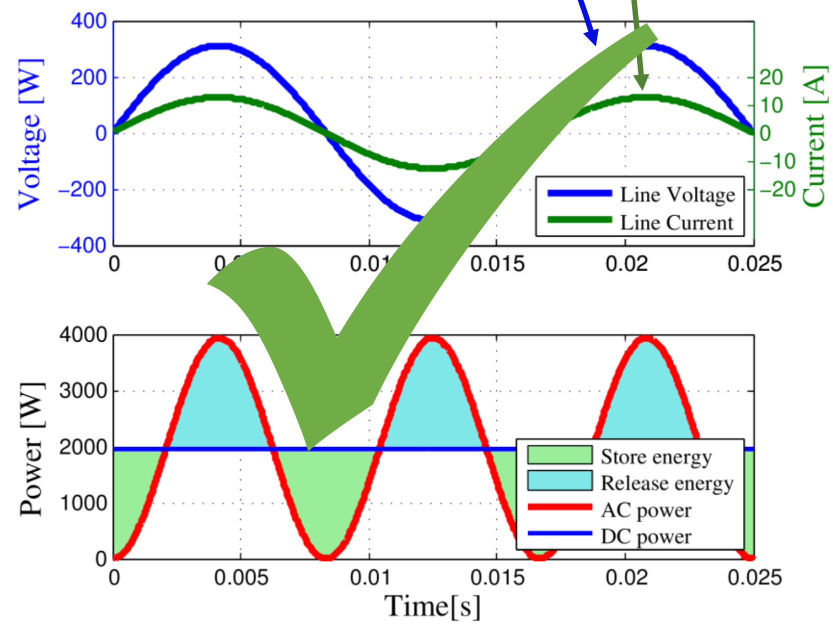
7-10x size reduction

Key Technical Challenges





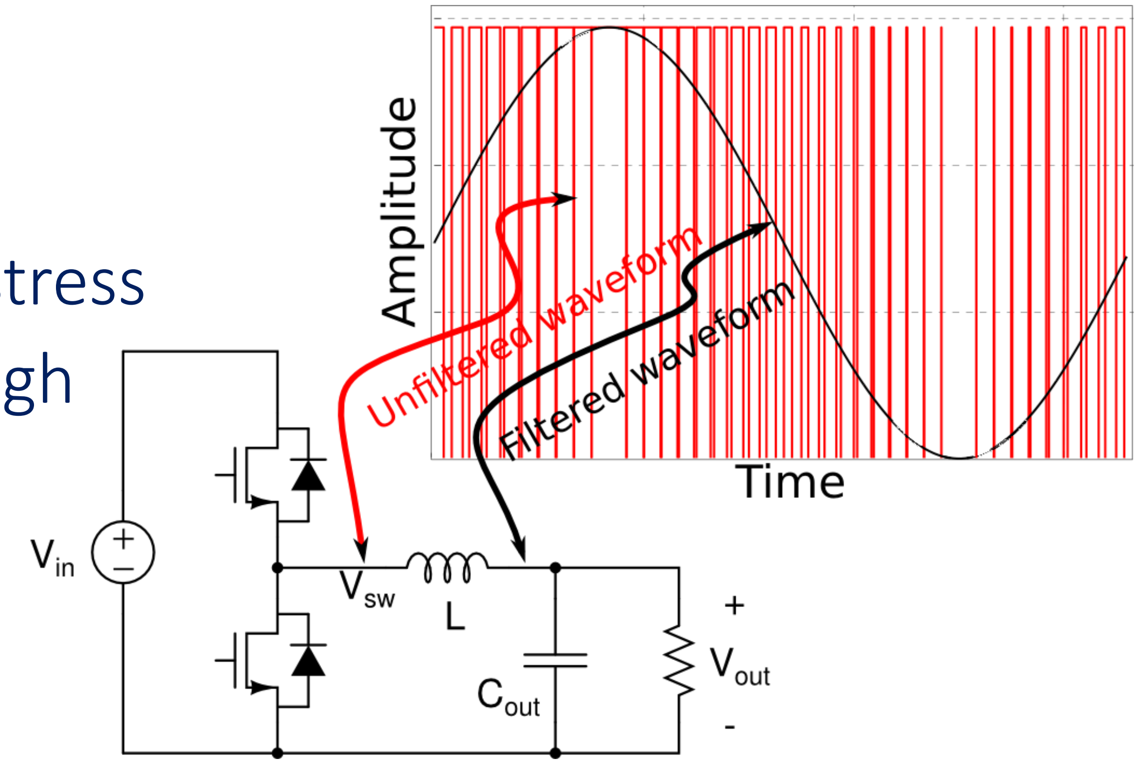




$$E_{store} = \frac{P_{dc}}{2\pi f_{line}}$$

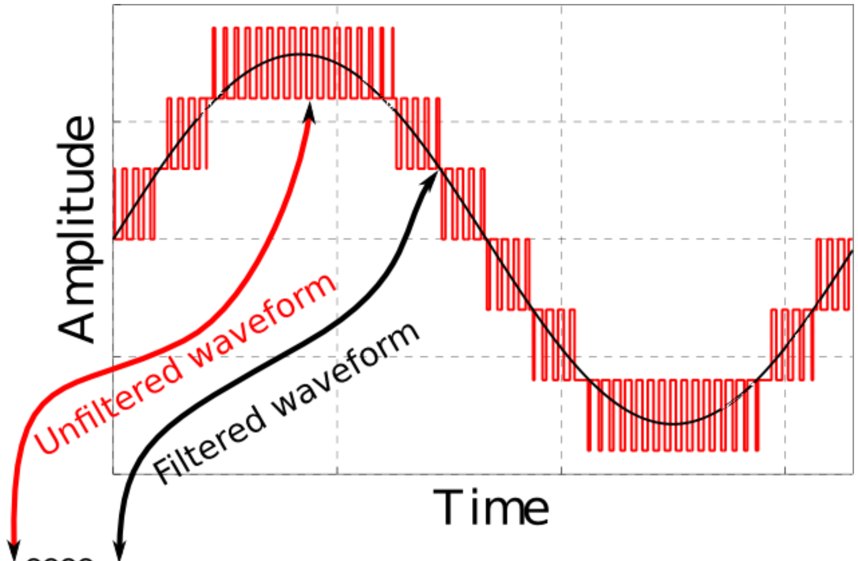
Inverter – Today's Practice

- High switch voltage stress
- High power loss at high frequencies
- Large inductor

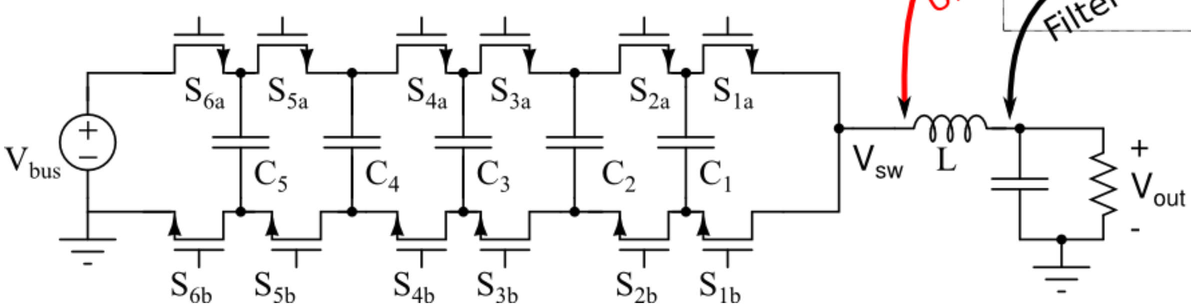


Wide band-gap semiconductors alone will not address these challenges. We need to consider new inverter architectures.

Multi-Level Flying-Capacitor Converter



7-Level Convert

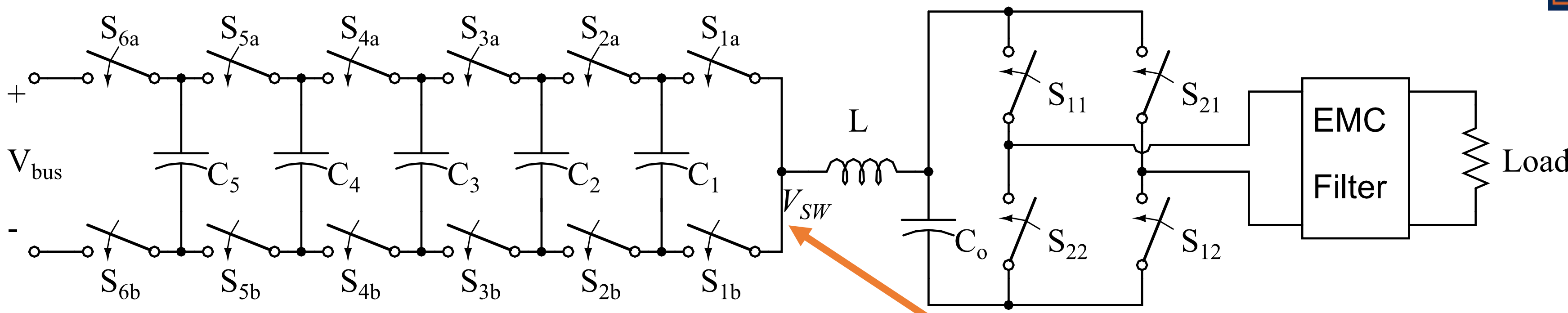


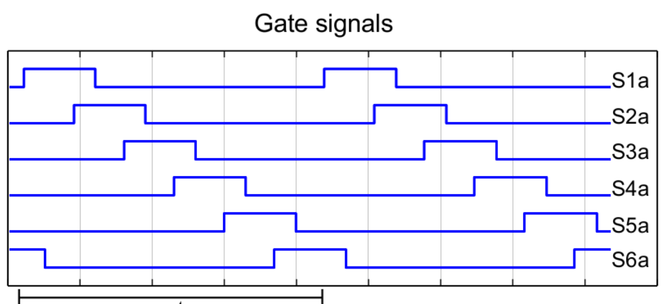
- Reduced switch voltage stress [V_{DC}/6]
  - Can utilize fast, low-voltage transistors
- Inductor ripple frequency [F_{sw}*6]
- Reduced ripple magnitude [V_{DC}/6]

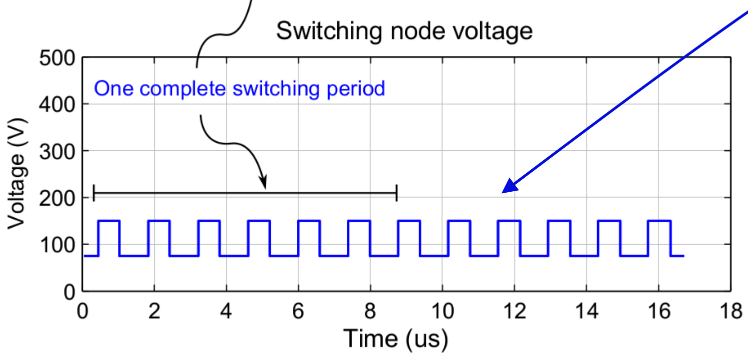
Much smaller inductor!

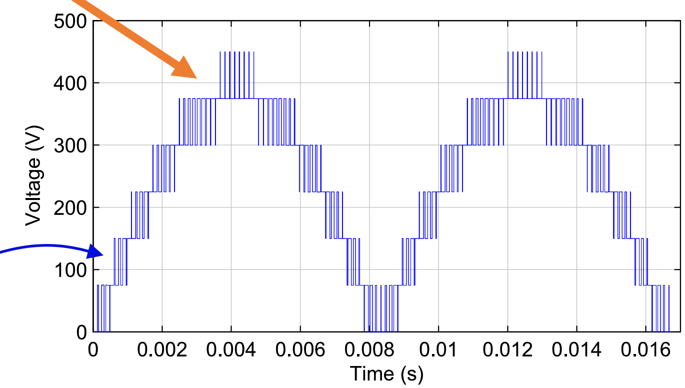
T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," PESC '92

7-level Flying Capacitor Converter







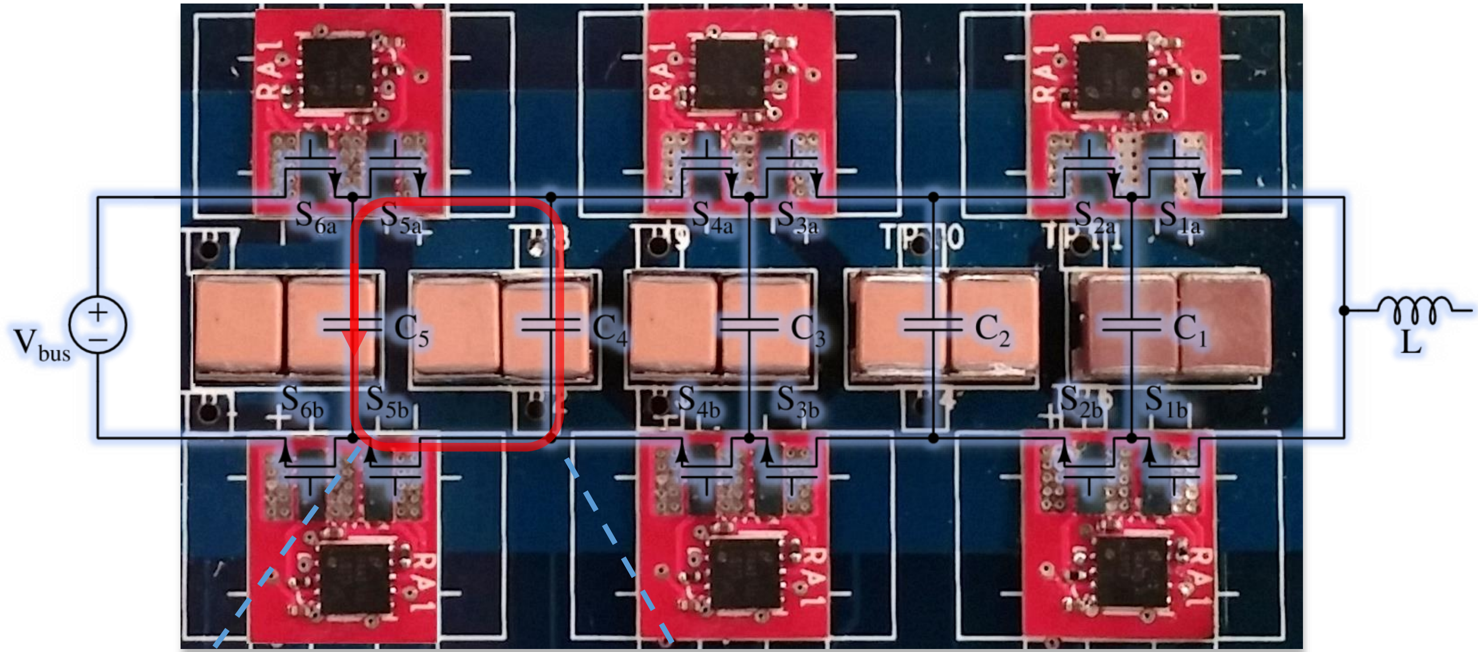


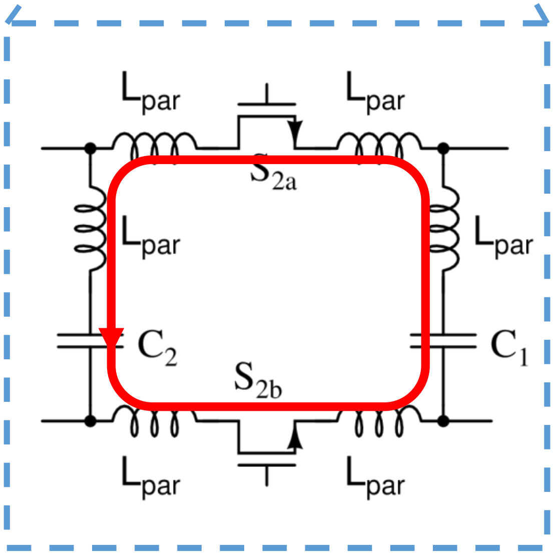
Challenges

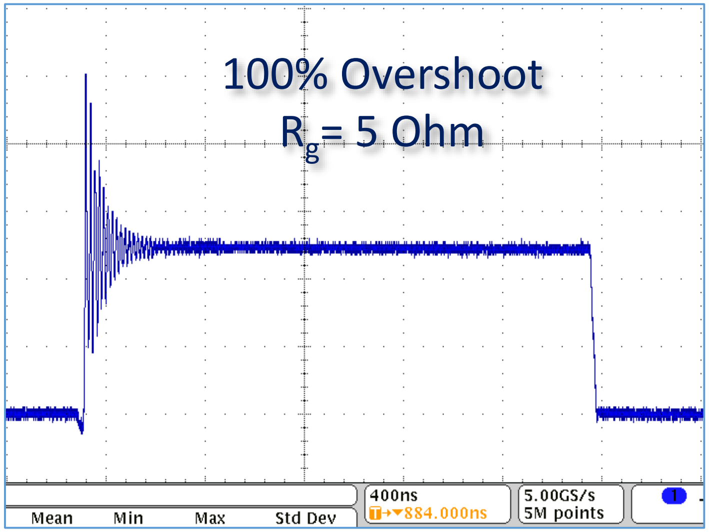
- Capacitor voltage balancing
- Gate driving complexity
- Parasitic inductance (especially with GaN devices)

No demonstrated examples of > 4 level flying capacitor multi-level inverter using GaN transistors, and none switching in the 100's of kHz at kW levels.

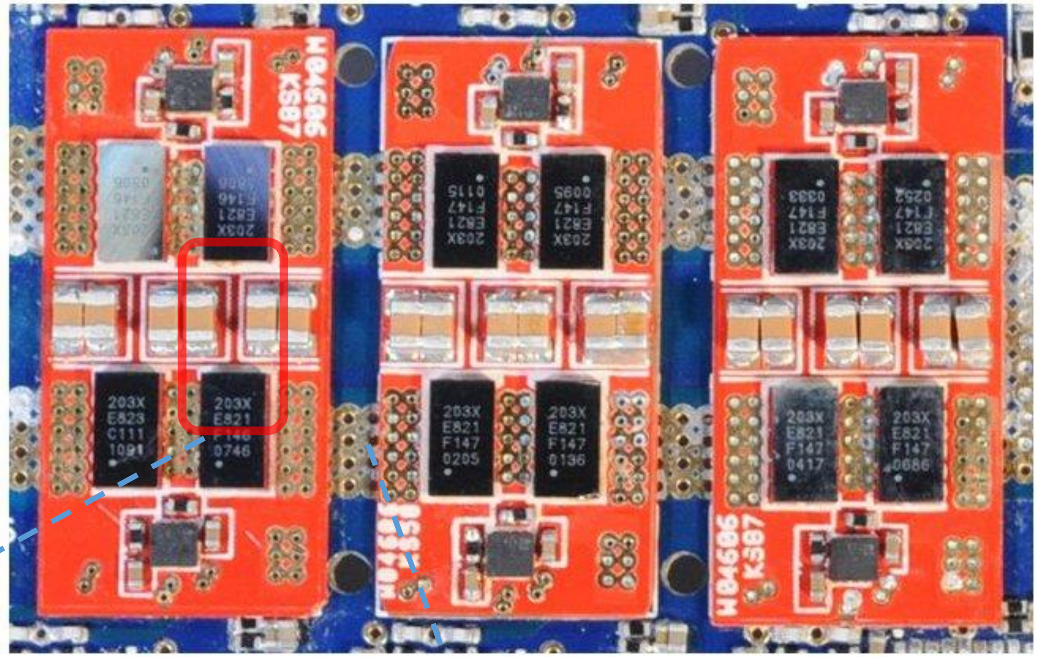
Key Challenge: Parasitic Loop Inductance

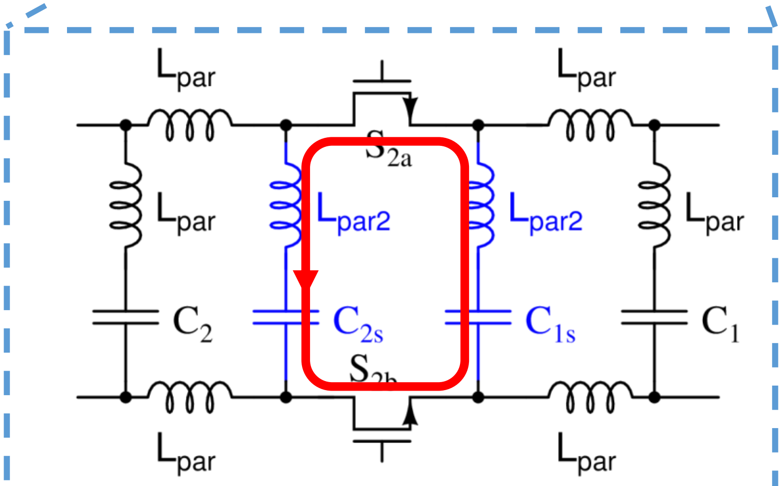


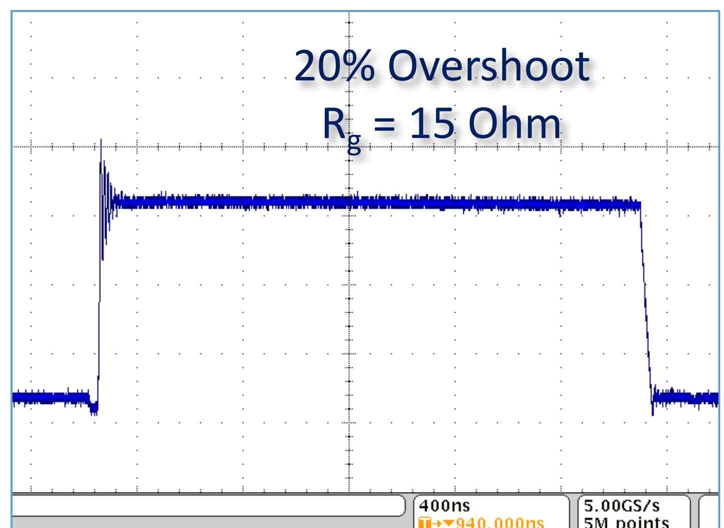




Modular Switching Cell

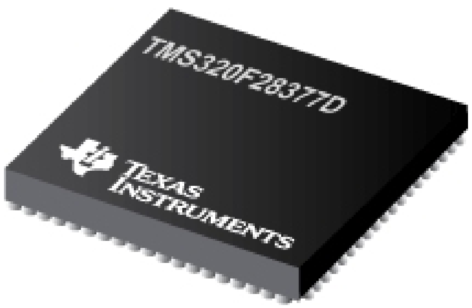


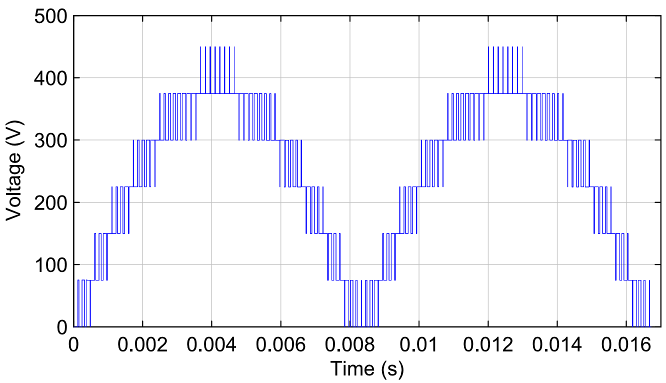


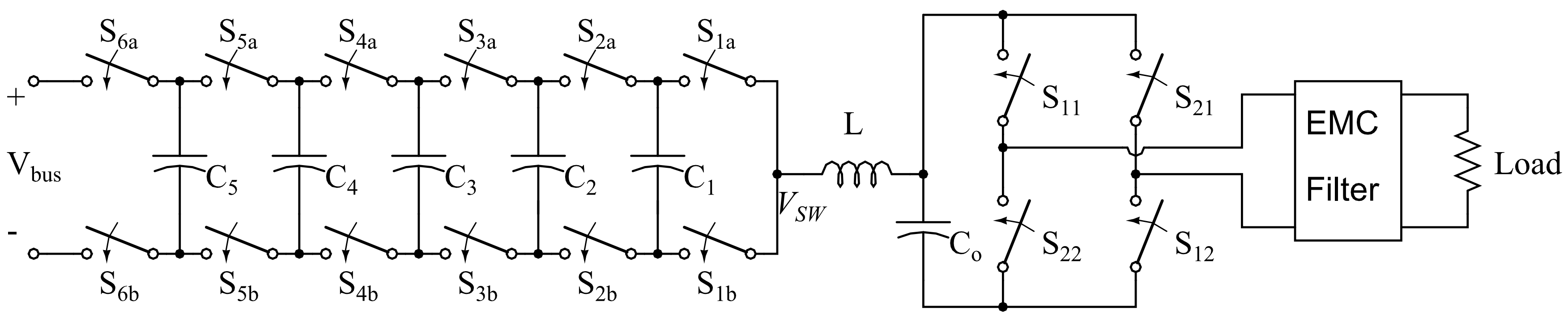


Digital Control

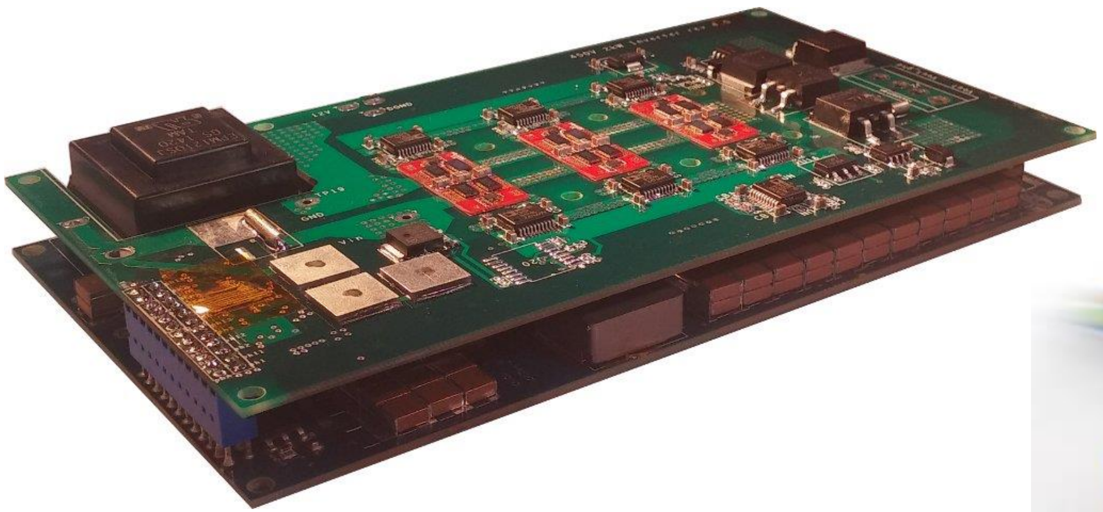
- Control objective:
  - Generate correct amplitude
  - Switch only minimum inductance loops
  - Maintain capacitor voltage balance

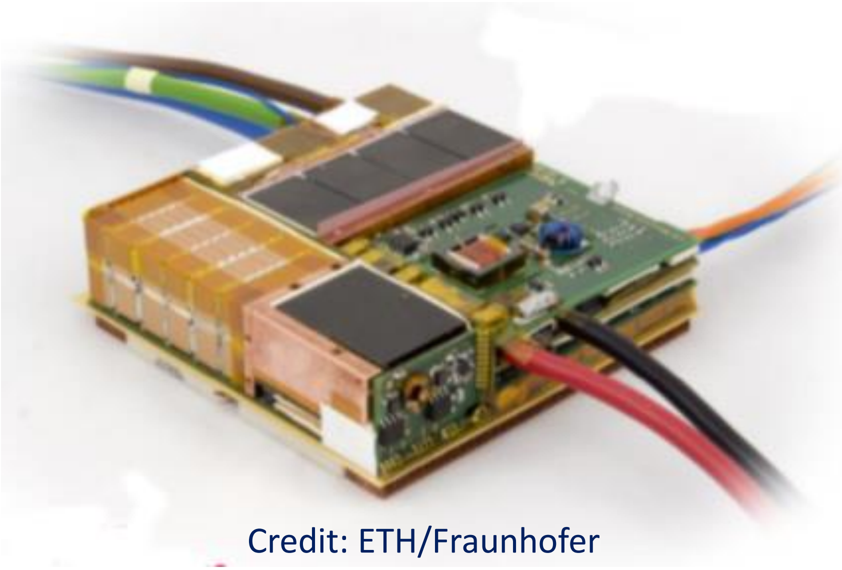






Prototype #1

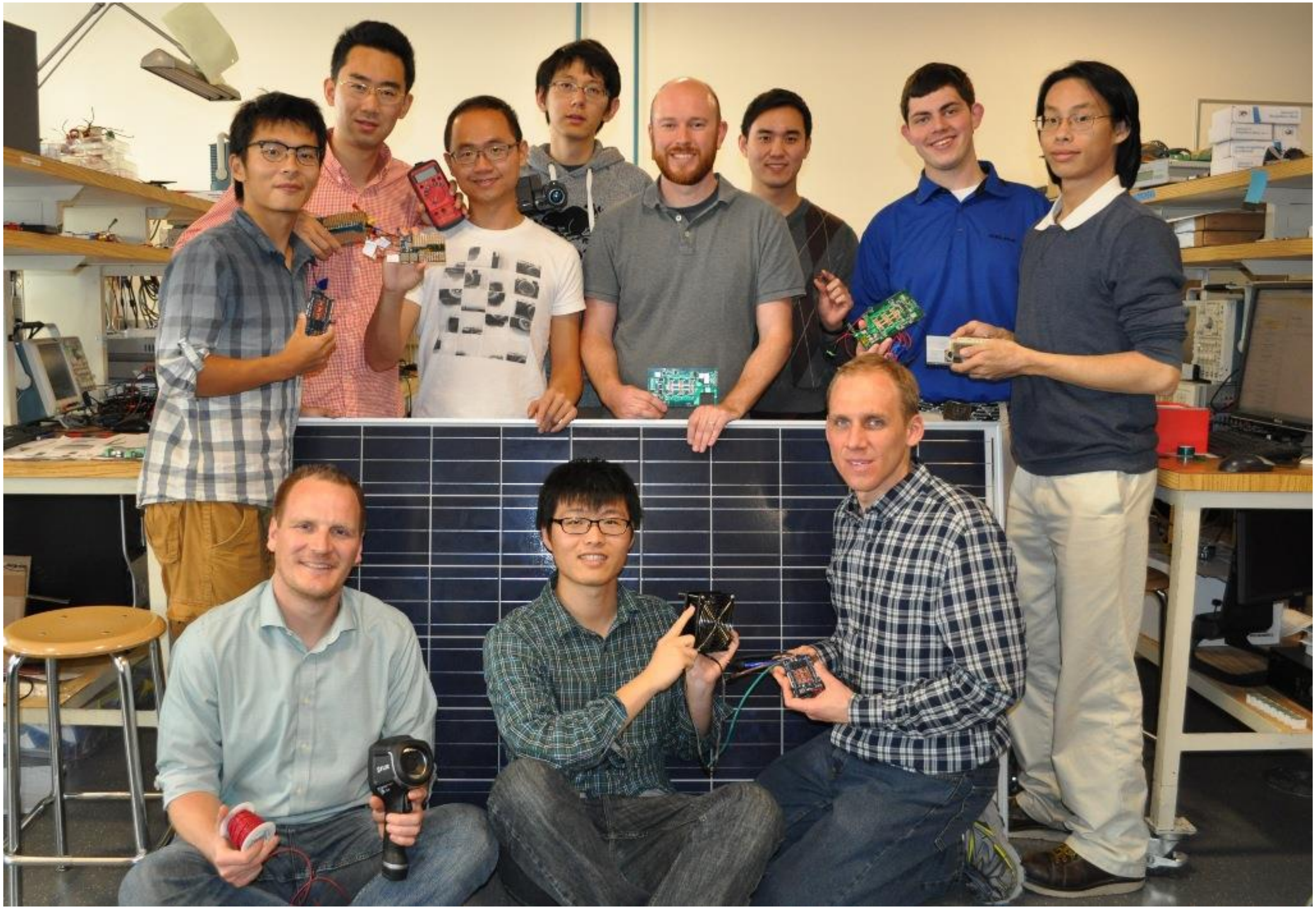




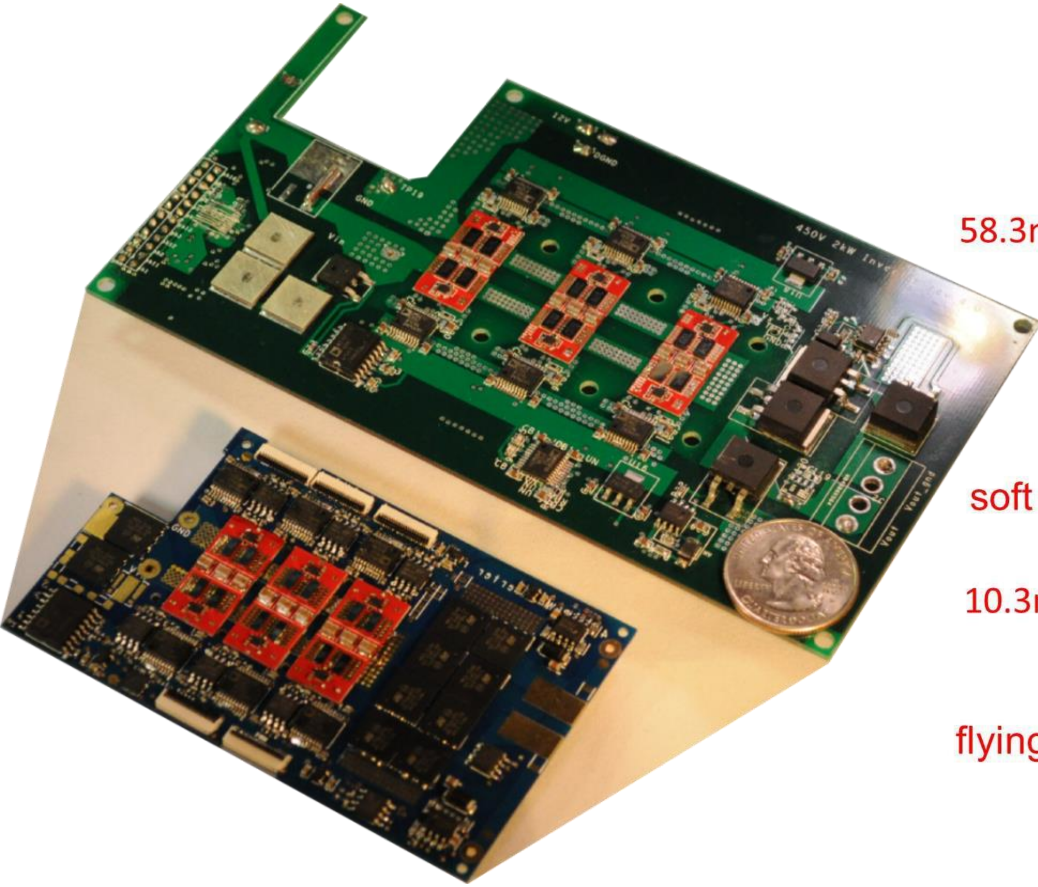
Credit: ETH/Fraunhofer

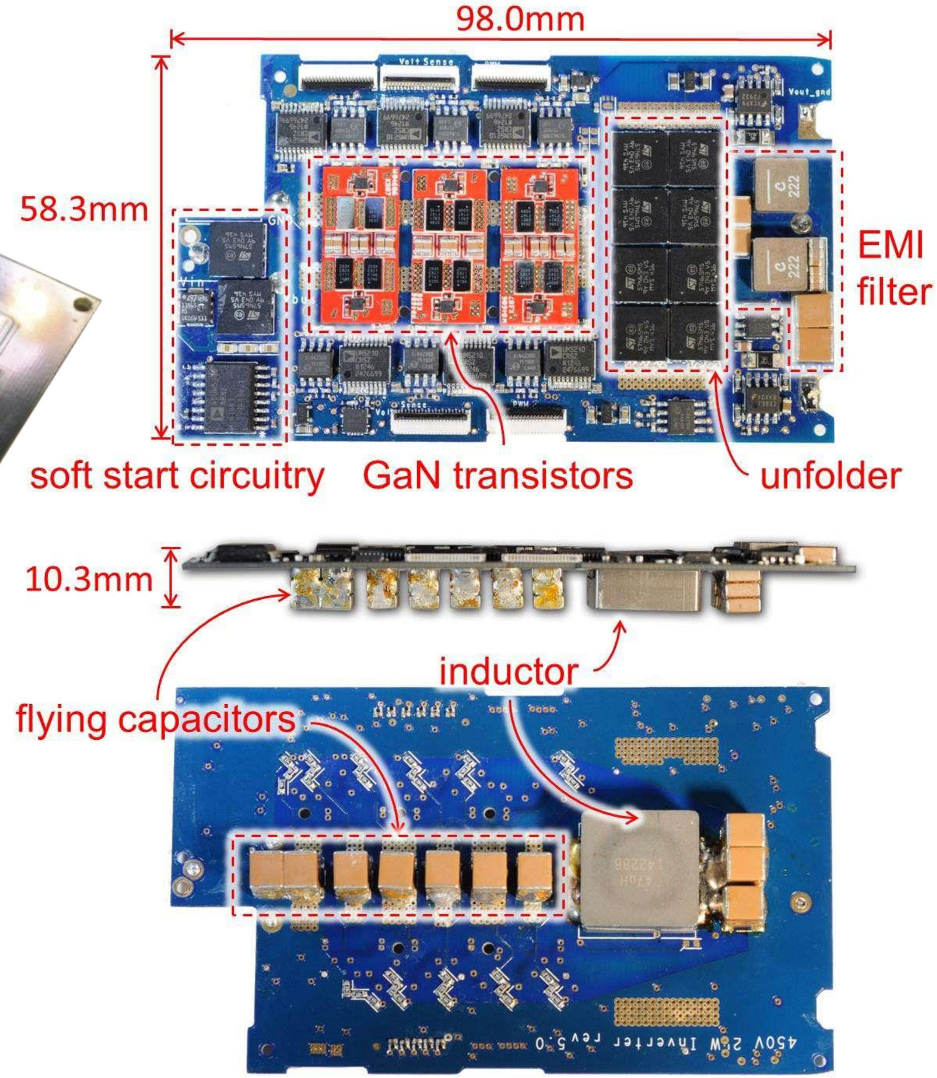
- 80 W/in^3, 98% efficient
- 500 total entries
  - July 23, 2015, 120 submitted final report
  - 18 finalists selected to October 21 NREL testing

Growing the Team

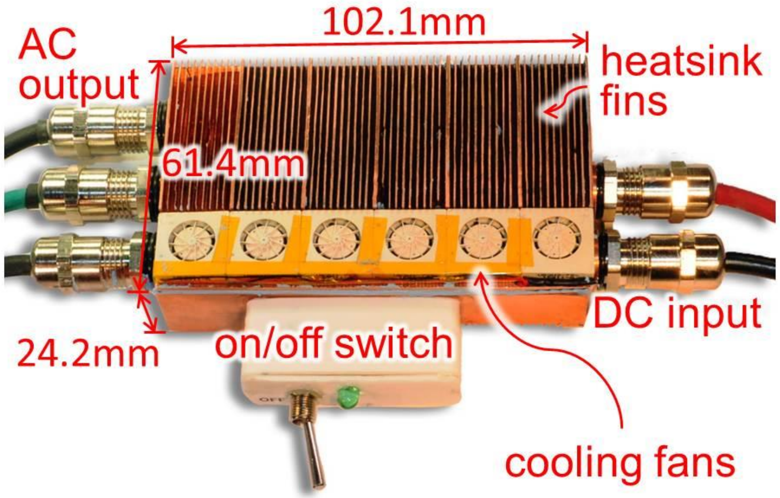


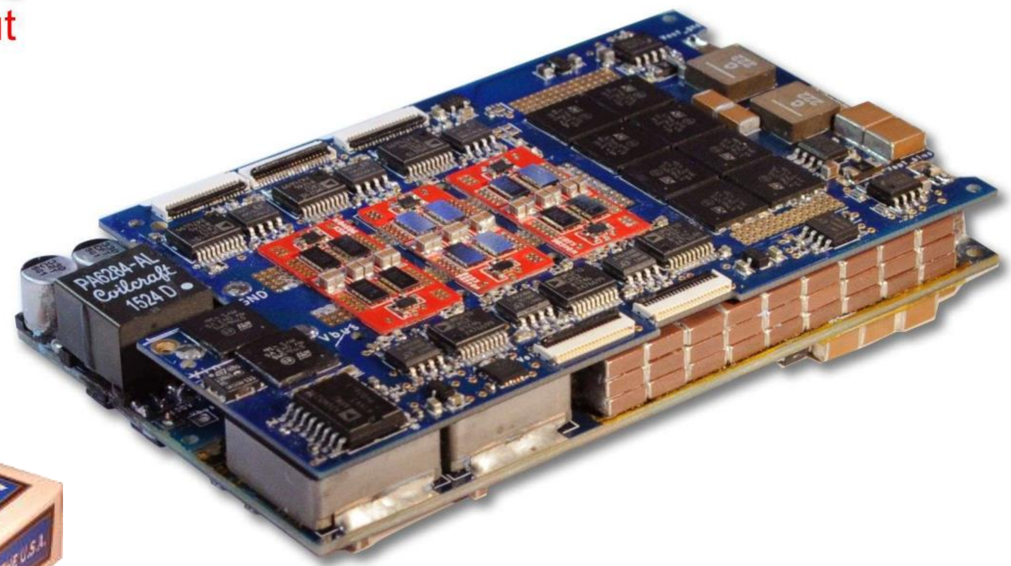
Shrinking the Hardware





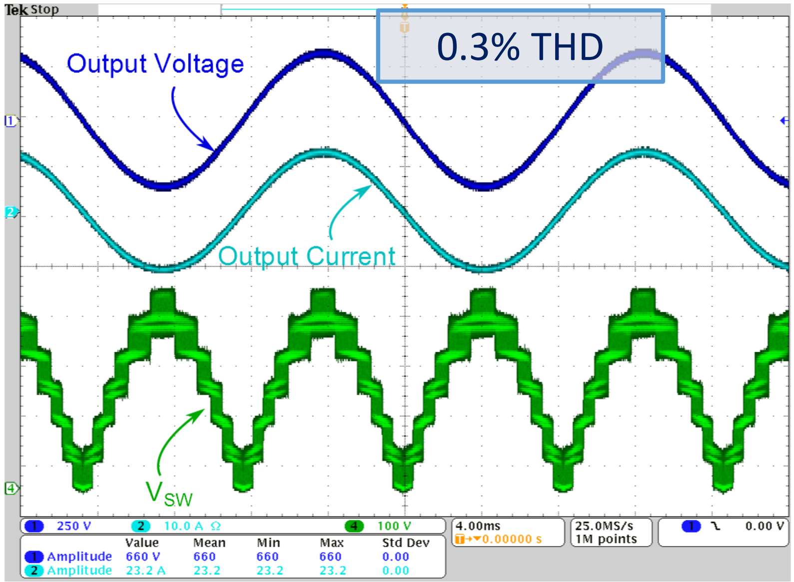
2 kW Hardware Prototype

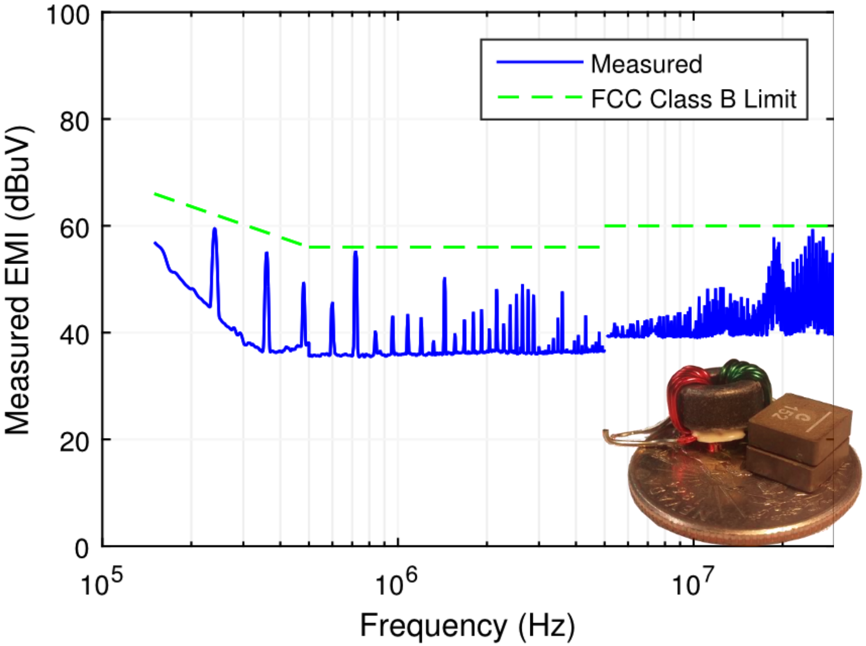


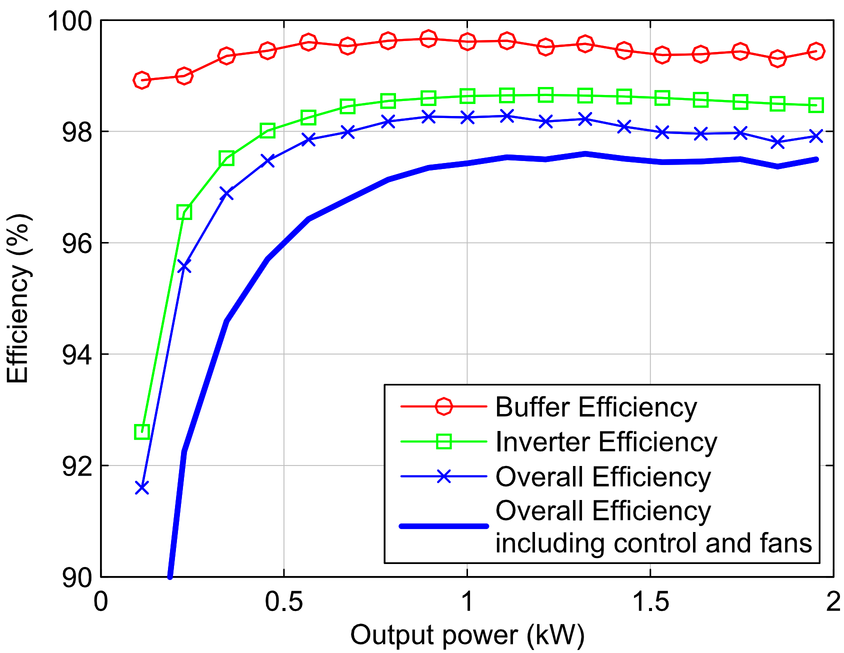


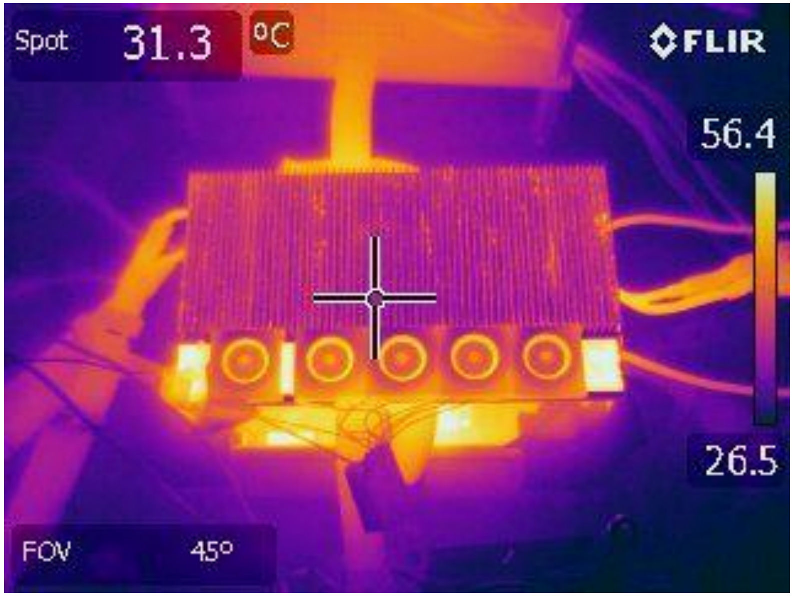
Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao and R.C.N. Pilawa-Podgurski “A 2 kW, Single-Phase, 7-Level, GaN Inverter with an Active Energy Buffer Achieving 216 W/in^3 Power Density and 97.6% Peak Efficiency”, IEEE Applied Power Electronics Conference, Long Beach, CA, 2016

Experimental Results

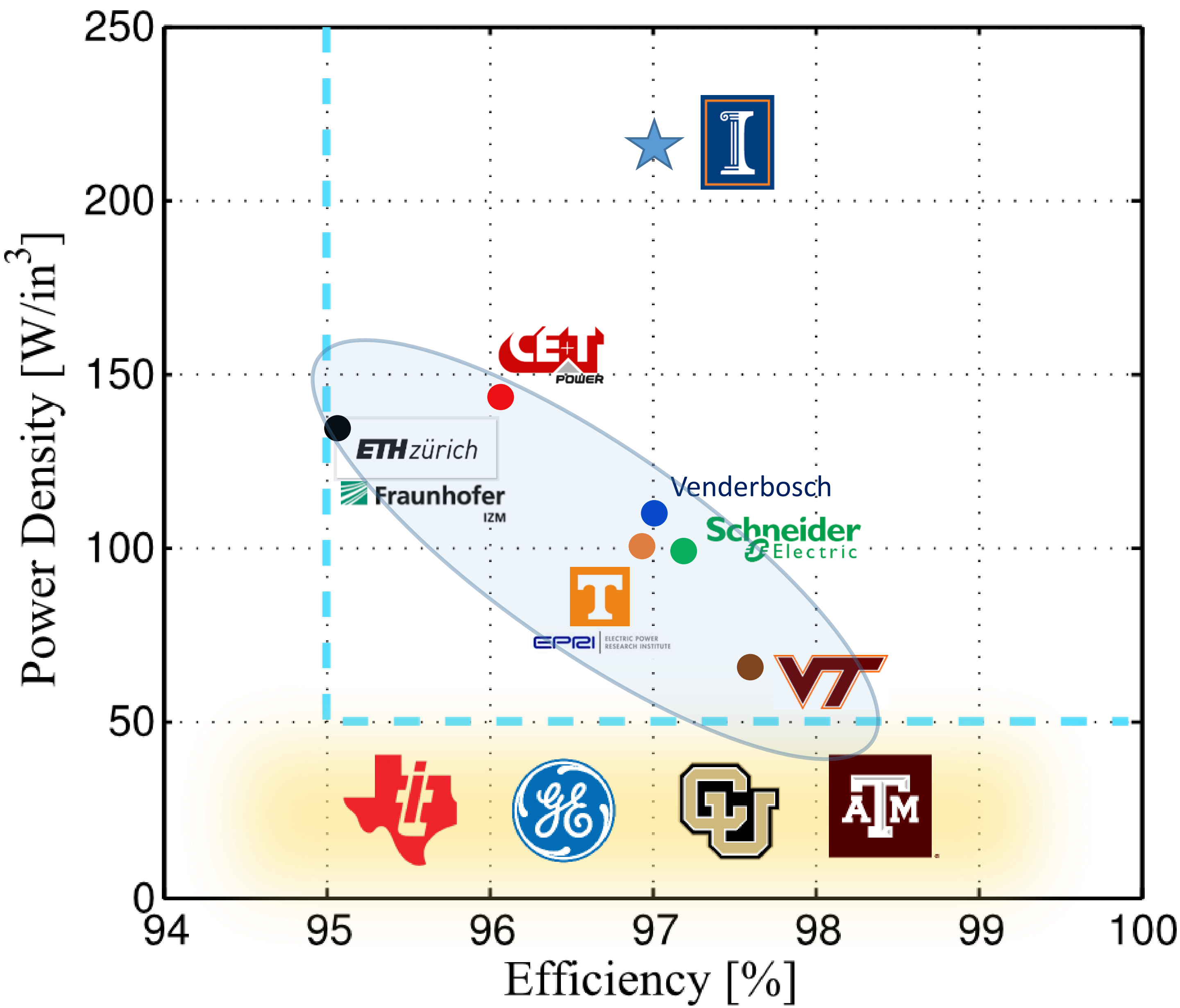




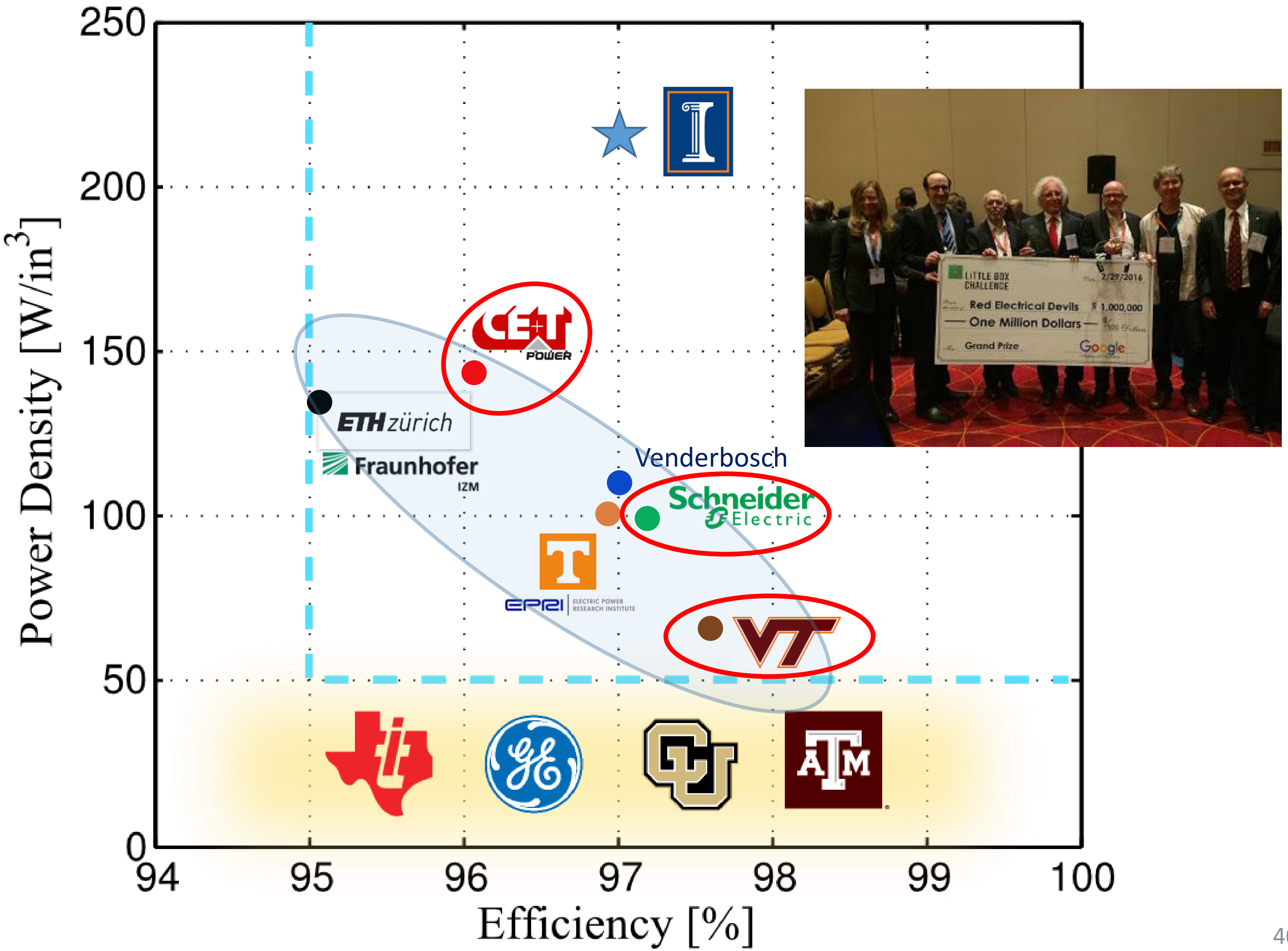




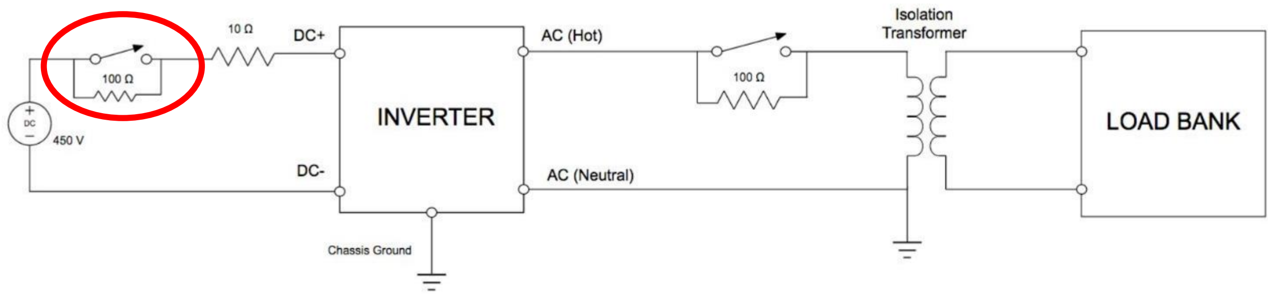
Little Box Finalists' Symposium

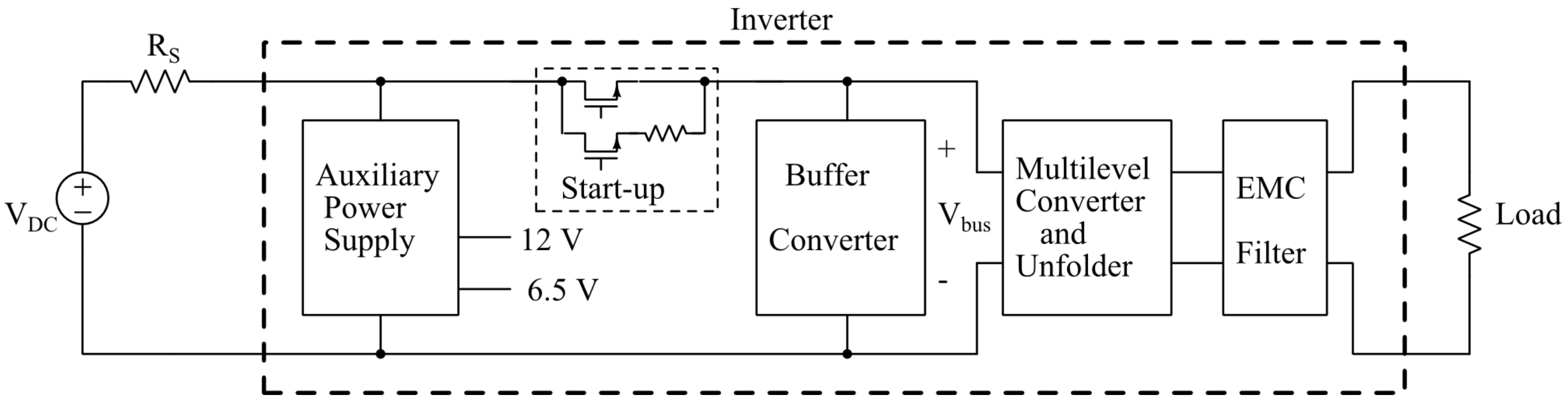


After NREL Testing



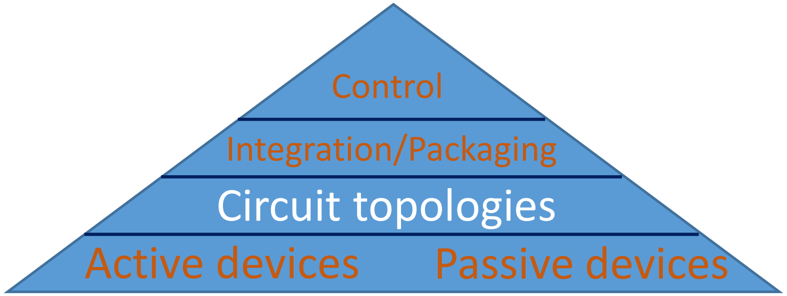
NREL Testing Details





Research Impact

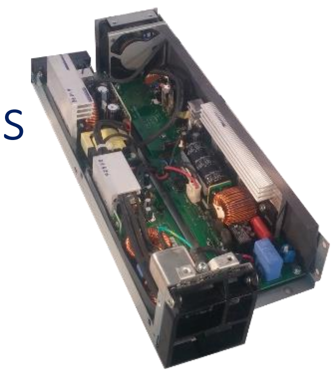
- Demonstrated the feasibility of multi-level flying capacitor power converters at kW-scale
- Achieved significant performance improvements compared to state-of-the-art
  - Integration
  - Digital control
  - Device utilization
    - GaN transistors
    - Multi-layer ceramic capacitors

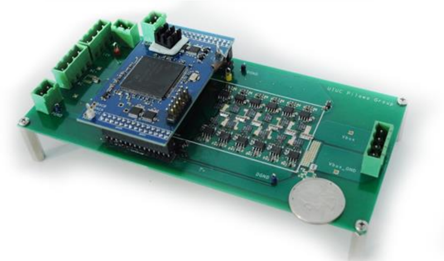


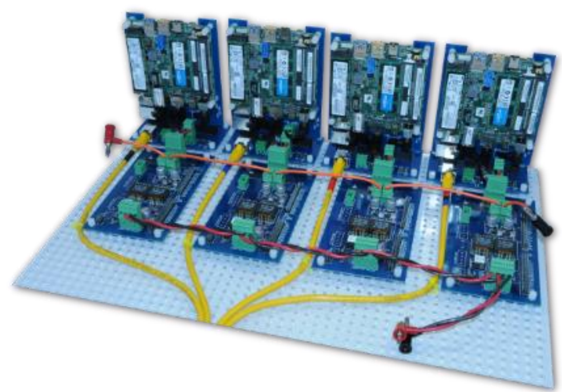
Laid the foundation for several promising future research areas

New Applications

- Electric vehicles
  - Bidirectional chargers (6.6 kW)
  - On-board dc-dc (50 kW)
  - Superchargers (150 kW)
- Consumer electronics
  - Ultra high efficiency power supplies for datacenters
  - LED lighting
  - Chargers
- Renewable integration
  - Grid-scale storage

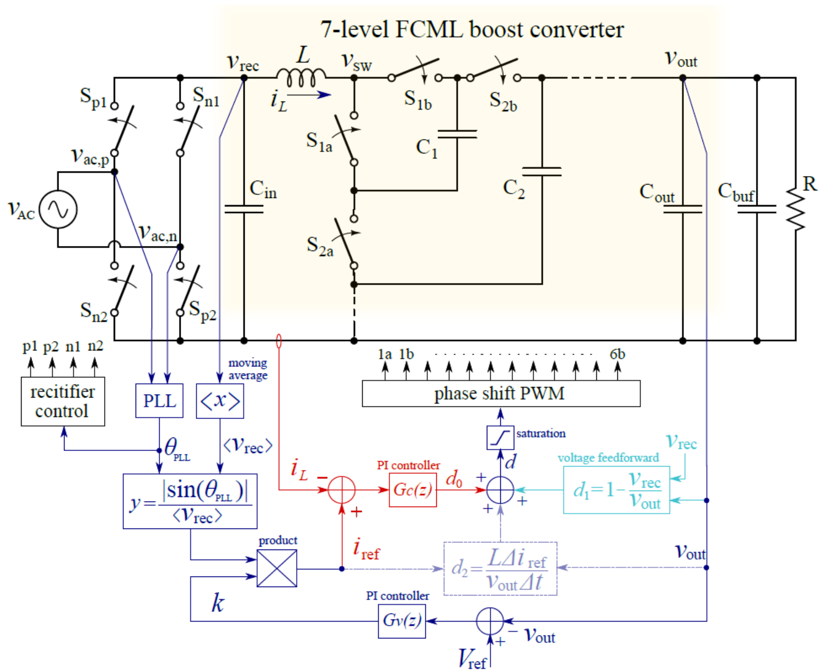




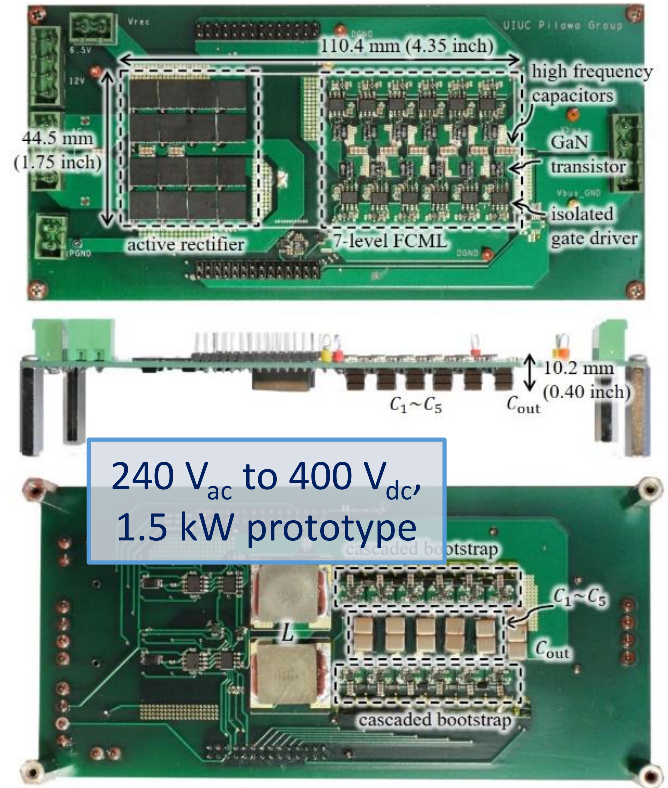


Specific Example: AC-DC PFC

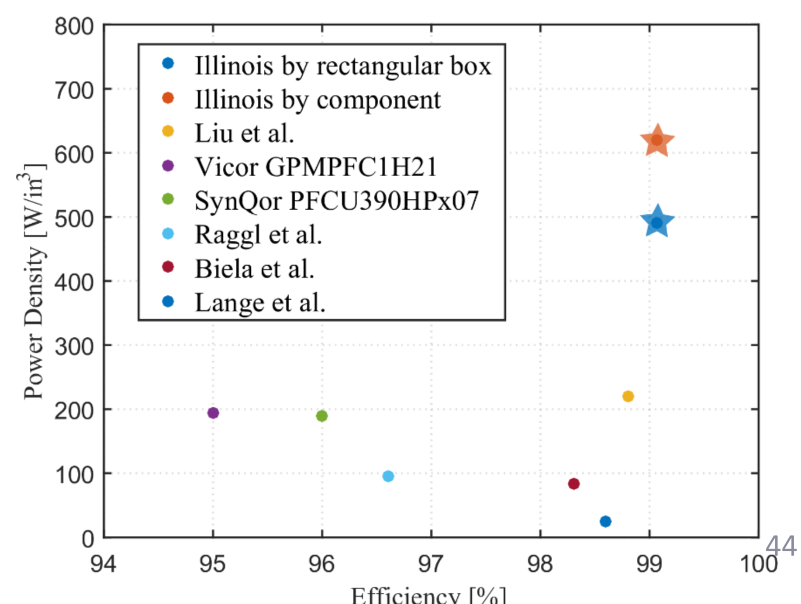
- Power factor correction (PFC) front-end
  - Datacenter applications (server)
  - EV charging
  - Any high power, single-phase grid connected device



Liu et al., Design of GaN-based mhz totem-pole PFC rectifier, JESTPE 2016
Raggl et al., Comprehensive design and optimization of a high-power-density single-phase boost pfc," TIE 2009.
Biela et al., Optimal design of a 5kw/dm3 98.3% rectifier," ECCE ASIA 2010
Lange et al., Three-level single-phase bridgeless pfc rectifiers," TPELS 2015

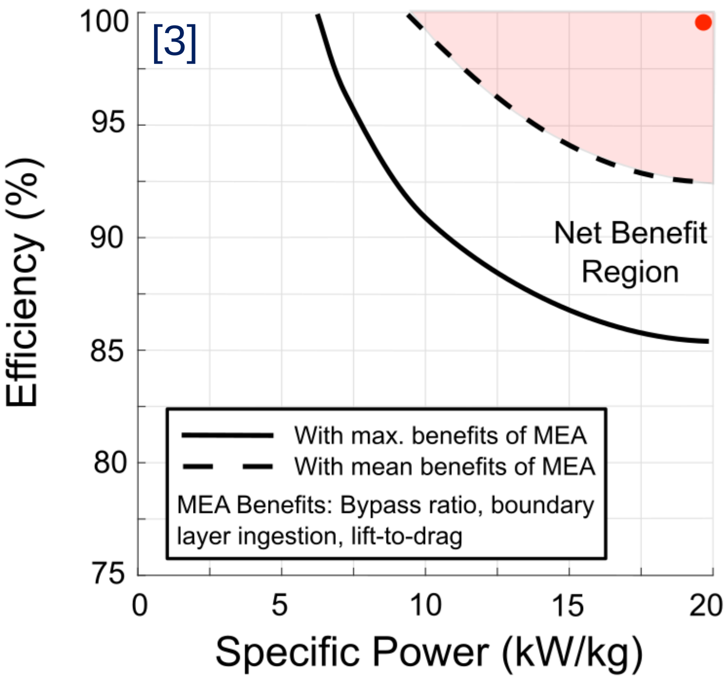


240 V_{ac} to 400 V_{dc}, 1.5 kW prototype



DC-AC Power Conversion for Electric Transportation

Aviation is the Last Horizon of Hybridization



NASA Roadmap for MEA for 2025 [2]:

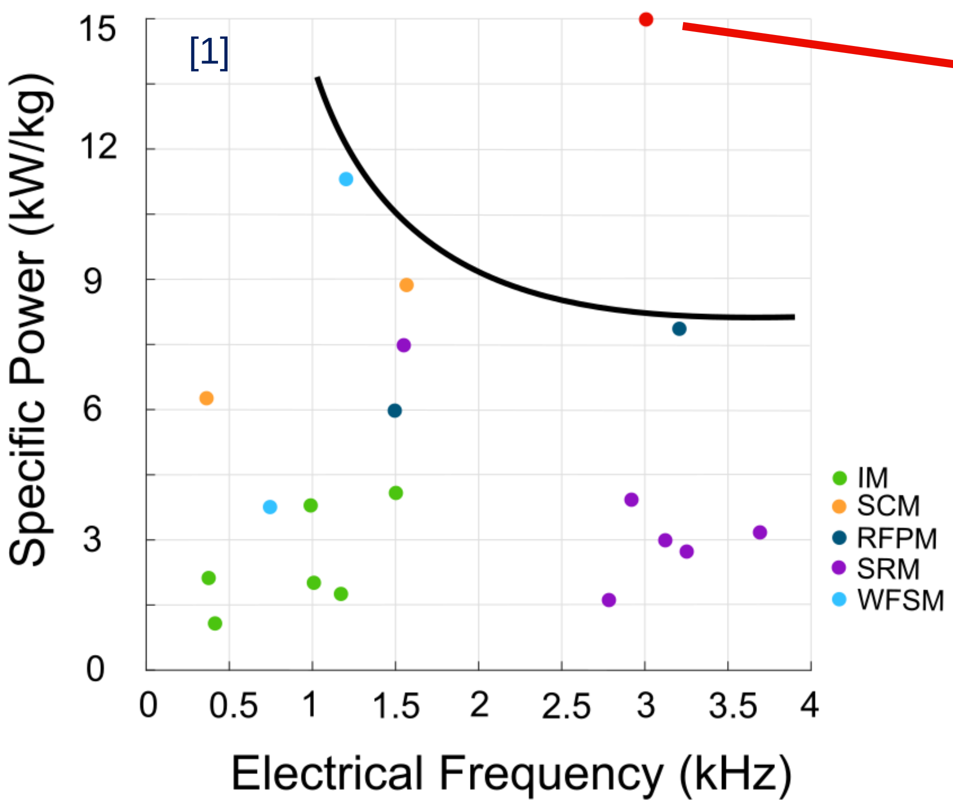
- Reduce landing/takeoff NOx emissions by 80%
- Reduce cruise NOx emissions by 80%
- Reduce fuel consumption by 60%
- Develop X-Plane concept aircraft

Obstacles for Electrifying Aircraft

- Electric and turbo-electric aircraft propulsion requires both very high efficiency and low weight

[1] NASA press release “NASA Electric Research Plane Gets X Number, New Name” (June, 17 2016)
[2] N. Madavan et al., “A NASA Perspective on Electric propulsion technologies for commercial aviation” April 2016
[3] Jansen, Ralph H., et al. "Turboelectric Aircraft Drive Key Performance Parameters and Functional Requirements." (2015).

High Specific Power, Low Inductance Motor



University of Illinois at Urbana-Champaign
1MW Outer-Rotor PMSM Architecture

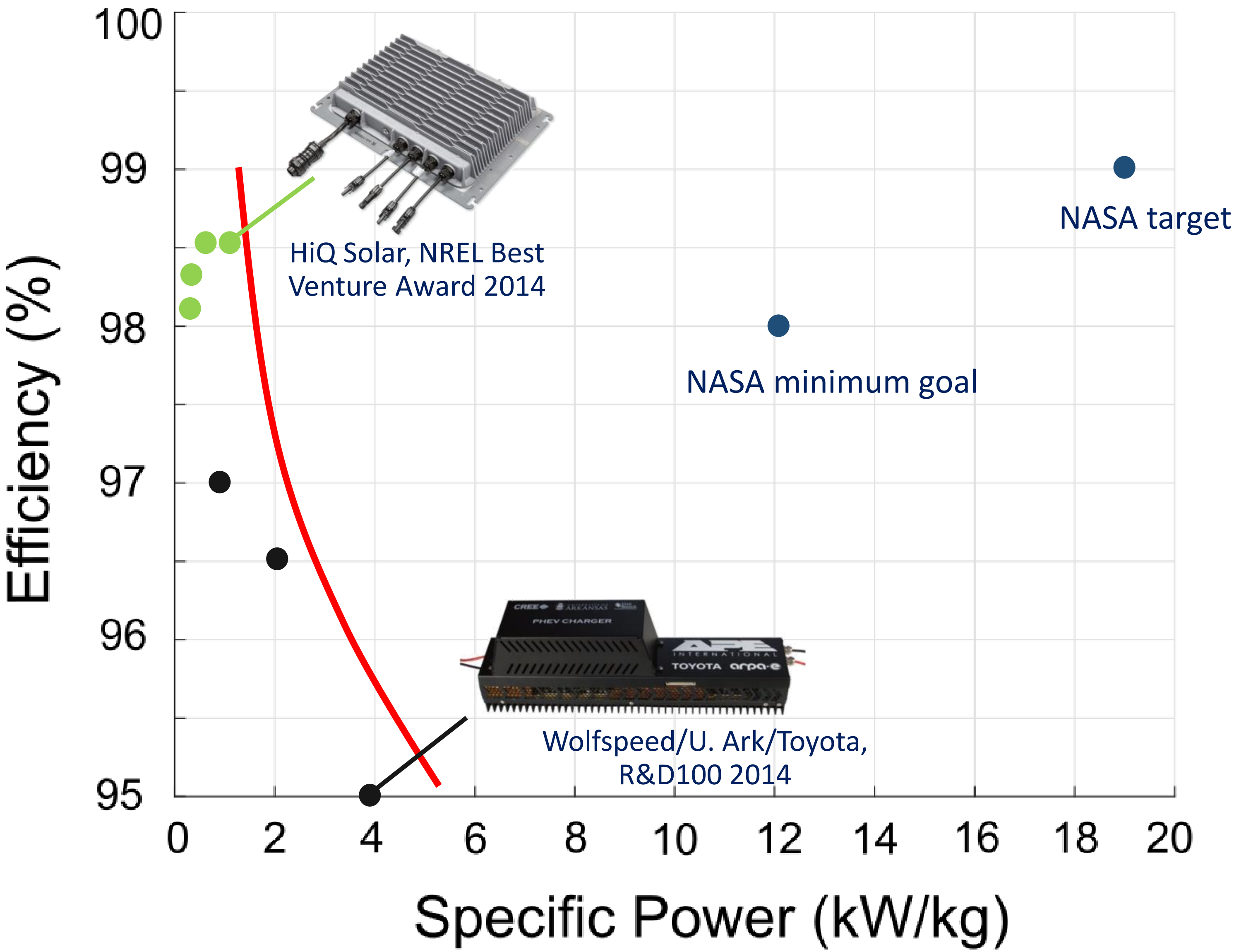
- Rated Power = 1 MW
- Rotational Speed = 14,000 RPM
- Pole Count = 20
- Electrical Frequency = 3 kHz
- Specific Power 15 kW/kg

Inverter Requirements:

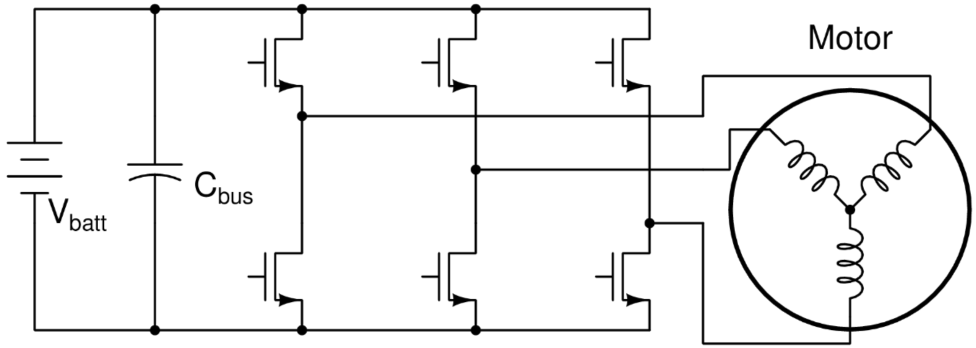
- Maintain high efficiency & specific power for high fundamental frequency (3 kHz)
- Provide sinusoidal voltage with low distortion since machine is ultra-low inductance (minimal iron)

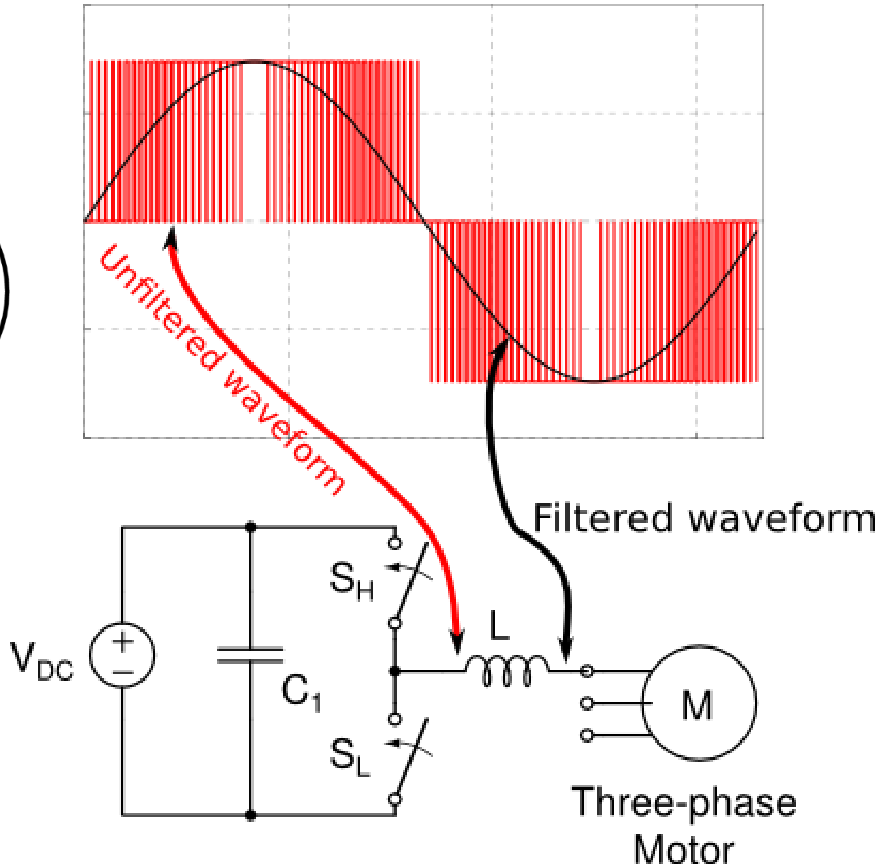
[1] Zhang et al., “High-specific-power electric machines for electrified transportation - technology options,” IEEE ECCE 2016

Aircraft Power Density/Efficiency Challenges



Conventional Solution

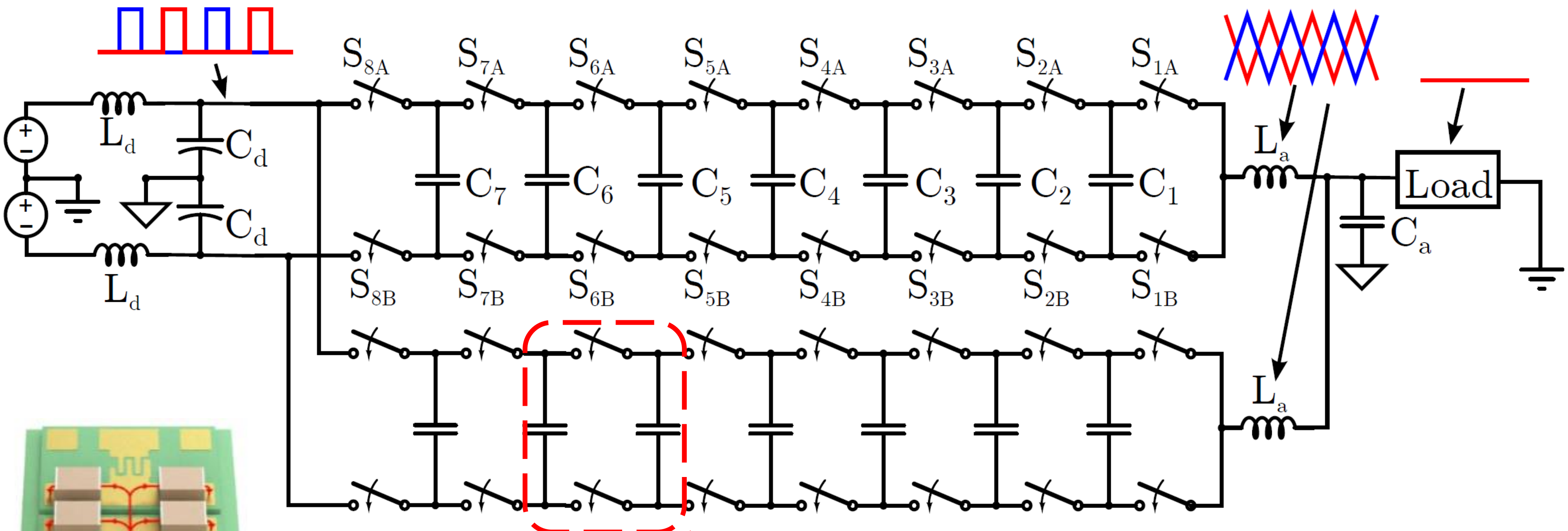


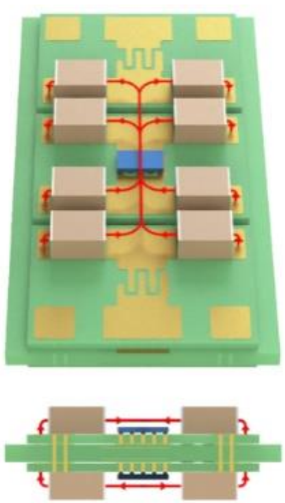


Achieving extreme power density through removal of all iron
-> very low inductance machine

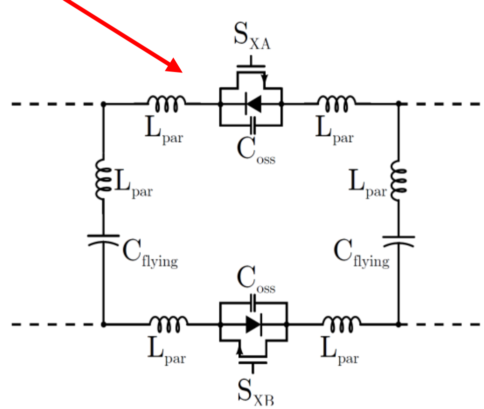
Our approach, 9-level FCML converter

- Each module contains two interleaved inverters.

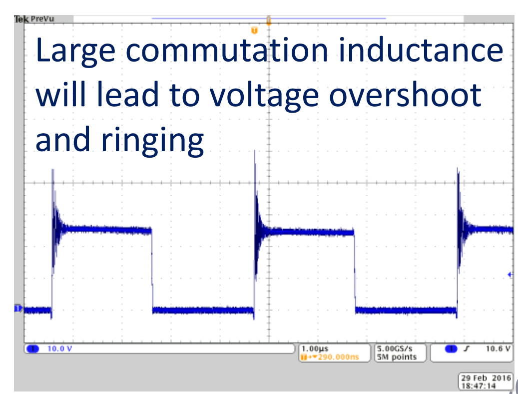




Double-sided integrated switching cell

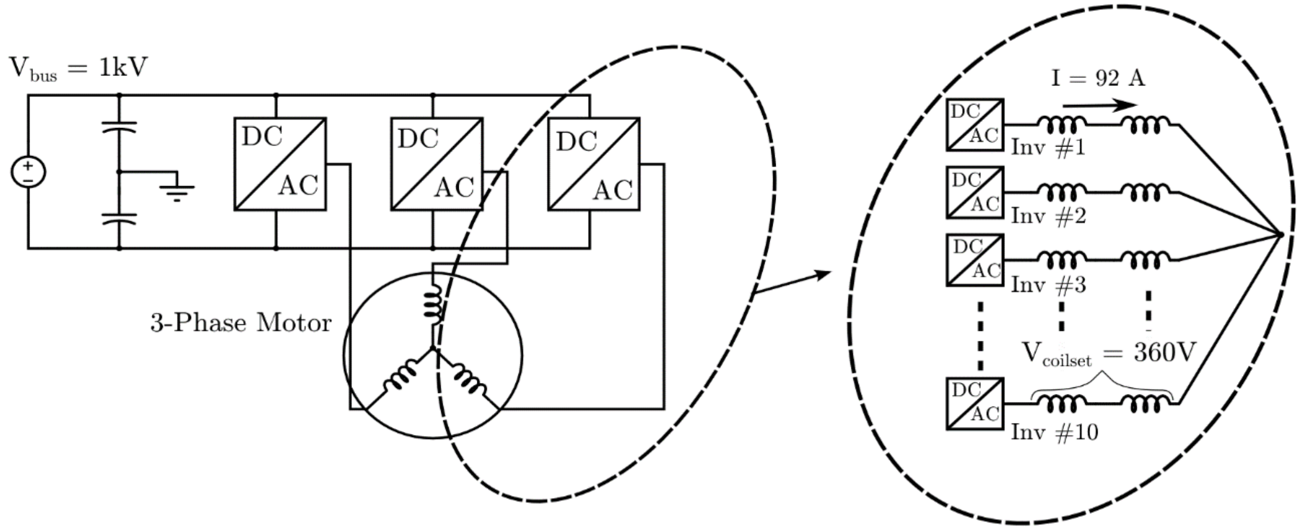


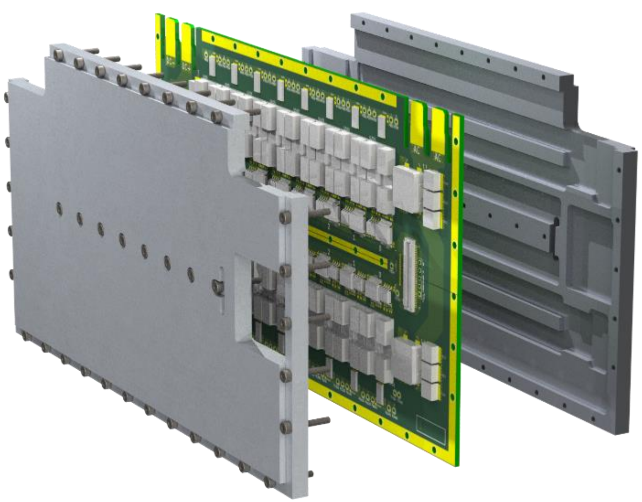
Inverter commutation loop



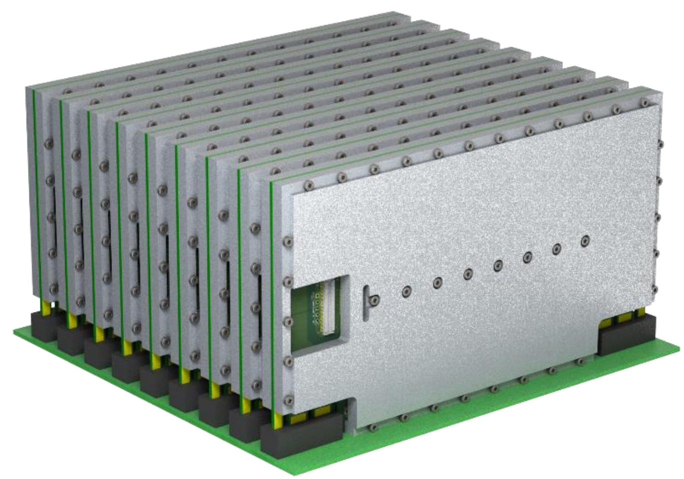
Modular FCML-based Inverter

- Modular Inverter Configuration





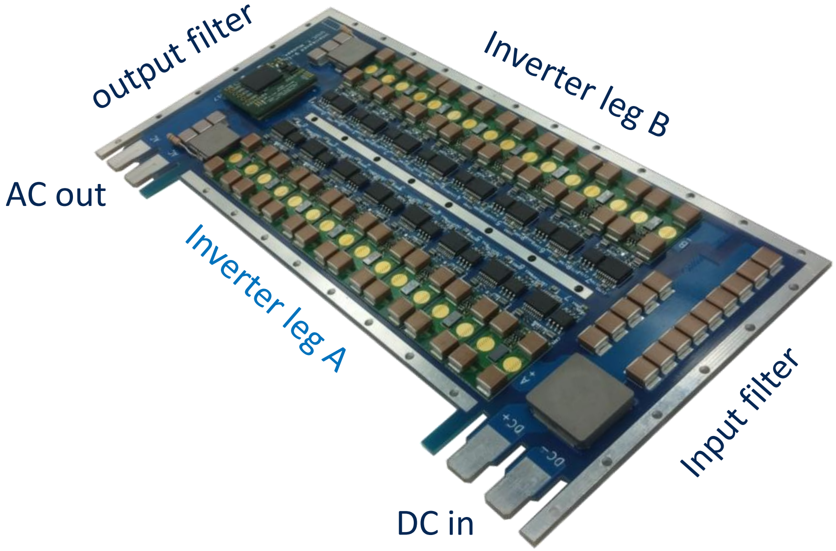
9-24X

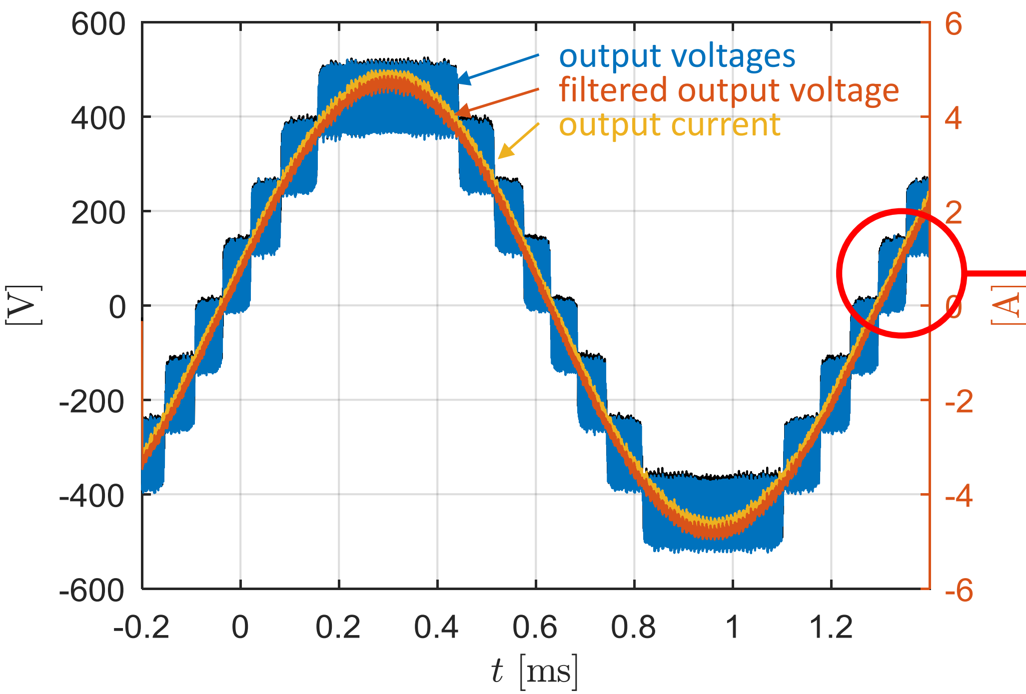


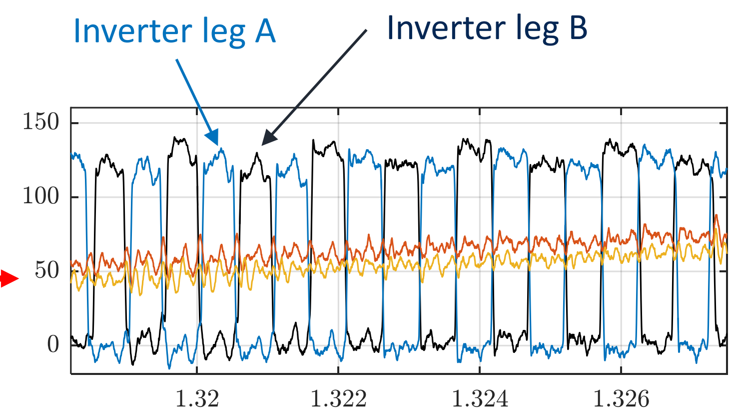
Double Interleaved Module

200kW inverter

Experimental Results, 9-level Interleaved FCML





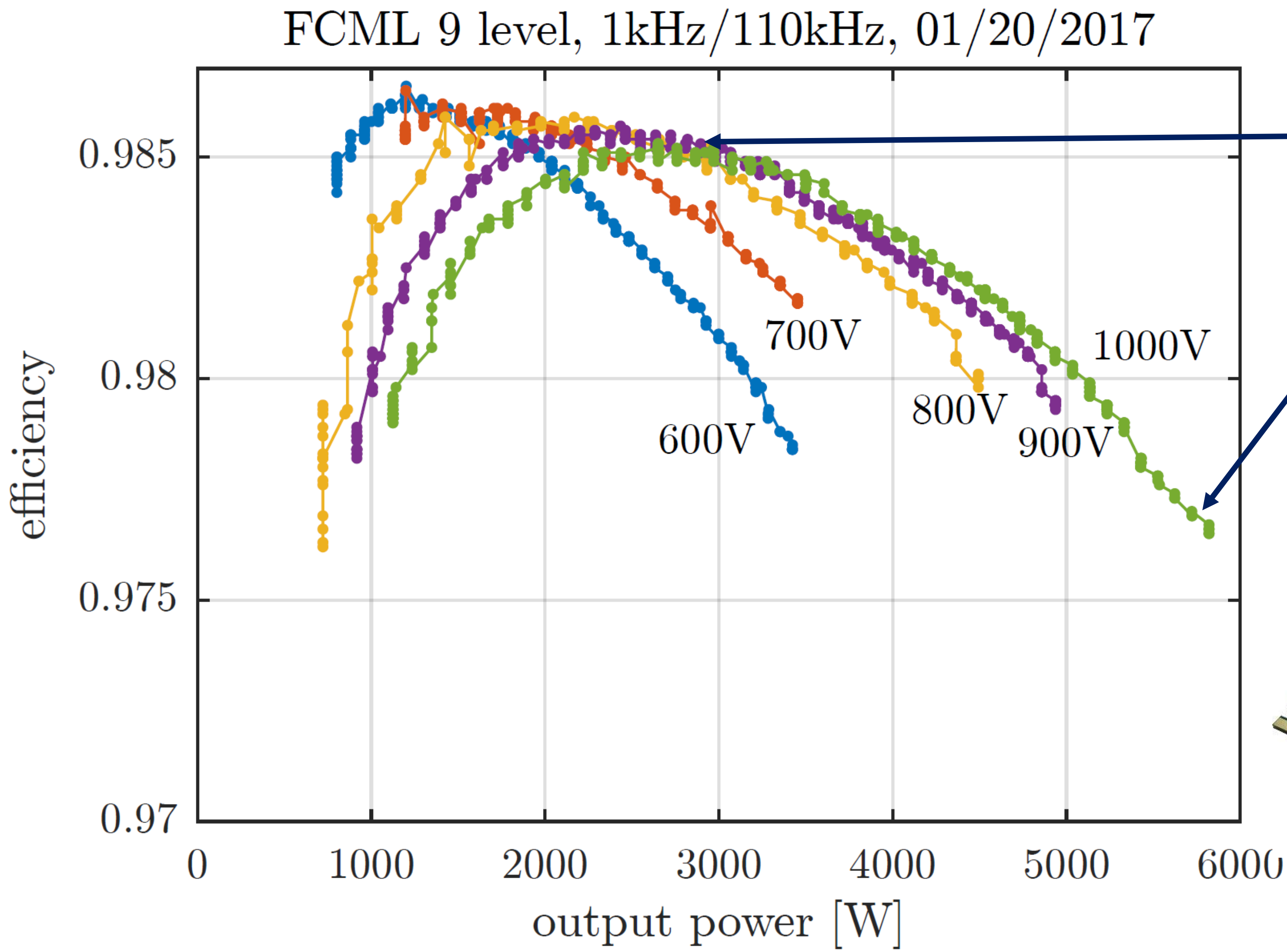


In: 1000V dc

Out: 345V_{rms}, 1.2kW, 750 Hz

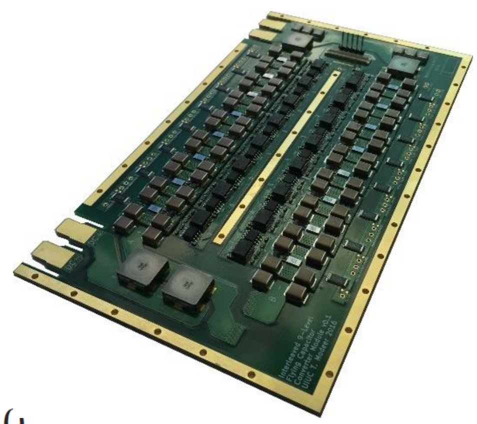
98.5% at 120kHz switching frequency

Efficiency – Single FCML Leg



Peak efficiency at 98.5% and 3kW

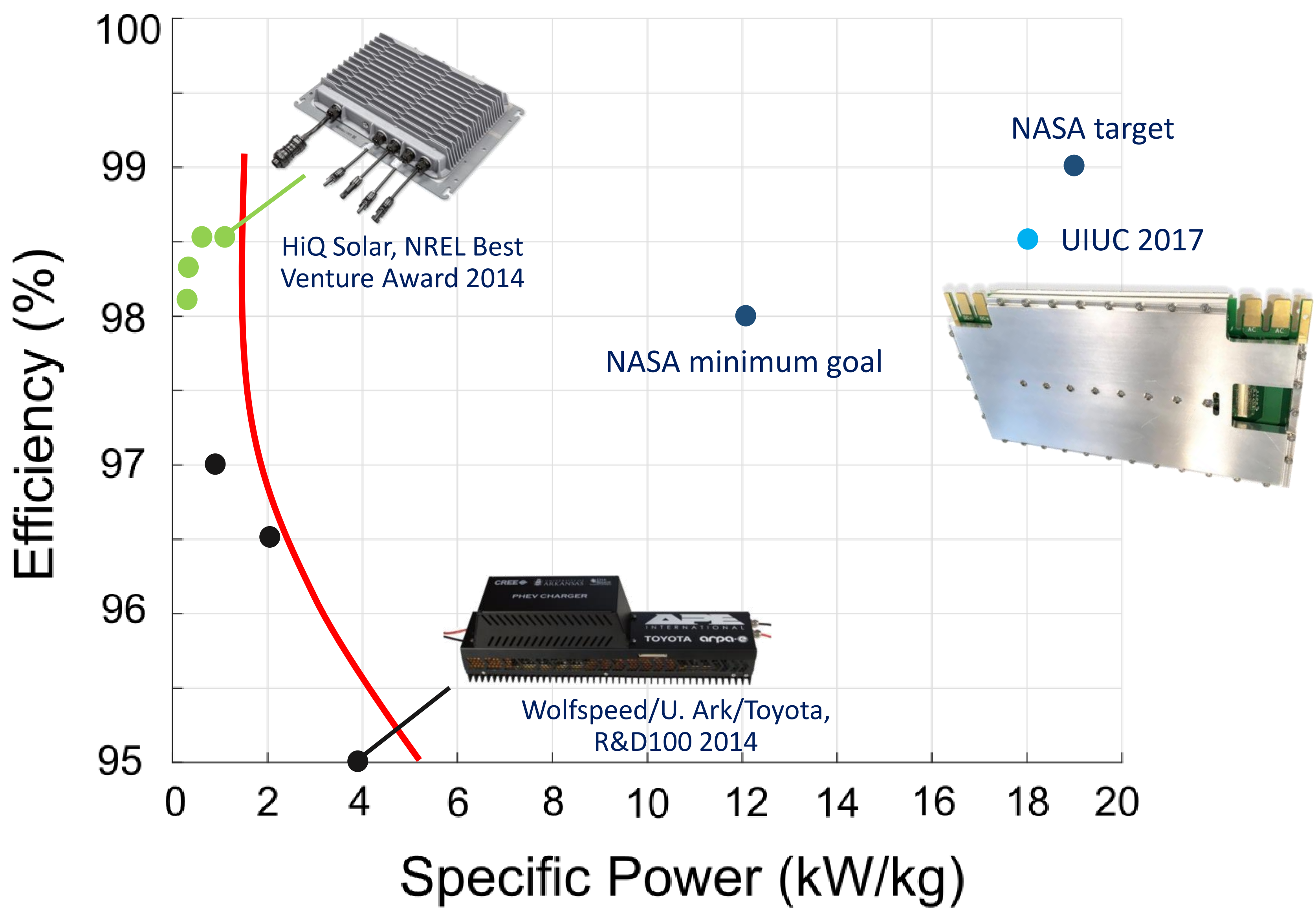
Close to Rev. 0 thermal limit.



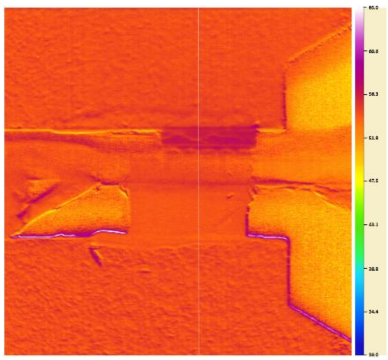
Target: efficiency ≥99.0% at 4.2kW (12 modules @16.7kW)
or at 5.6kW (9 modules @22.2kW)

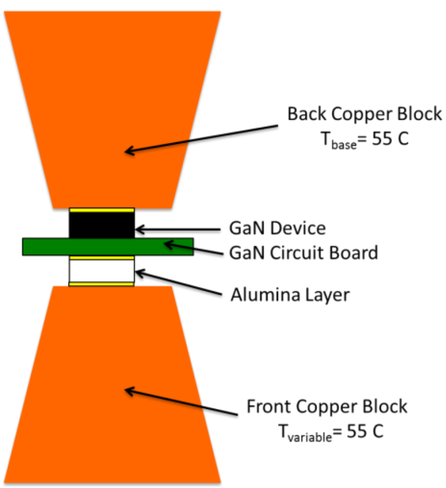
[1] T. Modeer, C. Barth, N. Pallo, W.H. Chung, T. Foulkes, and R. Pilawa-Podgurski, *Design of a GaN-based, 9-level Flying Capacitor Multilevel Inverter with Low Inductance Layout*, in Applied Power Electronics Conference and Exposition (APEC), 2017.

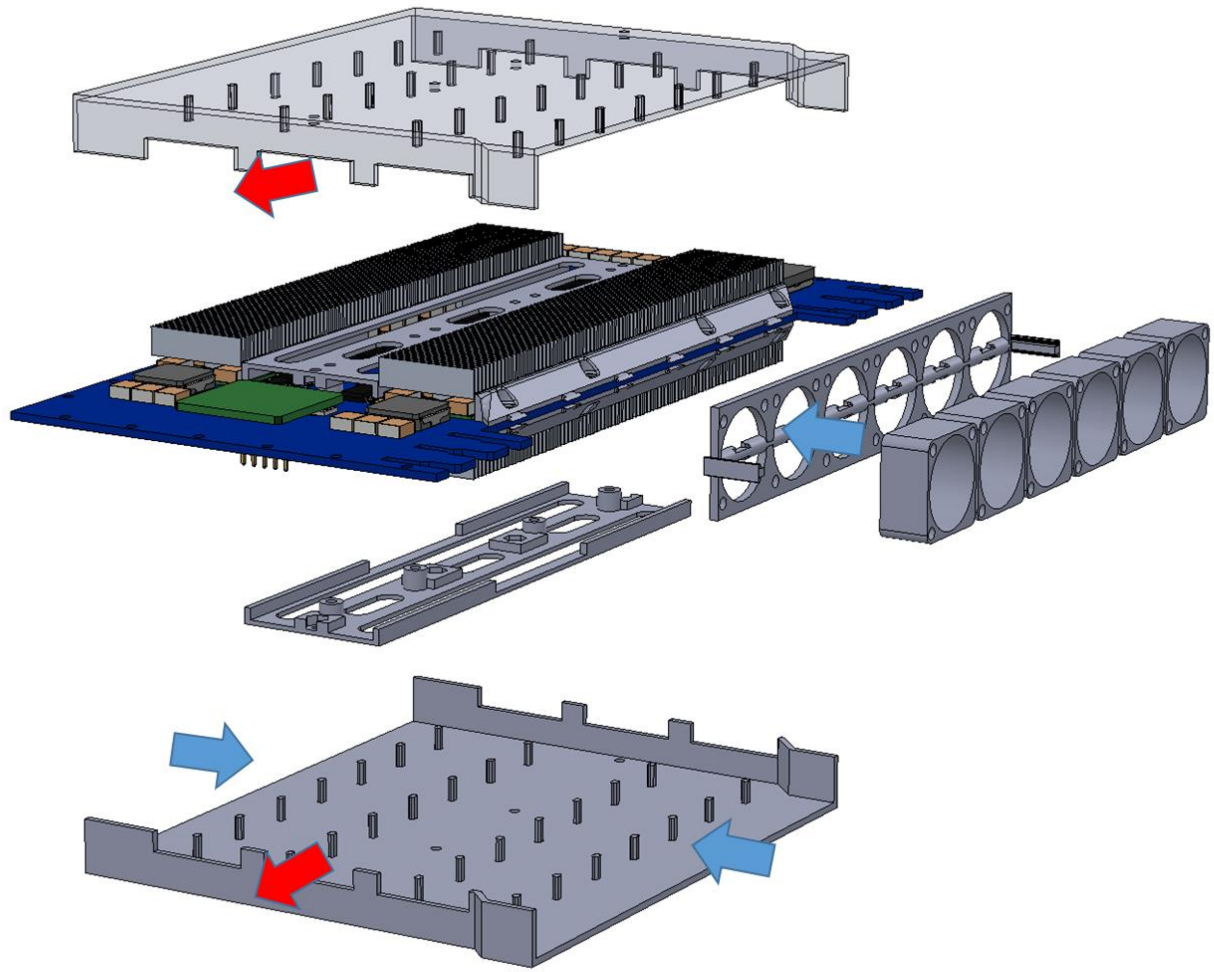
Performance Evaluation



Heatsink Optimization

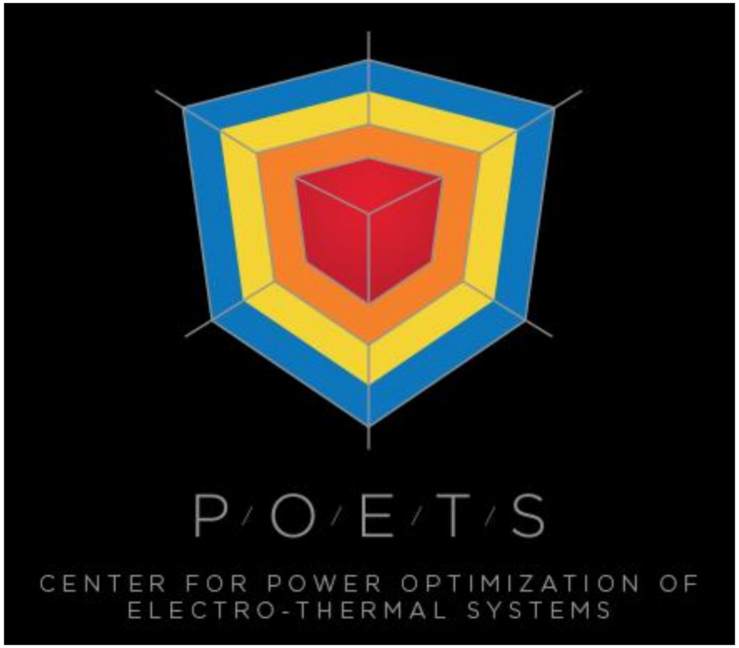


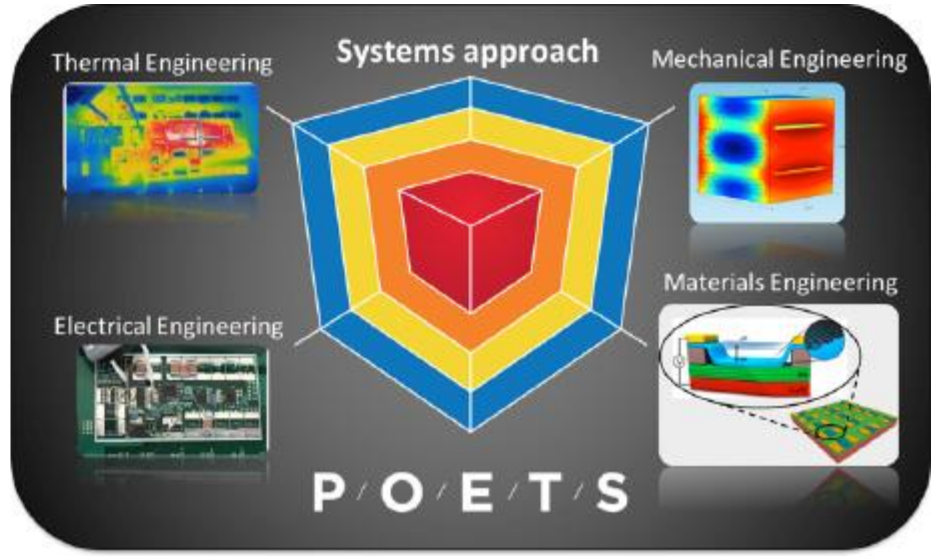




- Work in collaboration with Ken Goodson at Stanford

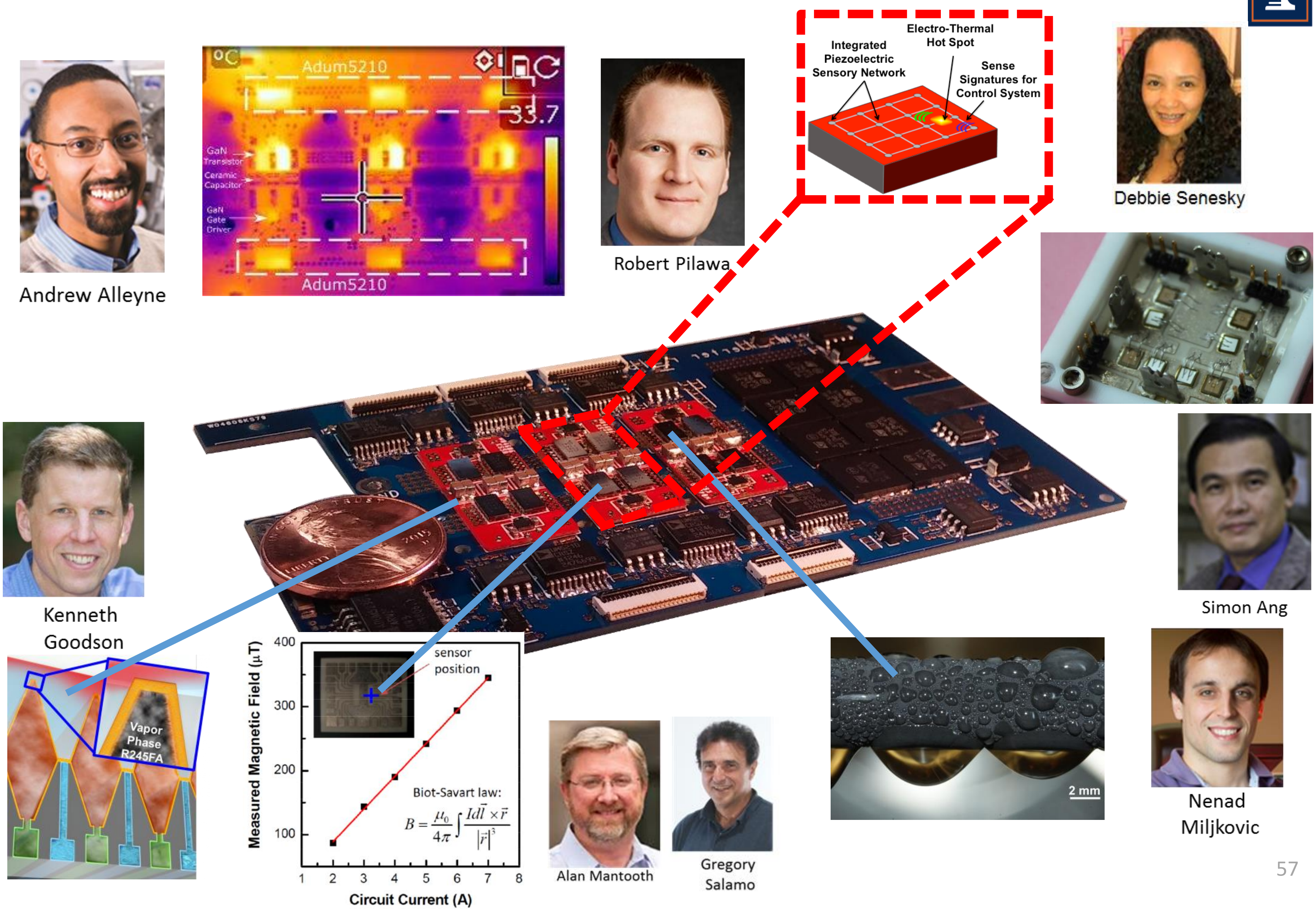
Interdisciplinary Research Challenges



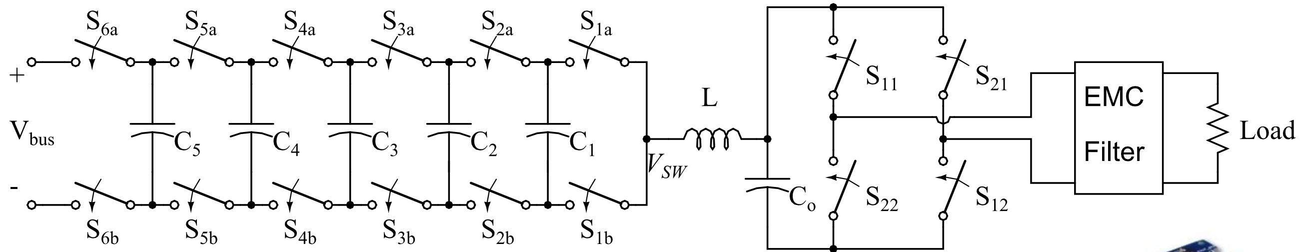


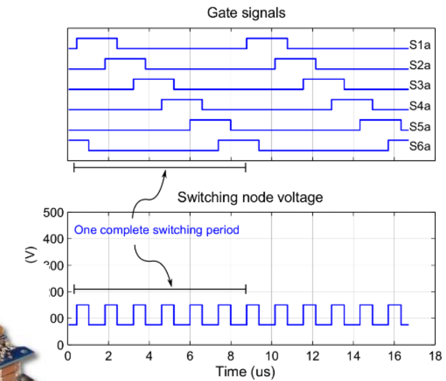
5-year, $4M/year NSF-funded Engineering Research Center, with Illinois, University of Arkansas, Stanford, and Howard University

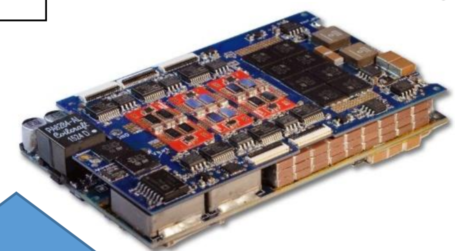
Interdisciplinary Research Examples

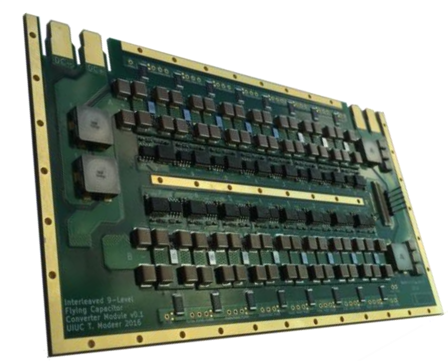


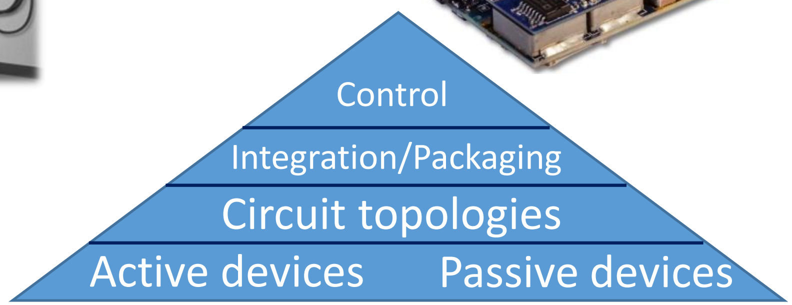
Conclusions

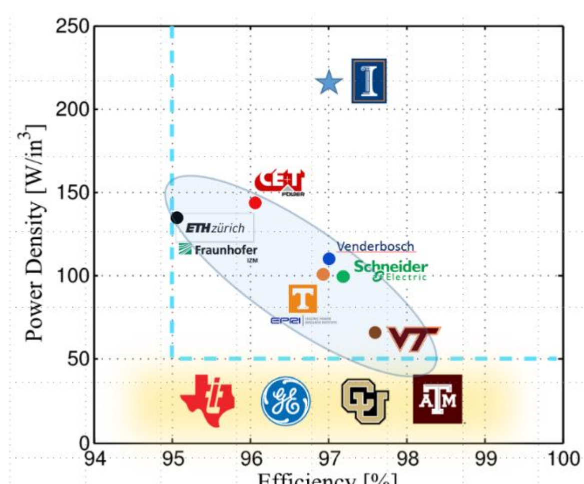


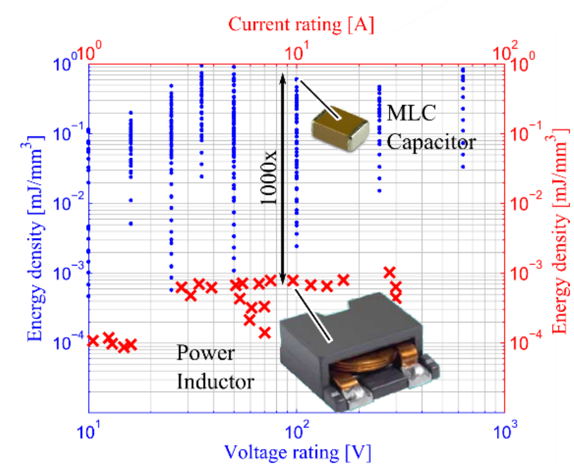












Acknowledgments

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UNITED STATES AIR FORCE

NASA

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