Today’s Virtual Seminar:

“Integrated Power – A Virtual Panel Session”

Steve Allen – pSemi (a Murata Company)
Wonyoung Kim – Lion Semi
Stephen Oliver – Navitas
Noah Sturken – Ferric
Kirk Bresniker – HP Labs / HPE

Intro and talks start at 4:30pm.

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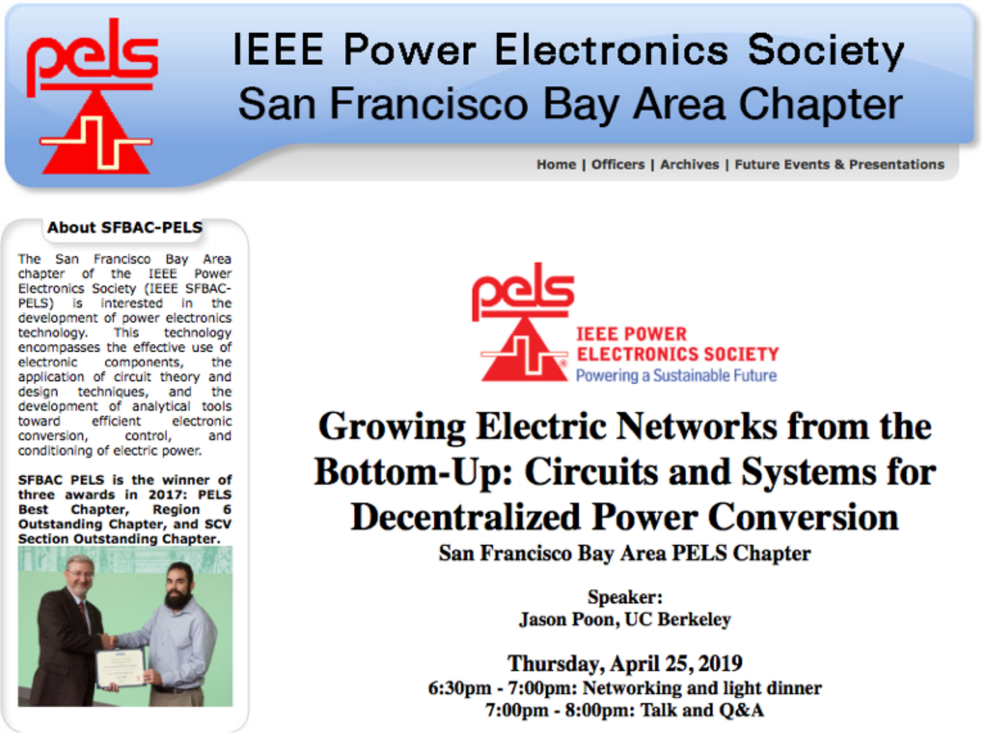
LION
SEMICONDUCTOR

Check out our website:

http://ewh.ieee.org/r6/scv/pels/index.html



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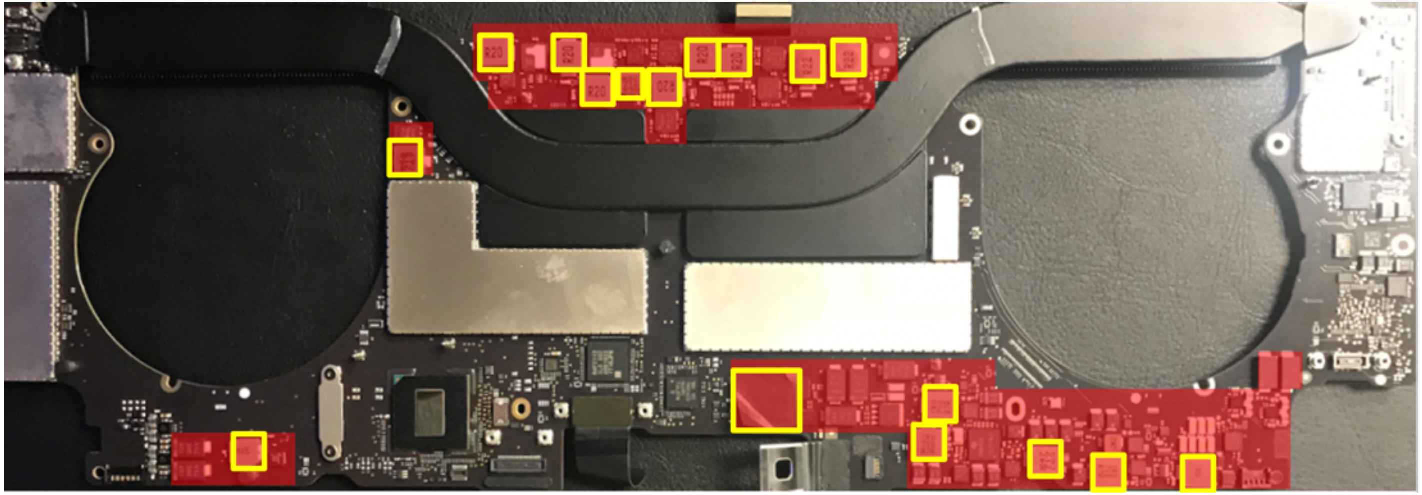
Go BIG!
....by Going Small

Architectural innovation using hybrid architectures accelerates the role of 3D packaging in power conversion to shrink form factors and improve performance

Stephen J Allen

PELS/IEEE 22nd October 2020

A Problem to Solve

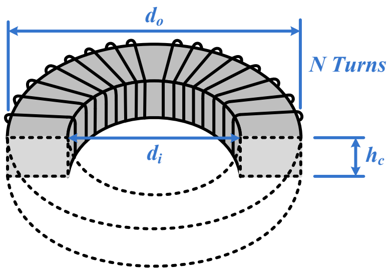


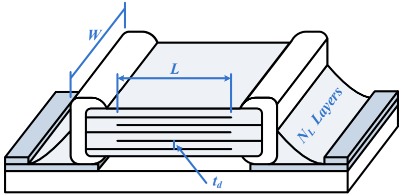
Power conversion can easily occupy 25-30% of a circuit board

….as much as 55% in high performance platforms such core routing, 5G etc.

Inductors typically the largest footprint and highest single components

The Problem With Inductors





$$u_{L,\max} = \frac{0.53 M_{sat}^2}{2\mu_0}\left[\frac{\mu_r}{(\mu_r - 1)^2}\right] = 0.53 \times u_{m,\max}$$

$$u_{C,\max} = \frac{U_C}{vol_C} = \frac{P_{sat}^2}{2\varepsilon_0}\left[\frac{\varepsilon_r}{(\varepsilon_r - 1)^2}\right] = u_{e,\max}$$

ε_0 is ~142,000 times smaller than μ_0

Structure	Material	Param 1	Param 2	Energy Density
MLCC	Thick Film $BaTiO_3$	ε_r = 3500	P_{sat} = 0.165 C/m^2	439.51 μJ/mm^3
Toroidal	N40 (NiZn Ferrite)	μ_r = 15	M_{sat} = 0.270 T	1.1761 μJ/mm^3

You want low ε_r and μ_r

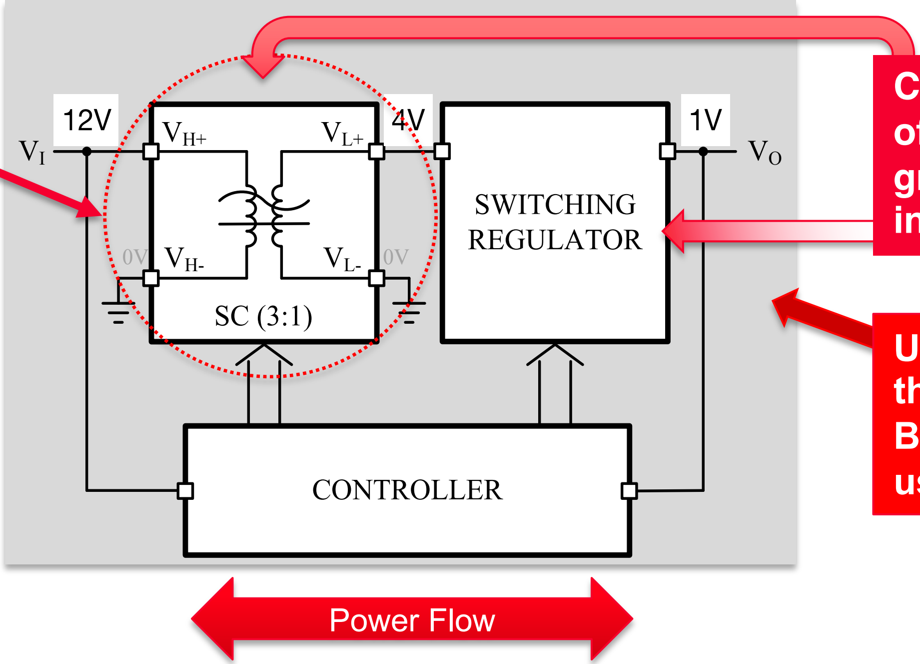
Capacitors have potentially 400x higher energy density compared with inductors

Using Architectural Innovation to Solve the 'Problem'

A highly flexible multi-stage architecture comprising a patented "pipeline" stage switched-capacitor network (charge pump) combined with either a buck or boost stage

Virtually lossless stage irrespective of conversion ratio!

Efficiency is largely independent of the difference between input and output voltage.

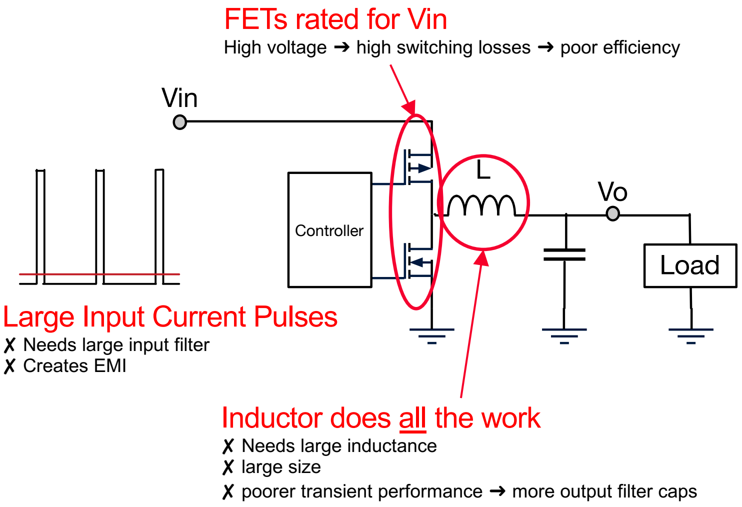


Capacitors do most of the work, enabling greatly reduced inductor sizing.

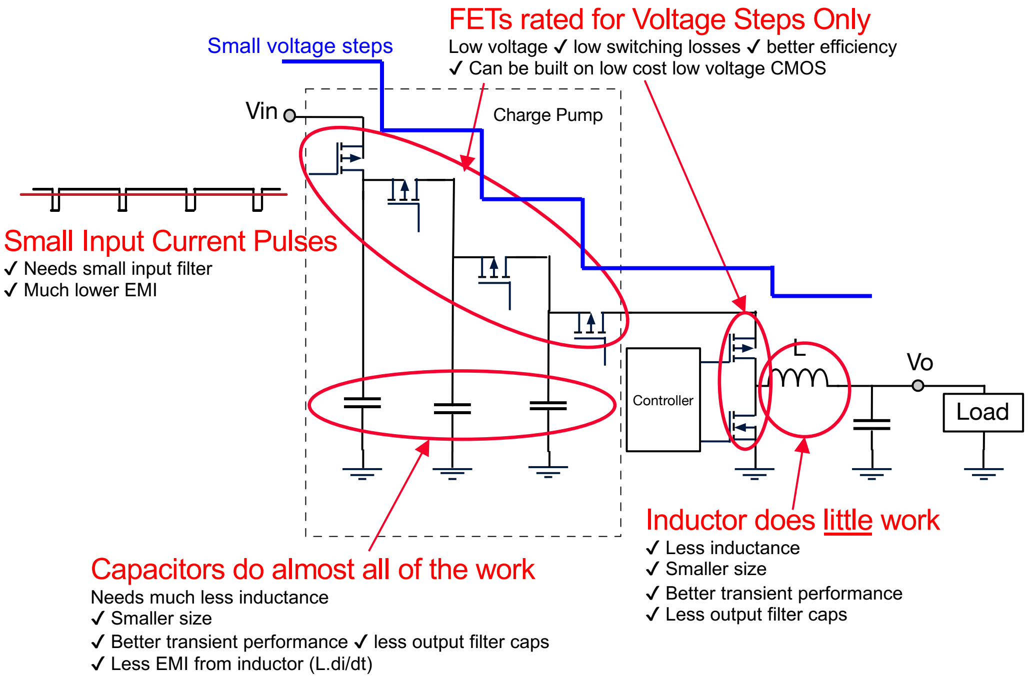
Uses low voltage FETs through the power train. Built on monolithic die using standard CMOS.

Conceptually

Traditional Solution

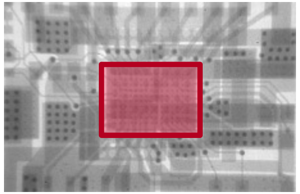


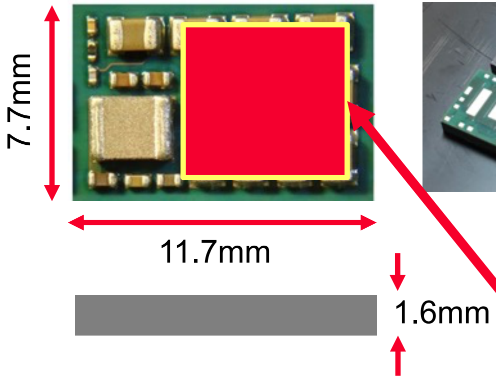
2-Stage Solution (simplified)

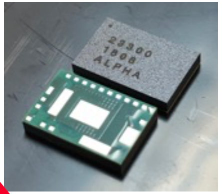


Example 1.
Small L = Increased Suitability for Advanced 3D Packaging

Smallest, fully integrated 10W LED Boost with highest efficiency at >92% over entire load range.

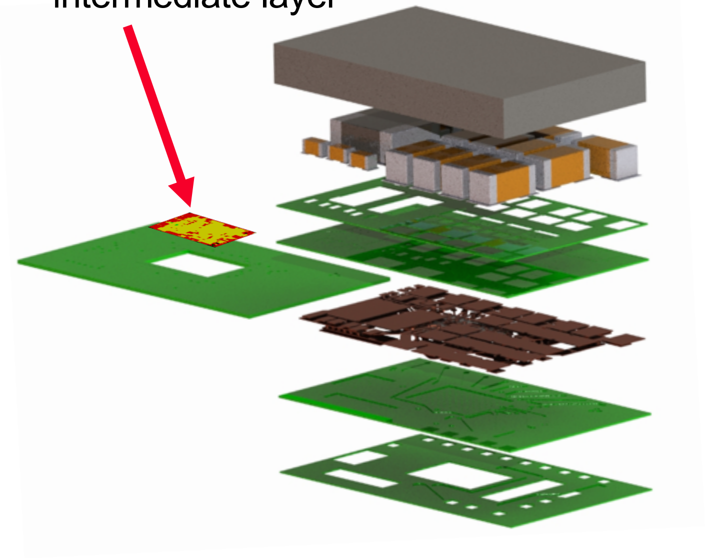






Traditional single stage architecture would need to use a 5x5mm 1.2mm high inductor to get to just 89% efficiency under same conditions.

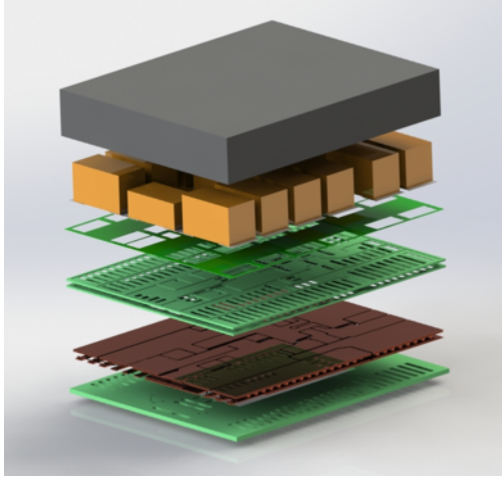
Die embedded in substrate in intermediate layer

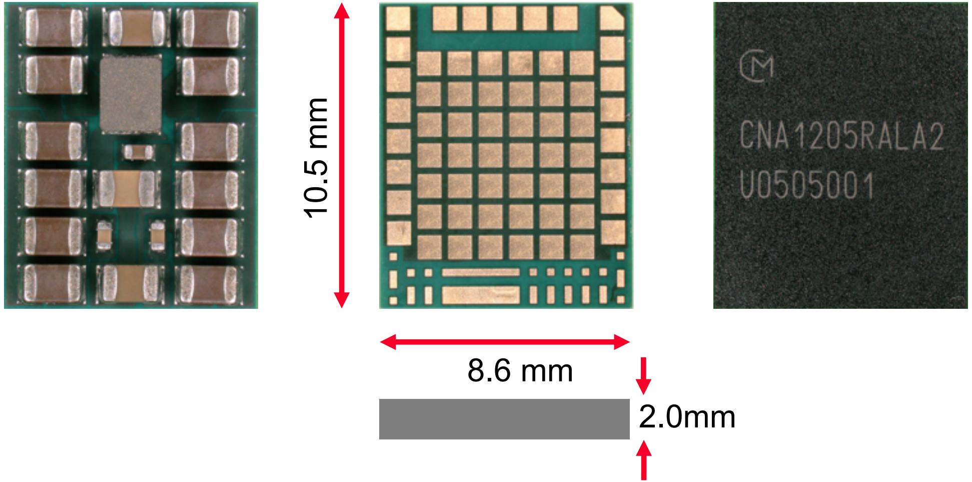


Copper plated direct to die.
No solder bumps on die.
Lowest possible parasitic losses.
Best possible thermal performance.

Example 2.
Using Capacitors + 3D Packaging for Maximum Power Density

72W 48V:12V Charge Pump





Die embedded in substrate in intermediate layer
Copper plated direct to die.
No solder bumps on die.
Lowest possible parasitic losses.
Best possible thermal performance.

Power density 398W/cm^3 (6.5kW/in^3)

Nearest comparable product in market:
17.34mm x 22.83mm x 7.417mm 720W
Power density 245W/cm^3 (4kW/in^3)

Conclusions

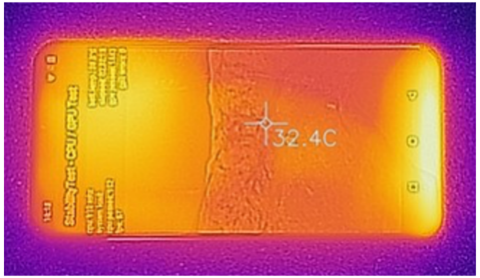
- 3D Packaging is here and becoming mainstream
- Getting the most benefit from 3D packaging requires power architectural innovation if not to trade off power performance
- Capacitive based architectures are gaining ground due to dramatically higher energy storage density possibilities.
- Scope for significant further improvements in passives (especially capacitors) provide opportunity for even smaller and more efficient products.

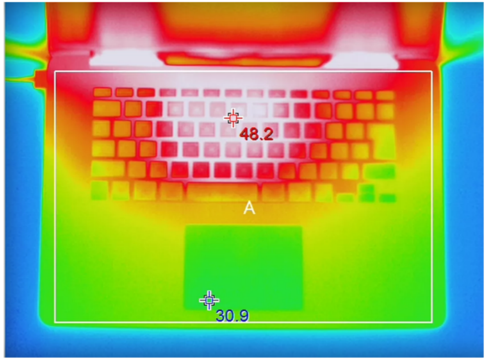
Thank You!

Switched-Capacitor Power ICs in Mobile Devices

Lion Semiconductor

Reducing Heat Dissipation is Key for Charger ICs and DC/DC Converters





Fast Charger IC

Charging speed throttles if heat dissipation is too high

DC/DC Converter

Processor speed throttles if heat dissipation is too high

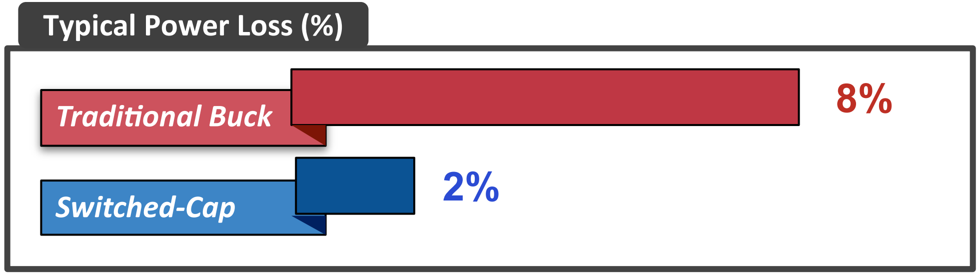
Nanjing Airport

Especially Important in Thermally Limited Mobile Devices

High Efficiency Switched-Cap Power ICs Offer Faster Charging and Longer Battery Use Time

Traditional Buck

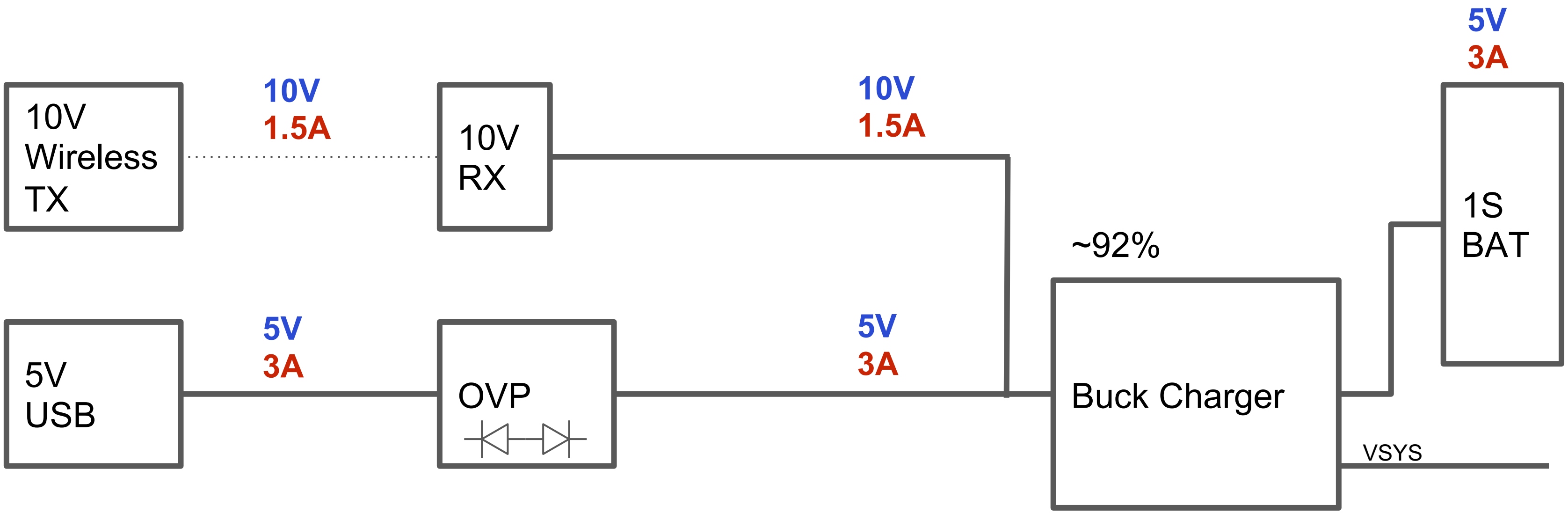
Switched-Cap



- Switched-Cap Power Loss is 1/4 of Traditional Buck
- 1/4 Heat Dissipation
  → **4x Faster Charging**
- 6pp Lower Power Consumption
  → **6% Longer Battery Use Time**
  → **Higher Processor Performance**

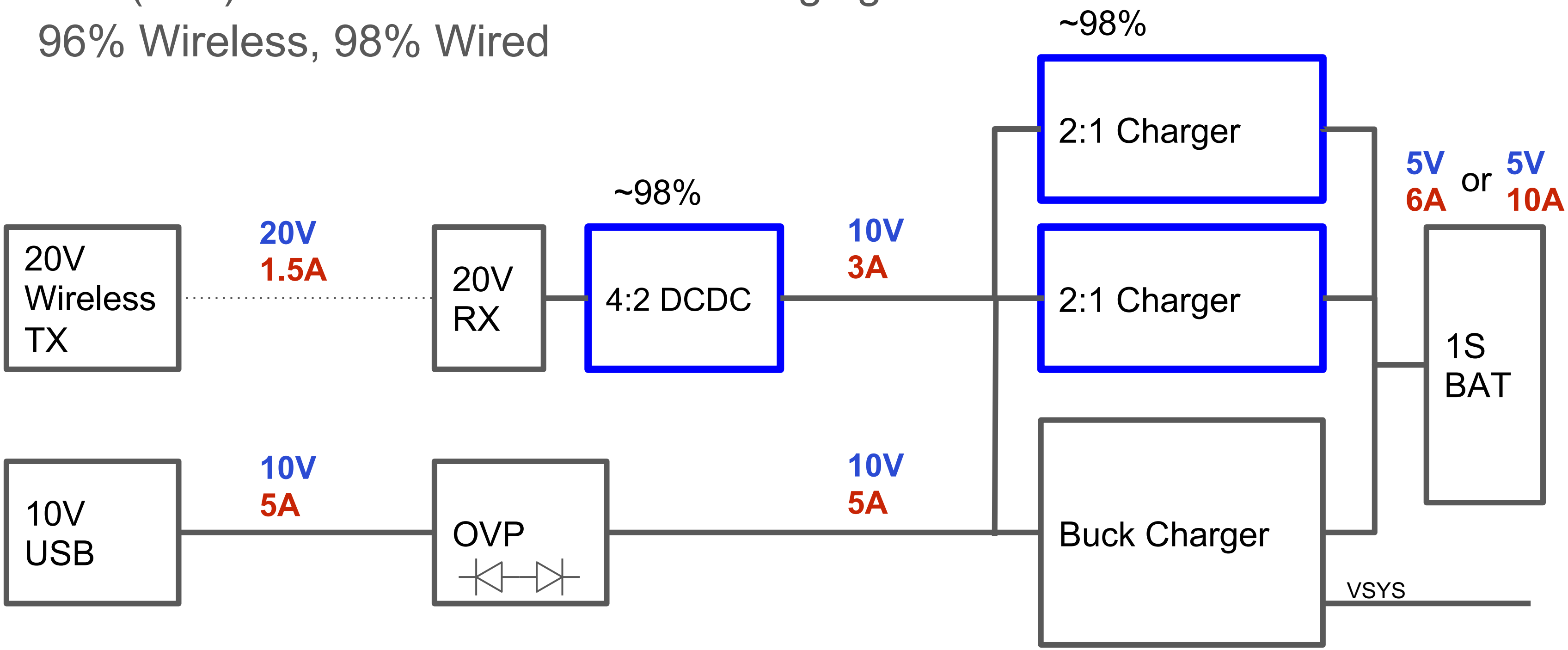
Traditional Charging Path Without Switched-Cap

- 15W(10V) Wireless + 15W Wired Charging
- 92% Efficiency for Wireless, Wired Charging



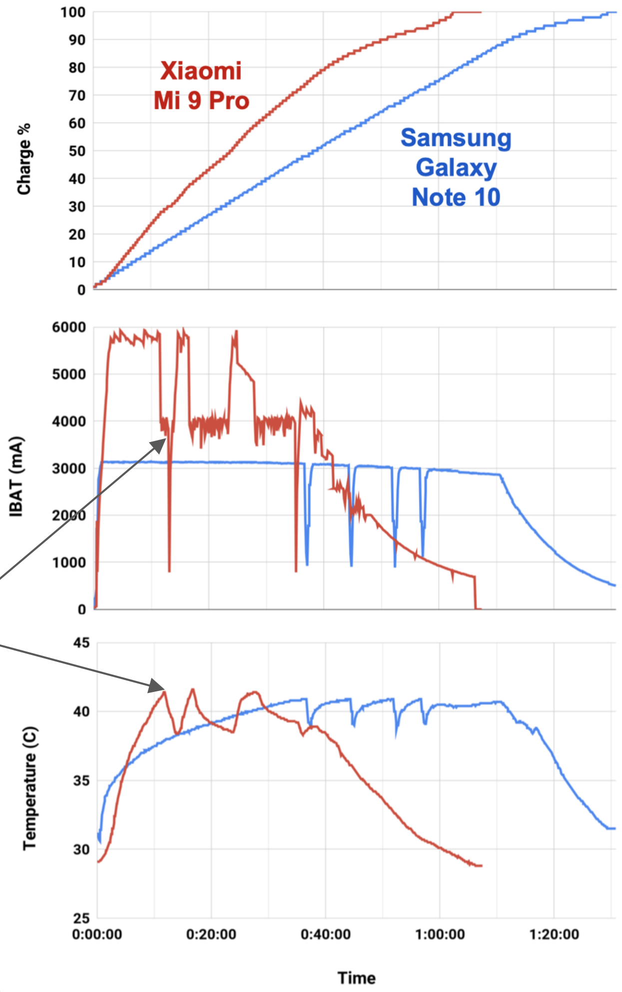
Example of New Charging System with Switched-Cap

- 30W(20V) Wireless + 50W Wired Charging
- 96% Wireless, 98% Wired



Xiaomi Phone with 98% Efficient Lion IC Enables Faster Wireless Charging

charging throttles when temperature reaches limit



Mobile Devices are Maximizing Efficiency with Switched-Capacitor Power ICs

- Maximize Efficiency by Minimizing # of Inductors in Power Path
  - 1 inductor for fine regulation. Bulk of the conversion done with switched-cap.
  - 20V buck → 4:1 switched-cap + 5V buck
  - e.g., AC/DC Wall Adapter with inductor provides regulation. Conversion inside mobile device all done with switched-cap.
- Switched-Caps are Widespread in Mobile Devices
  - Lion Semi shipped **70 million ICs** in past 2 years
  - Rapidy growing need for more advanced switched-cap topologies

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Navitas

GaNFast Power ICs: Integration is the Game-Changer

IEEE PELS / EPS Virtual Panel Session on Integrated Power

October 22nd, 2020

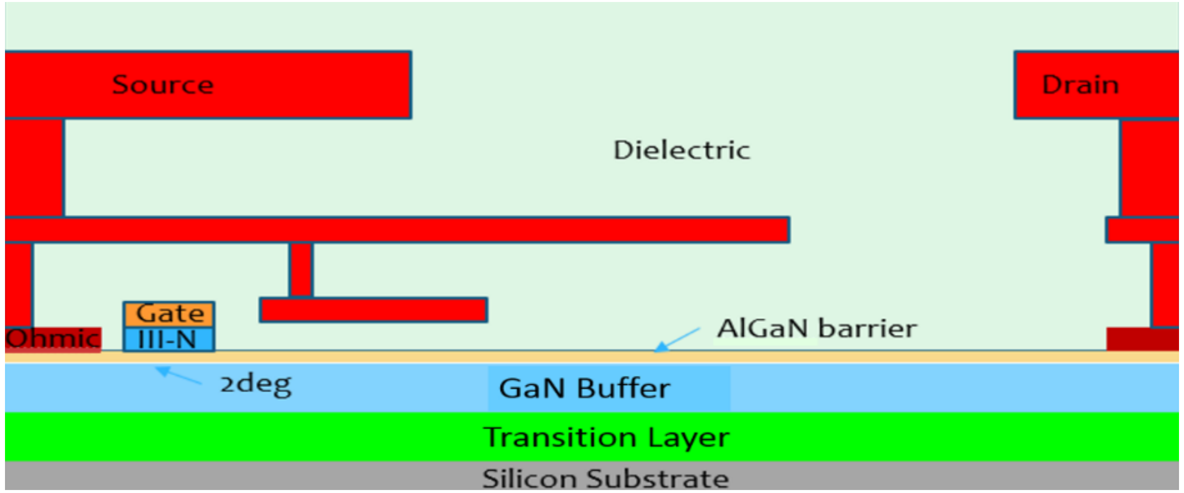
Let's go GaNFast™

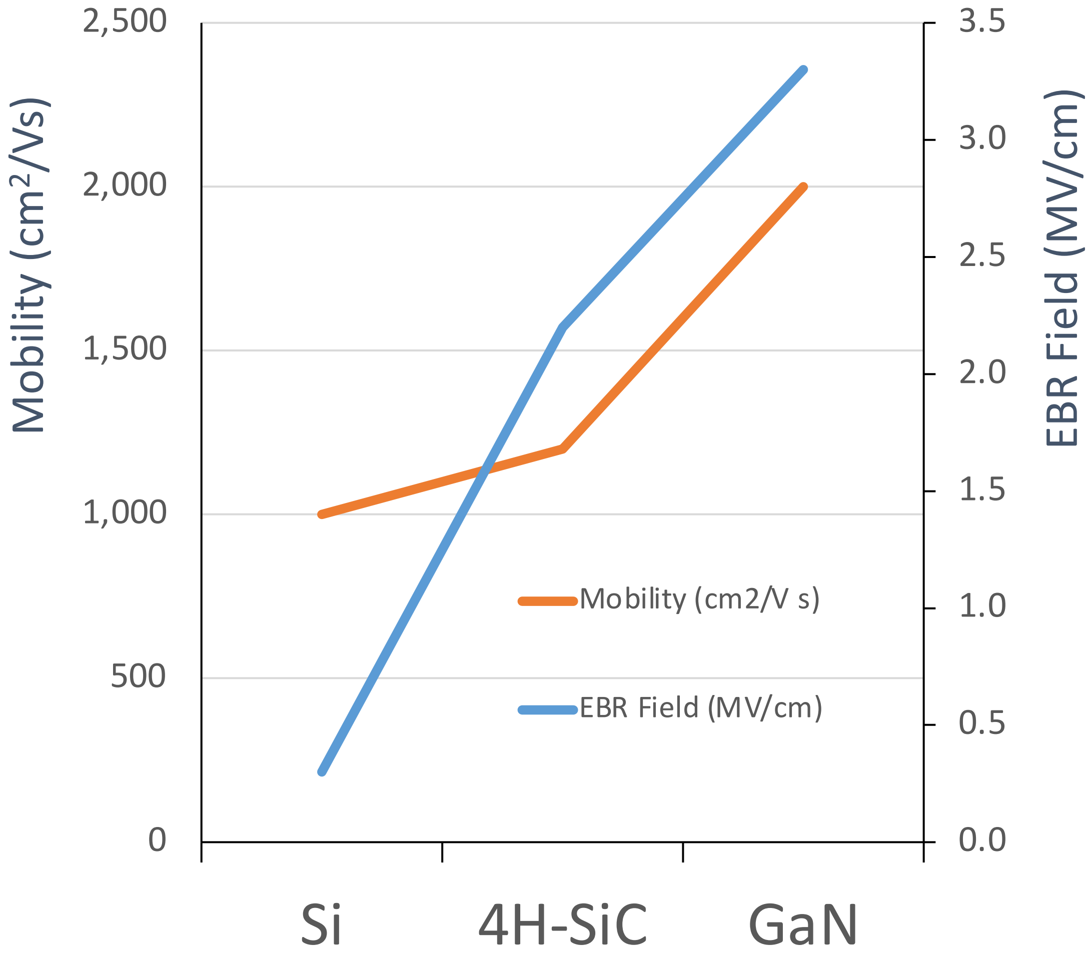
Navitas Semiconductor Ltd.

- World's first & only GaN power IC company
- Design:
  - Proprietary PDK, GaN-on-Si, 650V/800V
  - 100+ patents in GaN power, analog & digital, packaging and power systems
- Manufacturing
  - TSMC Hsinchu (6" wafers) and Amkor (5x6, 6x8 mm PQFN)
  - 10's millions per month capacity
  - 8M+ shipped
- Quality
  - "Beyond JEDEC": new, high-frequency reliability testing
  - Founder member of JEDEC JC-70.1 Subcommittee for "GaN Power Electronic Conversion Semiconductor Standards"
  - Zero failures

Lateral eMode GaN Advantages

- WBG GaN material allows high electric fields so high carrier density can be achieved
- Two-dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region
- Lateral device structure achieves extremely low Q_g and Q_{OSS} and allows integration
- Integration on silicon substrates means mature low cost wafer fabrication is available

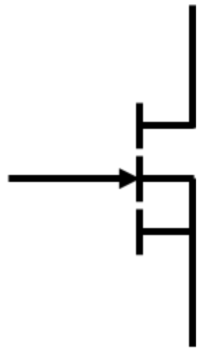




World's First GaNFast Power ICs

GaNFast™

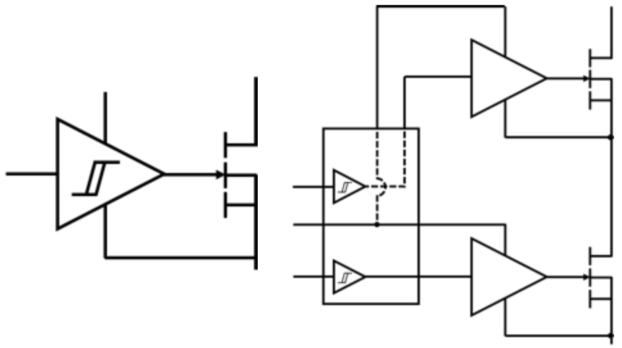
Fastest, most efficient GaN Power FETs



>20x faster than silicon
>5x faster than cascoded GaN

\+

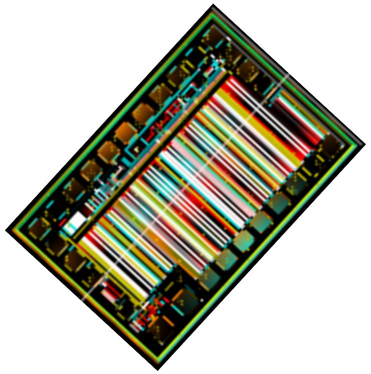
First & Fastest Integrated GaN Gate Drivers



>3x faster than any other gate driver
Stable, safe, superior efficiency

=

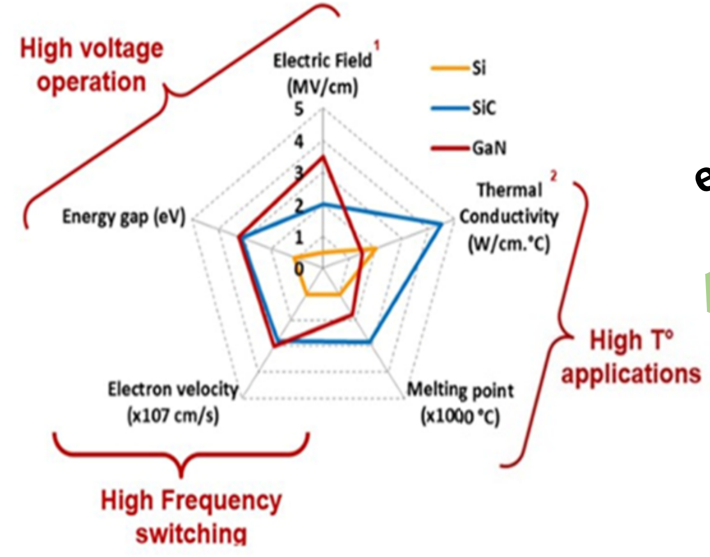
World's First GaNFast™ Power ICs



Power GaN Technologies

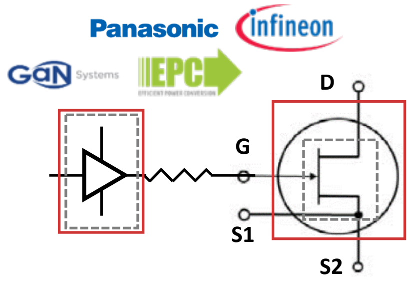
GaNFast™

GaN Physical Performance



eMode FET *(normally off)*

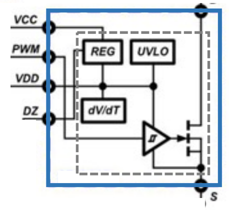
dMode FET *(normally on)*



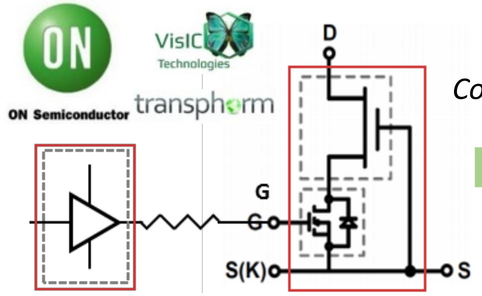
Need special gate driver to drive sensitive GaN input

Integration

纳微 Navitas



GaN Power (FET), Drive, Control, Protection

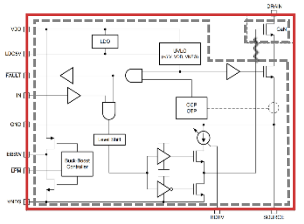


Need extra Si FET in 'cascode' configuration

Co-pack

Texas Instruments

power integrations



Si controller/driver + Si FET cascode + GaN dMode FET

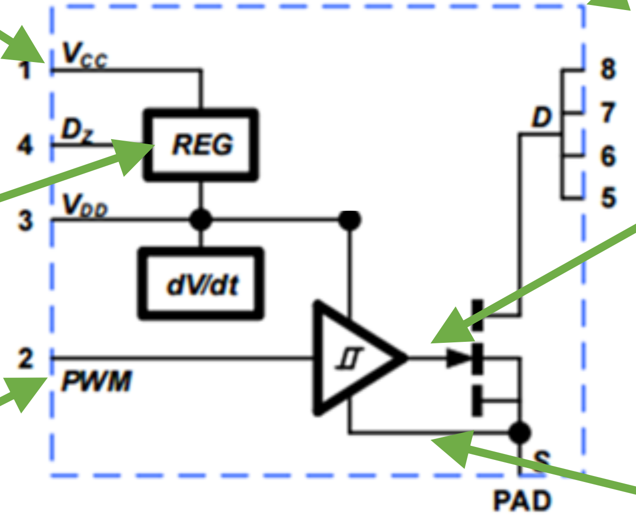
Simple & Robust

Wide Range V_{CC} (10-30V)

Total layout flexibility & simplicity

Regulator ensures V_{GS} within SOA

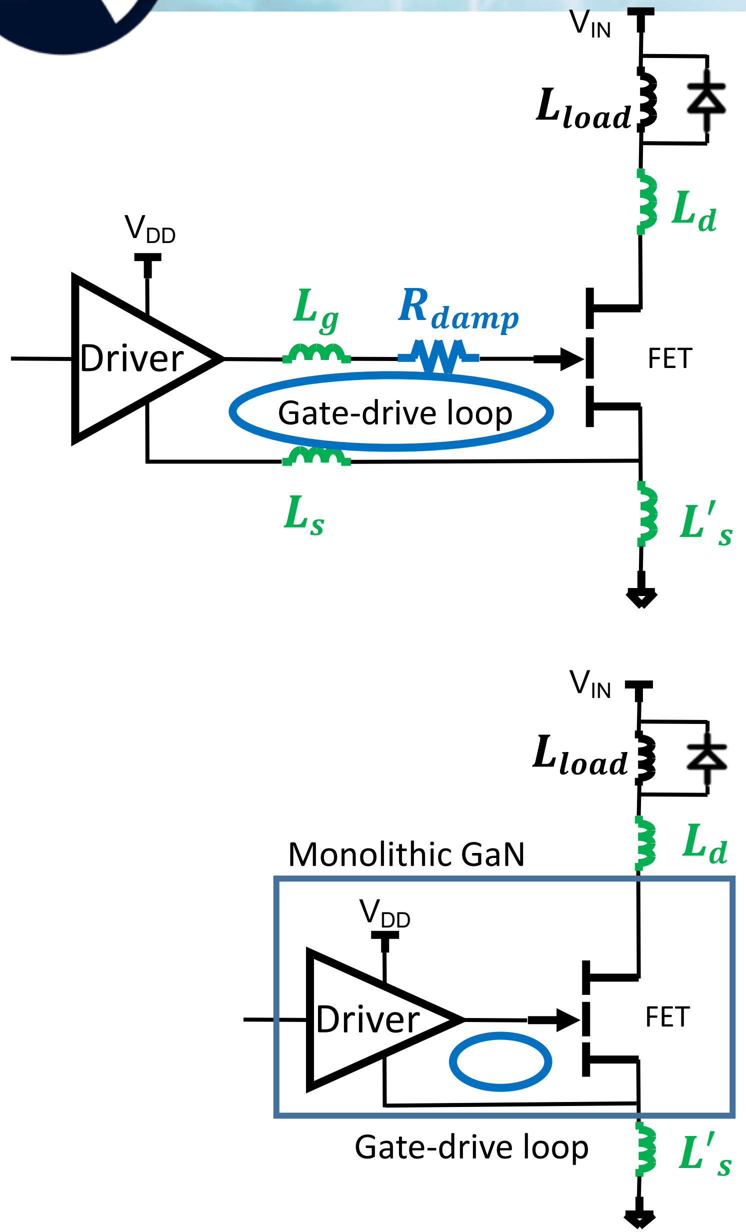
Gate protected from external noise (Not pinned out of package)

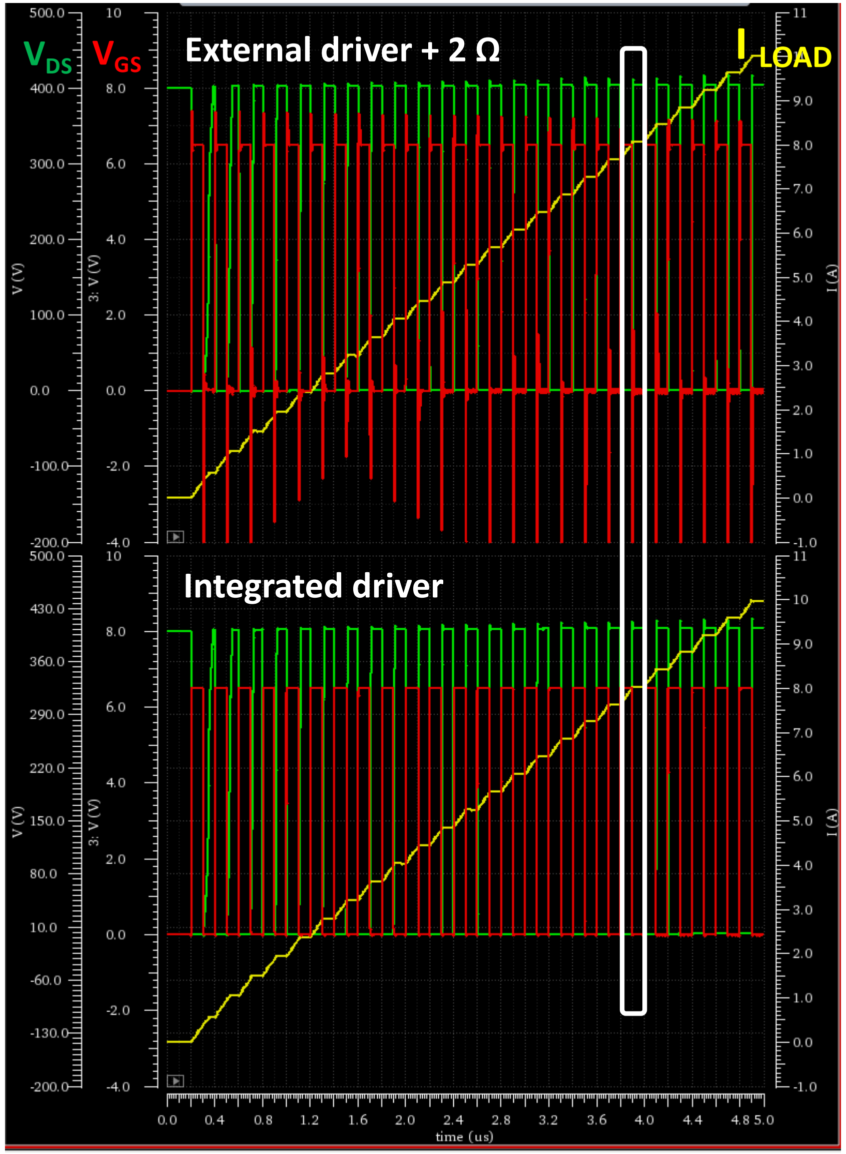


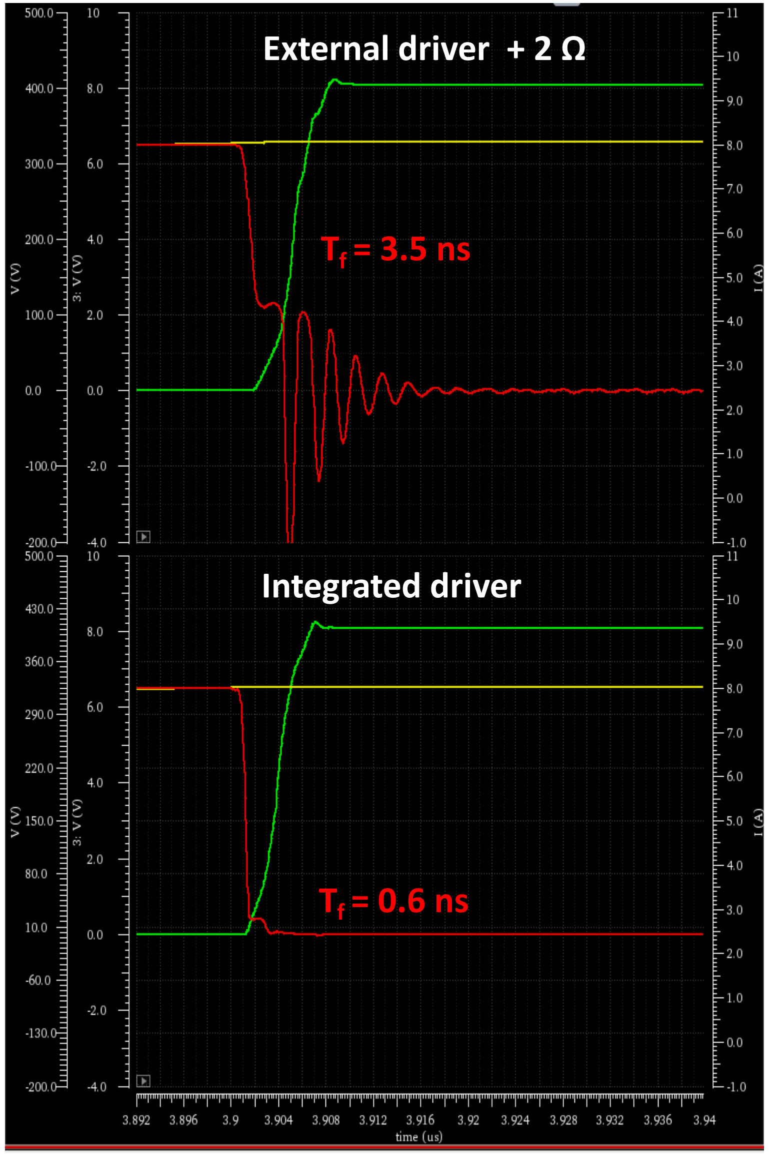
PWM Hysteresis for noise immunity

No inductance or ringing in gate loop

Fast & Stable Transient Response

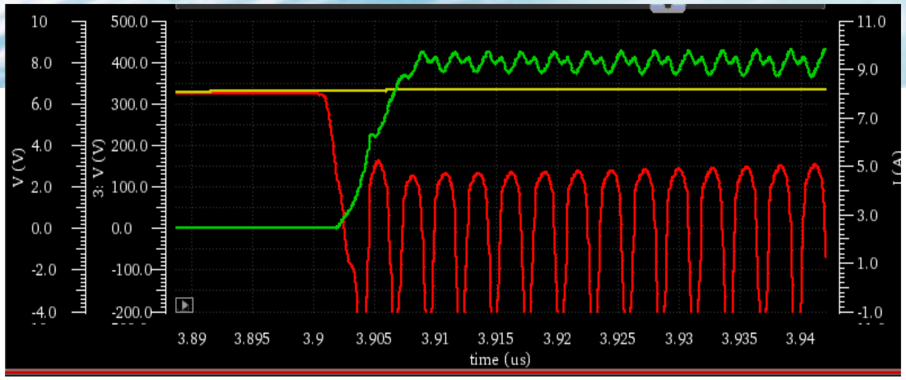






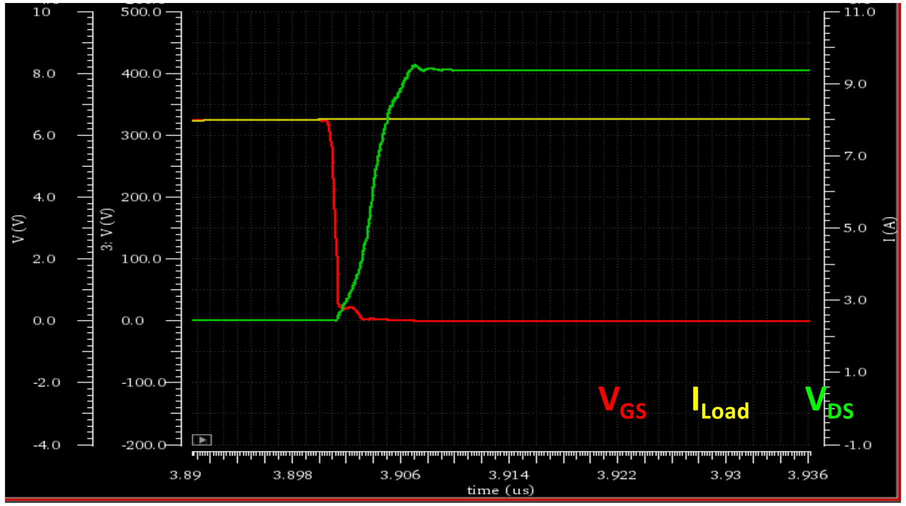
Stability & Efficiency

1. External driver: Oscillation



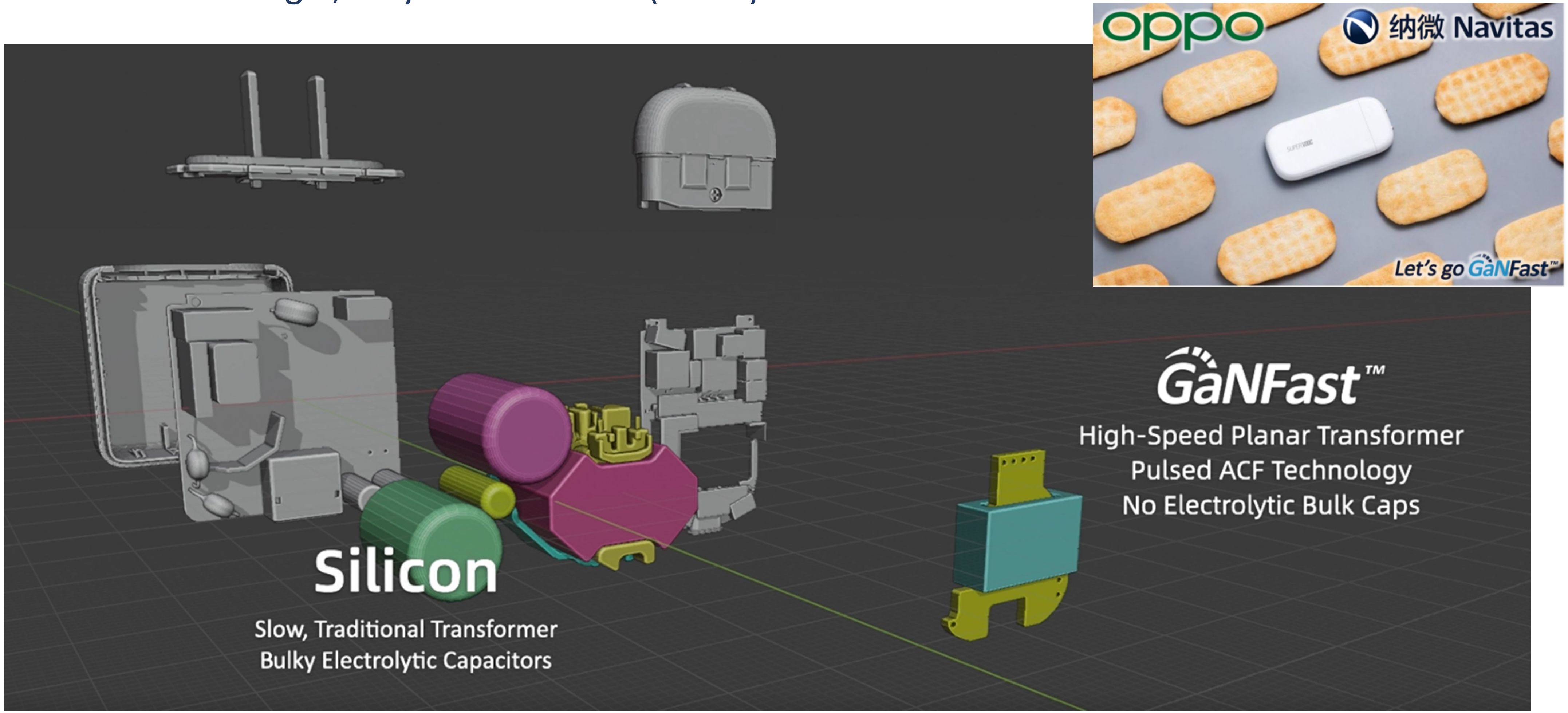
2. External driver + R_G: In control, Slow, Lossy

3. Integrated driver: In control, 10x faster, Zero loss



Integration: High-Freq. Example

- Rectified 100Hz pulsating DC feeds HF-ACF
- Smooth DC output with wide input range
- 50W ‘cookie’ charger, only 10.5 mm thin (cased)
- OPPO-proprietary ‘direct-charge’: pulse gaps eliminate polarizing effect, extend battery life



Single: Smaller, Lighter, Lower Cost

	Silicon			GaNFast		
Brand	Innergie	Apple	Lenovo	AUKEY	Xiaomi	Lenovo
						
Size (cc)	57	149	79	61	53	63
Weight (g)	86	193	127	92	82	93
Price ($)	$109	$69	$46	$36	$32	$30

Average 45% smaller, lighter, lower cost

60W - 65W single USB-C fast chargers. Retail price US$ at launch

Multi-port: Smaller, Lighter, Lower Cost

GaNFast™

Apple Si 18W
42 x 41 x 27 mm
= 47 cc, 60 g
(fixed AC pins)

Apple Si 30W
55.9 x 55.9 x 32 mm
= 87 cc, 158 g

Apple Si 61W
73 x 73 x 28 mm
= 149 cc, 193 g

USB-C #1 up to 65W
USB-C #2 up to 30W
USB-A up to 30W

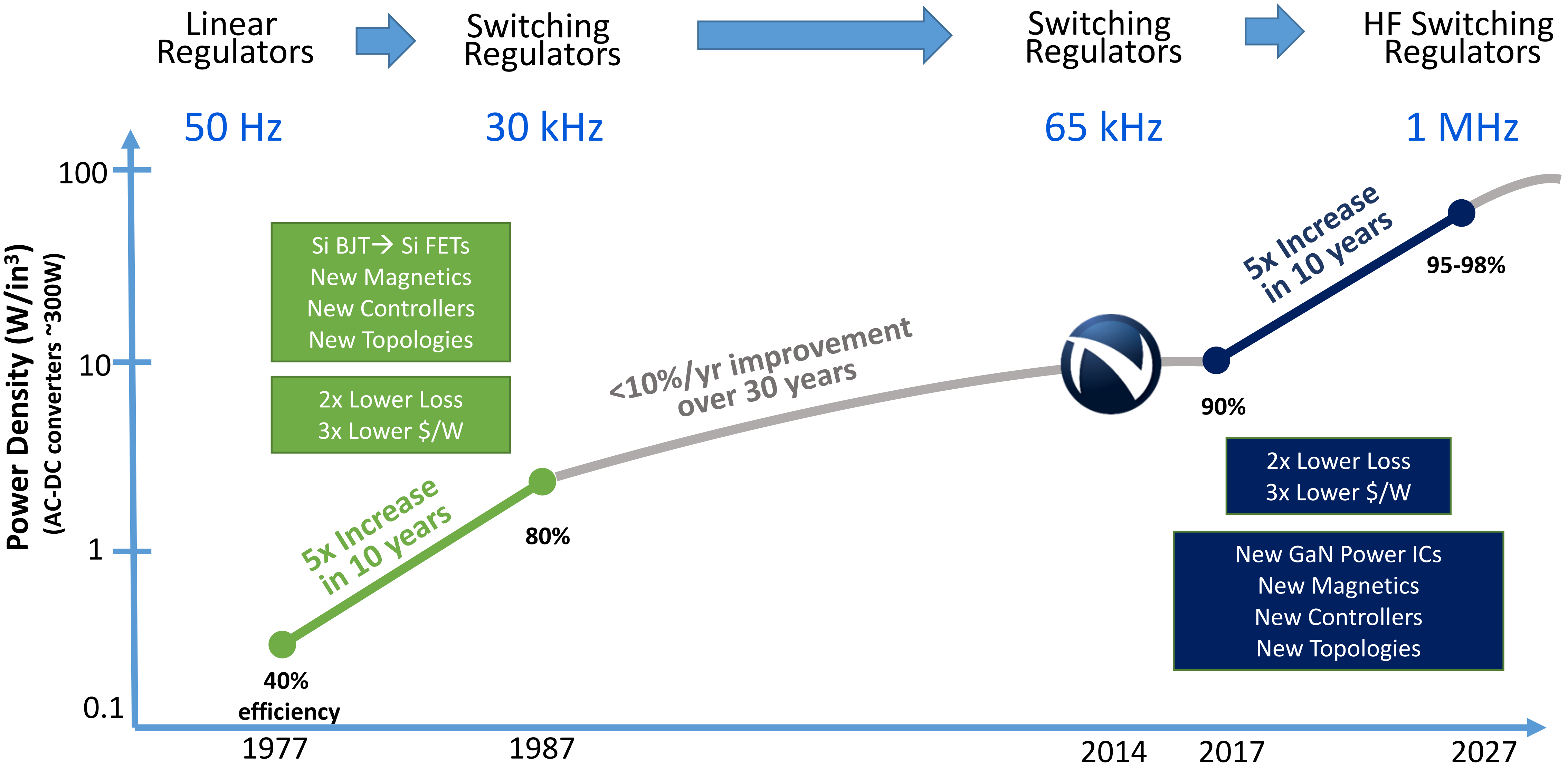
Baseus GaN 65W
75 x 35 x 32 mm
= 84 cc, 125 g

Retail $29 **$49** **$69**

283 cc, 411 g, $147 → **84 cc, 125 g, $35**

Images to scale

Game-Changer: Second Revolution in Power



Here come the GaN chargers

Visit www.GaNFast.com for more!

Ferric

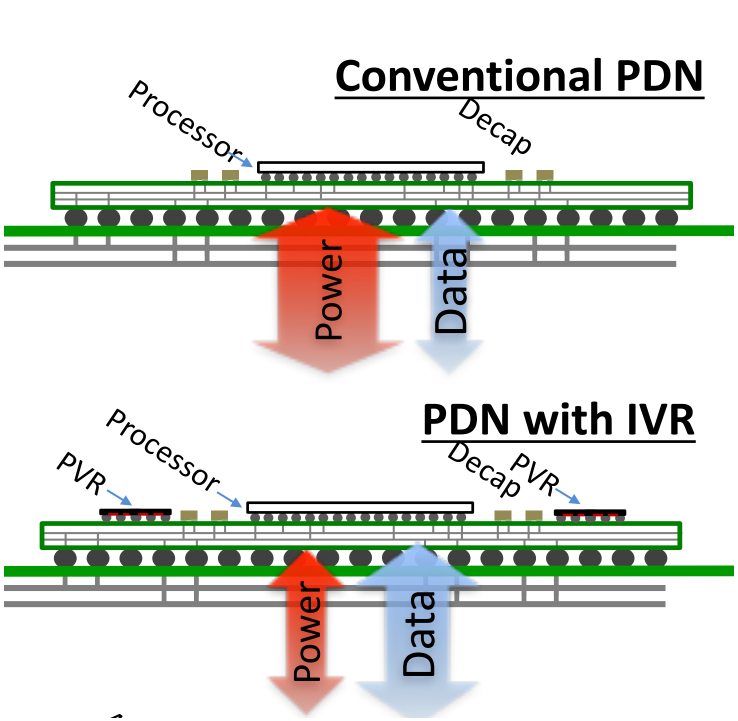
Efficient On-chip Power Conversion

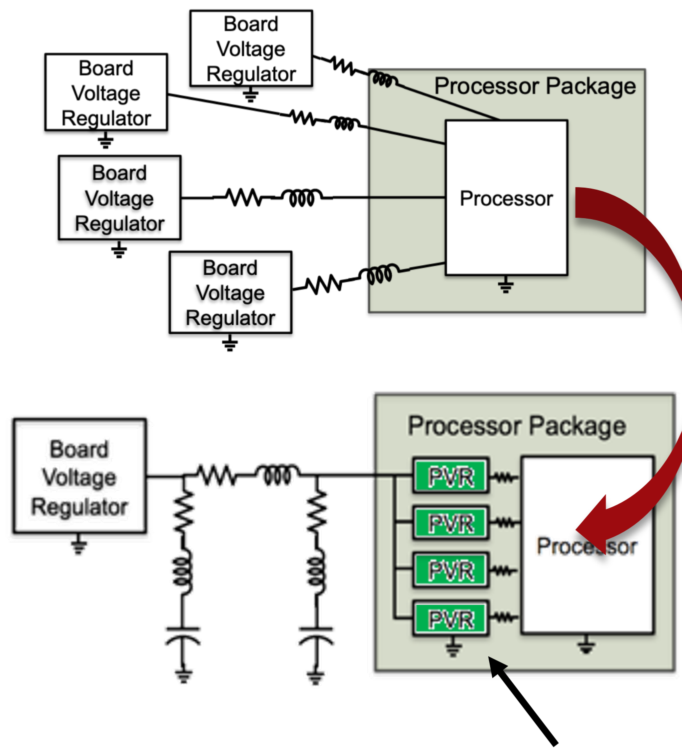
SFBAC PELS PANEL 10/2020

Noah Sturcken, PhD
Ferric President & CEO

FERRIC *PACKAGE VOLTAGE REGULATORS (PVRS)*

- Shrink power converters to be co-packaged with processors
- Reduce losses associated with high currents passed through board → socket → package → processor
- Enable delivery of many independently scalable supplies



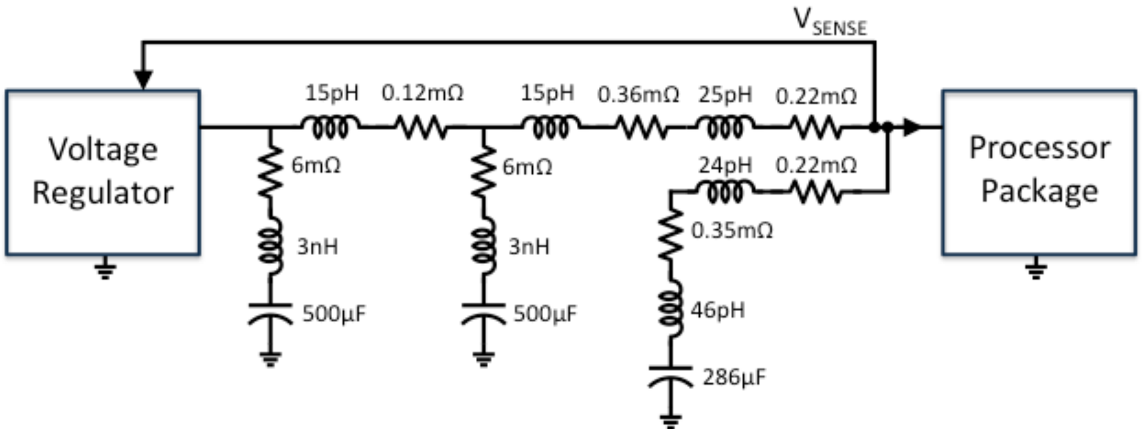


Save:
20% power
$20 BOM
20cm² area

US Pat. 16/129,305
PCT/US 18/48290
TW Pat. 107141297

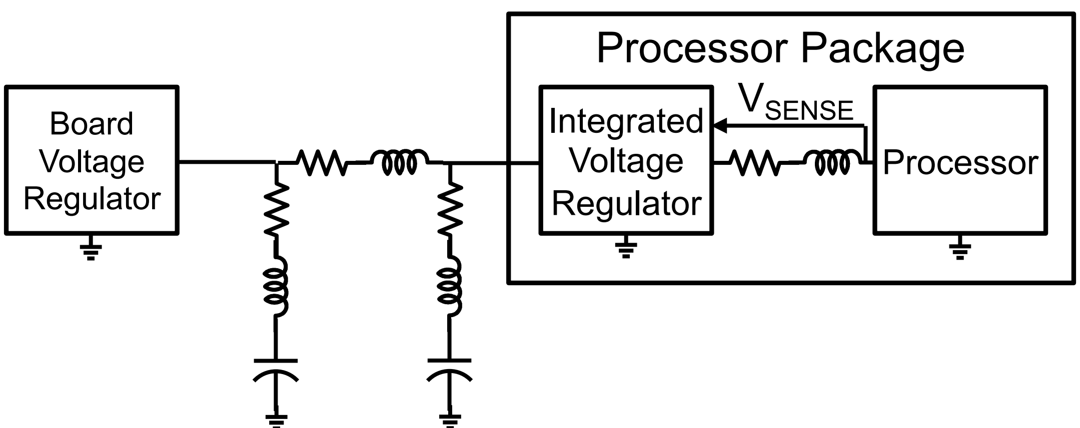
Ferric Single-Chip Power Converters

PACKAGE VR ***Improved Power Integrity***



Conventional Power Delivery Network (PDN)

Integrated Power Delivery Network (PDN)

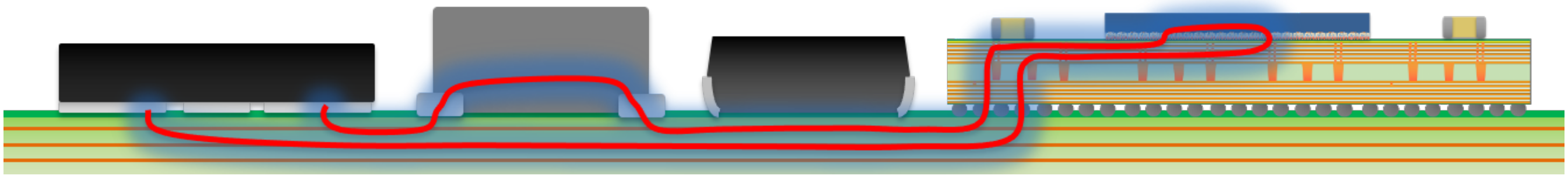


High bandwidth (>50MHz) feedback in immediate proximity to the load:

- *Reduce maximum broadband supply impedance to << 1mΩ*
- *Reduce processor supply voltage margins for improved efficiency*
- *Regulate resonant impedance peaks from upstream PDN*

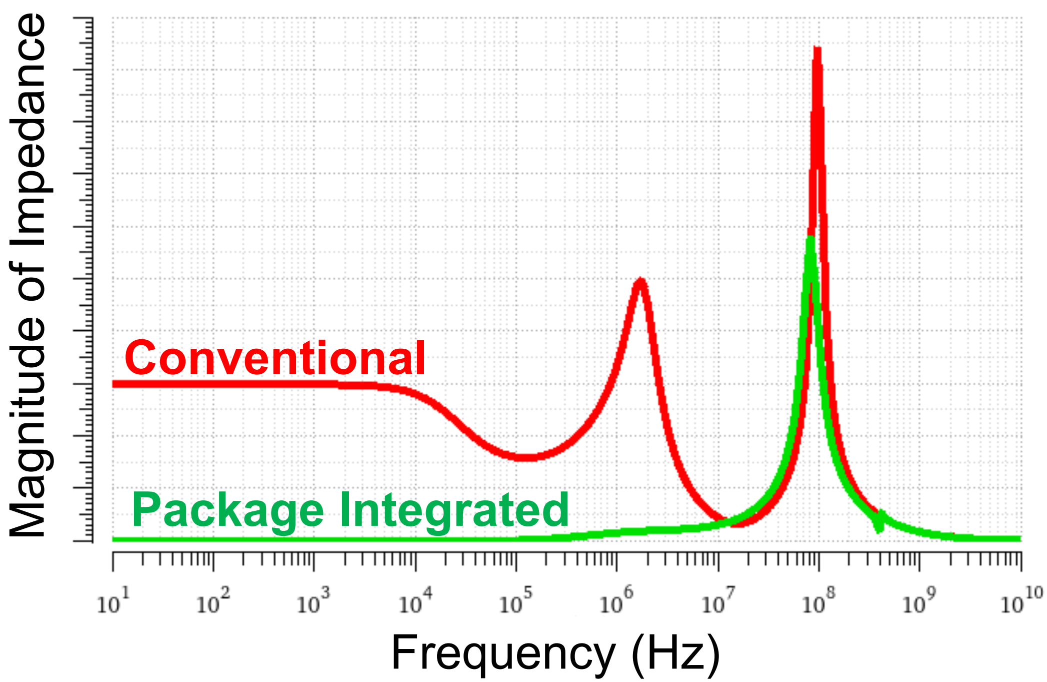
Fe

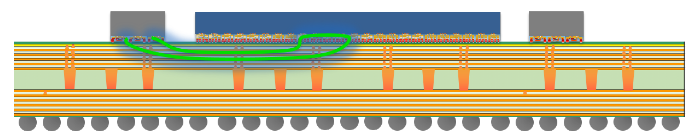
PACKAGE VR Improved Power Integrity



Conventional Power Delivery Network (PDN)

Integrated Power Delivery Network (PDN)





Smaller loop inductance

Less bulk capacitance

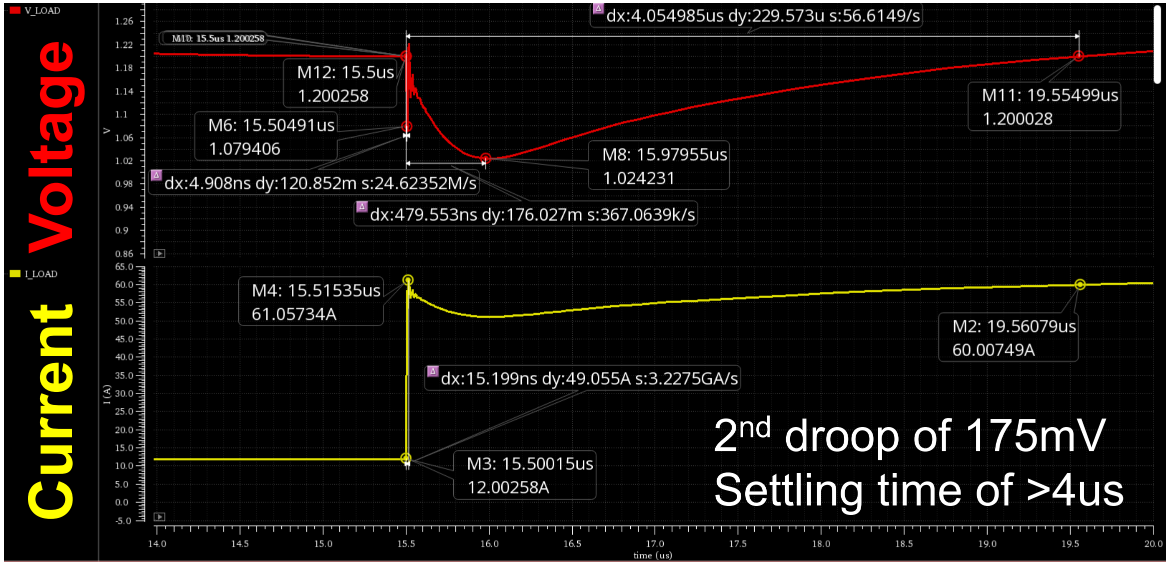
Higher feedback bandwidth

Fewer parasitics

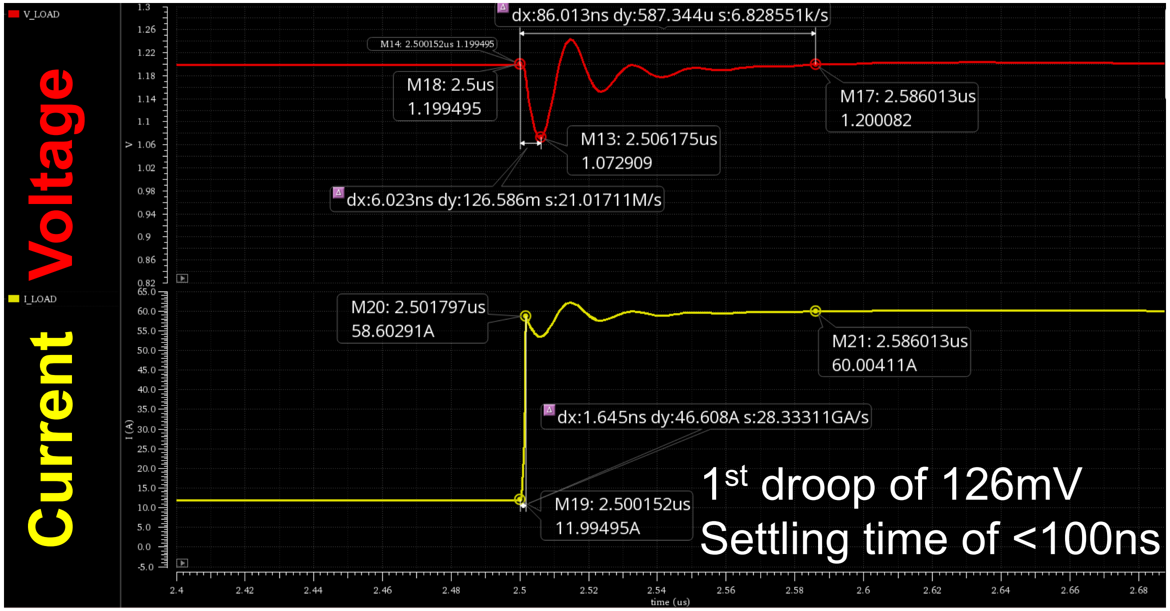
Less impedance overall

PACKAGE VR Improved Power Integrity

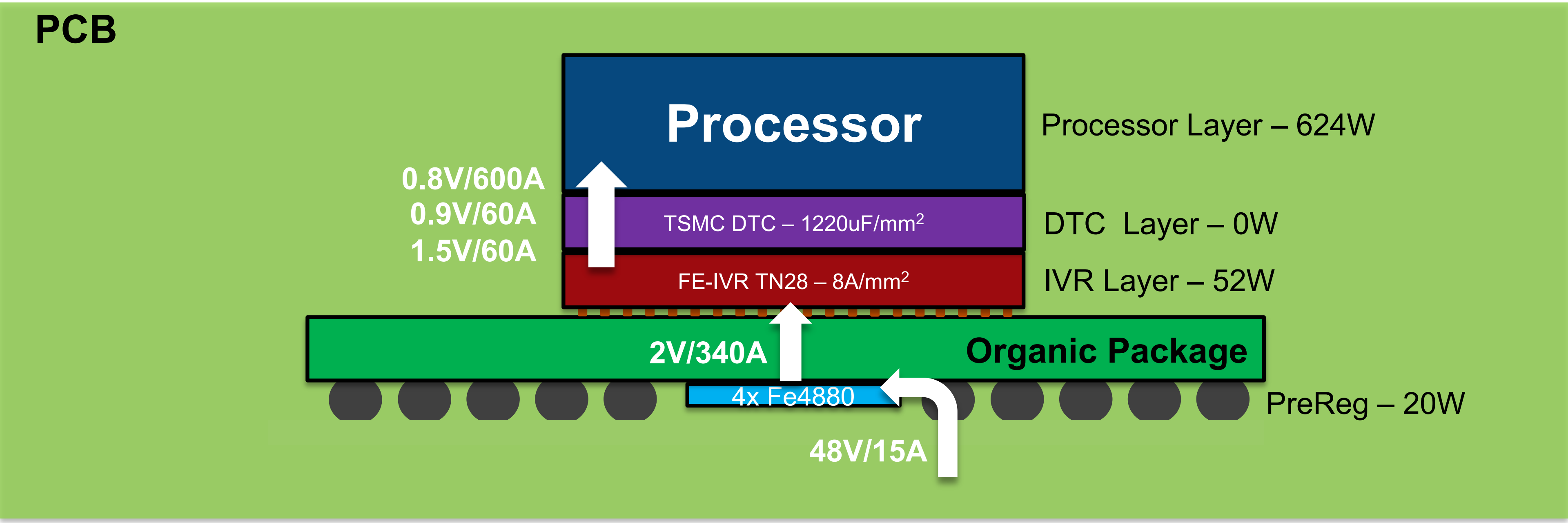
60A Processor Load Step with Mother Board VR



60A Processor Load Step with Ferric Package VR



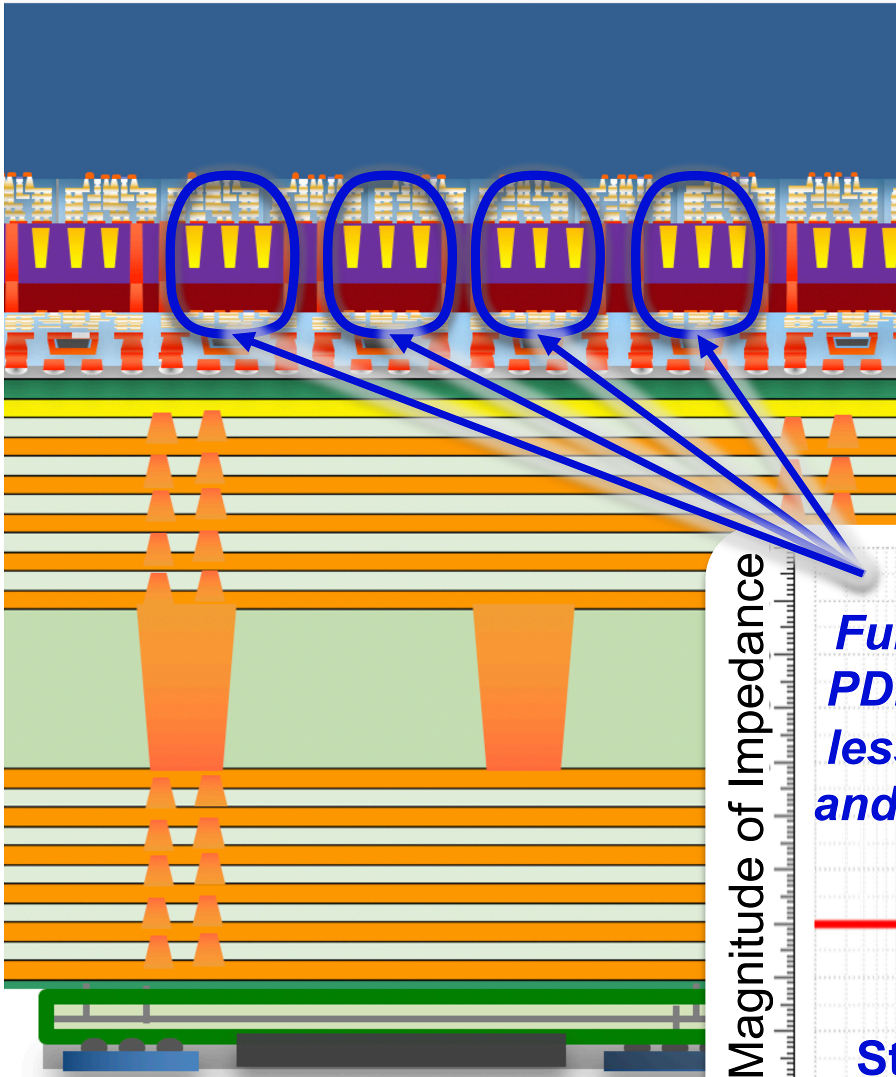
Stacked IVR Next Gen Datacenter Solution

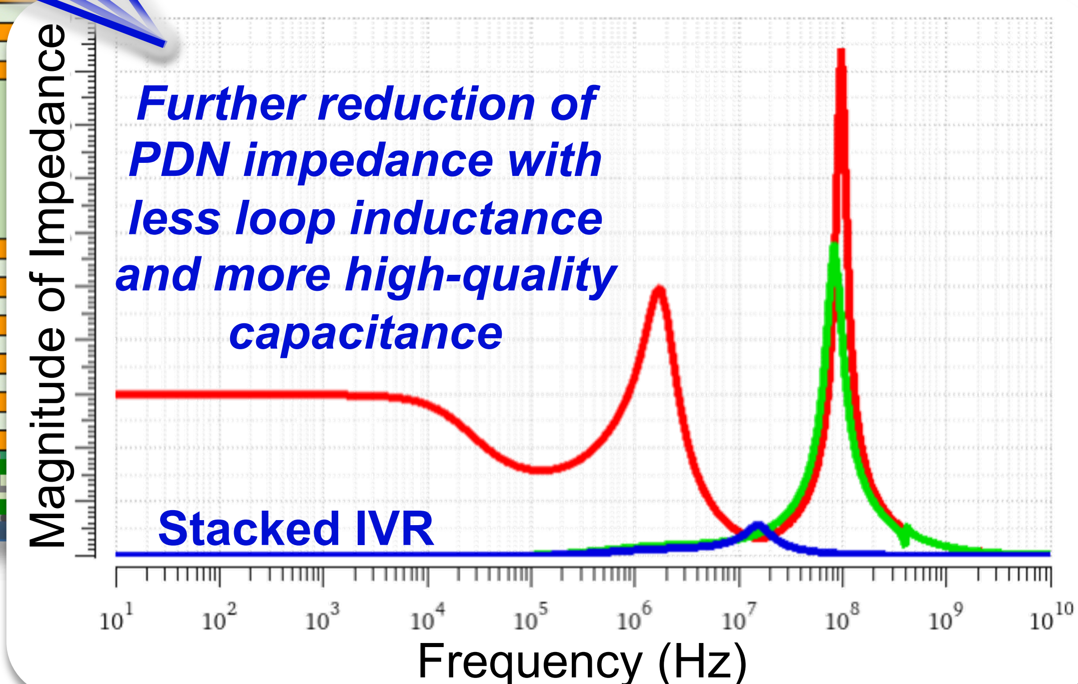


Supply	Converter	Converter Count	Converter Area (mm2)	Decap Area (mm2)	Decap (uF)	Voltage Ripple (mV)	ASIC Supply	Input Voltage (V)	Input Current (A)	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Total Eff. %	Power Dissipated (W)
1	FE-IVR TN28	1 Chip	75	45	54.9	<1	VDDC	2	260.9	521.7	0.8	600	480	92%	41.7
2			7.5	4.5	5.5	<1	AUX A	2	29.3	58.7	0.9	60	54	92%	4.7
3			7.5	4.5	5.5	<1	AUX B	2	47.9	95.7	1.5	60	90	94%	5.7
SUBTOTAL			90	54	65.9				338.1	676.2		720.0	624.0		52.2
INT	FE4880	4 Modules	480	N/A	N/A	<20	PVDD_PVR	48	14.5	697.1	2	338.1	676.2	97%	20.9
TOTAL								48	14.5	697.1			624.0	89.5%	73.1

*assume IVR junction temperature is 85C, otherwise ambient temperature of 75C

Stacked IVR Next Gen Datacenter Solution





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Oh, Inverted World!

New architectures for maximizing the economic potential of every single byte

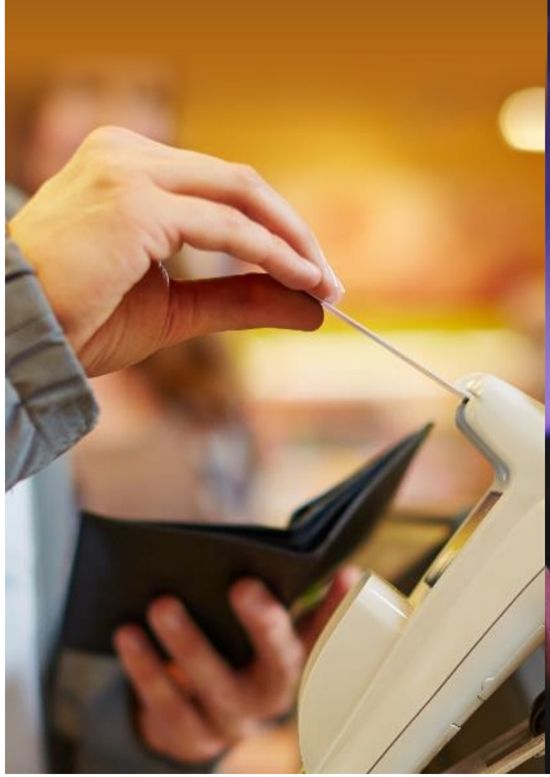
Kirk Bresniker, Chief Architect, Hewlett Packard Labs, HPE Fellow/VP
SFBAC/PELS/EPS Virtual Panel Session on Integrated Power

What's driving the data explosion?

Structured data

40 petabytes

Walmart's transaction database (2017)



Human interaction data

4 petabytes a day

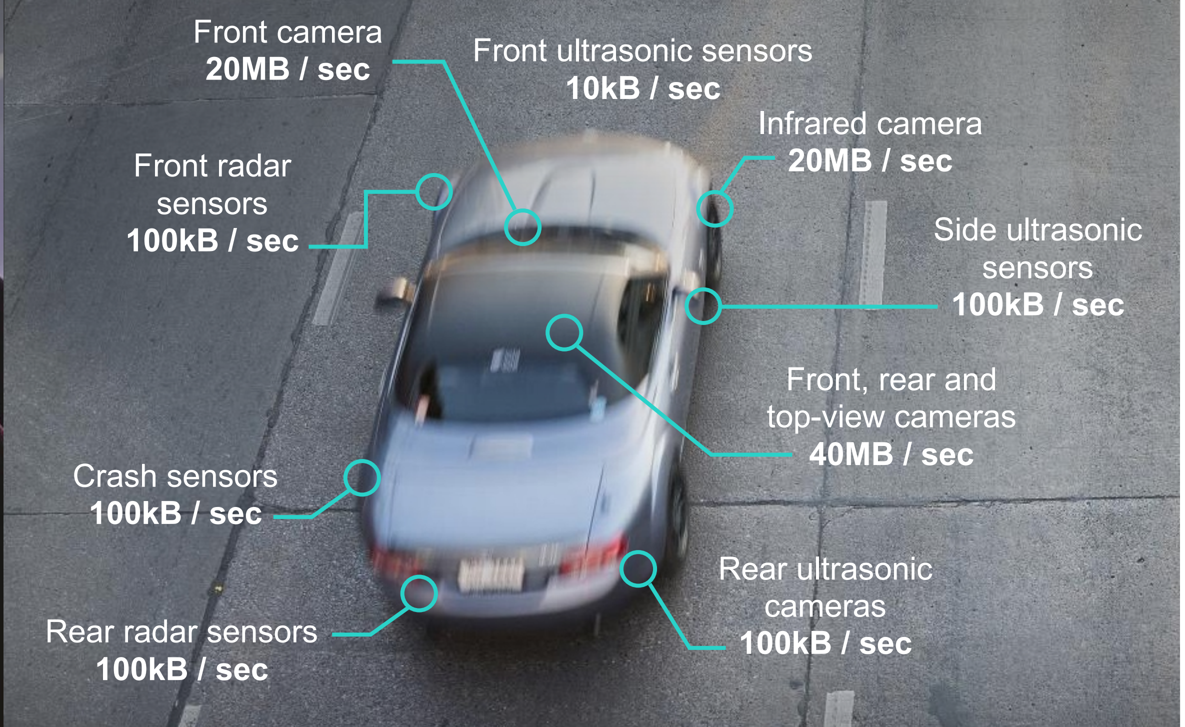
Per-day posting to Facebook across 2 billion users (2017)

2MB per active user

Digitization of analog reality

40,000 petabytes a day*

10m connected cars by 2020



* Driver assistance systems only

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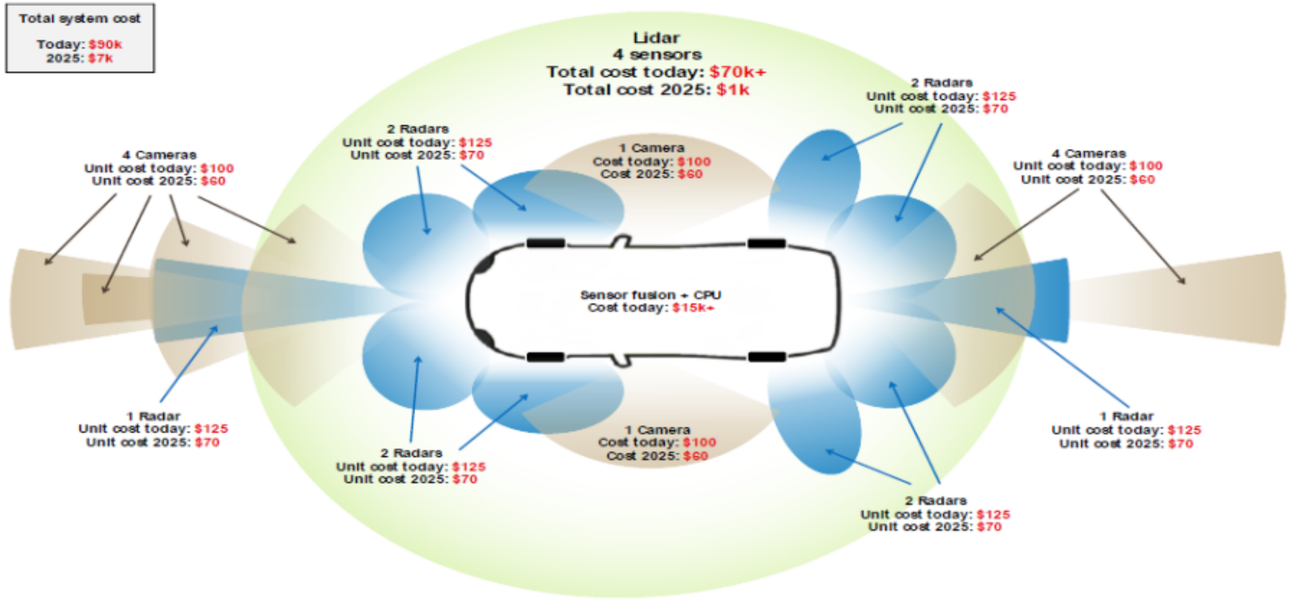
What is needed for an autonomous car?

LiDAR and HD map-based system (includes camera and radar as well)



We expect the prevailing sensor suite to include up to **12 cameras, 6 LiDARs and 6 radars …**

… and see the AV system cost below $10,000 in 2025, versus $100,000 today

Source: Infineon, UBS
Note: Excludes ultrasonic sensors for near-distance object detection (parking) – a minor cost item. Green = lidar, blue = radar, brown = camera.

The camera-only (and AI) AV system is cheaper, but has less redundancy. **Regulators' approval could be an issue** – potentially **negative for Tesla**

UBS

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Source: Colin Langan – Analyst – UBS – Presentation at CAR Palo Alto Detroit/Silicon Valley Event

The estimated costs of training a model

conventional car average including fuel, 1 lifetime 126,000 lbs CO2e

	Date of original paper	Energy consumption (kWh)	Carbon footprint (lbs of CO2e)	Cloud compute cost (USD)
Transformer (65M parameters)	Jun, 2017	27	26	$41-$140
Transformer (213M parameters)	Jun, 2017		192	$289-$981
ELMo	Feb, 2018		262	$433-$1,472
BERT (110M parameters)	Oct, 2018		1,438	$3,751-$12,571
Transformer (213M parameters) w/ neural architecture search	Jan, 2019		626,155	$942,973-$3,201,722
GPT-2	Feb, 2019	-	-	$12,902-$43,008

Estimate for in-vehicle compute power for Level 4 (hands off/eyes off) AEV

1kW ~ 3kW

Source: DoE Workshop on Advanced Computing for Connected and Automate vehicles, LBNL 05/07/2019

Note: Because of a lack of power draw data on GPT-2's training hardware, the researchers weren't able to calculate its carbon footprint.

Table: MIT Technology Review Source: Strubell et al. Created with Datawrapper

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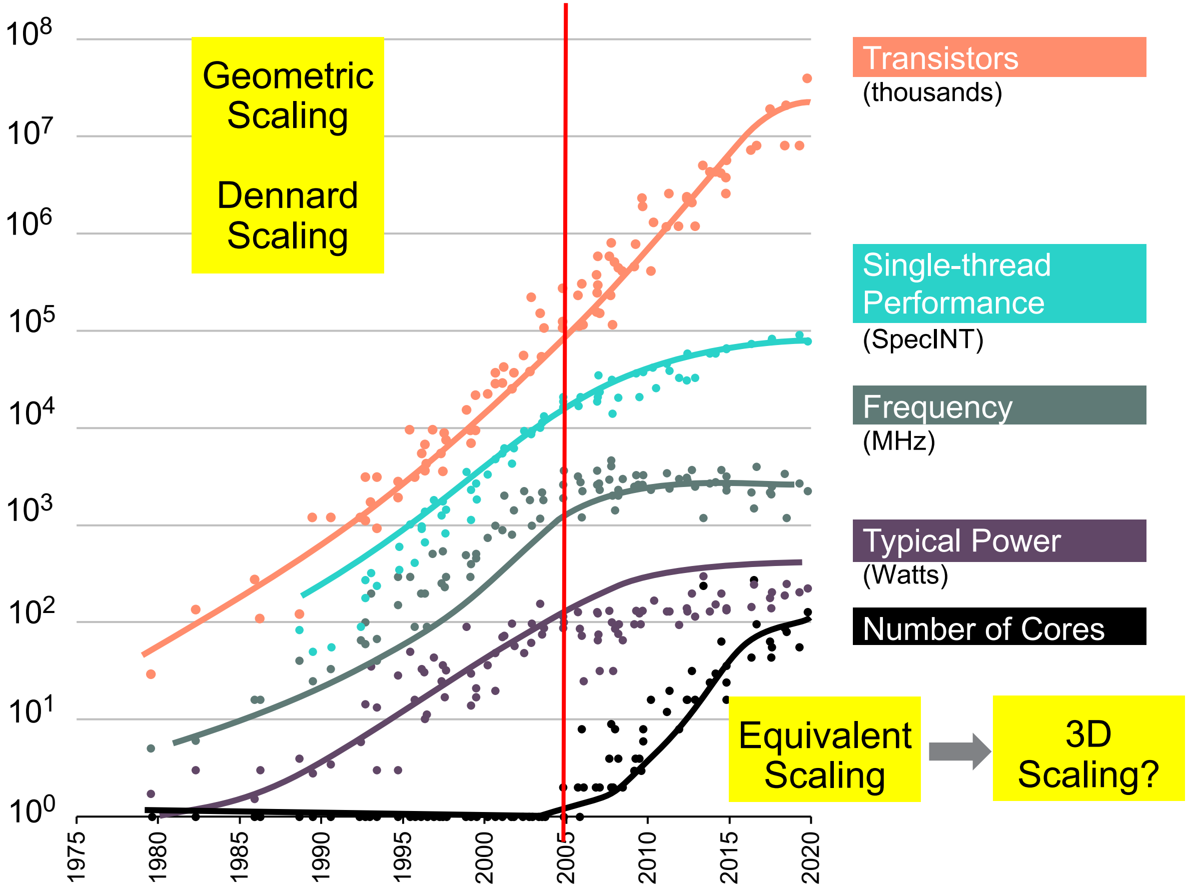
The New Normal: we are not keeping up

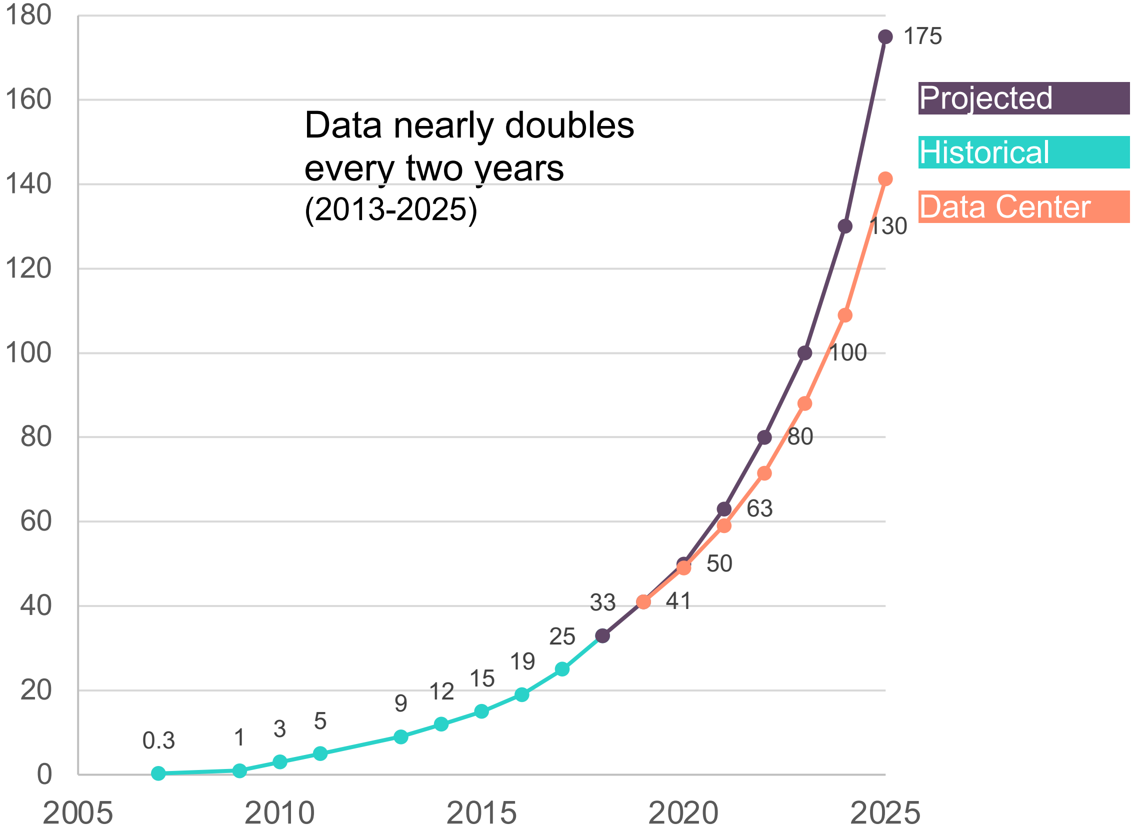
Microprocessors



Source: K. Rupp. 48 Years of Microprocessor Trend Data

Global Datasphere

(zettabytes)



Source: IDC Data Age 2025 study, sponsored by Seagate, Nov 2018

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Intelligent Mobility – Spanning Edge/Cloud/Core

Smart City DC

8. **Composable Memory-Driven Computing** enables fast processing of traffic and transportation data

7. **Edge-to-Core Resource & Data Management** through an integrated IoT platform that enables CICD deployment, aaS management of data & resources (compute, storage, stacks)

2. **Secure connectivity** with resilient platforms, services and data

4. **WiFI on-ramp to 5G Networks** allows seamless connectivity to LAN & WAN Network resources

Endpoint Devices

Edge IoT Platform

Terminal

SD-WAN

Cloud and/or Enterprise DC IoT Platform

1. **In-Vehicle Micro Data Center** with low power inference engines for safe, autonomous operations

3. **Mini Data Center** ingests vehicle data via WiFi as they return to Terminal during off-hours or maintenance

5. **SD-WAN** provides connectivity between Edge and Core Data Centers

6. **Composable Memory-Driven Computing** enables composable pools of memory & GPUs for big data training

Design envelopes from Edge/Cloud/Core

Beacon Sensor	“Lick and Stick” trusted data sources; 2.5D/3D integration of sensors, memory, accelerators, computation, and comms; **Energy Harvest with inducted power boost modes**; SRoT/Blockchain trust mechanisms
Access point	Unified 5G/WiFi/IoT radio access point; Identity, Activity, Locality triangulation; ML/AI augmented operation; **PoE today, but what to do if we switch to photonics?**
Aggregation Point	Robust environmentals; edge local secure hosting of containerized workloads; Static composition; smallest IT/OT Blended Platform target; **sub-50W footprint**
Edge Hardened	Robust environmentals; Legacy PXI/AXIe plus next gen modular FF; Static composition; Robust IT/OT Blended Platform target at several capacity points. **AC/DC, Crossover between Passive/Active Cooling up to carry on scale data center**
Single System Flex	**OPC/Rack/Tower systems** with next gen modular FF option bays and electrical/optical Gen-Z/CXL expansion; Static fabric configurations between reboots; low cost point-to-point expansion.
Enclosure Composable	Blade Enclosure augmented with next gen modular FF and memory fabric at the enclosure and rack level; Enclosure level switching of fabrics; Static/Dynamic fabric configurations. **Does this design envelope have legs?**
Rack Scale	Dense next gen modular FF enclosures with integrated switching; Enclosure as endpoint; Dynamic fabric configuration; Dematertialized and legacy free; Design for Flex Capacity, Co-Lo, aaS Consumption models. Containers on memory fabrics. **Roll-in, Plug-in, Turn-on for legacy or accelerators.**
Aisle/Pod Modular	Dense next gen modular FF enclosures with integrated switching; ToR switch; Dynamic fabric configuration; Dematertialized and legacy free; Design for Flex Capacity, Co-Lo, aaS Consumption models. Petascale HPC and Petascale Enterprise in-memory DB/Analytics **Balance between lowest possible PUE and modular design principles**
Exascale HPC	DC scale memory-semantic fabric over photonics; all liquid/conduction cooling environmentals; Aisle/Pod modular for I/O nodes; 2.5D/3D integrated CPU/GPU/Memory modules; **6pJ/bit * 8bit/FLOP * 1 EFLOP/s = 48 MW**

Discussion Points

– Edge-to-Cloud service meshes will be the confluence of three critical and interdependent supply chains: infrastructure, energy and information. Failure to understand the interplay of these supply chains or inadequately securing any one will force us to de-rate performance, sustainability or equitable access.

– AI/ML are data driven practices and will create the need for new, complex topologies of data flow, and thus energy flow, from edge to cloud. As CI/CD practices follow the integration of AI/ML into every system design type, IT security and performance features will follow towards edge systems and today's data center power solutions will follow.

– We need an energy calculus for distributed edge-to-cloud applications to enable tradeoffs of data movement versus data transformation inclusive of security and privacy.

Thank you

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