Coss Hysteresis in Advanced Superjunction MOSFETs

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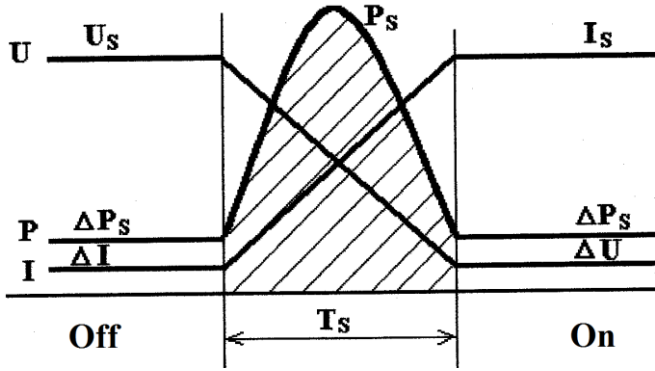
Introduction

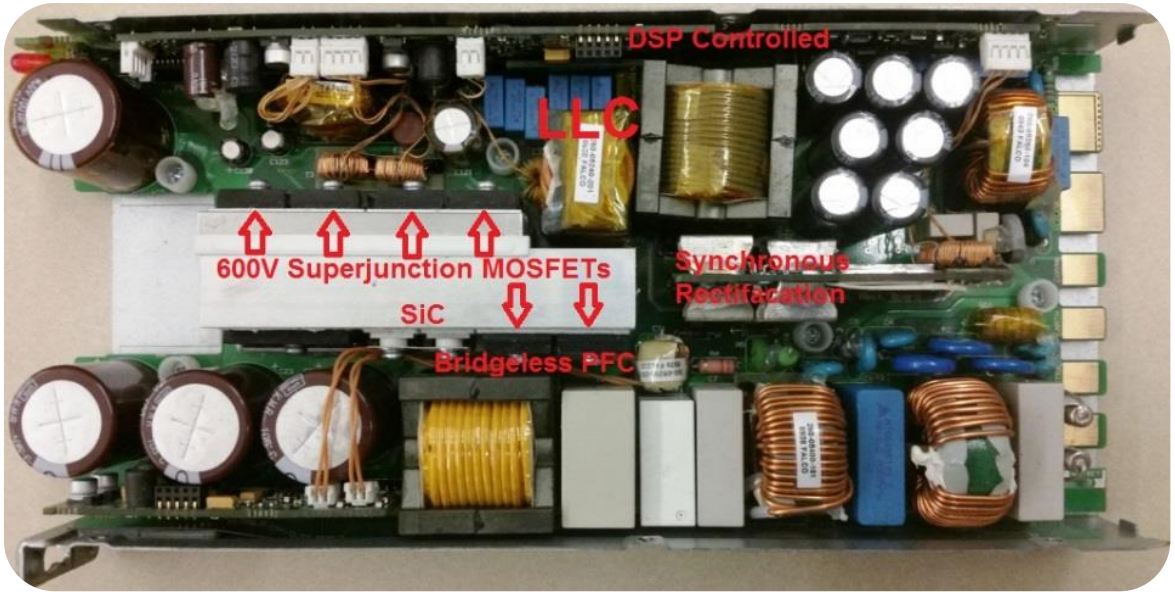
- The demand for improved power conversion efficiency:
  - Drives the advancement of superjunction MOSFET technology
  - Increased the popularity of Zero Voltage Switching (ZVS)
- ZVS eliminates two sources of switching losses:
  - Hard switched losses are eliminated
  - Coss energy is recovered (or is it?)



- The advancement of superjunction MOSFET technology appears to be creating a previously unknown Coss loss mechanism:
  - Fine geometry of the superjunction structure is causing non-ideal behavior of the output capacitance reducing the effectiveness of Coss energy recovery
- This work is focused on understanding this Coss loss mechanism

The Discovery of a New Loss Phenomenon

- Loss phenomenon first observed by author at Eaton in 2009:



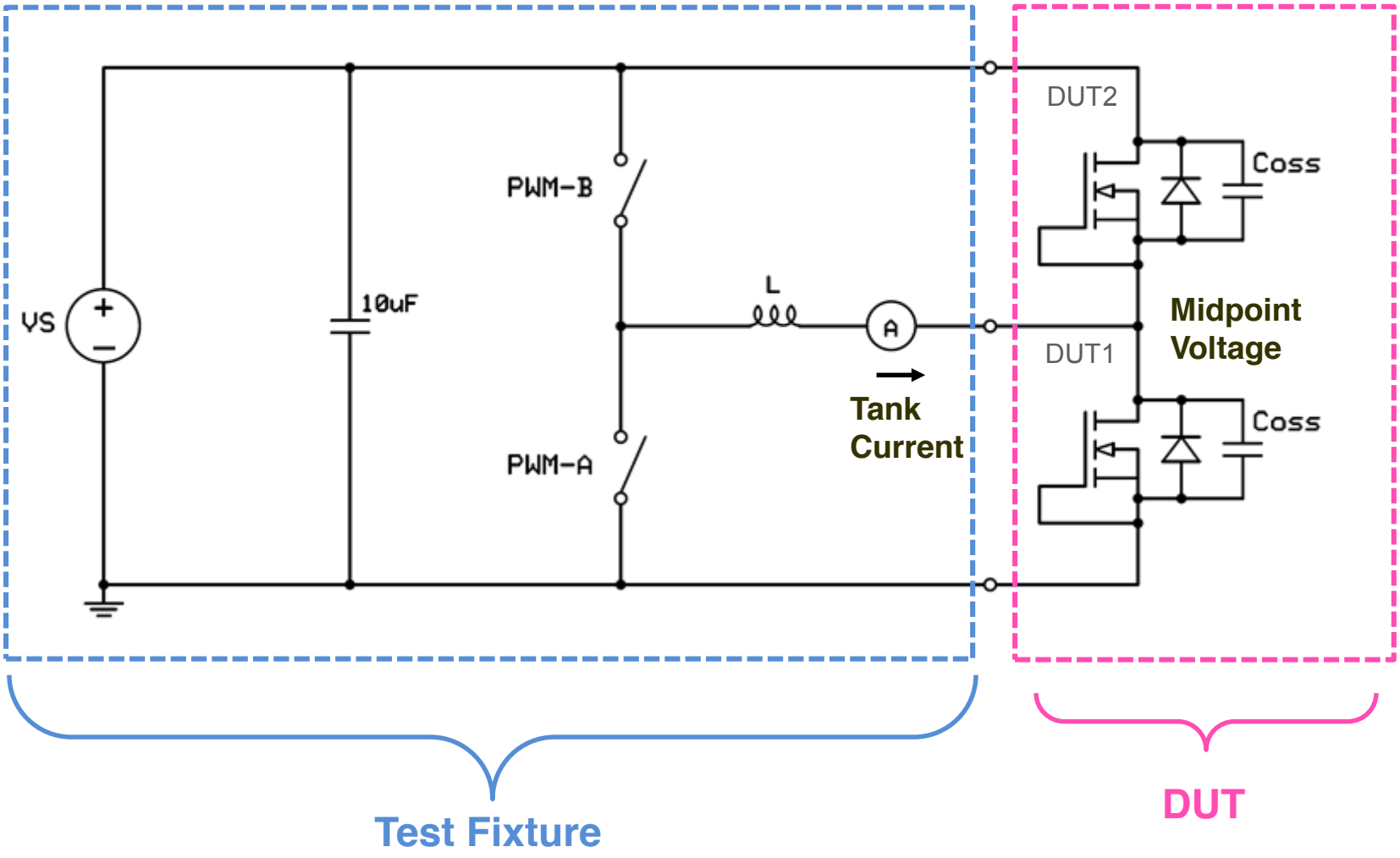
Telecommunications Rectifier
(APR48-ES – 2kW)
96%(pk) efficiency
SiC Bridgeless PFC
Resonant LLC
Synchronous Rectification
DSP controlled
New Superjunction MOSFET: "Device A"

- Investigation into phenomenon at Enphase Energy started in 2011:
  - [e] This presentation content is shared with Enphase Energy's authorization
- Results based on calorimetry measurements presented at APEC 2014*
- Results based on Sawyer-Tower measurements presented at APEC 2016^

* J.B. Fedison, M. Fornage, M.J. Harrison, and D.R. Zimmanck, "Coss Related Energy Loss in Power MOSFETs Used in Zero-Voltage-Switched Applications," APEC 2014 Proceedings, pp. 150-156, 16-20 March 2014

^ J.B. Fedison, and M.J. Harrison, "Coss Hysteresis in Advanced Superjunction MOSFETs," APEC 2016 Proceedings, pp. 247-252, 20-24 March 2016

Resonant Half-Bridge (RHB) Test Circuit



This circuit replicates real-world circuit conditions found in ZVS applications

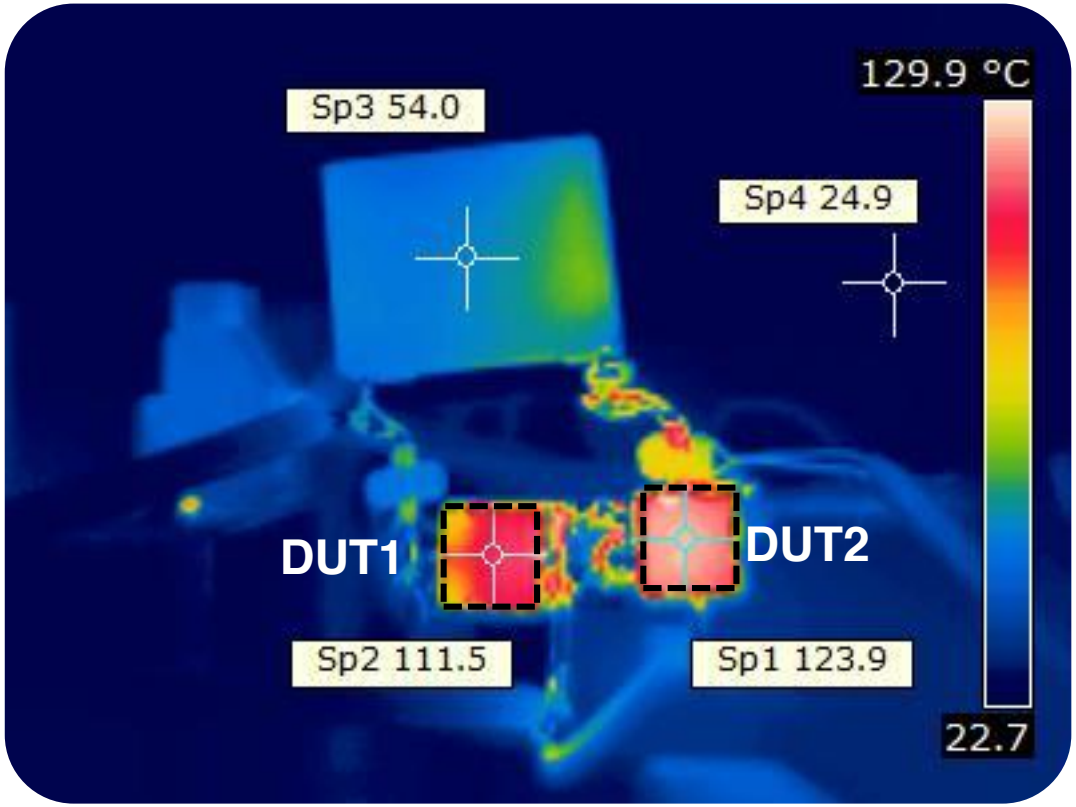
State-of-the-Art Superjunction MOSFETs Examined

MOSFET	V_{DSS} at 25ºC (V)	R_{DSON} max at 25ºC (mΩ)	C_{iss} at V_{DS}=0 (nF)	Area Specific R_{DSON} typ at 25ºC (mΩ cm^2)
Device A	650	148	2.0	19
Device B	600	160	2.1	27
Device C	600	178	2.0	26
Device D	600	158	3.3	30
Device E	600	160	1.9	33

All devices represent “state-of-the-art” superjunction MOSFET technology*

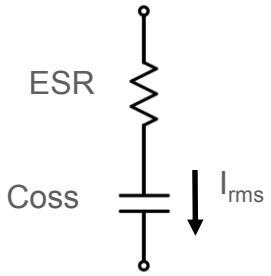
* As of the start of this investigation in 2012

Unexpected Heating of a Superjunction MOSFET



DUT: MOSFET A

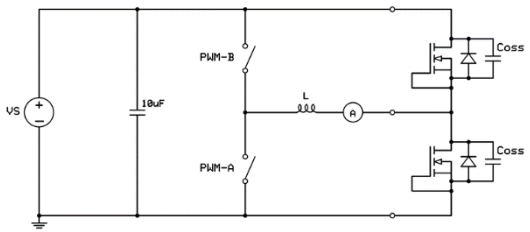
Conventional capacitor dissipation model:



$$ESR \approx R_{DSON}$$

$$P_{Dissipated} = I_{rms}^2 ESR$$

Temperature rise of DUT2	ΔT_{CA}
Expected	0.3ºC
Measured	99ºC



Conclusion: the conventional model is invalid

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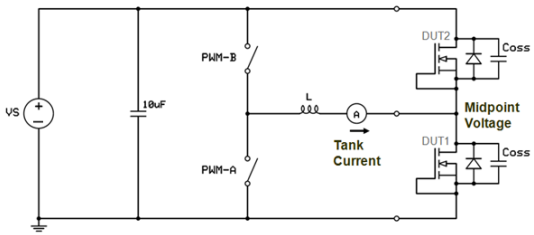
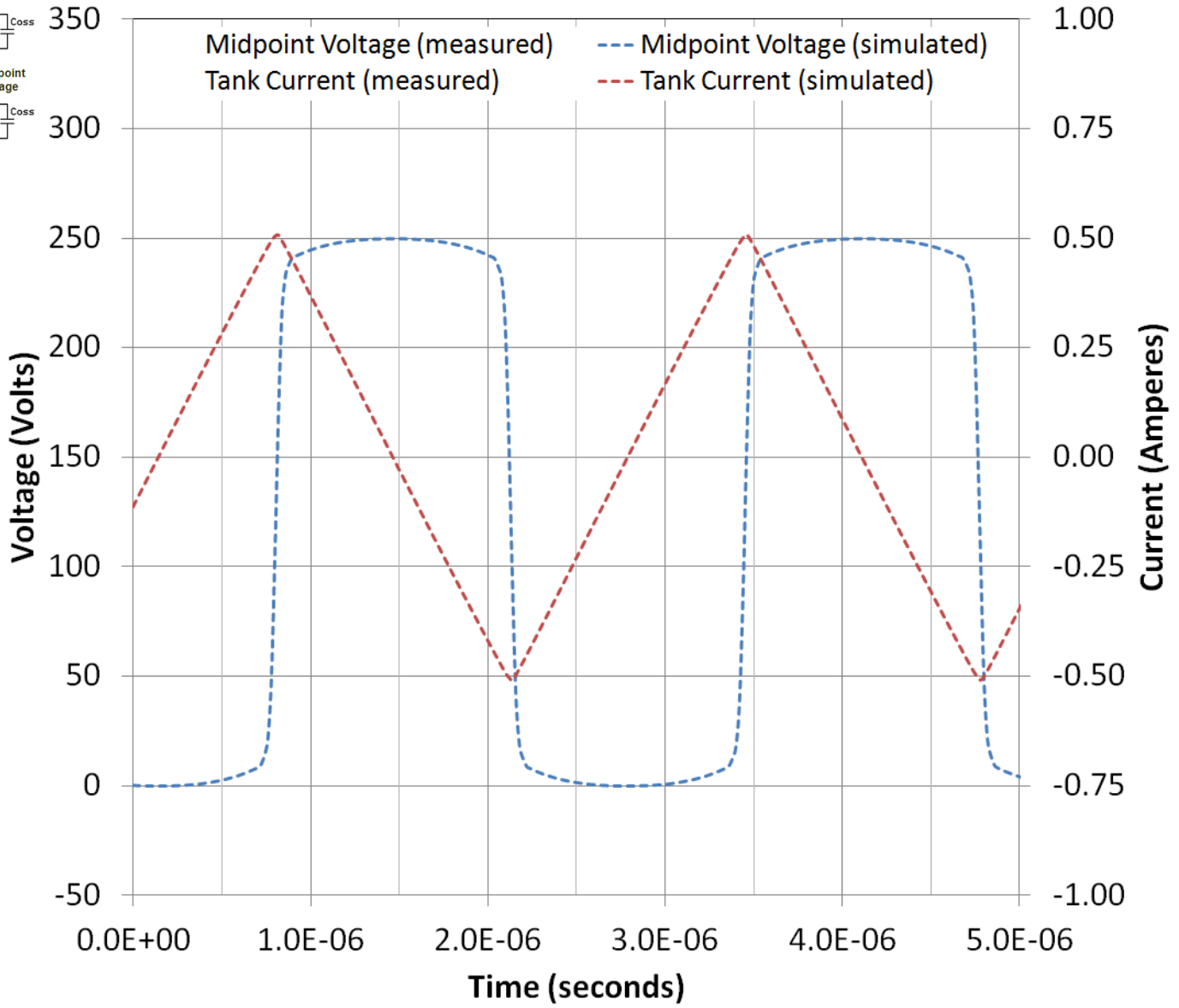
RHB Waveforms, MOSFET A – simulated



Simulations show non-sinusoidal voltage waveform due to C_{oss} nonlinearity versus V_{DS}

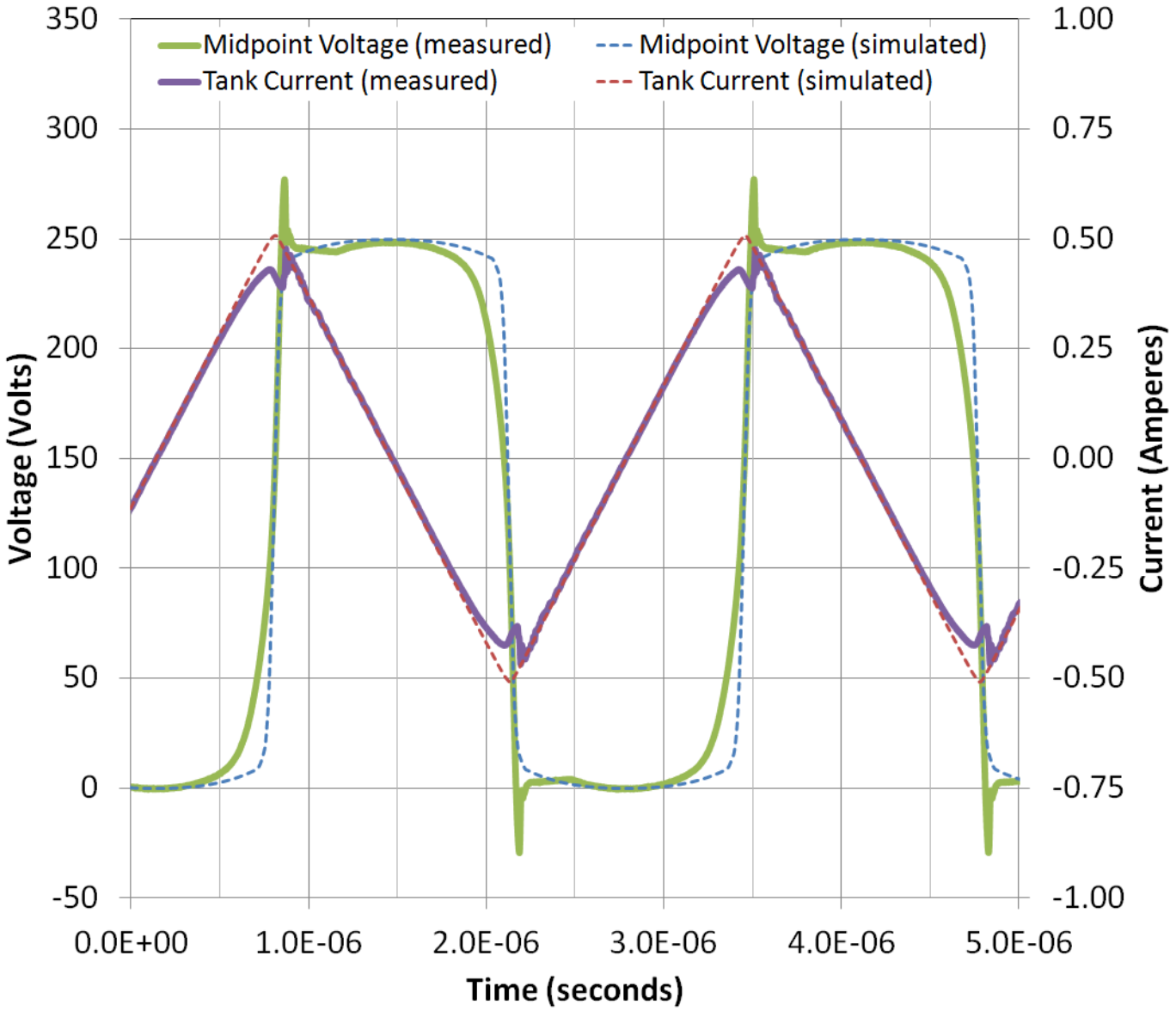
Notice that the start and end of each transition is symmetrical



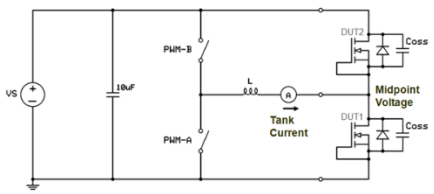
RHB Waveforms, MOSFET A – measured

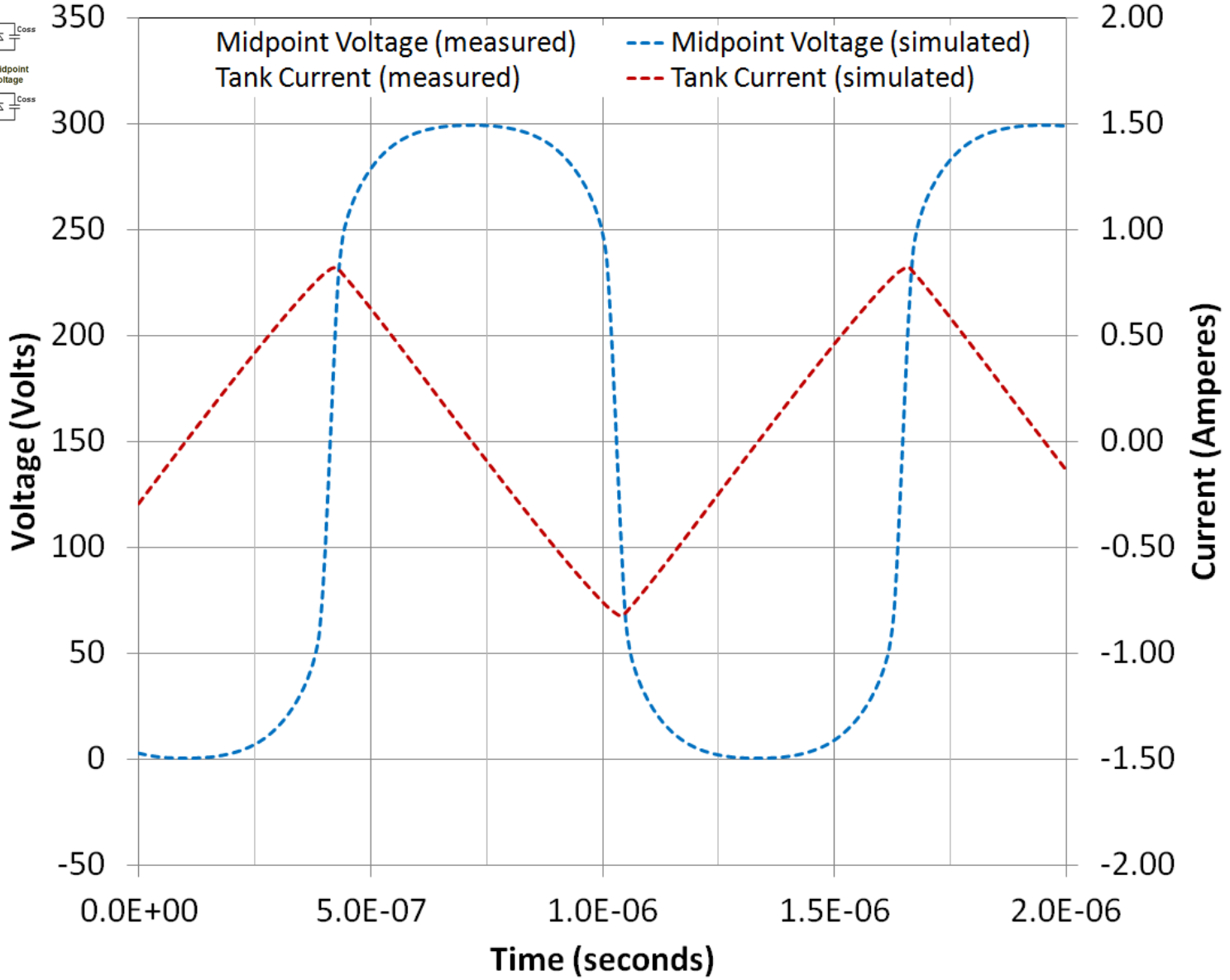
Measured and simulated waveforms show significant differences:

- Voltage waveform has dramatic asymmetry
- Voltage waveform has large voltage overshoot
- Notch at peak of tank current due to load inductance resonance



RHB Waveforms, MOSFET D – simulated





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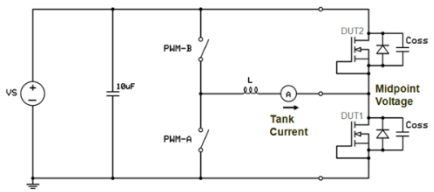
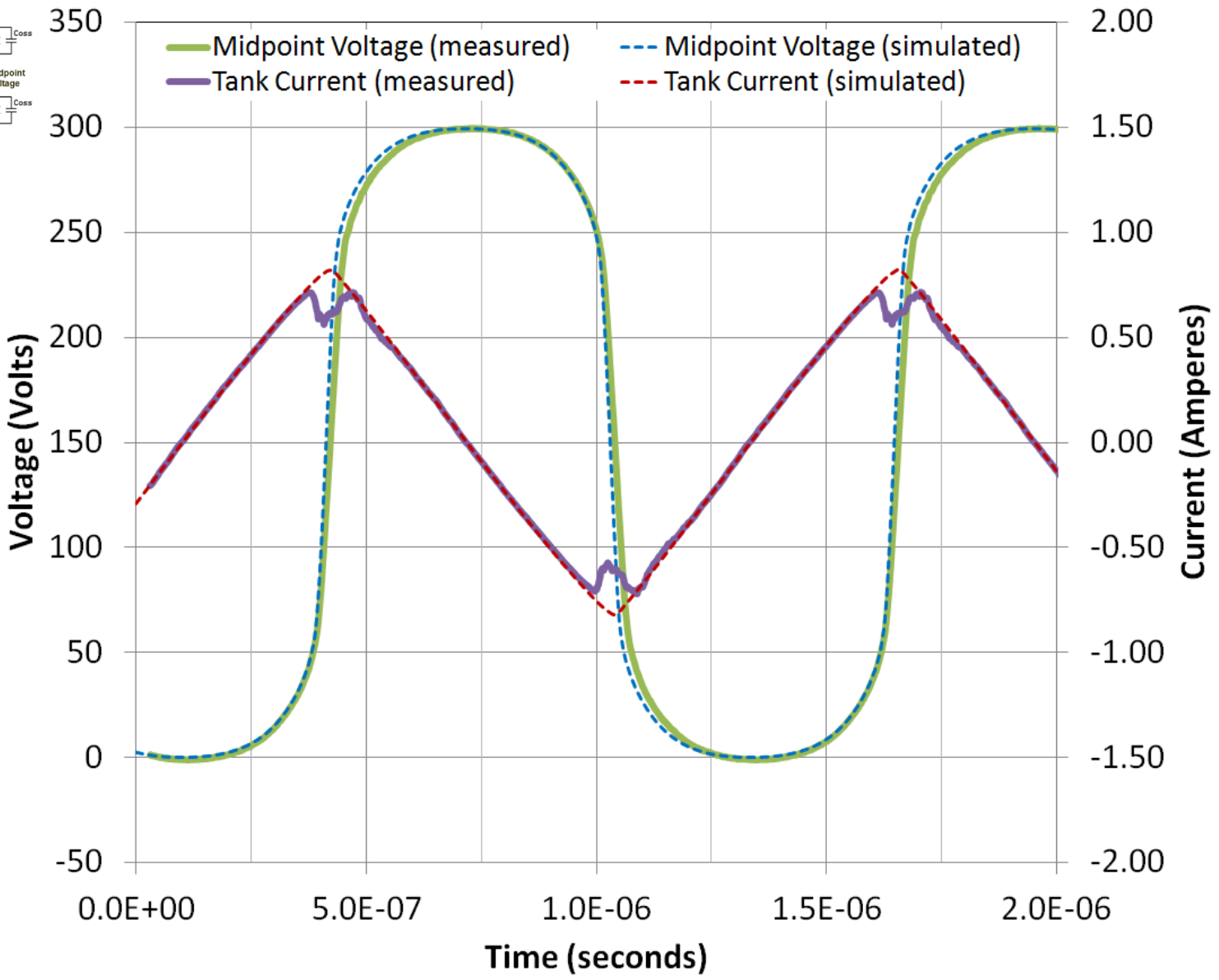
RHB Waveforms, MOSFET D – measured



Measured midpoint voltage still has some asymmetry, but is less pronounced



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Coss Energy Loss Definition

$$E_{dissipated} = \int_0^{V_{max}} C_{oss}(V_{DS})V_{DS}dV_{DS} - \int_{V_{max}}^{0} C_{oss}(V_{DS})V_{DS}dV_{DS}$$

Heat lost per switching cycle

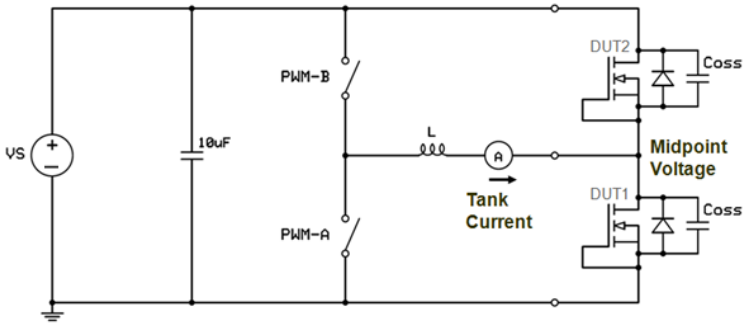
Energy to Charge

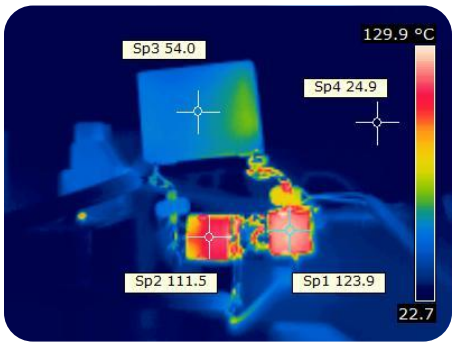
Energy to Discharge*

* This discharge energy is lost internally in hard-switched circuits when the MOSFET channel is turned on

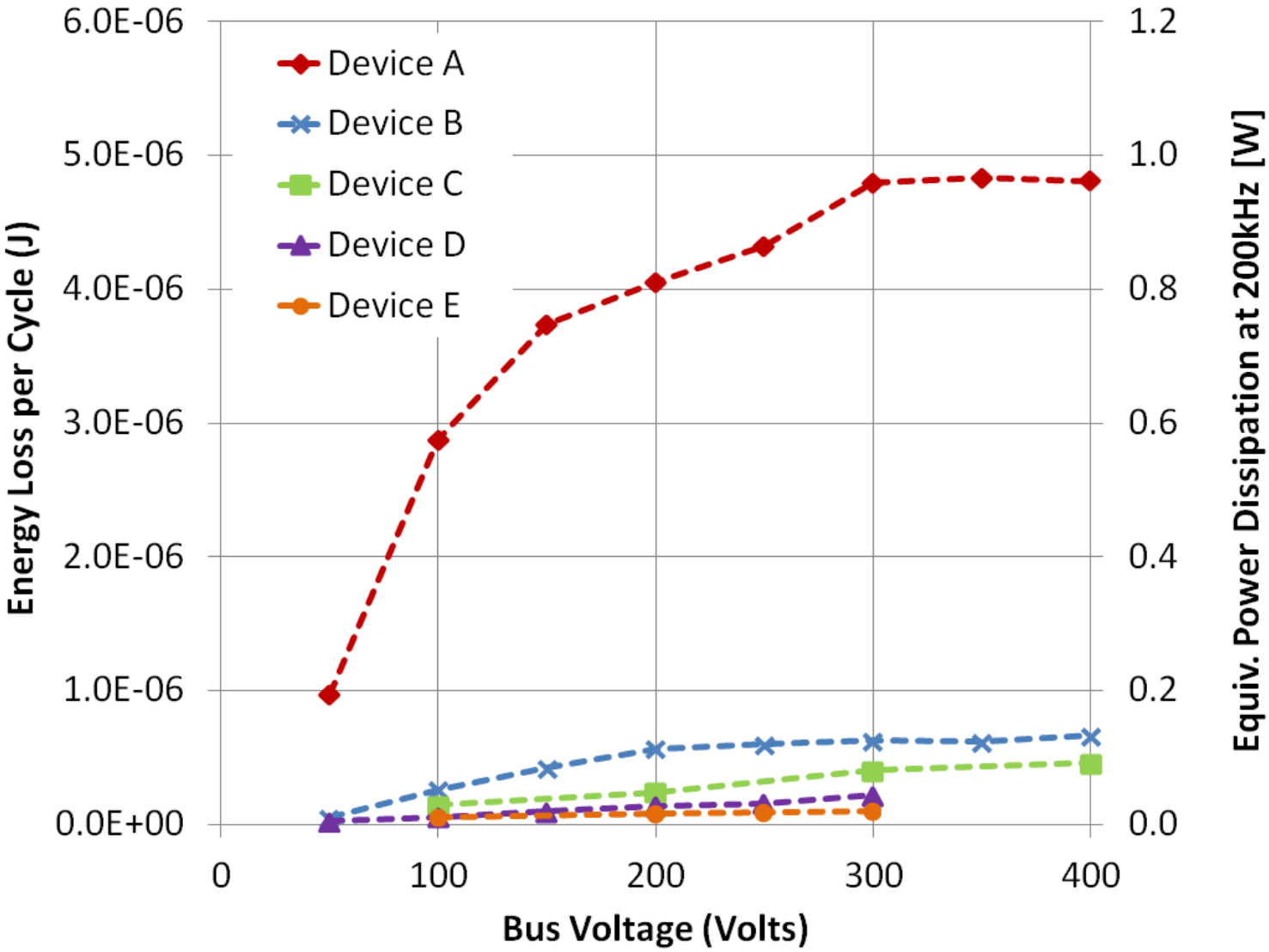
Calorimetry Method Used to Measure Coss Energy Loss

1. Determine the in-fixture steady-state $R_{th,CA}$ of each DUT
2. Apply a bus voltage, VS
3. Choose an appropriate test frequency and select a suitable power inductor L
4. Adjust the PWM drive frequency to above the resonant frequency until the magnitude of the midpoint voltage waveform equals the bus voltage
5. Measure the steady-state case temperature rise of the DUT above ambient, ΔT_{CA}
6. Calculate the energy loss per switching cycle: $$E_{dissipated} = \frac{\Delta T_{CA}}{f_{PWM} R_{th,CA}}$$

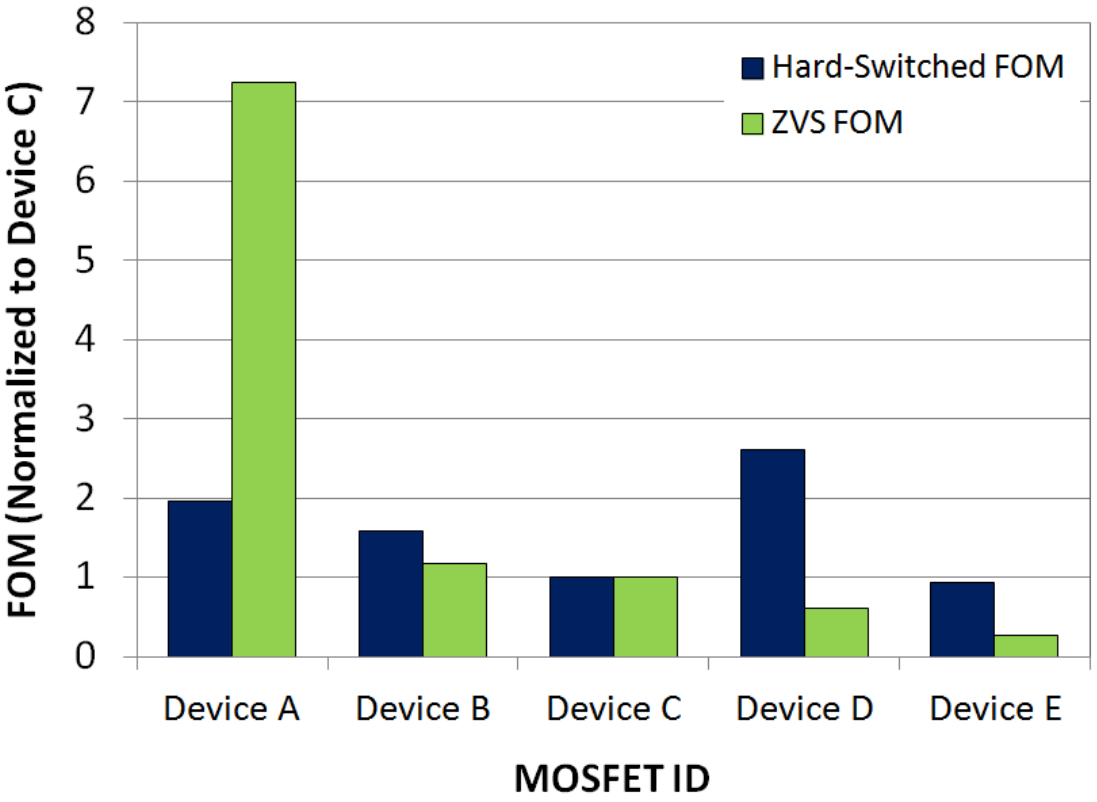




Measured Coss Energy Loss



Proposed ZVS Figure of Merit (lower is better)



Proposed ZVS figure of merit:

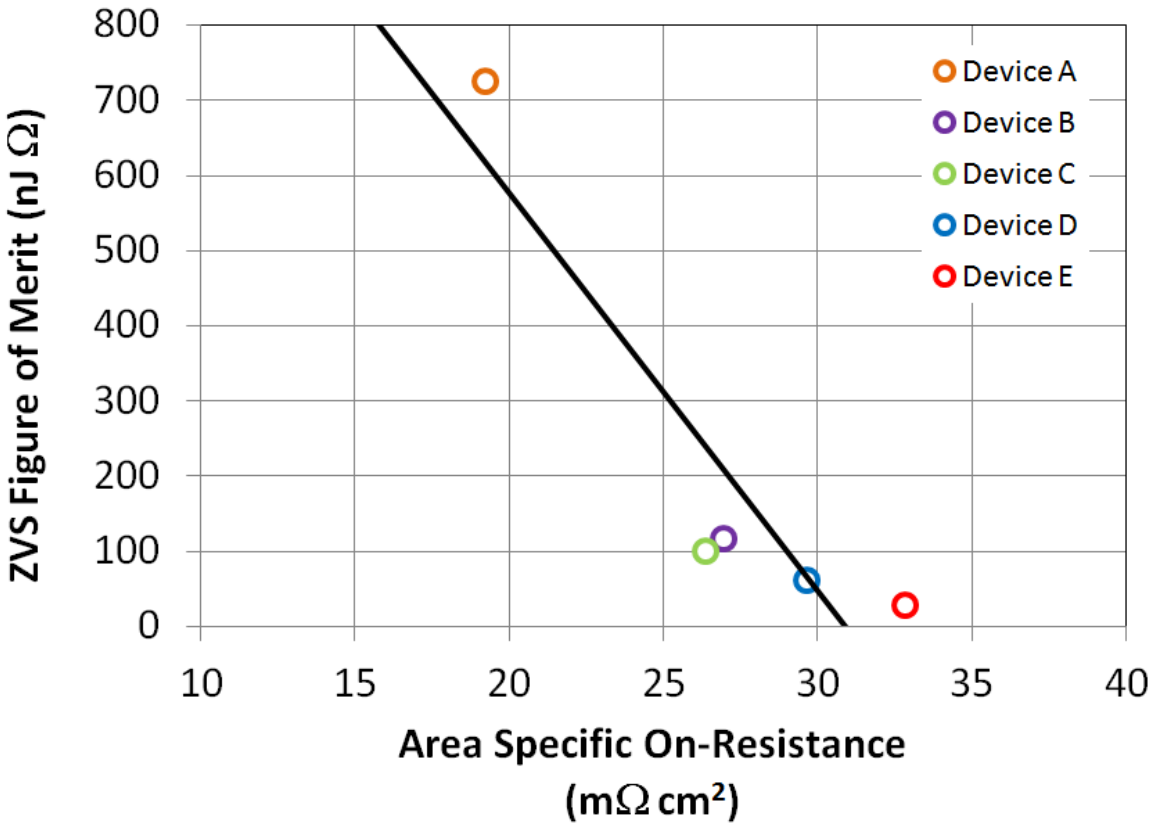
$$FOM_{ZVS} = R_{DSON} * (E_{dissipated} + E_{ciss})$$

$$E_{ciss} = \frac{1}{2} C_{iss} * V_{GS}^2$$

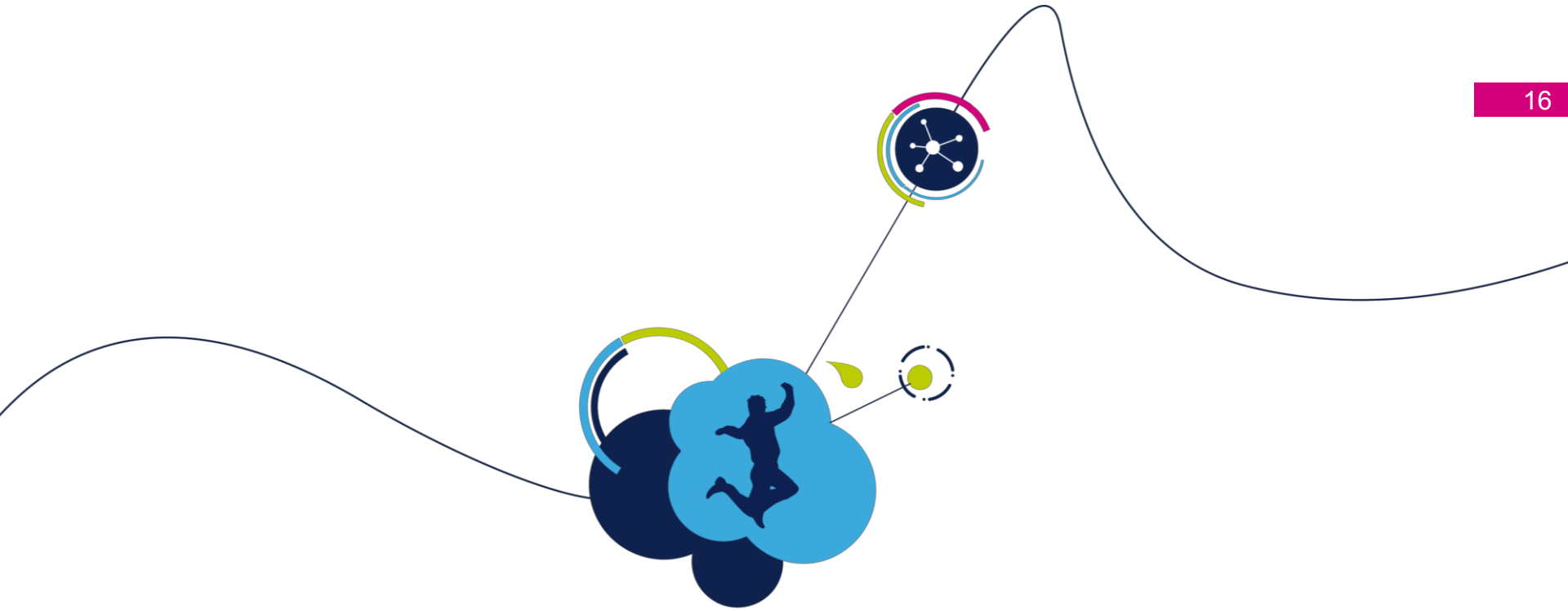
Conventional hard-switched figure of merit:

$$FOM_{HS} = R_{DSON} * Q_{gd}$$

ZVS Figure of Merit Versus Area Specific R_{DSON}



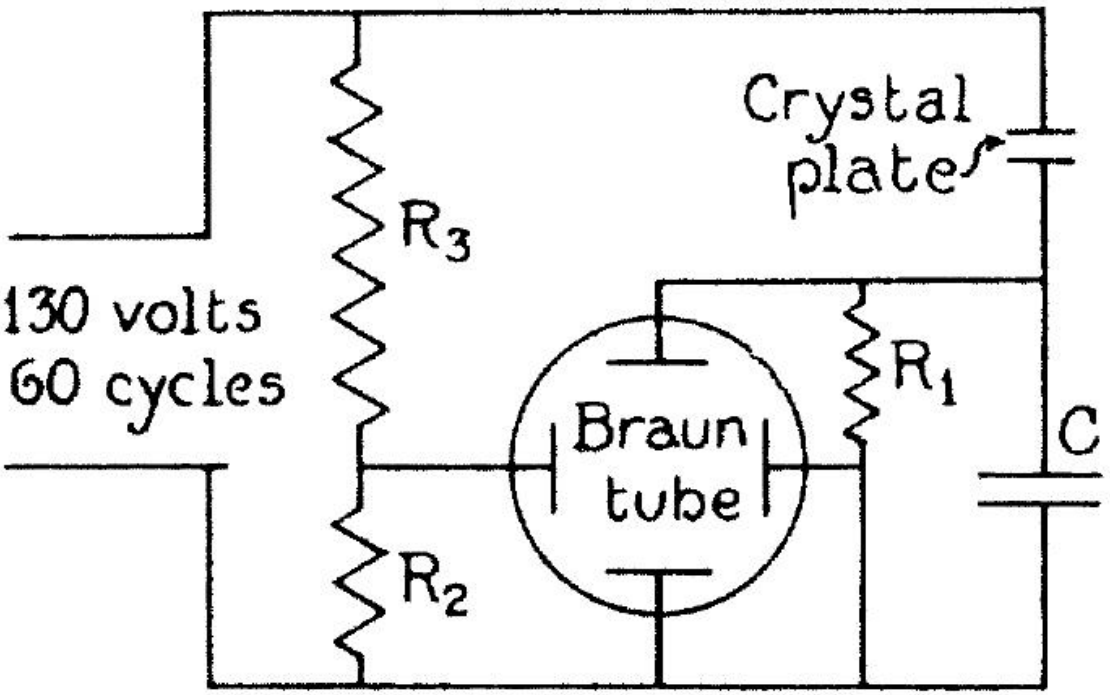
- FOM_{ZVS} gets worse as specific on-resistance decreases
- Specific on resistance decreases as superjunction column pitch decreases
- **However, there appears to be a tradeoff between high column density and good ZVS performance**

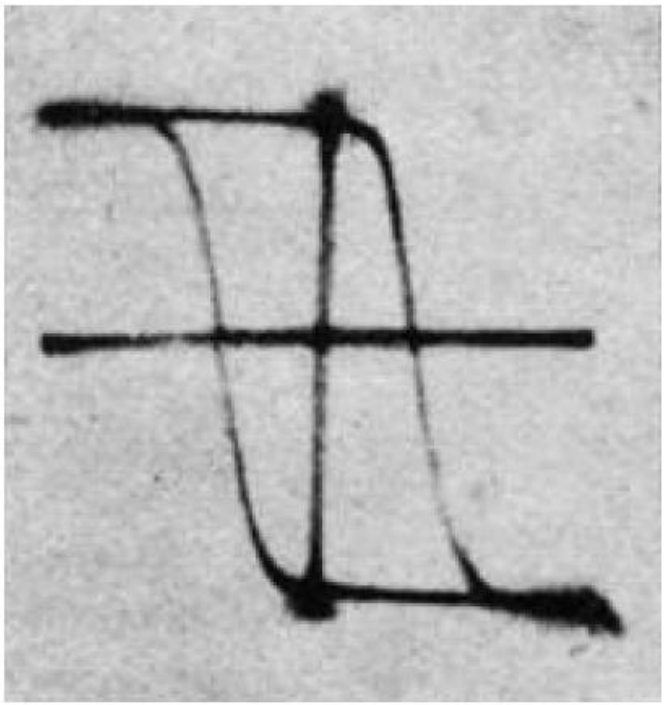


Results so far presented at APEC 2014

Further results presented at APEC 2016

Sawyer-Tower Test Fixture - 1930





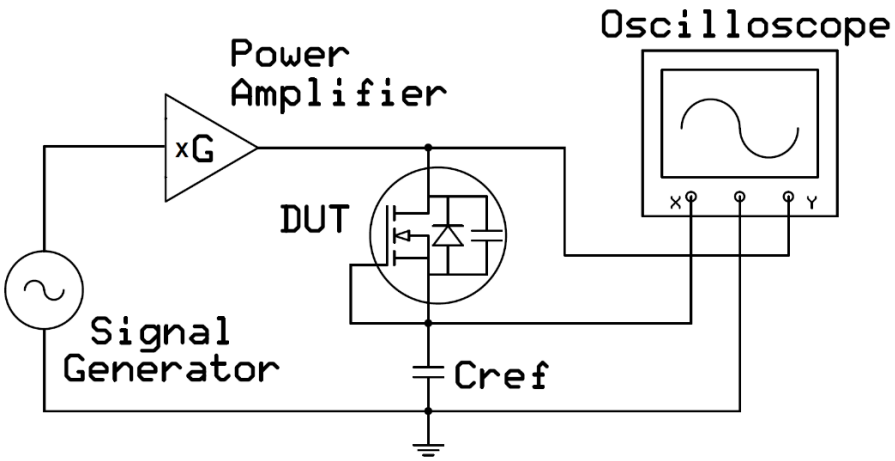
- Discovery of Ferroelectric behavior in Rochelle Salts by Sawyer & Tower 1930*
- Sawyer-Tower measurement method has been established as the only possible method for measuring capacitance if hysteresis present^
- Ceramic class-2 dielectric capacitors are Ferroelectric:
  - XR7, Z5U, Y5V, etc.

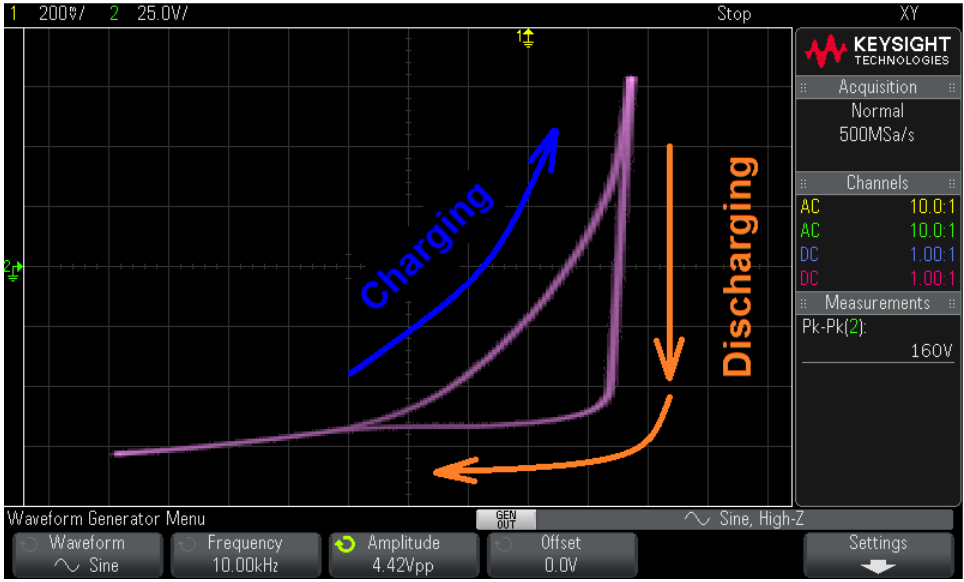
* C.B Sawyer, and C.H. Tower, "Rochelle Salt as a Dielectric," Physical Review, vol. 35, pp. 269-273, 1930

^ L.E. Mosley, and J.S. Schrader, "Hysteresis Measurements of Multi-Layer Ceramic Capacitors Using a Sawyer-Tower Circuit," CARTS USA 2007 Proceedings, pp. 309-319, Albuquerque, NM, 26-29 March 2007

Sawyer-Tower Test Fixture – 2015

https://github.com/SawyerTower





$Q_{OSS} = C_{Ref} V_X$ (Conservation of charge)

- Superjunction MOSFET output capacitance exhibits capacitive hysteresis
- Coss capacitance is consistent with Ferroelectric behavior*
  - Silicon is not a Ferroelectric dielectric
- Energy required to charge Coss is greater than energy returned during discharge:

$$E_{OSS,Charging} = \int_0^{Qmax} V_{DS}(Q_{OSS})\, dQ_{OSS} \qquad E_{OSS,Discharging} = \int_{Qmax}^0 V_{DS}(Q_{OSS})\, dQ_{OSS}$$

- Hysteresis energy lost to Joule heating:

$$E_{Hysteresis} = E_{OSS,Charging} + E_{OSS,Discharging}$$

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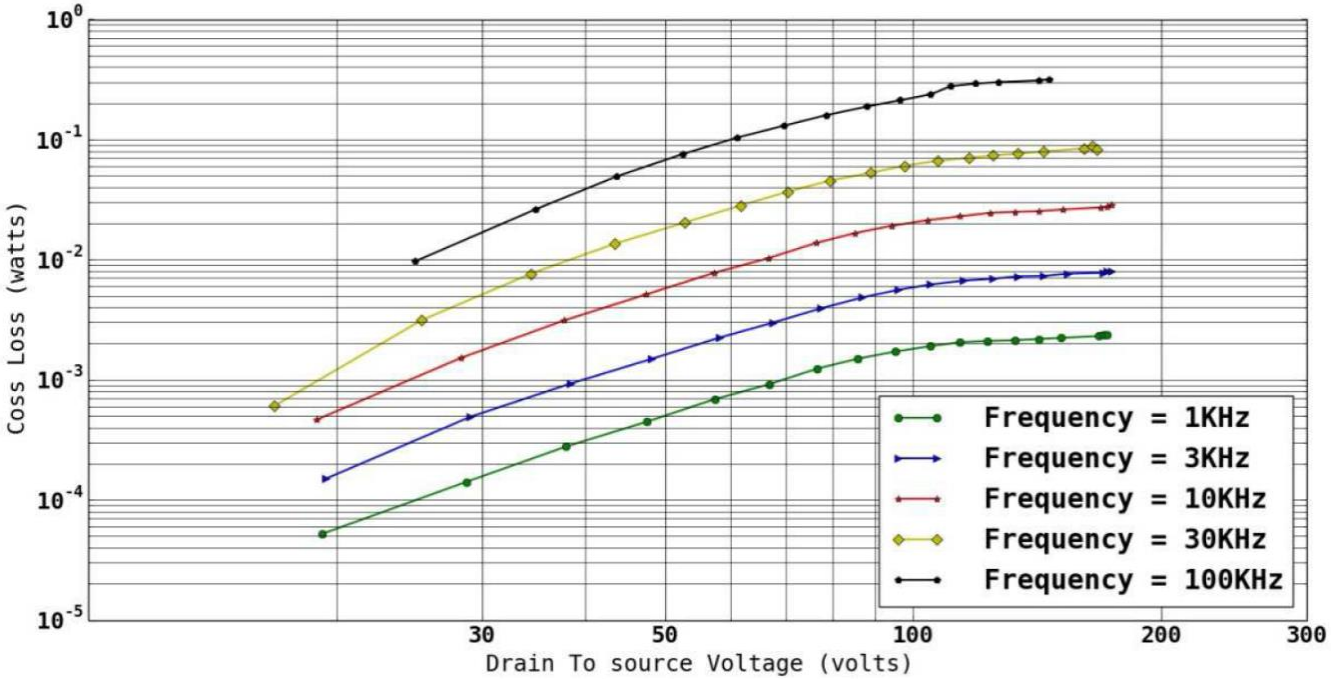
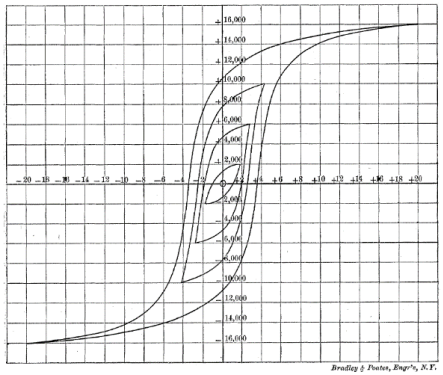
* J.F. Scott, “Ferroelectrics Go Bananas,” Journal of Physics: Condensed Matter, vol. 20, issue 2, 2008

Losses Presented on a Steinmetz Plot





- Steinmetz characterized magnetic hysteresis loss based on frequency and magnetic flux density*

$$P_{Hysteresis} = k\, f^{\alpha}\, V^{\beta}$$

- α = 1.04 ➔ hysteresis energy loss *per charge/discharge cycle* is almost independent of frequency
- β = 2.0 for low Vds reducing to 0.5 at higher Vds
  - Hysteresis is mainly a low Vds phenomenon – Consistent with pillar depletion voltage

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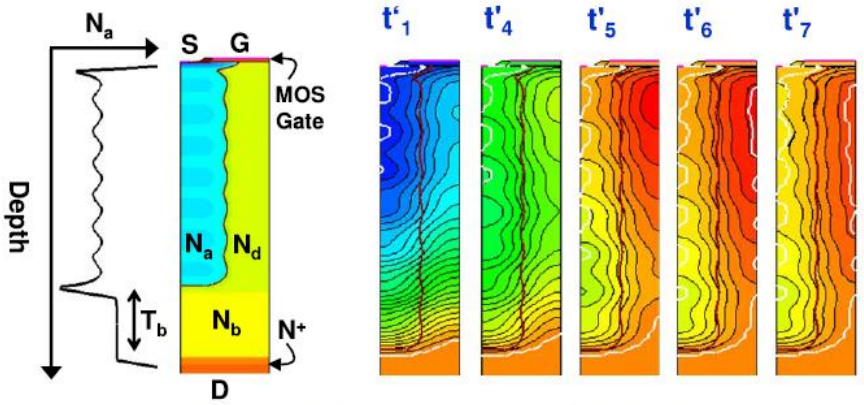
* C.P. Steinmetz, "On the Law of Hysteresis," AIEE Transactions, vol. 9, pp. 3-64, 1892

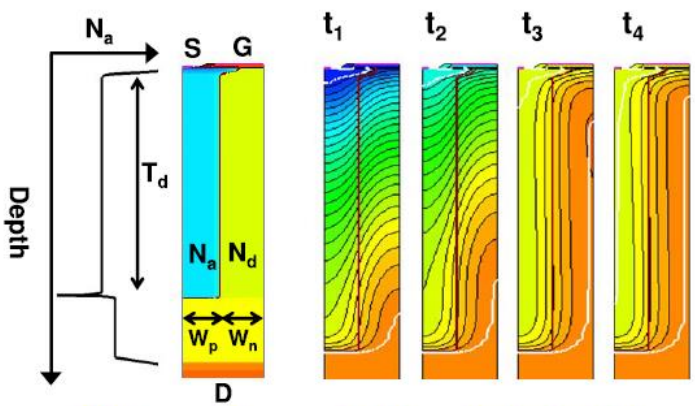
Explanation of Loss Mechanism:

"Origin of Anomalous COSS Hysteresis in Resonant Converters With Superjunction FETs"



"Device A" MEMI

	Value	Units
T_d	45	µm
T_b	12	µm
W_n	1.5	µm
W_p	1.5	µm
N_d	$8x10^{15}$	cm^{-3}
N_a	$8x10^{15}$	cm^{-3}
N_b	$2x10^{16}$	cm^{-3}



"Device C" TFEG

- Independent Researchers Jaume Roig and Filip Bauwens find a device level explanation for the existence of ferroelectric behavior in Superjunction structures*
  - Models based on the geometry of two devices are compared using TCAD simulation
  - A mechanism for “Islanded Charge” is discovered in the MEMI structure “Device A” during the period that charge depletion of the Superjunction pillars occurs (10V<Vds<20V) I.E. during Coss charging (Device turn-off)
  - Amount of “islanded charge” equates to observed Joule heating
- Power Semiconductor Industry has demonstrated that this loss mechanism can be mitigated in the MEMI structure through appropriate design

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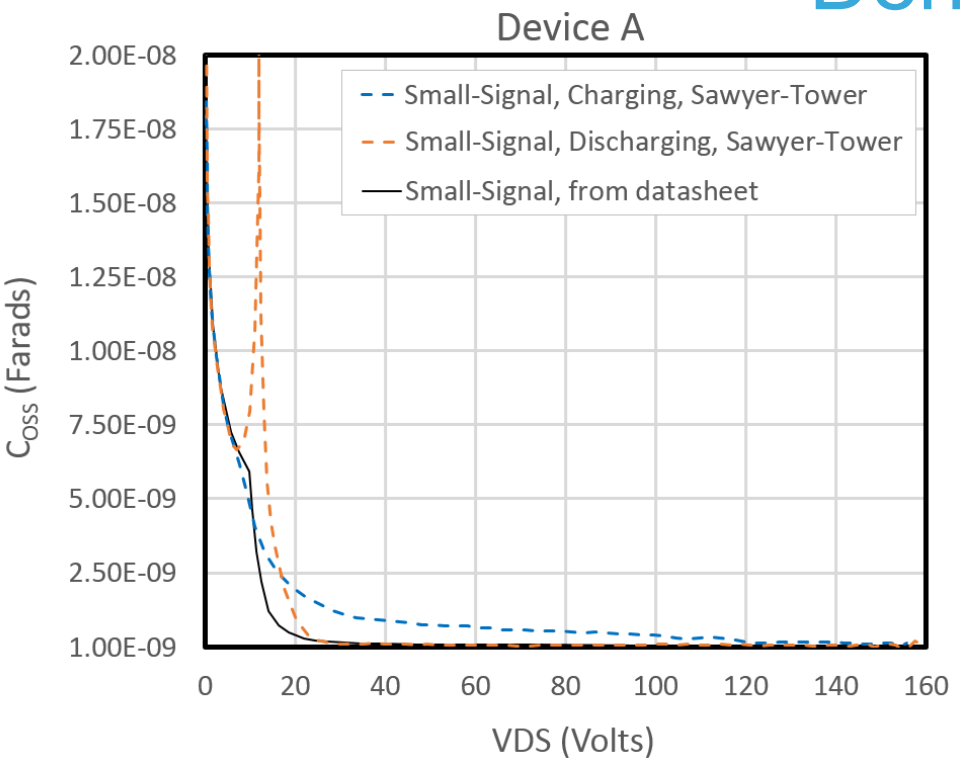
* J. Roig, F. Bauwens, "Origin of Anomalous COSS Hysteresis in Resonant Converters With Superjunction FETs," Electron Devices, IEEE Transactions on, vol.62, no.9, pp.3092-3094, Sept. 2015

Deriving Coss from Qoss



$$C_{oss_{Ls}} = \frac{Q_{OSS}}{V_{DS}}$$

$$C_{oss_{ss}} = \frac{dQ_{OSS}}{dV_{DS}}$$

- Data sheet Coss measurement is based on impedance analyzer results:
  - Provides a small signal Coss measurement
  - Can not measure capacitance accurately if hysteresis present
  - Presence of hysteresis causes a gross underestimation of Coss (Eoss, Qoss)
  - Hysteresis impact is a known limitation for impedance analyzer measurement*
- Capacitance artifact is at a Vds that is consistent with pillar depletion

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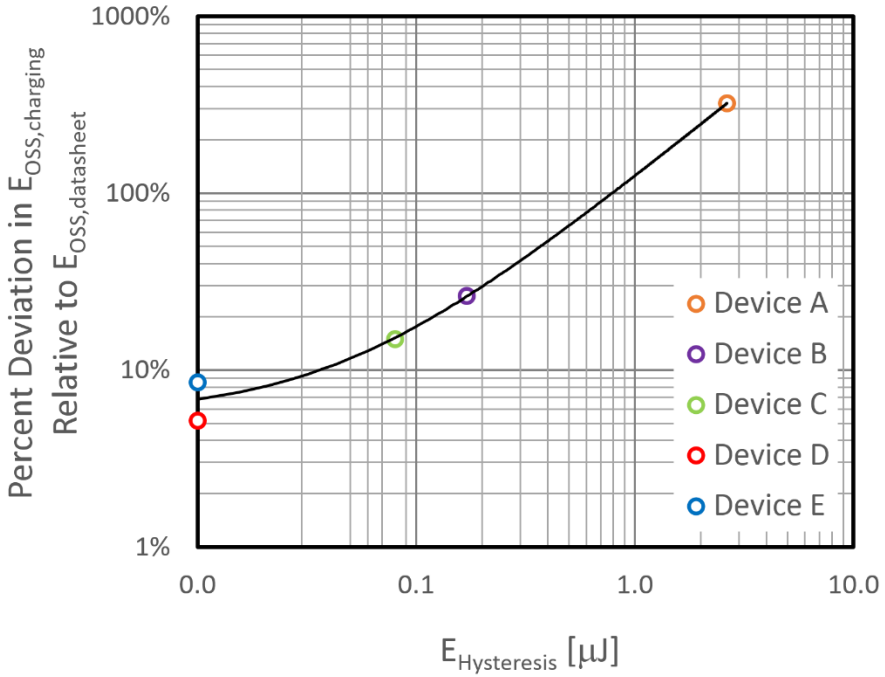
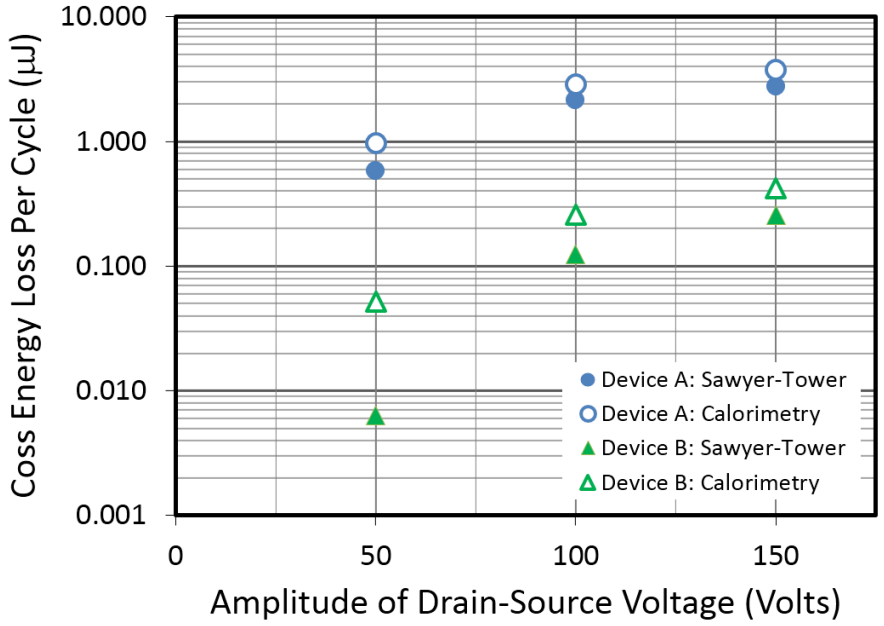
* L.E. Mosley, and J.S. Schrader, "Hysteresis Measurements of Multi-Layer Ceramic Capacitors Using a Sawyer-Tower Circuit," CARTS USA 2007 Proceedings, pp. 309-319, Albuquerque, NM, 26-29 March 2007

Interpreting the Results





- The greater the Coss hysteresis that is present in a SJ MOSFET the greater the discrepancy of Eoss between data sheet and reality
- Good agreement between Sawyer-Tower results and prior calorimetry results*

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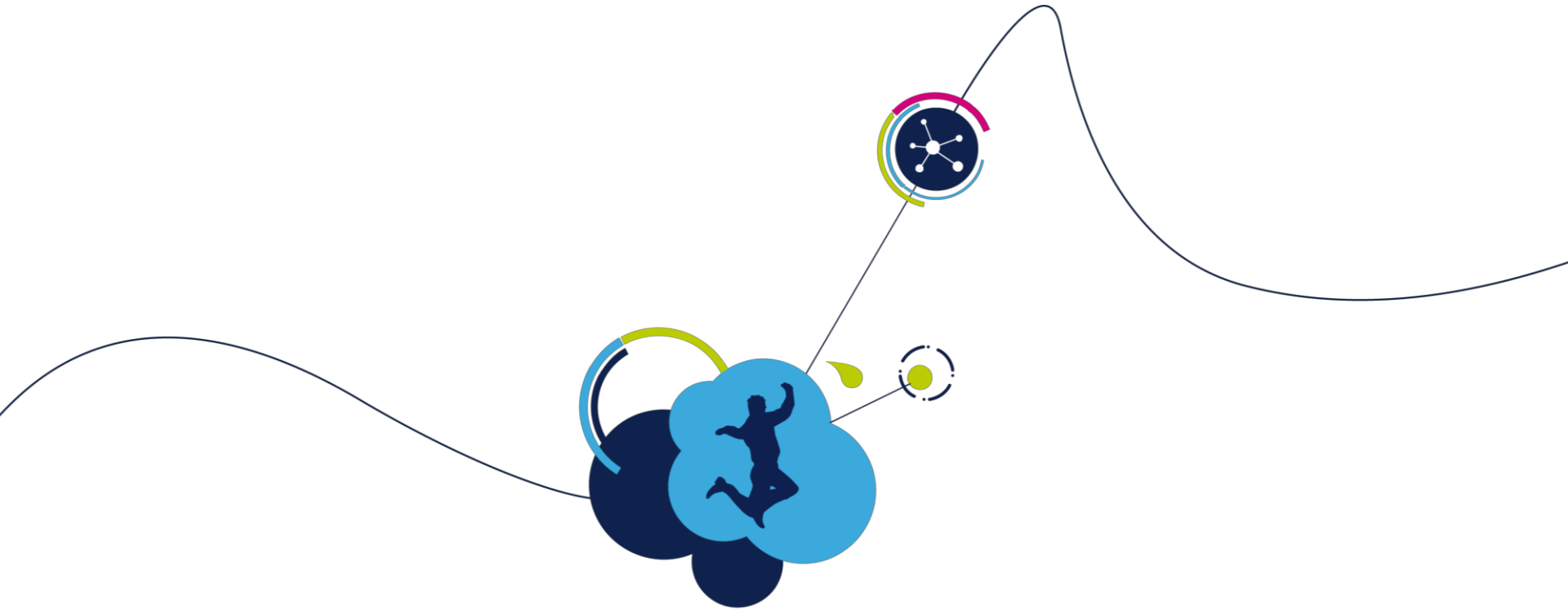
* J.B. Fedison, M. Fornage, M.J. Harrison, and D.R. Zimmanck, "Coss Related Energy Loss in Power MOSFETs Used in Zero-Voltage-Switched Applications," APEC 2014 Proceedings, pp. 150-156, 16-20 March 2014

Conclusions

- Advanced Superjunction MOSFETs have been shown to exhibit Coss hysteresis consistent with ferroelectric behavior
- Impedance analyzers are inappropriate for measuring Coss of advanced SJ MOSFETs:
  - Unable to identify the presence or degree of hysteresis
  - Capacitive hysteresis (ferroelectric behavior) creates significant measurement error
  - Can produce misleading, grossly optimistic measurements for Coss, Eoss, & Qoss
  - This measurement limitation is well understood within the electronics industry with ferroelectric capacitors
  - Small signal derived capacitance is not relevant for a switched mode (large signal) application
- Coss measurement error could misguide the advancement of Superjunction design:
  - Degree of Coss hysteresis increases as Superjunction design advances to finer geometry
  - Increased hysteresis results in lower Coss, Eoss, & Qoss measurements
- Power semiconductor industry has acknowledged this problem and are addressing it in the latest Superjunction MOSFET designs

Recommendations to The Power Semiconductor Industry

- Dispense with irrelevant and erroneous impedance analyzer based Coss measurements
- Adopt the Sawyer-Tower circuit for measuring Qoss for Superjunction MOSFETs
- Provide plots of both the Qoss charge and discharge curves in MOSFET data sheets
- Derive all MOSFET Figures of Merit – Eoss, Qoss & derivatives from Sawyer-Tower measurements



Questions

Bay Area PELS presentation

Venue: ON Semi, 3001 Stender Way, Santa Clara, CA95054

Date: 23rd February 2017 - 7:00PM

Format: 50 minute presentation followed by 10 minutes Q&A

Abstract:

This presentation explores a previously unrecognized loss mechanism that has become prevalent with the on-going advancement of superjunction MOSFET technology. The presentation starts by demonstrating a general method to measure the output capacitance (Coss) related energy loss per switching cycle in power MOSFETs used in zero-voltage-switched (ZVS) applications. It is shown that a simple model using Coss in series with a resistance Ross is inadequate for describing the observed energy loss and a different model is needed. This work also shows that the traditional hard-switched test methods for measuring the dynamic performance of power MOSFETs are inadequate for describing the dynamic performance of power MOSFETs used in ZVS applications.

The presentation then introduces a Sawyer-Tower circuit which is employed to characterize the output capacitance (COSS) of advanced superjunction MOSFETs. It is shown that some of the most advanced superjunction MOSFETs exhibit significant hysteresis in their output capacitance which leads to unrecoverable power loss. This work shows that the conventional impedance analyzer method can only measure COSS accurately when hysteresis is not present while measurement of COSS with a Sawyer-Tower circuit gives accurate results regardless of whether hysteresis is present or not. Accurate measurement of COSS with a Sawyer-Tower circuit not only enables designers to more accurately calculate and predict power loss but even more importantly allows the power semiconductor industry to more effectively advance future generations of superjunction MOSFETs for optimum efficiency, especially for use in resonant converter applications.

About the speaker:

Michael Harrison received the NZCE degree from AUT University, New Zealand in 1988 and the BE degree from the University of Auckland, New Zealand in 1991. He is currently employed by ST Microelectronics in the capacity of Senior Applications Manager with a focus on Power Electronics Applications.

He holds over 30 international patents related to switched mode power conversion techniques. In previous employment, he has been involved in the research and development of Photo-Voltaic Micro-Inverters, telecommunications power conversion rectifiers, grid-tied inverters for distributed generation applications, and single-stage single-phase power-factor corrected converters.

Original APEC presentation abstracts:

Coss Related Energy Loss in Power MOSFETs Used in Zero-Voltage-Switched Applications

The Applied Power Electronics Conference and Exposition (APEC) March 2014

This paper presents a general method to measure the output capacitance (Coss) related energy loss per switching cycle in power MOSFETs used in zero-voltage-switched (ZVS) applications. It is shown that a simple model using Coss in series with a resistance Ross is inadequate for describing the observed energy loss and a different model is needed. This work also shows that the traditional hard-switched test methods for measuring the dynamic performance of power MOSFETs are inadequate for describing the dynamic performance of power MOSFETs used in ZVS applications. Finally, this study proposes a new power MOSFET figure of merit suitable for differentiating the performance of MOSFETs for use in ZVS applications.

Coss Hysteresis in Advanced Superjunction MOSFETs

The Applied Power Electronics Conference and Exposition (APEC) March 2016

In this work, a Sawyer-Tower circuit is employed to characterize the output capacitance (COSS) of advanced superjunction MOSFETs. It is shown that some of the most advanced superjunction MOSFETs exhibit significant hysteresis in their output capacitance which leads to unrecoverable power loss. This work shows that the conventional impedance analyzer method can only measure COSS accurately when hysteresis is not present while measurement of COSS with a Sawyer-Tower circuit gives accurate results regardless of whether hysteresis is present or not. Accurate measurement of COSS with a Sawyer-Tower circuit not only enables designers to more accurately calculate and predict power loss but even more importantly allows the power semiconductor industry to more effectively advance future generations of superjunction MOSFETs for optimum efficiency, especially for use in resonant converter applications.