Common Mode EMI Analysis and Mitigation Methods in Three-Phase Inverters

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Overview

- Conducted EMI in Power Converters
  - Definitions
  - Common Mode EMI and Solutions
  - Modeling Common Mode Emissions
- Eliminating Common Mode Voltage in Three-Phase Inverters
  - Meeting the Common Mode Emission Limits in MIL-STD-461G
  - Grid-Forming Inverters with Sigma-Delta Modulation
  - Grid-Following Inverters with PDM
  - Application to Motor Drives
- Conclusions and Future Work
- References

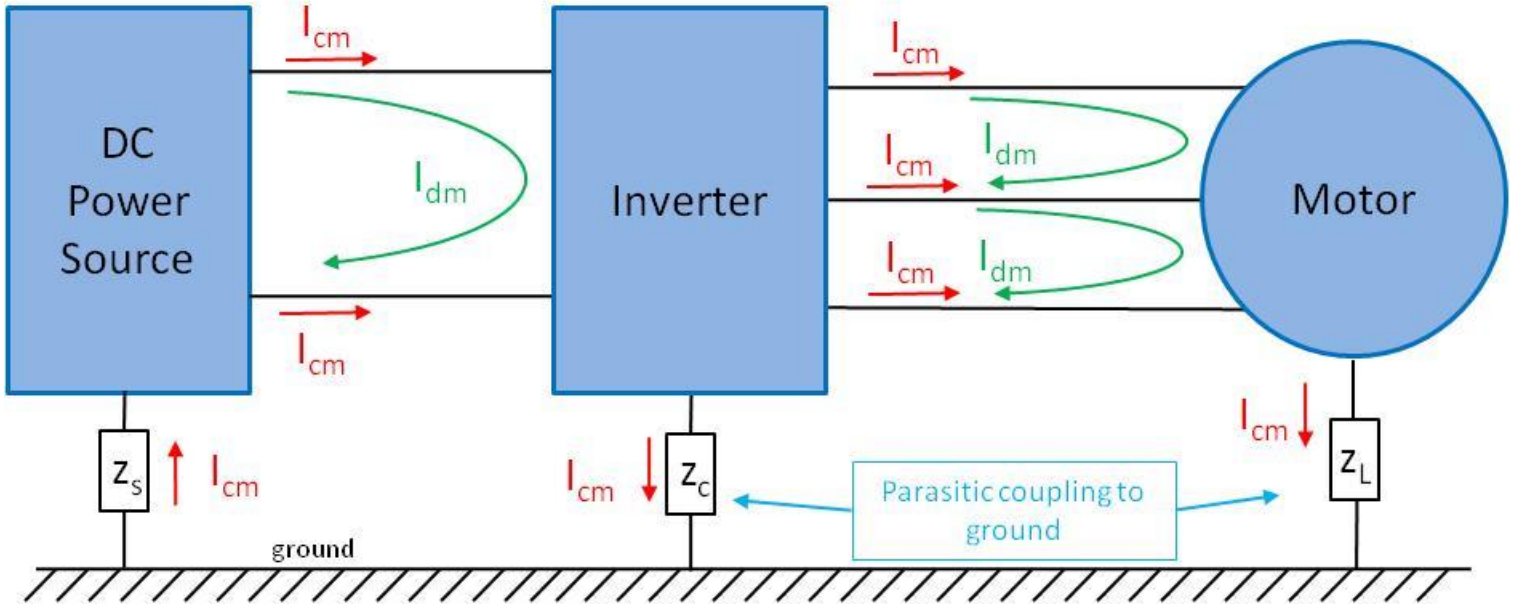
Definitions

- Electromagnetic Interference (EMI) - degradation of the performance of an equipment, transmission channel or system caused by an electromagnetic disturbance
  - can be **conducted** current that couples into other parts of an electrical system
  - or **radiated** electrical and magnetic fields that can potentially couple into nearby circuits
- Electromagnetic compatibility (EMC) - ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment

Ref: European Committee for Electrotechnical Standardization (CENELEC) Guide 24

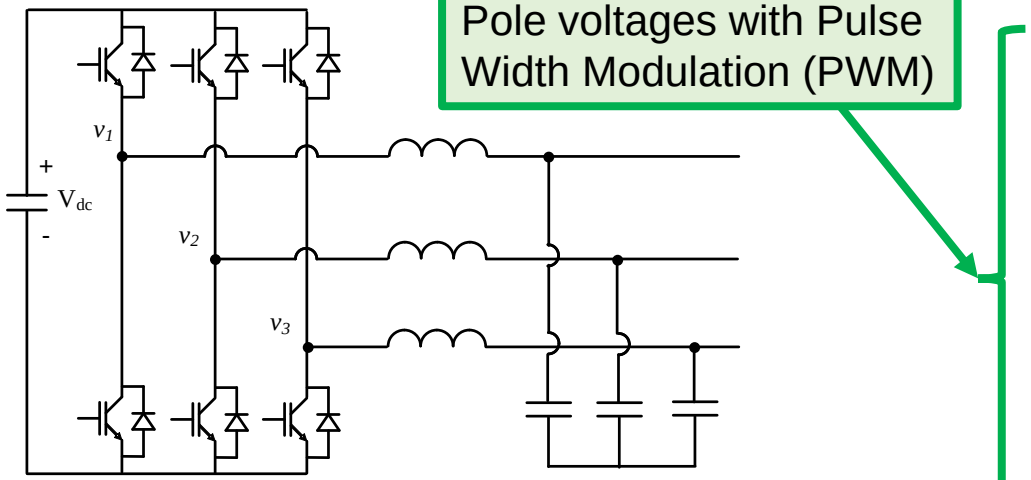
Differential Mode vs Common Mode

- Differential mode (DM) currents flow from and return to their source of origin and contain undesired high frequency components
- Common mode (CM) currents flow in the same direction through capacitive coupling to ground



CM Voltage in Three–Phase Inverters

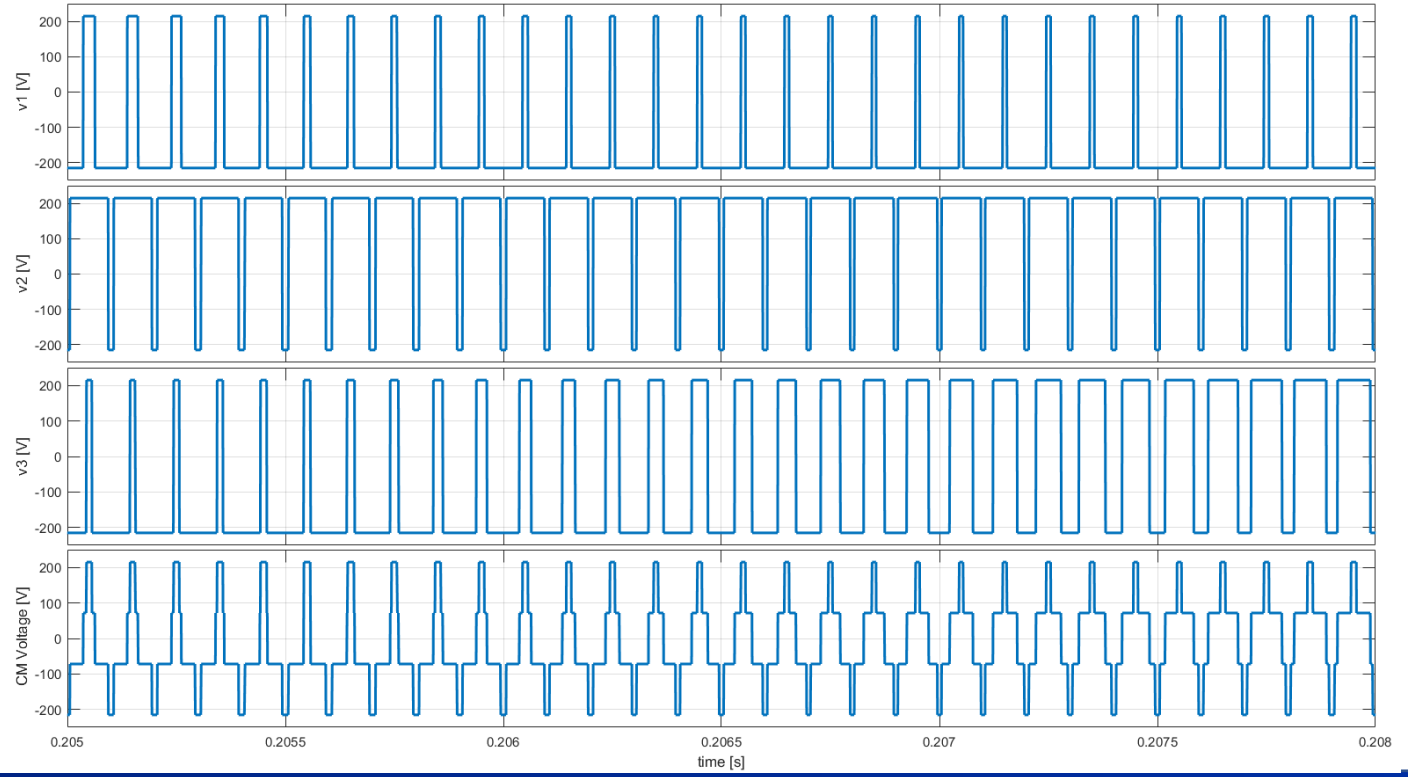
- The CM voltage generated by switching power converters can cause unwanted currents to circulate in ground paths
- CM currents can trip ground faults relays, damage motor bearings and produce radiated emissions



Pole voltages with Pulse Width Modulation (PWM)

CM Voltage

$$v_{CM} = \frac{v_1 + v_2 + v_3}{3}$$



Limits and Standards

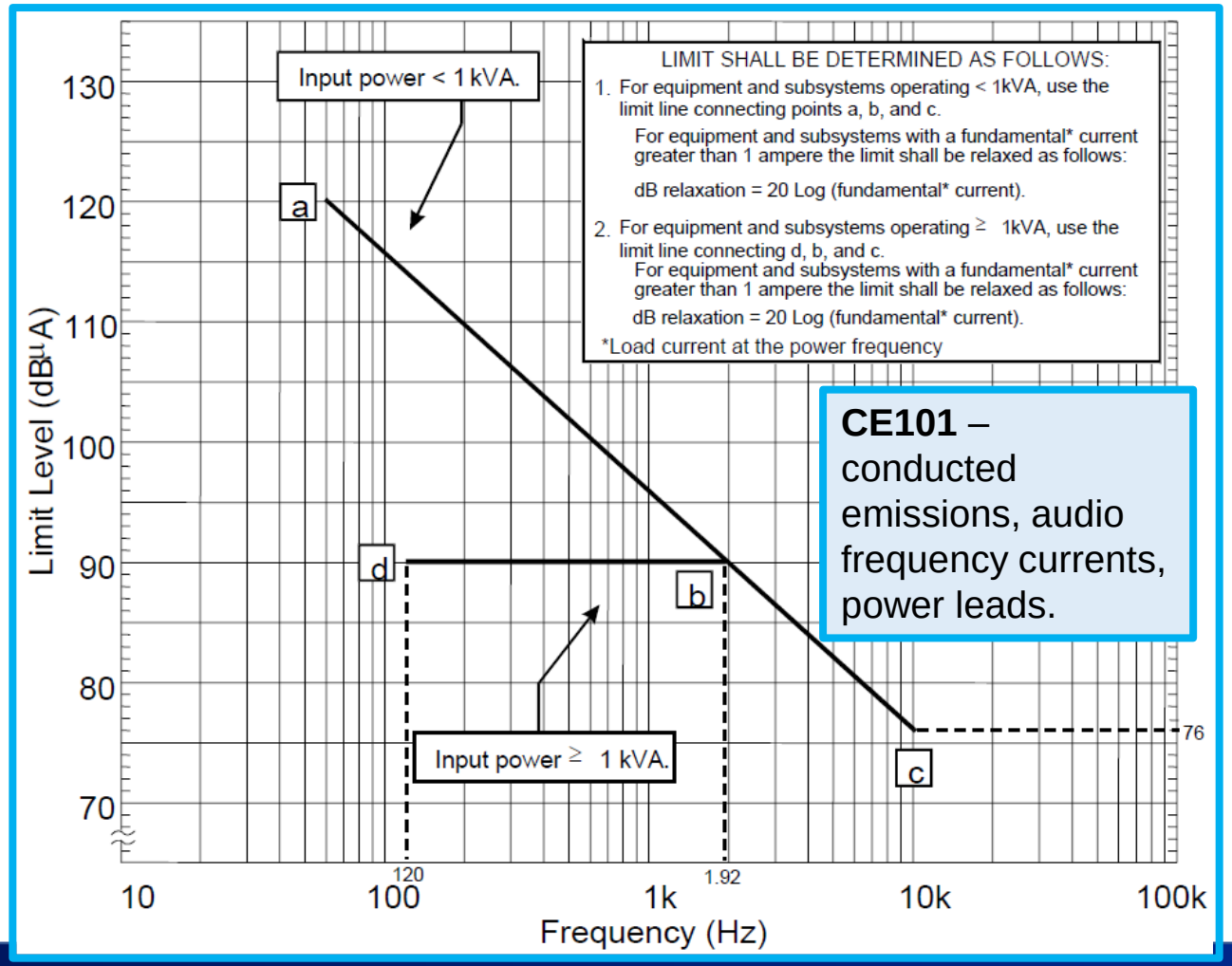
- Conducted EMI limits for commercial products are set by the FCC in the US and by CISPR and IEC in Europe, as examples
- Specific standards for commercial transportation applications include automotive (SAE J1113 and IEC CISPR25) and aviation (RTO -DO160-G)
- Military Standard 461G regulates conducted and radiated EMI for shipboard and aerospace applications, with the most stringent EMI limits
- Power converters onboard military ships must meet simultaneously the CE limits in MIL-STD-461G as well as the power quality limits in MIL-STD-1399, part 300 section 1 for low voltage AC applications, as examples

MIL-STD-1399 Section 300 Part 1

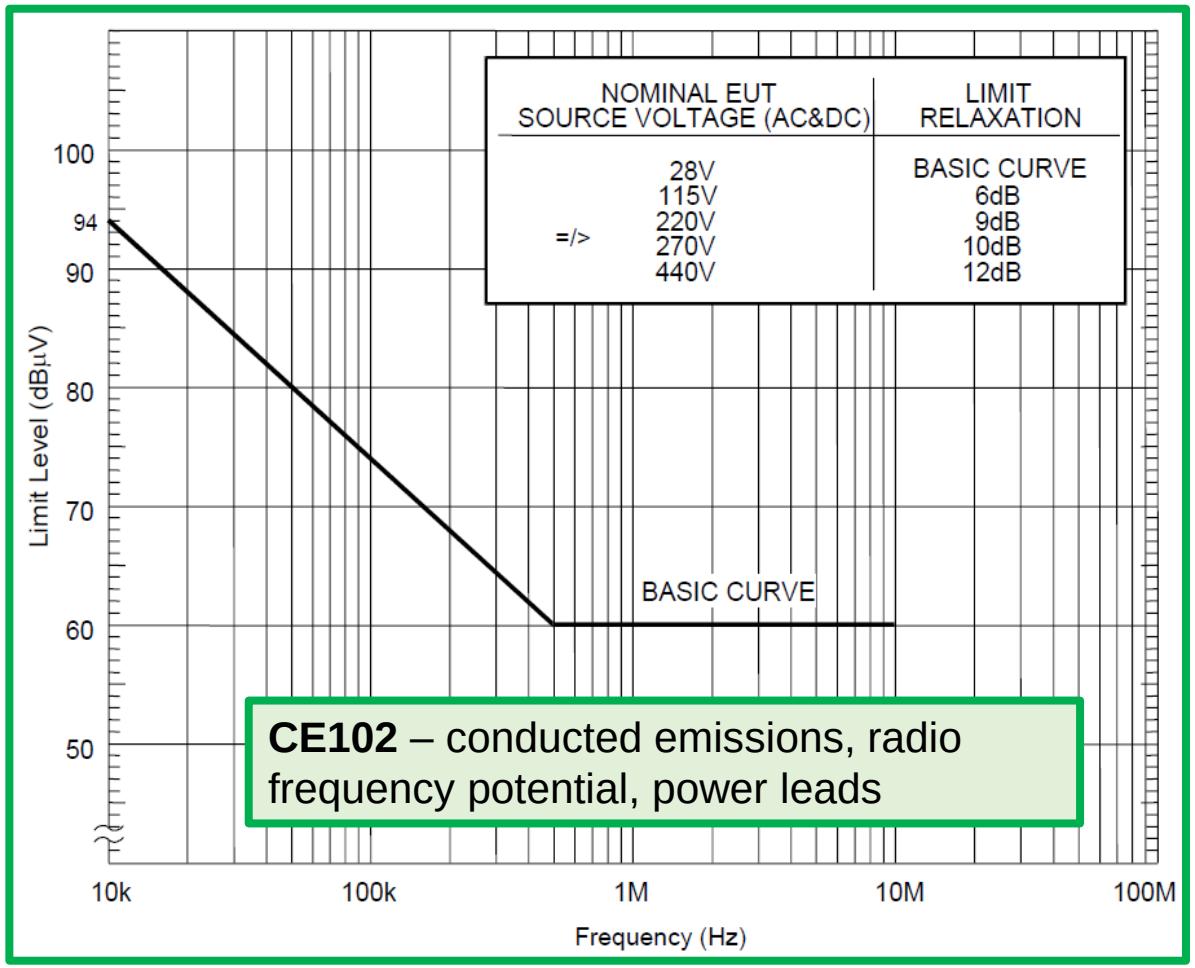
- Shipboard power systems use three-phase four-wire service for unbalanced and non-linear loads to meet the power quality requirements in MIL-STD-1399 section 300 part 1 “Low Voltage Electric Current, Alternating Power” – Sep 2018

Characteristics	Type I	Type II	Type III
Frequency			
1. Nominal Frequency	60 Hz	400 Hz	400 Hz
2. Frequency Modulation	0.5%	0.5%	0.5%
3. Frequency Tolerance	±3% (Submarines: ±5%)	±5%	±0.5%
4. Frequency Transient Tolerance	±4%	±4%	±1%
Voltage			
7. Designated Nominal User Voltage	440, 115, 115/200 V_{rms}	440, 115 V_{rms}	440, 115, 115/200 V_{rms}
8. Line-to-Line Voltage Unbalance	3% (Submarines: 0.5% for 440 V_{rms}; 1% for 115 V_{rms})	3%	2%
9. Voltage Modulation	2%	2%	1%
10. Average Line-to-Line Voltage from Nominal Tolerance	±5%	±5%	±2%

MIL-STD-461G "Requirements for the Control of EMI characteristics of subsystems and equipment" –2015

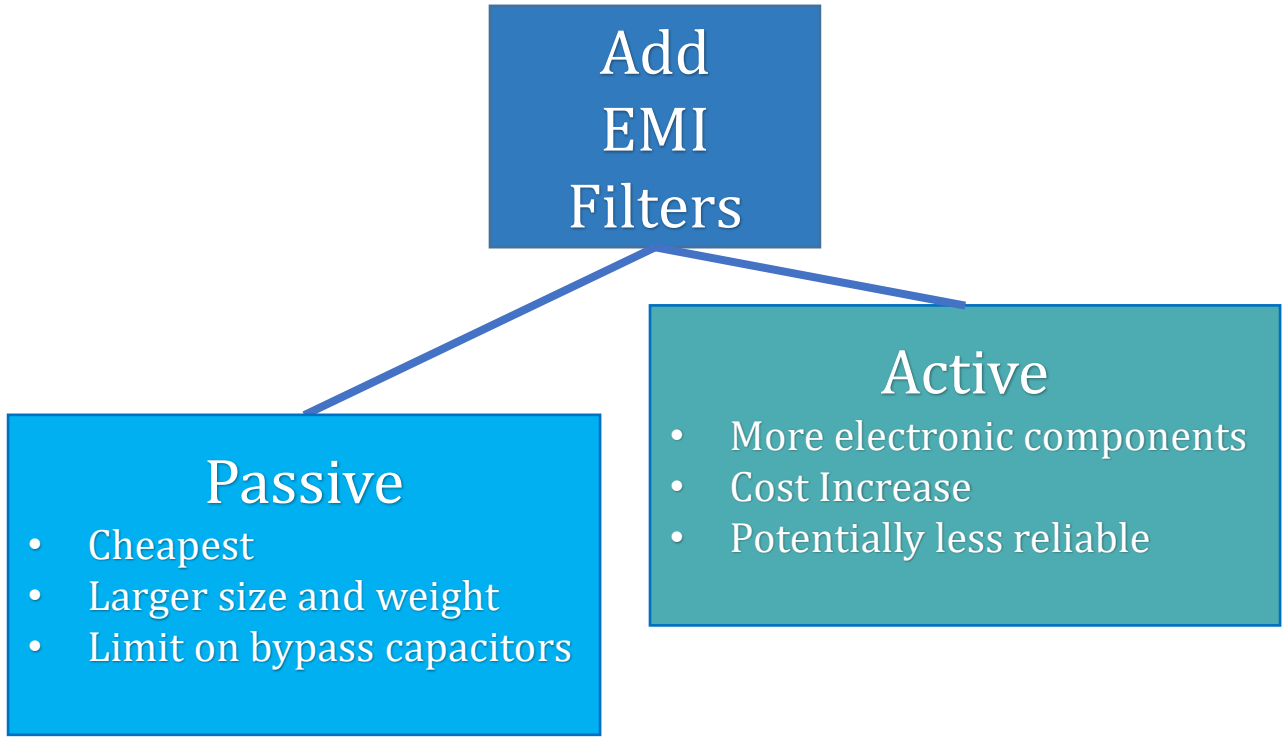


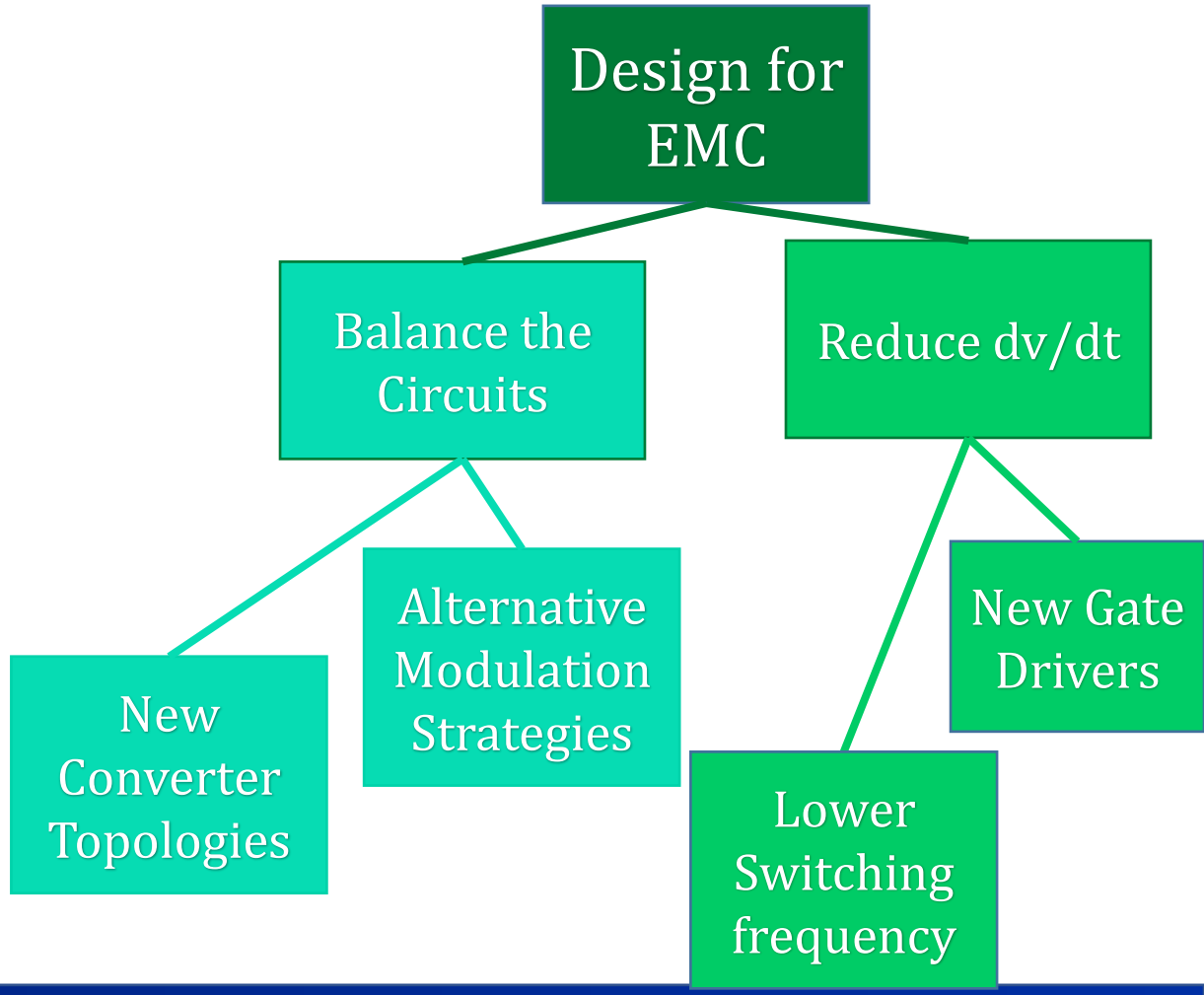
CE101 – conducted emissions, audio frequency currents, power leads.



CE102 – conducted emissions, radio frequency potential, power leads

Solutions to Reduce Conducted CM EMI





Modeling CM is key to designing for EMC

Background

- The four-leg inverter is an alternative topology to the traditional three-leg three-phase voltage source inverter (VSI)
- In the late-1990s a four-leg inverter was demonstrated* to suppress CM conducted emissions when the appropriate modulation strategy is adopted
- Pulse density modulation (PDM) was typically used for soft-switching inverters and today we are revisiting its application to hard-switching inverters thanks to the availability of wide bandgap devices (WBG)
- The goal is to increase the power density of power converters by eliminating large CM chokes and bypass capacitors and still meet the conducted EMI limits in MIL-STD-461G

*A.L. Julian, G. Oriti, T.A. Lipo, "Elimination of common mode voltage in three phase sinusoidal power converters", IEEE Trans. on Power Electronics, Vol.14, No 5, Sep.1999.

Modeling to Include CM

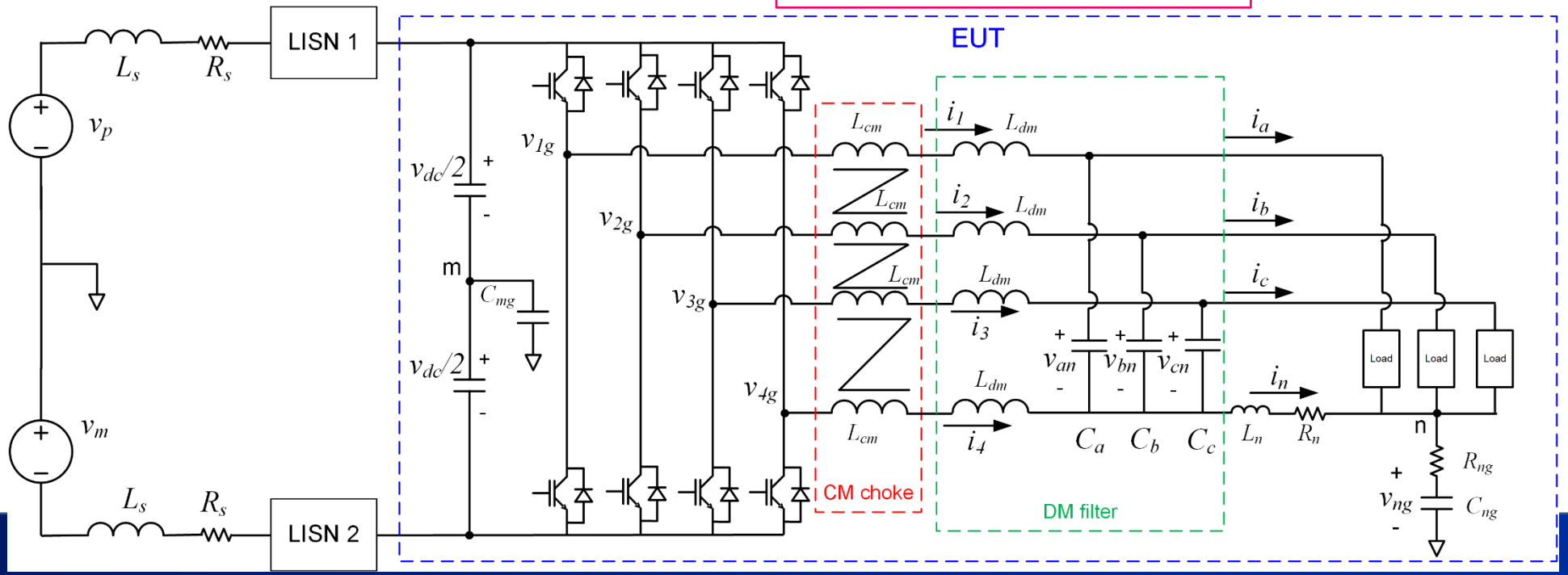
- Three-phase, four-wire VSI without CM Voltage
- CM, DM filters and LISN
- State space equations of AC bus:

$$\mathbf{x} = \begin{bmatrix} i_1 & i_2 & i_3 & i_4 & i_a & i_b & i_c & v_{an} & v_{bn} & v_{cn} & v_{ng} \end{bmatrix}^T$$

$$\mathbf{u} = \begin{bmatrix} v_{1g} & v_{2g} & v_{3g} & v_{4g} \end{bmatrix}^T$$

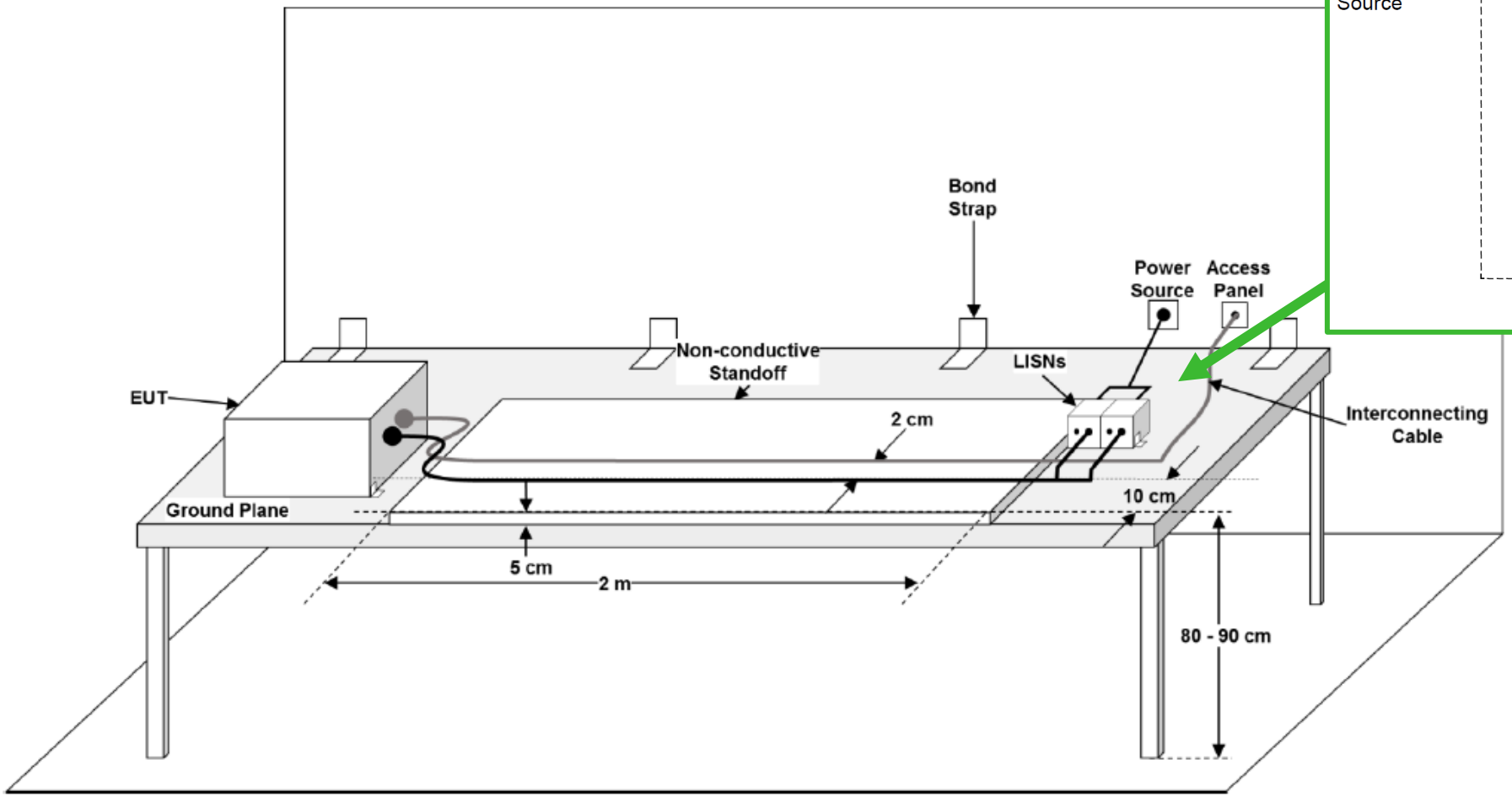
$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}$$

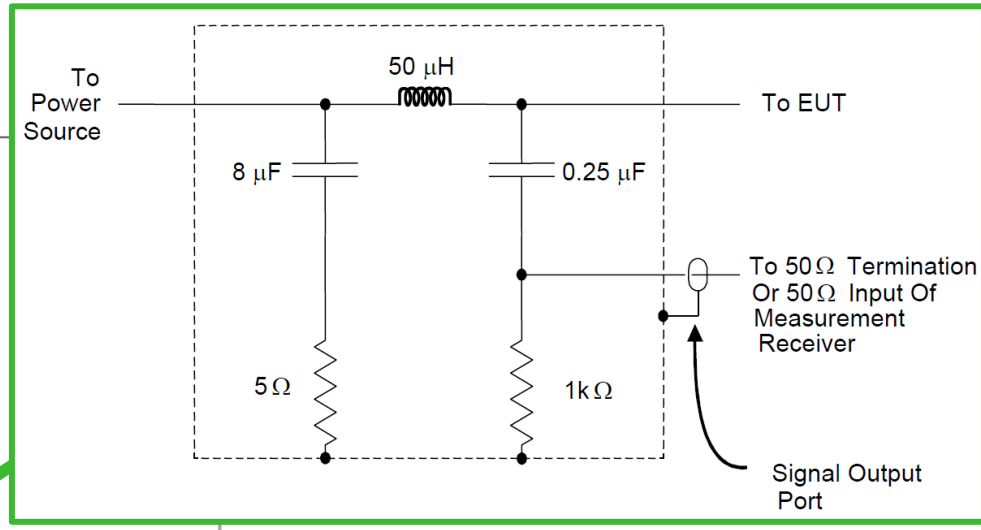
$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u}$$



MIL-STD-461G General Setup

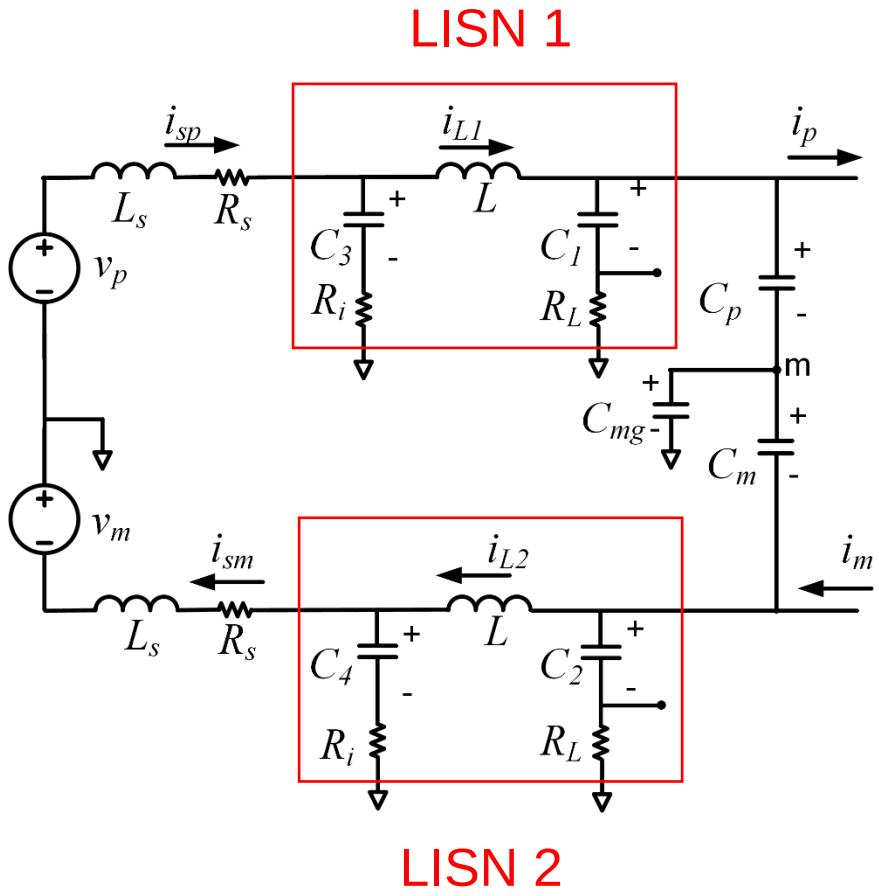
Conducted Emissions (CE)





Line Impedance Stabilization Network

State Space Model of DC Input and LISNs

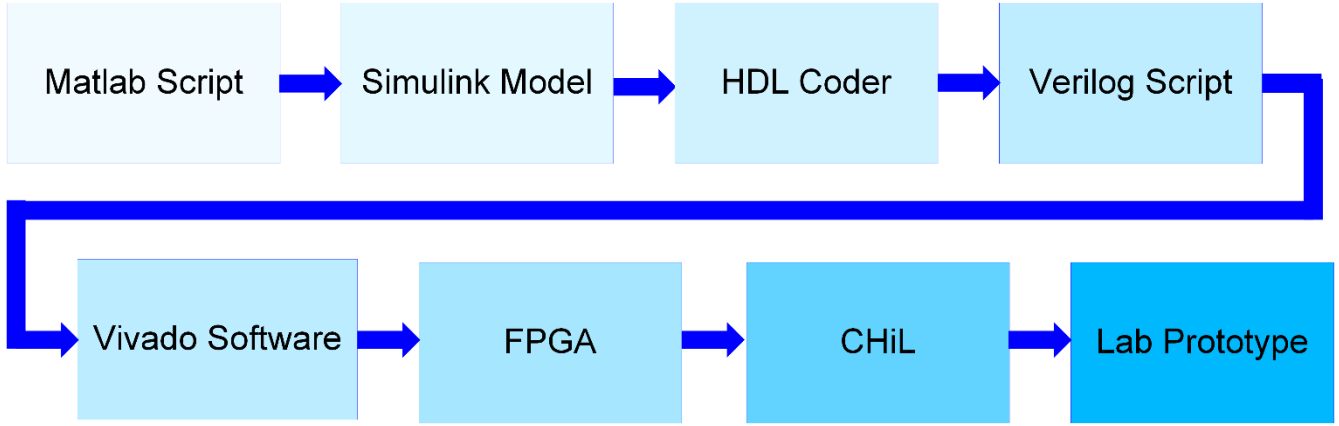


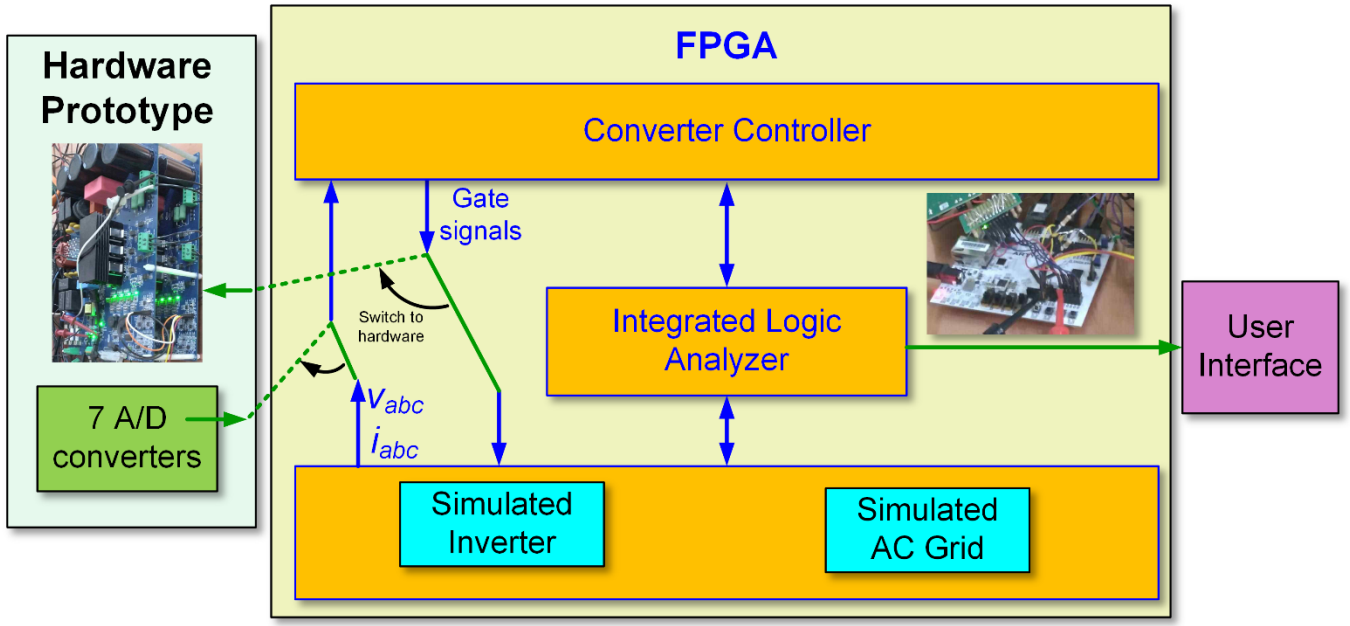
$$\mathbf{P}_{\mathbf{DC}} \begin{bmatrix} v_p \\ v_m \\ i_p \\ i_m \end{bmatrix} = s\mathbf{N}_{\mathbf{DC}} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{c1} \\ v_{c2} \\ v_{cp} \\ v_{cm} \\ v_{mg} \\ i_{sp} \\ i_{sm} \\ v_{c3} \\ v_{c4} \end{bmatrix} + \mathbf{M}_{\mathbf{DC}} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{c1} \\ v_{c2} \\ v_{cp} \\ v_{cm} \\ v_{mg} \\ i_{sp} \\ i_{sm} \\ v_{c3} \\ v_{c4} \end{bmatrix}$$

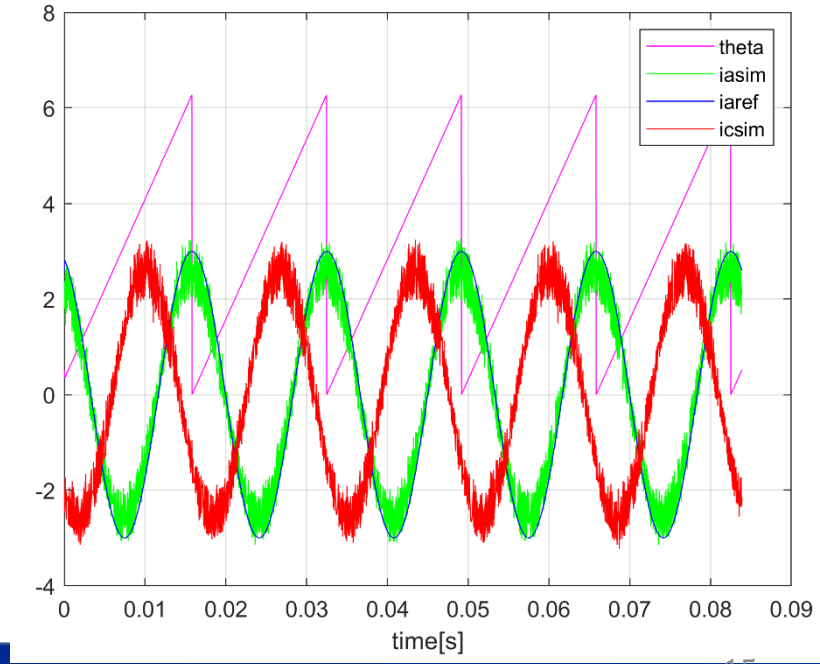
CM Voltage Elimination Strategies

- Pulsed Density Modulation (PDM)
  - PDM allows simultaneous switching transitions in all 4 inverter legs to output zero CM voltage
- Prototyping for Experimental Validation
- Grid-Forming Inverter for AC power distribution
  - Must meet power quality requirements in MIL-STD-1399
- Grid-Following Converter to interface Distributed Energy Resources
- Application to Motor Drives

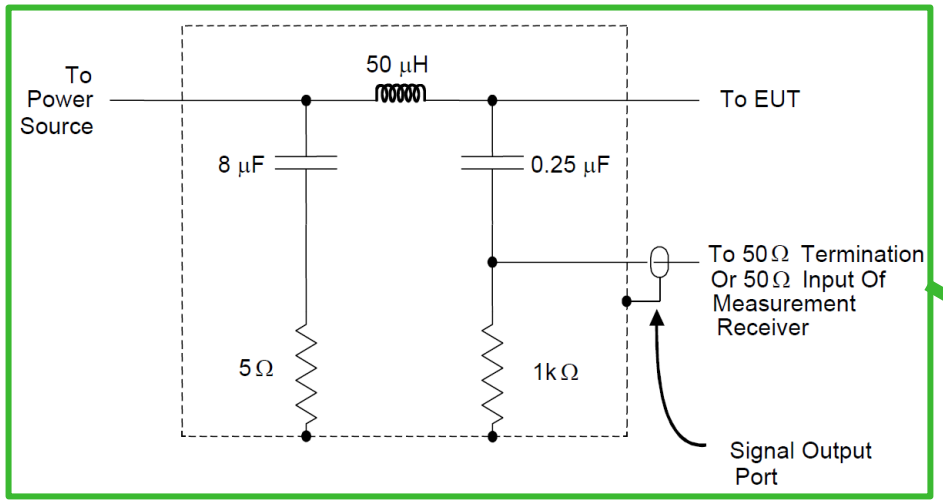
Low-Cost Rapid Prototyping





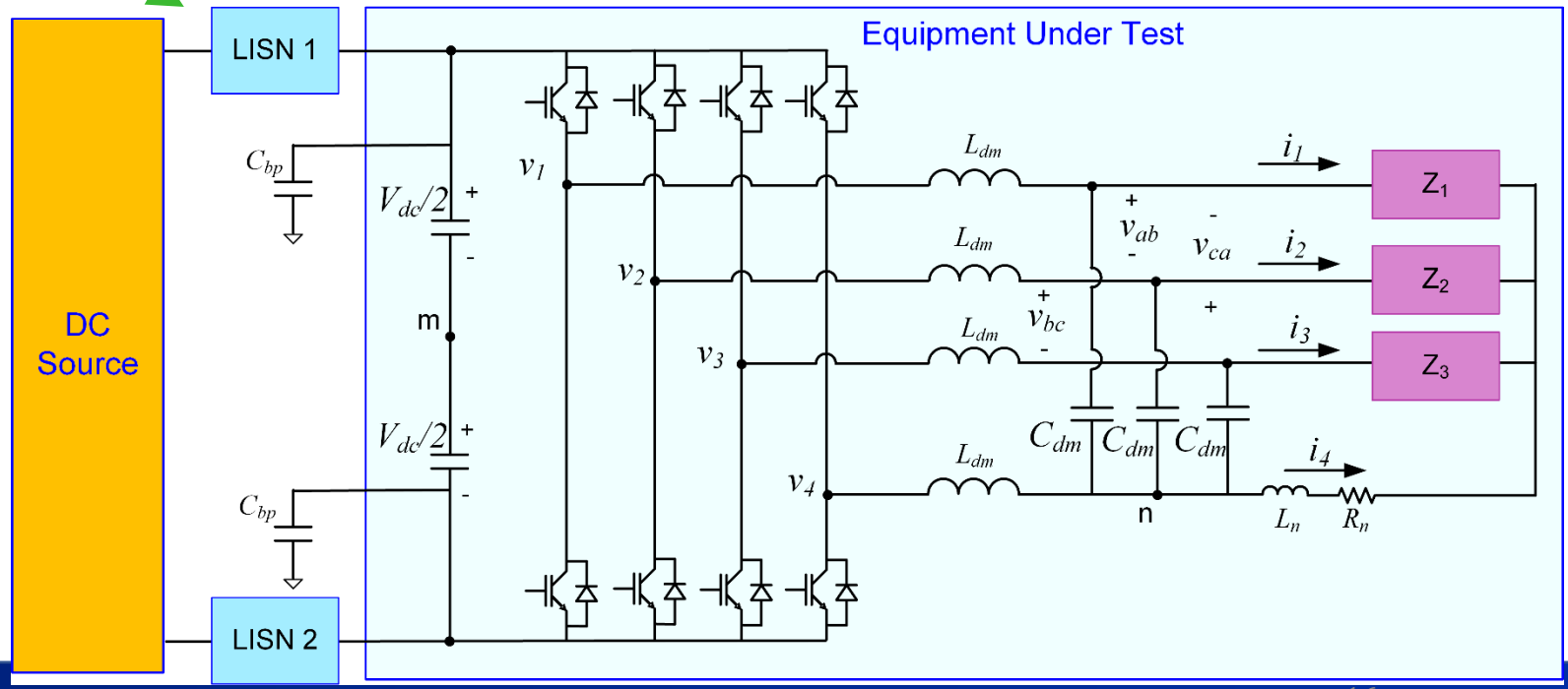


Grid-Forming System Architecture



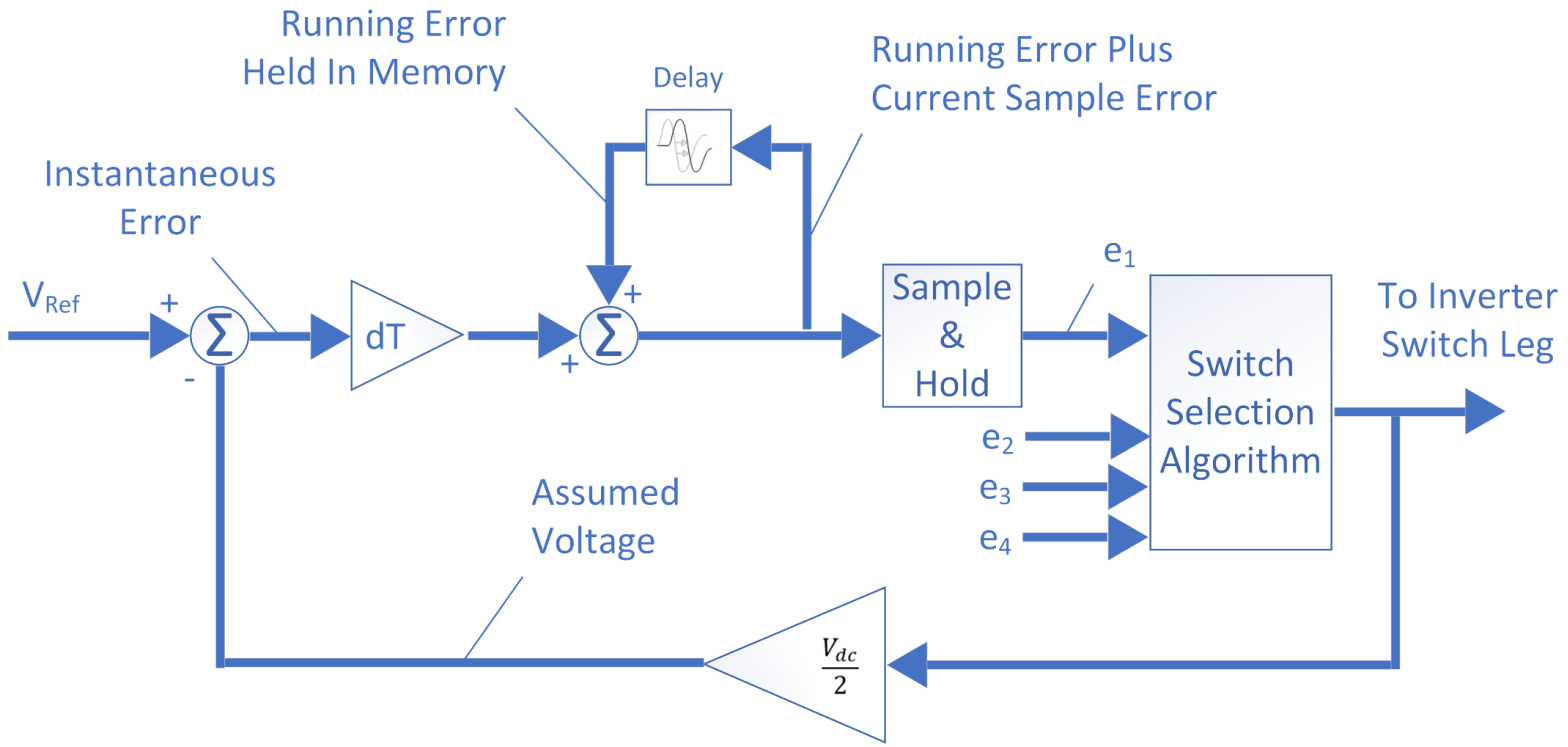
Line Impedance Stabilization Network from MIL-STD-461G

The CM voltage is the sum of the four inverter pole voltages, and it is controlled to zero by switching two top devices on and two bottom devices on

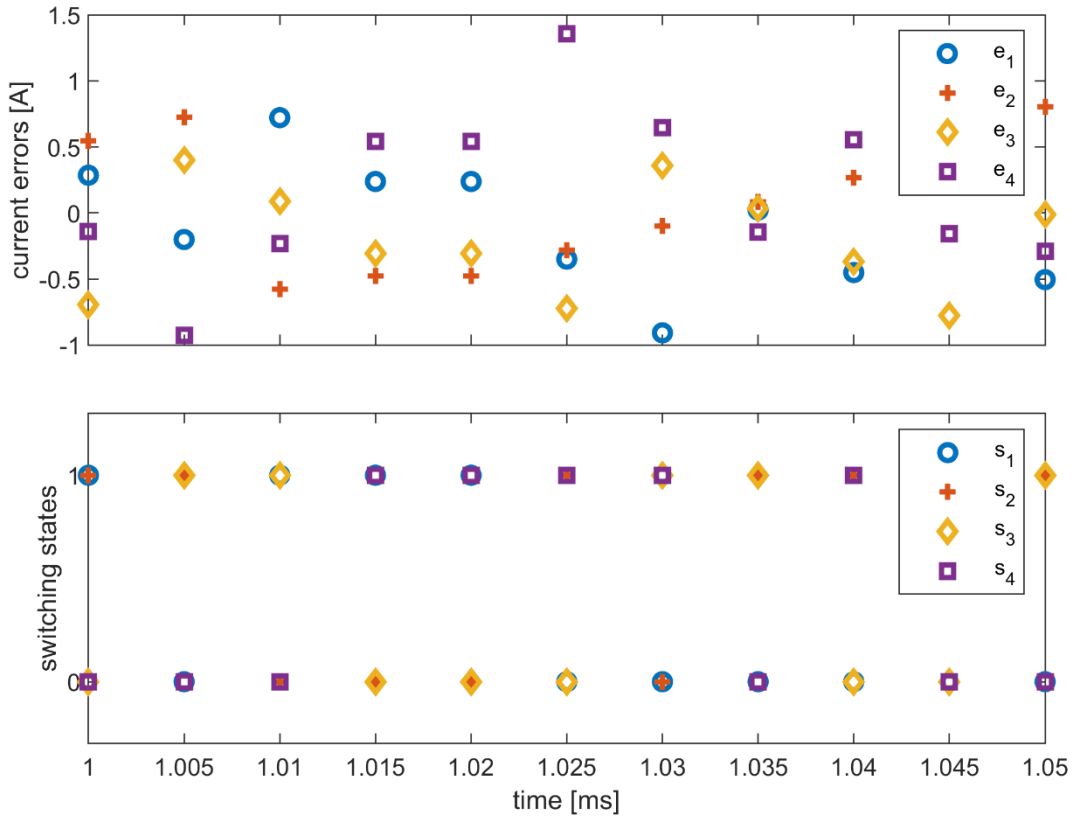


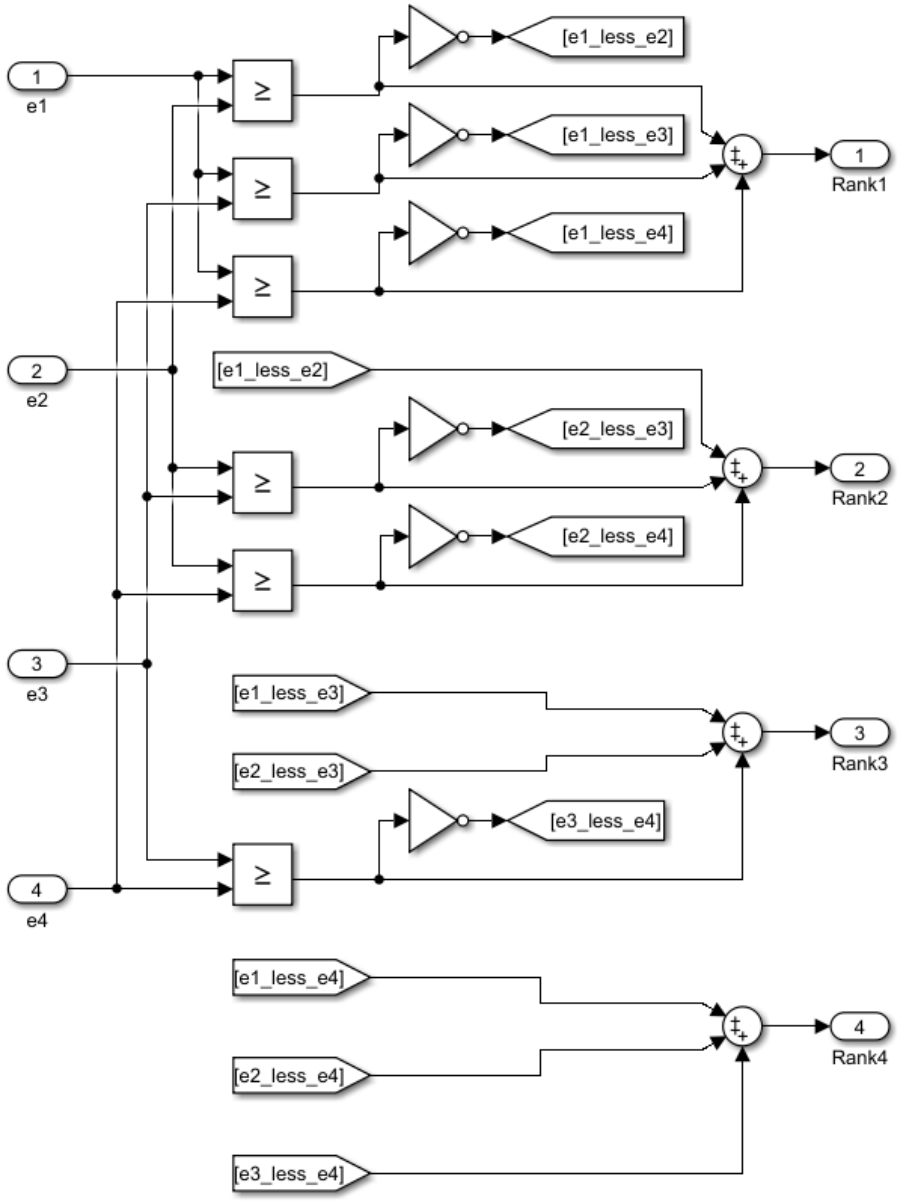
Control System

- The switch selection algorithm sets the two phases with the largest error to +Vdc/2 and the two phases with the smallest error to – Vdc/2.
- If any phase current exceeds the limit, then the switch selection modifies the next switch state to reduce the overcurrent



Ranking Algorithm



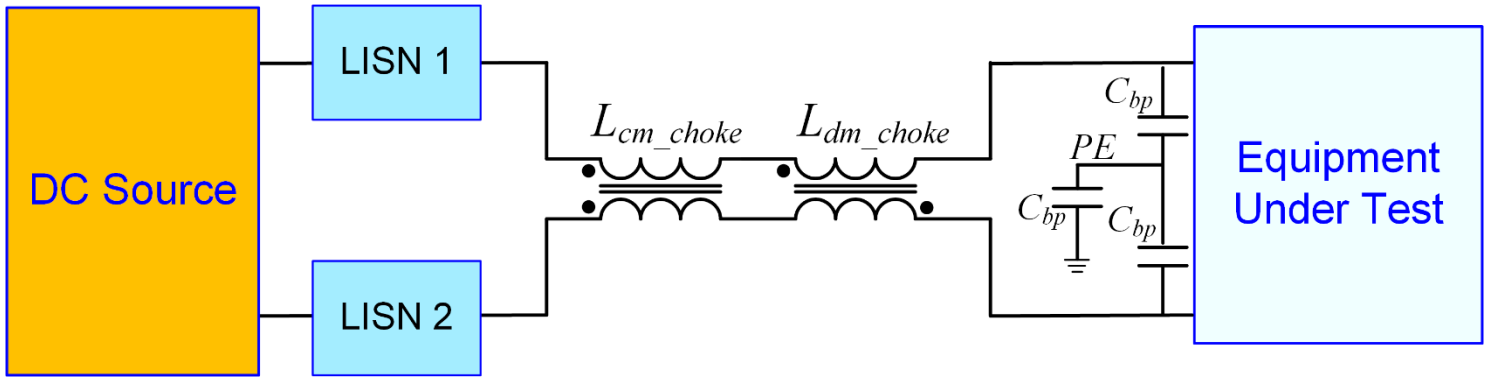


Experimental Setup

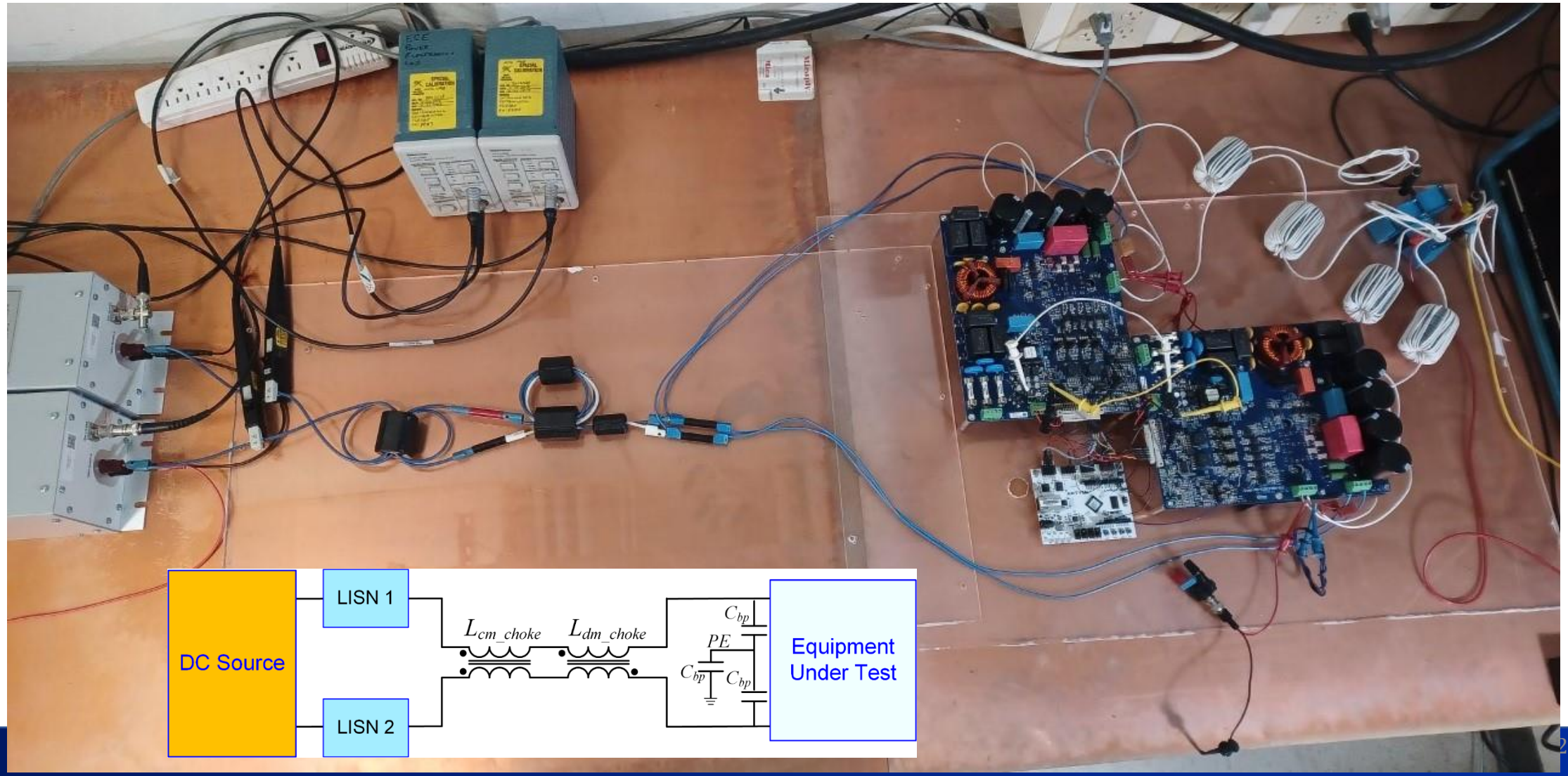
- Power Converters built with 1200 V SiC Infineon MOSFETs
- AC 200 Vrms line-to-line, 10 A rating
- The DC source is a three-phase diode rectifier fed by the AC laboratory grid
- Small bypass capacitors and clip-on chokes were added to meet the limits

CIRCUIT PARAMETERS

V_{dc}	340V
modulation index	0.95
L_{dm}	$750\mu H$
C_{dm}	$20\mu F$
L_n	$10\mu H$
R_n	$100m\Omega$
Z_1, Z_2, Z_3	29 Ω
Z_3 (unbalanced)	38.7 Ω
C_{bp}	$200nF$

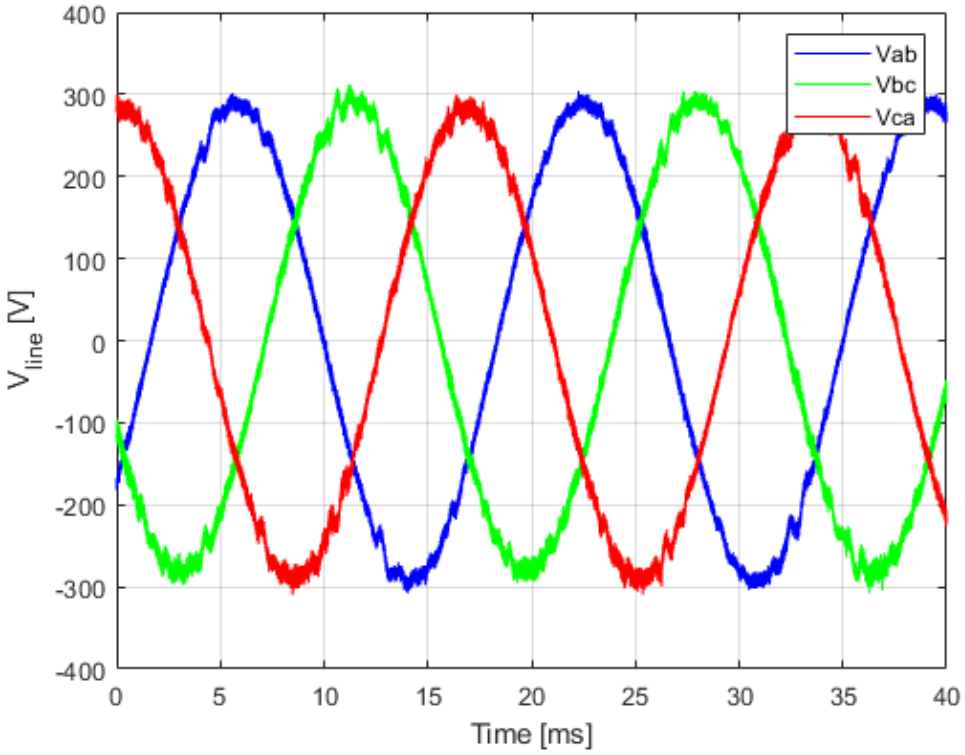


Laboratory Setup

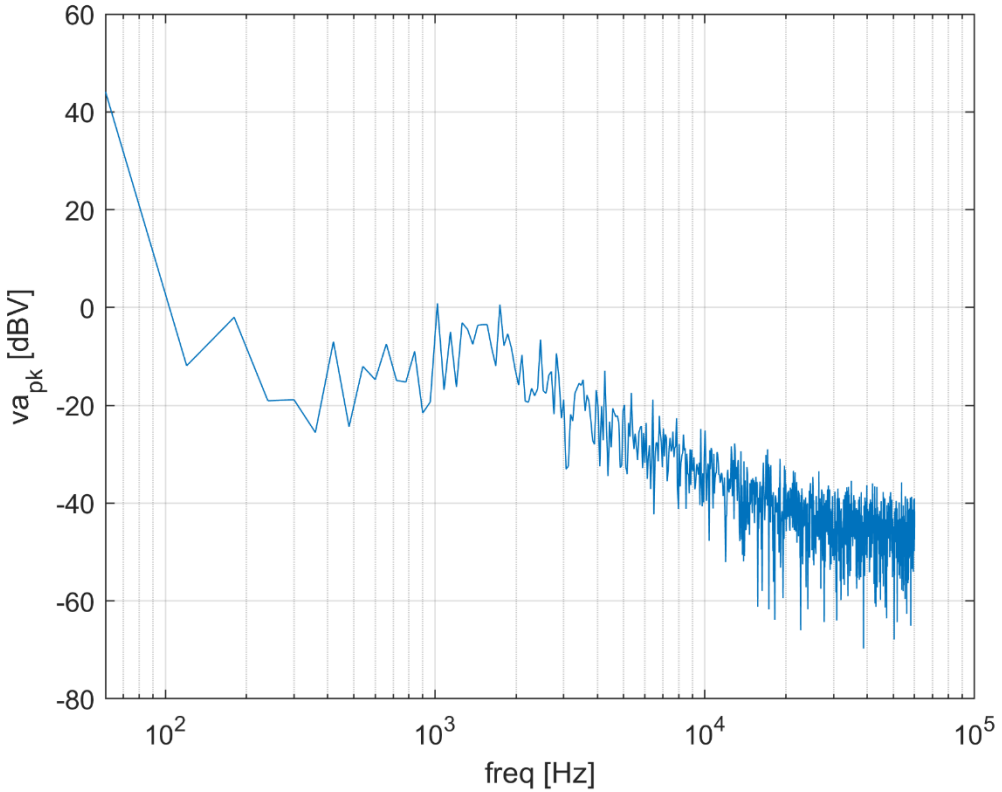


Experimental Measurements

- The measured THD was 2% with either balanced or unbalanced load, meeting the 3% limit specified in MIL-STD-1399

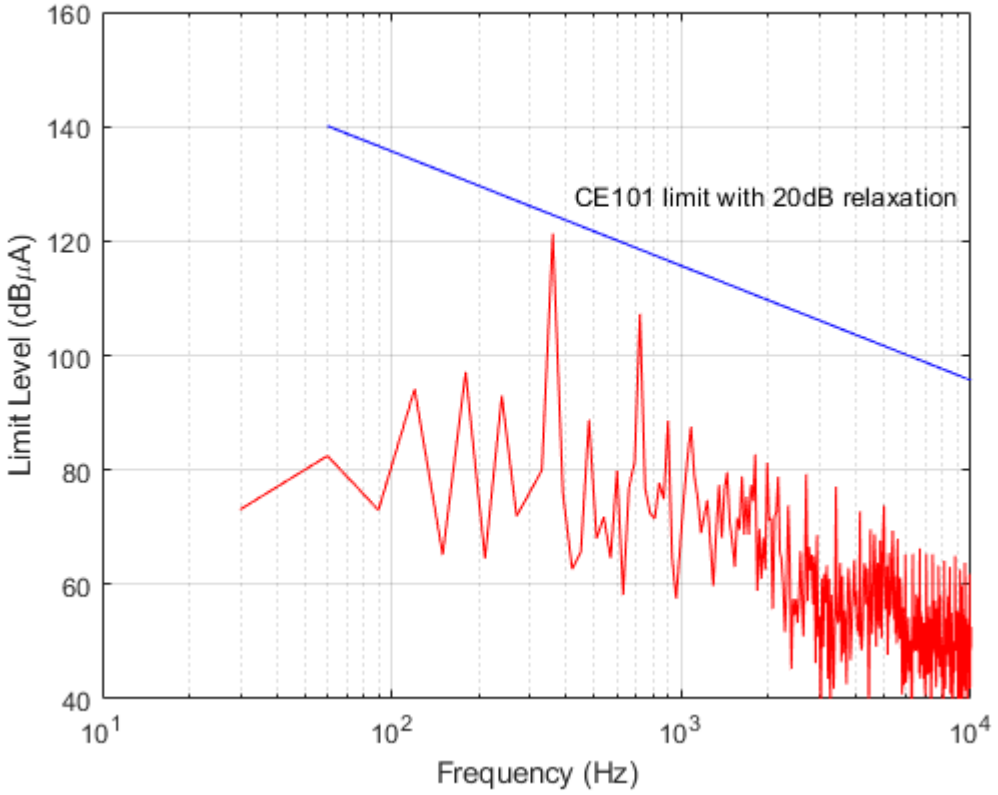


Load line voltages

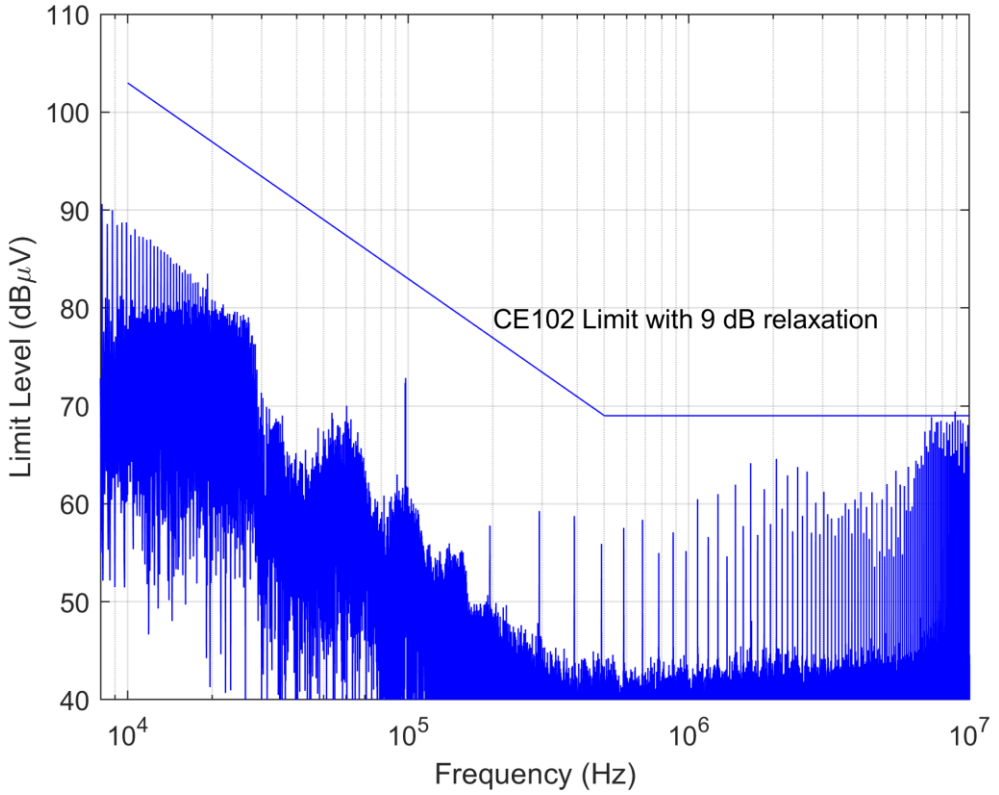


Phase a voltage spectrum

Conducted EMI Measurements

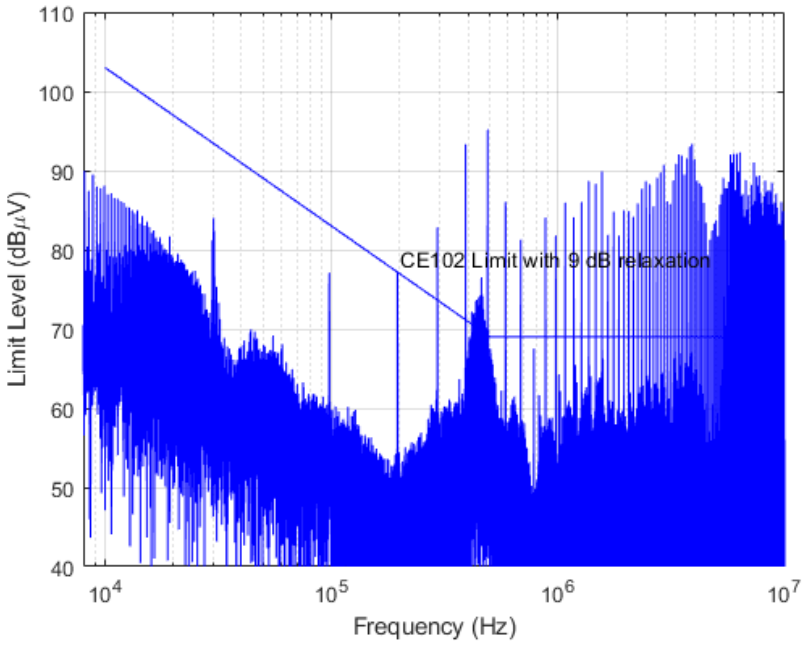


LISN current spectrum versus CE101 limit

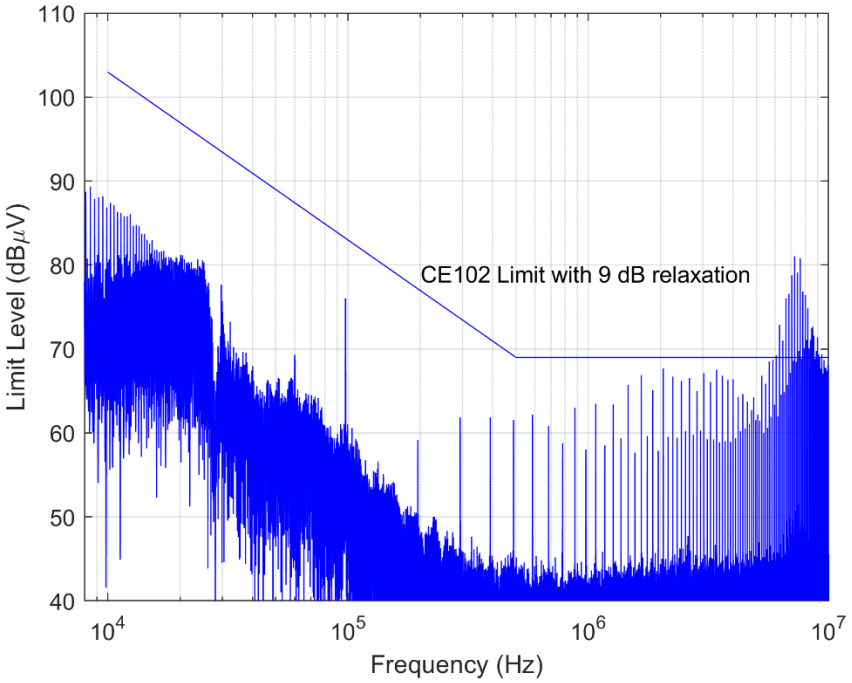


LISN voltage spectrum versus CE102 limit

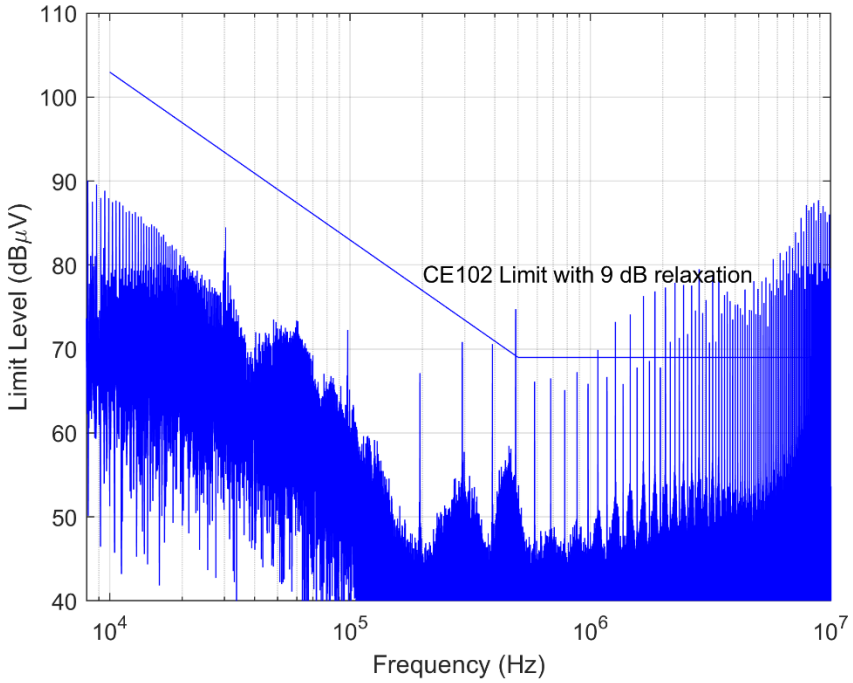
Intermediate CE102 Measurements



With bypass capacitors and no chokes

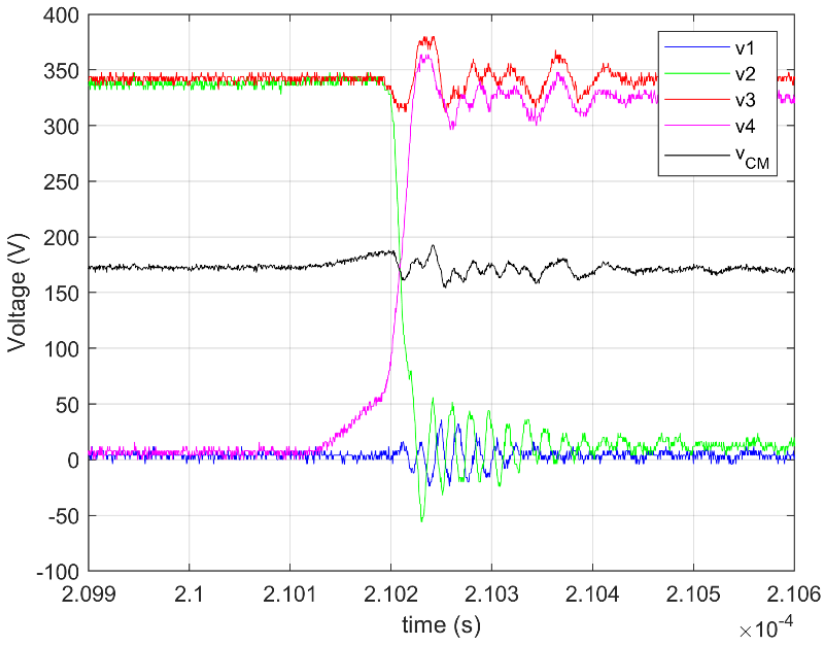


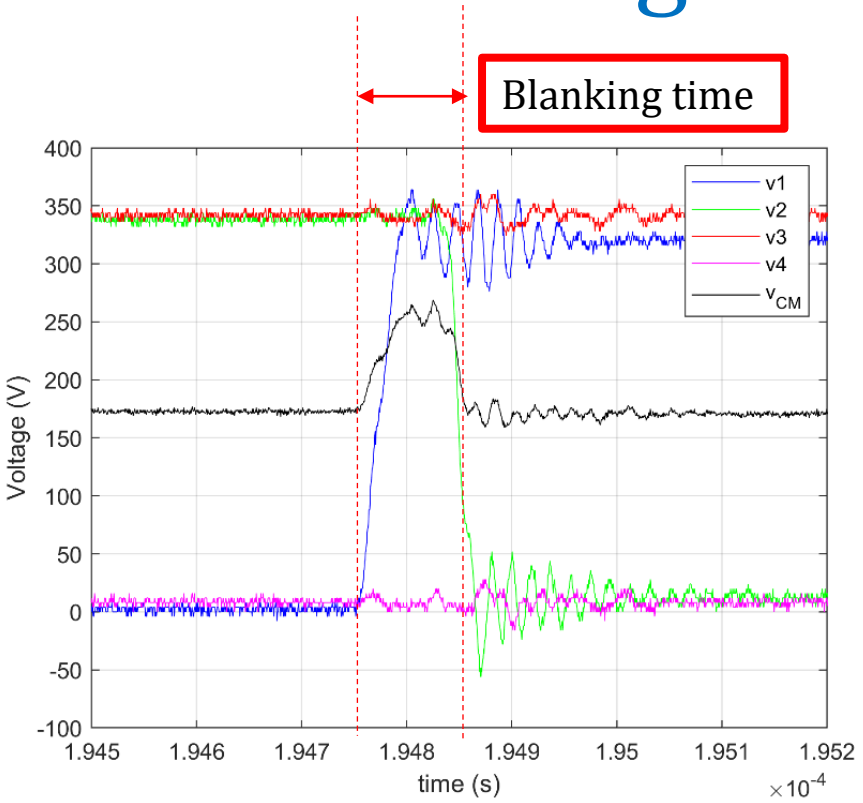
With CM chokes and no DM choke

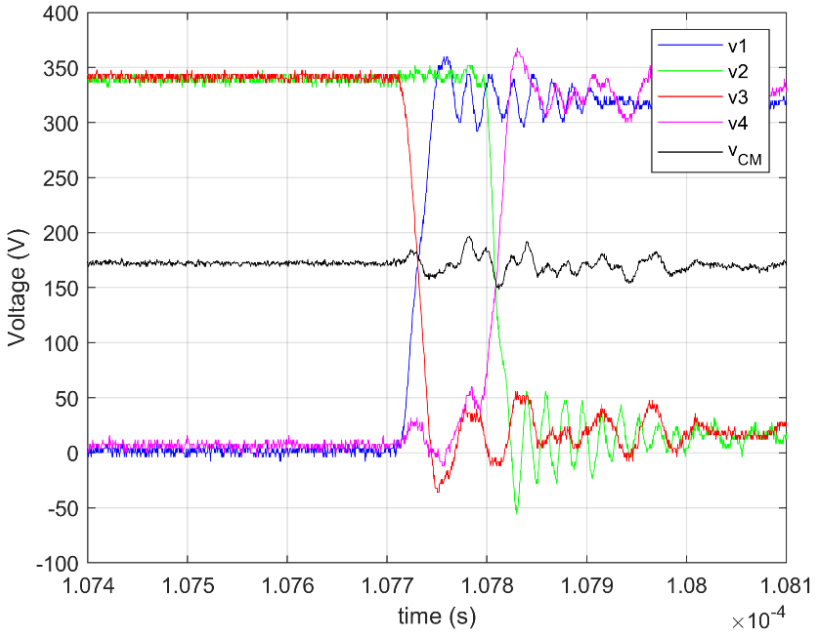


With DM choke and no CM chokes

Switching Events and CM Voltage







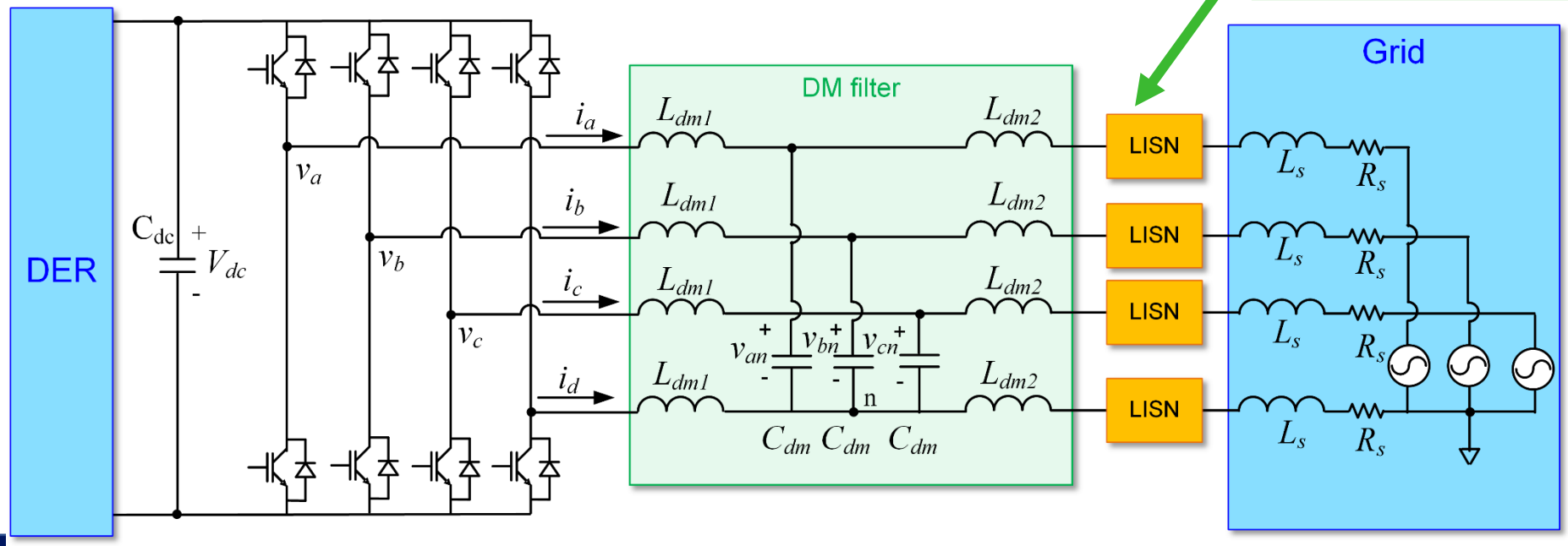
Simultaneous Transition with current in 2 diodes or 2 transistors.

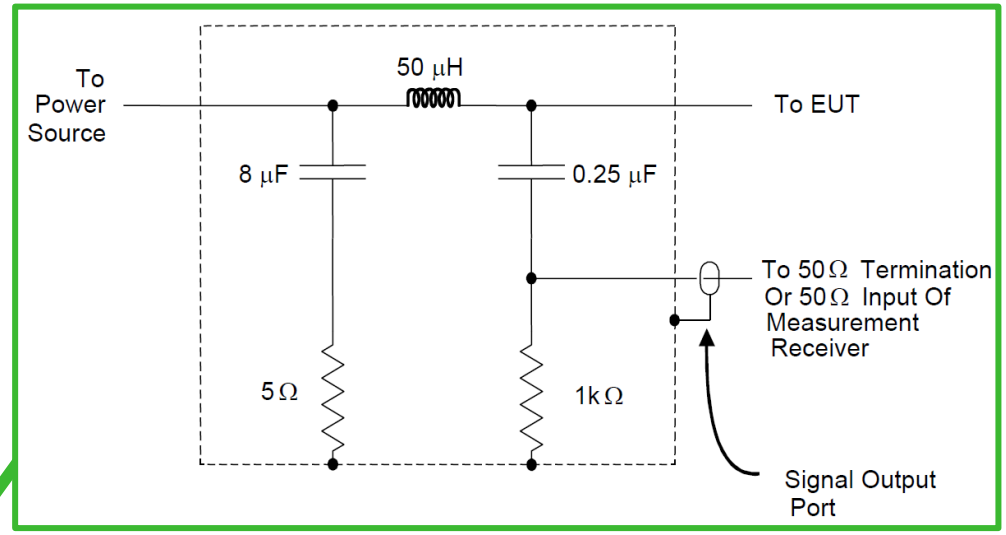
Delayed Transition due to blanking time with current in 1 transistor and 1 diode.

Simultaneous Transitions with current in 2 diodes and 2 transistors.

Grid-Following Architecture

- Delta Modulation or Model Predictive Control (MPC) demonstrated with similar performance
- Novel switch selection algorithm does not require the arctangent function for MPC

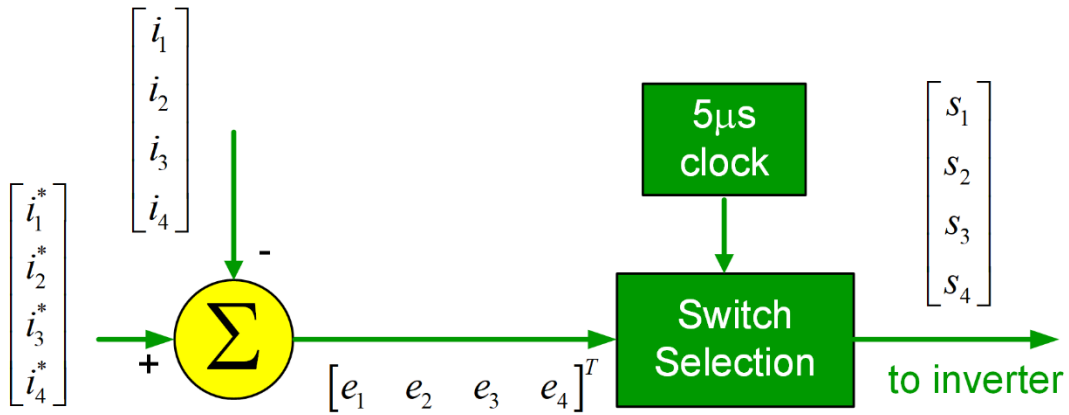


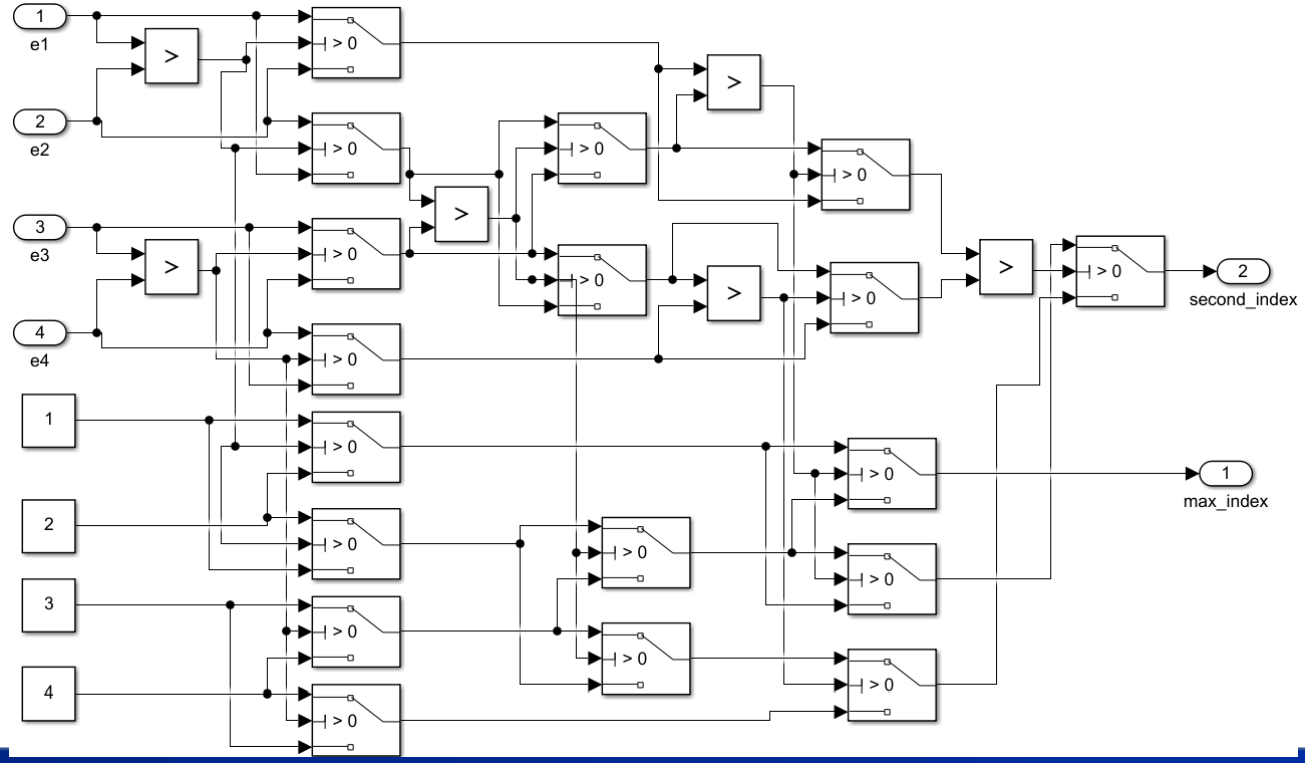


Line Impedance Stabilization Network from MIL-STD-461G

Control System – Delta Modulation

- Alternative to Sigma-Delta modulation used in grid-forming inverters
- The switch selection algorithm sorts the current errors [e1…e4] from largest to smallest so that the two phases with the largest errors are switched high (top device on), while the other two are switched low (bottom device on)



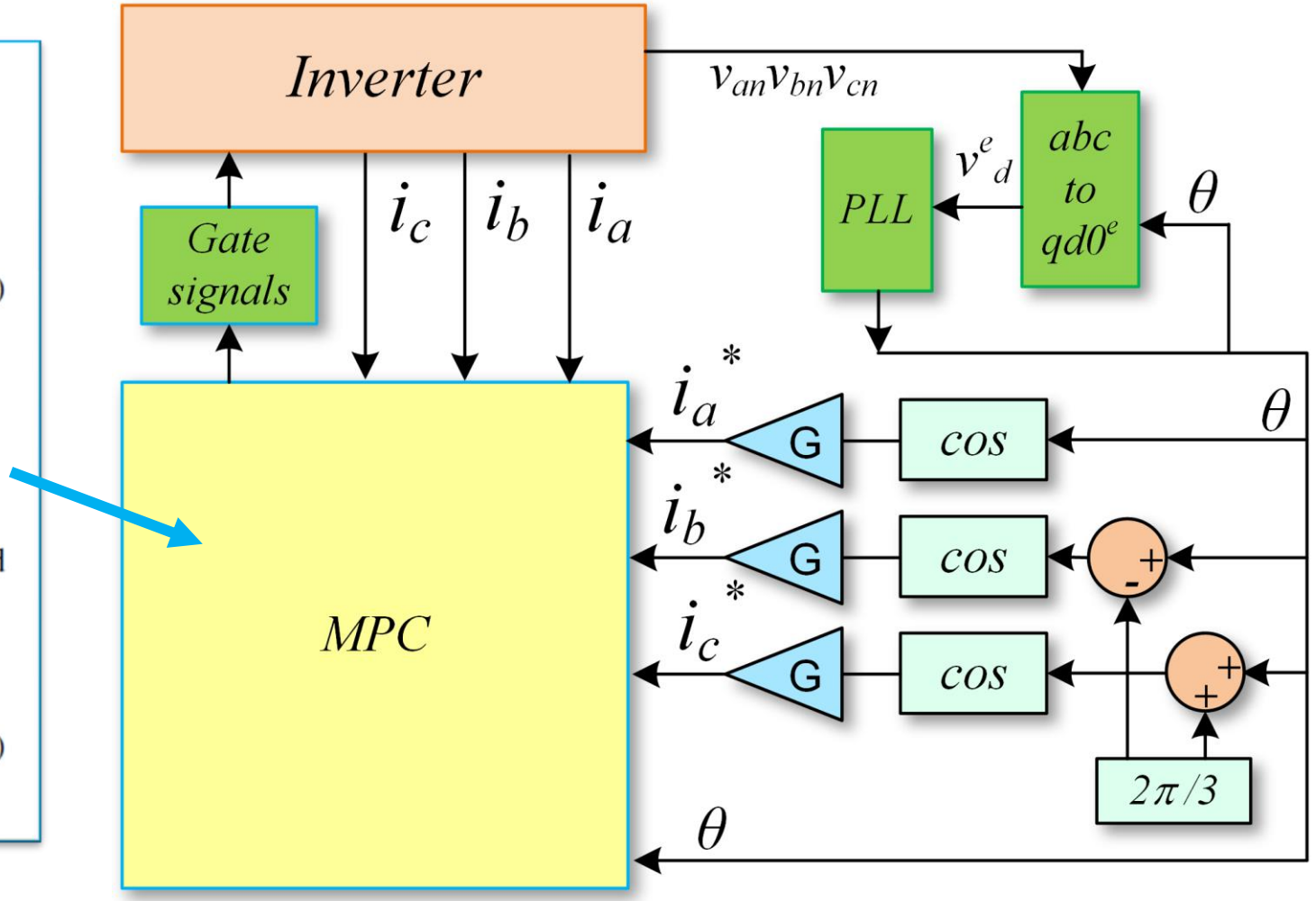


Control System – Model Predictive Control

$$\begin{bmatrix} V_a^*(k) \\ V_b^*(k) \\ V_c^*(k) \end{bmatrix} = \begin{bmatrix} \frac{L_{dm}}{T_s} & 0 & 0 \\ 0 & \frac{L_{dm}}{T_s} & 0 \\ 0 & 0 & \frac{L_{dm}}{T_s} \end{bmatrix} \begin{bmatrix} i_a^*(k+1) - i_a(k) \\ i_b^*(k+1) - i_b(k) \\ i_c^*(k+1) - i_c(k) \end{bmatrix} + \begin{bmatrix} R_{dm} & 0 & 0 \\ 0 & R_{dm} & 0 \\ 0 & 0 & R_{dm} \end{bmatrix} \begin{bmatrix} i_a(k) \\ i_b(k) \\ i_c(k) \end{bmatrix} \quad (1)$$

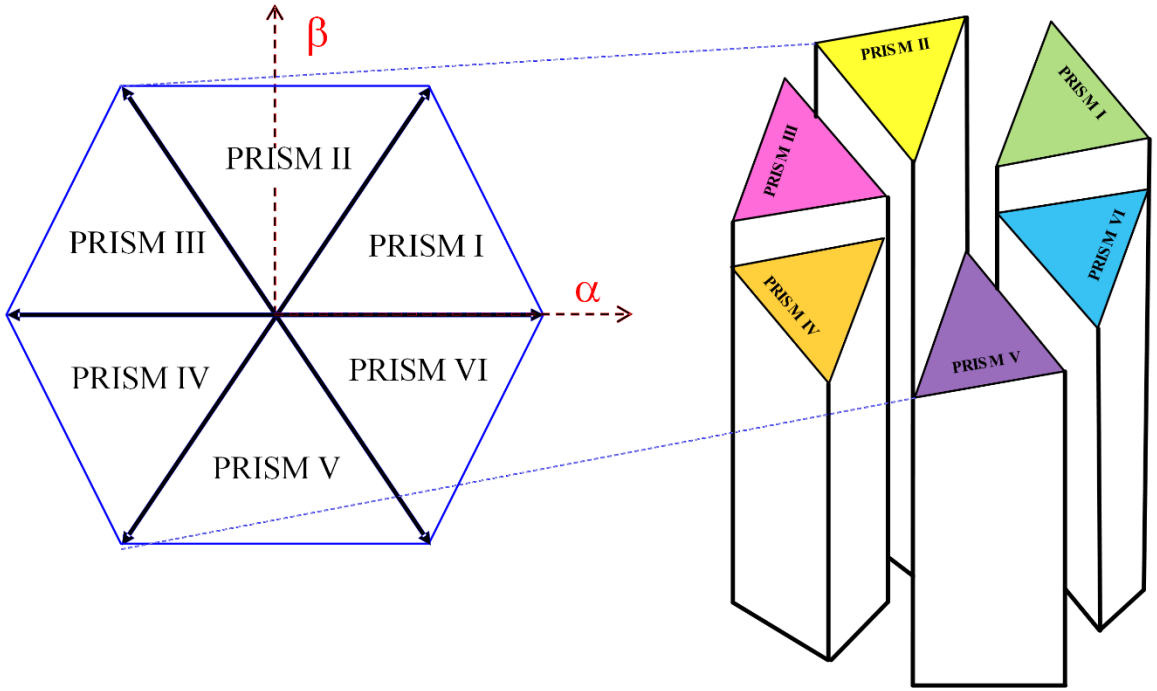
The reference voltages computed with (1) are transformed from the $a-b-c$ to the α-β-γ frame using (2).

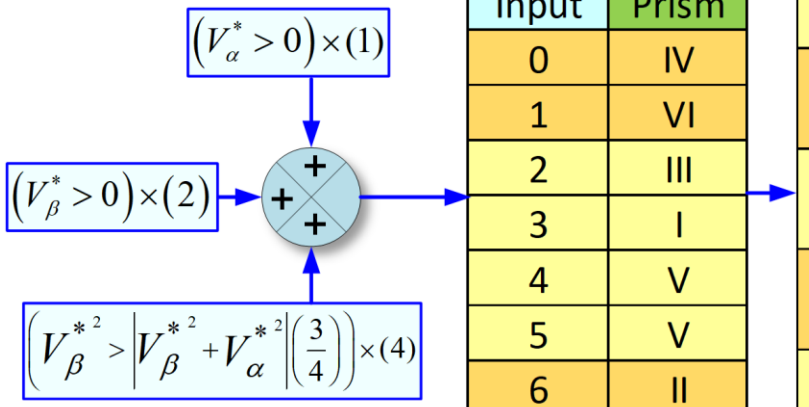
$$\begin{bmatrix} V_\alpha^*(k) \\ V_\beta^*(k) \\ V_\gamma^*(k) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a^*(k) \\ V_b^*(k) \\ V_c^*(k) \end{bmatrix} \quad (2)$$



Model Predictive Control – Switch Selection

- The appropriate prism is chosen by the angle of the α and β components
- This novel switch selection algorithm only requires lookup tables and is executed by the FPGA in a single clock cycle



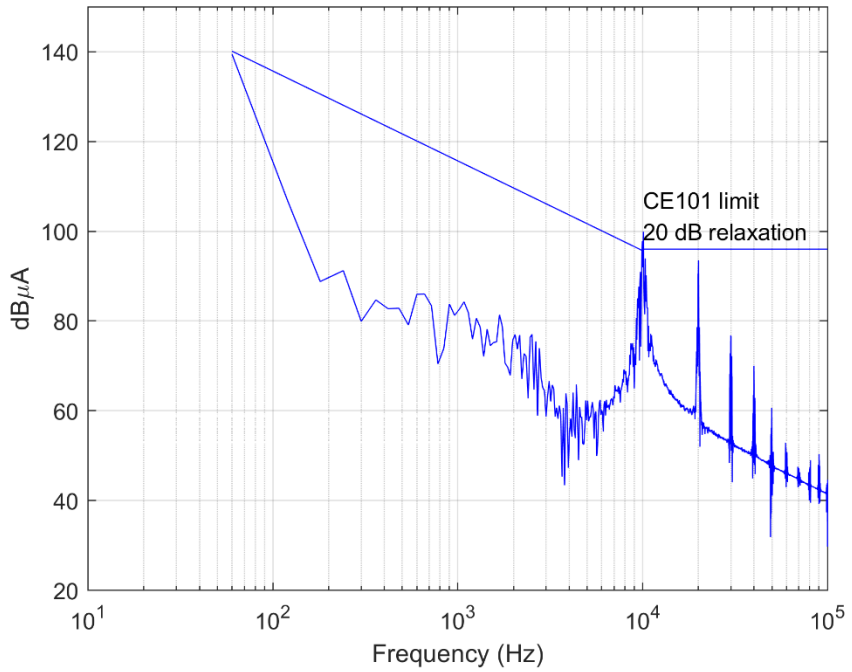


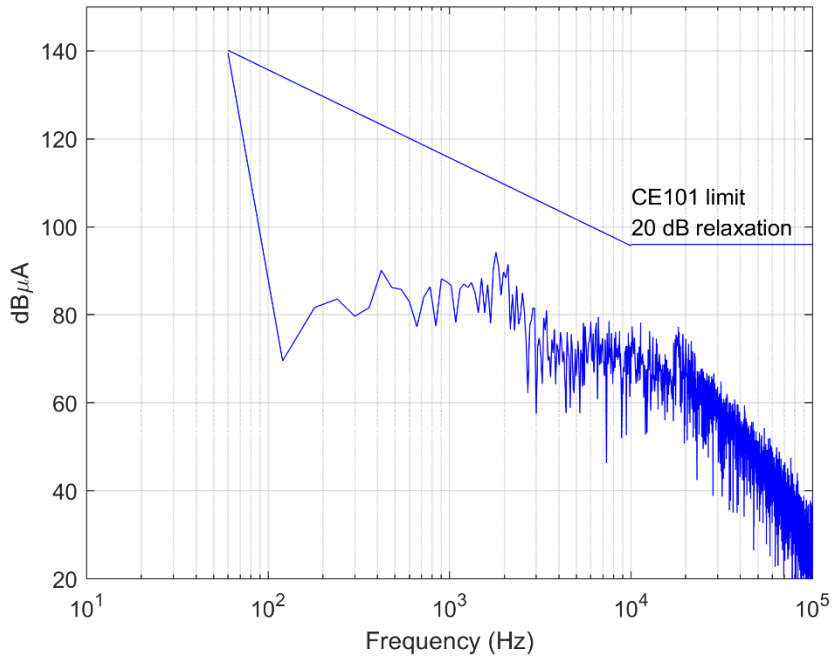
Prism Lookup	
Input	Prism
0	IV
1	VI
2	III
3	I
4	V
5	V
6	II
7	II

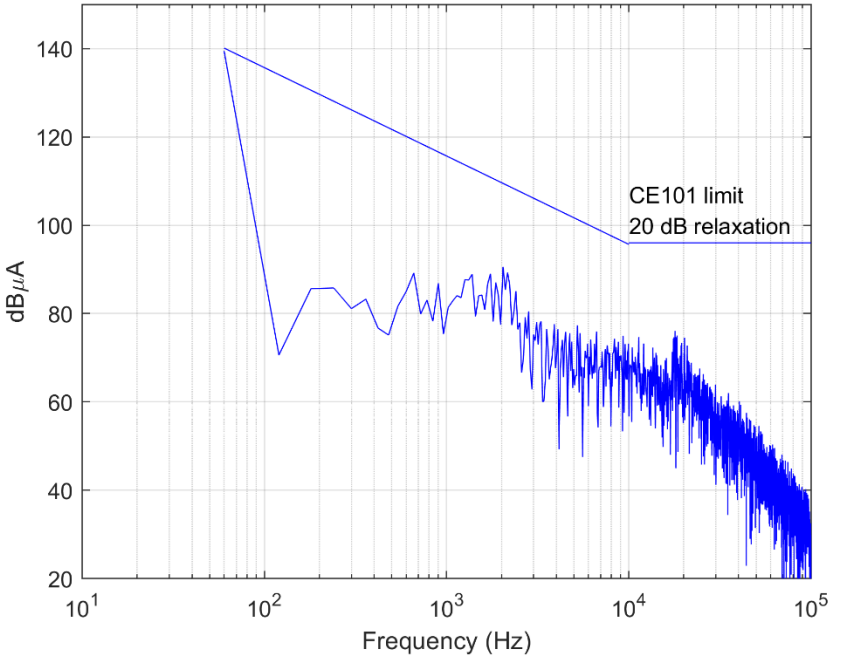
Switch Selection Algorithm		
Prism	$V_a^* V_b^* V_c^*$	Switches
I	+--/---	1001
	++-/+++	1100
II	++-/+++	1100
	-+-/---	0101
III	-+-/---	0101
	--+/+++	0110
IV	--+/+++	0110
	--+/---	0011
V	--+/---	0011
	+-+/+++	1010
VI	+-+/+++	1010
	+--/---	1001

Simulations MIL-STD-461G CE101

- Grid-following application
- 20dB relaxation for converters rated 10 A_{rms}







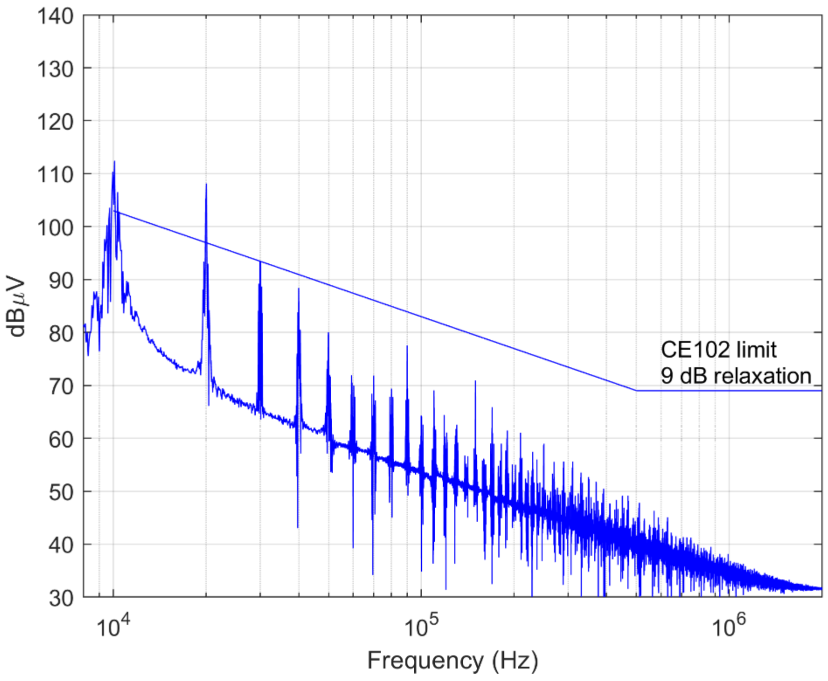
3D SVM with a 2 mH CM choke

ΔM and no CM choke

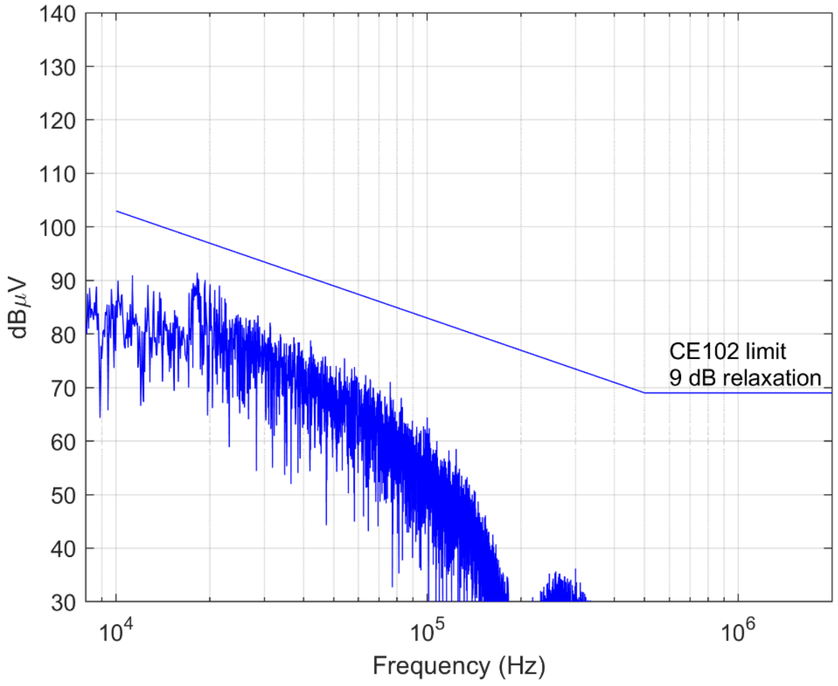
MPC and no CM choke

Simulations MIL-STD-461G CE102

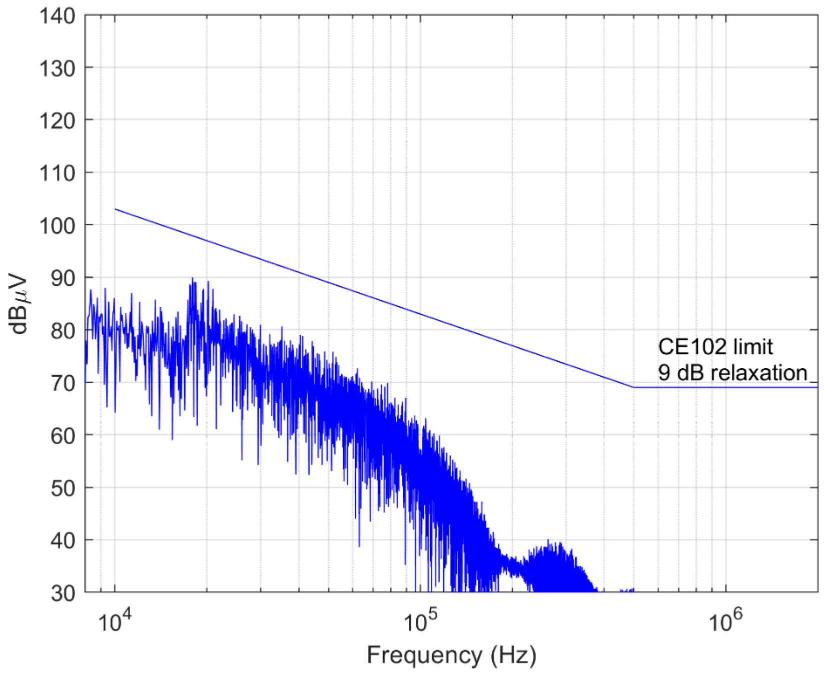
- Grid-following inverter
- 9dB relaxation for nominal EUT source voltage 220 Vrms



3D SVM with a 2 mH CM choke



ΔM and no CM choke



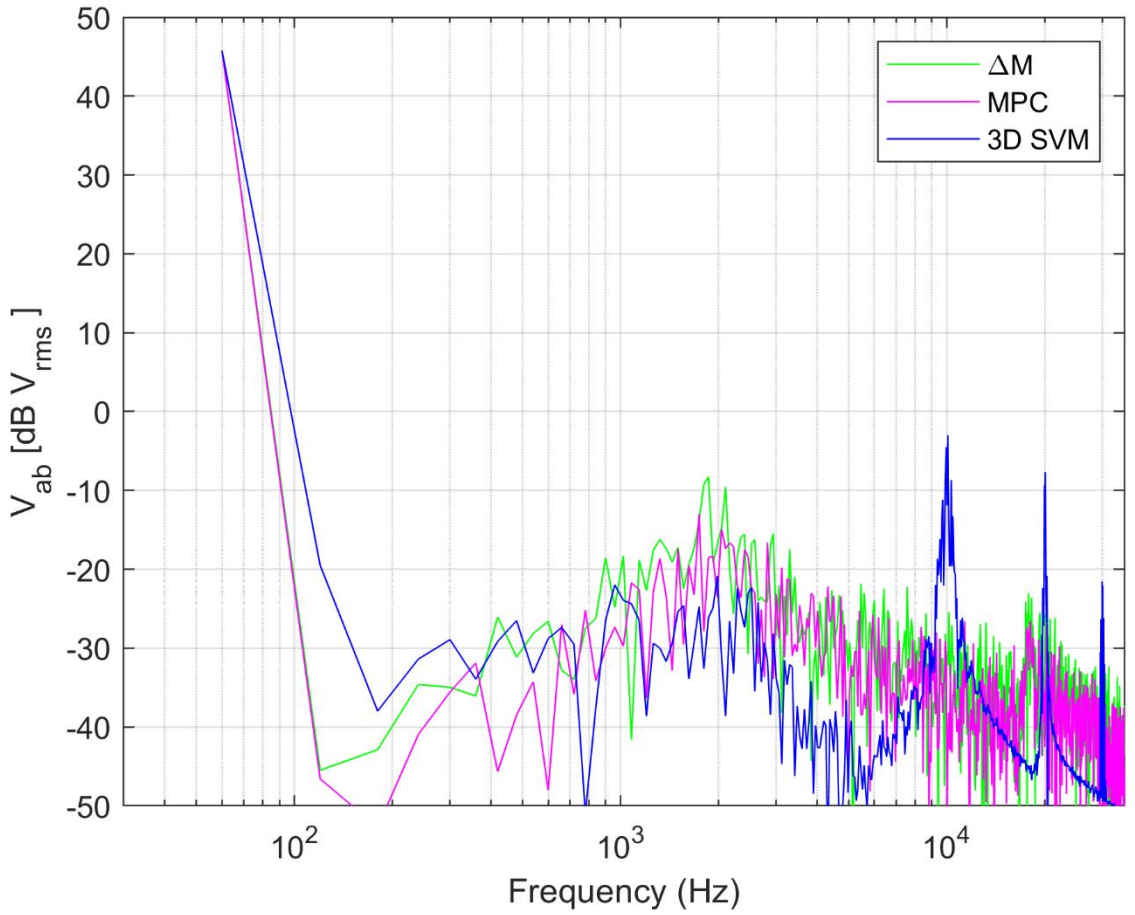
MPC and no CM choke

Simulations of Differential Mode Performance

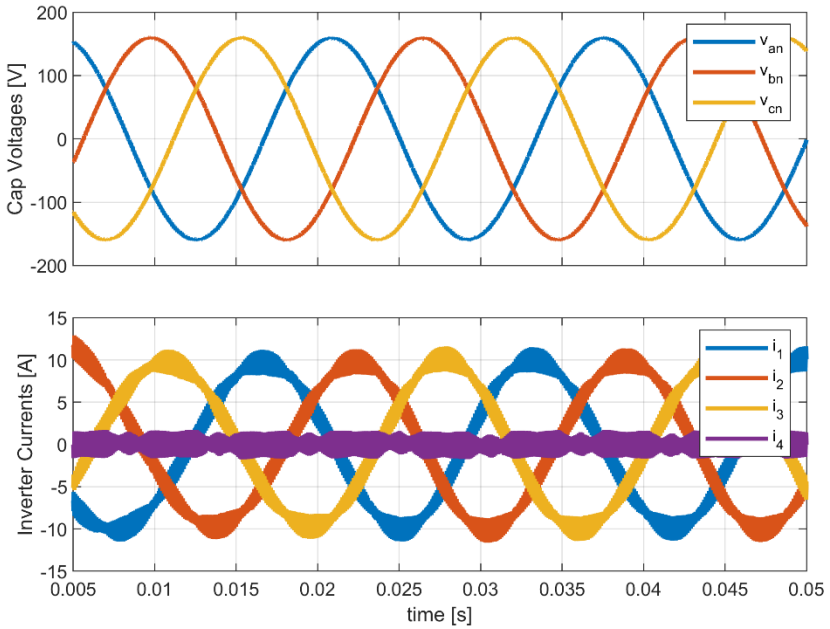
- The simulated DM performance is comparable for all three methods

Control Method	v_{an} THD	i_1 THD
ΔM	0.58%	0.87%
MPC	0.56%	0.98%
3D SVM	0.2%	2.32%

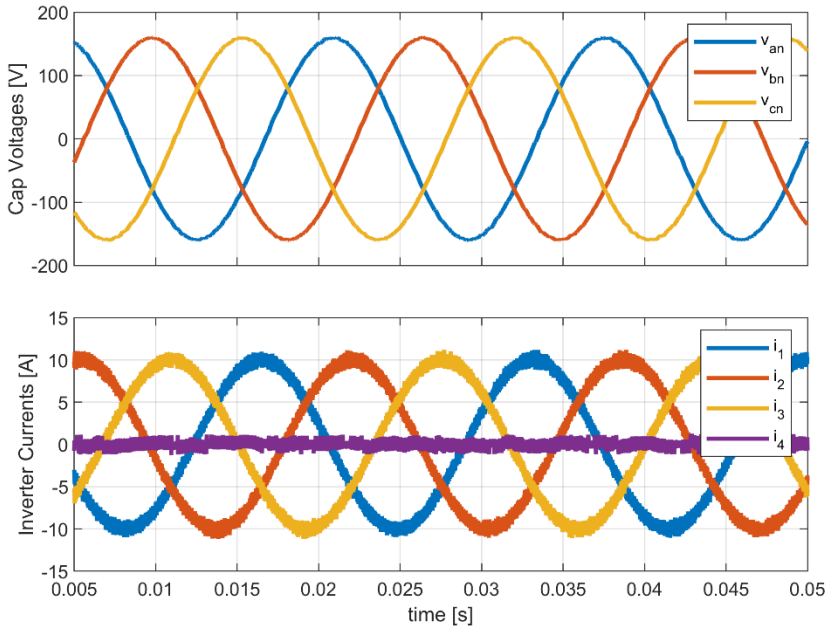
- The line-to-line rms voltages obtained with the three control methods show that 3D SVM has lower harmonics in the 1kHz-10kHz range in the DM voltage compared to the PDM controllers



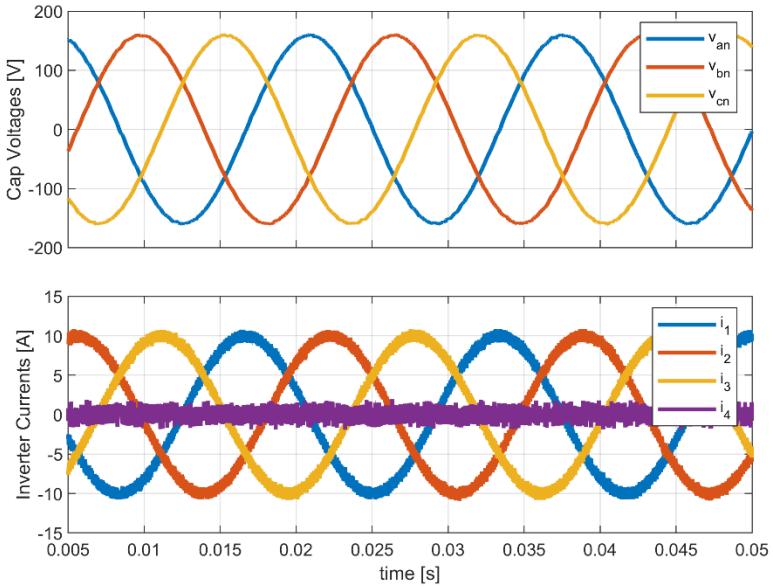
Differential Mode Simulated Waveforms



3D SVM with CM choke



ΔM and no CM choke



MPC and no CM choke

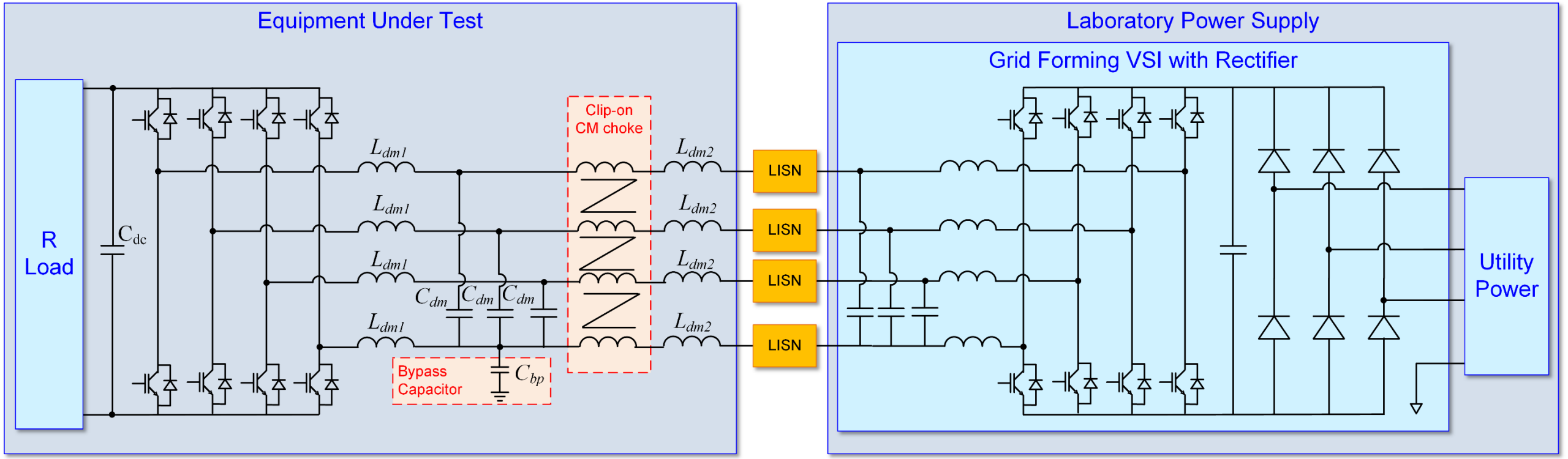
Control Method	v_{an} THD	i_1 THD
ΔM	0.58%	0.87%
MPC	0.56%	0.98%
3D SVM	0.2%	2.32%

Experimental Setup

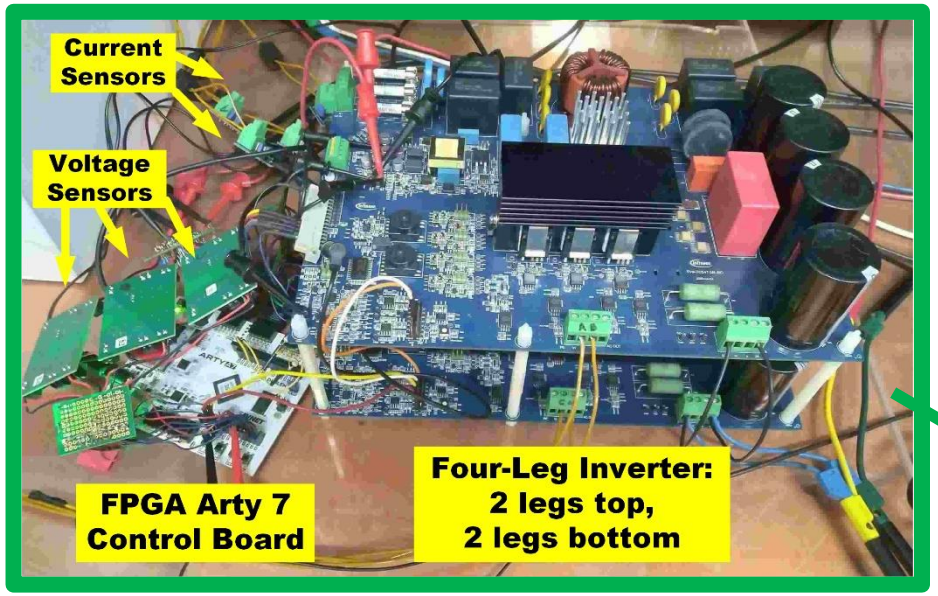
- Power Converters built with 1200V 36A SiC Infineon MOSFETs
- AC 200Vrms line-to-line, 10A rating

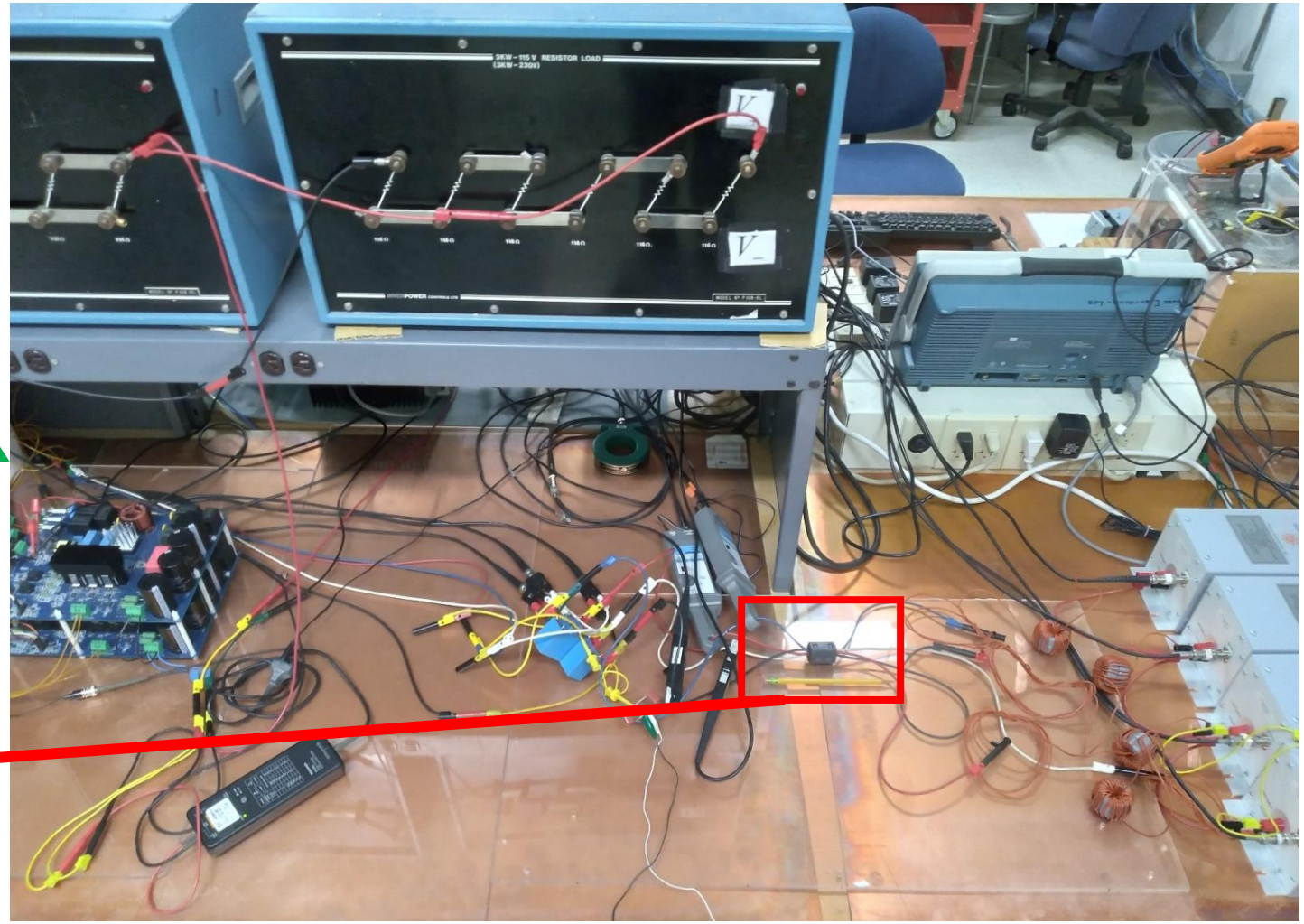
PARAMETERS FOR THE EXPERIMENTAL MEASUREMENTS

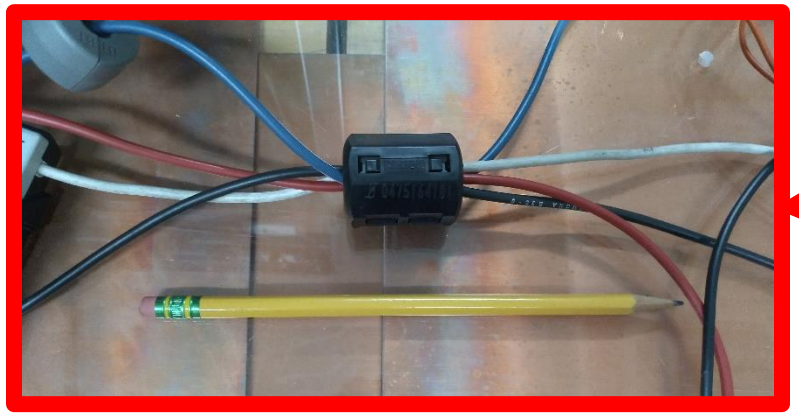
Symbol	Description	Value
C_{dc}	DC bus capacitance	$1.2mF$
V_{dc}	DC bus voltage	380 V
L_{dm1}	DM inductance 1	$500\mu H$
L_{dm2}	DM inductance 2	$400\mu H$
C_{dm}	DM capacitance	$20\mu F$
R_{dcload}	DC load resistance	170Ω
C_{bp}	Bypass capacitance	$240nF$



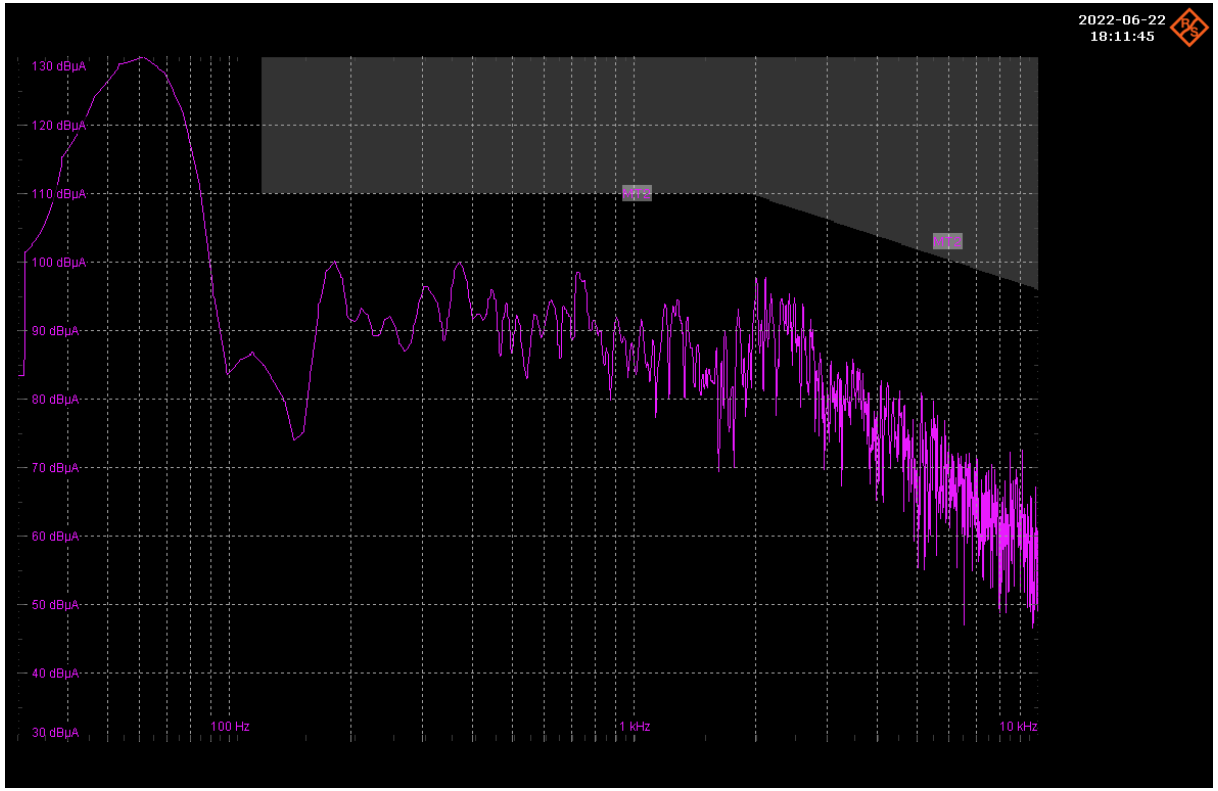
Laboratory Set-Up



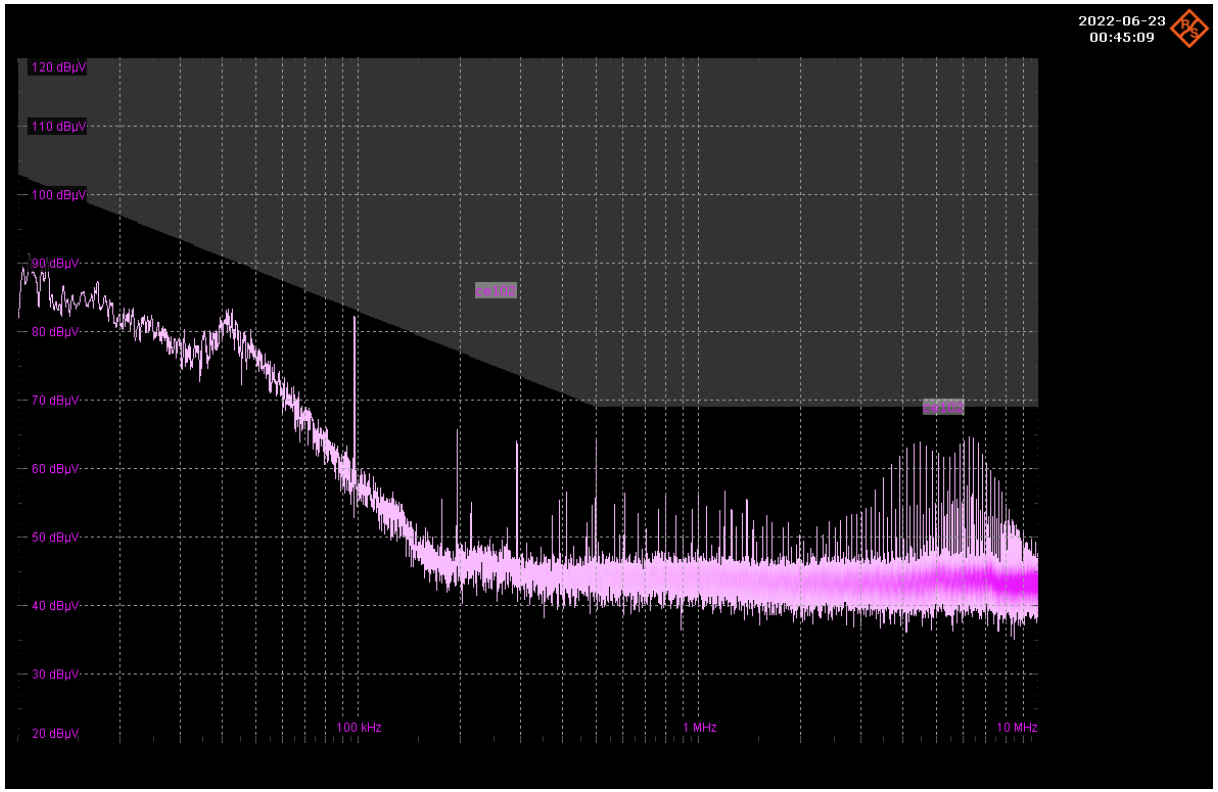




Conducted EMI Measurements



LISN current spectrum versus CE101 limit.



LISN voltage spectrum versus CE102 limit.

GaN Inverter at Baylor Laboratory

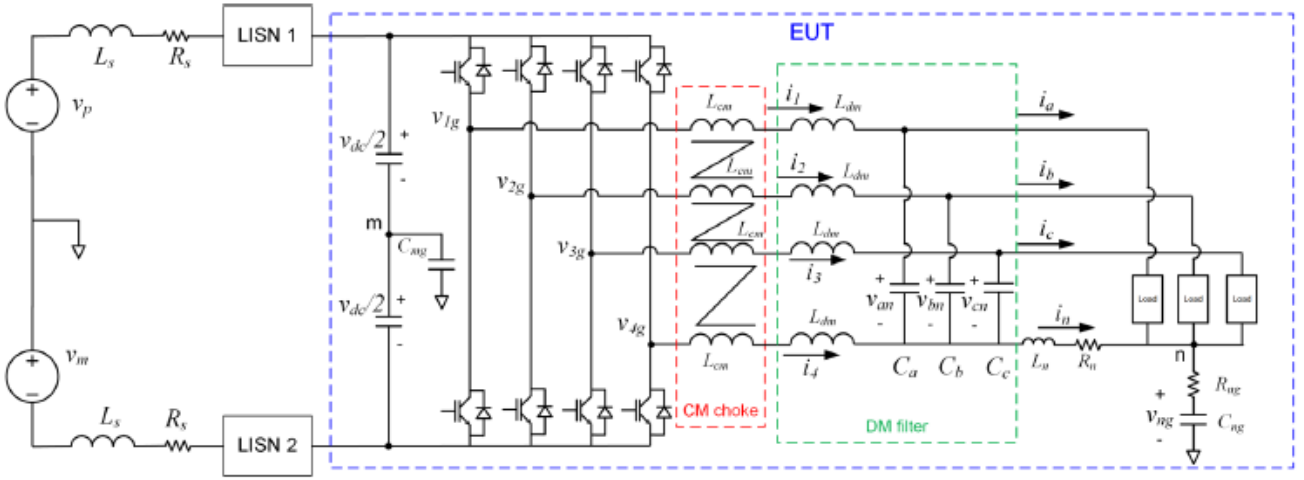
Four-leg inverter realizes balanced three-phase output voltages to prevent CMV (now sum of four legs, where fourth leg connects to load/motor neutral)

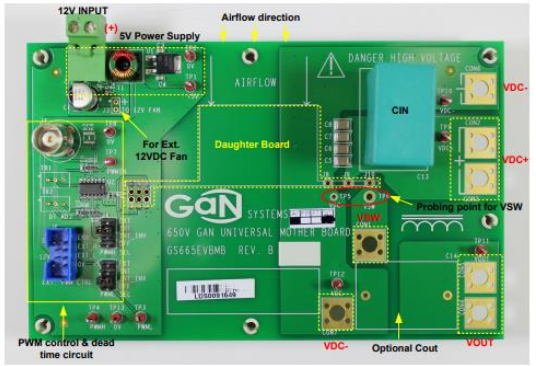
$$V_{1g} + V_{2g} + V_{3g} + V_{4g} = 0$$

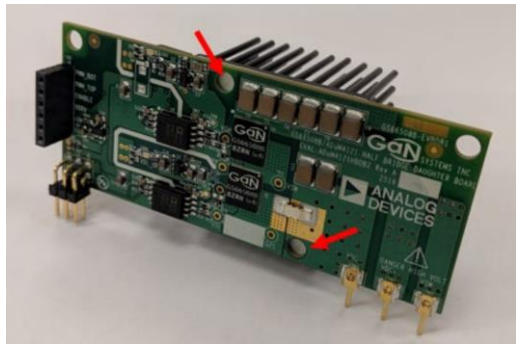
Fourth leg enables 16 switching states including states with 0 CMV

Using GaN Systems:
4x GaN 650V 2kW half bridge daughter boards
4x GaN universal evaluation boards

Four-leg inverter with WBG devices enables using Pulse Density Modulation (PDM) at higher switching frequencies while minimizing power losses due to faster turn-on/off times





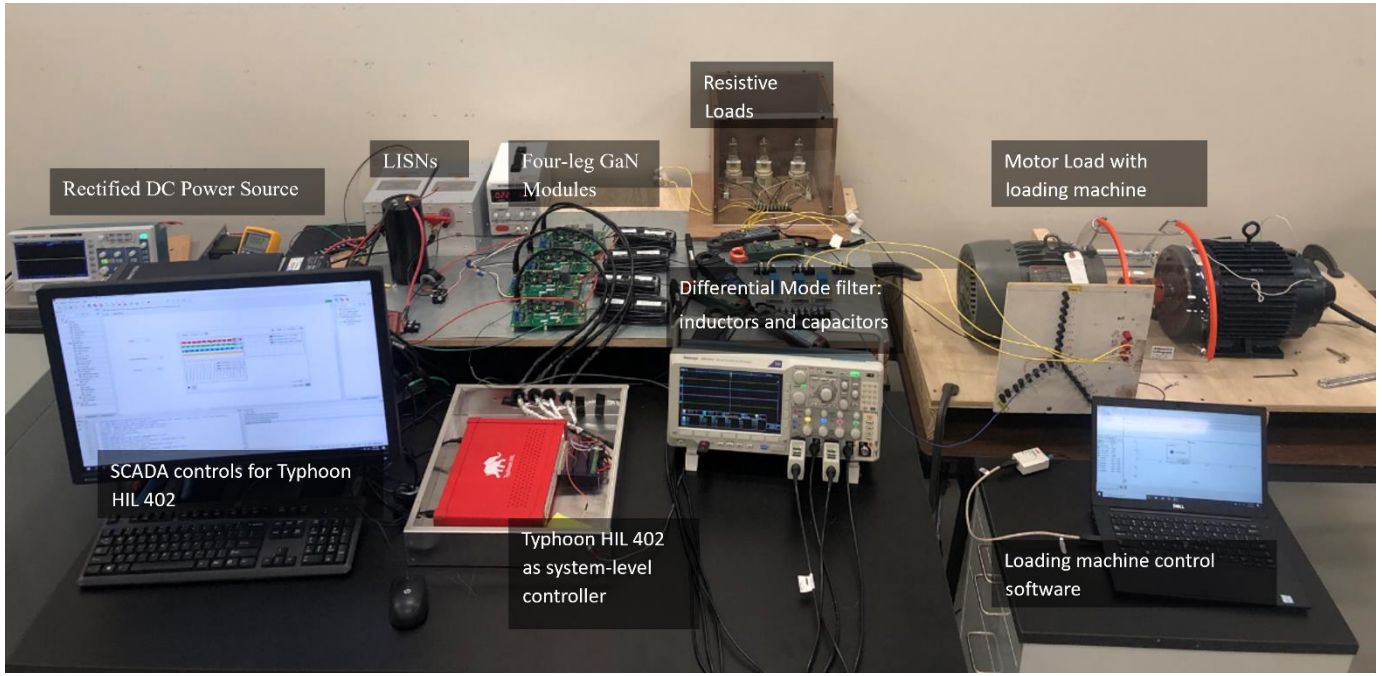


Keep two top switches on and two bottom switches on for 0 CMV →

Switching States	CMVs
1111	$\frac{V_{dc}}{2}$
1110, 1101, 1011, 0111	$\frac{V_{dc}}{4}$
1100, 1001, 0011, 0101, 1010, 0110	0
0001, 0010, 0100, 1000	$-\frac{V_{dc}}{4}$
0000	$-\frac{V_{dc}}{2}$

Baylor Testbed with Typhoon HIL 402

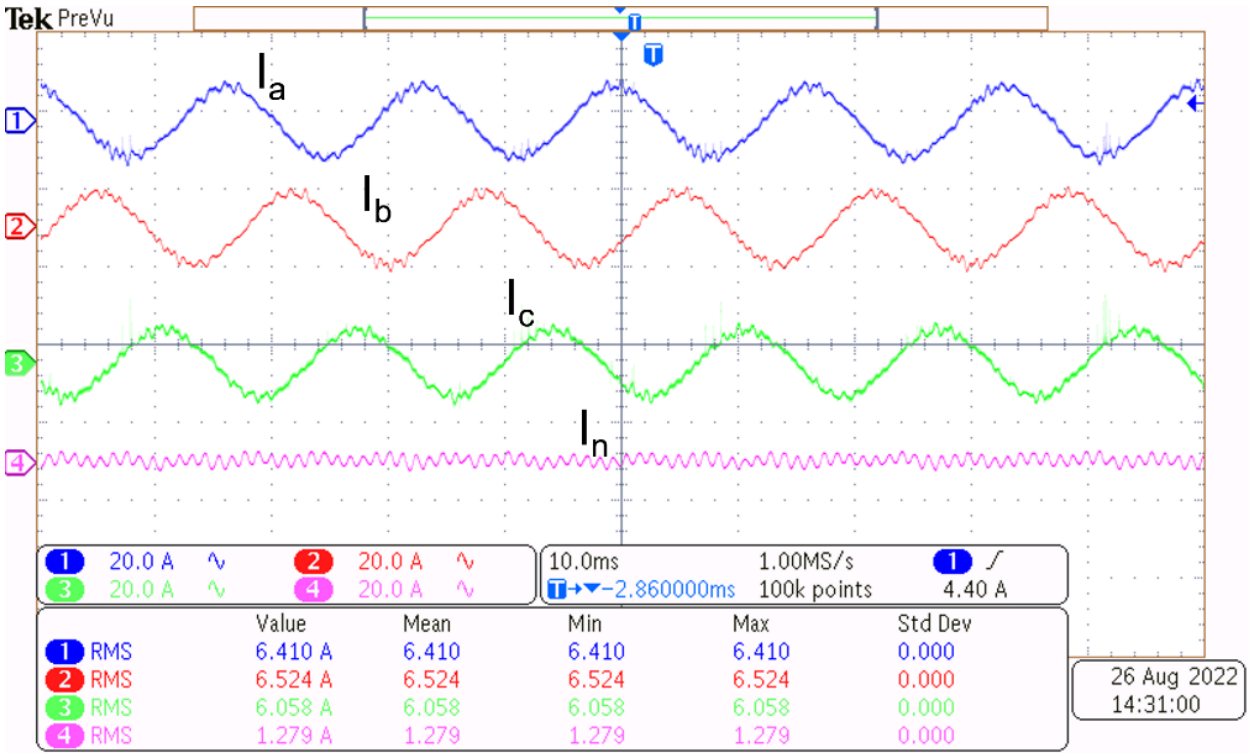
- GaN devices, four 650V, 2kW half bridge modules with high switching frequency capabilities (> 10 MHz)
- The switching frequency of the GaN module in the four-leg inverter at step of 1 µs is ~84kHz
- Typhoon HIL 402 is capable of 0.5 µs simulation step
- Models have different execution rates, including FPGA solvers. All execution rate related computations are completed within the defined 1 µs simulation step
- Thus, the ΣΔM is updating every 1 µs
- The LISNs and grounding plane were implemented according to MIL standard

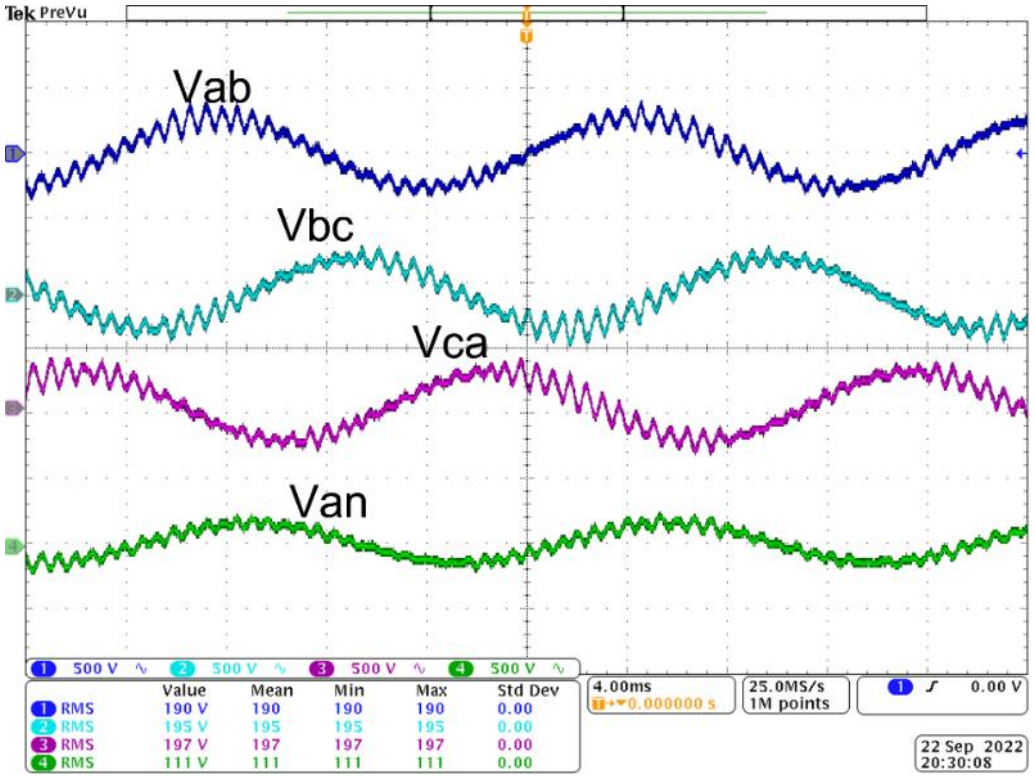


Four-leg inverter testbed for 230V/460V applications with various load options (balanced and unbalanced resistive loads and 5hp motor load with neutral access)

For motor load control, an ABB bidirectional/regenerative VFD is used to provide the proper current to the loading machine, to apply the desired torque to the motor under test

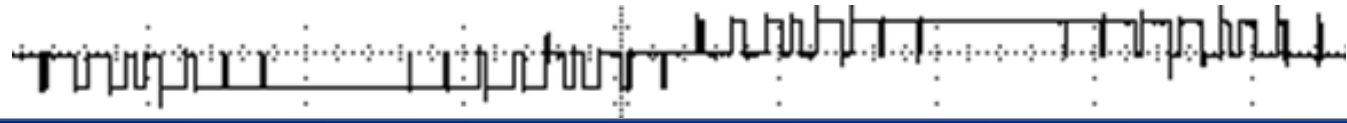
Experimental 230V 5hp Motor at 50% Load



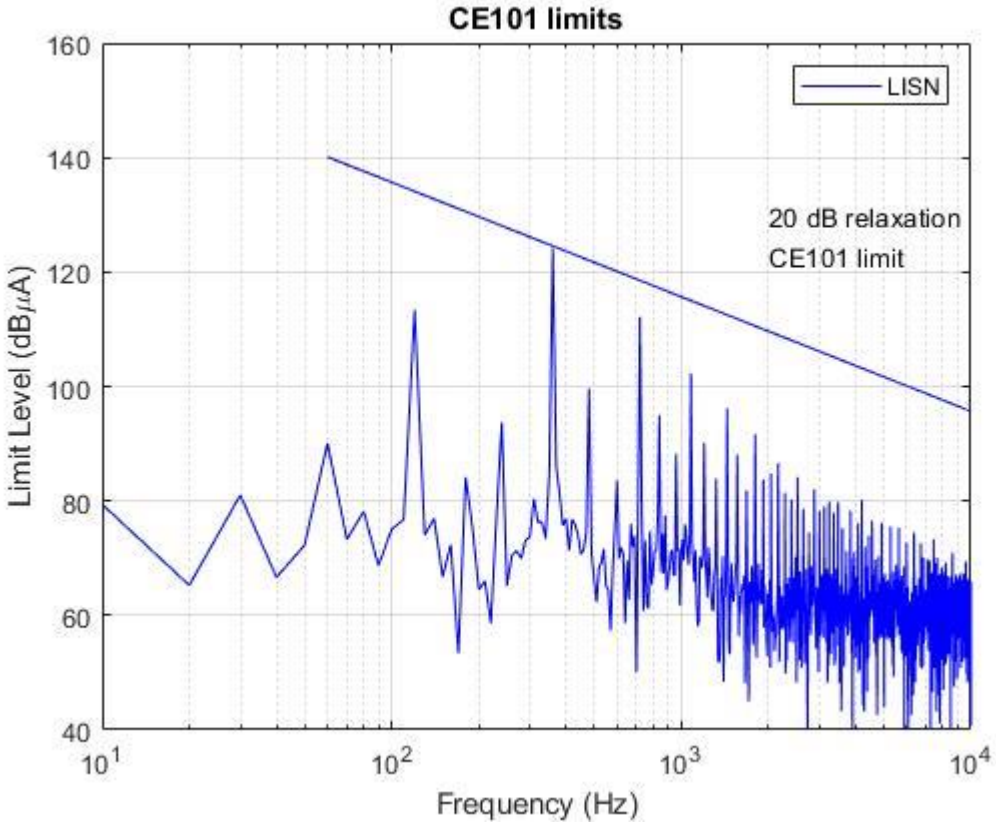


- Verification of sigma-delta PDM control of four-leg inverter for motor load applications
- Note the PDM voltages (reduced filtering requirements, $600\mu H$, 22nF LC filter) compared to square wave PWM (below)

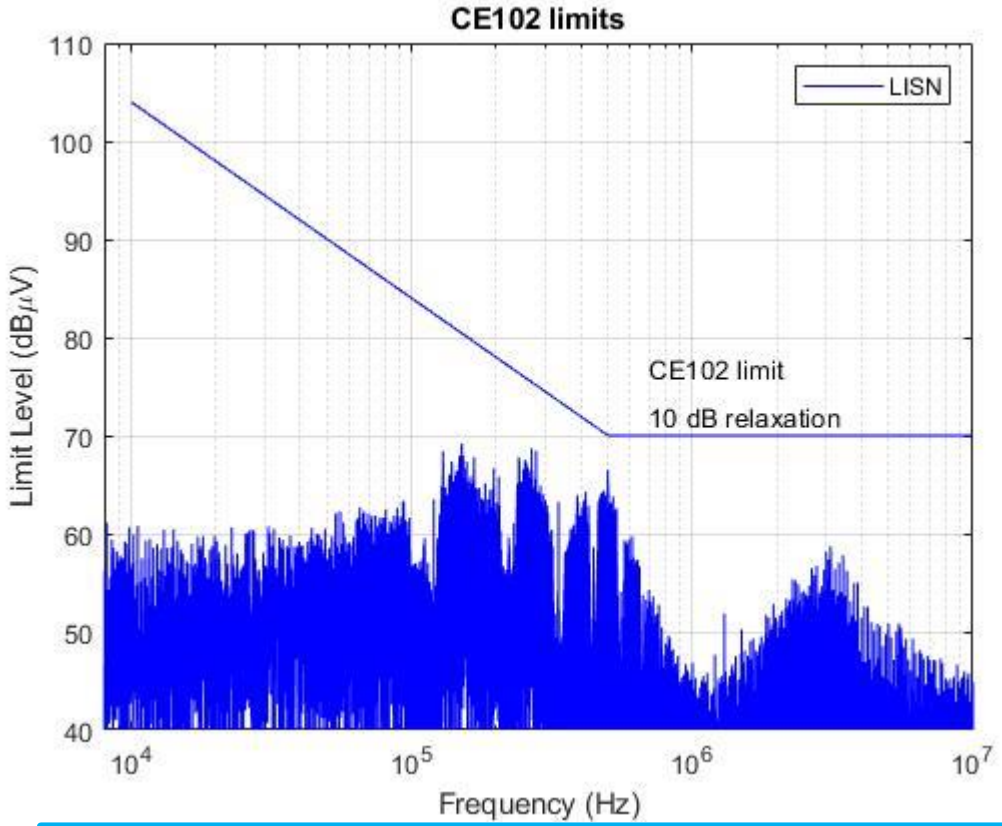
Courtesy of Prof. Annette von Jouanne – Baylor University



Conducted EMI on 5hp Motor at 50% Load



Measured LISN current versus CE101 limit



Measured LISN voltage versus CE102 limit

CE 101 and CE 102 limits are both met with no common mode choke

Conclusions and Future Work

- Physics-based models of power converters with CM paths are useful to predict conducted CM EMI and to explore mitigation strategies
- Three-phase inverters with a fourth leg and with PDM produce theoretically zero CM voltage
- CME methods simulated and experimentally validated for grid-forming and grid-following inverters using WBG devices
  - High frequency EMI not entirely eliminated, but easily suppressed with small passive filters
- Future work includes
  - Apply high frequency EMI modeling (from literature and collaborations) to improve predictions
  - Blanking time compensation methods to address high frequency EMI
  - PDM on multilevel converters

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  - Surface Navy Association's Award
- LT Ethan Foster, US Navy, NPS MSEE with Distinction - June 2022
- Capt Rob Tubbs, USMC, NPS MSEE expected Sep 2023

Collaborators at Baylor University

- Prof. Annette von Jouanne
- Prof. Emmanuel Agamloh
- Prof. Alex Yokochi
- Mr. Caleb Li, PhD candidate

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- A. L. Julian and G. Oriti, "Novel Common Mode Voltage Elimination Methods in Three-Phase Four-Wire Grid-Connected Inverters," in *IEEE Transactions on Industry Applications*, 2022, doi: 10.1109/TIA.2022.3211910.
- M. P. Storm, A. L. Julian, and G. Oriti, “Hardware implementation of a sic three-phase four-leg vsi with sigma-delta modulation to comply with the military standards 1399 and 461,” in Proc. of the 2022 IEEE Energy Conversion Congress and Exposition (ECCE), 2022.
- E. B. Foster, A. L. Julian, G. Oriti, M. P. Storm, “Rapid Prototyping of Model Predictive Control in a Grid-Following Three-Phase Inverter to Meet the Conducted EMI Limits in MIL-STD-461G” in Proc.of the 2022 IEEE Energy Conversion Congress and Exposition (ECCE), 2022.
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- A. L. Julian, G. Oriti, "Novel Common Mode Voltage Elimination Methods in Three-Phase Four-Wire Grid-Connected Inverters" in Proc. of IEEE 13th Energy Conversion Congress and Expo (ECCE) 2021, 10-14- Oct 2021.
- A. L. Julian, G. Oriti, A. J. Krener, "Eliminating Common Mode Conducted Emissions in Three-Phase Four-Leg Inverters" in Proc. of IEEE 2021 Electric Ship Technologies (Virtual) Symposium, August 2021.

Thank you!

Questions?