Stanford University

SUPER-Lab

Trials & Tribulations of Evaluating GaN and SiC switching devices

Kawin Surakitbovorn, Jungwon Choi, Lei Gu, Sanghyeon Park, Wei Liang, Luke Raymond, Emily Hernandez, Grayson Zulauf, Juan Rivas jmrivas@stanford.edu

Good progress made in low voltage power electronics

VICOR 400 V to 50 V dc-dc

Low Voltage Power Conversion

- Focus on moderate gain ratio step down
- Efficient, power dense converters commercially available
- Efficiencies in the upper 90%s
- Power densities approaching 3 kW/in³

≥ 2750 W/in³
≈98% efficient
► 1750 W



www.vicor.com

High voltage supply development has Lagged

- High voltage power supplies remain expensive and relatively inefficient
- If fast pulses are needed a high voltage switch is generally used in conjuction with a capacitor
- ► Efficiencies in the 60%s are common
- ► Typical power densities <10 W/in³

Ultravolt High Power C Series ▶ 9 W/in³

▶ 30 V to 2000 V dc-dc



www.ultravolt.com

high voltage circuits

- Various circuits can be used to generate high voltages:
 - Fly-back converters
 - Marx generators
 - Cockcroft–Walton multiplier
 - Quasi-resonant, resonant converters
 - and cascaded versions of these



- Parasitics, output impedance, device stress, etc, impose practical limits to the number of stages that can be cascaded to produce large voltage gains
 - CockcroftWalton multiplier limited to 10-12 stages due to loading effects

Resonant converter structure



Inverter	Transformation stage	Rectifier
Takes dc input power, deliver ac power	Provides impedance matching	Takes ac power, delivers dc power to R_L

[2] J.M. Rivas, O. Leitermann, Y. Han, et al, "A very high frequency dc-dc converter based on a class Φ_2 resonant inverter," in Proc. Power Electronics Specialists Conference, 2008. pp. 1657-1666 [4] W. Liang, J. Glaser, and J. Rivas, 13.56 MHz high density dc-dc converter with PCB inductors, in Proc. 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2013, pp. 633640.

Previous work involving a single stage resonant design



- ▶ 40 V to 500 V 27.12 MHz step up design was tested
- Output voltage limited by rectifier diode ratings
- ► Matching network quality factor (*Q*) increases with increasing gain ratio

[5] Raymond, L.; Wei Liang; Jungwon Choi; Rivas, J., "27.12 MHz large voltage gain resonant converter with low voltage stress," Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, vol., no., pp.1814,1821, 15-19 Sept. 2013

Class-D rectifier modification

$$\blacktriangleright$$
 $v_{\text{diode,max}} = V_{OUT}$

- Relatively low equivalent input resistance compared to related resonant rectifier topologies
- DC blocking capacitor can be split to achieve isolation



Isolation allows for multiple rectifiers



- Isolated rectifiers can be driven in parallel from a single input source
- Equivalent resistance seen by the ac source is R_{rect}/n
- Outputs can be added in series to achieve voltage gain
- Elimination or reduction of matching network
- ► *L_R* of each rectifier can be combined into a single inductor of value *L_R/n*
- Overall efficiency is equal to efficiency of each individual stage

High voltages at 10's of MHz



- Capacitive isolation feasible at 10's of MHz
- Cascading multiple converters for high voltage gain
- Also effective for impedance matching
- Fast pulse capability

12 Stage Design with Silicon



- ▶ 100 W 40 V to 2000 V dc-dc 27.12 MHz converter
- Silicon devices exhibit more ideal behavior allowing for 27.12 MHz operation
- ► 12 class-D stages for a voltage gain of 50 using a matching network with a quality factor of 2
- A single stage design would require a Q > 20

40 V to 2 kV Converter Performance



DC-DC Performance

- Ability to produce very square pulses
- ▶ 90% conversion efficiency (dc-dc)
- Silicon diodes yield 95 % rectification efficiency as expected

Pulsed electric field pasteurization



- ▶ High electric field $\approx 20 50$ kV/cm pulses causes rupture bacterial membranes
 - Render bacteria un-viable
 - ► Non-thermal means to pasteurize foodstuffs
 - Less energy intensive than thermal pasteurization
 - Effective for pasteurization, algai oil extraction, dehydration, wastewater treatment

Current PEF systems are costly and limited to industrial settings

Miniature PEF Experimental Setup: Water



- ► 2 kV/mm field strength
- Variable speed pump
- Pulse rate selected to ensure all water is treated at least once



Bacteria Test Results







- ▶ Tested Effectivness on E. Coli and Coliform
- 2-3 log reduction in measured bacteria levels
- ► Energy requirement of 0.5 Wh/L

40% of milk in some emerging markets spoils

- Small farmers can't afford current pastuerizing equipment
- Communities rely on a network of aggregators and milk collectors to process and distribute milk
- ▶ Weather, road conditions etc., can risk milk delivery





Photo credit: Nestle, Sri Lanka & Varick Schwartz, Kiva Fellow serving in Nairobi, Kenya

2 kW 13.56 MHz 275 V to 2 kV output isolated dc-dc



- ▶ 250 W/in³ including gate drive and cold plate
- 3 μ s transient response
- $2 \times \Phi_2$ inverters using GaN Systems 650 V MOSFETs
- ▶ 94% inverter efficiency
- ▶ 4x500 W rectifiers (SiC) with 500 V outputs in series
- ▶ 90% rectifier efficiency vs. 97% predicted by simulation model

Part I

Losses in WBG rectifying devices

Class D and Φ_2 Rectifiers Prototypes (40 V-500 V)



(a) Φ_2 Inverter- Φ_2 rect.



(b) Φ_2 Inverter–D rect Fig.: Schematic of implementd dc-dc converters



Fig.: Φ2 Inverter - L.P. Matching Network - Class D Rectifier

V_{IN} [V]	$\stackrel{\rm V_{OUT}}{[V]}$	Rectifier Class	Designed P _{OUT}	Sim. $\%\eta$	Exp. %η
40	500	Φ_2	40	89	35
30	300	$\Phi_{2}^{\tilde{2}}$	36	84	64
30	300	Φ_2^{-}	42	86	70
28	280	Ď	46	92	80

Losses in the diode were principal suspect as source of discrepancy

Class D and Φ_2 Rectifiers Prototypes (40 V-500 V)

Part	1 st Design
MOSFET diode	FDMC86116LZ C4D02120E
$\begin{array}{c} C_S\\ C_M\\ C_{MR}\\ C_P\\ C_{RMR}\\ C_{Extra}\\ C_B\end{array}$	2 nF 20.5 pF 99 pF 170 pF 13 pF 15 pF NA
$\begin{array}{c} \mathbb{L}_{F} \\ \mathbb{L}_{MR} \\ \mathbb{L}_{S} \\ \mathbb{L}_{M} \\ \mathbb{L}_{R} \\ \mathbb{L}_{RMR} \end{array}$	81.6 nH 81.6 nH 81.6 nH 1380 nH 750 nH 570 nH



The initial design utilized a Φ_2 rectifier

- Inverter alone was 93 % efficient as simulated.
 - Impedance matching was excellent.

Diode losses



Fig.: Thermal image of 27.12 MHz $\Phi_2 - \Phi_2$ dc-dc converter. Here $V_{IN} = 40$ V and $V_{OUT} = 500$ V. Converter is modulated on/off at 10 kHz with 10 % duty cycle. This was necessary to keep the temperature low for long enough to take pictures.

Initial design was 35 % efficient

Losses were not accounted for by models or information provided by manufacturers

Characterizing diode losses



Fig.: Class D rectifier connected to a low-pass matching network. Z_{IN} is designed to be resistive with a value of \approx 50 Ω

- Class D selected to it minimizes diode stress
- Rectifier tuned to look resistive at given *I*_{OUT}, *V*_{OUT}
- Low-pass matching network matches Z_{rec} to 50 Ω
- lower Z_i makes tuning of matching network easier

There should be only conduction loss in theory



- V_{out} = rectifier output voltage f_s = switching frequency I_{out} = rectifier output current
 - ► Voltage across diode *v*_D
 - Zero voltage turn-on
 - Current through diode i_D
 - Zero current turn-off
 - Junction capacitance energy recycled through resonance
 - Zero reverse recovery if SiC diodes are used

Characterizing Diode losses



- ► $f_s = 27.12$ MHz, $I_{OUT} = 75$ mA, $Z_i \approx 50\Omega$
- $\frac{d}{dt}v(t)$ can exceed 100 V/ns
- Notice discrepancy between simulated loss breakdown and total measured loss





Diodes studied

Mfg	Part no.	Туре	V _{Rmax}	I _{Fmax}
Cree	C4D02120E	SiC	1200 V	4.5 A
STMicro	STPSC6H12	SiC	1200 V	6 A
Genesic	GB02SLT12	SiC	1200 V	2 A
Cree	C3D04060E	SiC	600 V	7.5 A
Cree	CSD04060E	SiC	600 V	4 A
STMicro	STPSC406	SiC	600 V	4 A
Infineon	IDD03SG60C	SiC	600 V	3 A
Diodes Inc.	DFLS1200	Si	200 V	1 A



Datasheet and spice models can be incomplete or inaccurate

Rapid method to evaluate junction capacitance

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Test setup





- Z_i matched to $\approx 50 \Omega$
- Constant *V*_{OUT}, Zener load
- Different design for each diode and V_{OUT}
- ▶ Minor tuning through C_{extra}



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Performance measurements of 600 V CREE SiC diode





Measured vs. Simulated Efficiency for C3D04060E

- $V_{OUT} = 170 \text{ V}, 350 \text{ V} \text{ and} 500 \text{ V}$
- Experiments and simulations match well
- In all cases $I_{OUT} = 75 \text{ mA}$

 Discrepancies between measurement and simulation increase with increasing V_{OUT}

600 V SiC diode loss comparison

Estimated Diode loss at various output voltages, I_our=50mA (600V SiC Diodes)



Notice that the diode loss is similar at both current levels but increases significantly with output voltage.

1.2 kV SiC diode loss comparison



Notice that the Diode loss is similar at both current levels but increases significantly with output voltage

Direct Comparison



6/11/2014, 15:15:22.885.7

6/11/2014, 15:39:36.763.1



D₁ ST Microelectronics
 D₂ Infineon



D₁ Infineon
 D₂ ST Microelectronics

GaN's zero reverse recovery raised hopes for improvement

▶ Tying the gate to the source makes GaN FET behave like a diode.



Eric Person (Infineon) "Practical Application of 600 V GaN HEMTs in Power Electronics", Professional Education Seminar, APEC 2015

The experimental efficiency did not match the simulation

▶ 100 W 500 V 27.12 MHz class-D resonant rectifier with *GS66502B* working as a diode.



	Simulation	Experiment
Efficiency	94%	90%
Power loss in total	6W	11 W
Power loss per device	0.8W	3.0W

Power loss comparison of devices with similar V-I ratings

- ▶ Blue bars are GaN FETs and red bars are SiC diodes.
- ► GaN FET power loss is much larger than predicted by simulation.



Power loss comparison of devices with similar V-I ratings

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The observed power loss is not switching loss

- Voltage across GaN Systems part in 50mA 27.12MHz rectifier at various output voltages
- The waveforms show that soft switching is occurring and the capacitor energy is being recycled.



The power loss increases with voltage

- The offset from the conduction loss remains almost constant with the increasing dc current.
- This additional power loss increases with the voltage across the device.

The additional power loss from the conduction loss *GaN Systems* part at f = 27.12 MHz



The power loss increases with frequency

- The offset from the conduction loss remains almost constant with the increasing dc current.
- ▶ This additional power loss increases with the frequency.



The power loss increases with temperature

Power loss per device in 25 W rectifier at 27.12 MHz and 500 V output voltage



Part II

Evaluation of GaN transitors at high frequencies

How do we achieve precise simulation?

Accurate models for passive components

Circuits only contain air-core high Q inductors and high Q ceramic capacitors

 Equivalent Series Resistance (ESR) approx. is accurate enough



Accurate parasitic component values matching

Done by reverse-calculating parasitic component values from the measured drain impedance



How de we achieve precise simulation?

Accurate models of the semiconductor devices

Rely on manufacturer provided models

- ► Most of the time the models are accurate
- Some time the models are incomplete or wrong



• Two most important parts of the model are:

- ► On Resistance $(R_{ds,ON})$
- ► Nonlinear output capacitance *C*_{OSS}

How accurate do we typically get?

- ▶ 100 W Inverter @ 27.12 MHz with FDMS8622
 - ▶ 100 V Fairchild N-Channel Power Trench Silicon MOSFET
 - Max $R_{ds,ON} = 56 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}, I_D = 4.8 \text{ A}$
 - Simulated with manufacturer provided model
 - ► Simulation efficiency: 90%
 - ► Test efficiency: 89%





Advantages of GaN transistors

Lower input and output capacitance (C_{ISS} and C_{OSS})

- ► Faster rise time and fall time
 - Lower switching loss
 - Lower gate loss
 - ► Higher switching frequency



Lower on resistance $(R_{ds,ON})$

- Lower conduction loss
 - ► Higher efficiency
 - Smaller heatsink

Better packages!

- Most GaN devices come in low inductance packages
- Can't say the same on SiC (T0-220, To-247)

The problem comes when we started designing converters with GaN transistors

Test efficiencies greatly differ from the simulation

- #1 Class Φ_2 inverter with GS61008P
 - ▶ 27.12 MHz, 40 Vdc input, 100 W output
 - Simulation predicts 94.5% efficiency
 - $\blacktriangleright \approx 1.4$ W loss in the FET
 - ► Test result $\approx 89\%$ efficiency
- ▶ #2 Class D rectifier with GS66502B
 - ► V_{gs} = 0 V, GaN transistors configured as diodes
 - 27.12 MHz, 260 Vpp AC input, 400 V, 80 W output
 - Simulation predicts 93% efficiency
 - $\blacktriangleright \approx 1 \text{W}$ loss in each FET
 - ► Test result $\approx 84.5\%$ efficiency





Thermal images show the losses in the FETs to be up to 3-4 times the losses predicted by the simulations





This is very interesting to us because

Resonant converters only have conduction loss

- ► If on-resistance (and forward voltage) is accurately model, the experimental losses should match the simulation losses
- ► This suggests that there are extra losses beyond the Ron loss
 - ► Not yet accurately modeled
 - Not switching loss
- Could vary significantly depending on manufacturers technologies and voltage level
 - ► The same as in the SiC diodes study
- ▶ Potentially a high frequency (MHz) phenomena
 - Designers using GaN at standard switching frequencies (100s of kHz) do not notice this problem

What are potential sources of the extra losses?

Losses in the output capacitance of the transistor (C_{oss})

- ► Usually modeled with a series resistance
 - ► But could also be distributed and require a more complicated model in MHz frequency
- If this loss dominates, using a bigger device to reduce Rdson will not necessary reduce the overall loss

Losses due to dynamic $R_{ds,ON}$

- Due to charge trapping, devices on-resistance presents a value many times its DC value immediately after being switched on
- This behavior has been mitigated, but may still affect converters operating at MHz frequencies



Acknowledgent

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6.78 MHz SiC MOSFET RF inverter

Parameter	Measured	Simulated
V _{ds.max}	940 V	942 V
Vout, rms	332 V	333 V
Pout	2204 W	2224 W
efficiency	93%	96%



Class Φ_2 inverter with the SiC MOSFET

- ► Gate driver: IXRFD630 (IXYS 30 A Low-Side RF MOSFET Drive)
- Switching frequency: 6.78 MHz (ISM band frequency)
- ▶ Inductors: air-core, solenoidal type inductors. Q is above 250.