Reliability of GaN Power Transistors in Power Supply Applications

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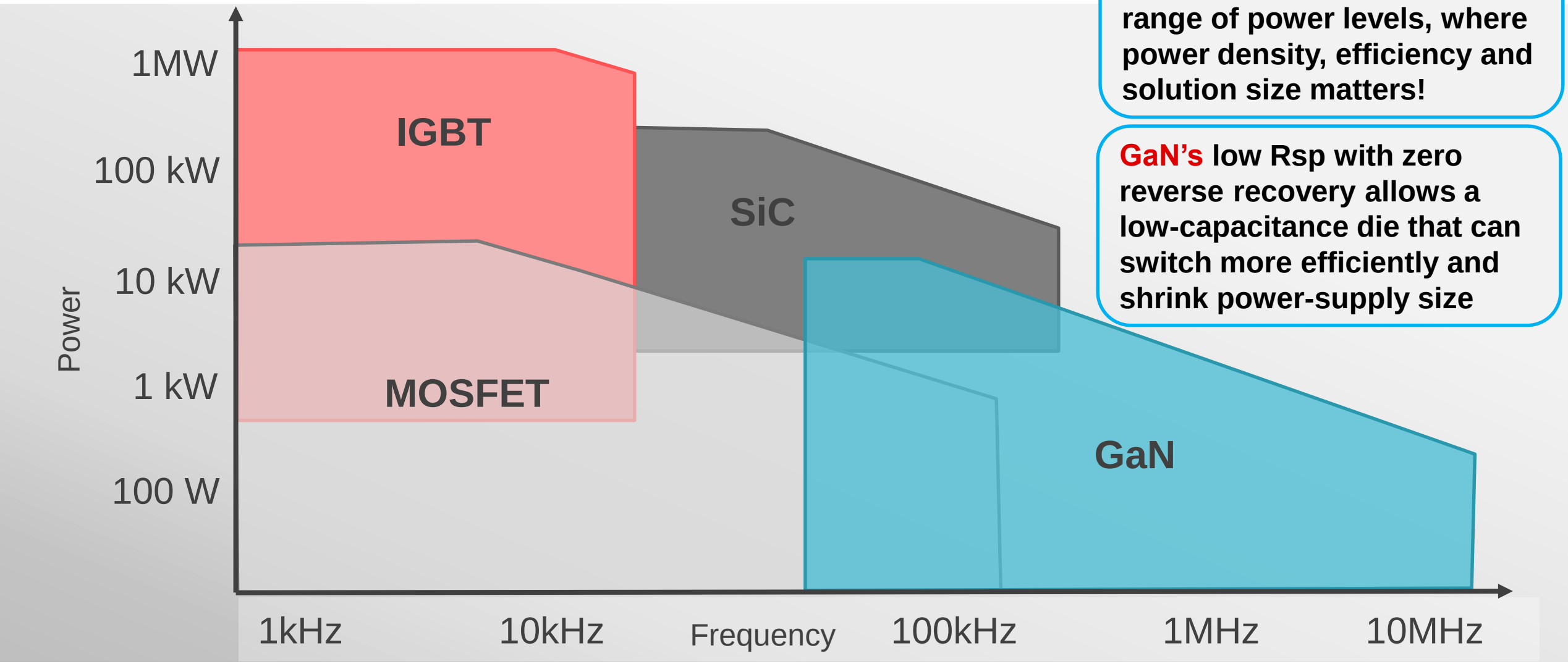
Outline

- Introduction
- Traditional Si qualification and gaps for power management
- Steps to achieving reliable GaN
- Validating application reliability
  - Component-level reliability
  - Datacenter, server, telecom mission profiles
  - Power-supply level reliability (DHTOL, JEP180)
- Reliability for unusual and extreme conditions
  - Surge robustness without avalanche
  - Short circuit withstand

Benefits of GaN

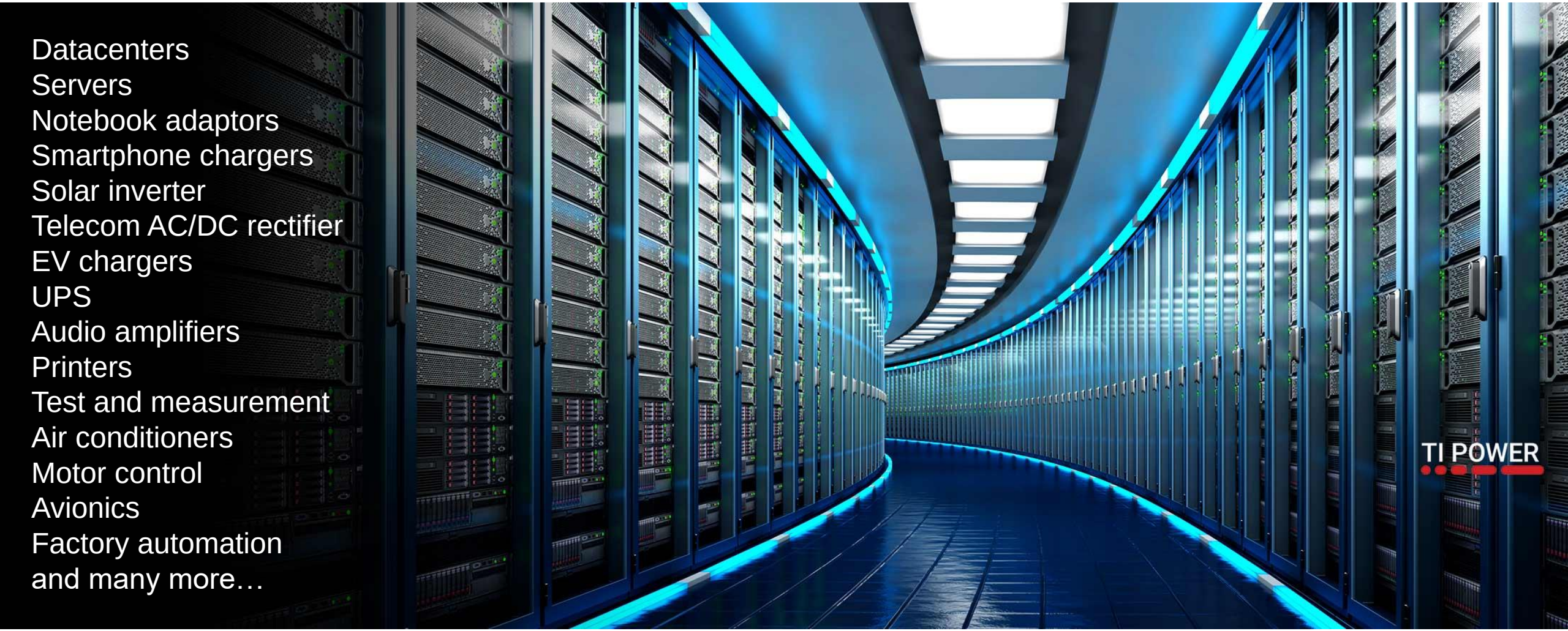


GaN enables high-frequency power converters for a wide range of power levels, where power density, efficiency and solution size matters!

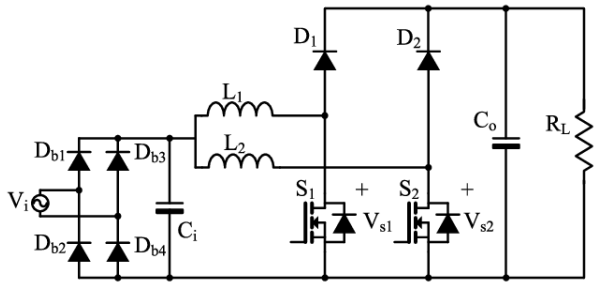
GaN's low Rsp with zero reverse recovery allows a low-capacitance die that can switch more efficiently and shrink power-supply size

GaN is used for a wide variety of applications

Datacenters
Servers
Notebook adaptors
Smartphone chargers
Solar inverter
Telecom AC/DC rectifier
EV chargers
UPS
Audio amplifiers
Printers
Test and measurement
Air conditioners
Motor control
Avionics
Factory automation
and many more…



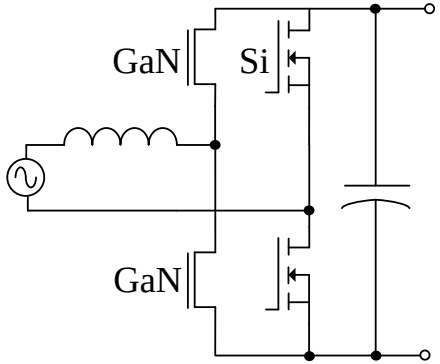
GaN enables datacenter energy savings Lowers Opex $



4kW Interleaved PFC with Silicon MOSFETs

Efficiency

98.0% → 98.8%



4kW Bridgeless totem-pole PFC with GaN

Calculations	Total	Units
Datacenter power per year	100,000	kW
Energy in 1yr (computing + cooling), 24/7, 365	876,000,000	kWh
Energy for computing	438,000,000	kWh
Efficiency improvement using TP PFC	0.8	%
Energy savings in computing	3,504,000	kWh
Energy savings in computing + cooling	7,008,000	kWh
Electric energy unit cost	0.1	$/kWh
Savings/yr	700.8	$k
Energy savings over 10-yrs	**7,008**	**$k**

- GaN enables totem-pole bridgeless PFC, which is not realizable with Si MOSFETs
  - high Qrr of Si power MOSFETs can cause shoot-through in this topology
  - GaN has zero Qrr
- **GaN provides $7M savings in a 100MW data center over 10-yrs through +0.8% efficiency gain**
- *Let's see what is the reliability of GaN for this application?*

What does traditional Si qualification mean?

1. **Devices should not fail with best-practice stress testing**

Use case	Qualification condition			Use condition	
	Tj (°C)	Time (h)	Ea (eV)	Tj (°C)	Time (y)
Traditional	125	1000	0.7	55	8.9
Power	150	1000	0.7	105	1.1

2. **There should not be many field returns**
   - Zero fails out of 3x77 parts leads to the defectivity and FIT rate statistics below

Metric	Value	Confidence	criteria
Fail% (LTPD†)	<1%	90%	0 fails/231 for non-accelerated time
FIT rate¶	<50	60%	0 fails/18.2M run hours

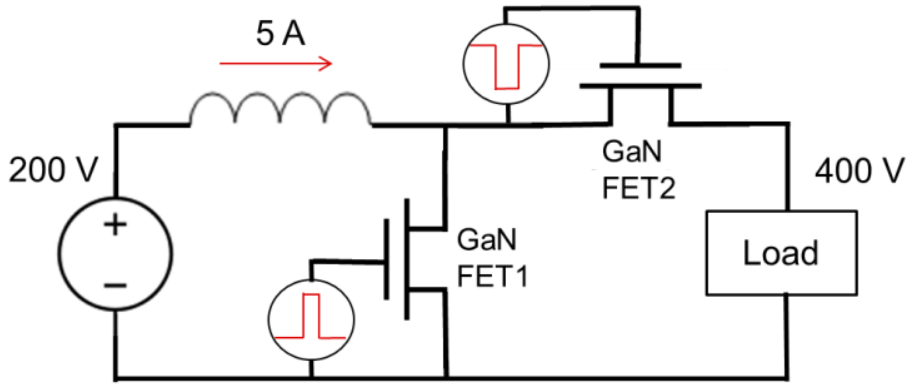
However, this assumes that the stress testing is representative of actual-usage.

- Traditional Si qualification testing does not consider the switching conditions of power management. This is a weakness in the Si methodology itself.

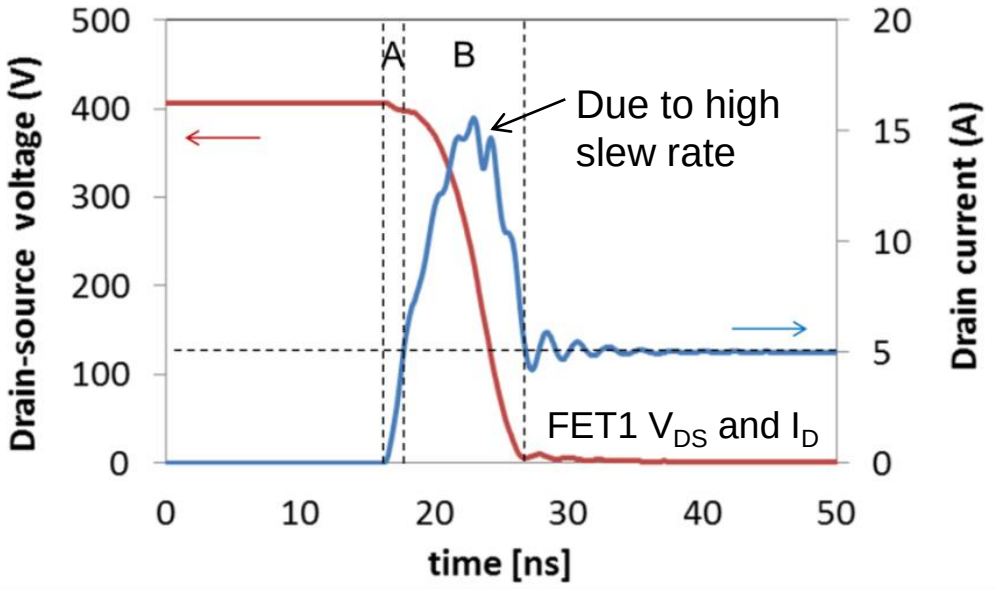
† LTPD=Lot Tolerant Percent Defective
¶ 1 FIT=1 fail in 1E9 device hours

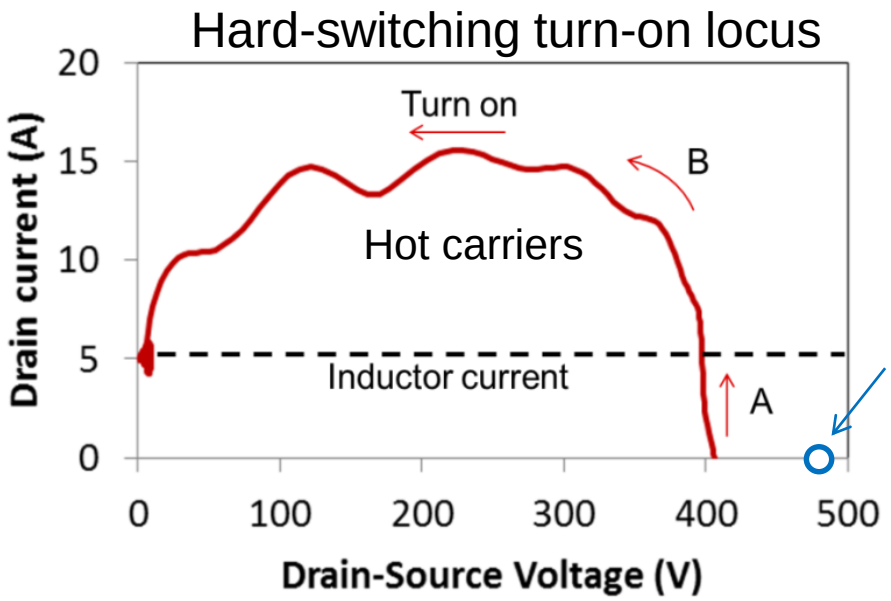
"*A comprehensive methodology to qualify the reliability of GaN products*", available at www.ti.com/lit/wp/slyy070/slyy070.pdf

Switching reliability is not traditionally covered



state	mode	coverage
Static	off	HTRB
	on	HTGB
Switching	(hard) turn-on	(?)
	(soft) turn-off	(?)
Power-supply level	shoot-through, reverse recovery etc	(?)





Typical High Temperature Reverse Bias (HTRB) test (off-state)

Switching can excite different failure mechanisms vs off-state, e.g. hot-carrier related, power-supply level

"*Product-level Reliability of GaN Devices*", IEEE IRPS 2016, available at www.ti.com/lit/ml/slyy093/slyy093.pdf

Is GaN* reliable?
Is that the right question….. *anymore*?

*(power FET)

- For mature technologies, customers do not ask, e.g *is Si reliable*?
- The question is typically “did this FET pass qualification?”

- GaN now has considerable reliability experience, and a JEDEC committee (JC70) with GaN-specific guidelines, e.g. *JEP180*
- There is now a common approach to validate the reliability of GaN power FETs

- The question is not “Is GaN reliable?”, but “did this GaN FET pass qualification?”

“*Is GaN reliable, or is that the right question?*”, available at https://e2e.ti.com/blogs_/b/powerhouse/posts/is-gan-reliable

Steps to achieving reliable GaN

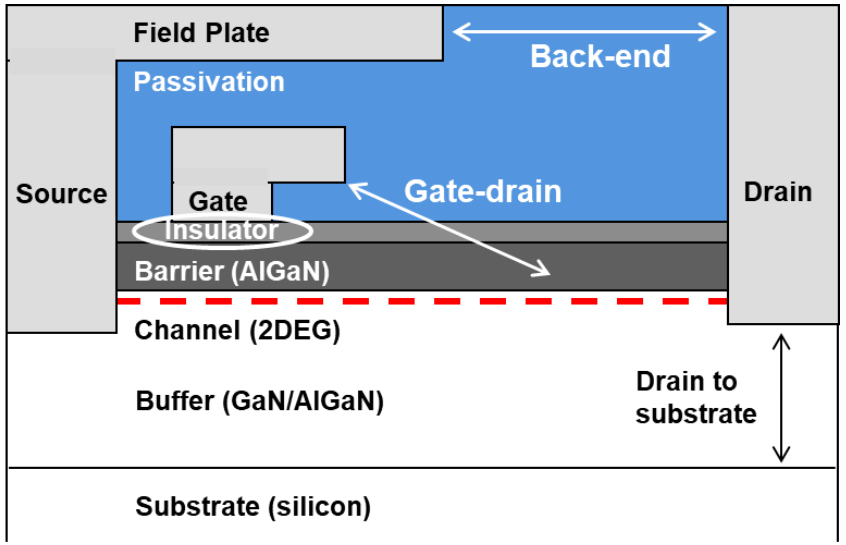
Component level	Standards/guidelines
Established framework for Si qualification and reliability	**JESD47, AEC-Q100/Q101, JEP122**
GaN failure mechanisms, Lifetime extrapolation	**JEP122, JEP180**
GaN-specific test methods	**JEP173:** Dynamic ON-Resistance Test Method **JEP182**: Continuous Switching Test Method

Power-supply level	
Switching reliability for power management usage of GaN	**JEP180:** Switching Reliability Evaluation for GaN Power Devices
Extreme operation (lighting surge, short-circuit)	**IEC 61000-4-5, VDE0884-11**

"*Achieving GaN Products With Lifetime Reliability*", TI Technical Whitepaper, available at www.ti.com/lit/wp/snoaa68/snoaa68.pdf

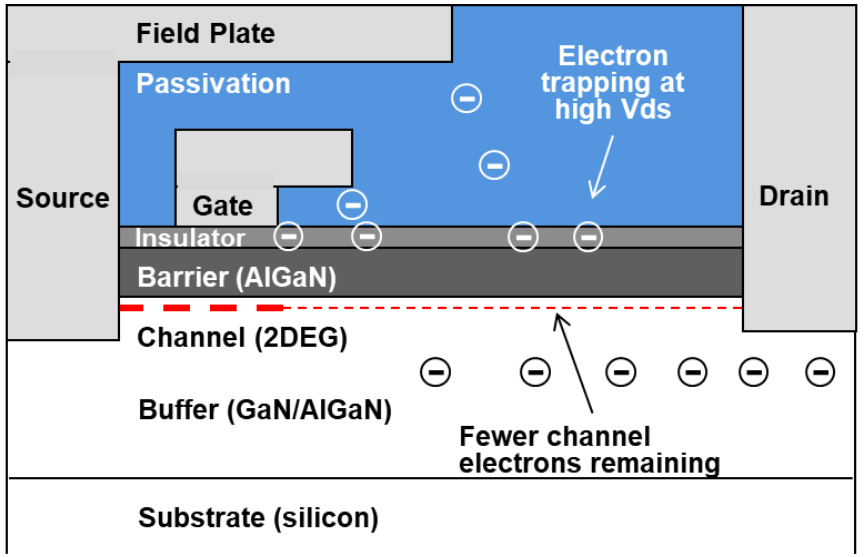
Component-level failure mechanisms

1. Time dependent breakdown (TDB)



- High fields cause defect generation over time, increasing the leakage currents and causing eventual hard-failure
- Well known and studied for dielectrics used in Si IC's

2. Charge trapping

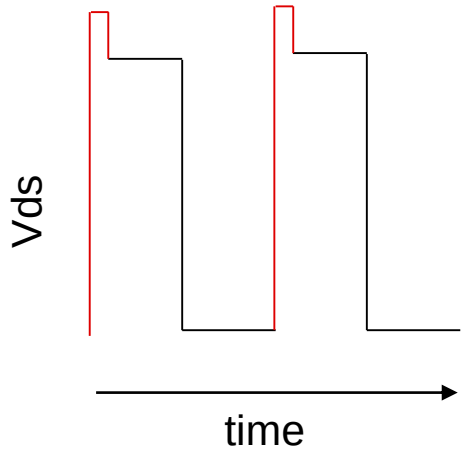


- Charge is trapped due to high voltages and by hot electrons created by hard-switching
- This increases on-resistance by repelling channel electrons, which increases channel resistance.
- Dynamic Rds-on is high on the timescales of switching. It is difficult to measure on a tester, since the traps discharge quickly.

3. Hot carrier wearout (discussed later)

Reliability calculations need mission profiles

A mission profile is the simplified representation of all of the relevant conditions to which a device will be exposed in its intended application throughout the full life cycle (1)



50% duty cycle
60 V ring, 30 ns
150 kHz

Datacenter and server

Load level	Time spent	Tj (°C)
10%	10%	72
20%	20%	73
50%	50%	79
100%	20%	97

Typical bus voltages are 400-450 V

Telecom

Load level	Time spent	Tj (°C)
80%	90%	88
100%	10%	97

Typical bus voltages are 400-430 V

(1) JEDEC JEP148B

Reliability assessment for TDB failure mechanism

TI has built a Time Dependent Breakdown (TDB) model incorporating 1.8M device hours of testing using special test structures

Datacenter and server

Load level	Time spent	Tj (°C)
10%	10%	72
20%	20%	73
50%	50%	79
100%	20%	97

Telecom

Load level	Time spent	Tj (°C)
80%	90%	88
100%	10%	97

10 year FIT rate calculation for LMG3422R030 part for the TDB failure mechanism (1 FIT is one failure in 10^9 operating hours)

1.44×10^{-2} FITs for V_bus=450 V

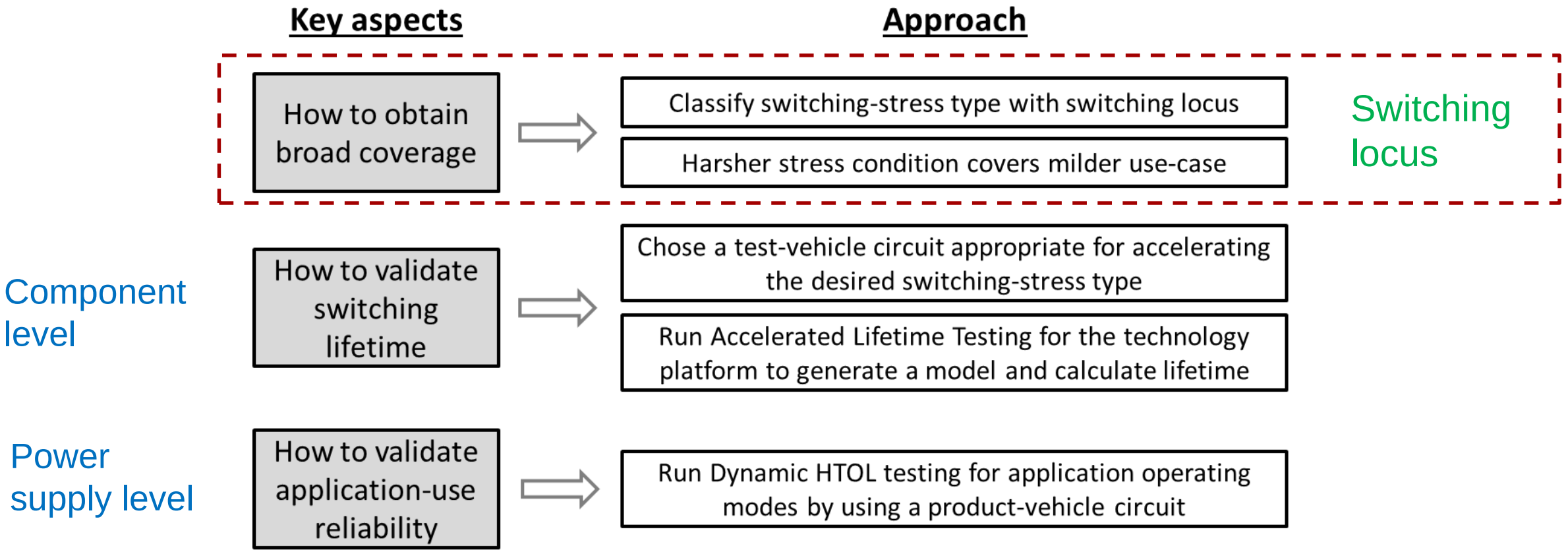
1.52×10^{-2} FITs for V_bus=430 V

TI GaN parts are reliable to TDB for datacenter, server, and telecom mission profiles

Switching reliability: JEP180

(JEP180 is a free download with a guest account at www.jedec.org)

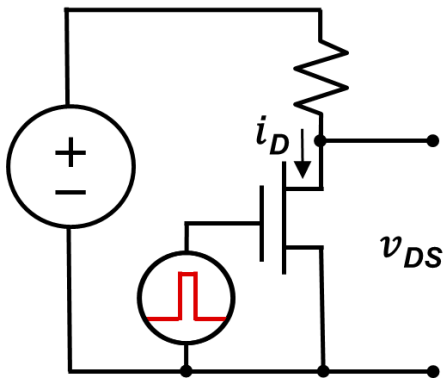
- Traditional qualification does not consider the switching stress of power supplies
- JEP180 assures that GaN parts will operate reliably in the intended application



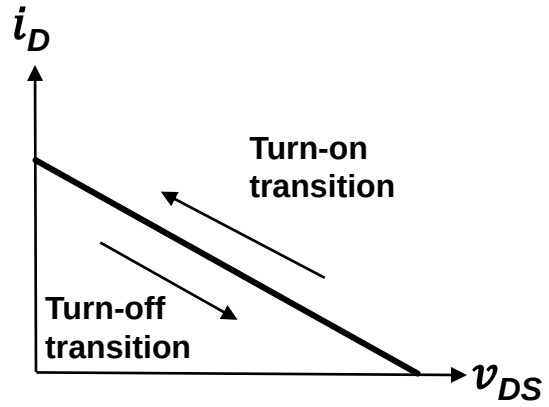
JEDEC JEP180, "*Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices*", Fig. 1

Switching locus curve - introduction

- The switching locus curve is familiar to many engineers
- Switching locus curve shows the trajectory of the i_D-v_{DS} waveform during a switching cycle
- A common example is the load line for resistive-load switching



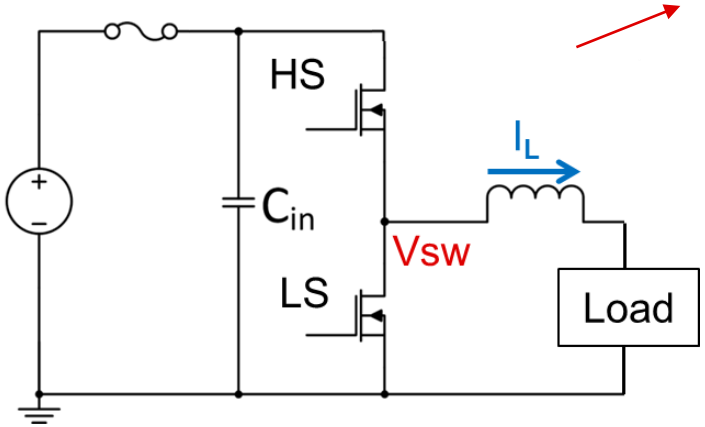
Switching locus curve for resistive switching



Source: Fig. 2, JEDEC JEP180

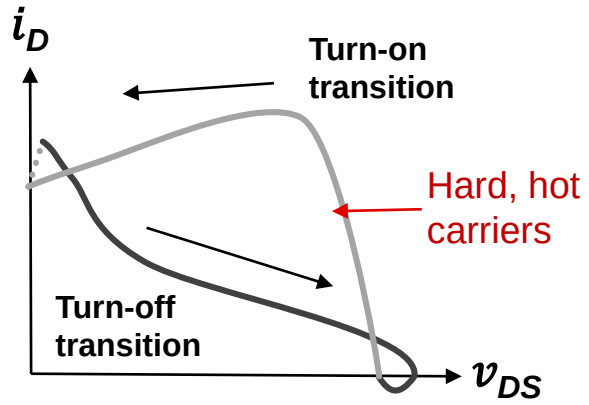
Switching locus : classify switching stress

Buck converter

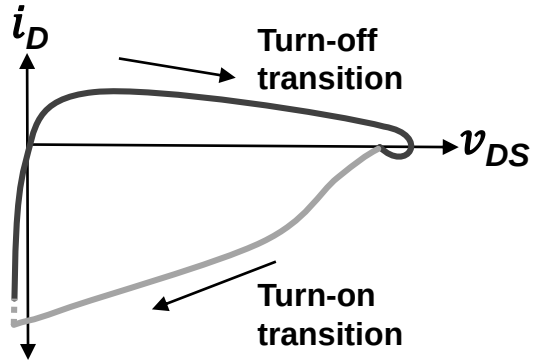


Boost converter: Interchange high and low-side loci

High-side device in a buck converter (hard turn-on). Turn-off is not hard since the channel is off while Vds rises (i_D is from Coss charging).



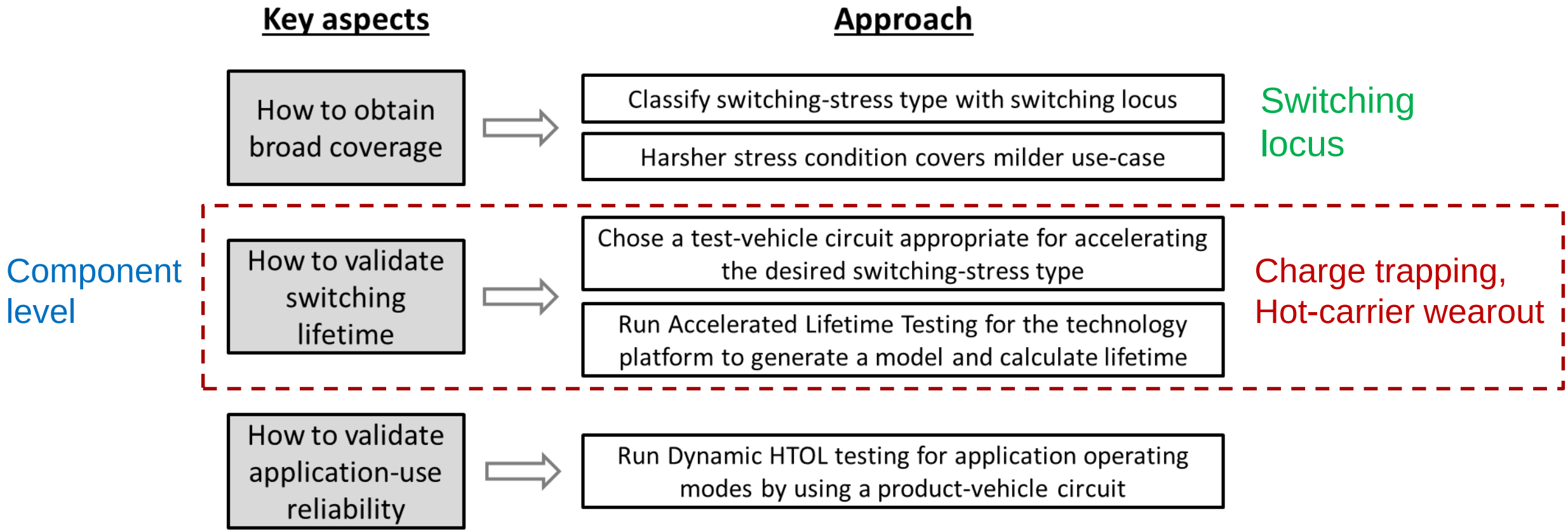
Low-side device in a buck converter (soft turn-on and turn-off)



Switching locus figures source: Fig. 2, JEDEC JEP180

A test-vehicle circuit applying relevant switching stress (judged by the switching locus) will provide broad coverage for all circuits with that type of locus

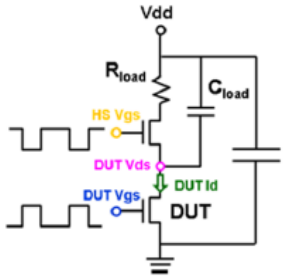
Determining switching lifetime: JEP180

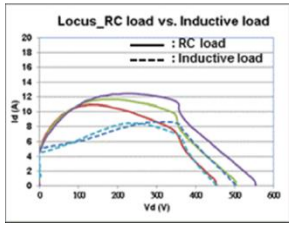


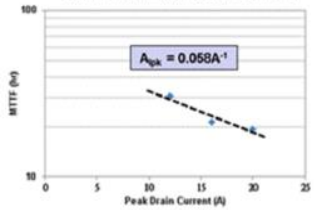
Source: Fig. 1, JEDEC JEP180

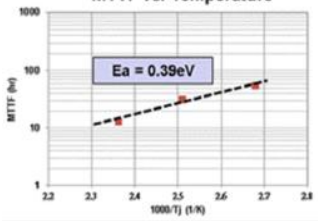
Literature summary on switching lifetime

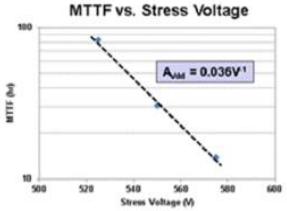
600 V – 650V GaN FETs





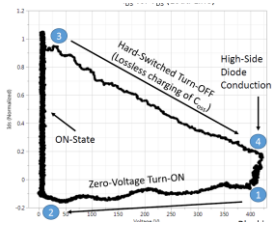


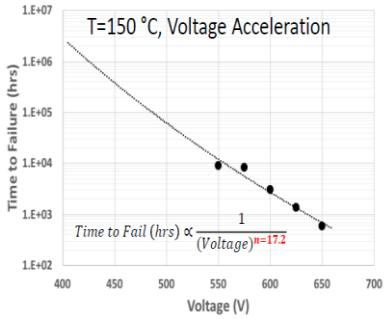


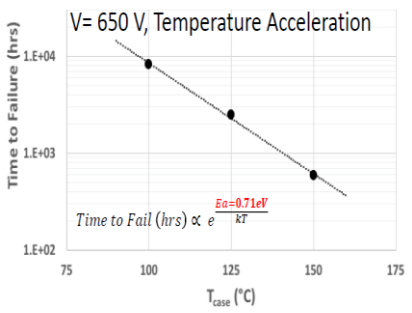


M. Lin et al. (TSMC) "New Circuit Topology for System-Level reliability of GaN", ISPSD 2019, p299

Switching locus

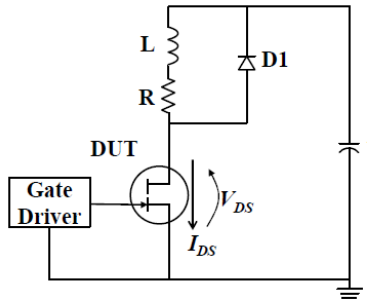


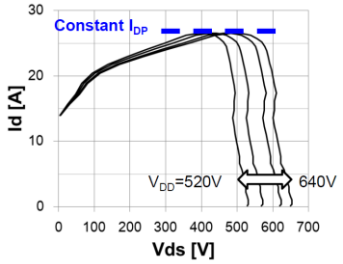


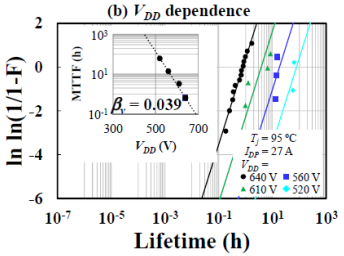


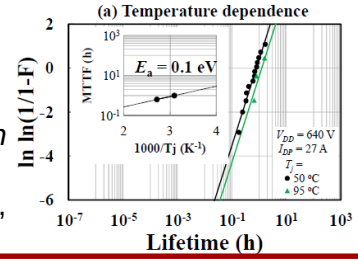
D. Gandhi (Navitas), "Systematic Approach to GaN Power IC Reliability, APEC PSMA Industry session IS11, 2019

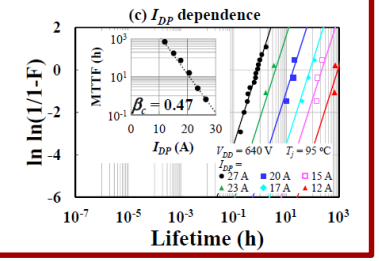
TI switching lifetime: following slides



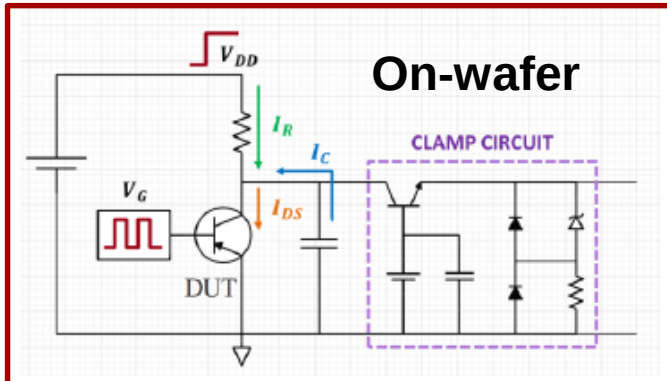


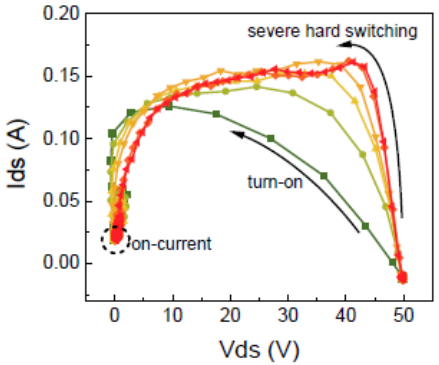






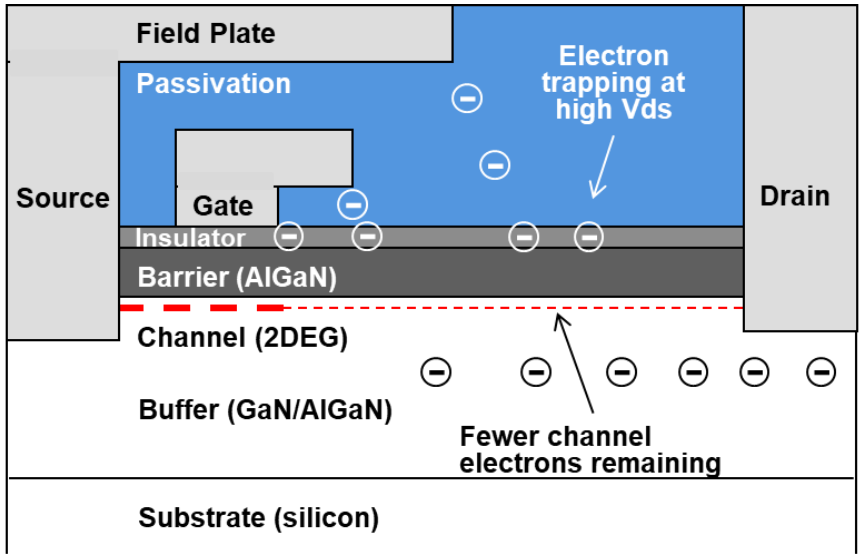
A. Ikoshi et al. (Panasonic), *Lifetime Evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under Practical Switching Operations*, IRPS 2018, p4E2-1

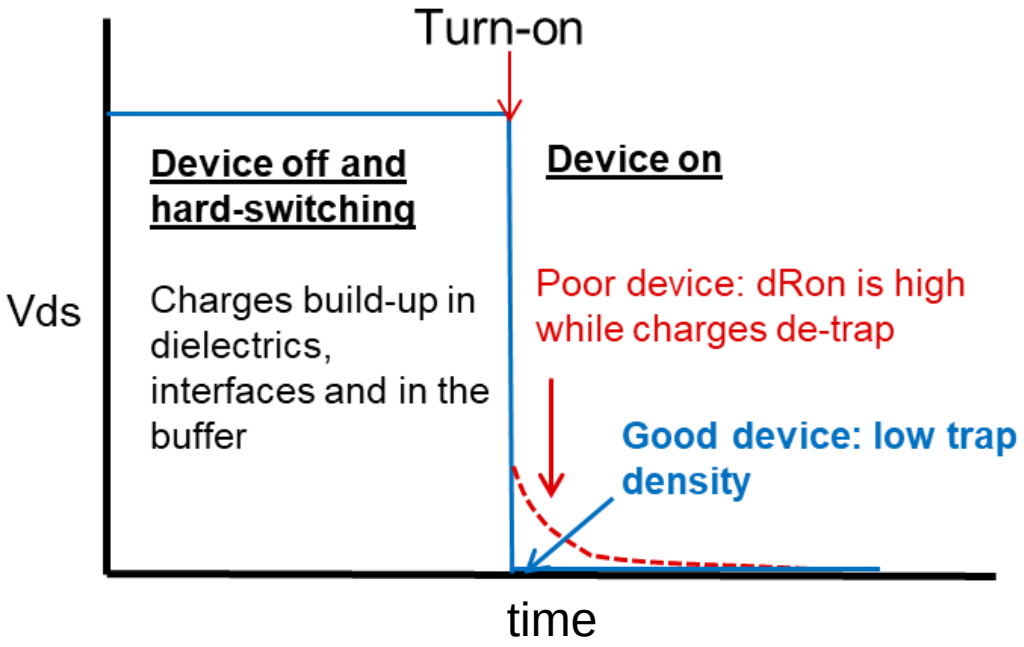




N. Modolo et al. (U. Padova), "*A Generalized Approach to Determine the Switching Reliability of GaN HEMTs on-Wafer Level*", IRPS 2021

Charge trapping: dynamic Rds-on with aging

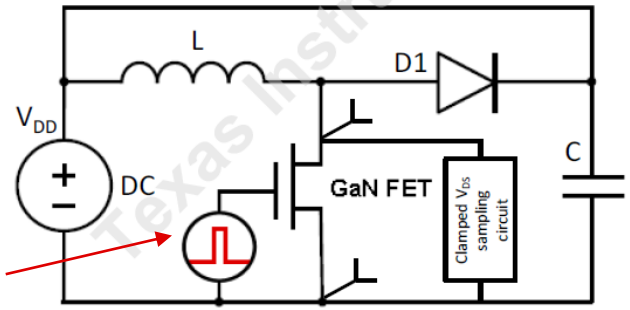




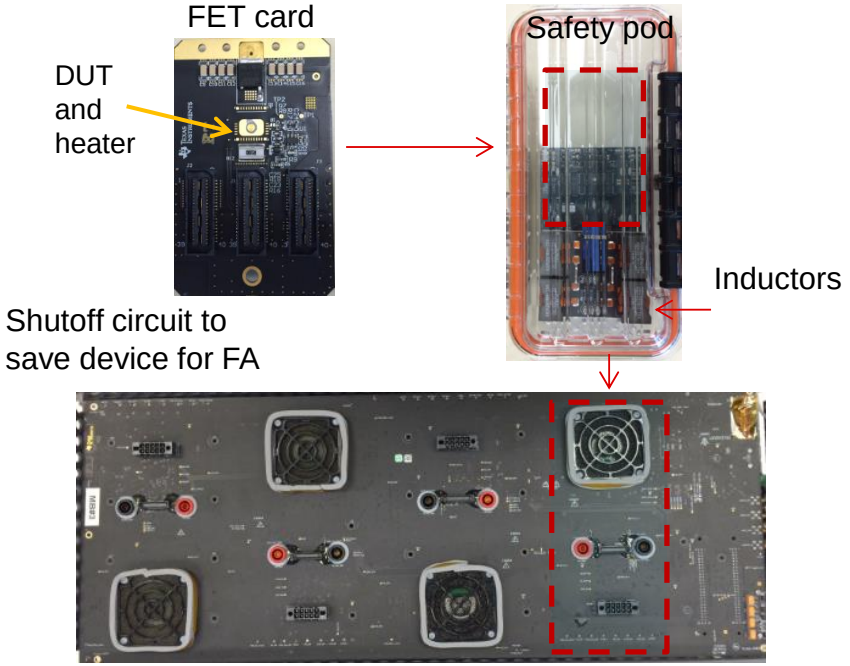
- Charge trapping causes higher dynamic Rds-on, which results in more self-heating and lower efficiency
- Device aging can increase trap density and result in higher dynamic Rds-on
- Need to validate that new traps are not being generated with aging

Validating dynamic Rds-on reliability

Stress circuit per
JEP 182
dRon measured
per JEP 173



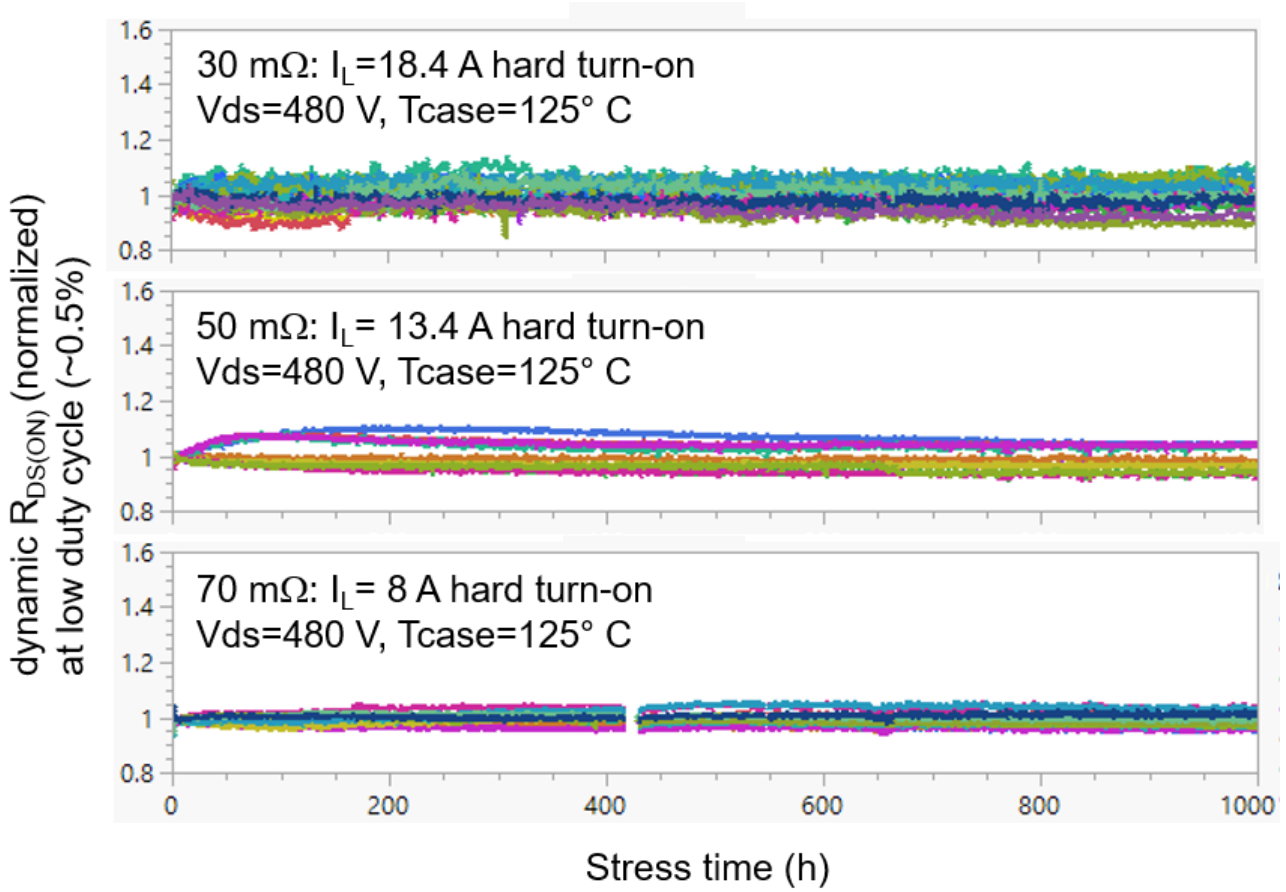
Turn on to measure
dRon within 1-usec



Hard-switching test system, for dynamic Rds-on (and hot-carrier wearout) reliability

Dynamic Rds-on does not increase with aging

- Low duty-cycle stress provides high trap filling and higher sensitivity to charge trapping (1)
- It provides an early detection method for aging by making dRon sensitive to early-stage traps (less electrically active).
- Stable dRon at low duty cycle demonstrates lack of new trap creation and excellent material quality with aging

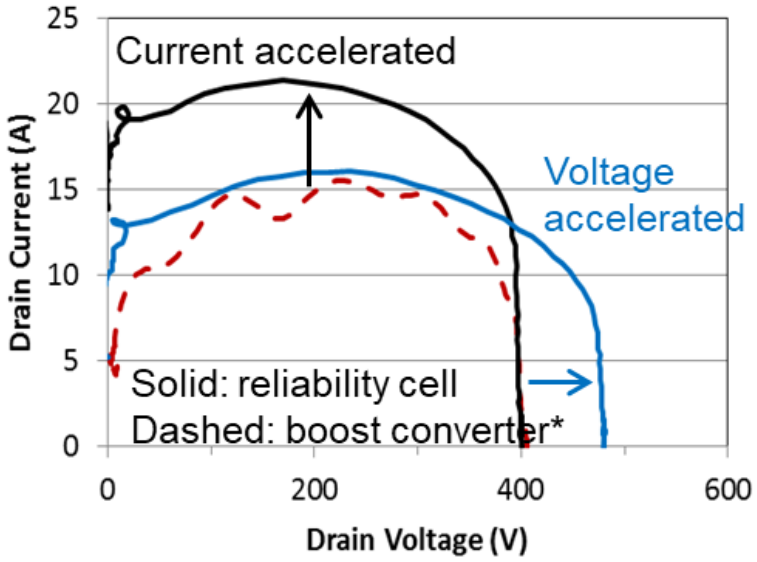


Stable dynamic Rds-on with aging at high-voltage, high-current, high-temperature, hard-switching

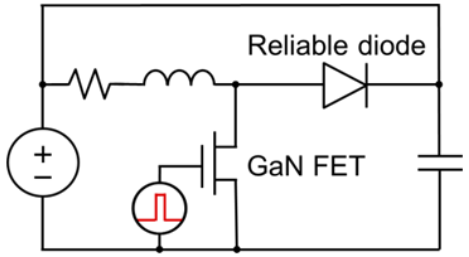
(1) J. Bocker et. al, "*Ron Increase in GaN HEMTs – Temperature or Trapping Effects*", IEEE Energy Conversion Congress and Exposition (ECCE), p. 1975, 2017.

Hot carrier wearout: switching lifetime model

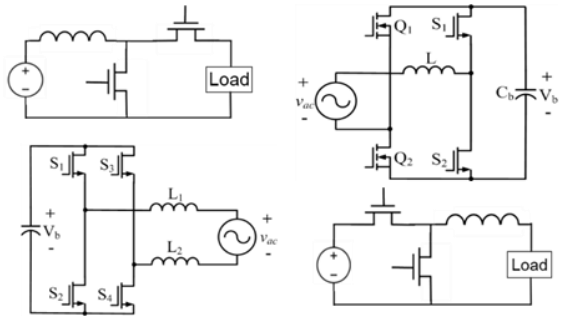
- Hard switching generates hot carriers, which can cause hard-failure from wearout.
- TI tests for hot carrier wearout by using accelerated hard-switching



Stress using a test-vehicle circuit suitable for accelerated stress



Evaluate switching lifetime for broad application use



Construct switching stress model

Voltage acceleration

- **Exponential model (TDDB):** $TTF \propto e^{-\beta_V(V_{DS})}$ — β_V=0.109

Current acceleration

- **Exponential model:** $TTF \propto e^{-\beta_C(I_{Ch})}$ — β_C=0.283
- **Power-law model:** $TTF \propto (I_{Ch})^{-n}$ — n=3.1

(electromigration, hot-carrier)

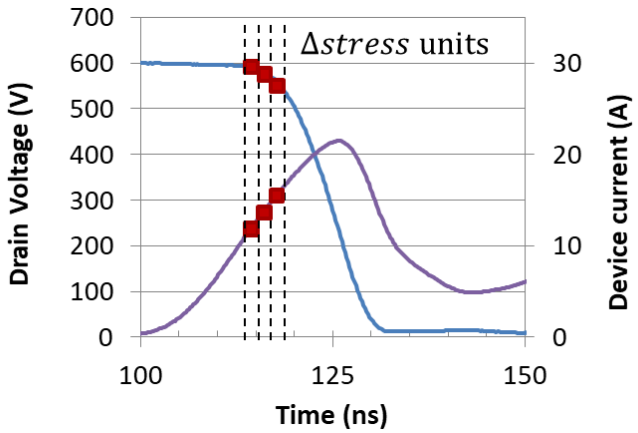
Temperature acceleration

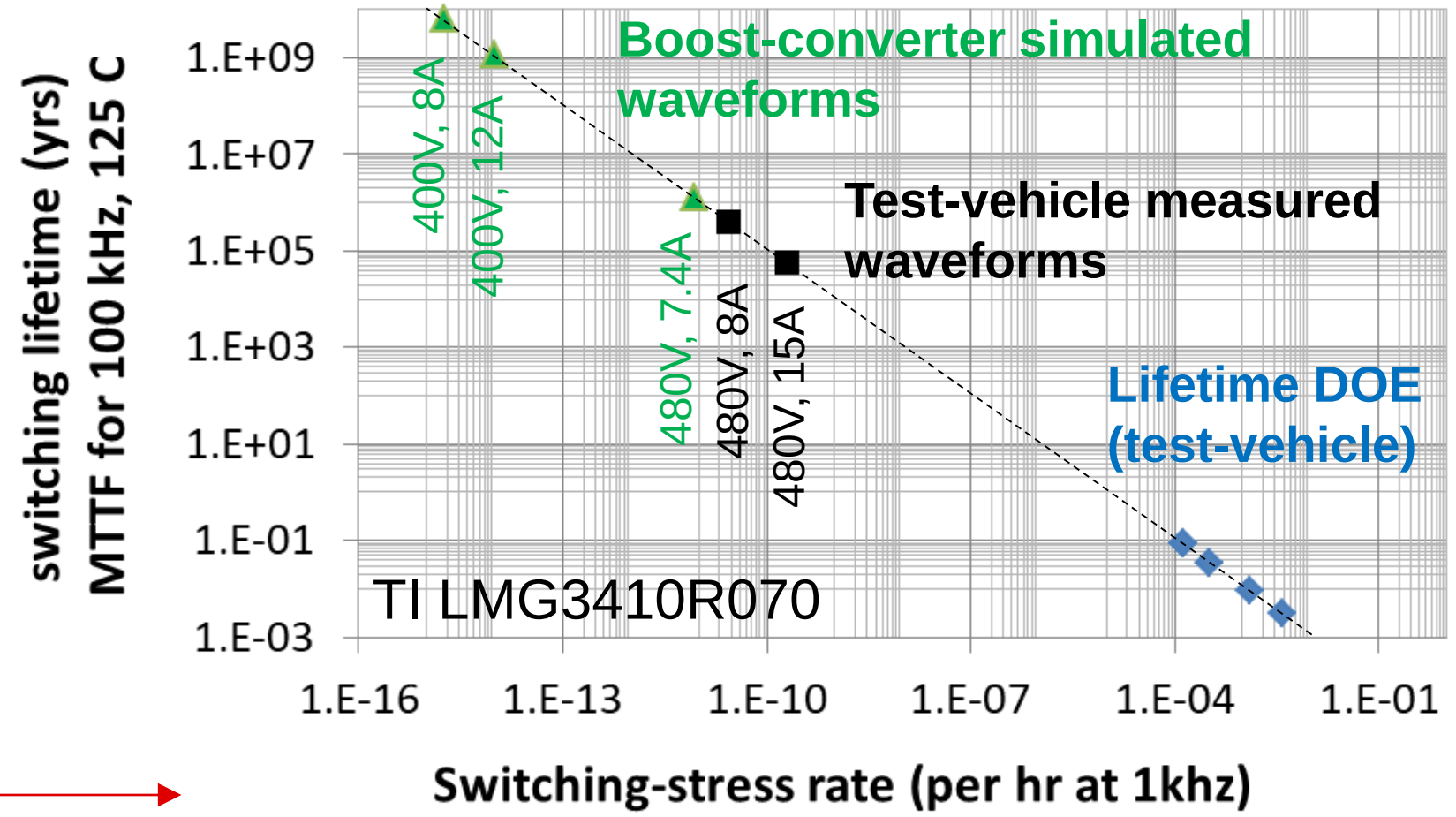
- **Arrhenius model:** $TTF \propto e^{\frac{Ea}{k}[\frac{1}{T}-\frac{1}{To}]}$ — E_a=0.7 eV

"*A Generalized Approach to Determine the Switching Lifetime of a GaN FET*", IEEE IRPS 2020, available at www.ti.com/lit/ml/slyy196/slyy196.pdf

Hot-carrier wearout: hard-switching lifetime

Switching stress:
Integrate Vds and Id
while applying
acceleration factors





- Over 1 billion years switching lifetime for 400 V, 8 A hard-switching at 100 kHz
- *Hot carrier wearout is not an issue!*

Hard-switching reliability for datacenter/telecom

Calculation using TI Hot-carrier wearout model

Datacenter and server

Load level	Time spent	Tj (°C)
10%	10%	72
20%	20%	73
50%	50%	79
100%	20%	97

Telecom

Load level	Time spent	Tj (°C)
80%	90%	88
100%	10%	97

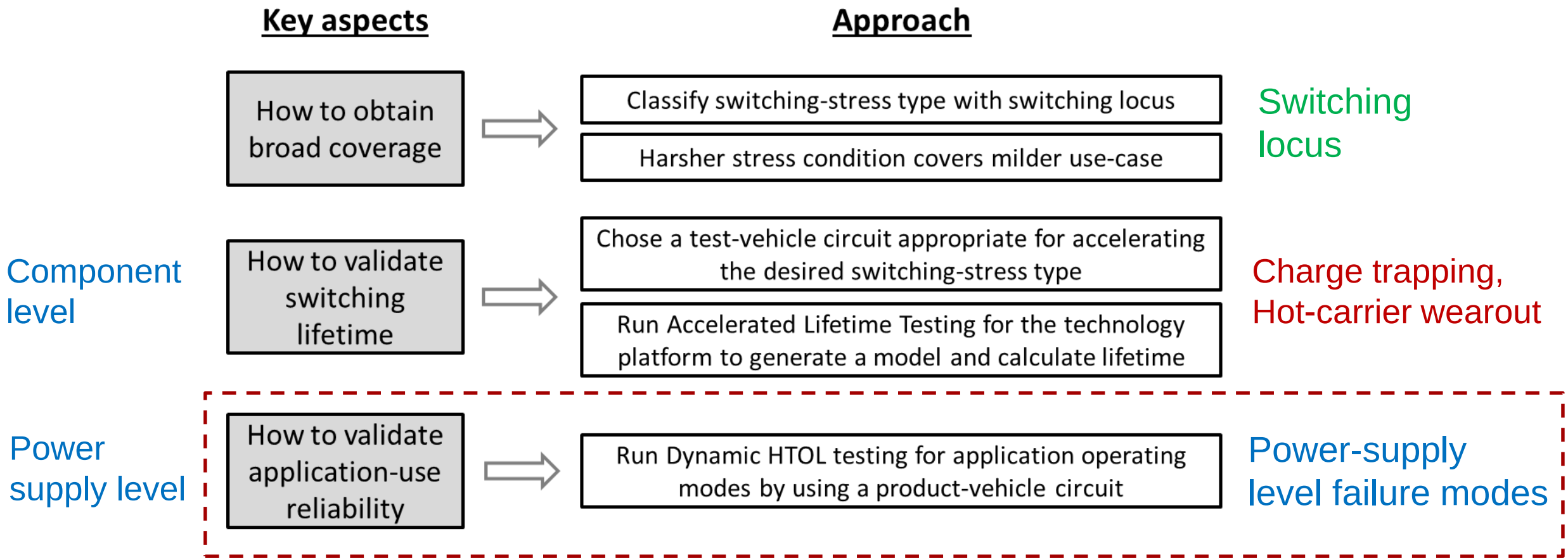
MTTF (Mean Time to Failure) calculation for operation at 150 kHz

8×10^8 yrs for V_bus=450 V

4.4×10^9 yrs for V_bus=430 V

TI GaN parts will not fail in datacenter/telecom applications due to hot-carrier wearout

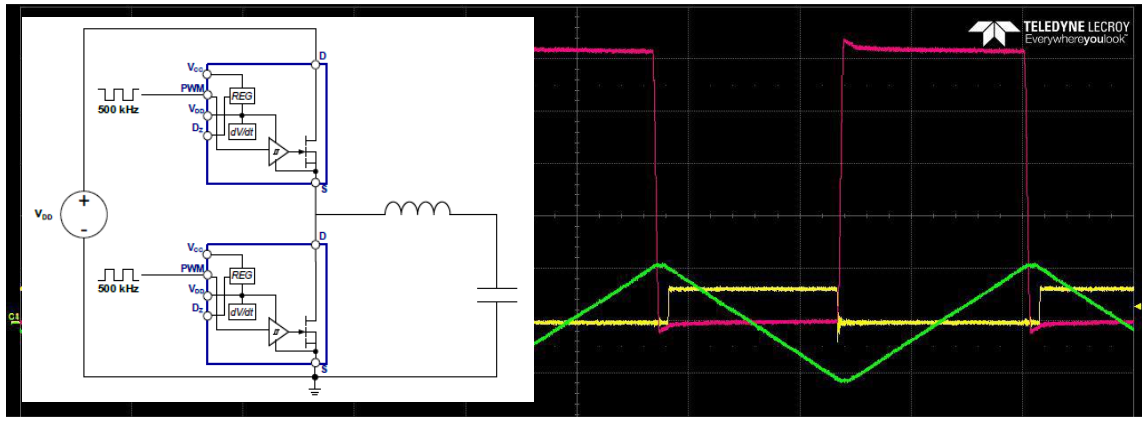
Validating power supply usage reliability: JEP180



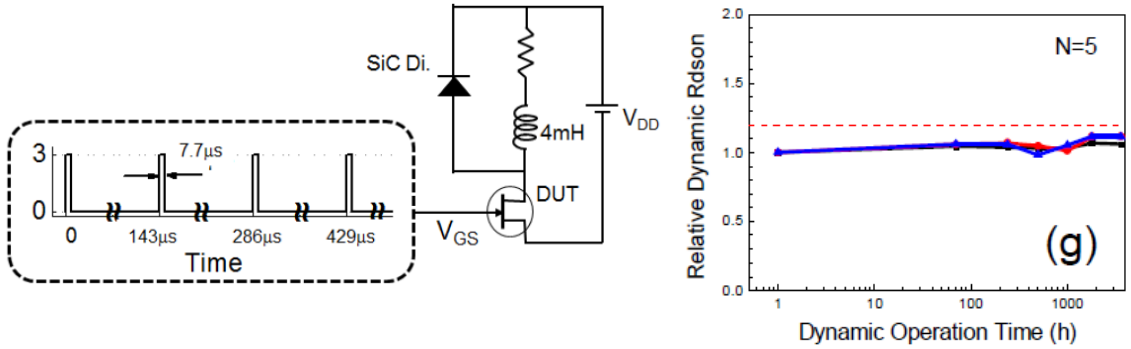
Source: Fig. 1, JEDEC JEP180

Literature summary on DHTOL

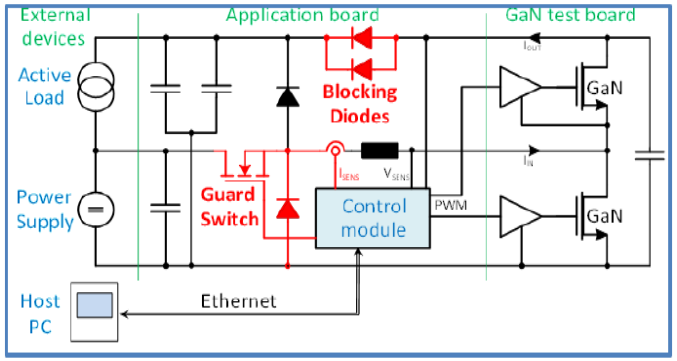
600 V – 650V GaN FETs

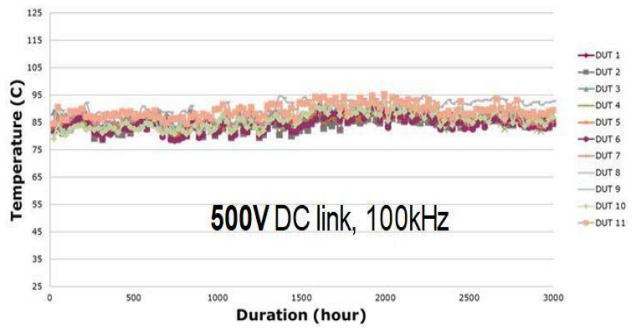


D. Gandhi (Navitas), "*Systematic Approach to GaN Power IC Reliability*", APEC PSMA Industry session IS11, 2019

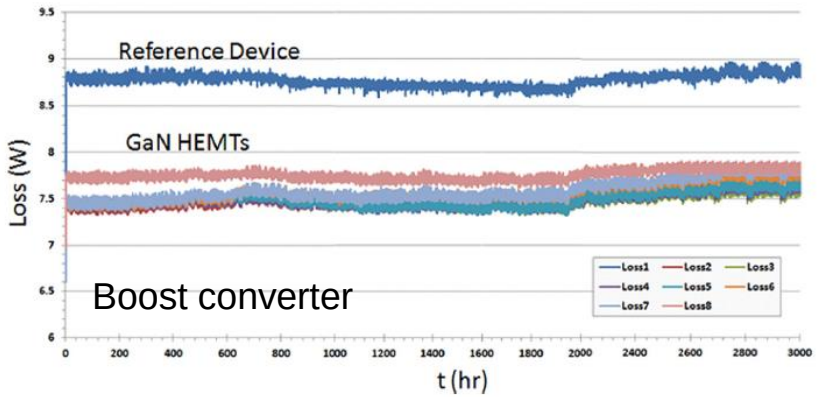


A. Ikoshi et al. (Panasonic), "*DHTOL Life Tests for GaN Hybrid-Drain GITs*", APEC Industry Session IS16-02, 2018





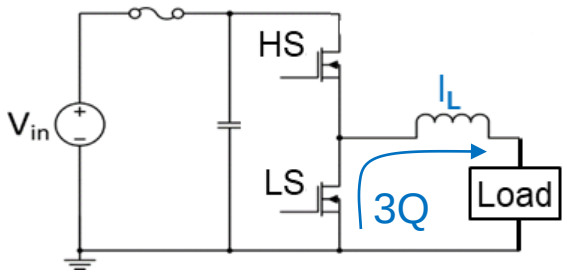
T. McDonald, "*Reliability and qualification of CoolGaN*", Infineon whitepaper



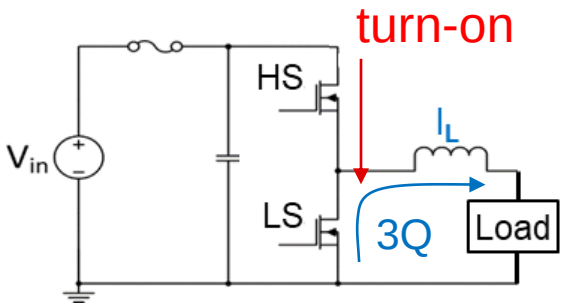
K. Smith, et al., (Transphorm) "*Lifetime tests of 600-V GaN-on-Si power switches and HEMTs*", Microelectronics Reliability, p.197, 2016

TI DHTOL summary: following slides

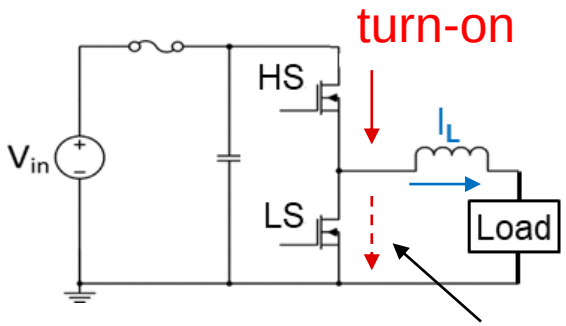
Power-supply level stresses



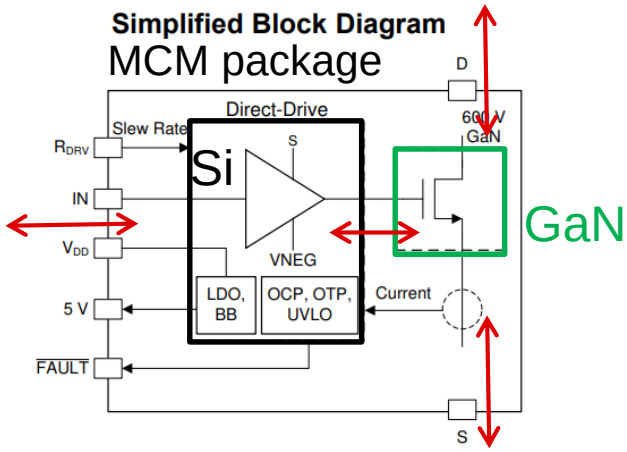
Third quadrant



Hard-commutation (reverse recovery)

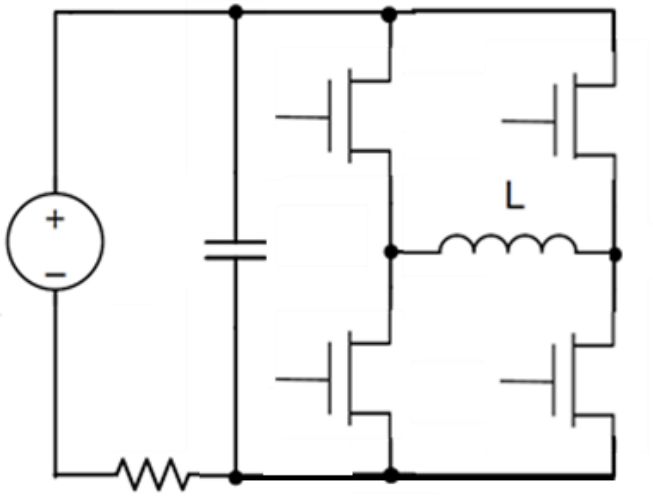


Miller turn-on shoot-through



GaN device interaction with driver (and other system components)

Reliable power-supply operation: DHTOL testing



Loss current sensing

<u>H-bridge circuit</u>

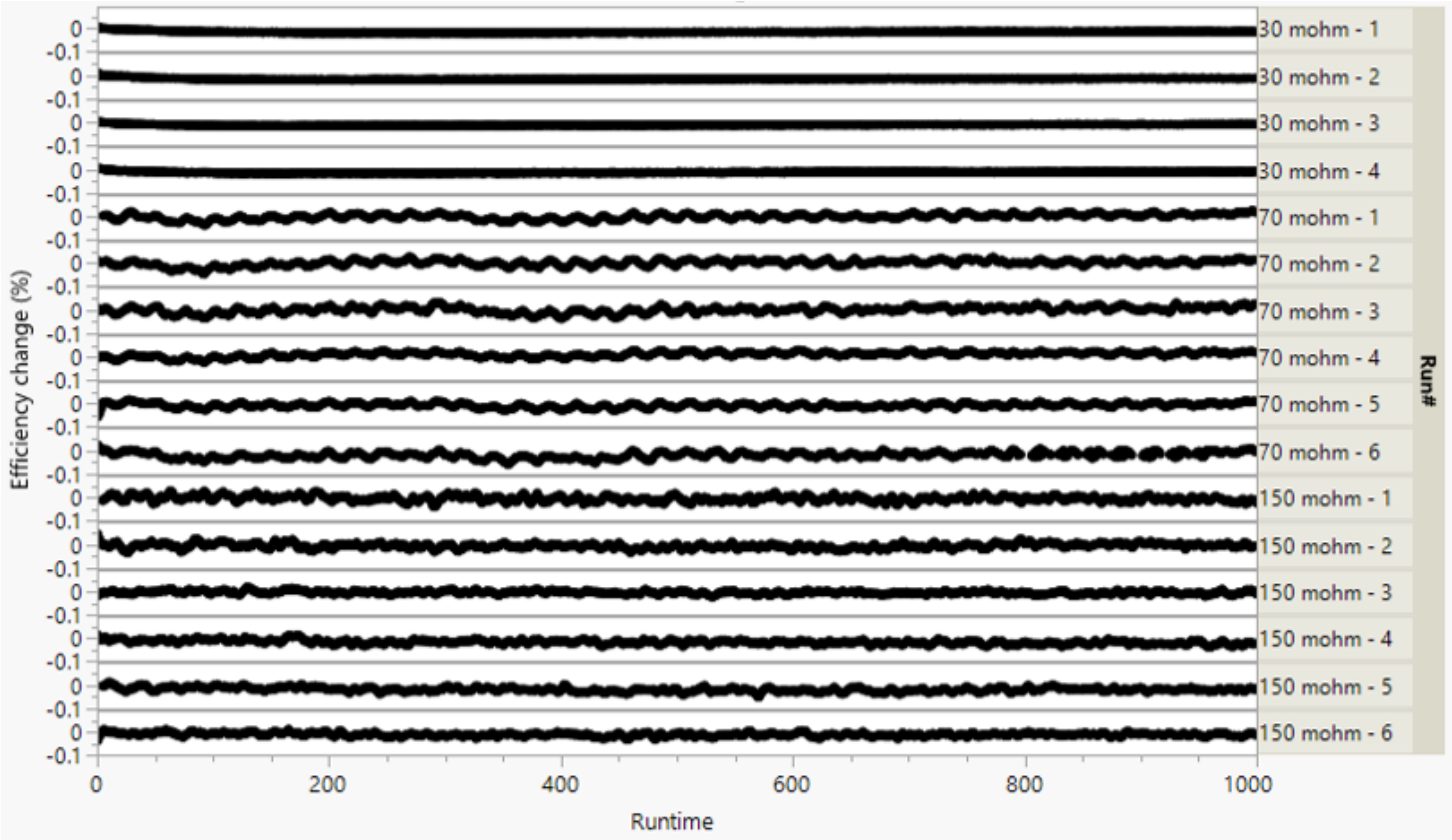
- Recycle power
- Both hard and soft-switching stress at high power
- Power supply stress modes

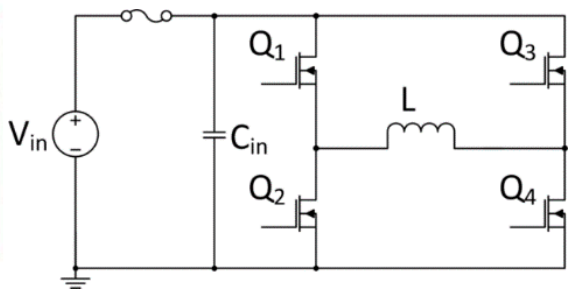
Application half-bridge boards under stress

Stress rack

Validating in-system reliability (DHTOL, JEP180)

LMG34xx TI GaN half-bridges run at 480V/125C, 150 kHz, 100 V/ns slew rate and maximum-power hard-switching stress conditions for 1000h.





Rds-on (mohm)	Power (kW)	no. of half-bridges	no. of parts
30	3.8	8	16
50	1.9	12	24
150	1.4	12	24

64 parts ran from multiple lots of the LMG34xx product family

*Reliable in-system operation for **both hard and soft switching**: stable running with efficiency within 0.1%*

Reliable operation under all conditions

During operation, abnormal or extreme conditions can occur

- A line surge can occur from an event like a lightning strike
  - The power FET needs to be surge robust
- The load can short circuit
  - Overcurrent protection would turn the FET off in a latched or cycle-by-cycle manner
- The supply voltage may dip
  - If the supply voltages go below a threshold, UVLO protection would pause power FET switching until the voltage recovers.
- The die temperature may get too high, such as if there is a cooling issue
  - If the die temperature exceeds the threshold, overtemperature protection turns the power FET off and notifies the system.

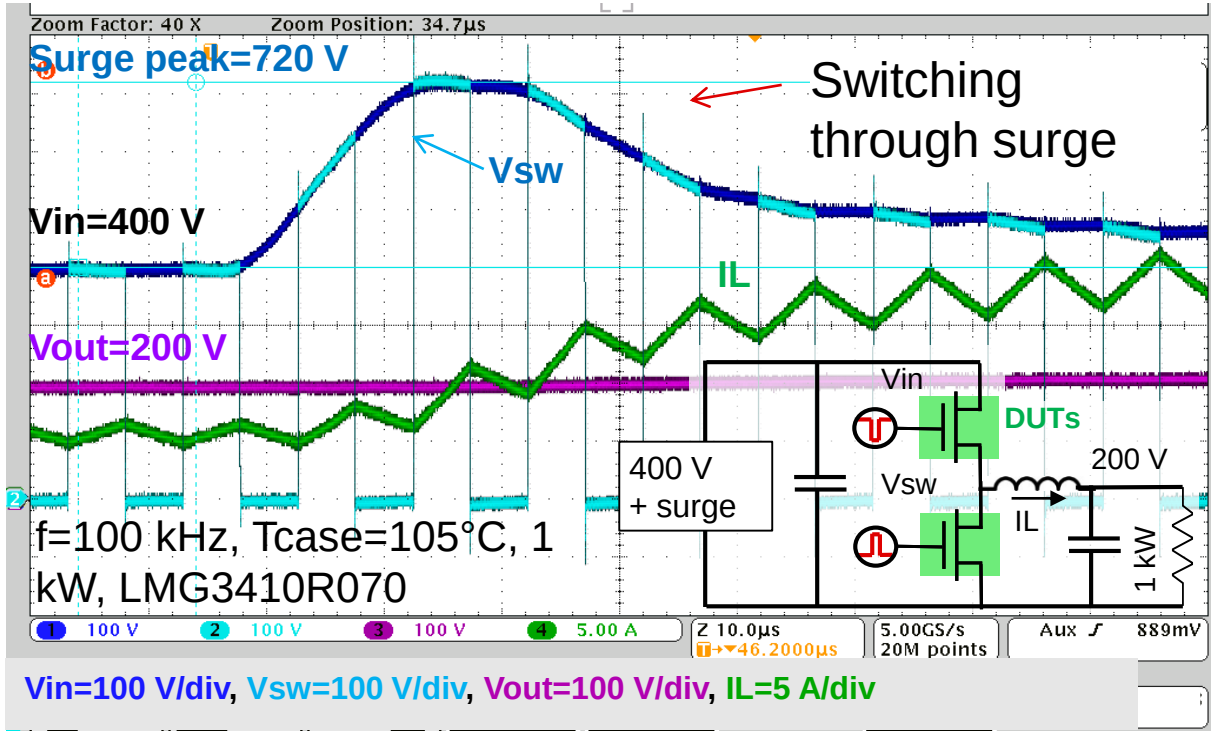
Surge robustness: No avalanche? No problem!

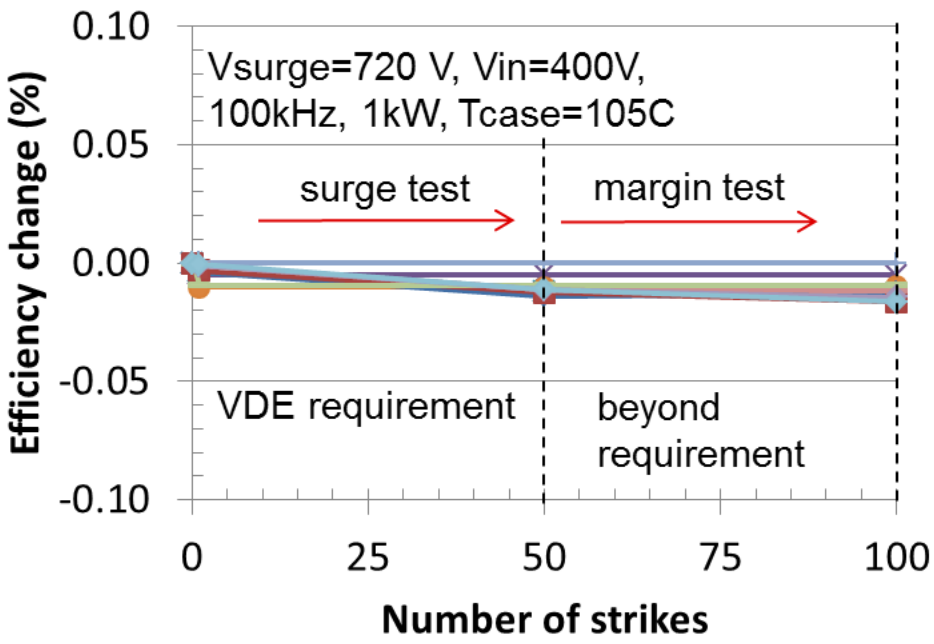
- Power line disturbances can occur due to lightning strikes, malfunction, load and capacitor bank switching, etc.
- Silicon devices use their avalanche rating property to survive these events.
- The use of avalanche is historical. It arises because silicon FETs do not have much voltage headroom above their maximum voltage rating. When a surge strikes, they break down (by impact-ionization).
- GaN has good transient overvoltage capability. This allows GaN FETs to switch through surge *without avalanche breakdown* and disruption. It also improves system reliability, since MOV degradation can cause failure of Si FETs by subjecting them to higher levels of avalanche.

"*No avalanche? No problem! GaN FETs are surge robust*", available at https://e2e.ti.com/blogs_/b/powerhouse/posts/no-avalanche-no-problem-gan-fets-are-surge-robust

TI GaN: Robust to surge

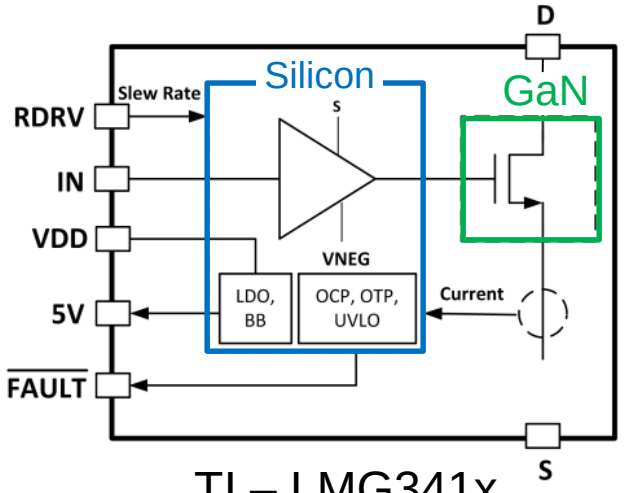
- The IEC 61000-4-5 standard specifies the surge waveform
- The VDE 0884-11 standard specifies the application of 50 strikes
- We applied additional 50 strikes to assure margin
- Parts had very stable efficiency and there was no hard failure



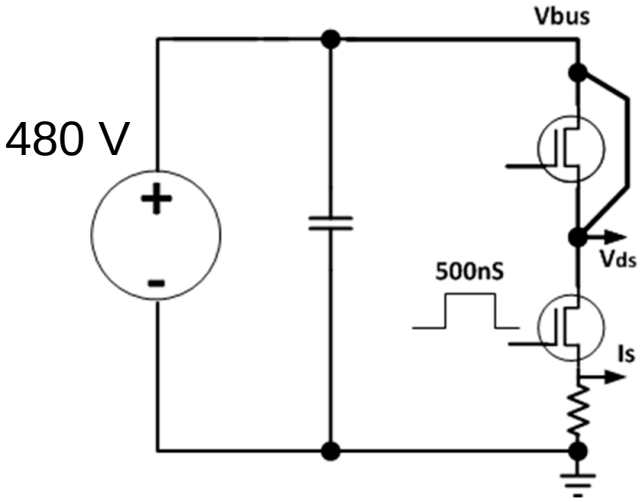


"A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use-conditions",IEEE IRPS 2019, available at www.ti.com/lit/ml/slyy162/slyy162.pdf

Short circuit detection and protection

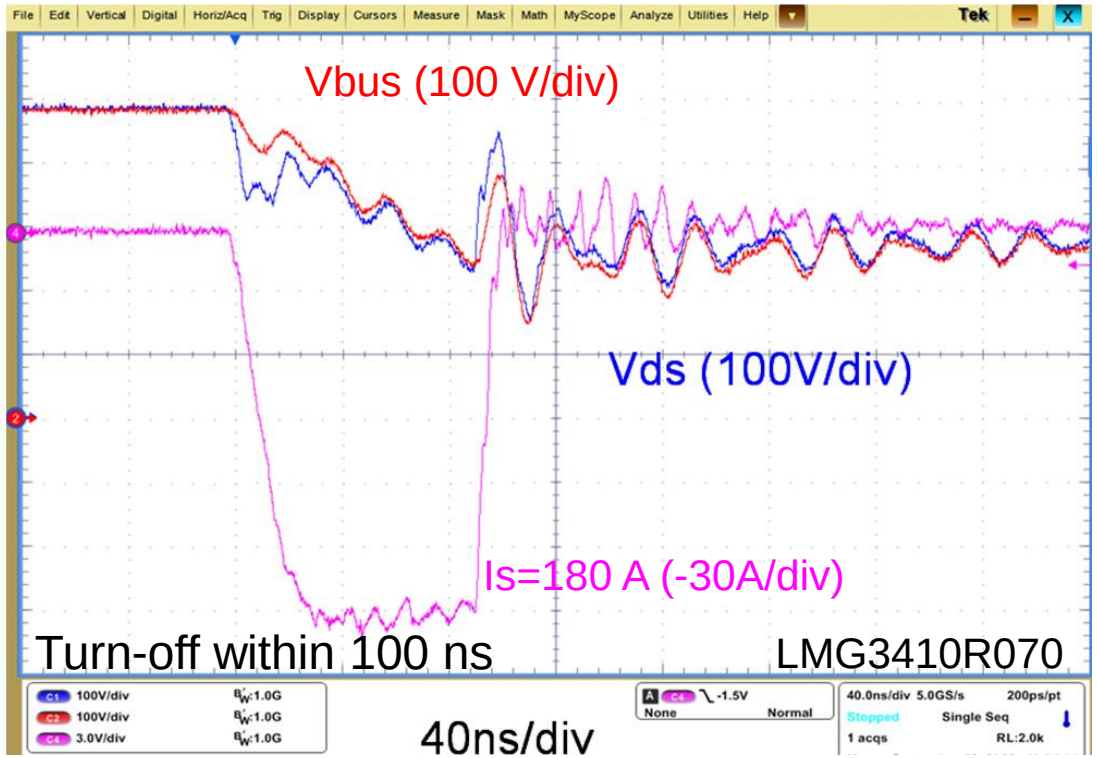


TI – LMG341x



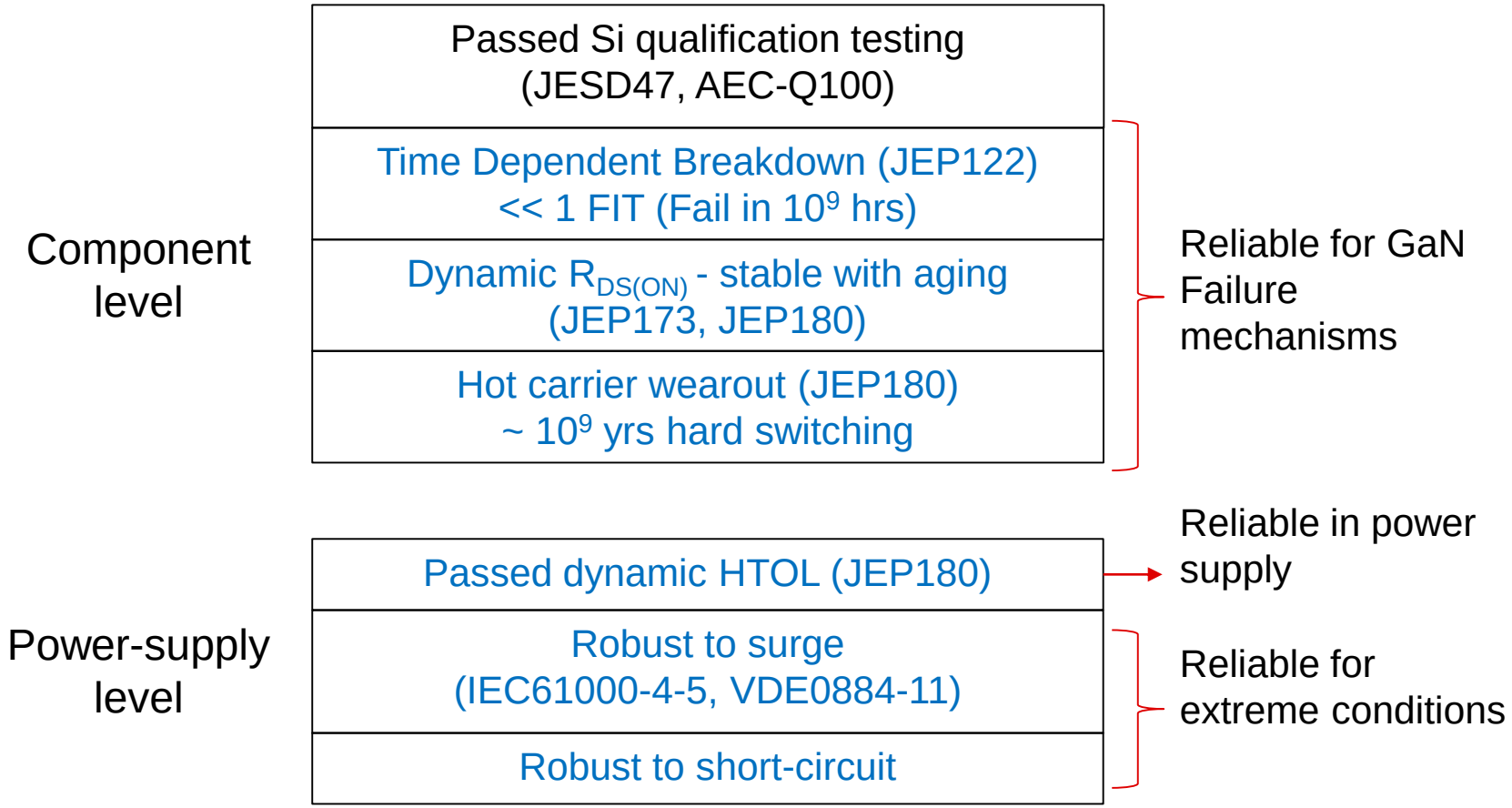
Hard short-circuit test

- Integration of GaN power FET in a low-inductance package with a Si driver and protection allows fast detection and turn-off (1).
- Built-in protection eliminates delay needed for external components (2).



(1) "*Overcurrent Protection in High-Density GaN Power Designs*", TI Application Report, www.ti.com/lit/an/snoaa15/snoaa15.pdf
(2) External gate drivers are also much faster now, e.g. TI UCC21750 can respond within 0.5 µs

Reliability outcome for TI GaN parts



Conclusion

- GaN power FETs are now reliable and the customer conversation is moving from "*Is GaN reliable?*" to *"What are the steps to validate GaN reliability?"*
- GaN reliability is validated by GaN specific guidelines developed by the JEDEC JC70 committee.
- The JEDEC JEP 180 guideline assures that GaN power FETs will operate reliably in the intended application. It addresses the gap in the Si methodology itself which does not consider the switching stresses of power supply usage.
- TI GaN FETs are demonstrated reliable for a wide range of power supply applications both for normal and extreme operating conditions
- Calculations are presented for mission profiles of datacenter, server and telecommunication power supply applications, showing excellent reliability.