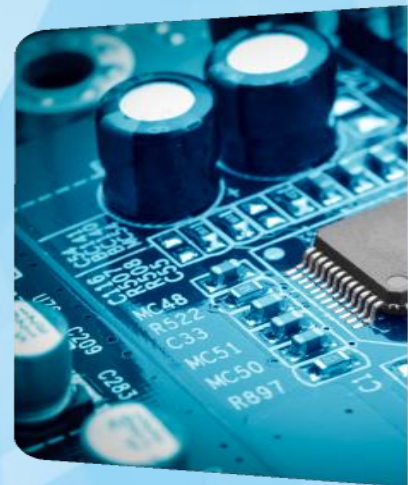


**Co-Packaged Optics:
Heterogeneous Integration of Chipllets in
Switch, Photonic IC, and Electronic IC
(IEEE Santa Clara Valley EPS Chapter Distinguish Lecture)**

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Co-Packaged Optics (CPO)

Co-packaged optics (CPO) are heterogeneous integration packaging methods to integrate chiplets:

- Photonic IC (PIC) such as Photodiode, laser, etc.
- Electronic IC (EIC) such as transimpedance Amplifier (TIA), laser driver, etc.
- Application-specific IC (ASIC) Switch

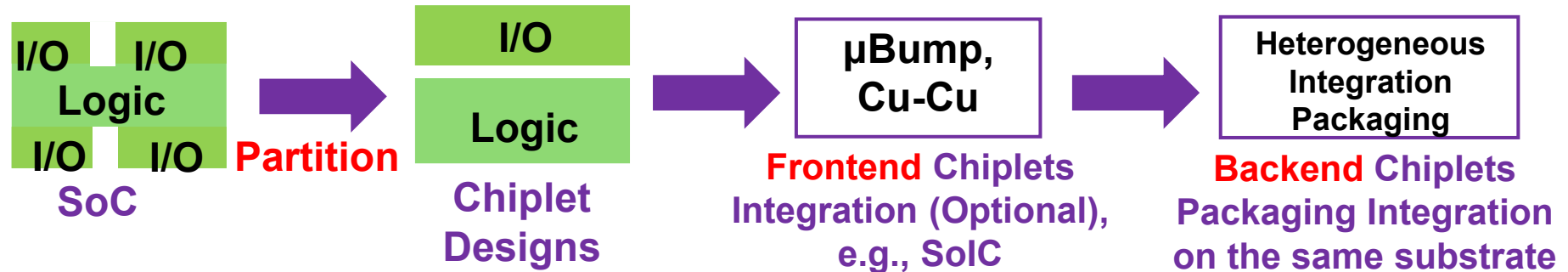
The advantages of CPO are:

- Reducing the length of the electrical interface between the PIC, EIC, and the Switch
- Reducing the energy required to drive the signal (lower power)
- Cutting the latency, which leads to better electrical performance

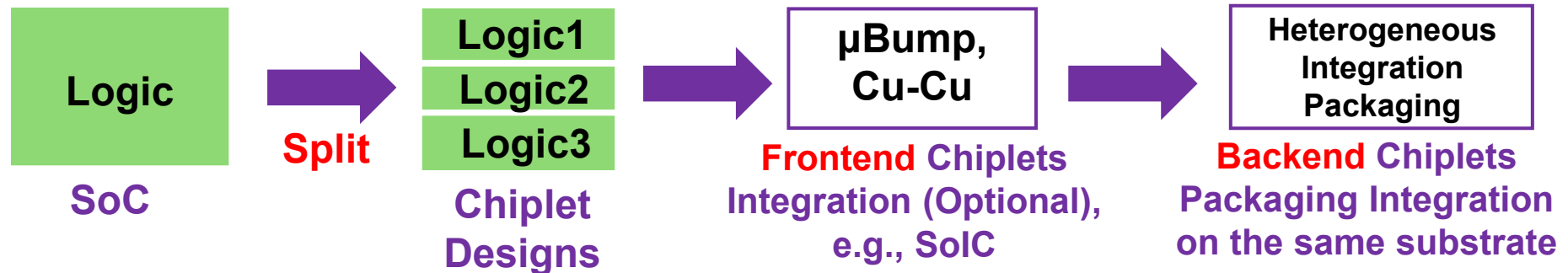
Chiplets and Heterogeneous Integration

Chiplet Design and Heterogeneous Integration Packaging

Chip partition and integration (Driven by cost and technology optimization)

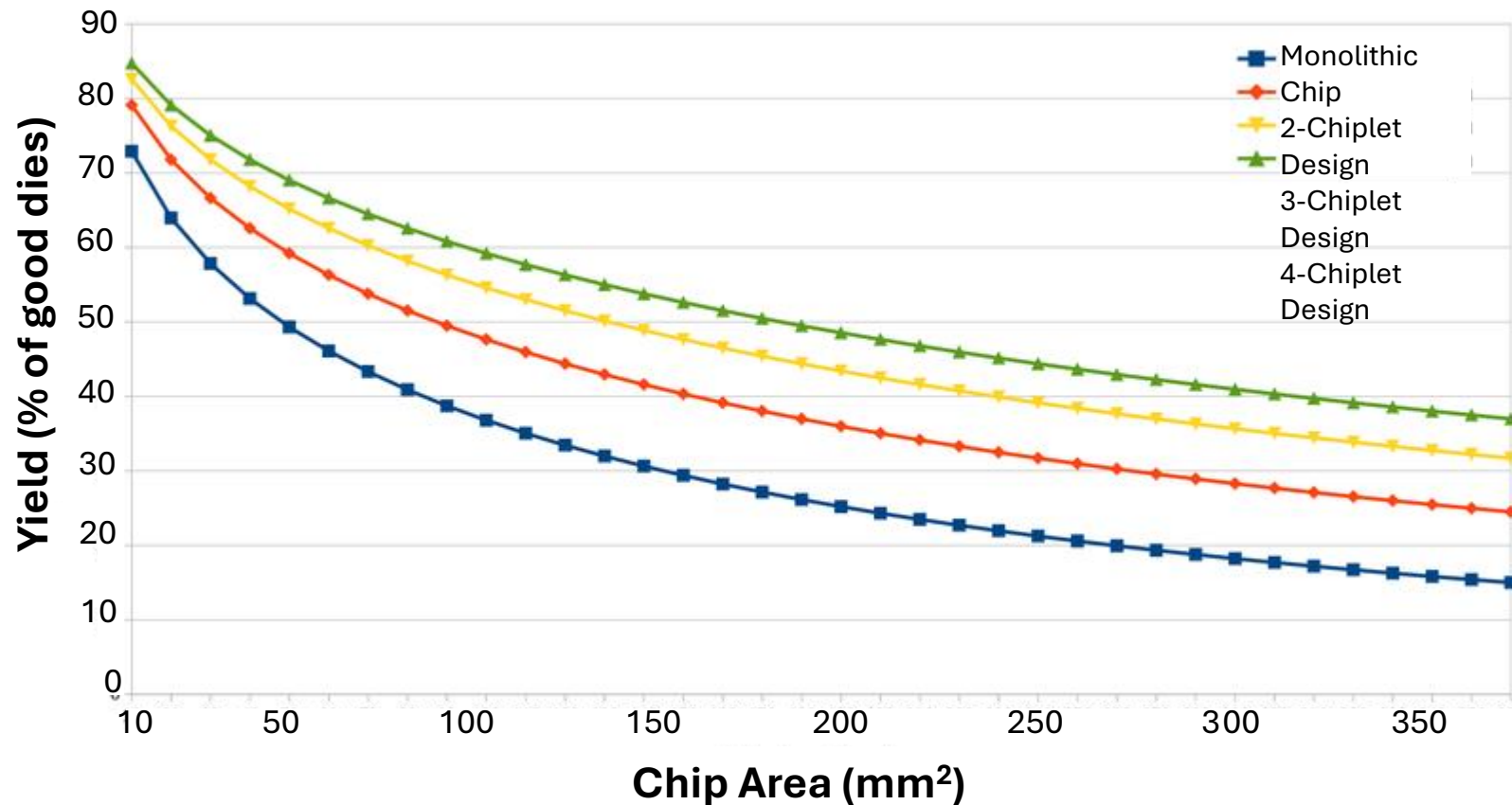


Chip split and integration (Driven by cost and yield)



1. Lau, J. H., and K. Chiang, *Cu-Interconnects, Glass, and AI-Assisted Simulation for Chiplets and Heterogeneous Integration*, Springer, New York, 2026.
2. Lau, J. H., and X. Fan, *Hybrid Bonding, Thermal Management for Chiplets Heterogeneous Integration*, Springer, New York, 2025.
3. Lau, J. H., *Flip Chip, Hybrid Bonding, Fan-In, and Fan-Out Technology*, Springer, New York, 2024.
4. Lau, J. H., *Chiplet Design and Heterogeneous Integration Packaging*, Springer, New York, 2023.
5. Lau, J. H., *Semiconductor Advanced Packaging*, Springer, New York, 2021.
6. Lau, J. H., *Heterogeneous Integrations*, Springer, New York, 2019.

Yield (Cost) per Wafer vs. Chip Size for SoC and Chiplets

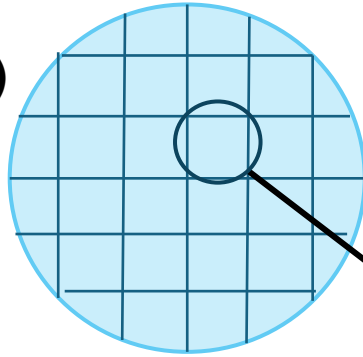


Sources: <https://en.wikichip.org/wiki/chiplet>, March 27, 2020.

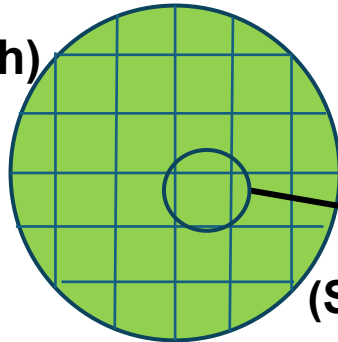
The smaller the chip size, the higher the semiconductor manufacturing yield, which translates into lower cost.

Chiplet Design and Heterogeneous Integration Packaging

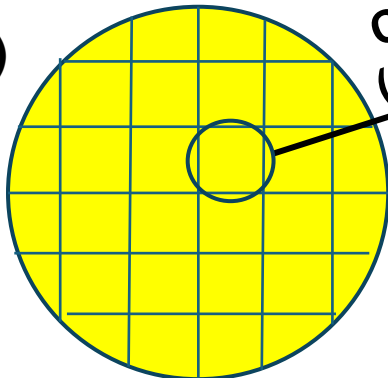
- Chip (CPU)
- FAB-1
- 5nm
- 12"-wafer



- Chip (Switch)
- FAB-2
- 14nm
- 8"-wafer



- Chip (GPU)
- FAB-3
- 7nm
- 12"-wafer

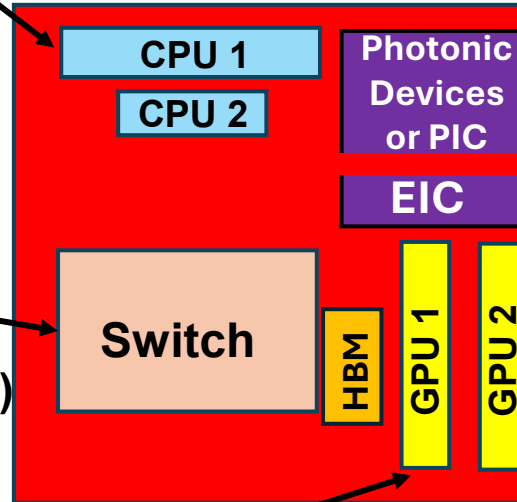


Chip (CPU)

Chip (Switch)

Chip (GPU)

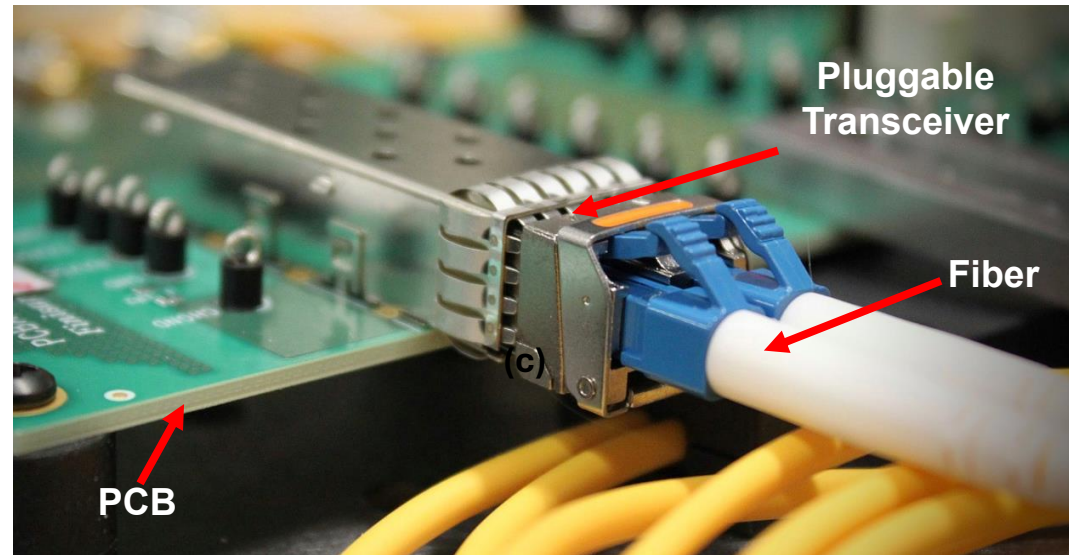
Heterogeneous integration or SiP



Heterogeneous integration uses packaging technology to integrate dissimilar chiplets, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.

Data Centers, TOSA, ROSA, OE, EE, PIC, and EIC

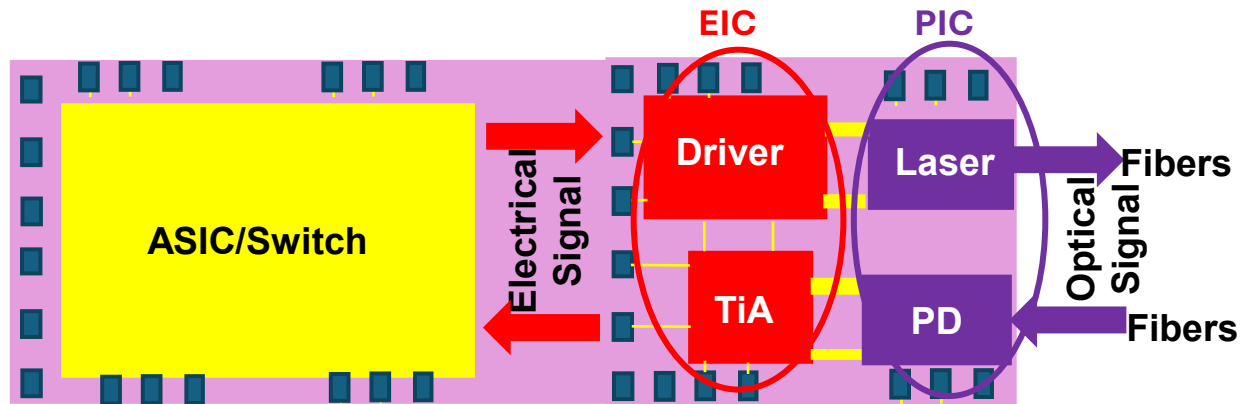
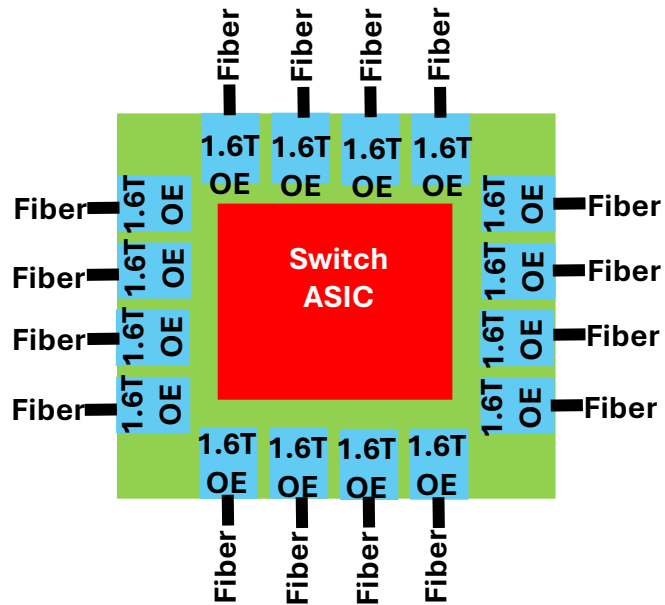
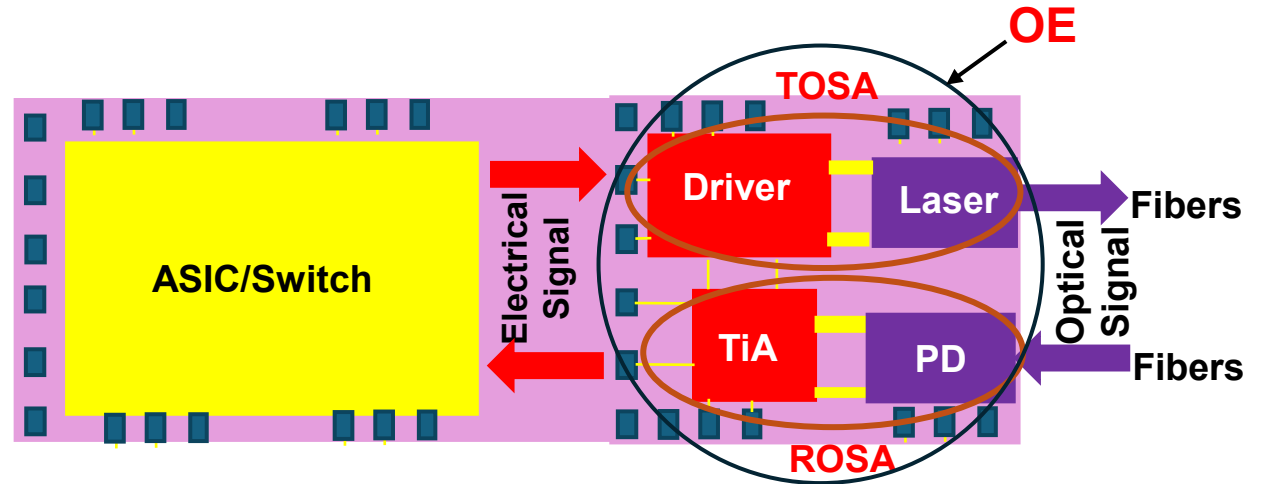
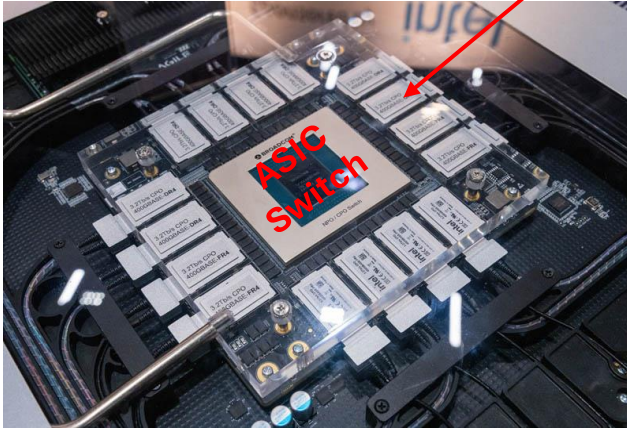
Datacenter with Pluggable Transceiver



Today, more than 90% are pluggable transceivers

Data Center Tomorrow (Co-Packaged Optics)

Optical Engine (OE)



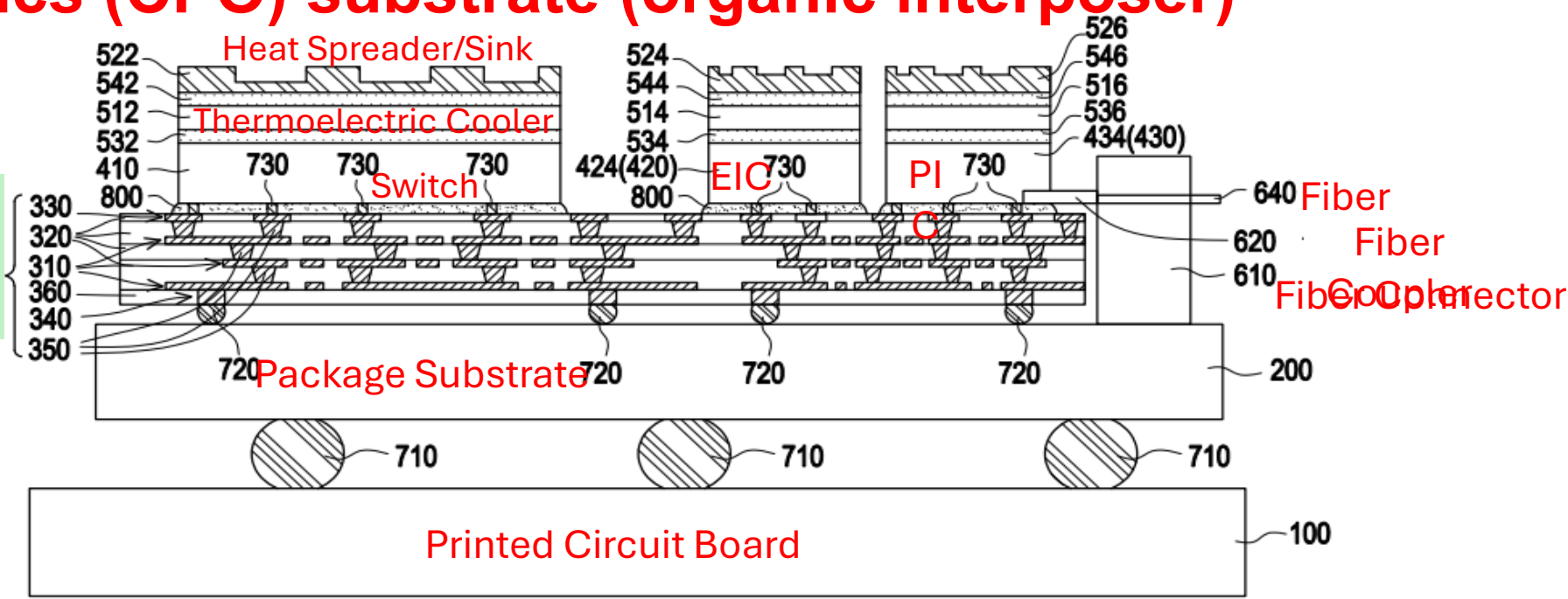
- EICs are complementary metal-oxide semiconductor (CMOS) devices and are used as the PICs controller.
- PICs are usually not CMOS devices and are used to receive and transmit light (photon) and convert it to electrical signal (electron) and vice versa.

OE (Optical Engine); EIC (Electronic IC); PIC (Photonic IC); PD (Photodiode); TIA (transimpedance Amplifier)
TOSA (Transmitting Optical Sub-Assembly); ROSA (Receiver Optical Sub-Assembly);

2D heterogeneous integration of ASIC, EIC and PIC on a co-packaged optics (CPO) substrate (organic interposer)

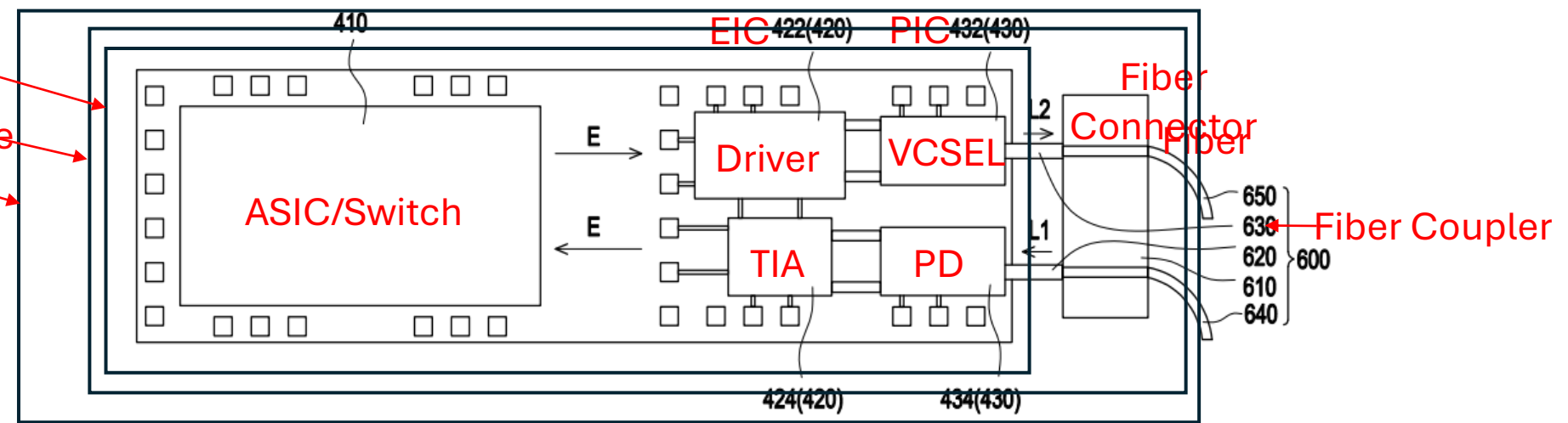
Co-Packaged Optics (CPO)-substrate (Organic Interposer)

Cross-section View



Organic Interposer
Package Substrate
Printed Circuit Board

Top View



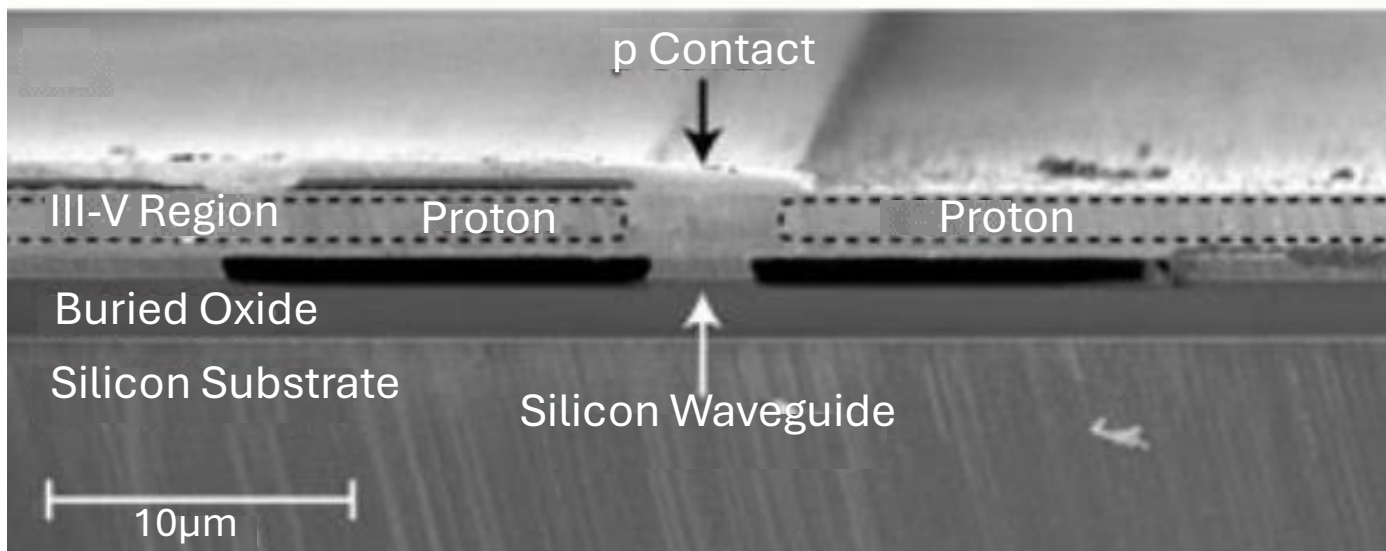
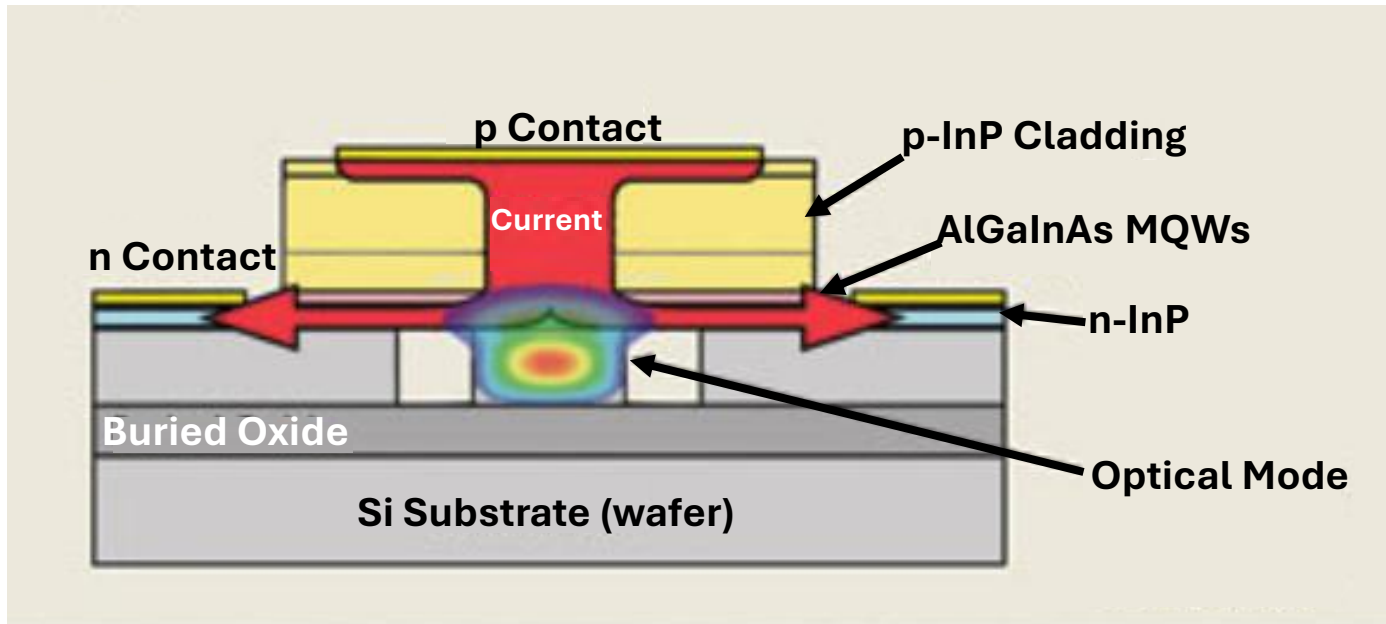
Photonic Devices and Silicon Photonics

Photonic Devices are components that generate, manipulate, and detect light, e.g., : LED (Light Emitting Diode), Lasers, etc..

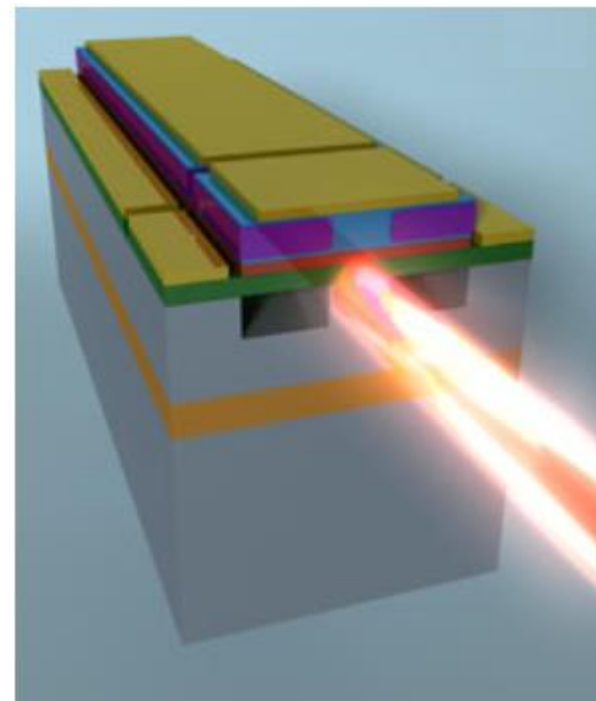
Silicon photonics is a technology that integrates optical components onto a silicon chip, enabling the transmission of data using light instead of traditional electrical signals. Si photonics is the semiconductor integration of PIC and EIC on a silicon substrate (wafer) with **CMOS** (complementary metal-oxide semiconductor) technology.

Twenty years ago, due to **Moore's law**, silicon integration was very popular. Companies like Intel have been promoting the silicon photonics that integrate some of the PICs and EICs on a chip from a silicon wafer with CMOS technology. The **holy grail** of silicon photonics is to integrate all the PICs, and EICs on a chip fabricated from a Si wafer with CMOS technology. Intel's hybrid laser technology is an example.

Intel is the company who is in high volume manufacturing of Silicon Photonic

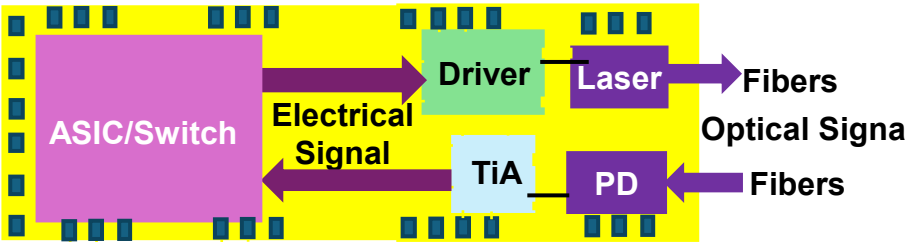
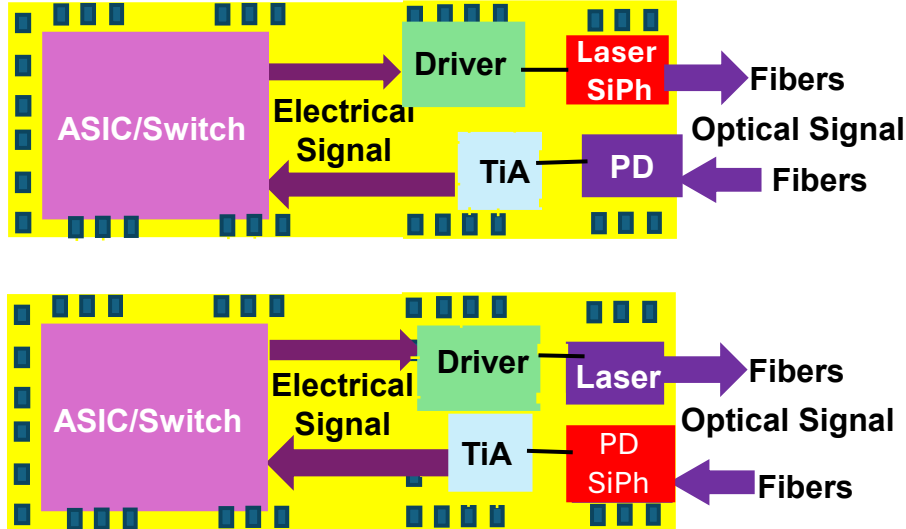
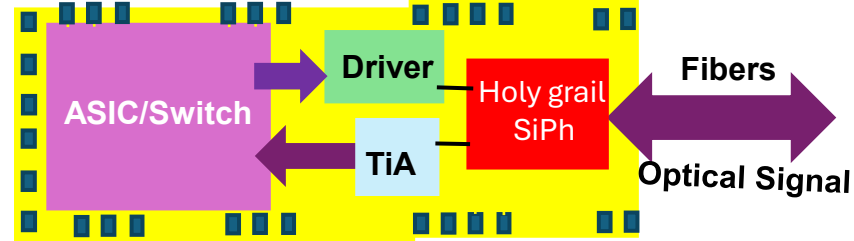


Hybrid laser technology

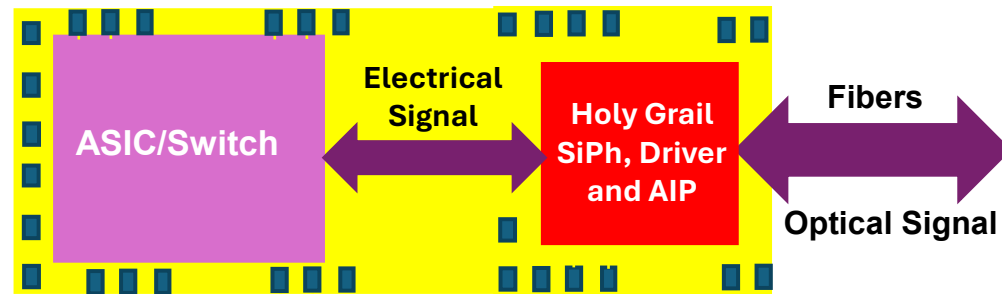
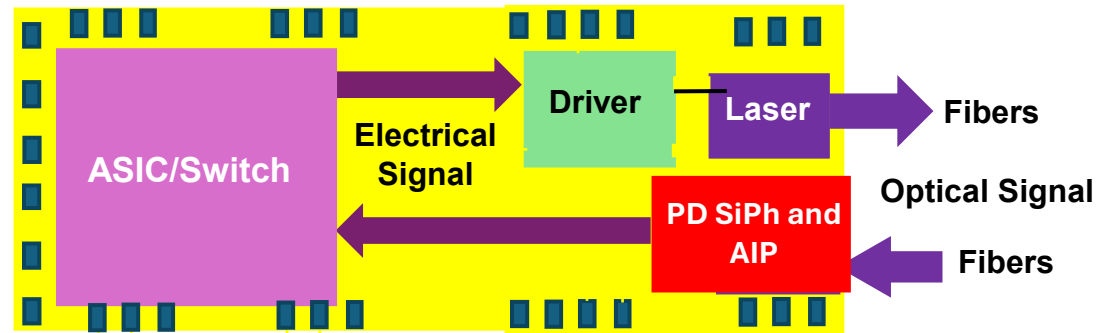
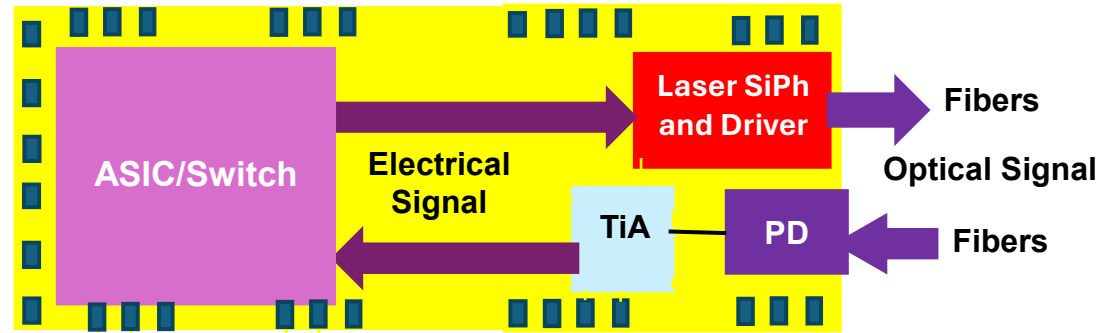


Indium phosphide (InP), the light-emitting material, is bonded to the top of the silicon with a thin layer of glass glue.

Various Forms of CPO

	CPO	Advantages	Disadvantages
<p>CPO with Basic Chiplets (Photonic Devices)</p>		<ul style="list-style-type: none"> ➤ Lowest cost ➤ Most flexible ➤ Good performance 	<ul style="list-style-type: none"> ➤ Largest CPO package size ➤ Most work in test and burn-in
<p>CPO with Advanced Chiplet (Silicon Photonic)</p>		<ul style="list-style-type: none"> ➤ Better performance ➤ Easier to test and burn-in ➤ Smaller CPO package size 	<ul style="list-style-type: none"> ➤ Higher cost ➤ More rigid infrastructure ➤ More work in testing and burn-in
<p>CPO with Holy Grail Silicon Photonic Chiplet</p>		<ul style="list-style-type: none"> ➤ Best performance ➤ Very easy to test and burn-in ➤ Smallest COP package size 	<ul style="list-style-type: none"> ➤ Highest cost ➤ Most rigid infrastructure

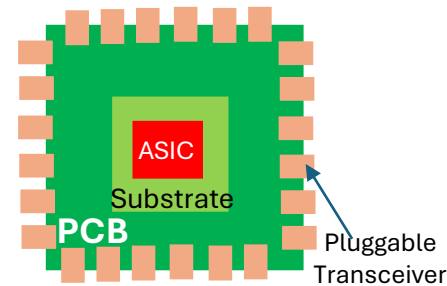
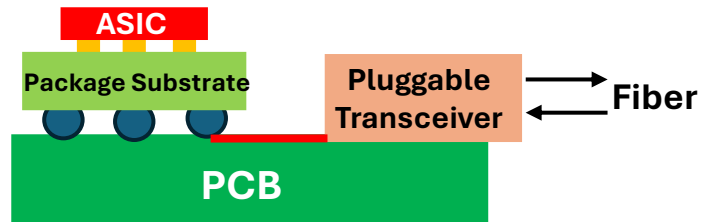
Silicon Integration of EIC and PIC for CPO



**Pluggable Optics,
OBO (on-board optics),
NPO (near-board optics),
CPO (co-packaged optics)**

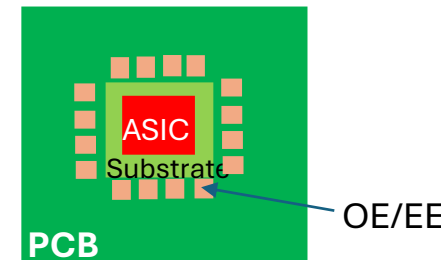
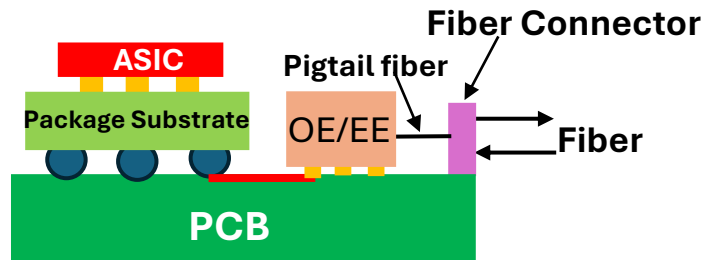
Pluggable Optics, OBO, NPO, and CPO

Pluggable Optics



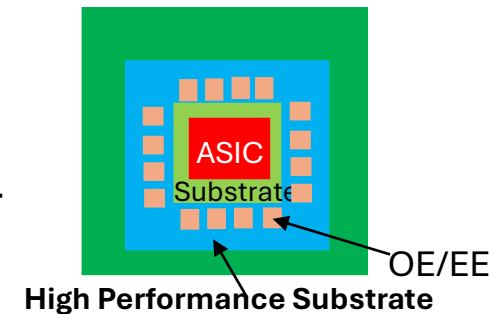
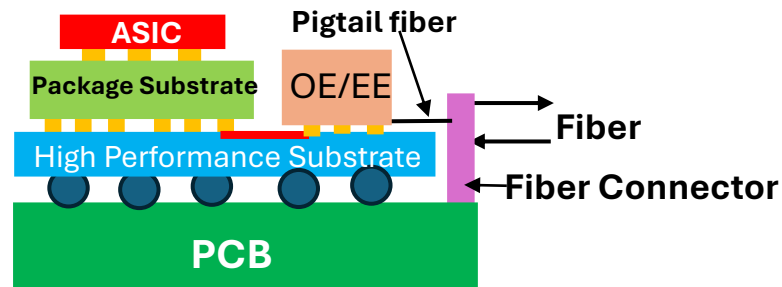
The distance from the pluggable transceivers to the ASIC switch is the farthest and thus the power consumption and electrical performance are the worst.

On-Board Optics (OBO)



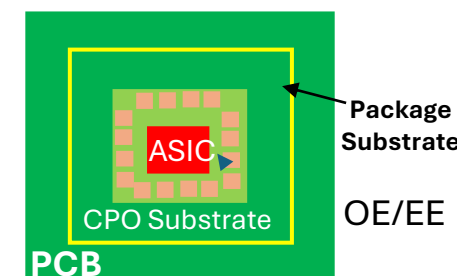
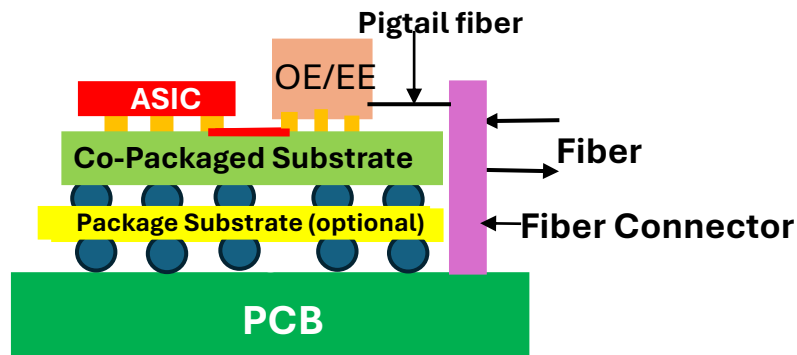
OE/EE (PIC/EIC) are mounted around the ASIC switch package, which is an improvement in power and electrical performance. However, the signals are still traveling on the PCB.

Near-Package Optics (NPO)



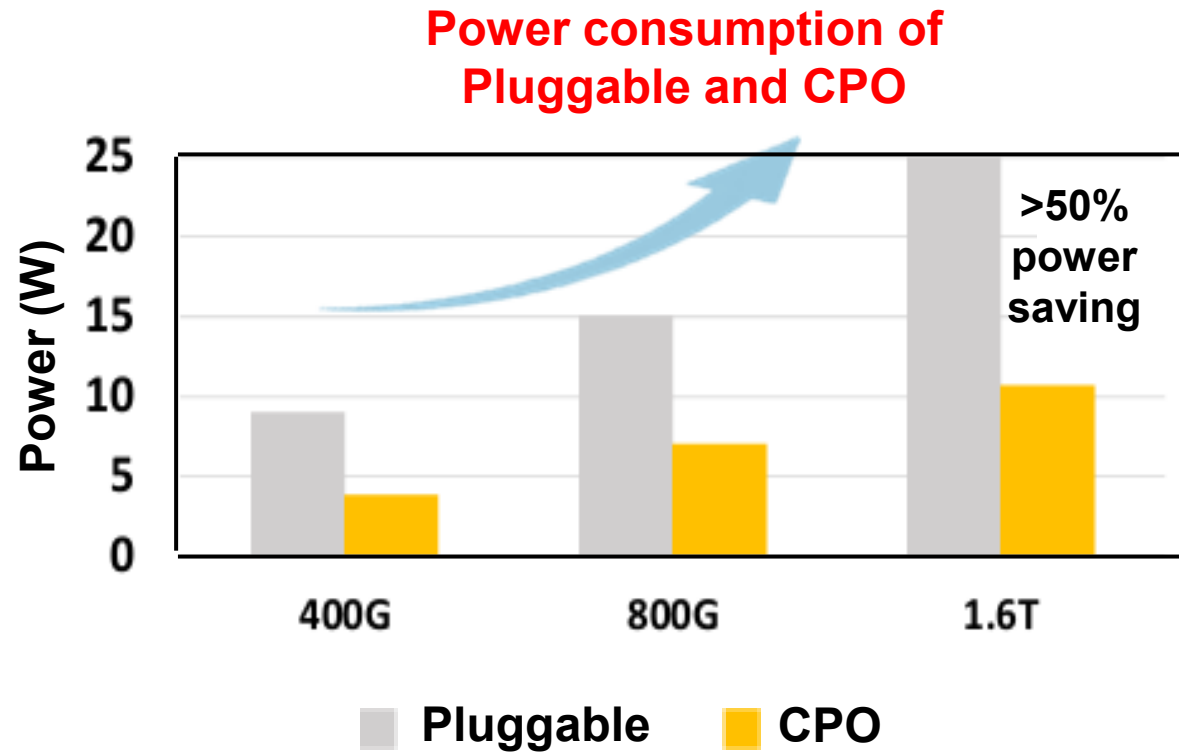
For better power and electrical performance, a high-performance substrate is used to support the ASIC switch package and the OE/EE. (No high-speed data bandwidth going through the PCB.)

Co-Packaged Optics (CPO)



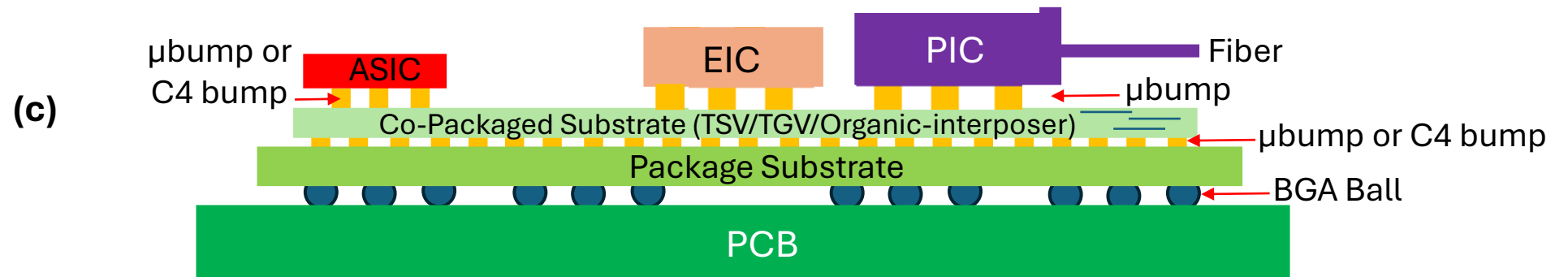
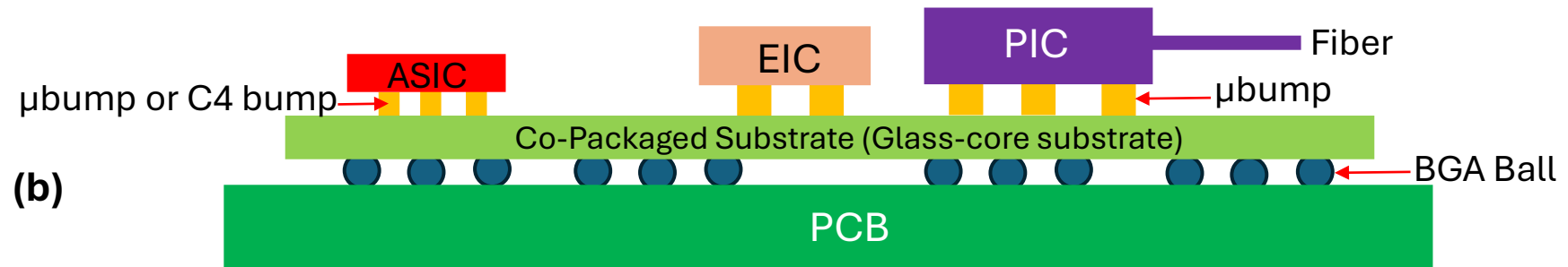
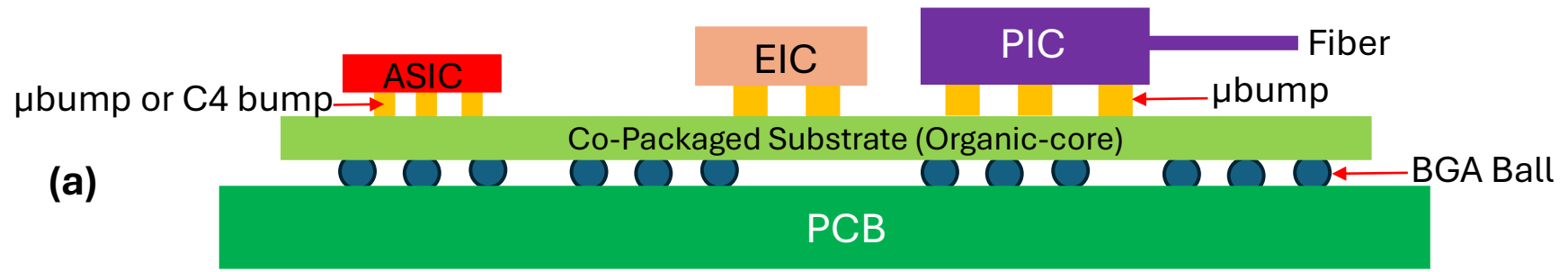
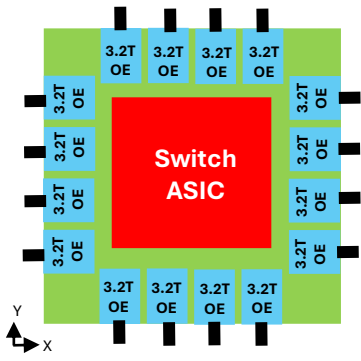
For the best electrical and power performance, a high-performance substrate (CPO substrate) is used to support the ASIC switch device and the OE/EE. The package substrate is optional.

Power consumption: Pluggable vs. CPO

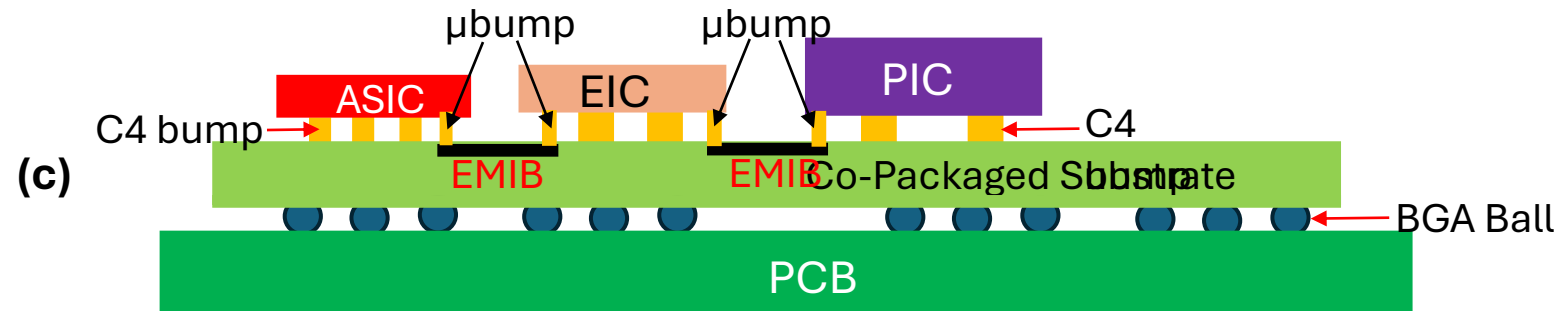
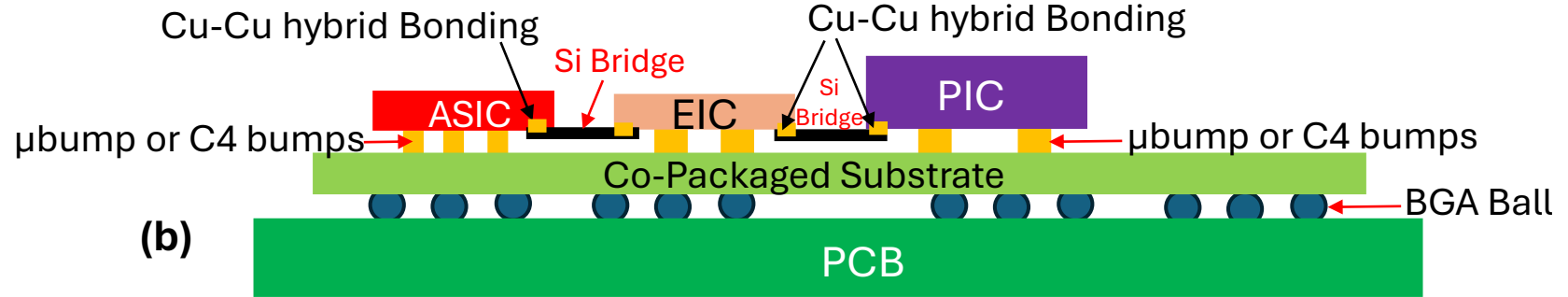
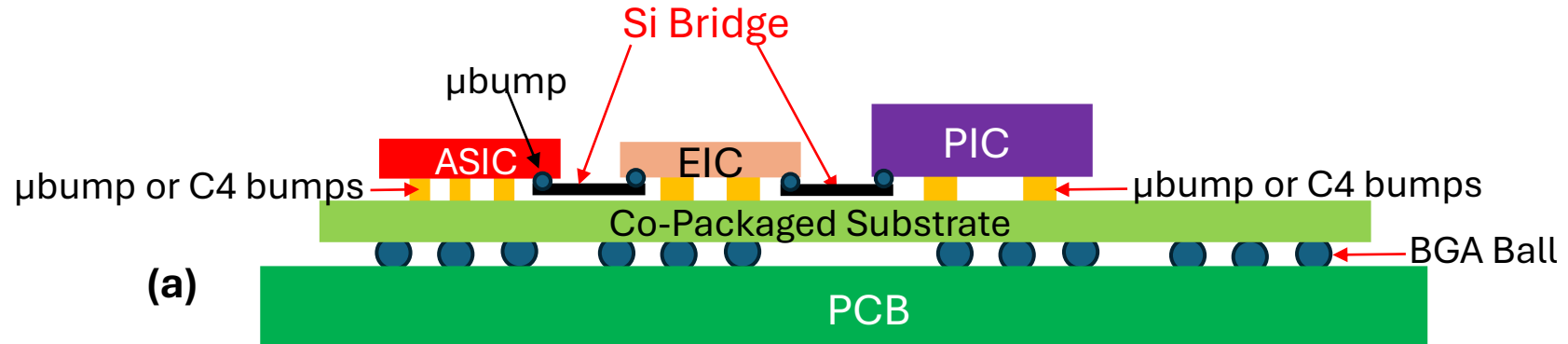
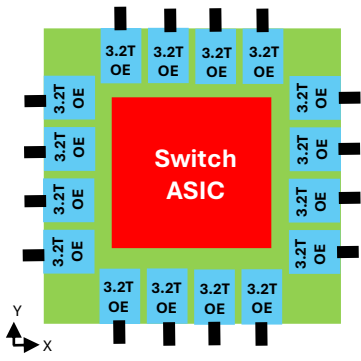


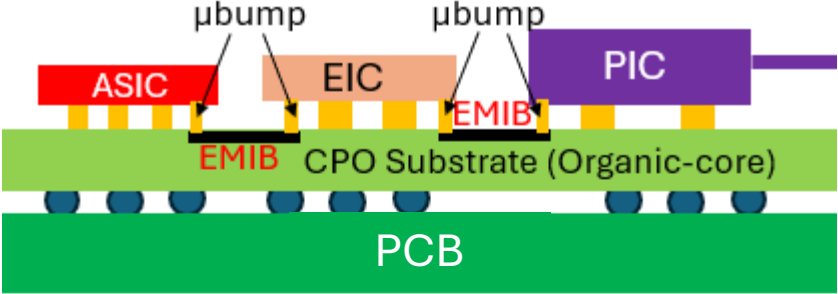
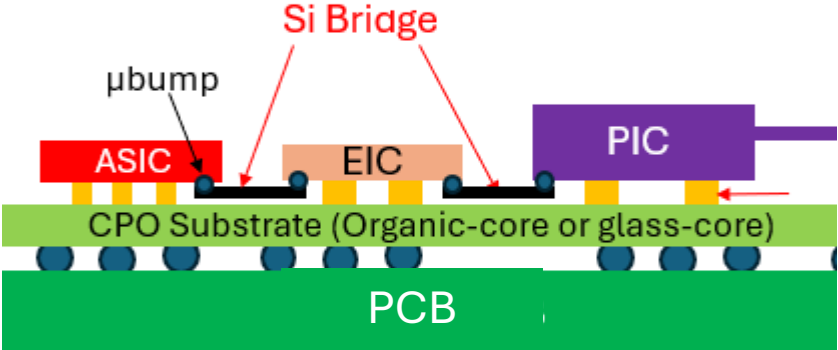
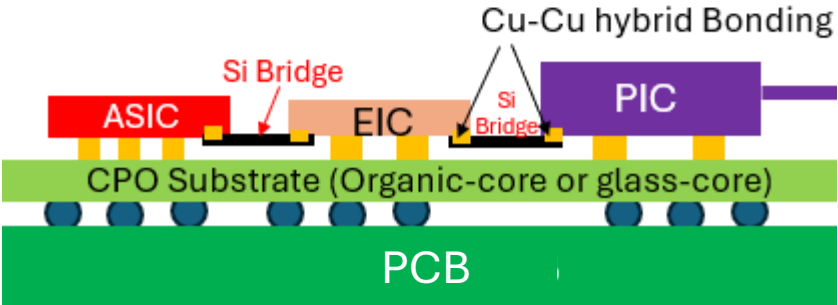
J. E. Johnson, K. Bacher, R. Schaevitz, V. Raghunathan, "Performance and Reliability of Advanced CW Lasers for Silicon Photonics Applications", 2022 Optical Fiber Communications Conference and Exhibition (OFC), Tu2D.1, 2022.

2D heterogeneous integration of ASIC, EIC and PIC

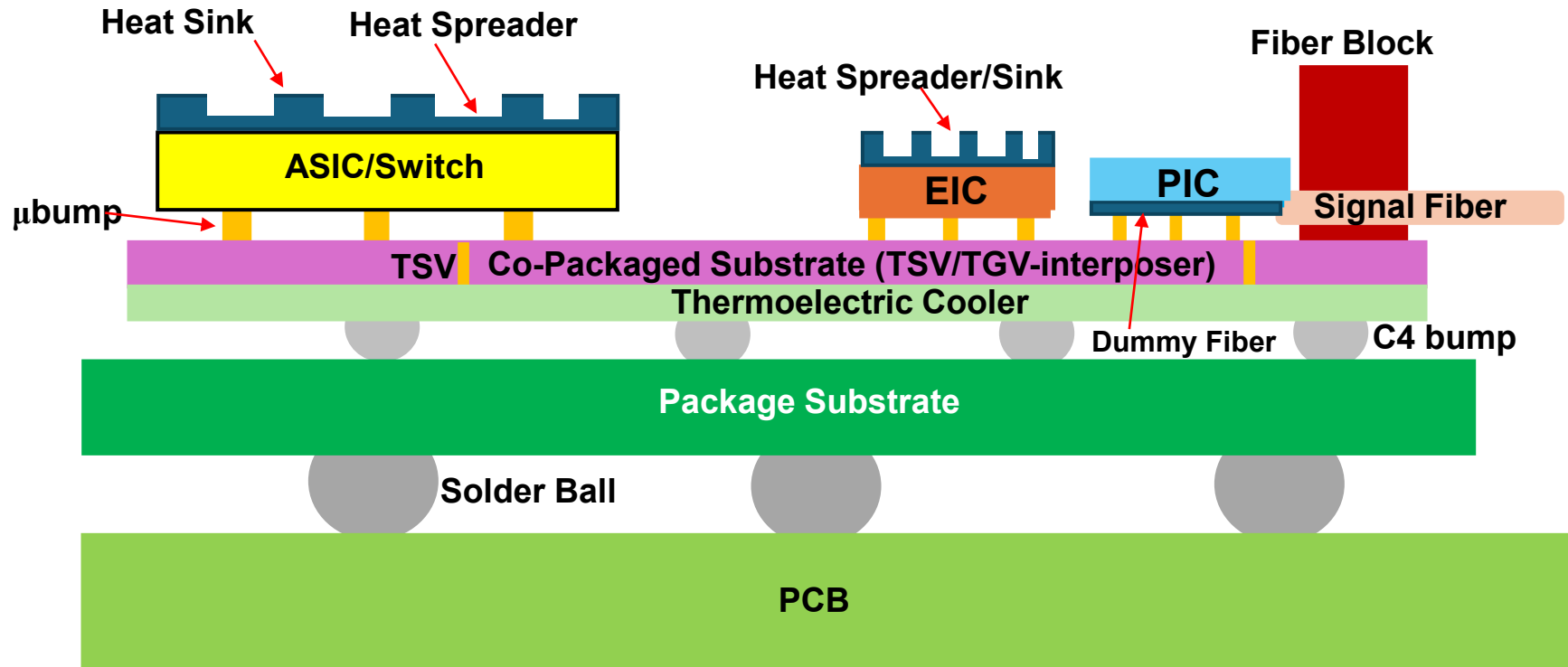
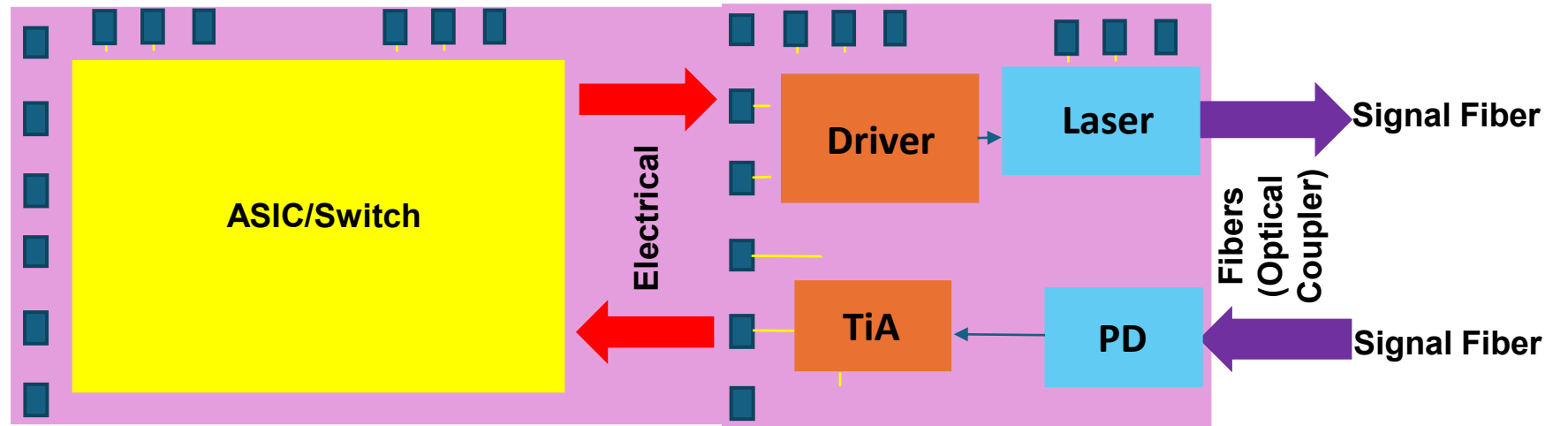
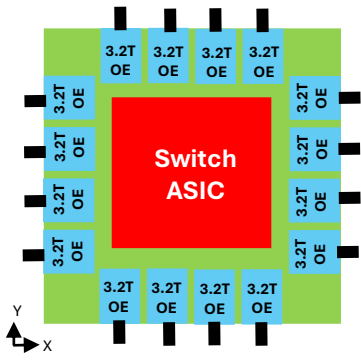


2D heterogeneous integration of ASIC, EIC and PIC with silicon bridges on a co-packaged substrate



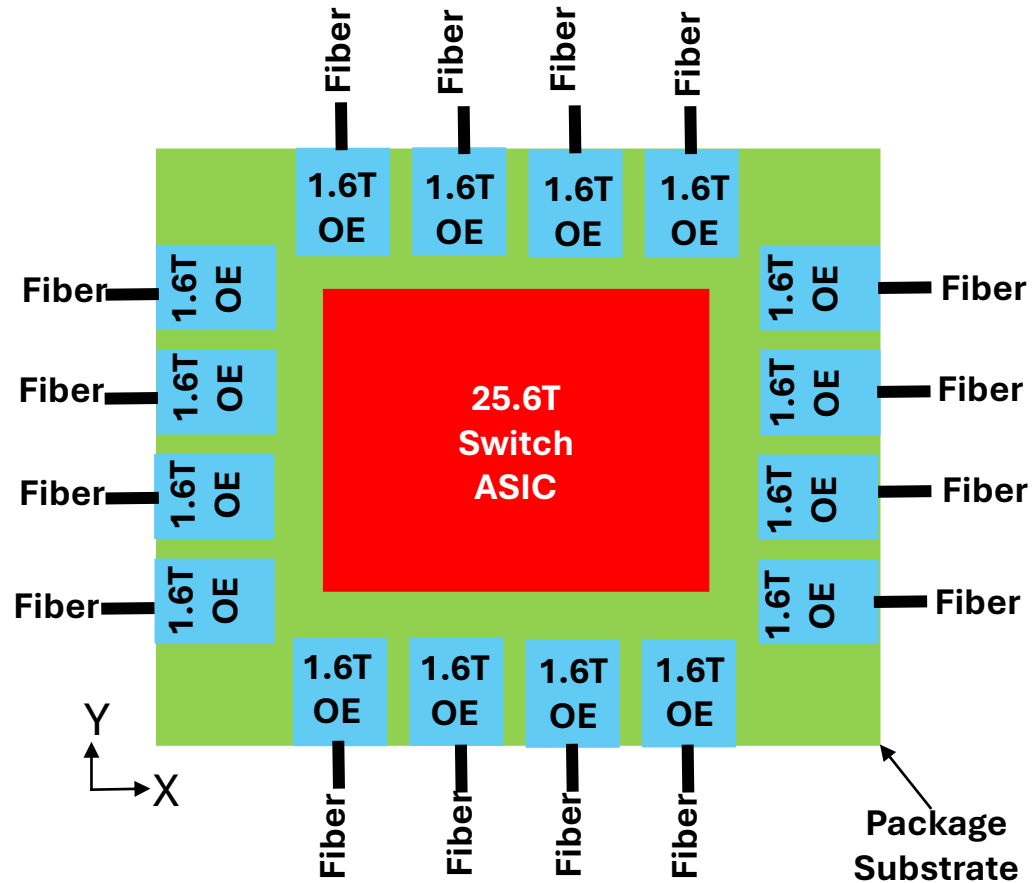
CPO Structures	Advantages	Disadvantages
 <p>μbump</p> <p>ASIC</p> <p>EIC</p> <p>PIC</p> <p>EMIB</p> <p>CPO Substrate (Organic-core)</p> <p>PCB</p>	<ul style="list-style-type: none"> ➤ High performance ➤ Fine pitch ➤ High density 	<ul style="list-style-type: none"> ➤ Higher cost ➤ EMIB involves complicated CPO substrate fabrication
 <p>μbump</p> <p>ASIC</p> <p>EIC</p> <p>PIC</p> <p>Si Bridge</p> <p>CPO Substrate (Organic-core or glass-core)</p> <p>PCB</p>	<ul style="list-style-type: none"> ➤ Higher performance ➤ Finer pitch ➤ Higher density ➤ Simple CPO substrate 	<ul style="list-style-type: none"> ➤ High cost
 <p>μbump</p> <p>ASIC</p> <p>EIC</p> <p>PIC</p> <p>Si Bridge</p> <p>Cu-Cu hybrid Bonding</p> <p>CPO Substrate (Organic-core or glass-core)</p> <p>PCB</p>	<ul style="list-style-type: none"> ➤ Highest performance ➤ Finest pitch ➤ Highest density ➤ Simple CPO substrate 	<ul style="list-style-type: none"> ➤ Highest cost ➤ Hybrid bonding involves complicated chip bonding processes

2.5D heterogeneous integration of EIC and PIC (side-by-side)

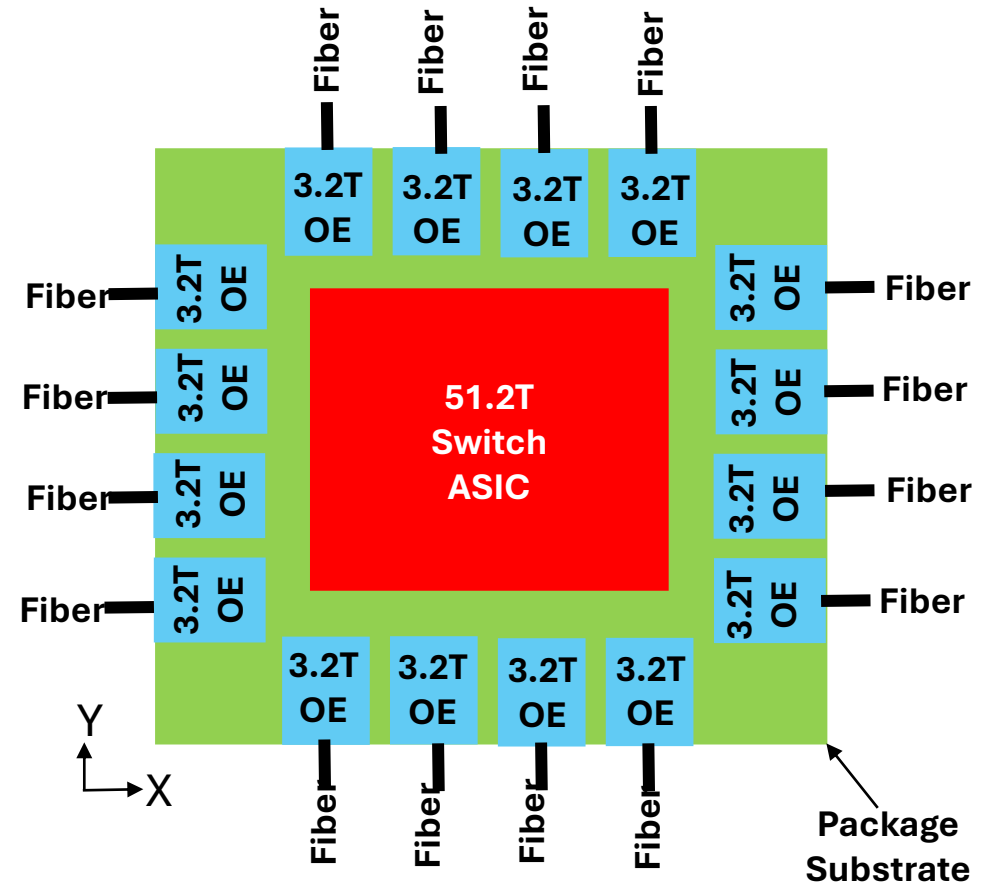


3D Heterogeneous Integration of ASIC Switch, PIC and EIC

Co-Packaged Optics (CPO)



Present

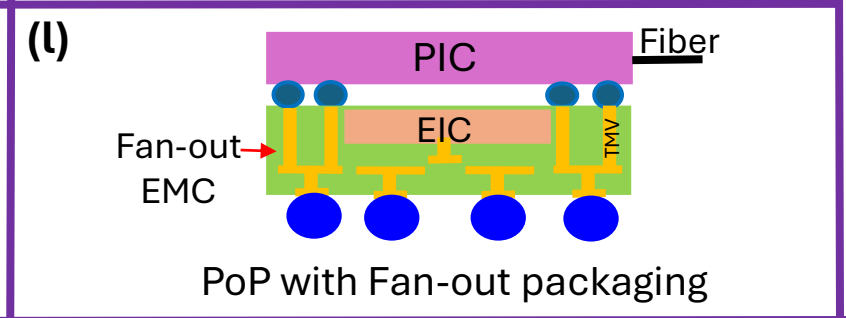
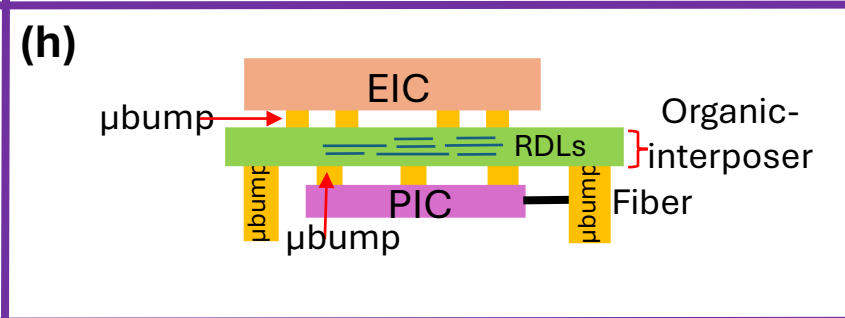
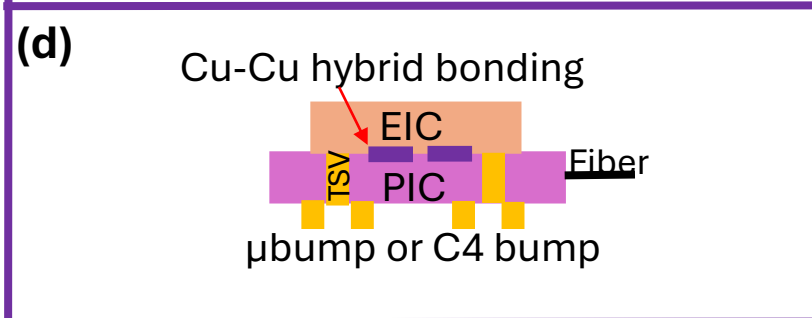
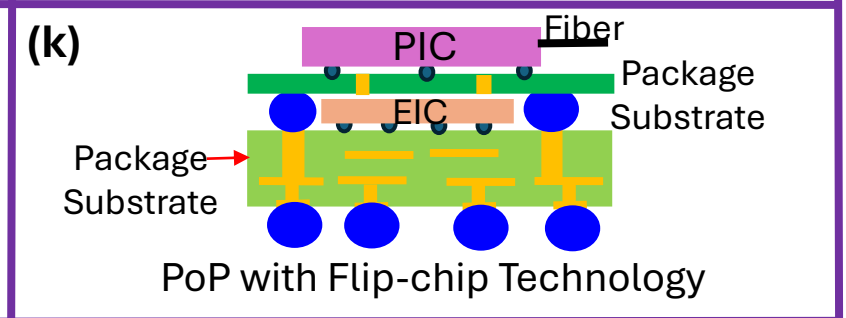
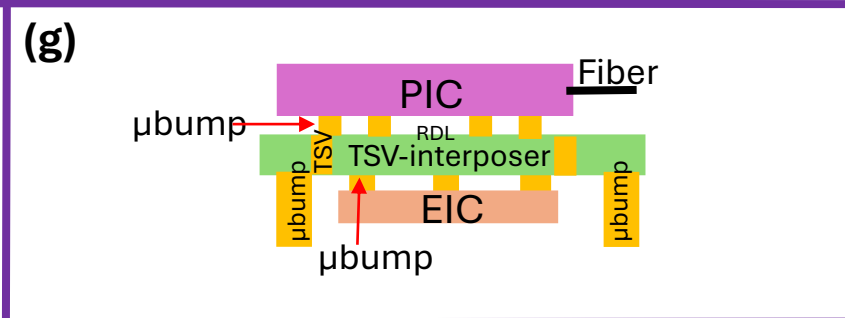
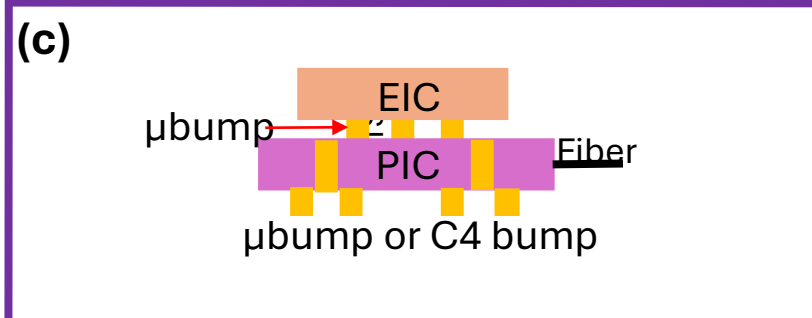
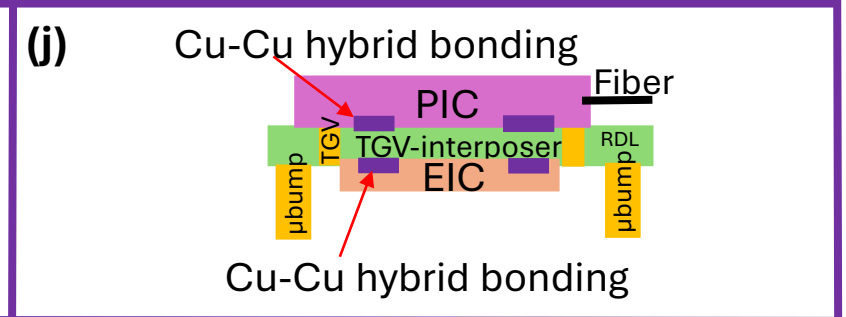
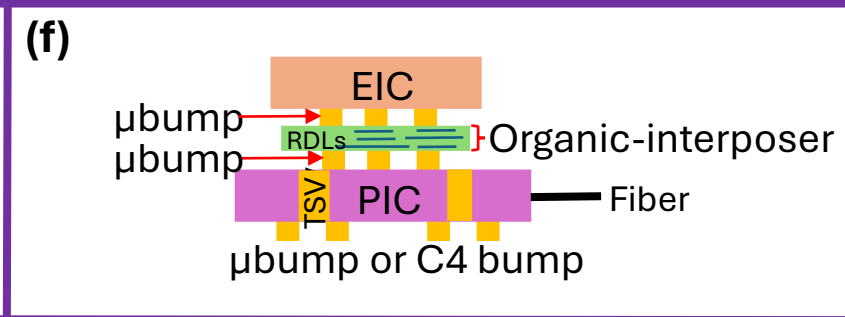
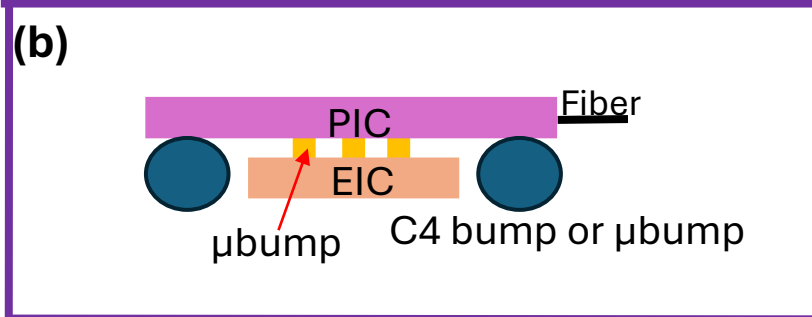
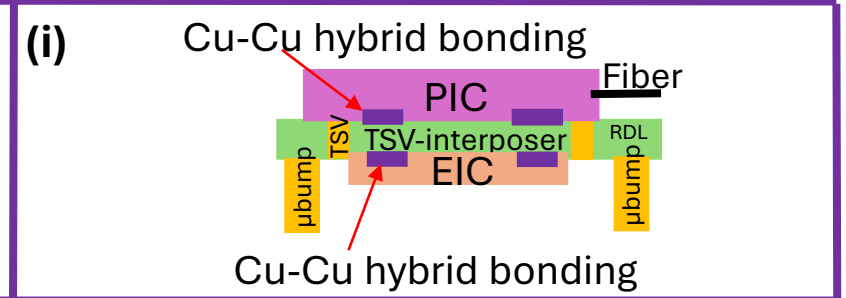
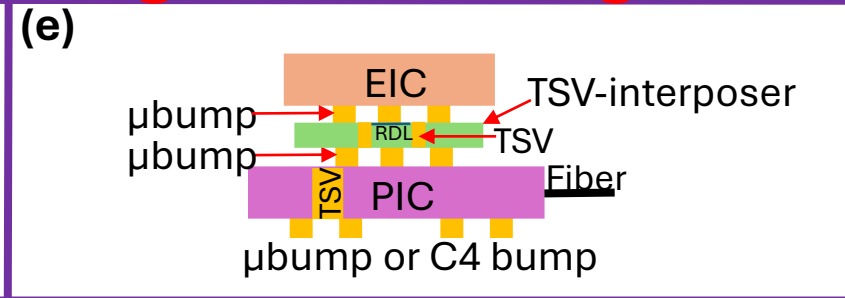
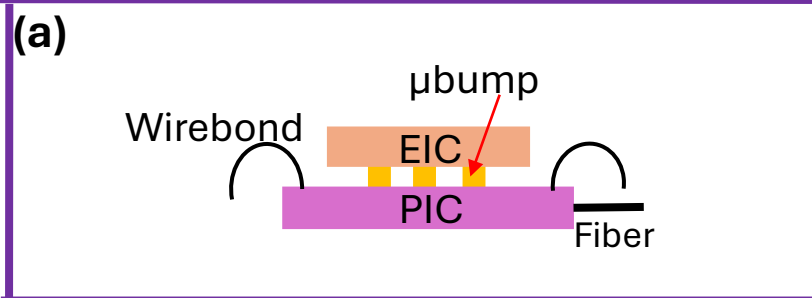


Future

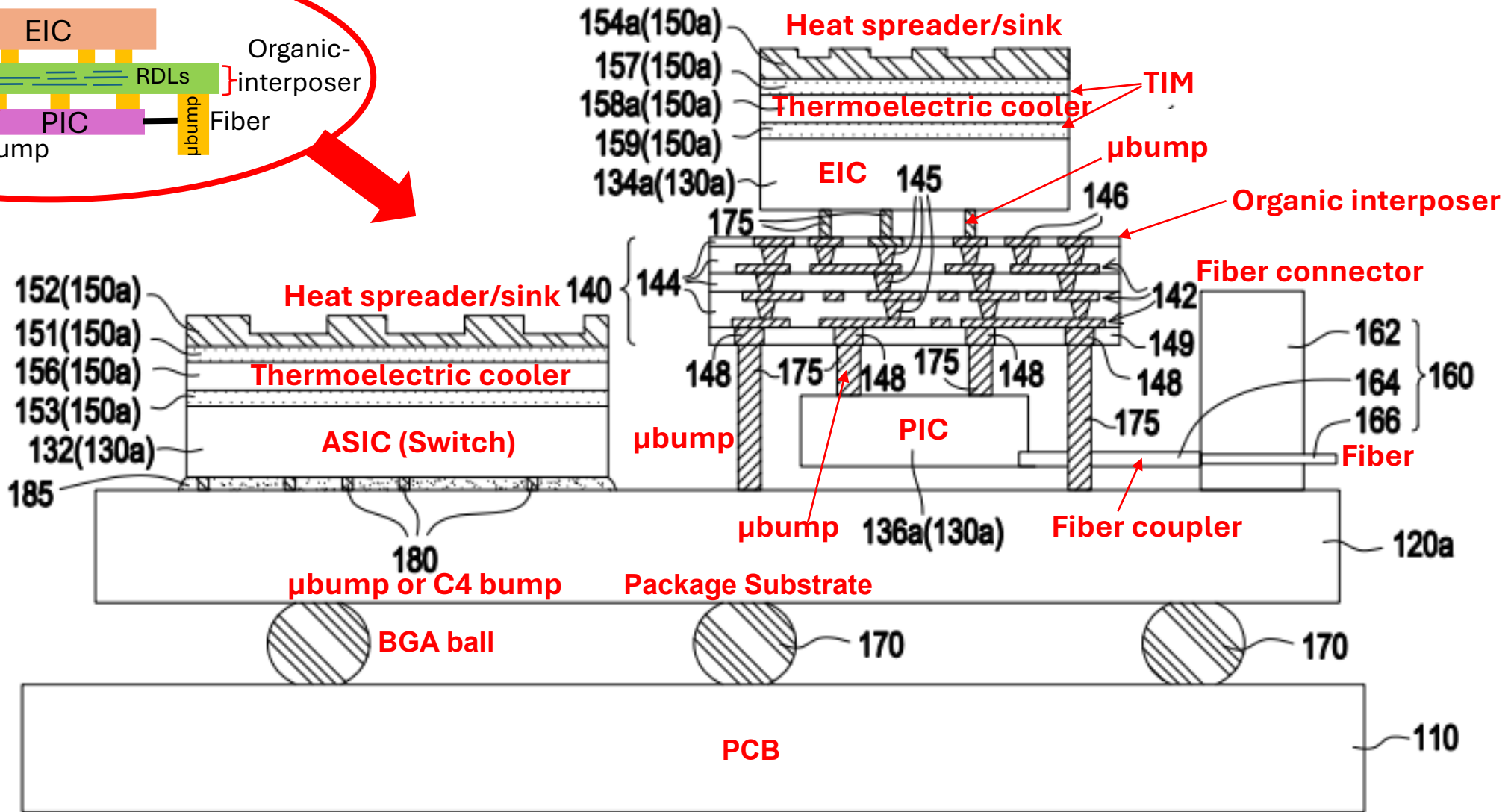
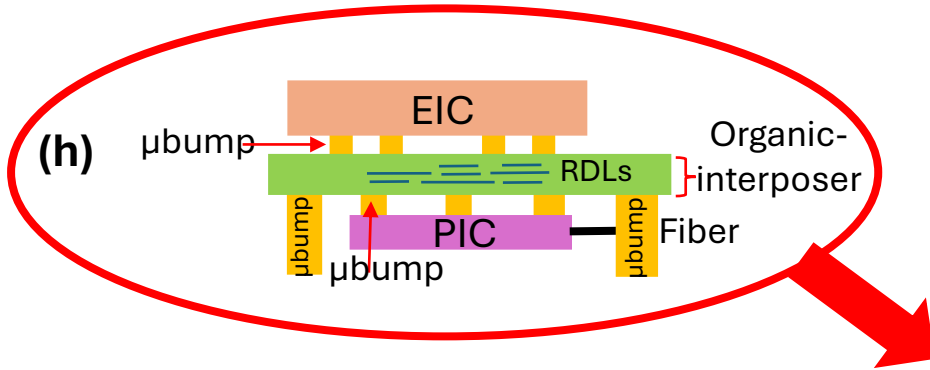
With co-packaged optics (CPO), the switch chip is typically surrounded by 16 OEs (optical engines), all placed on an organic package substrate (see figures above).

Currently, the 25.6-terabit Ethernet switch chip requires 16@1.6 terabits-per-second (1.6Tbps) OEs while the upcoming **51.2-terabit switch chips** will use **3.2Tbps OEs** (the size of EIC and PIC of the OE will be larger). The **issue** is that the multi-chip module can only be so large. It is **challenging** with today's packaging technology to surround the 51.2-terabit ASIC with 16@3.2Tbps OEs.

Various 3D Heterogeneous Integration of PIC and EIC



3D Heterogeneous Integration of EIC and PIC Devices (A)



3D heterogeneous integration of EIC and PIC on a co-packaged substrate (organic interposer)

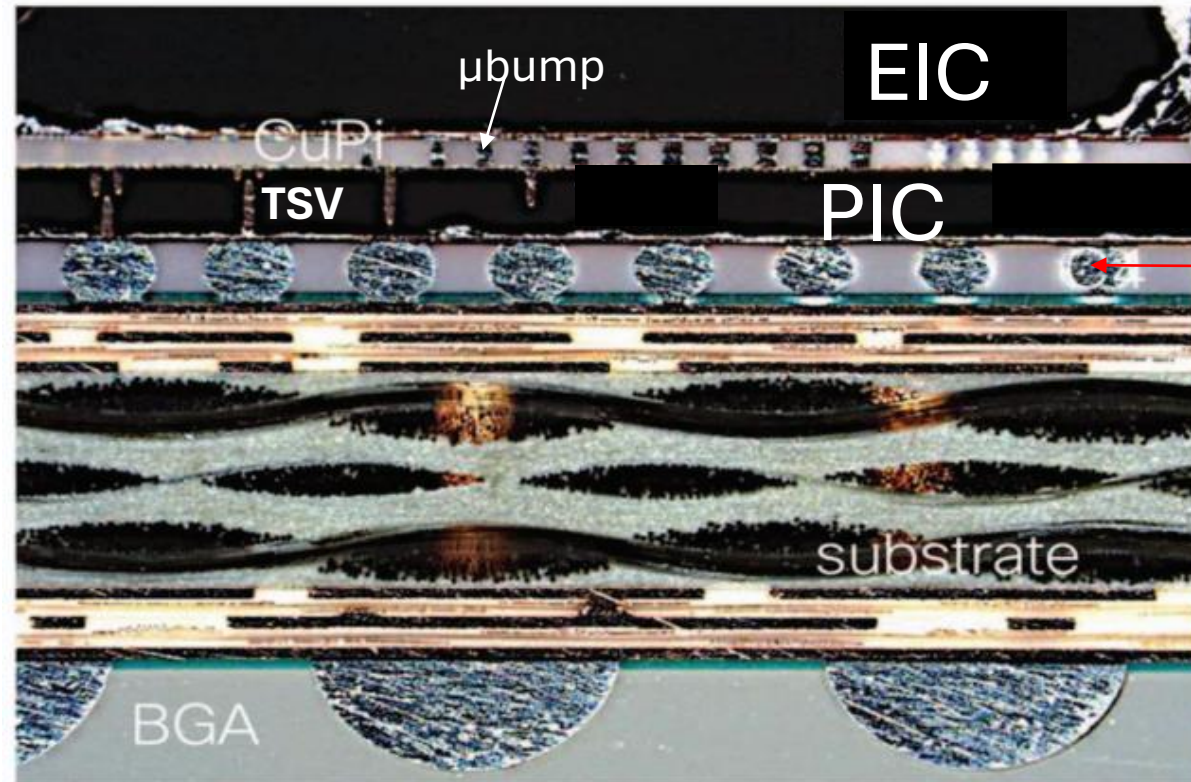
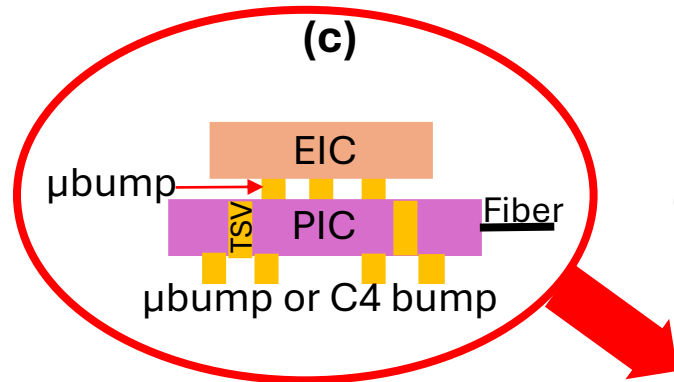
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CISCO ECTC2023

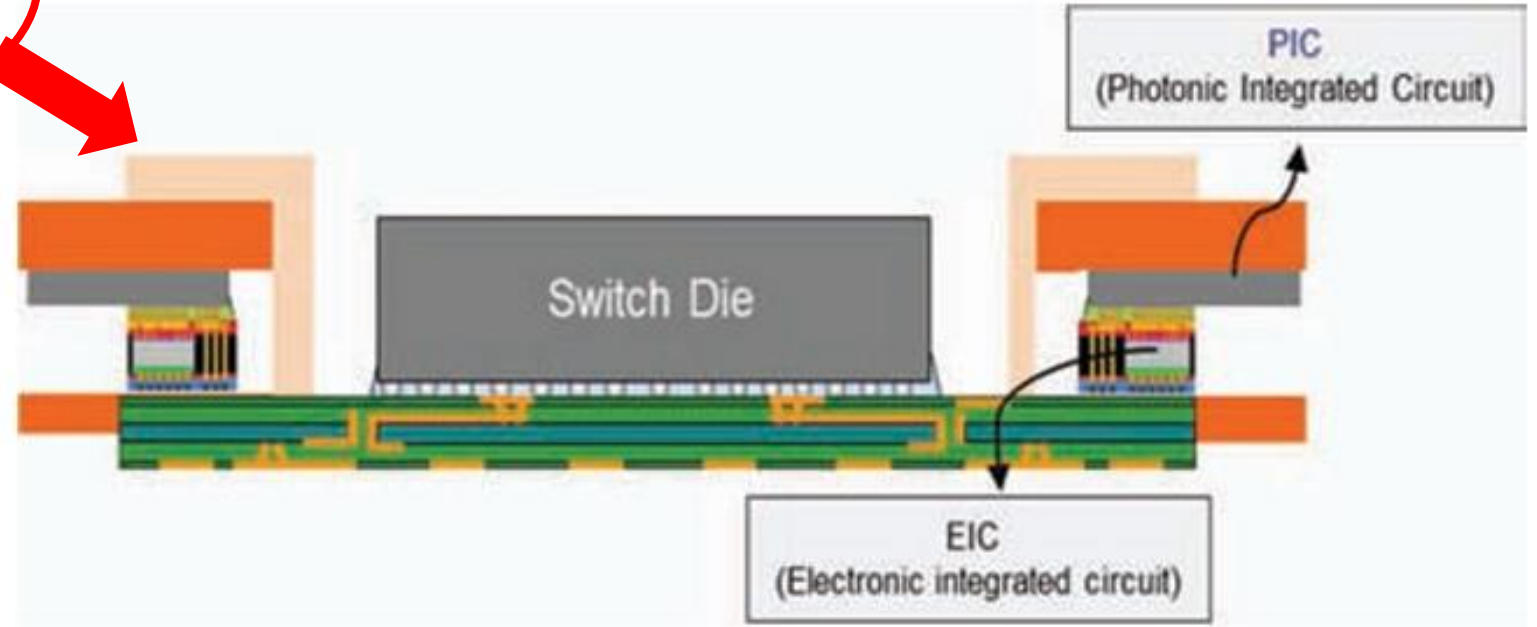
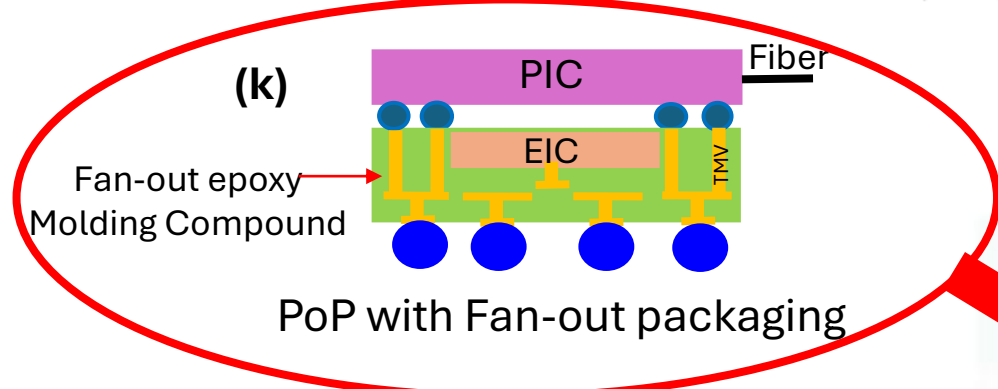
3D Fan-Out Embedded Bridge Structure for Co-Packaged Optics Characterization and Evaluation

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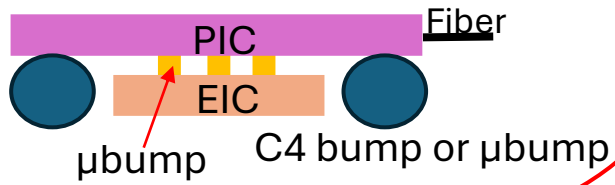
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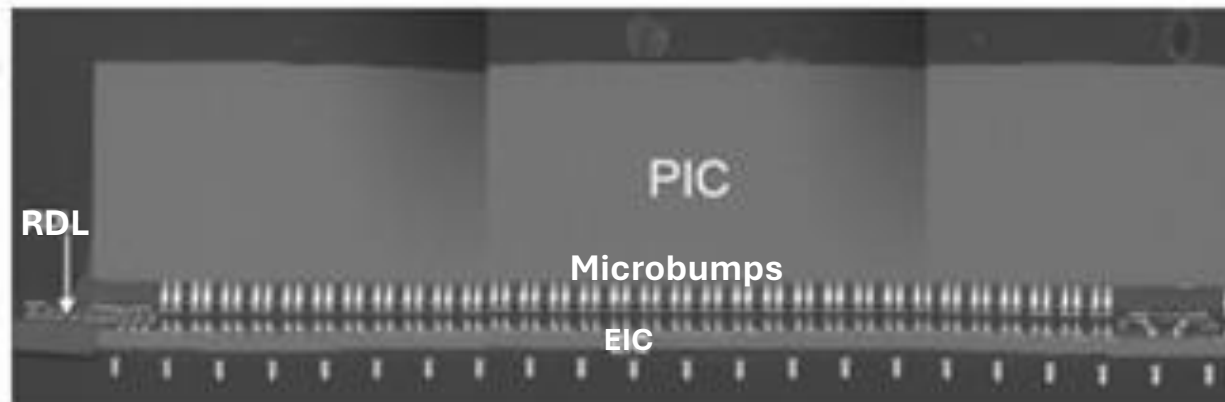


3D Broadcom's 51.2-Tbps Bailly Co-Packaged Optics (CPO)

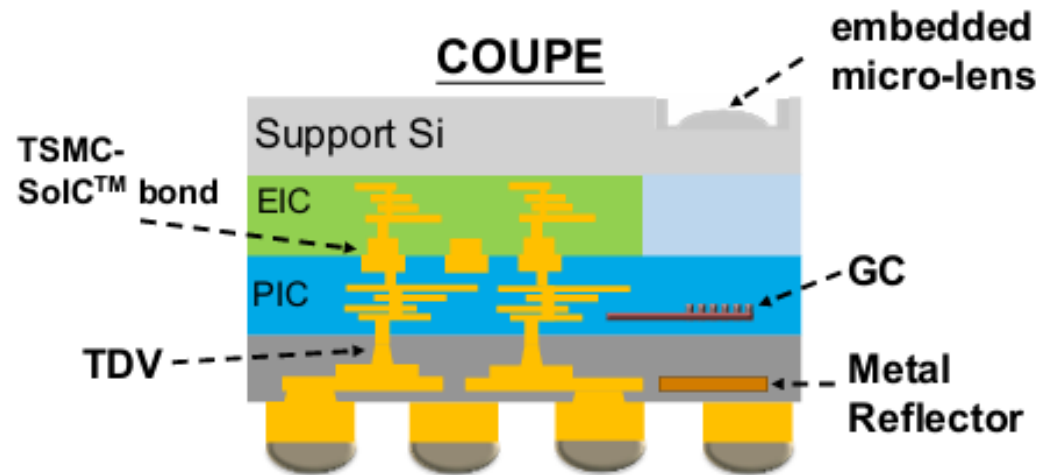
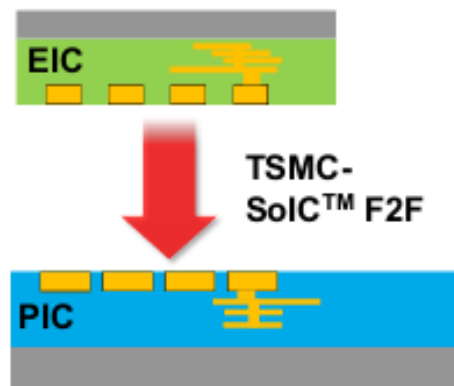
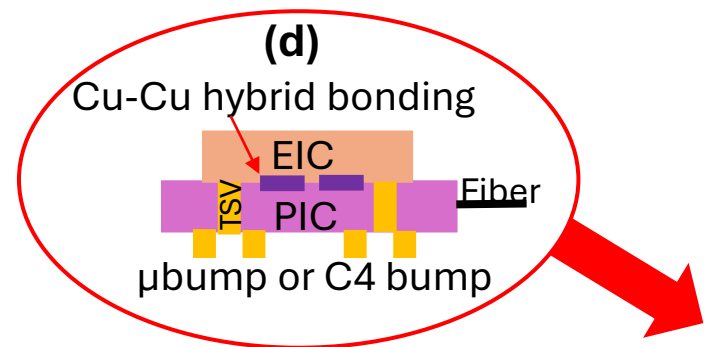
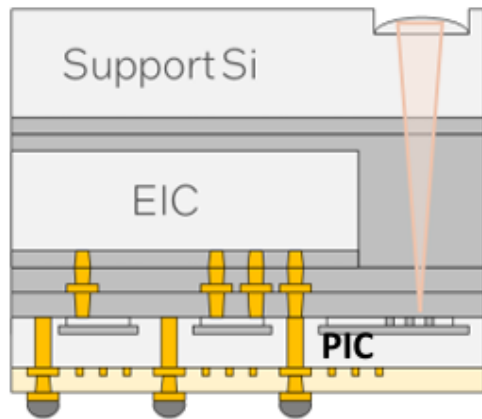
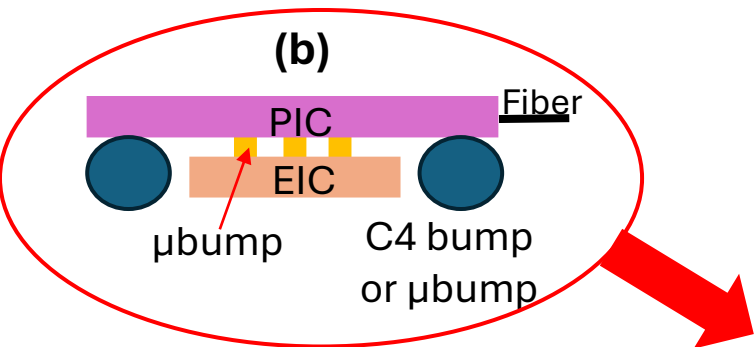
(b)



51.2-Tbps CPO switch



3D TSMC's COUPE (Compact Universal Photonic Engine) for NVIDIA's COP

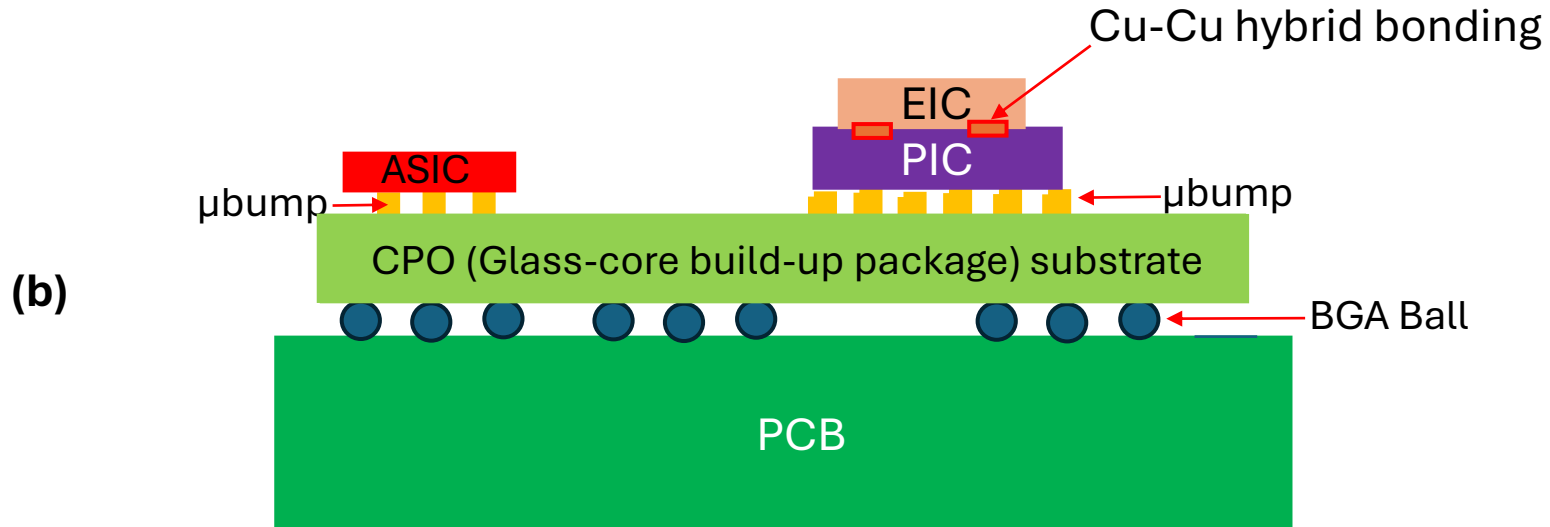
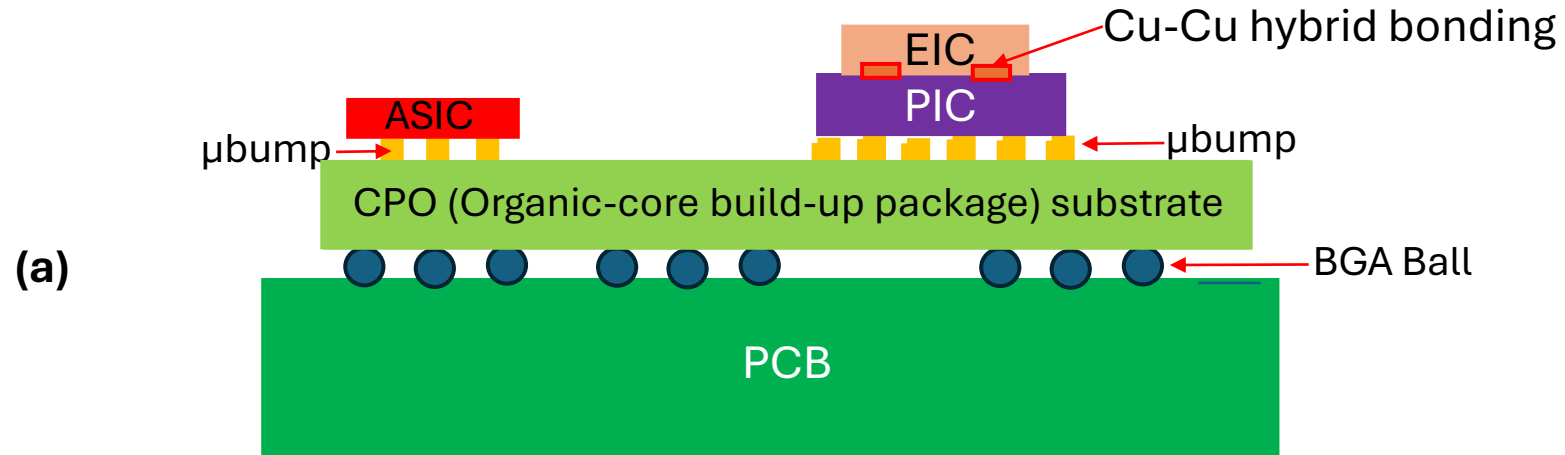
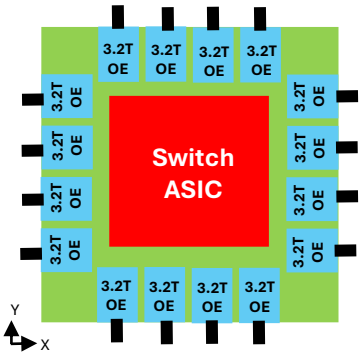


Due to the requirement of:

- **higher interconnect density,**
- **finer pitch,**
- **more compact 3D integration,**
- **lower power consumption,**
- **lower latency,**
- **higher bandwidth,**
- **better signal integrity**

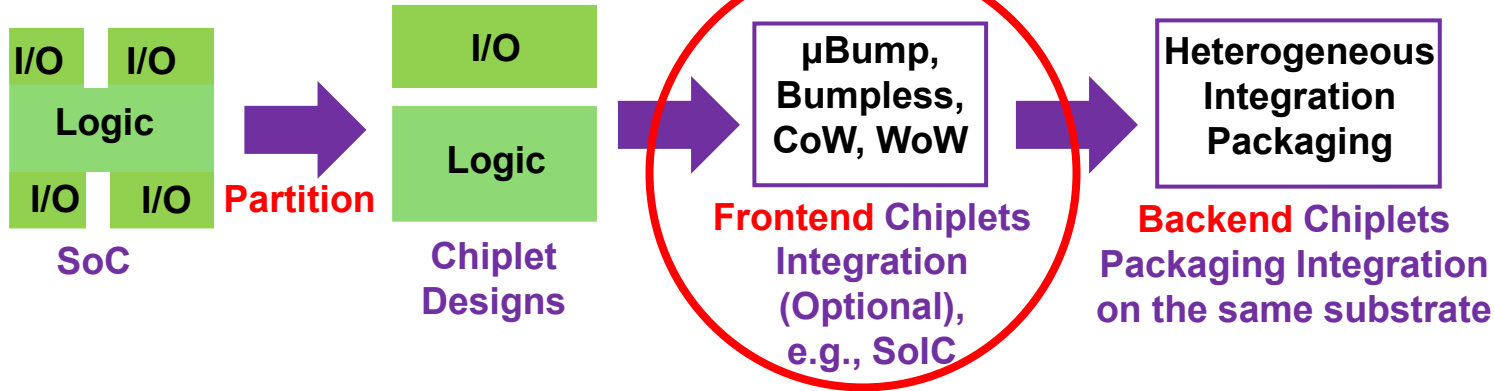
of a CPO system driven by future AI/Data Center, the Cu-Cu hybrid bonding of some of the PICs and EICs are strongly recommended.

3D heterogeneous integration of ASIC, EIC and PIC. (a) On an organic-core build-up package substrate. (b) On a glass-core build-up package substrate.

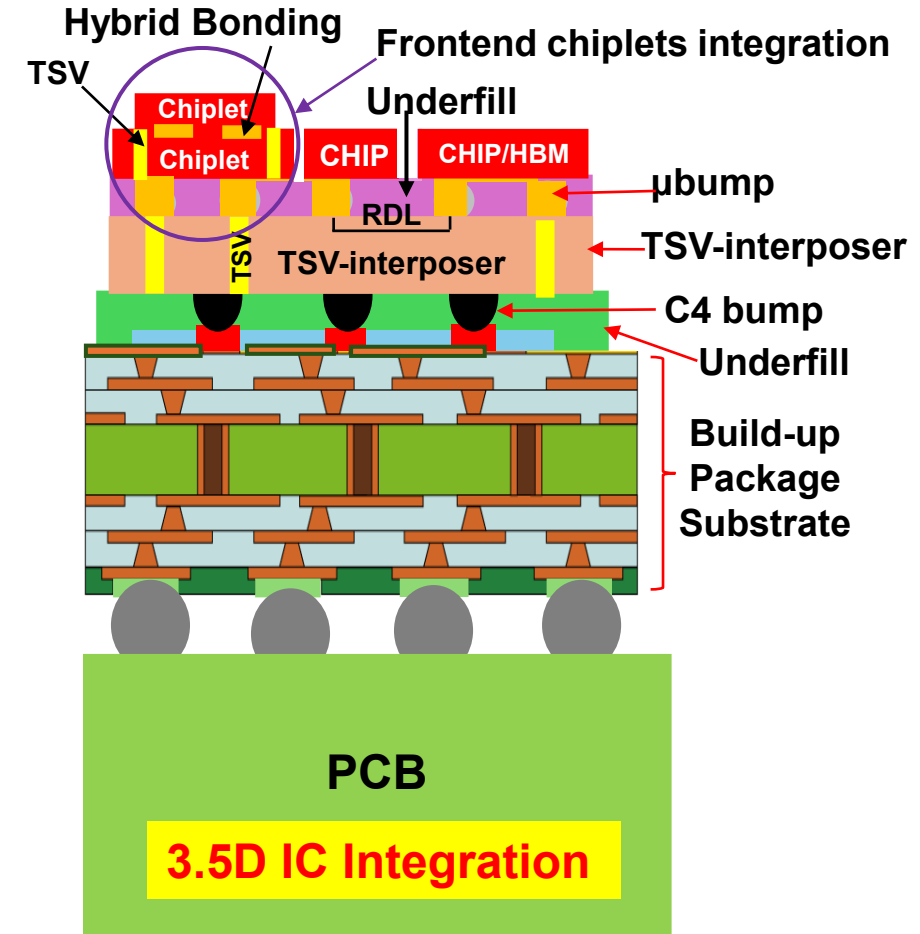
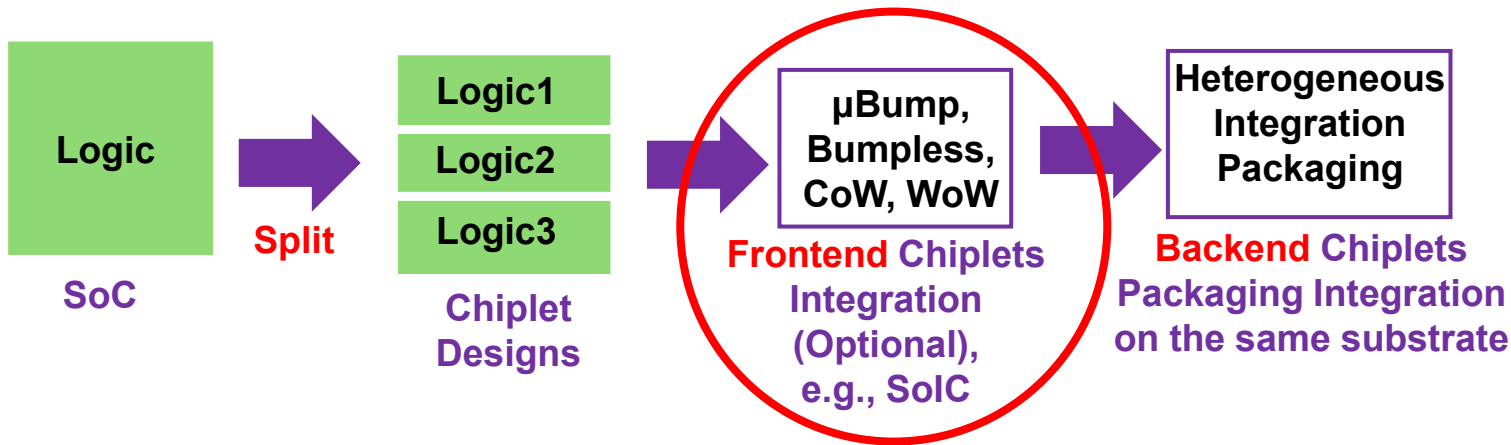


Unimicron's 3.5D IC Heterogeneous Integration

Chip partition and integration (Driven by cost and technology optimization)



Chip split and integration (Driven by cost and yield)

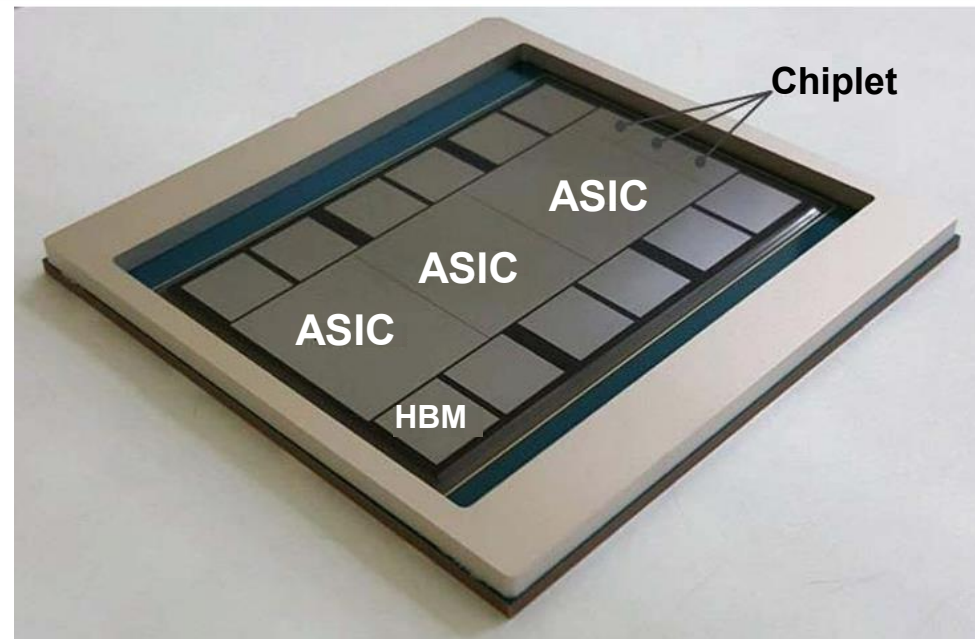
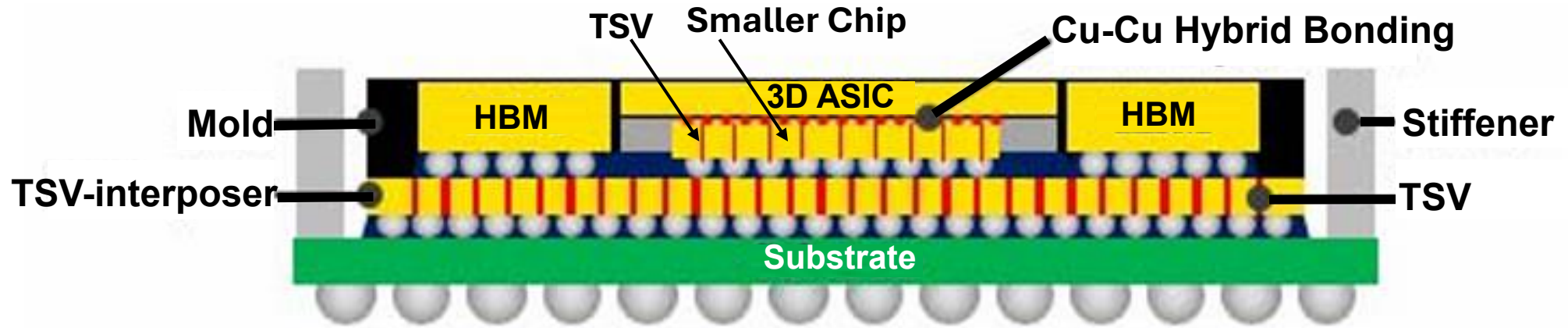


3.5D IC Integration

- **Smaller Package Size**
- **Better Electrical Performance**

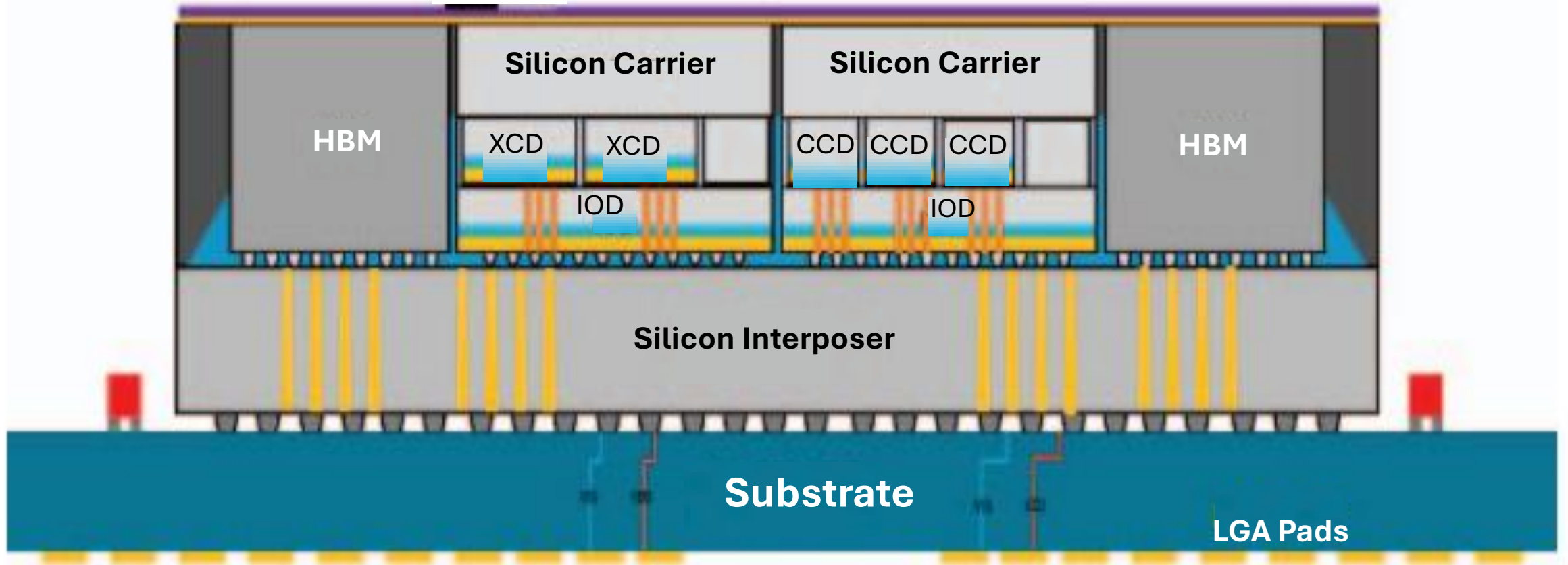
J. H. Lau, "Recent Advances and Trends in Chiplet Design and Heterogeneous Integration Packaging", *ASME Transactions, Journal of Electronic Packaging*, published online: June 2023, and hard-copy: March 2024, pp. 010801-1 – 31.

Samsung's 3.5D IC Heterogeneous Integration



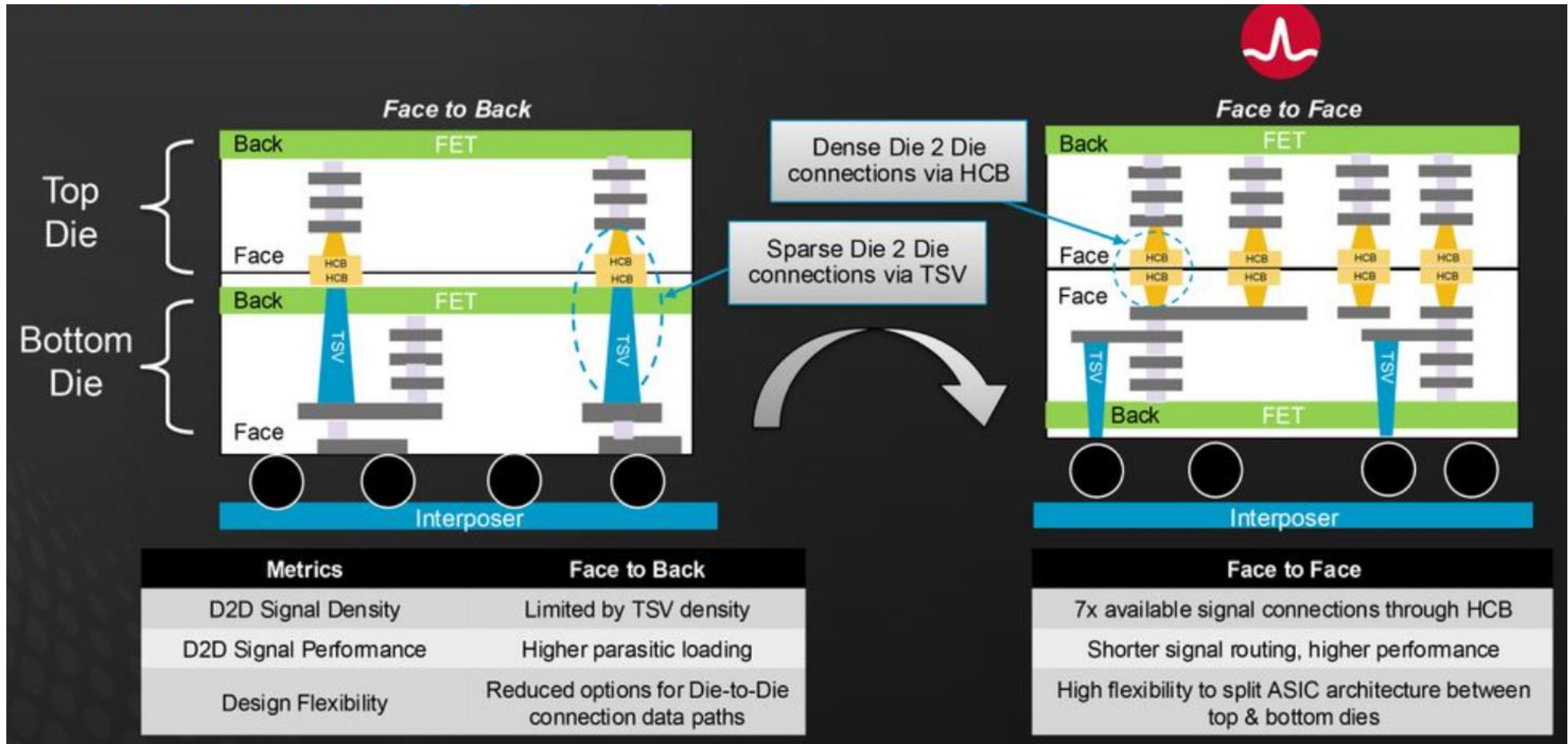
I. Lee, et al., "Extremely Large 3.5D Heterogeneous Integration for the Next-Generation Packaging Technology", *IEEE/ECTC Proceedings*, June 2023, pp. 893-898.

AMD's 3.5D IC Heterogeneous Integration



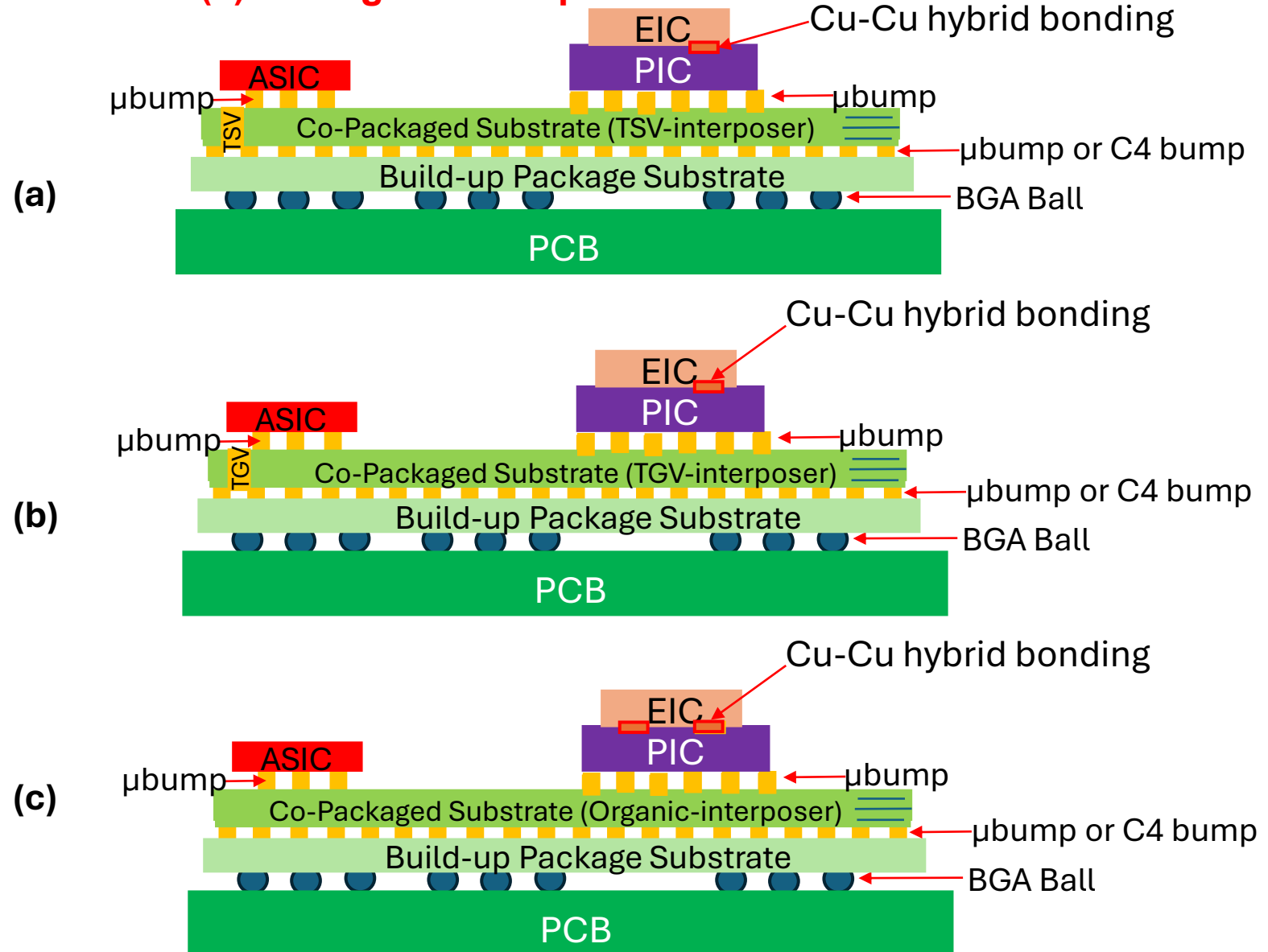
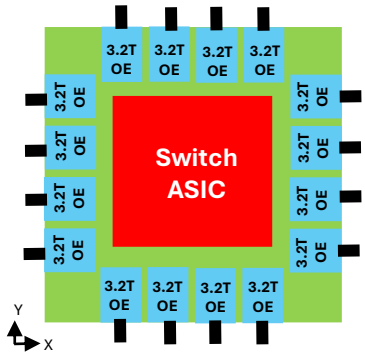
C. Mandalapu, C. Buch, P. Shah, R. Topacio, P. Cheng, L. Wang, et al., "3.5D Advanced Packaging Enabling Heterogeneous Integration of HPC and AI Accelerators", *IEEE/ECTC Proceedings*, May 2024, pp. 798-802.

Broadcom's 3.5D IC Heterogeneous Integration



<https://www.tomshardware.com/tech-industry/artificial-intelligence/broadcom-unveils-gigantic-3-5d-xdsip-platform-for-ai-xpus-6000mm2-of-stacked-silicon-with-12-hbm-modules> (Dec 7, 2024)

3.5D heterogeneous integration of EIC and PIC and ASIC. (a) On TSV-interposer. (b) On TGV-interposer. (c) On organic-interposer.

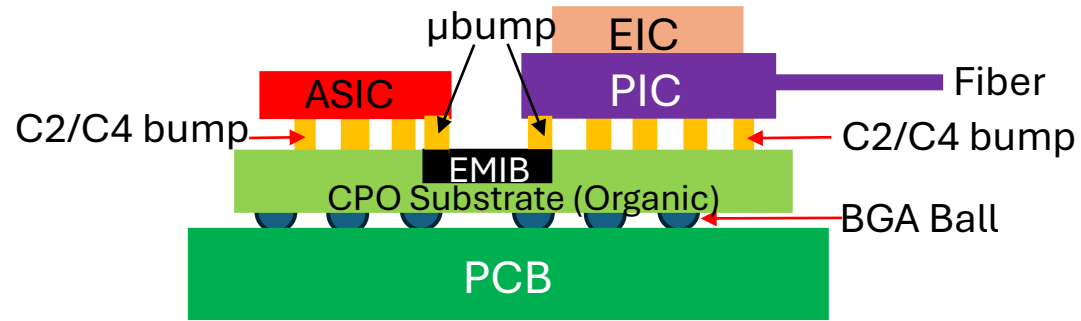


3D Heterogeneous Integration of Switch, PIC and EIC with Bridges

CPO Structures

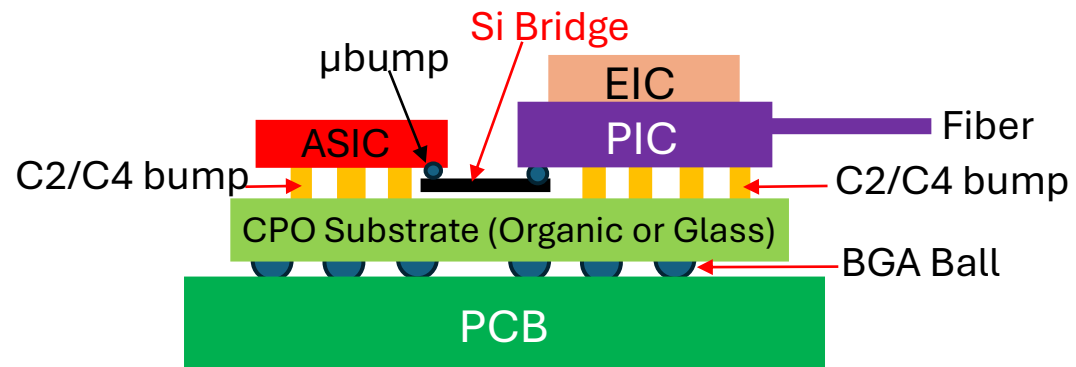
Advantages

Disadvantages



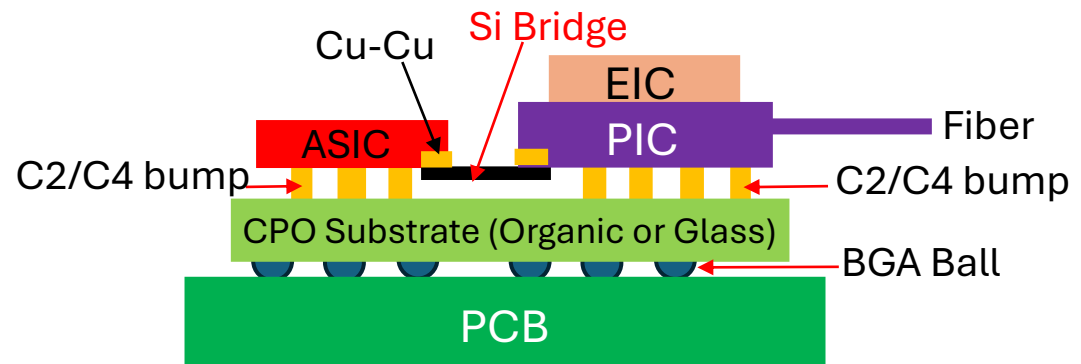
- High performance
- Fine pitch
- High density

- Higher cost
- EMIB involves complicated CPO substrate fabrication



- Higher performance
- Finer pitch
- Higher density
- Simple CPO substrate

- High cost



- Highest performance
- Finest pitch
- Highest density
- Simple CPO substrate

- Highest cost
- Hybrid bonding involves complicated chip bonding processes

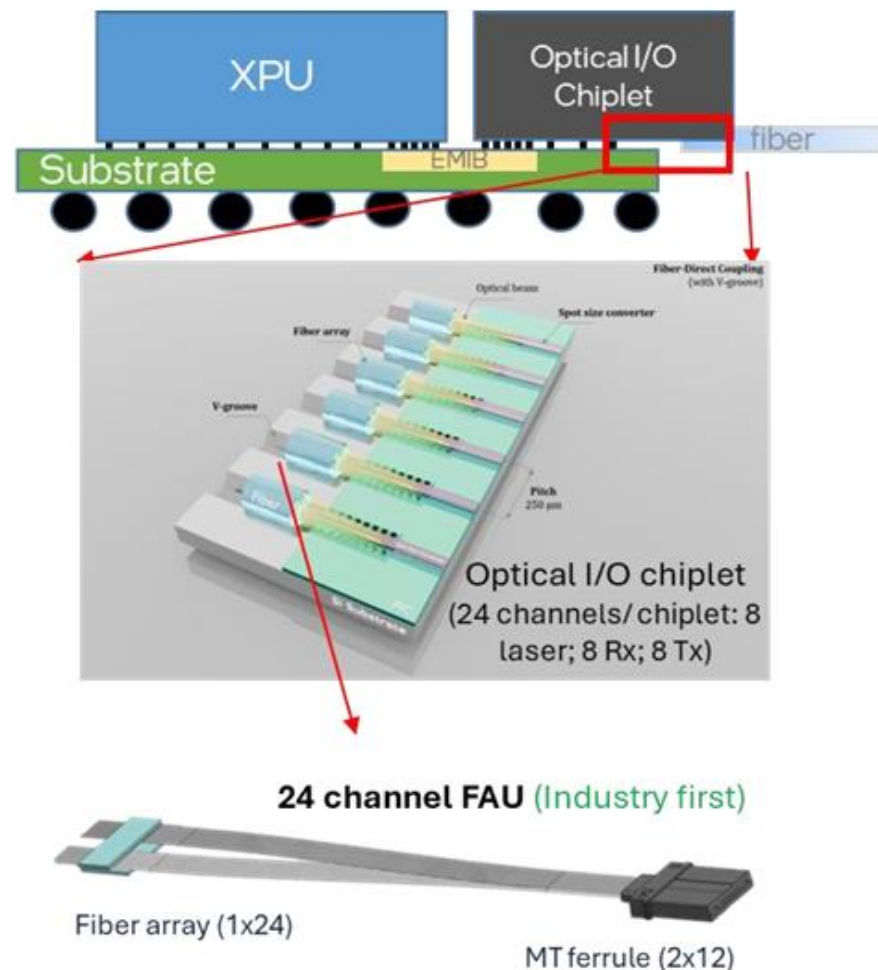
Heterogeneous Integration of Fiber-Based Co Packaged Optics with EMIB technology: Assembly, Performance, and Reliability

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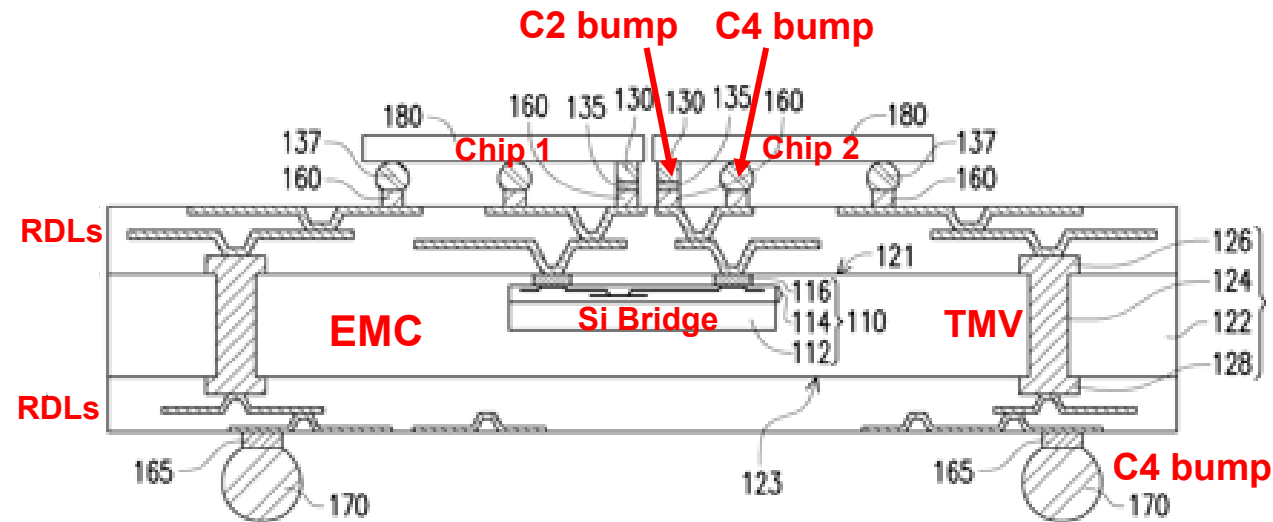
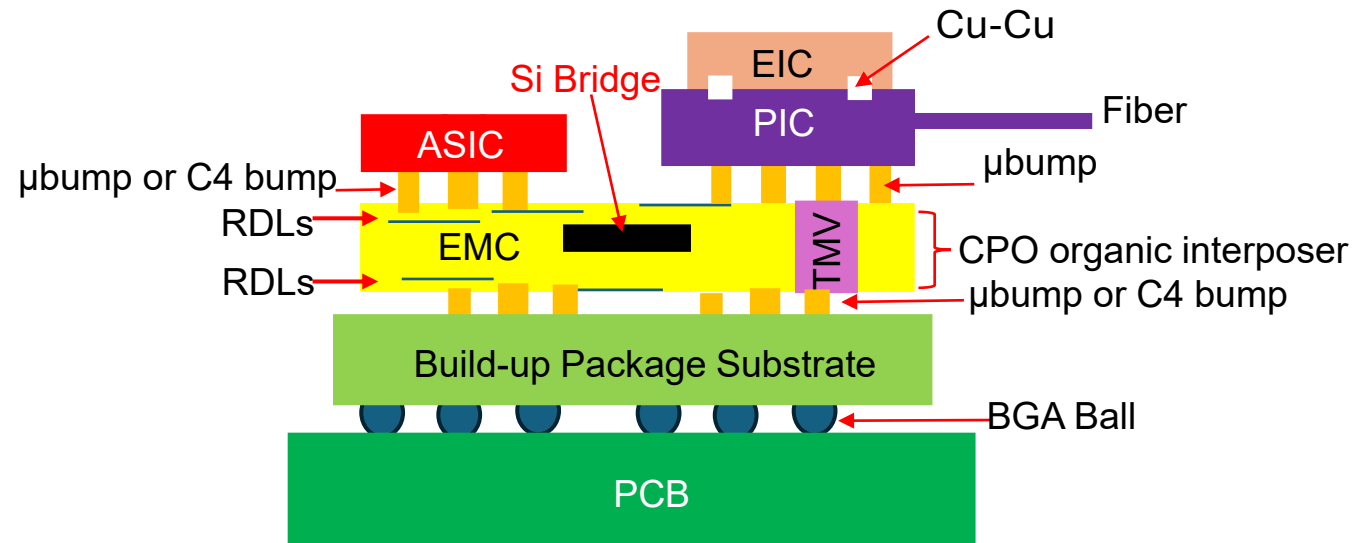
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ECTC June 2025

Bridges in Fan-out Epoxy Molding Compound (EMC) + RDLs



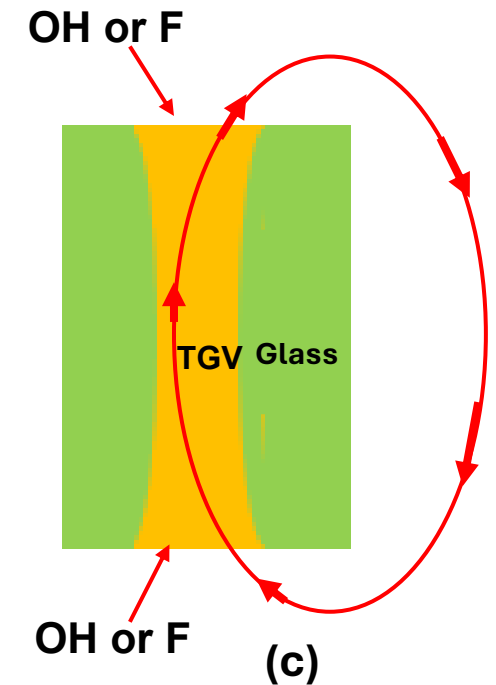
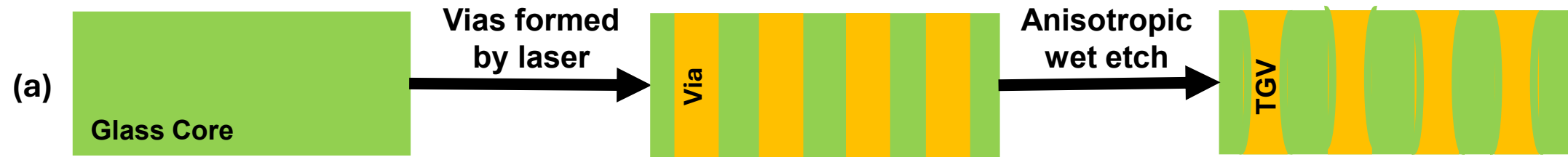
US Patent no. 11,410, 913.
Filed on May 7, 2021.

Package Substrate

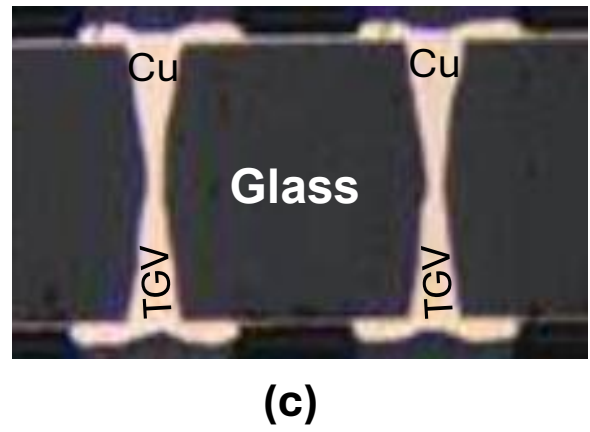
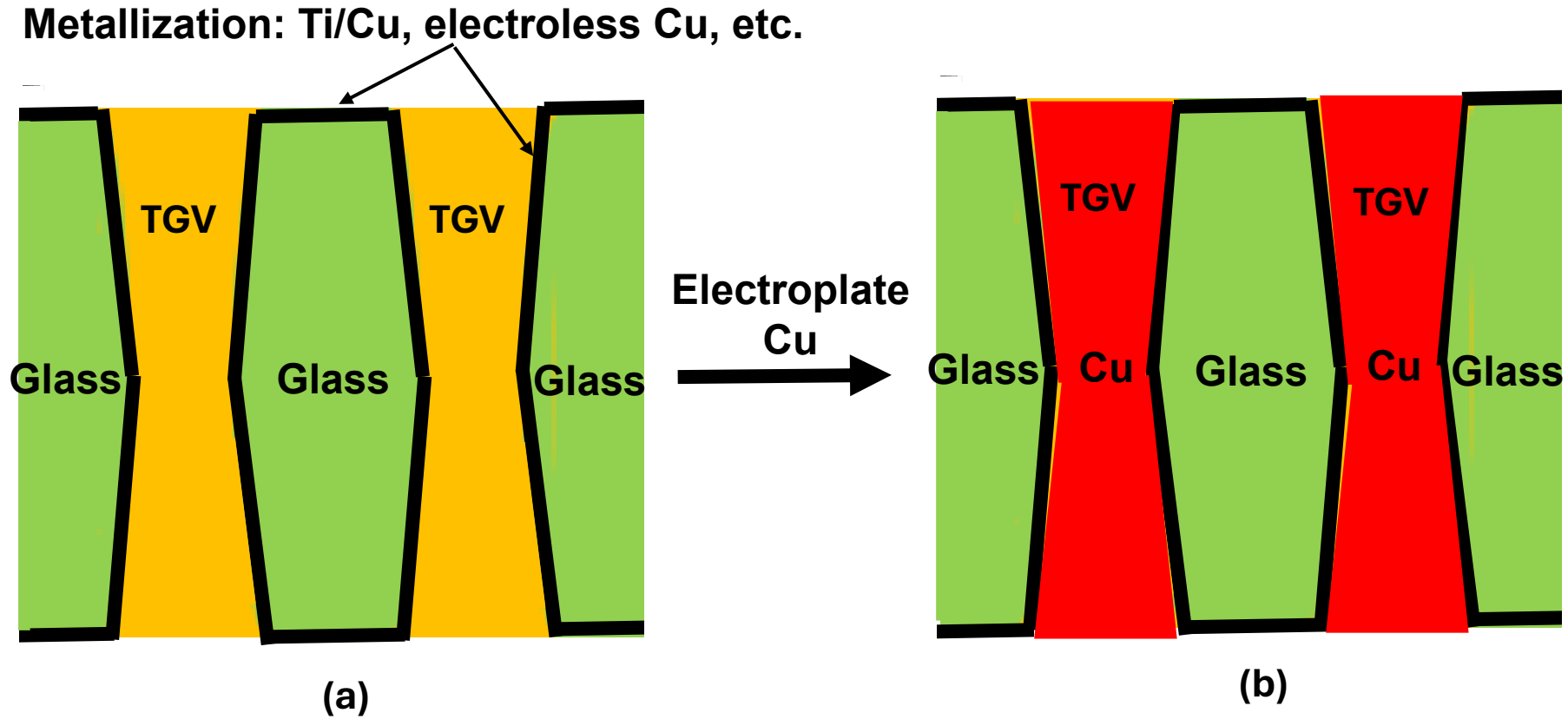
3D Heterogeneous Integration of Switch, PIC and EIC on Glass Substrate

Because glass has a higher ability to seamlessly integrate optical interconnects, more use of the glass substrate or glass interposer for CPO is recommended.

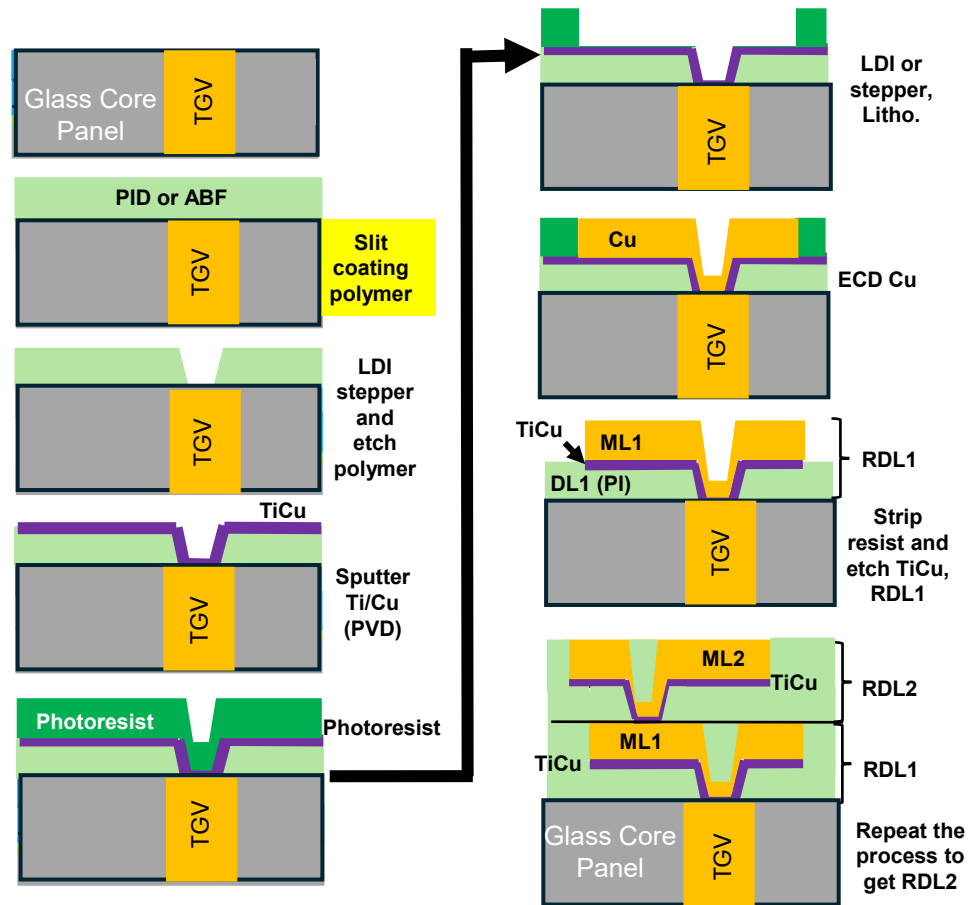
(a) TGV Process flow. (b) SEM image of a TGV. (b) (c) Etch solution mechanism



(a) TGV sidewall metallization. (b) Cu plating. (c) An image of Cr-filled TGV

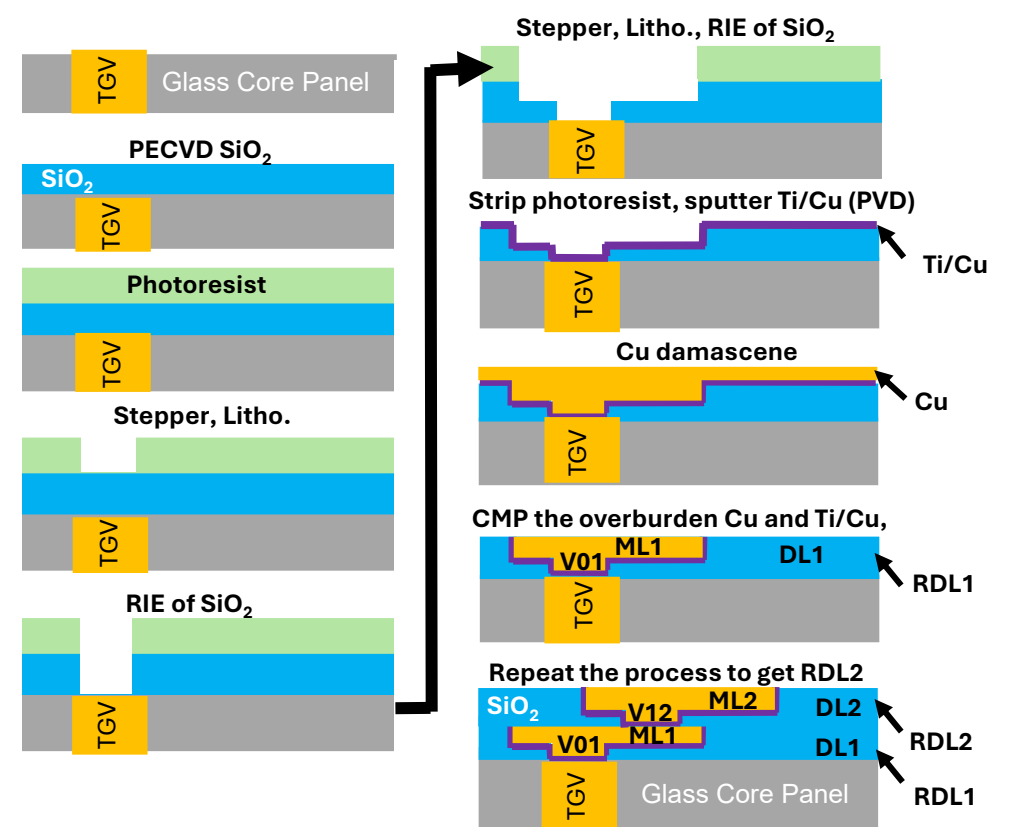


TGV RDL Process Flow. (a) L/S $\geq 2\mu\text{m}$. (b) L/S $< 2\mu\text{m}$.



- PID or ABF as dielectric layer ($\leq 5\mu\text{m}$)
- L/S ($\geq 2\mu\text{m}$)
- LDI or Stepper
- PVD
- ECD Cu

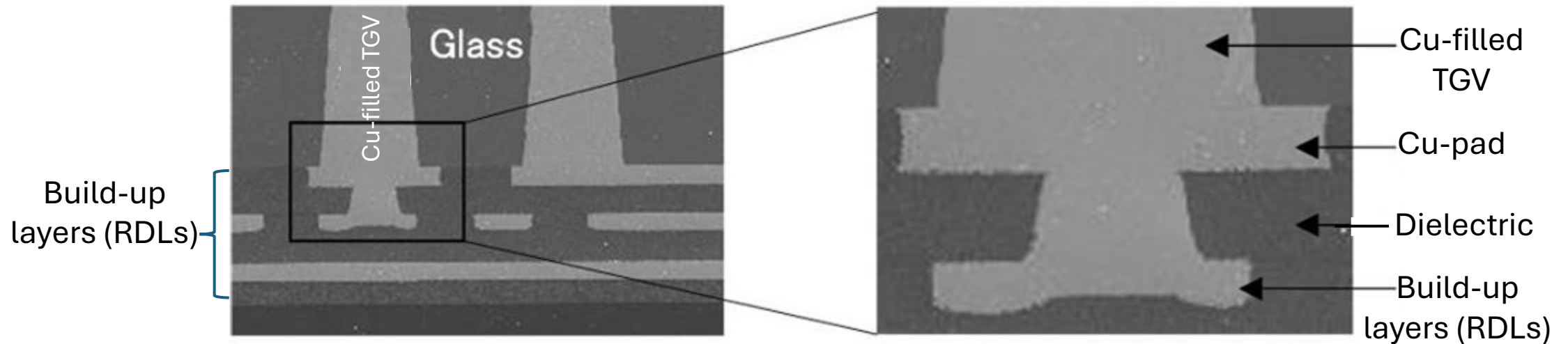
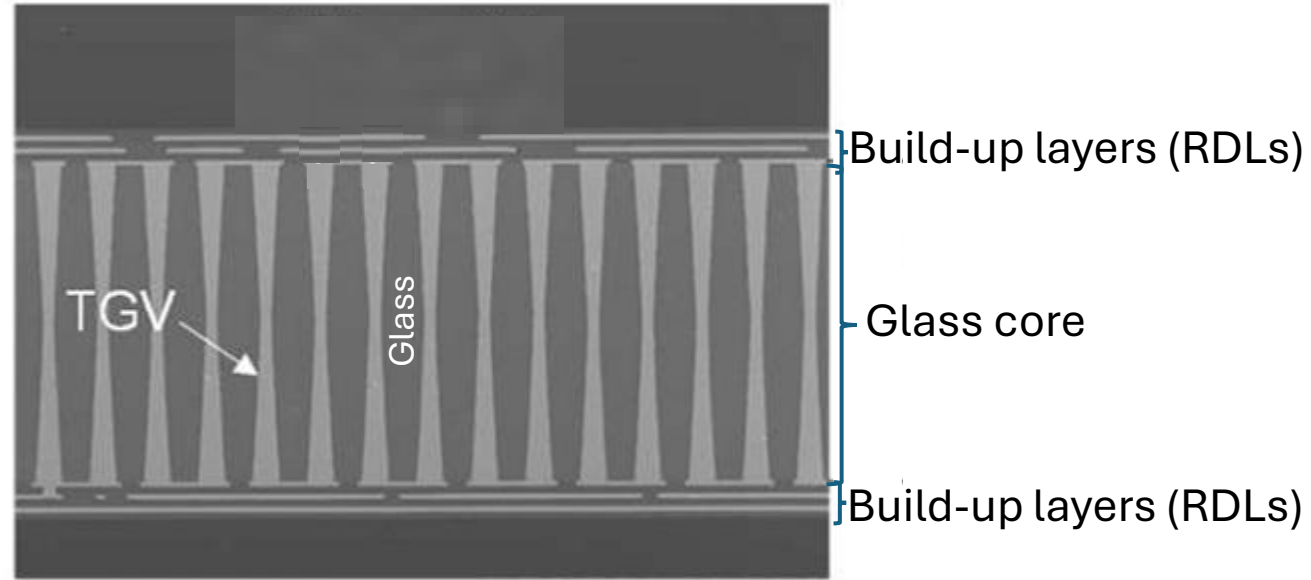
(a)



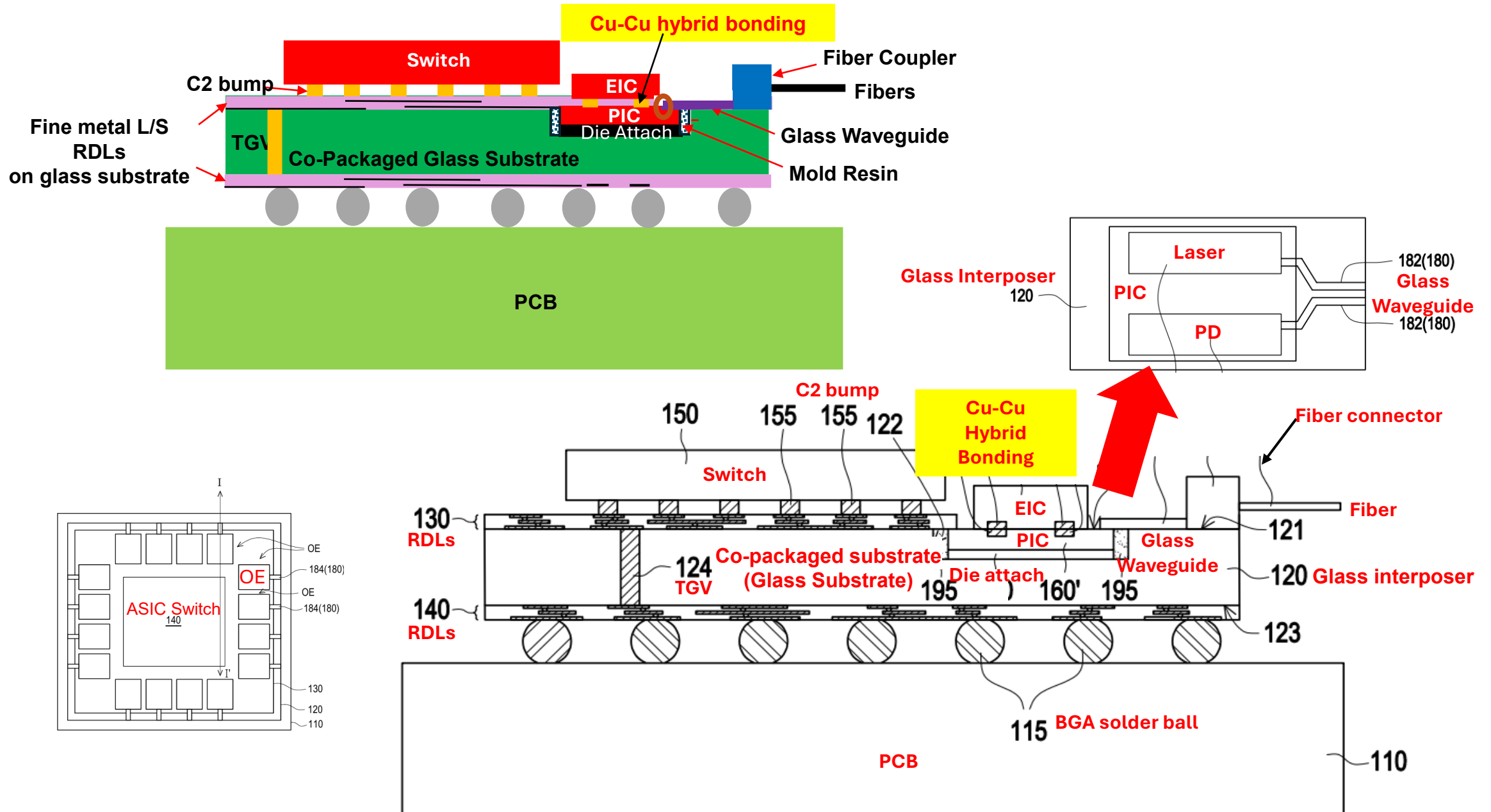
- SiO₂ as dielectric layer ($\sim 1\mu\text{m}$)
- L/S ($< 2\mu\text{m}$)
- PECVD
- Stepper
- PVD
- Dual Cu-damascene
- CMP

(b)

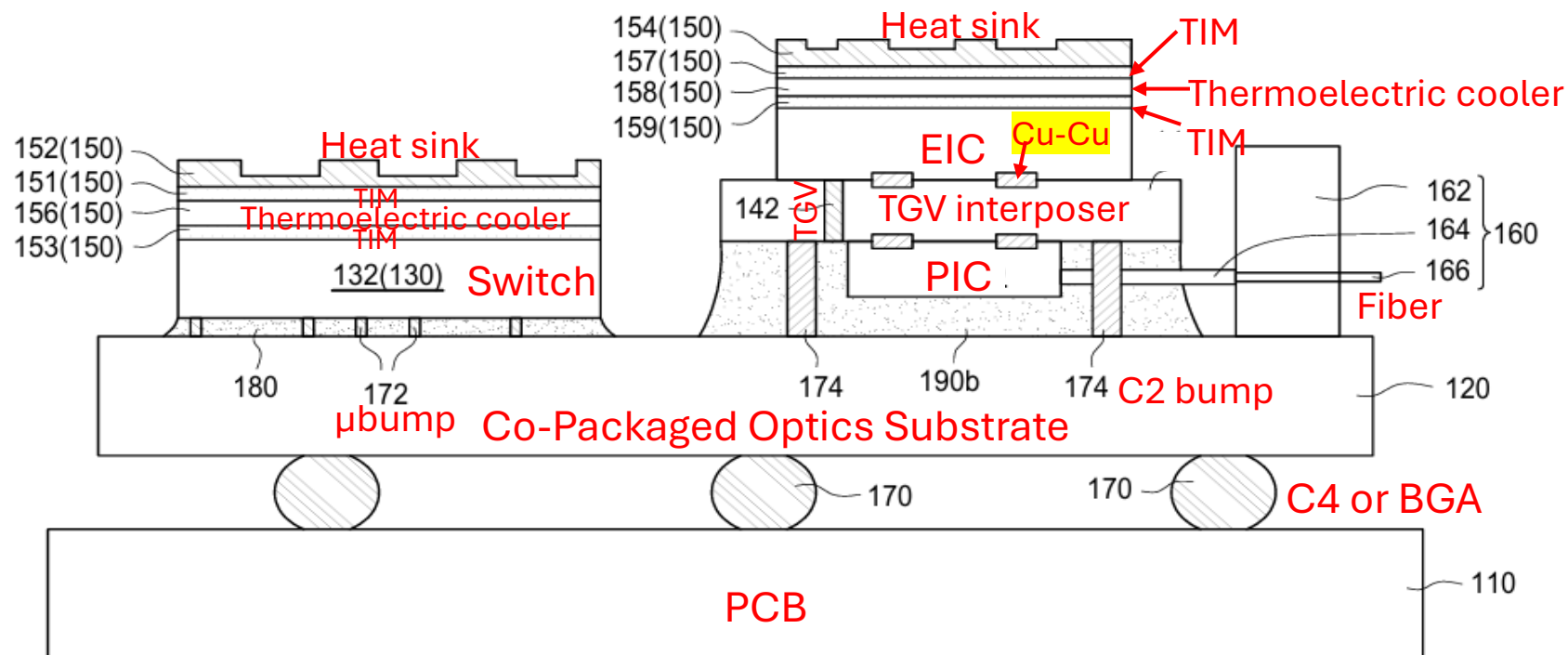
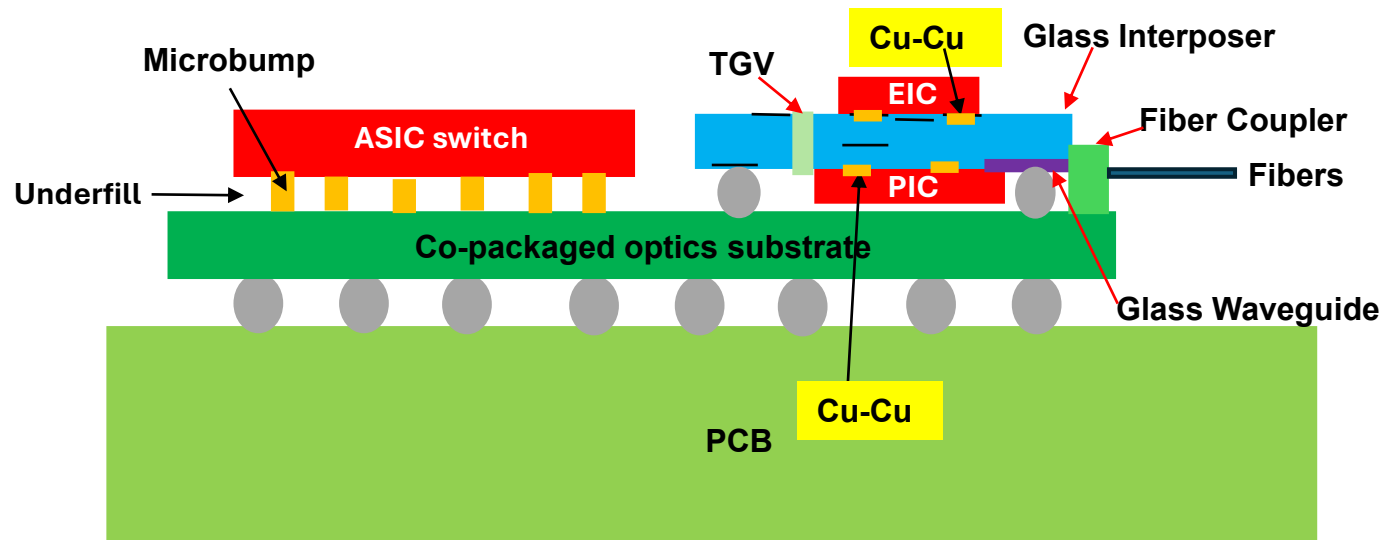
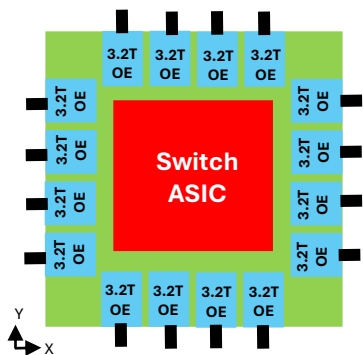
SEM image of glass-core substrate with TGV and RDLs (build-up layers)



3D Heterogeneous Integration of EIC and PIC by Cu-Cu Hybrid Bonding with the PIC Embedded in a Co-Packaged Glass Substrate

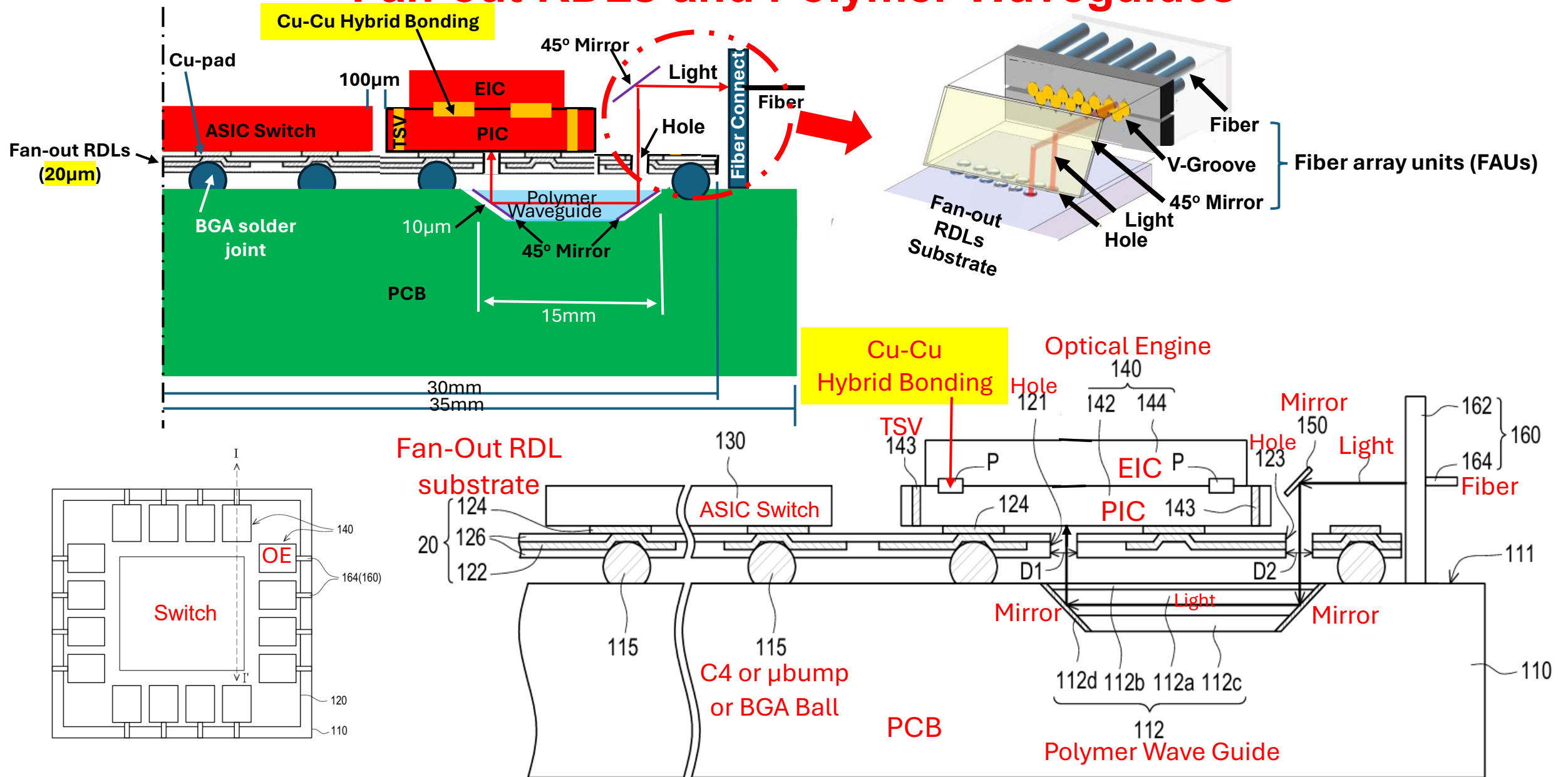


3D Heterogeneous Integration of PIC and EIC with Glass Interposer and Cu-Cu Hybrid Bonding

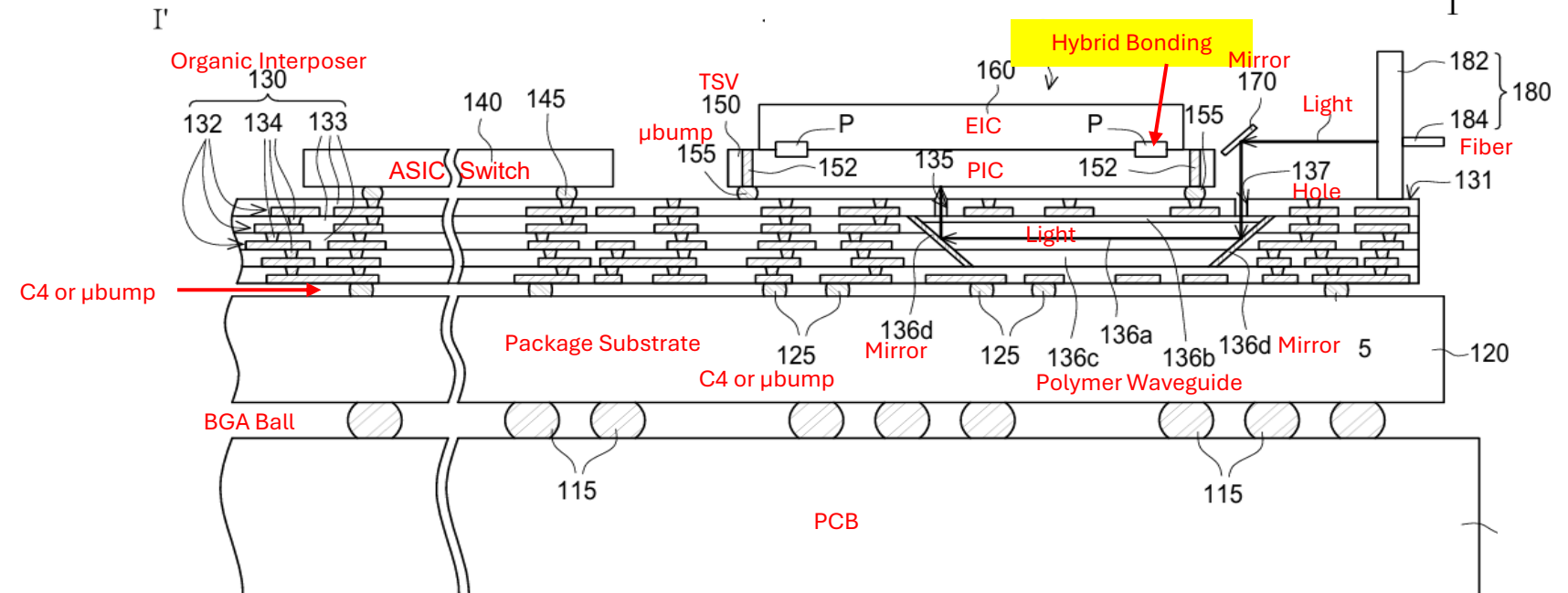
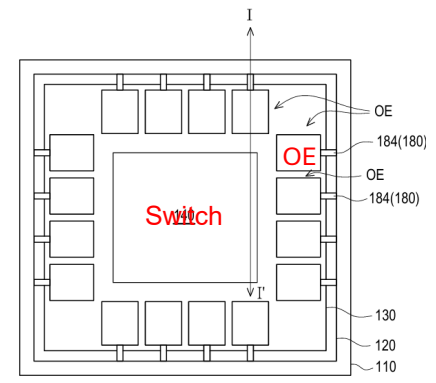
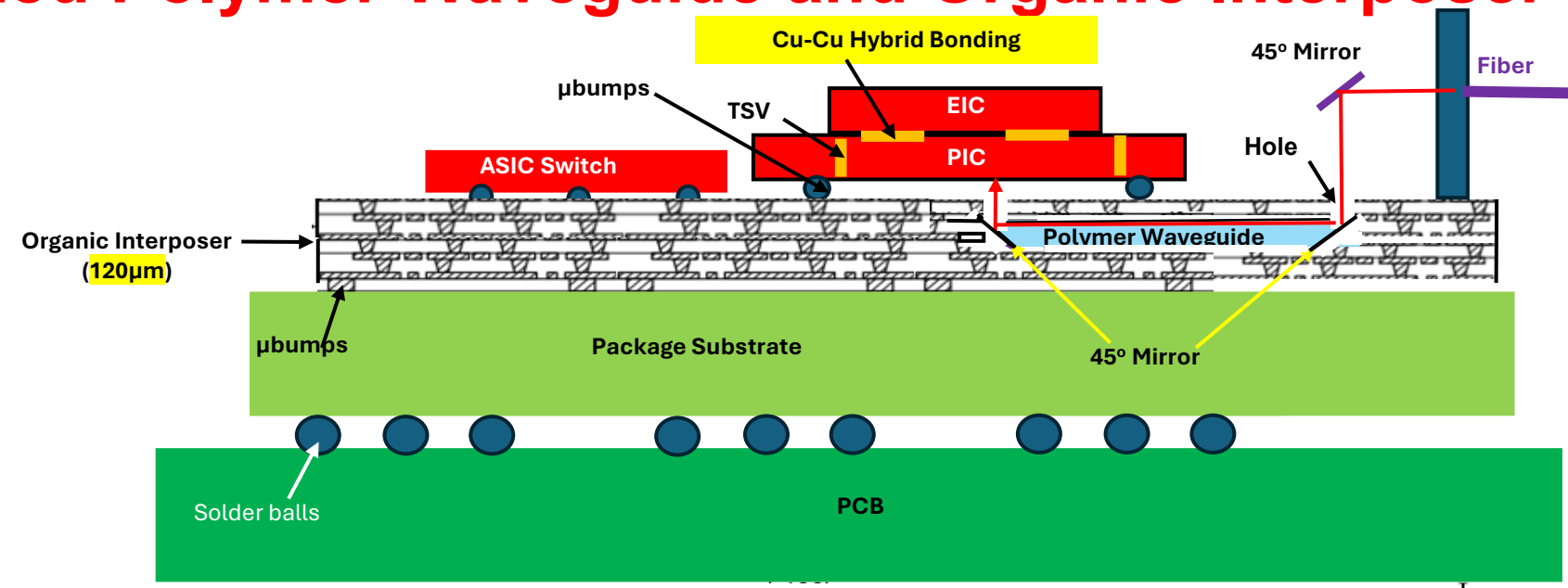


More COP structures

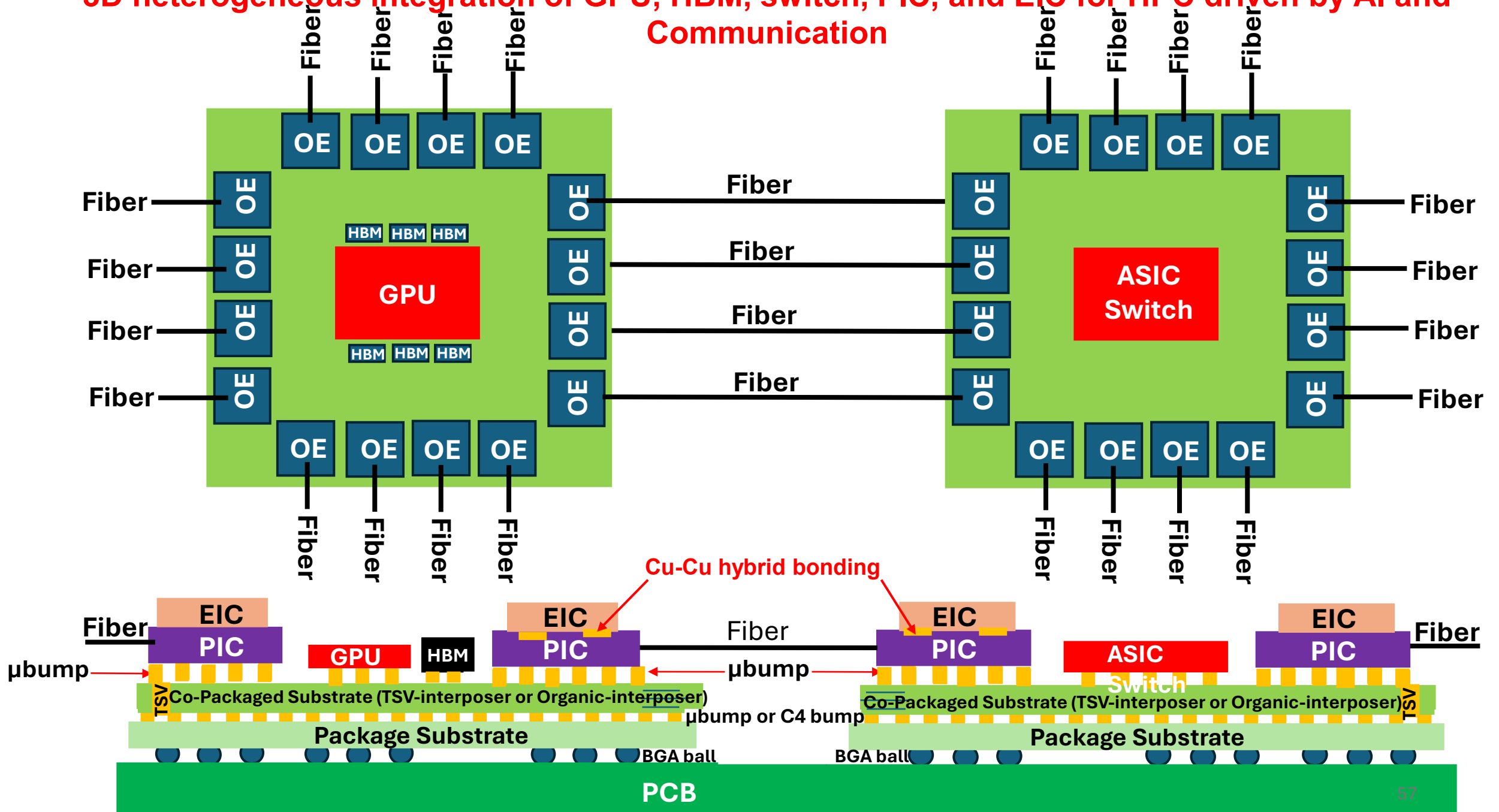
3D Heterogeneous Integration of PIC and EIC with Hybrid Bonding on Fan-out RDLs and Polymer Waveguides



3D Heterogeneous Integration of OE (EIC and PIC) and ASIC Switch on Embedded Polymer Waveguide and Organic Interposer



3D heterogeneous integration of GPU, HBM, switch, PIC, and EIC for HPC driven by AI and Communication



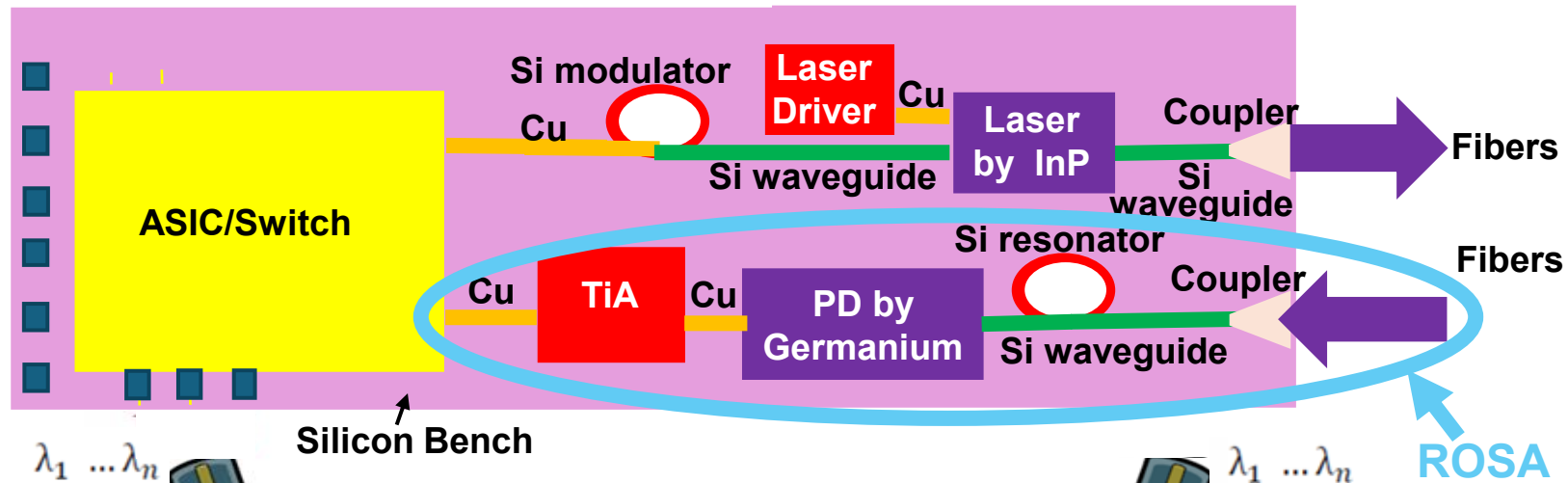
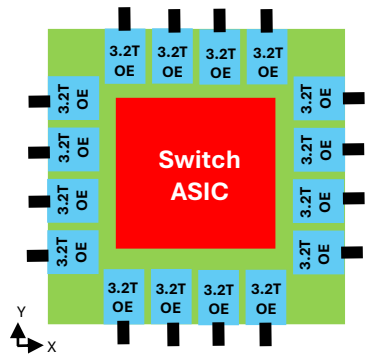
CPO with Silicon Photonic

- The silicon InP laser, silicon Germanium photodetector, silicon waveguides and silicon modulators/resonators are fabricated on a silicon wafer with CMOS technology.
- These elements enable high-speed, high-bandwidth, energy-efficient **optical interconnects** that overcome the **physical limitations of traditional copper wiring** in high-performance computing driven by artificial intelligence (AI) and data centers.
- **High volume manufacturing of CPO** with silicon photonic are expected as soon as in **2027**.
- **GlobalFoundries** acquired Advanced Micro Foundry (AMF) for their silicon photonic in **November 2025**.
- In the past few years, **TSMC** have been working on CPO with silicon photonic for their customers such as Broadcom and NVIDIA.

CPO with Silicon Photonic

Receiver Optical Sub-Assembly (ROSA)

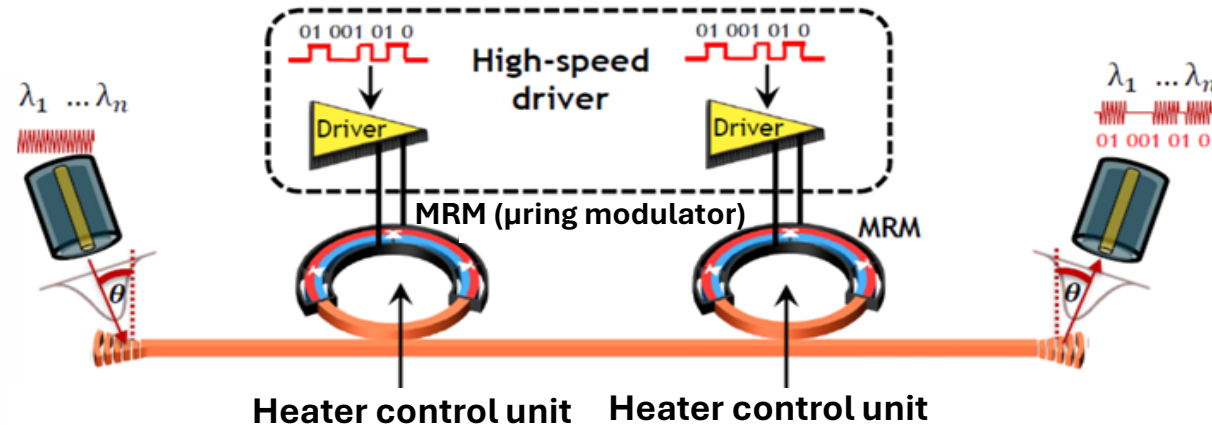
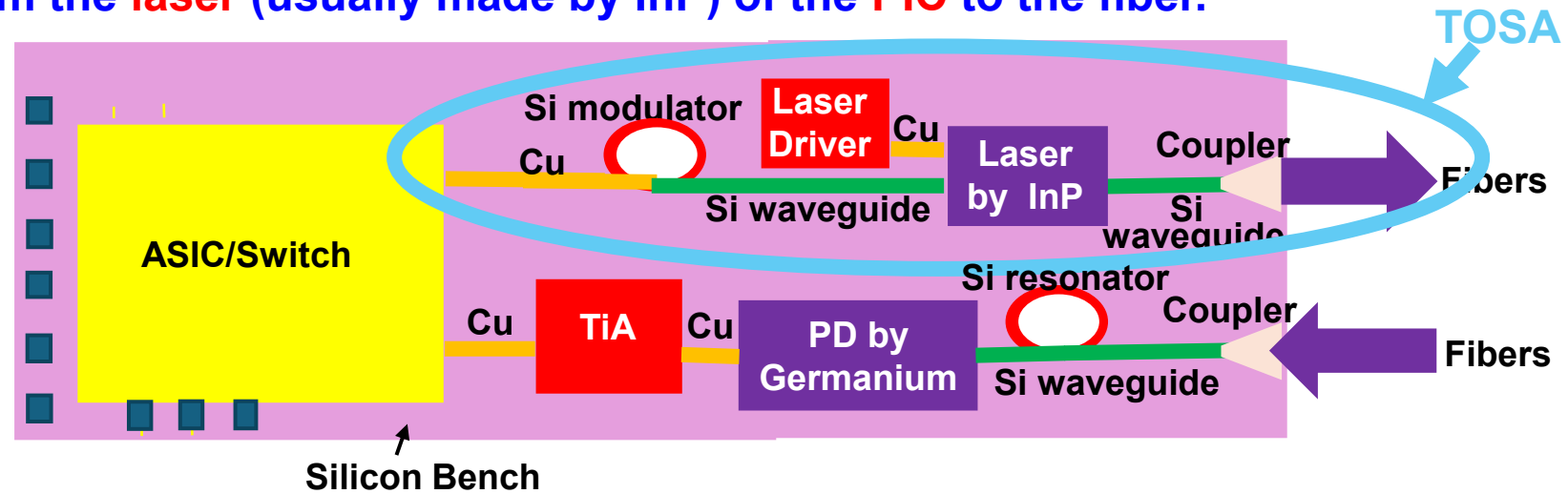
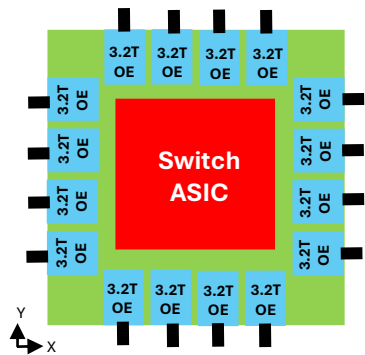
- The light from a fiber coupled to the **silicon waveguide** which confines the light.
- Then the **silicon resonator** (with Germanium) changes light to optical signal.
- Finally, the photodetector (**PD**), usually made by Germanium, of **the PIC** changes the optical signals to electrical signals, which are then amplified by the transimpedance amplifier (**TIA**) of **the EIC** before connected to the switch.



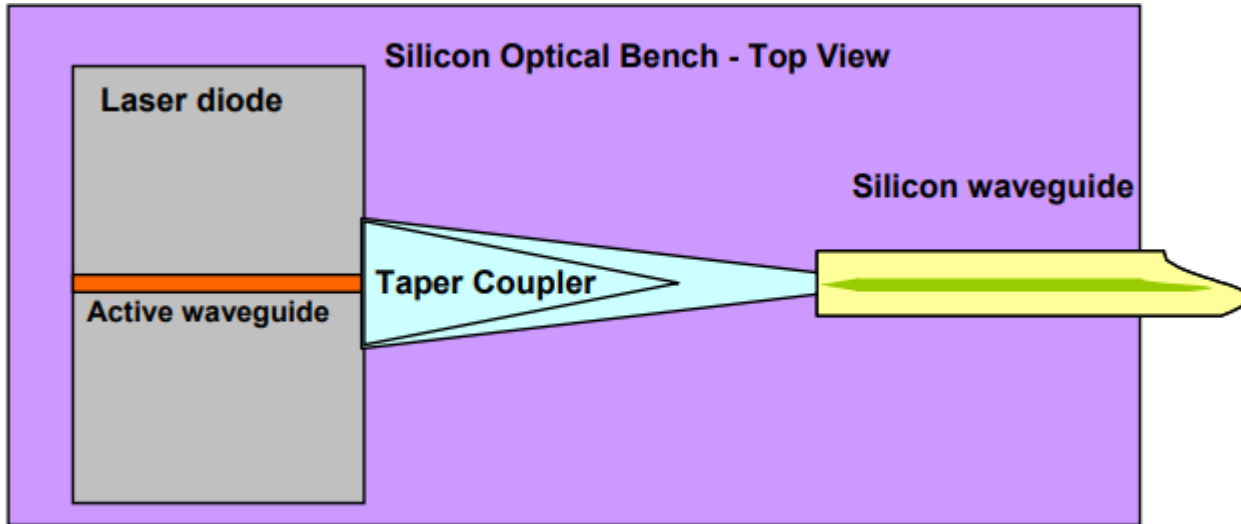
Wavelength division multiplexing

CPO with Silicon Photonic Transmitting Optical Sub-Assembly (TOSA)

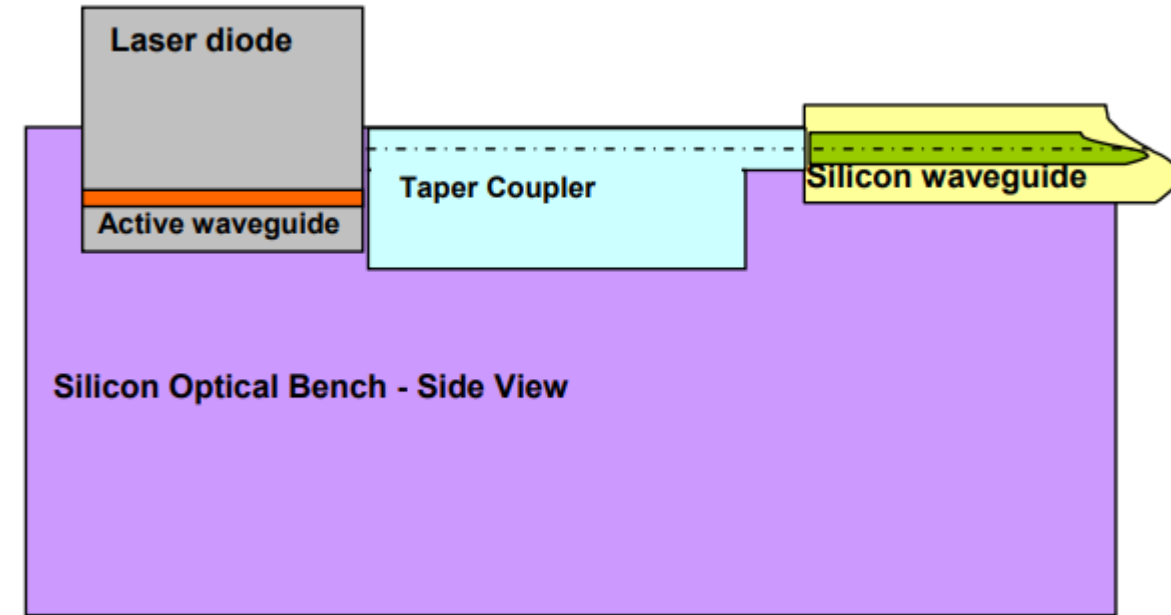
- ❑ The **silicon modulator** injects or depletes the electrons and holes (charge carriers) of the electrical signal (voltage) of the switch in the **silicon waveguide**.
- ❑ While the silicon modulator processes the data, the **laser driver** of the **EIC** is the power and control engine for the light source itself. It provides stable power supply and signal amplification before the light is shot out from the **laser** (usually made by InP) of the **PIC** to the fiber.



TAPER COUPLERS FOR COUPLING BETWEEN LASER AND SILICON WAVEGUIDE WITH LARGE ALLOWABLE TOLERANCE



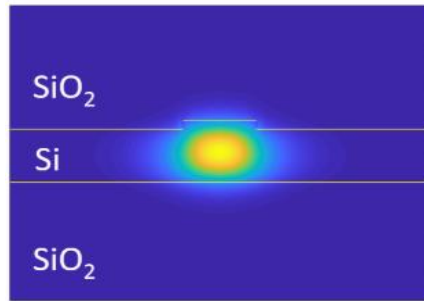
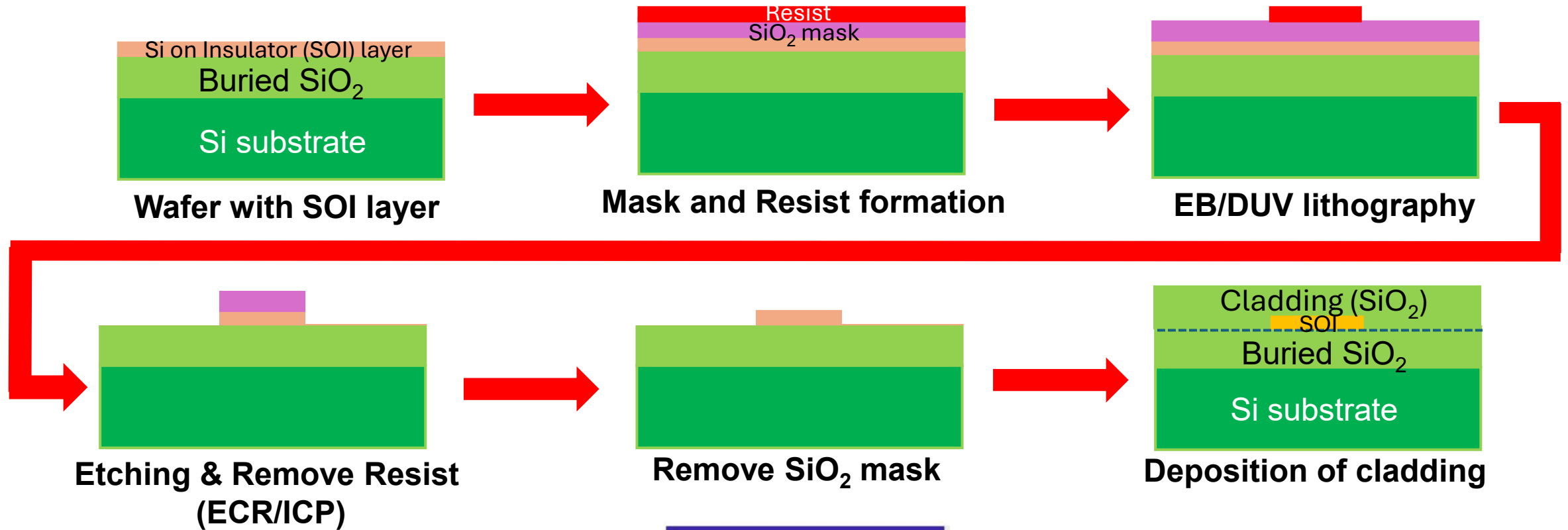
Top view of a taper coupler between laser diode and silicon waveguide



Side view of a taper coupler between laser diode and silicon waveguide

- [Jing Zhang, John H. Lau](#), et al., “Design and Characterization of Taper Coupler for Effective Laser and Single-Mode Fiber Coupling With Large Tolerance”, *Journal of IEEE Photonics Technology*, Vol. 20, No. 16, August 2008, pp. 1375-1377.
- [Jing Zhang, John H. Lau](#), et al., “Taper Couplers for Effective Coupling Between Laser and Silicon Waveguide with Large Allowable Tolerance”, *Proceedings of SPIE – Photonics Packaging, Integration, and Interconnects VIII*, San Jose, CA, January 19-24, 2008, Vol. 6899, pp. 09.1-09.6

Process Flow of Silicon Waveguide



EB (Electron Beam)
DUV (Deep Ultraviolet)
ECR (Electron Cyclotron Resonance)
ICP (Inductively Coupled Plasma)

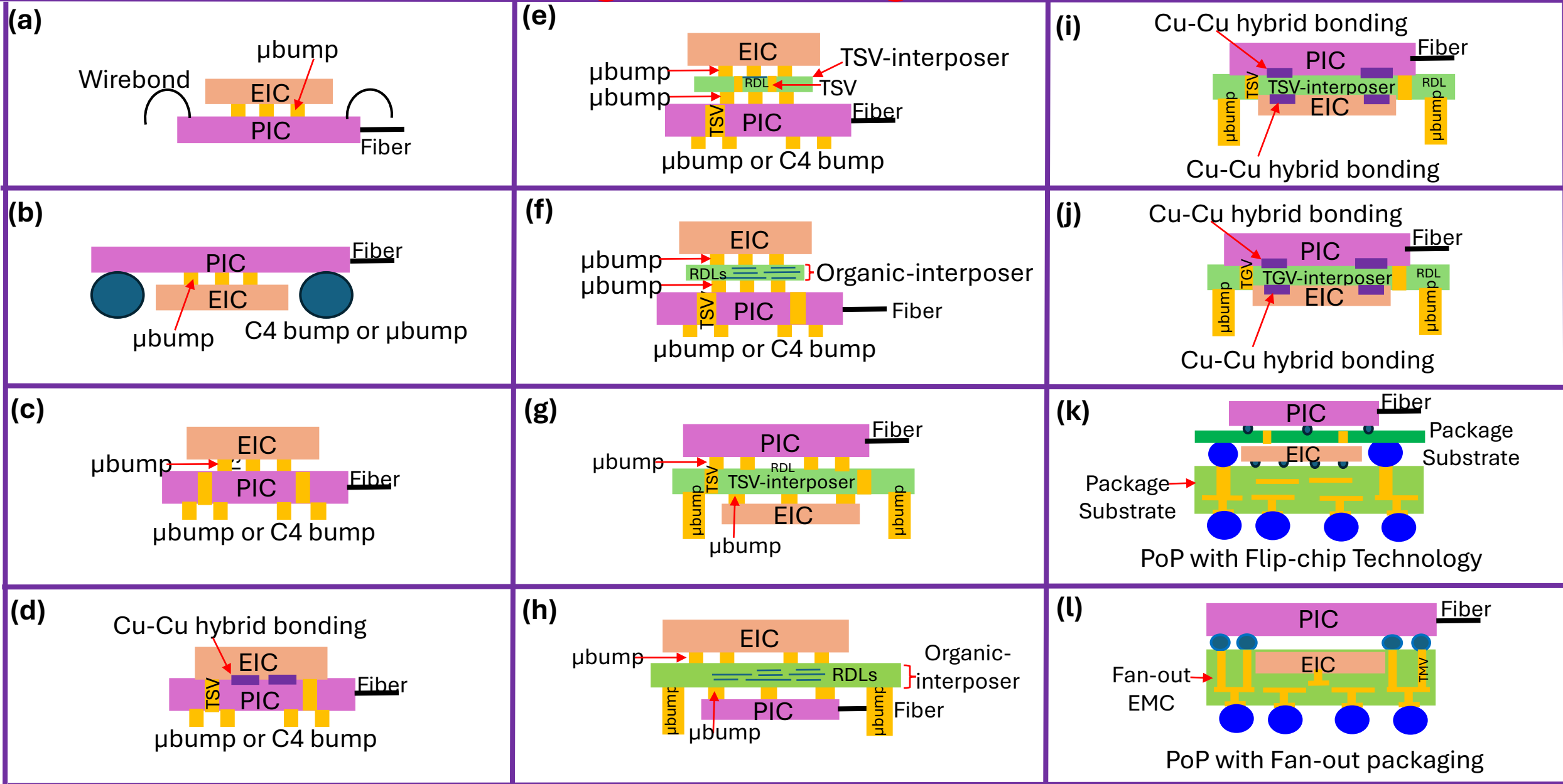
- [Jing Zhang, John H. Lau](#), et al., “Design and Characterization of Taper Coupler for Effective Laser and Single-Mode Fiber Coupling With Large Tolerance”, *Journal of IEEE Photonics Technology*, Vol. 20, No. 16, August 2008, pp. 1375-1377.
- [Jing Zhang, John H. Lau](#), et al., “Taper Couplers for Effective Coupling Between Laser and Silicon Waveguide with Large Allowable Tolerance”, *Proceedings of SPIE – Photonics Packaging, Integration, and Interconnects VIII*, San Jose, CA, January 19-24, 2008, Vol. 6899, pp. 09.1-09.6

SUMMARY

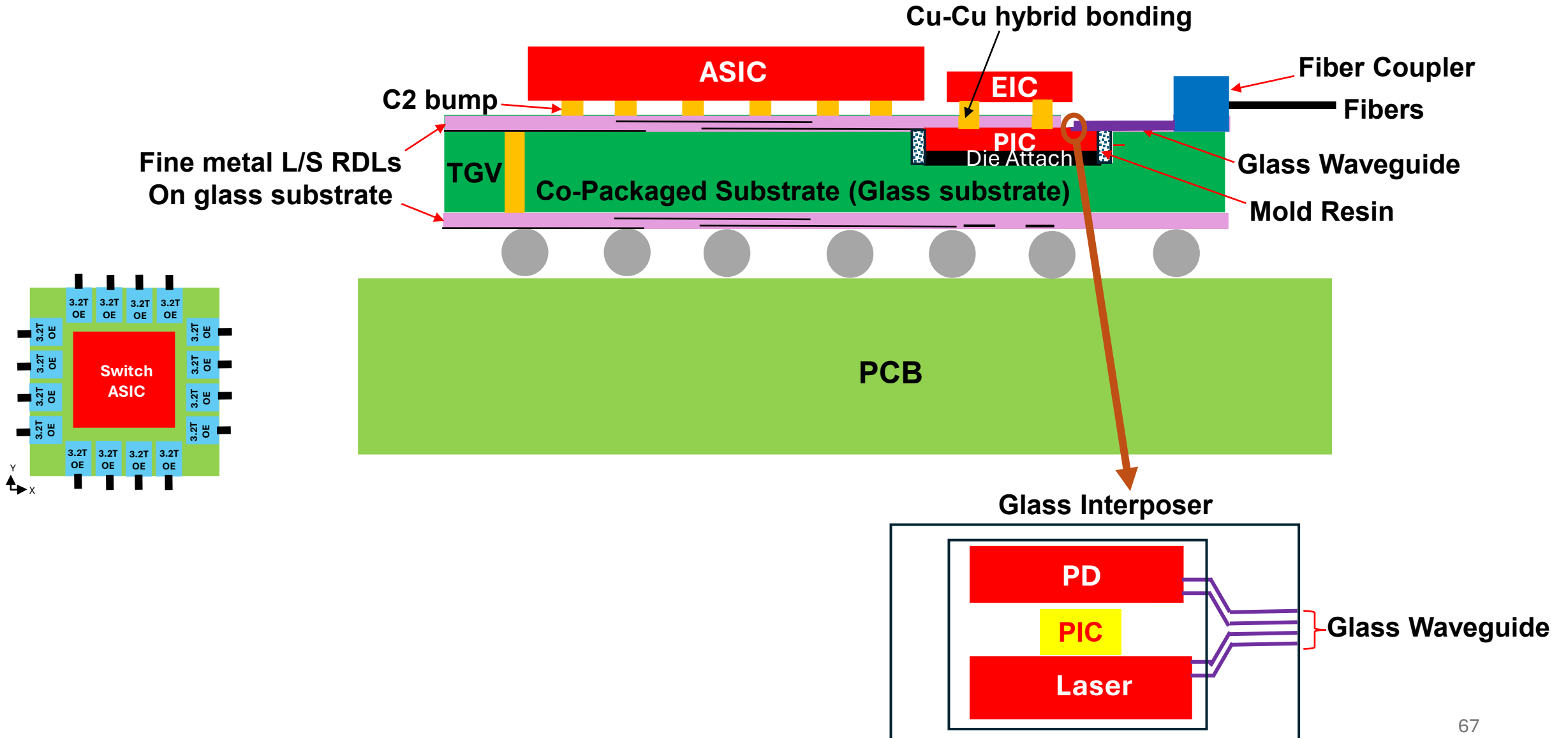
- CPO is the **heterogeneous integration** packaging method to integrate all the **chipllets**, such as the switch, PIC, EIC on a CPO substrate or interposer.
- **Thermal management** of 3D CPO will be an important topic.
- Because **glass** has a higher ability to seamlessly integrate optical interconnects, more use of the glass substrate or glass interposer for CPO is recommended.
- Due to the requirement of higher interconnect density, finer pitch, more compact 3D integration, lower power consumption, lower latency, higher bandwidth, and better signal integrity of a CPO system—the **Cu-Cu hybrid bonding** of some of the PICs and EICs are strongly recommended.
- In the past couple of years, because of the great demands of **lower power consumption, higher bandwidth and speed in the future artificial intelligence and data center environments**, **CPO with silicon photonic** is a very hot topic.
- For example, **companies in Taiwan (including TSMC)** are working around the clock so they can ship the CPO with silicon photonic products in **2027**.

Proposed R&D Problems

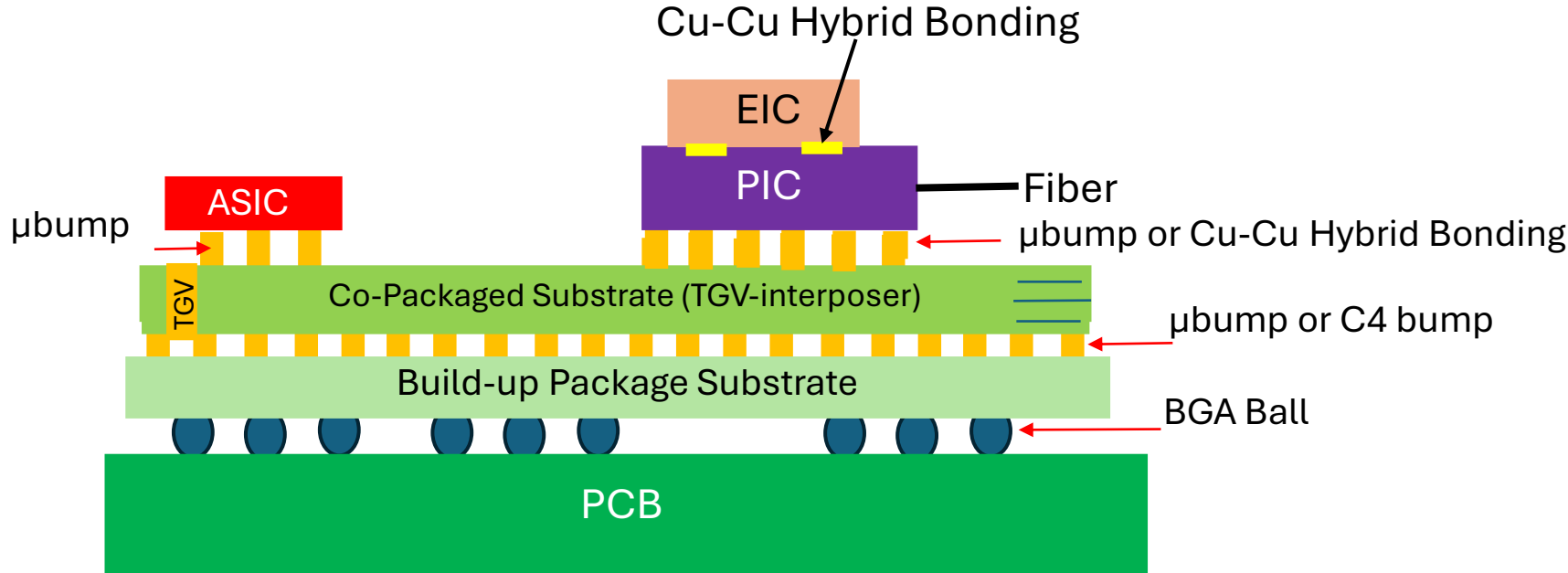
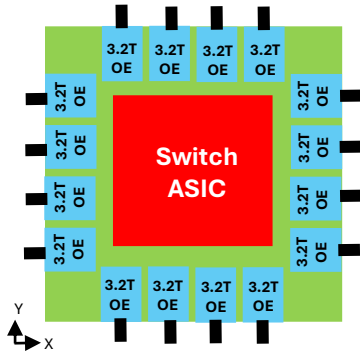
Various 3D Heterogeneous Integration of PIC and EIC



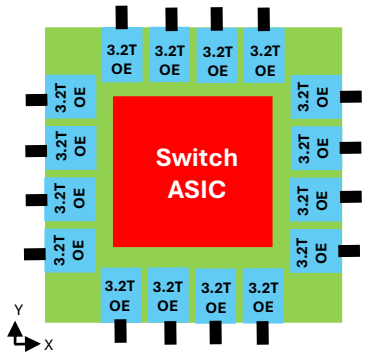
More use of CPO on Glass-core Substrates



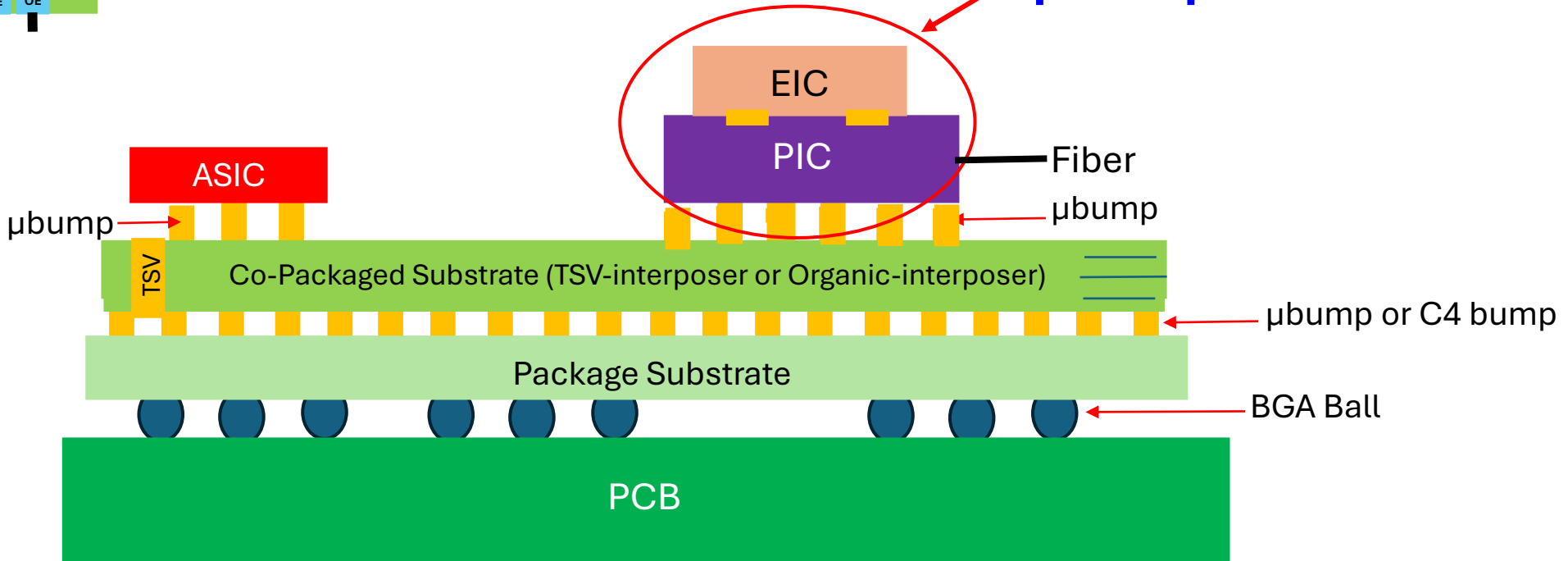
More use of CPO on Glass-Interposer (3.5D IC Integration)



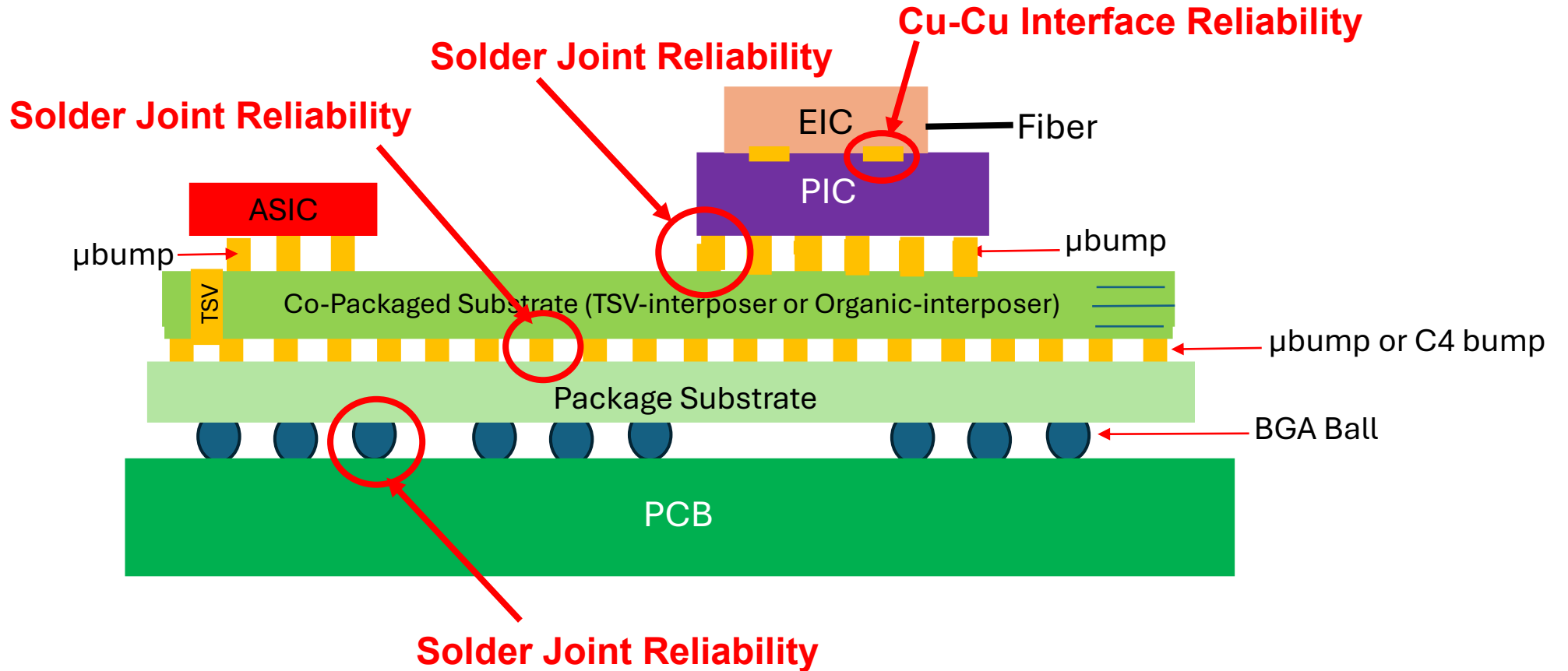
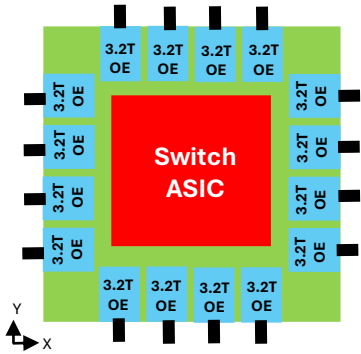
Thermal Management of 3.5D Heterogeneous integration of PIC and EIC



How to take the heat out before it affects to the electrical and optical performance?



Reliability of 3.5D Heterogeneous Integration of PIC and EIC



Some Recent Advanced Packaging Papers Published by the Lecturer and his Colleagues

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4. Lau, J. H., N. Liu, M. Ma, and T. Tseng, “Solder joint reliability - glass core substrate versus organic core substrate”, *Journal of Microelectronic Reliability*, Vol. 168, May 2025, pp. 115701.
5. Lau, J. H., “Current Advances and Outlooks in Hybrid Bonding”, *IEEE Transactions on CPMT*, Vol. 15, No. 3, March 2025, pp. 651-681.
6. Lau, J. H., “Co-Packaged Optics - Heterogeneous Integration of Photonic IC and Electronic IC”, *ASME Transactions, J. of Electronic Packaging*, published online June 20, 2024, Vol. 147, March 2025, pp. 1-12.
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17. Lau, J. H., C. Ko, C. Lin, et al., “Fan-Out Panel-Level Packaging of Mini-LED RGB Display”, *IEEE Transactions on CPMT*, Vol. 11, No. 5, May 2021, pp. 739-747.
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29. Peng, C., J. H. Lau, C. Ko, et al., “High-Density Hybrid Substrate for Heterogeneous Integration”, *IEEE Transactions on CPMT*, Vol. 12, No.3, March 2022., pp. 469-478.
30. Lee, Z., J. H. Lau, C. T. Ko, et al., “Characterization of Low-Loss Dielectric Materials for High-Speed and High-Frequency Applications”, *Materials Journal*, 15, 2022, pp. 1-16.
31. Ko, C. T., H. Yang, Lau, J. H., et al., “Chip-First Fan-Out Panel Level Packaging for Heterogeneous Integration”, *IEEE Transactions on CPMT*, 2018, Vol. 8, Issue 9, September 2018, pp. 1561-1572.

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2. Lau, J. H., and X. Fan, *Hybrid Bonding, Advanced Substrates, Failure Mechanisms, and Thermal Management for Chiplets and Heterogeneous Integration*, Springer, New York, April 2025.
3. Lau, J. H., *Flip Chip, Hybrid Bonding, Fan-in, and Fan-out Technology*, Springer, New York, 2024.
4. Lau, J. H., *Chiplet Design and Heterogeneous Integration Packaging*, Springer, New York, 2023.
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18. Lau, J. H., and Y. Pao, *Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies*, McGraw-Hill, New York, 1997.
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24. Lau, J. H., (editor) *Handbook of Tape Automated Bonding*, Van Nostrand Reinhold, New York, November 1992.
25. Lau, J. H., (editor) *Solder Joint Reliability: Theory and Applications*, Van Nostrand Reinhold, New York, April 1991.

**Thank You Very Much for Your
Attention!**

