The Applications of Simulation and Artificial Intelligence in Advanced Packaging

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Outline

- Introduction
- AI Applications in Advanced Packaging Co-Design
- AI Applications in Advanced Packaging Process Simulation and Monitoring
- AI Applications in Yield Enhancement and Reliability Risk Assessment of Advanced Packaging
- AI Applications in Failure Analysis of Advanced Packaging
- Conclusions

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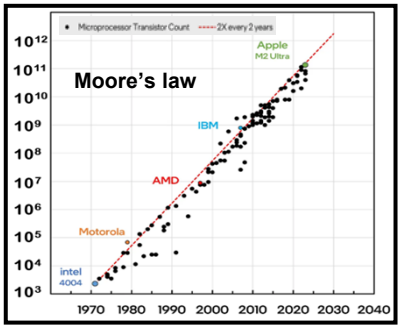
Introduction

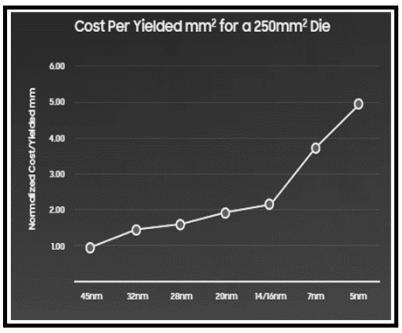
Why advanced packaging?

Advanced packaging techniques are utilized to meet the market needs



Moore's law predicts the exponential growth of ICs since 1970s---***Market needs***

https://semiconductor.substack.com/p/the-relentless-pursuit-of-moores



The exponential growth of cost per Yielded mm^2 for 250 mm^2 die ----***Challenges for Si level scaling and yielding***

- **Chiplet**
- **Heterogeneous integration**
- **Die stacking**

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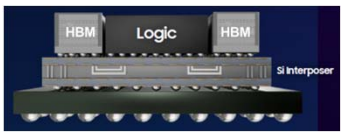
Introduction

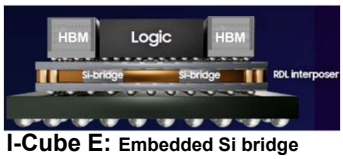
Advanced packages on market

https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=10195617

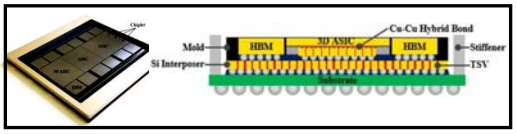
Smaller interconnects; Higher performance; Lower power consumption



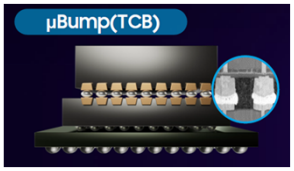
I-Cube S: Si interposer from Samsung



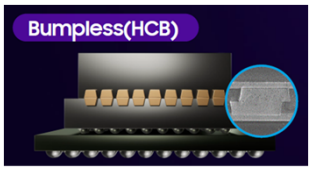
I-Cube E: Embedded Si bridge RDL interposer from Samsung



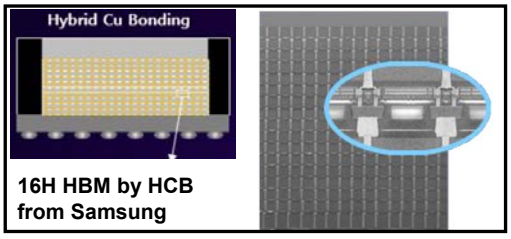
3.5D packaging hybrid bonding 3D chips on Si interposer from Samsung



X-Cube: logic to logic die stacking- µBump from Samsung



X-Cube: logic to logic die stacking- Hybrid Cupper Bonding Samsung



16H HBM by HCB from Samsung

W. Kim, "Advanced Packaging in the Era of HPC and AI" Seventh Annual Symposium on Heterogeneous Integration, February, 2024.
https://ieeetv.ieee.org/video/heterogeneous-integration-platform-for-next-generation-computing-beyond-moore

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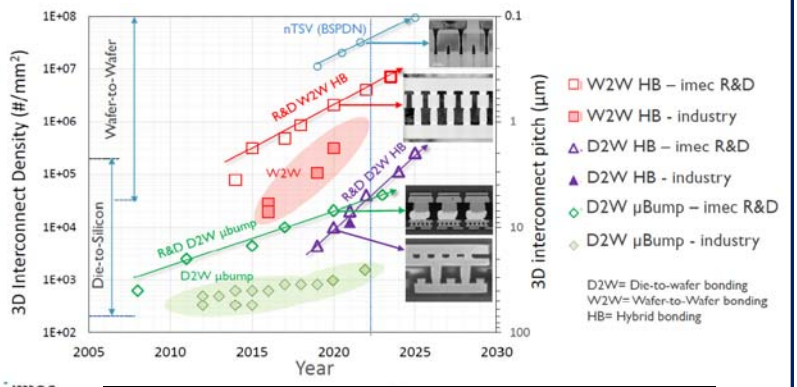
Introduction

The Boundary between Si and Advanced Packaging is blurring

Dramatic scaling down of interconnects in 3D Packaging



- ✓ **Design**
- ✓ **Process**
- ✓ **Yield & Reliability**
- ✓ **Failure Analysis**

Adopting well-developed **methodologies** currently used in **Si Fabs** to advanced packaging area is **imperative** to meet the short product development cycle demands

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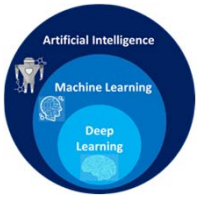
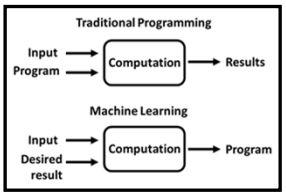
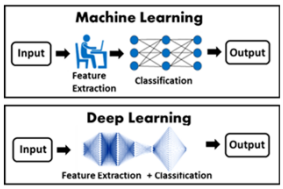
Introduction

Artificial Intelligence (AI), Machine Learning (ML), and Deep Learning (DL)







- ✓ **ML based Chip design, Si Fab process simulation** and **control**, as well as **yield and reliability prediction** have been demonstrated as efficient methodologies to tackle complex design and process challenges.
- ✓ **DL** has successful applications in **defect detection and classification** in **semiconductor manufactory**
- ✓ **The Adoption** of **similar methodologies** proven to be effective **in Si Fabs to Advanced Packaging** area is one of the efficient approaches to help address challenges and reduce product development cycle time.

S. Lubin et al, "Design-aware virtual metrology and process recipe recommendations" Proc. Of SPIE Vol. 12495, DTCO and Computational Patterning II, 124951V (28 April 2023).
G. Tello, O. Y. Al-Jarrah, P.D. Yoo, Y. Al-Hammadi, S. Muhaidat, and U. Lee, "Deep-Structured Machine Learning Model for the Recognition of Mixed-Defect Patterns in Semiconductor Fabrication Processes", IEEE Transactions on Semiconductor Manufactoring, VOL. 31, NO. 2, May 2018.

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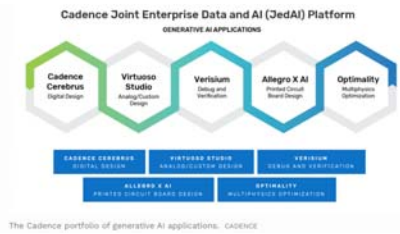
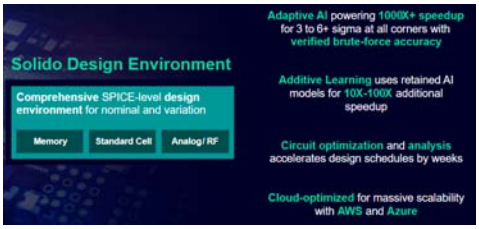
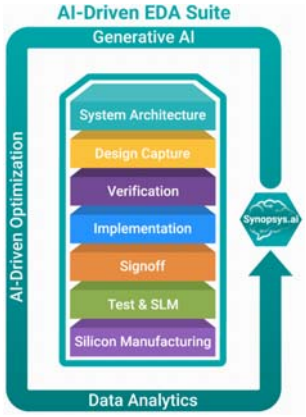
AI Applications in Advanced Packaging Co-Design

Chip Co-Design AI based platforms

EDA tool vendors, such as **Synopsys, Cadence design systems,** and **Siemens** have provided ML and DL based EDA platforms for IC designers. Additionally, EDA tool vendors and many hyperscale chip designers are now adopting **generative AI capabilities** to facilitate chip design







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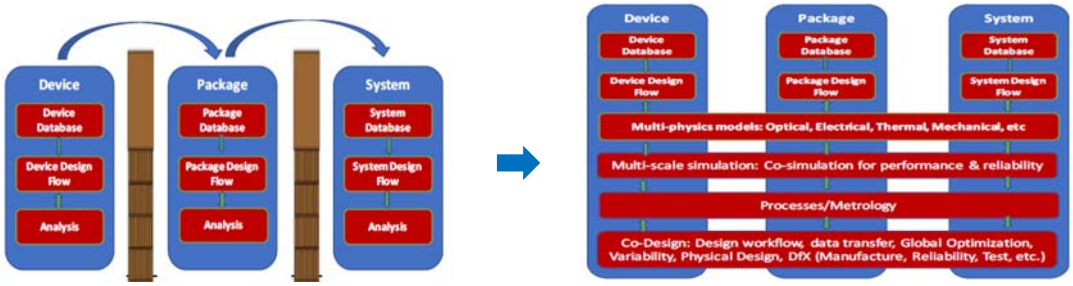
AI Applications in Advanced Packaging Co-Design

AI based EDA platforms for package co-design are desired

Similar Methodology used in chip Co-Design has been adopted for 3D IC (chip) Co-design, further development in Package Co-design is needed.



Effective system optimization at design stage is highly desired

- Robust modeling and simulation to accurately **predict the electro-thermal and thermo-mechanical coupling across multi-domains** within a co-design optimization environment
- Accurate simulation methodologies to forecast the **thermo-mechanical stress** across multi-domain as well as **die and substrates warpage** during assembly process and reliability tests

Heterogeneous integration roadmap, Chapter 13: "Co-Design for Heterogeneous Integration", 2021, https://eps.ieee.org/hir.

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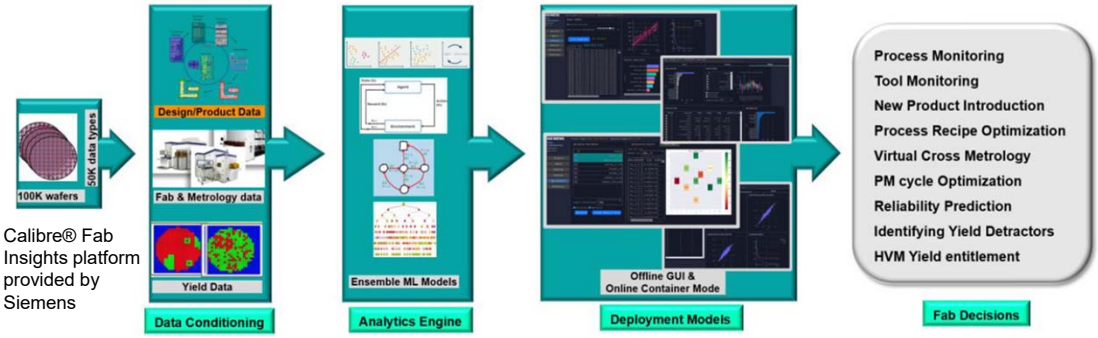
AI Applications in Advanced Packaging Process Simulation and Monitoring

Machine learning based infrastructures in Si Fab Process simulation & Monitoring:

- ✓ **Front-end lithography Process**
- ✓ **High Aspect Ratio Process (HARP)**
- ✓ **Inline Virtual Metrology (VM)**



Calibre® Fab Insights platform provided by Siemens

S. Jayaram, "Enabling smart manufacturing in semiconductor fabs using predictive design and process insights," Semicon Europa, November 2023

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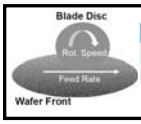
AI Applications in Advanced Packaging Process Simulation and Monitoring

Similar ML based infrastructures and concepts can be used in the process simulation and monitoring of advanced packaging.

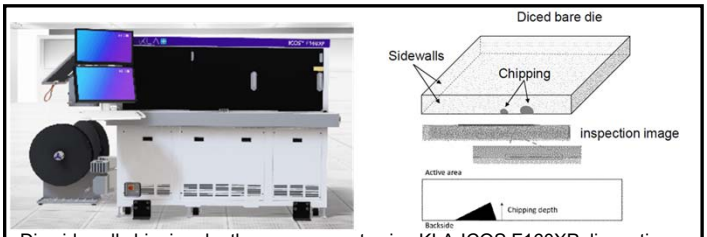
Wafer Dicing ML model built with very limited input data



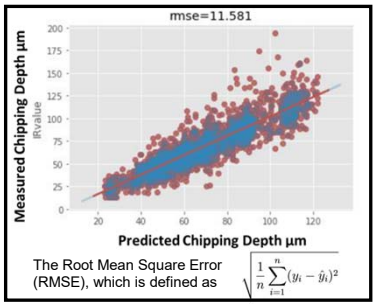
Conditions	1	2	3	4	5	6	7	8	9
Spindle speed (rpm)		30000			50000			40000	
Feed rate (mm/s)	5	10	25	25	10	5	5	10	25

Table 1. wafer dicing conditions

- **Accurate for first order predictions**
- **More input data to further improve the model.**
- **Adopt to any other assembly steps**



Die sidewall chipping depth measurement using KLA-ICOS F160XP die sorting and inspection system.



The Root Mean Square Error (RMSE), which is defined as $\sqrt{\frac{1}{n}\sum_{i=1}^{n}(y_i - \hat{y}_i)^2}$

M. Bahnas et al, "ML-based Optimization for High Precision Wafer Dicing Process", APCSM Conference 2021

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AI Applications in Yield Enhancement and Reliability Risk Assessment of Advanced Packaging

Deep Topological Data Analysis (DTDA) clusters and models the data in the form of geometric objects, **reduces the multidimensional dataset to two-dimensional networks or graphs**

DTDA **provides insights** to conduct accurate analysis and helps engineers **identify the features contributing to yield and quality issues, enabling corrective actions.**

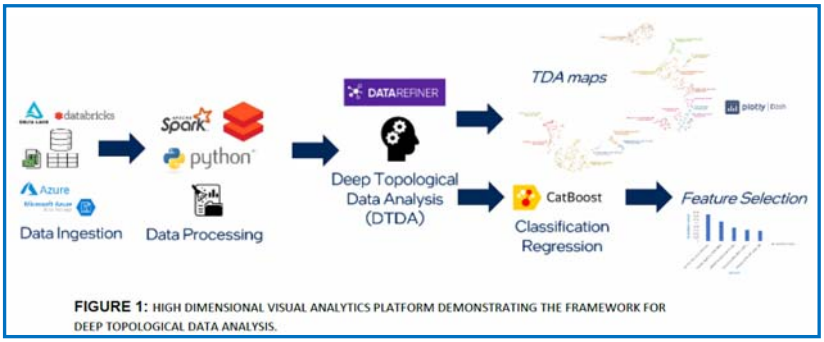

FIGURE 1: HIGH DIMENSIONAL VISUAL ANALYTICS PLATFORM DEMONSTRATING THE FRAMEWORK FOR DEEP TOPOLOGICAL DATA ANALYSIS.

- **DTDA in Si Fab yield analysis**
- **Adopt in Advanced Packaging yield analysis**

J. Giri, and A. Iengyel, "Explainable machine learning approach to yield and quality improvements using deep topological data analytics", Proceedings of the ASME 2023 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems (InterPACK), October, 2023, San Diego, California.

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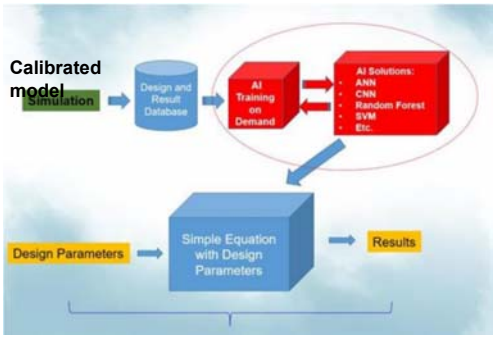
AI Applications in Yield Enhancement and Reliability Risk Assessment of Advanced Packaging

Combining AI with Finite Element Analysis (FEA) simulation for Wafer Level Packaging (WLP) Reliability Prediction



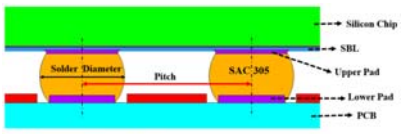


Figure 6. WLP geometry structure.

Table 7. Training data 1296 of FEM for four input features.

Feature Name	Level (mm)
Upper Pad Diameter	0.18, 0.19, 0.20, 0.21, 0.22, 0.23
Lower Pad Diameter	0.18, 0.19, 0.20, 0.21 0.22, 0.23
Chip Thickness	0.20, 0.25, 0.30, 0.35, 0.40, 0.45
Stress Buffer Layer Thickness	0.0075, 0.0125, 0.0175, 0.0225, 0.0275, 0.0325
Total Number	1296

Table 8. WLP finite element results for five test vehicles.

Test Vehicle	Experimental Reliability (Cycles)	Simulation Reliability (Cycles)	Difference
TV1	318	313	−5
TV2	1013	982	−31
TV3	587	587	0
TV4	876	804	72
TV5	904	885	19

- **Five Test Vehicles (TV) to calibrate the FEA model.**
- **Calibrated FEA model generates Design and results database for AI training**
- **Various AI solutions evaluated and find the best AI solution for the AI model**
- **Customer input design parameters, and get the predicted reliability results within seconds.**

S. K. Panigrahy, Y. C. Tseng, B. R. Lai, and K. N. Chiang, "An Overview of AI-Assisted Design-on-Simulation Technology for Reliability Life Prediction of Advanced Packaging", Materials, Vol. 14, pp. 5342, https://doi.org/10.3390/ma14185342, Sept. 2021.

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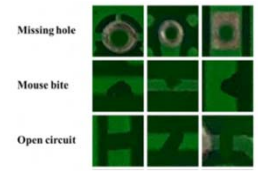
AI Applications in Failure Analysis of Advanced Packaging

Why AI?

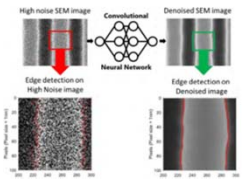
- Enable high volume FA support on complex packages
- Cost saving;
- Reduce Through Put Time

Current applications

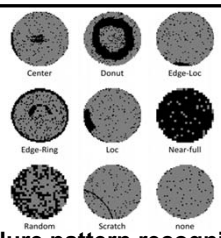
- Defect identification and classification;
- Noise mitigation in microscopy images;
- Failure mode recognition by clustering and pattern detection;
- Failure report classification and failure mode prediction



Defect detection and classification



Noise reduction in SEM/TEM/SAM images



Failure pattern recognition

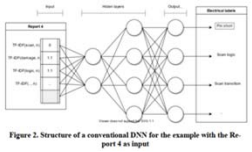


Figure 2. Structure of a conventional DNN for the example with the Report 4 as input

Failure Analysis report Classification and Failure mode prediction

C. Schmidt et al, "Package Innovation Roadmap", Electronic Device Failure Analysis Technology Roadmap, ASM International, 2023. ISBN electronic: 978-1-62708-462-8, DOI: https://doi.org/10.31399/asm.tb.edfatr.9781627084628

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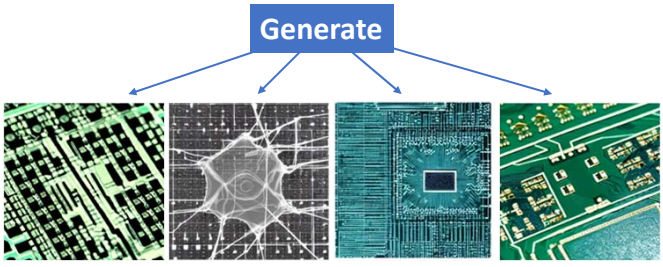
AI Applications in Failure Analysis of Advanced Packaging

Challenges

- How to **normalize** and **share training data** for generic failure modes.
- How to **develop AI algorithms** without hundreds or **thousands** of **training datasets.**



Future Trends

- **Assisting FA data collection and performing full FA**
- **Training new FA engineers**
- **Generation or modification of detailed measurement data from rare failure modes of different samples**
- **Automatic FA report generation and evaluation**

C. Schmidt et al, "Package Innovation Roadmap", Electronic Device Failure Analysis Technology Roadmap, ASM International, 2023. ISBN electronic: 978-1-62708-462-8, DOI: https://doi.org/10.31399/asm.tb.edfatr.9781627084628

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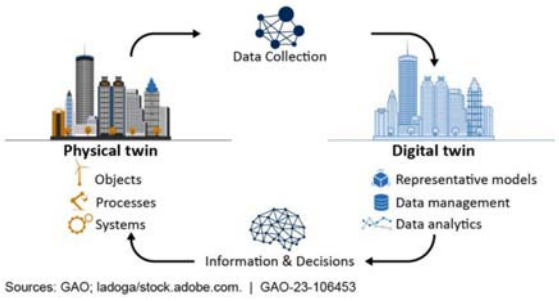
Conclusion

- **Adopting well-developed AI based methodologies currently used in Si Fabs to advanced packaging area is imperative**
- **AI applications in Design, Process Simulation & Monitoring, Yield, Reliability and FA**
- **Future Development Trends**



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