Advancing Opto-Electronics With Thermo-Electric Technology

IEEE – Silicon Valley Area Chapter

Mark Smitt | August 22nd, 2024

Thermoelectric Fundamentals

Thermoelectric Device Fundamentals

- Known as Thermoelectric Coolers ("TEC"), Modules ("TEM"), or Devices ("TED")
    - Phononic internal nomenclature is "TEM"

- Solid state heat pump
    - Primary function is to convert Electrical Work  Heat Flow

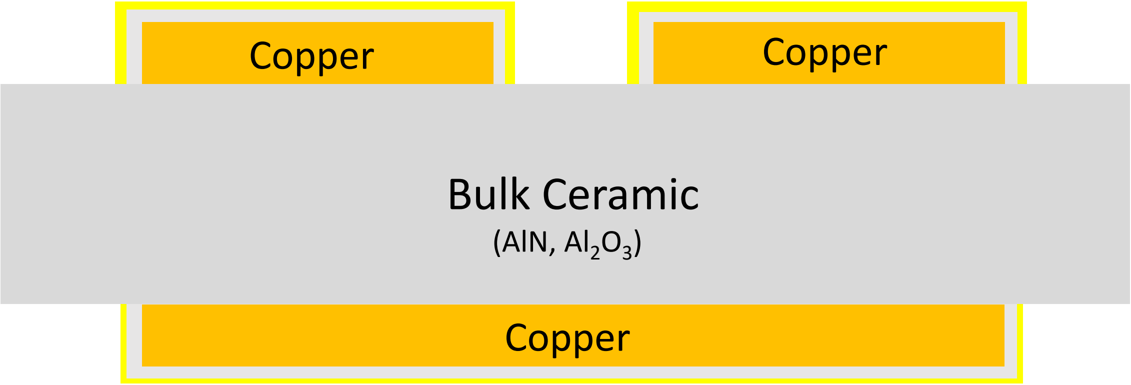
- Direct conversion of a temperature difference to electric current and vise versa through the Seebeck and Peltier effects ($S = {}^{\Delta V}/_{\Delta T}, \pi = ST$)

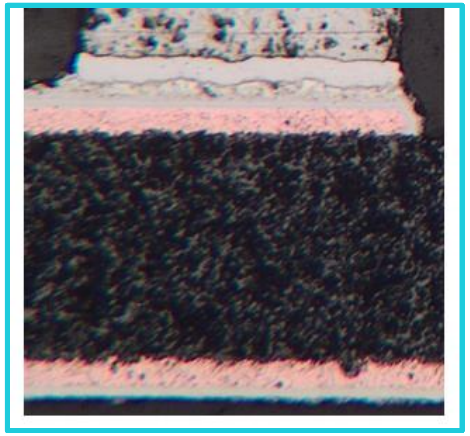
- Three primary components:
    1. Thermoelectric Elements
    2. Substrates
    3. Solder

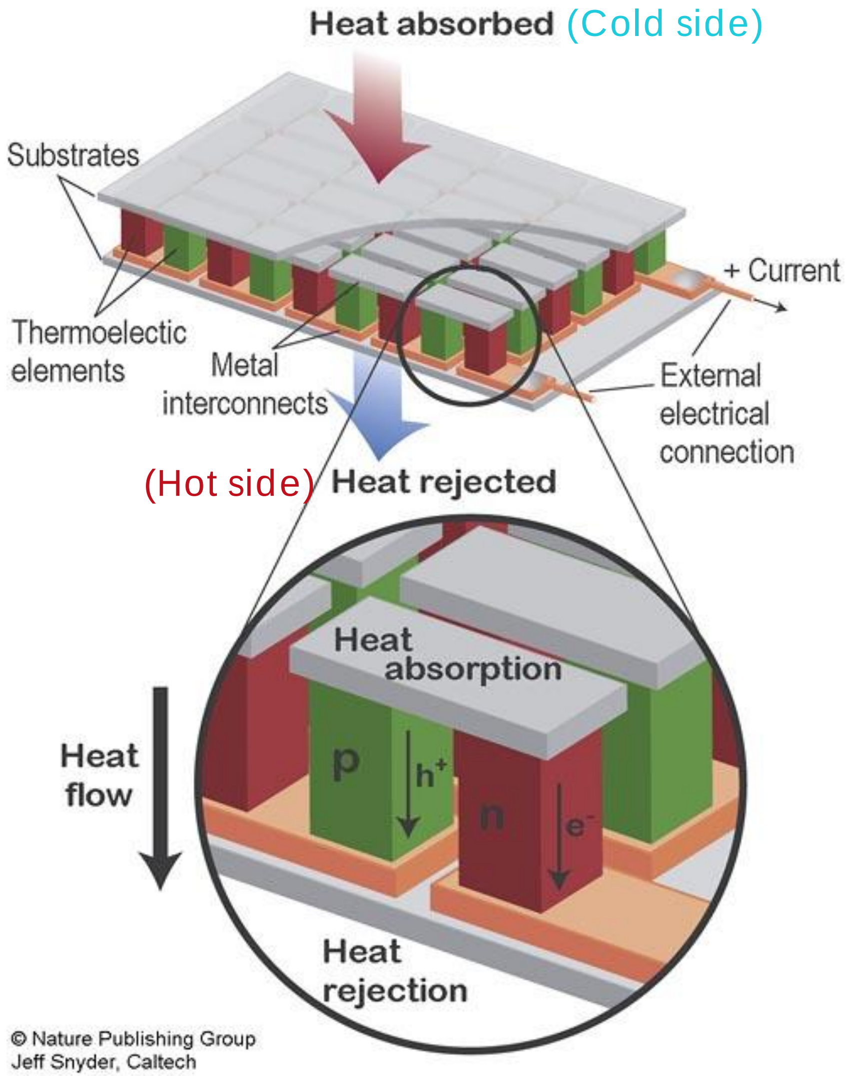
- Other components or features can be added!

Substrates

- Ceramic panels with patterned metallization (“headers”)
  - Top Header (“TH”), typically the Cold Side
  - Bottom Header (“BH”), typically the Hot Side
- Desired substrate material properties:
  - High thermal conductivity – in the heat transfer path
  - Electrical insulation
  - Mechanical robustness
- Typical Phononic construction:
  - Electroplated copper conductor
  - Electroless nickel, electroless palladium, immersion gold (“ENEPIG”)

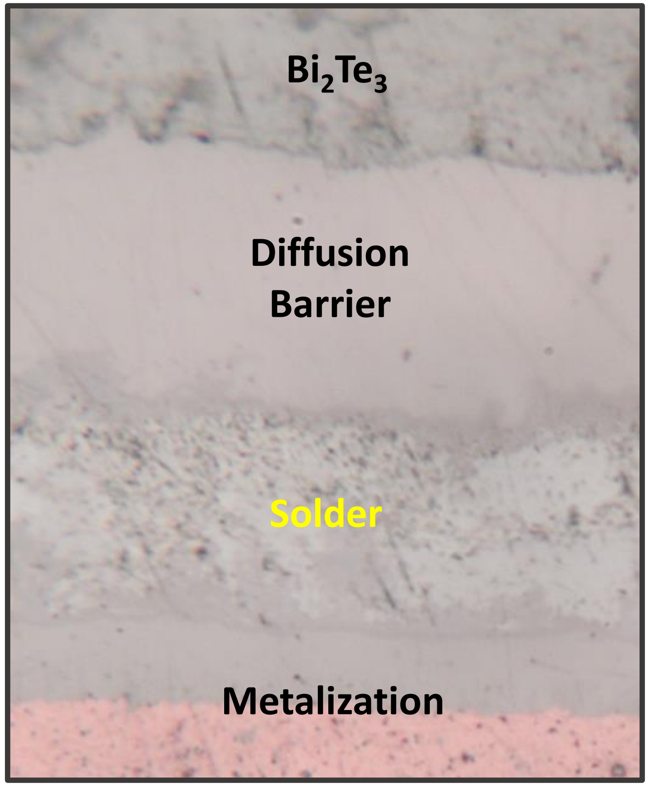




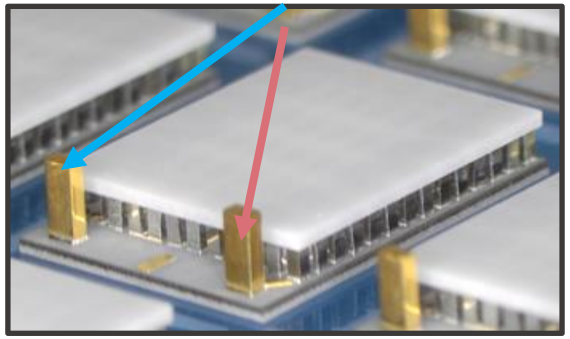


Solder and Other Features

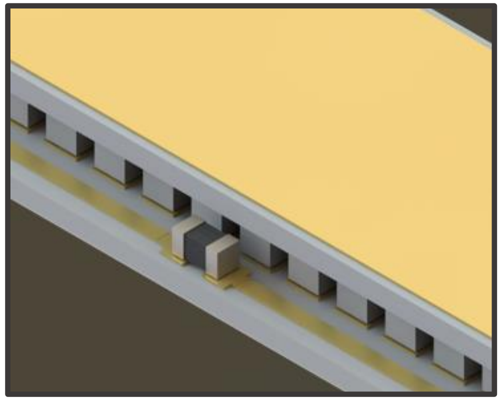
- Bonds elements to metalized ceramics
- Primary considerations:
  - Material compatibility (Ag, Cu negatively impact Bi_2Te_3 properties)
  - Aligned with customer integration process (e.g. low MP BiSn)
  - Manufacturing process
  - Regulatory (RoHS, REACH) compliance (Pb-free)
- Solder of choice: SnSb (240°C)
  - AuSn (280°C) is available as a higher temperature alternative
- Phononic can also integrate other components during TEC assembly
  - Bonding Posts: enable wire bonding in deep package applications
  - Thermistor
  - Other SMT components



Posts



Thermistor



Anatomy of a TEC

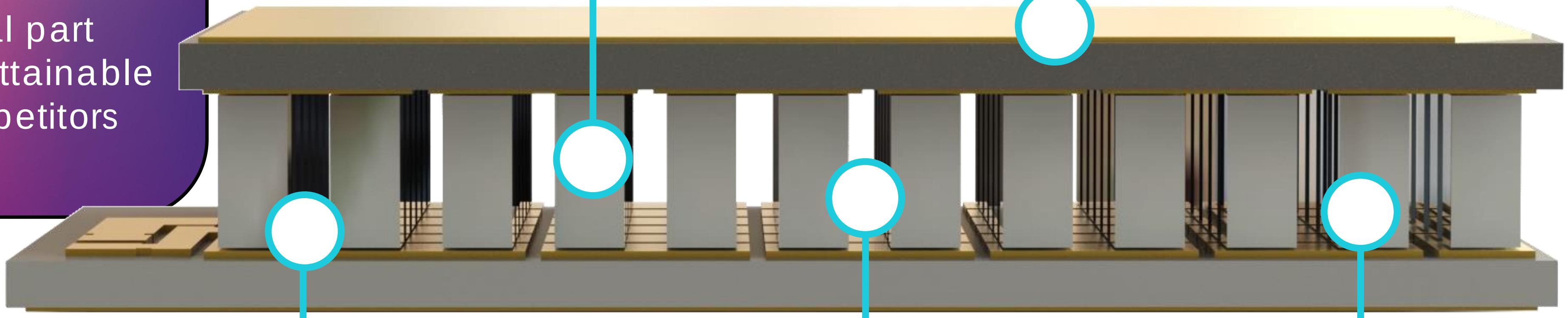
Phononic's approach to TEM manufacturing enables designs, performance levels and annual part volumes not attainable by our competitors

Thermoelectric materials

High performance, mechanically robust, enables ultra-thin devices (<700um), extremely high heat pumping flux and/or efficacy

Custom metal patterning

Metallization layouts to suit your package design



Ultra-thin substrates

Minimize thermal resistance, increase TEC ΔT_{MAX}

Hyper-dense element packing

Enables higher power lasers in smaller package footprints

Superior contact metallization

Industry-leading contact resistance, high reliability, excellent solderability

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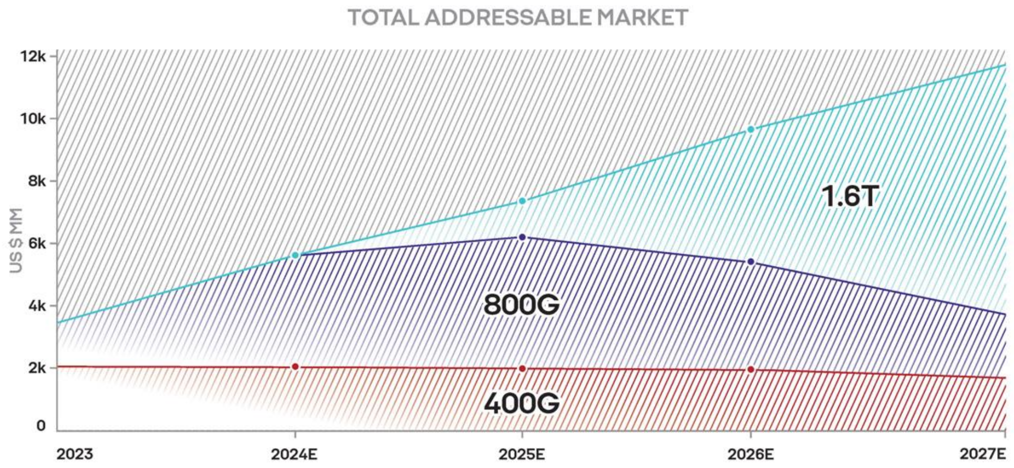
Applications

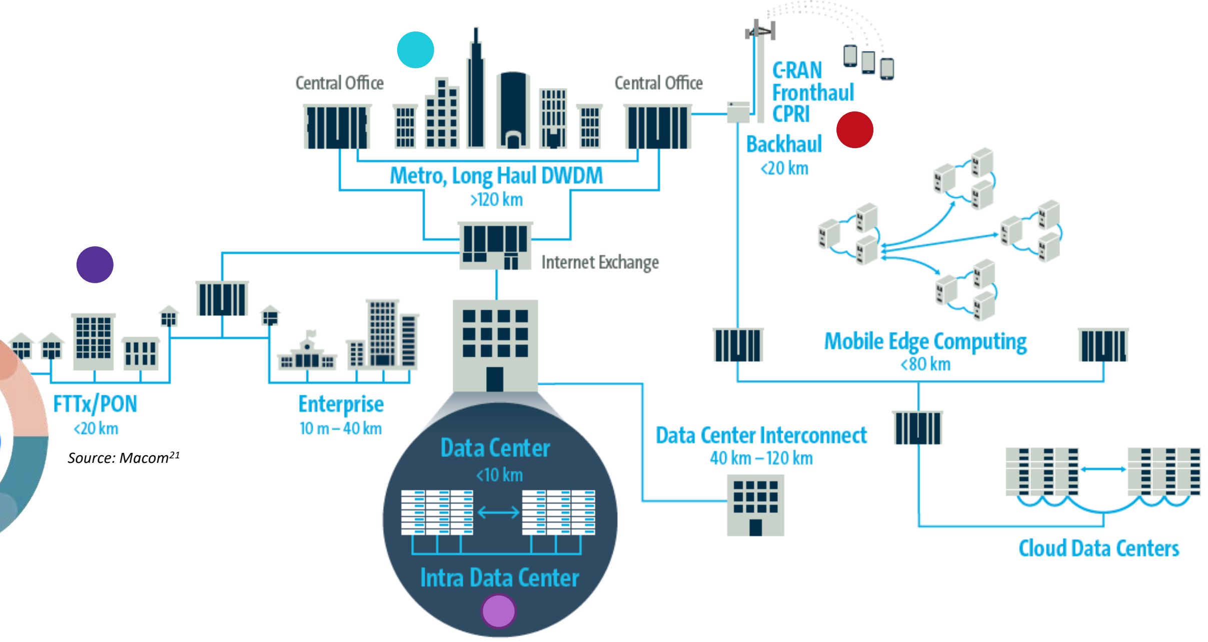
Datacenter & Fiber Optic Solutions

Optical Transceiver Market Trajectory



Source: Goldman Sachs Global Investment Research

Network Communications Equipment: Where We Cool



- Telecom: transport equipment; Cisco, Nokia, Ciena & Infinera drive Phononic customers
- Access: fiber-to-the home; China Telecom, ATT & Verizon driving deployment
- Datacenter: optically connecting servers/switches; Google, Facebook, Amazon, Arista
- Wireless: 5G expected to move to 'cooled' optics as bandwidth needs increase

Market Applications

Optical Transceivers

Datacenter Cooling

LiDAR

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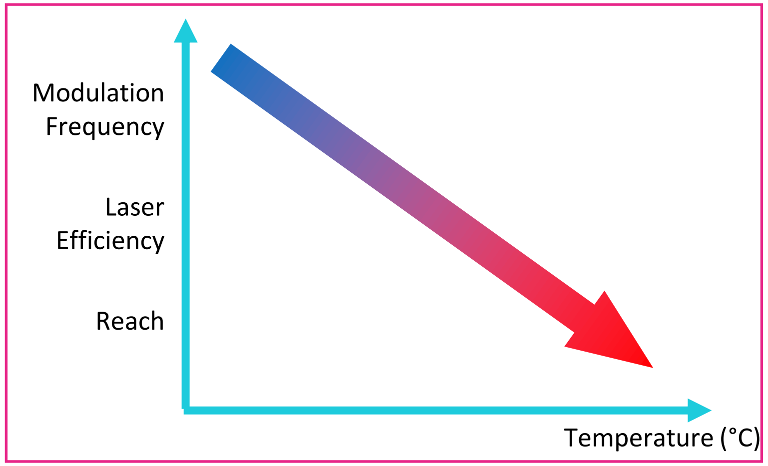
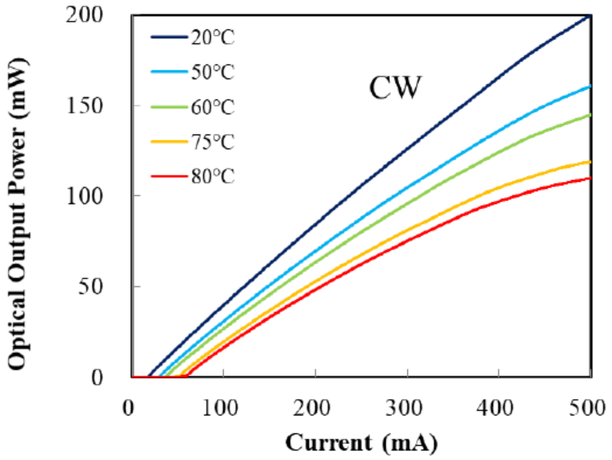
Cooled Optics

- Light Sources – Use cases: Wavelength(s) / bandwidth / reach
  - VCSEL – Inexpensive, very low power, typically uncooled
  - DML/DFB – up to ~200G per channel, and typically 2 – 10km reach; cooled and uncooled
  - EML – Typically Higher: bandwidths, reach (>10km), power, and cost
  - Others – DBR, LED, SLED, Comb, Fabry Perot
- Lower temperatures increases Power Conversion Efficiency (PCE), but trade off with added TEC Power, cost, and complexity
- Stabilized temperature over ambient to maintain output wavelength preventing blue/red shifts
- LD+TEC Power budget subject to transceiver type
- Biggest Thermoelectric competitor is getting designed out!





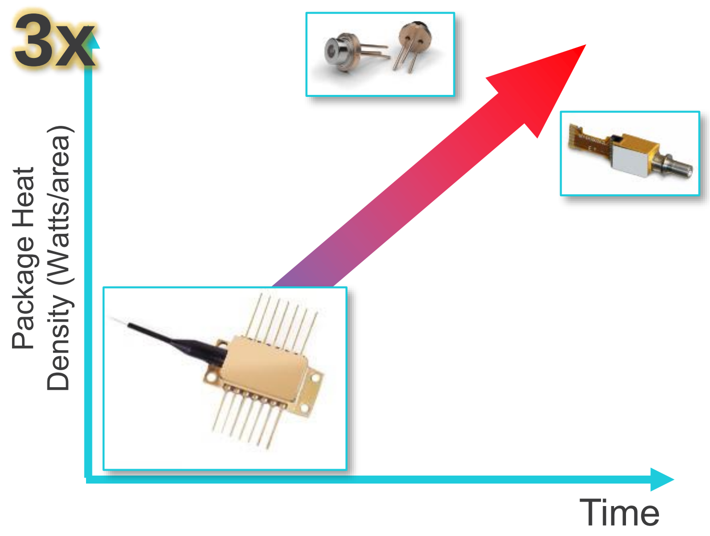
CPO ELS Market Use Cases and Laser Solutions
https://www.lightwaveonline.com/home/webinar/14301411/co-packaged-optics-status-check

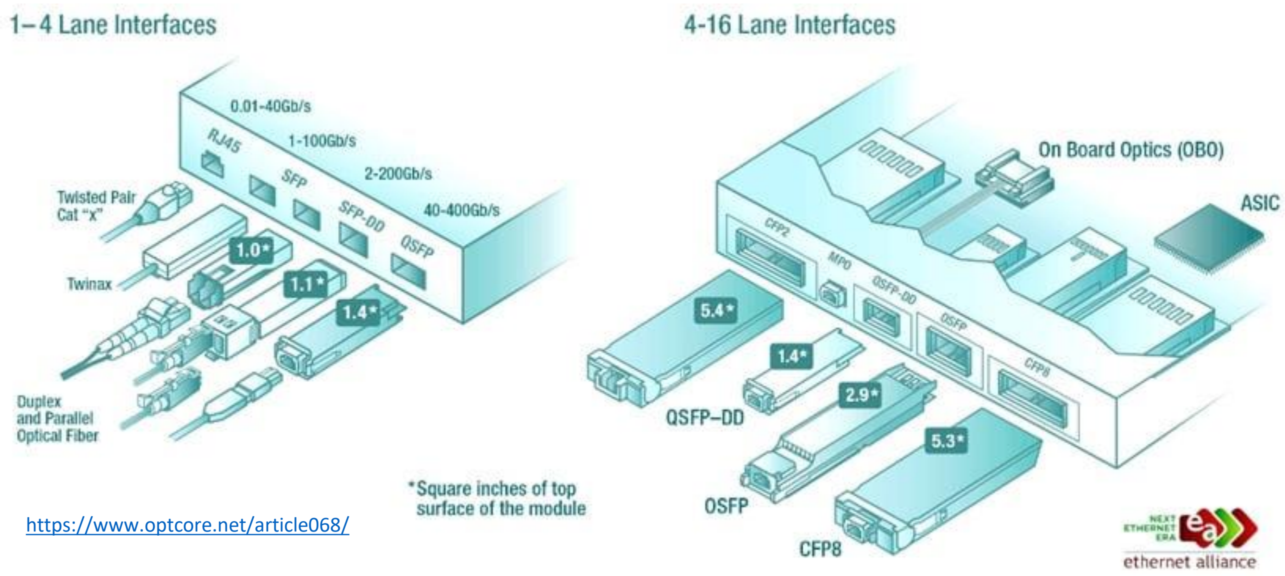
Thermoelectrics are the ONLY technology that can achieve the cooling required for optical components

Understanding Fiber Optic Lasers
https://www.prooptix.com/news/fiber-optic-lasers/

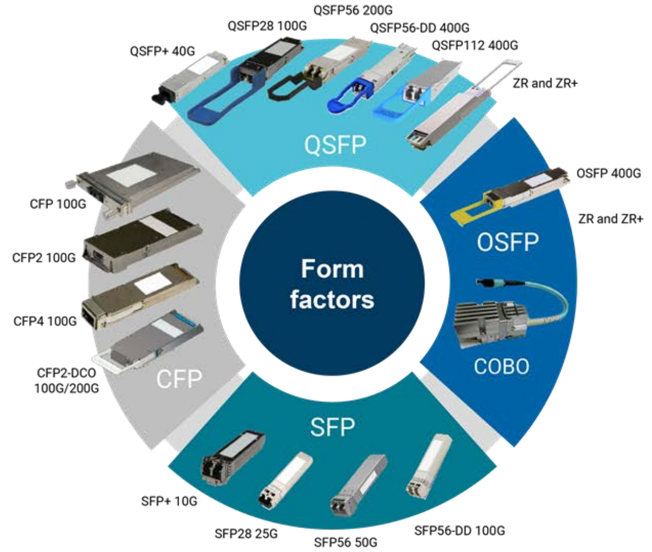
Transceiver Form Factors

- Increasing package heat density
  - Correlates with transceiver form factor shrinking, 12 – 20W+ in QSFP–DD/OSFP
- Increasing maximum ambient temperature requirements
  - C-Temp (0 to 70°C max) → I-Temp (-40 to 85°C max)
- Increasingly stringent power consumption requirements
  - Strict, industry-wide transceiver power limits defined in MSA specifications
- Non-hermetic packages
  - Reduces package complexity/cost, but introduces environmental challenges





https://www.optcore.net/article068/

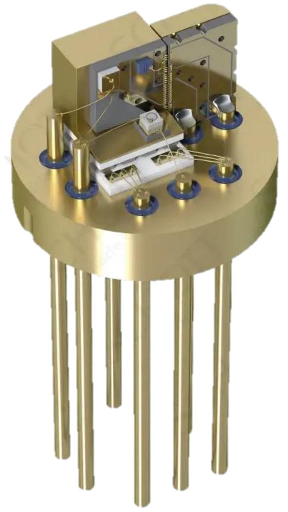


https://www.exfo.com/en/resources/blog/data-centers-move-400g/

Package Types

TO CAN

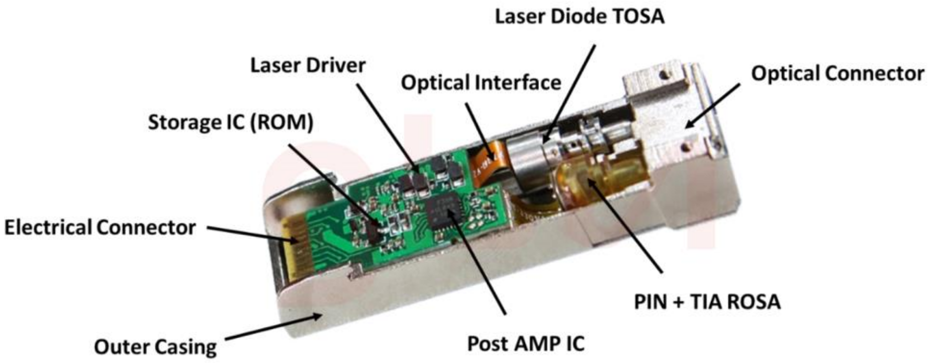
- Single Channel/LD
- <100G
- TEC < ~4mm2
- LD: ~50 – 60°C
- Up to 0.20W active



https://www.schott.com/en-gb/products/t/transistor-outline-packages/content/product-variants/dml-tec-to-package

TOSA/ROSA/BTF/Gold Box

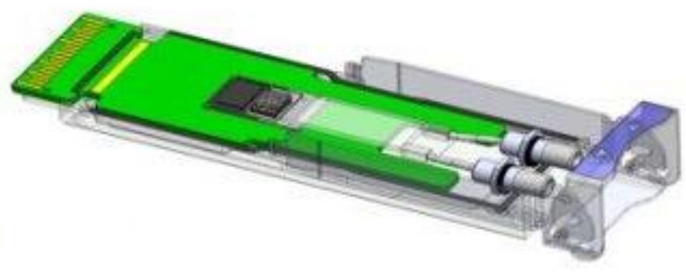
- Single/Multi Channel / LDs
- Tunable, Up to 800G/1.6T and beyond
- TEC < ~20mm2
- LD: ~25 – 70°C
- Up to 0.50W active, per laser
- Additional heat generating components (SOAs)



https://www.glsunmall.com/fiber-optic-articles/sfp-transceiver-modules.html

Non-Hermetic

- Single/ Multi Channel / LDs
- Up to 800G/1.6T and beyond
- TEC < ~20 – 100mm2
- LD: ~60 – 70°C
- Up to ~0.50W active and higher, per laser
- Subject to condensation!



Lumentum via LightWave

Package Types Continued

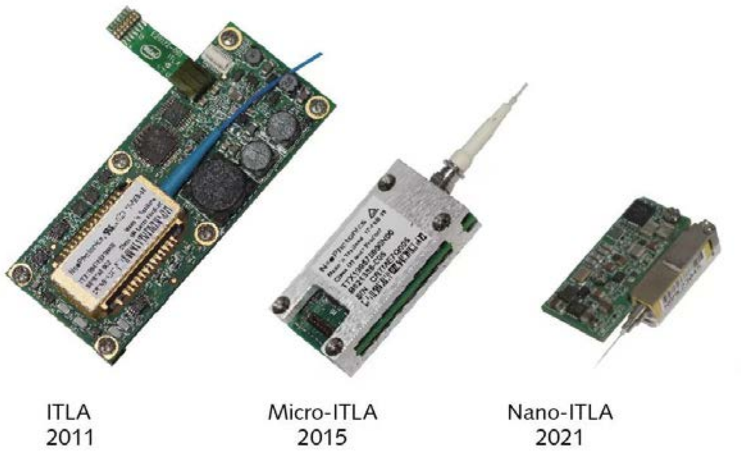
TROSA

- Single Channel (Coherent) & Optics/MZ/Locker
- Tunable, Up to 130 gbaud
- TEC < ~200mm2 (total area)
- LD: ~25 – 70°C
- Up to 0.50W active, per laser
- Additional heat generating components (SOAs)

https://www.infinera.com/products/coherent-trosa/

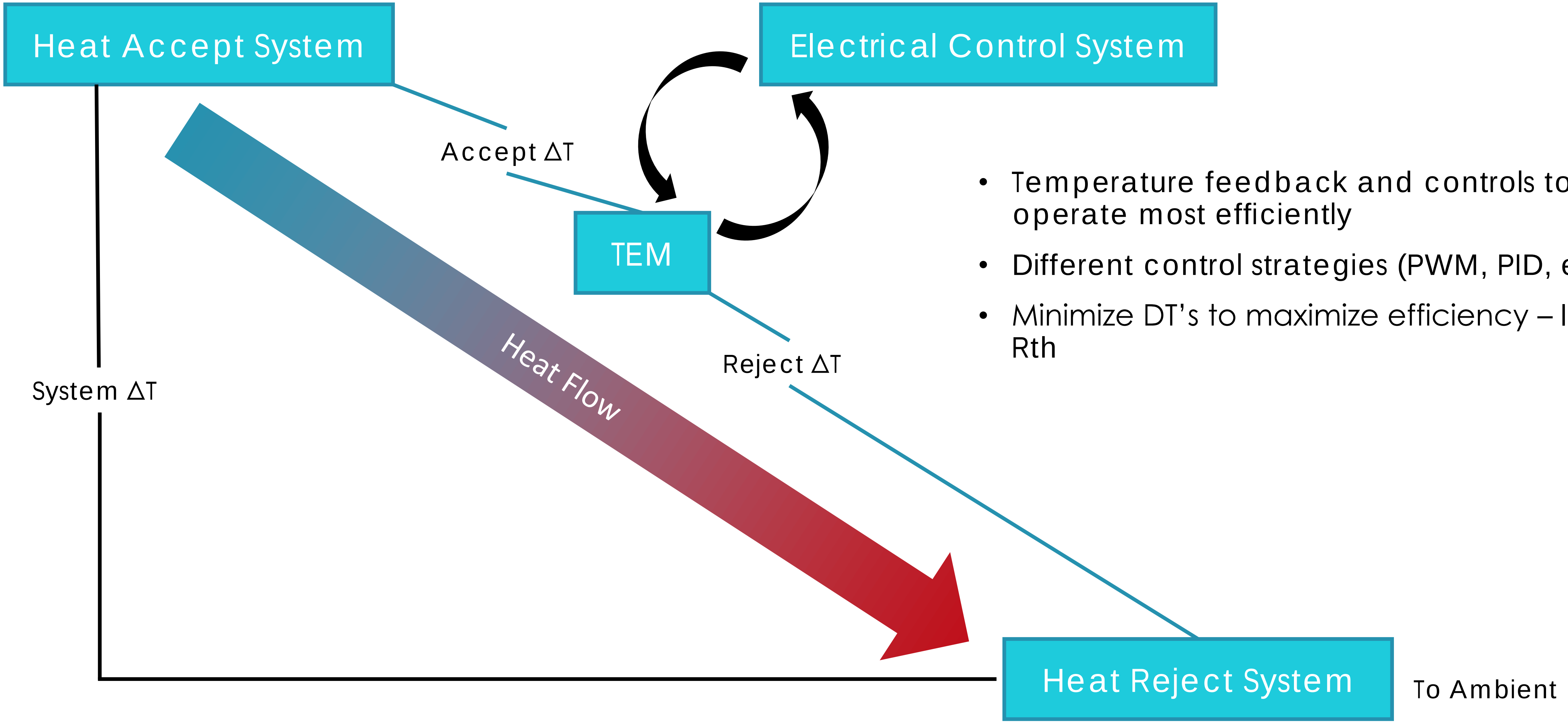
ITLA (Micro/Nano)

- Single Channel (Coherent)
- Tunable, Up to 128 gbaud
- TEC < 20 – 50mm2
- LD: ~50 – 60°C
- Up to ~1W active
- Additional heat generating components



https://effectphotonics.com/insights/the-growing-market-for-tunable-lasers/

What Makes a Thermoelectric System?



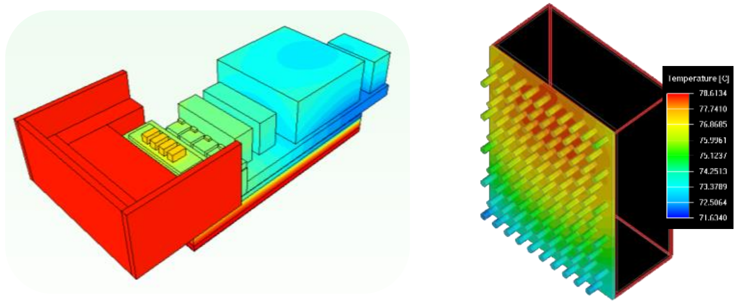
- Temperature feedback and controls to operate most efficiently
- Different control strategies (PWM, PID, etc)
- Minimize DT's to maximize efficiency – low Rth

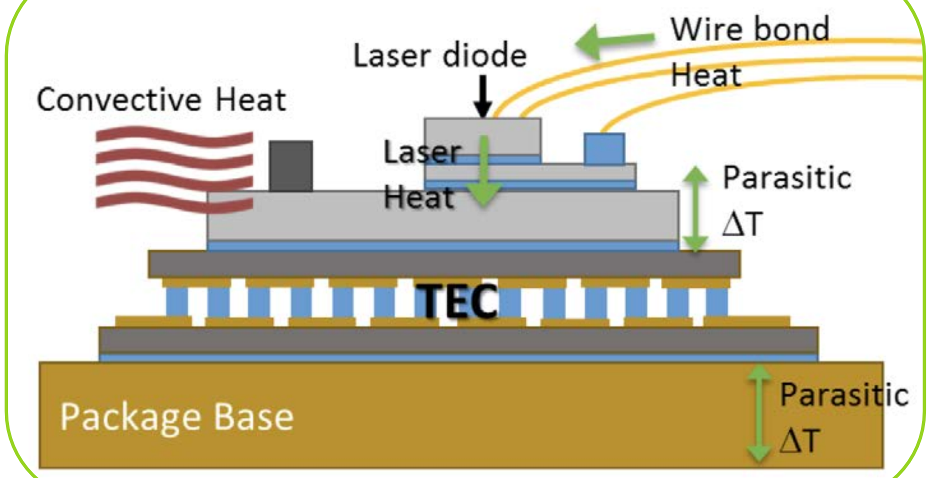
Phononic Value Add: Custom Device Design

Thermal Modeling & Design

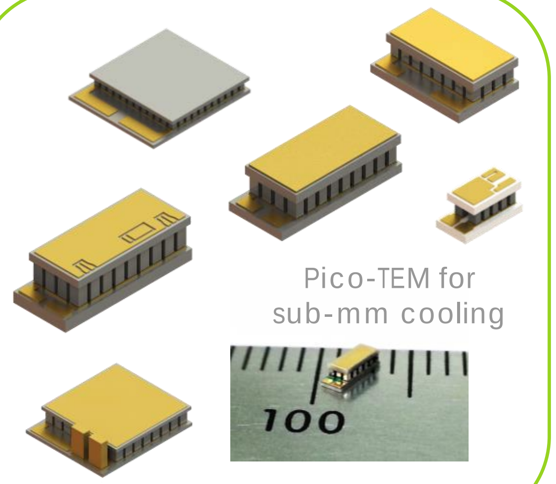
- Complete accounting of package thermal properties achieves the best TEC performance
- First design done right: Full 3D thermal modeling of package and TEC to predict operating point
- Can provide insight into package design to reduce package operating power

Full 3D Thermal Model





Requirements and Thermal Properties



Application-Specific Design

Requirements

Spec Request Sheet, Info Transfer

Thermal
- Temperatures (Boundary)
- Loads
- Thermal Resistances

Electrical
- Desired/Max Voltage & Current
- Driver / Control
- Target Power/ CoP

Mechanical
- Desired/Max envelope
- Cold / Hot Side
- Thickness
- Interfaces
- Robustness

Other
- Features / Add-Ons
- Integration
- Complexity / Cost
- Manufacturability

First Principles: What does the TEC need to do?

Understanding the entire system is critical to TEM optimization

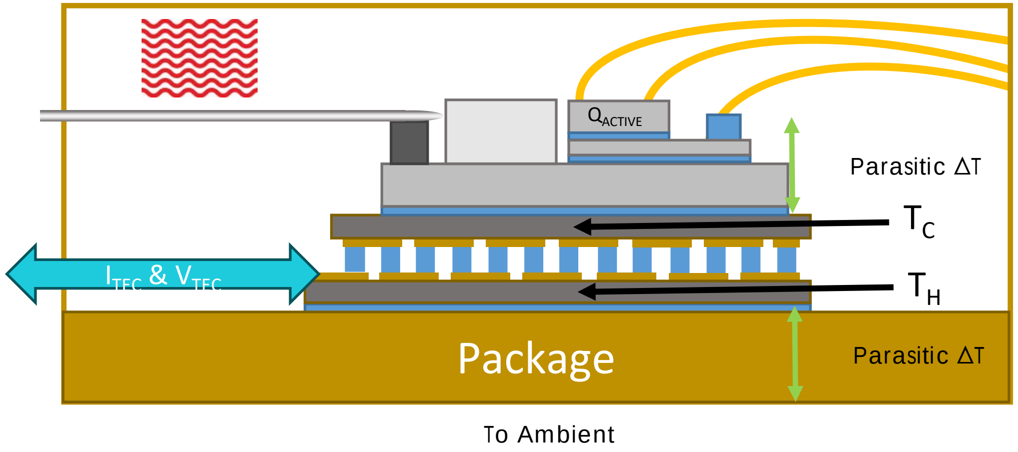
Application Example

Laser Package

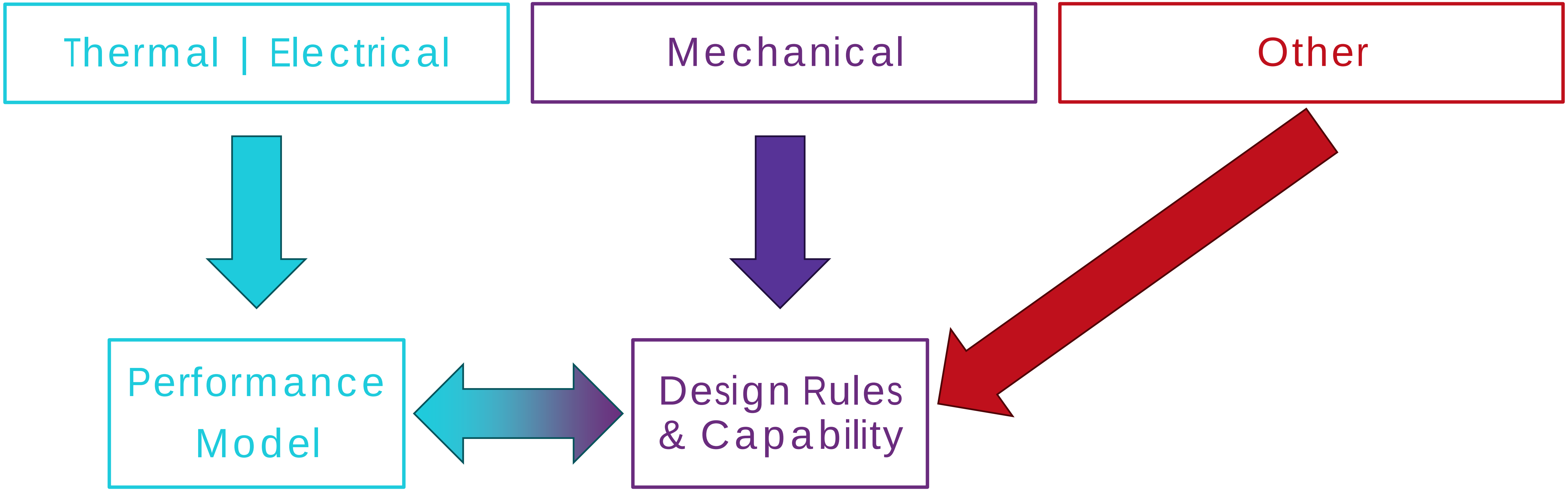
- Laser diode assembly and optical components directly mounted to the TEM and sealed in a hermetic butterfly package
- Thermistor outputs temperature to controller and electrical power is adjusted to the TEM to maintain a temperature set point
- TEM Power proportional to the heat load of the laser, set temperature, and ambient as well as the TEM Design
- TEM Design optimized for specific conditions, typically worst case cooling mode but heating mode can also be considered

Operating Conditions:

- T_C [°C] = Cold side ceramic temperature
- T_H [°C] = Hot side ceramic temperature
- Q_C [Watts] = Total heat load (active + passive)
- ΔT, DT = Delta temperature, $T_H - T_C$
- I_{Device} [Amps] = Operating Current at specified conditions,
  - I_{TEM} or I_{TEC} or I_{OP}
- V_{Device} [Volts] = Operating Voltage at specified conditions,
  - V_{TEM} or V_{TEC} or V_{OP}
- Coefficient of Performance – TEM efficiency, can exceed 100% !



Methodology

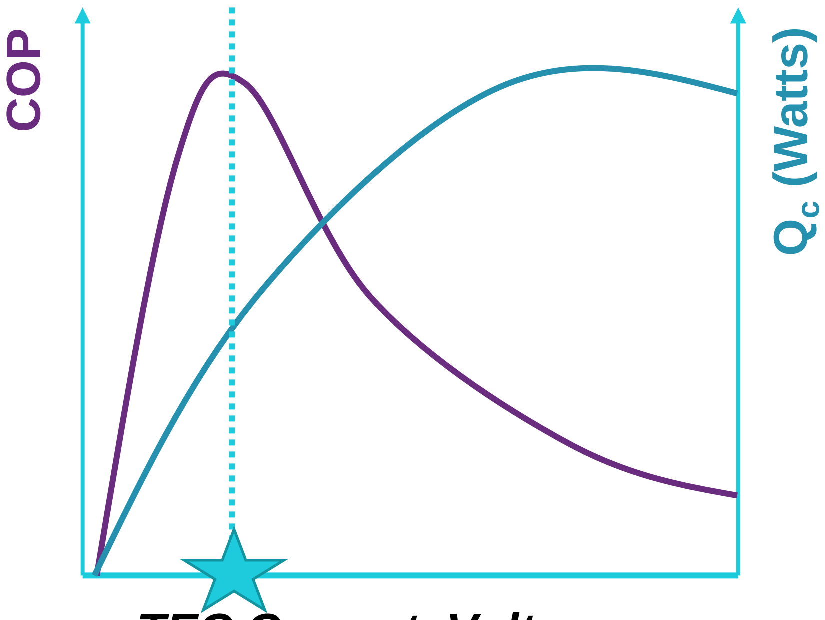


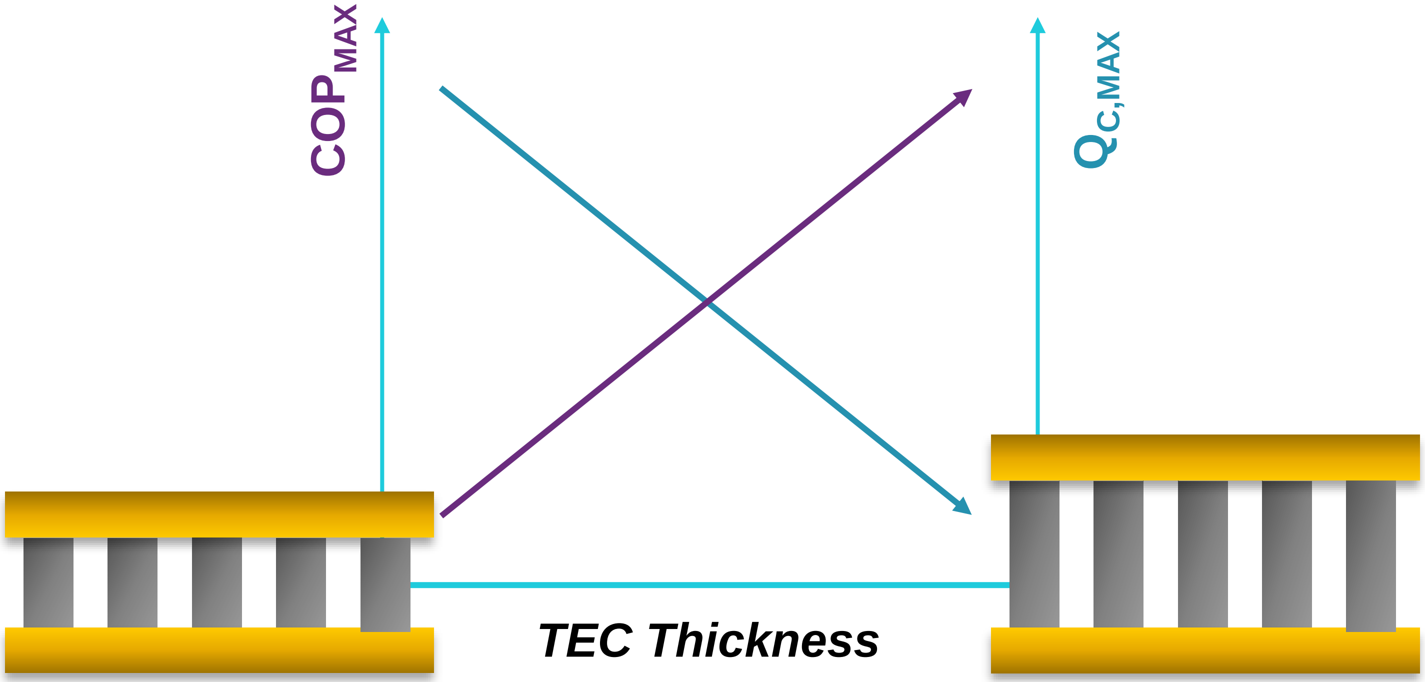
Iterate and evaluate at multiple options! Good design is a balance of customer requirements and flexibility, and packaging it into a form factor that Phononic is comfortable manufacturing in HVM

Performance

- Goal: Optimize TEC coefficient of performance (COP) at operating condition within design rule limitations
- COP reaches maximum at $Q_C \ll Q_{CMAX}$ and shape primarily dictated by ΔT
- TEC thickness, element layout are key design parameters to optimizing
- Efficiency and heat pumping capacity are trade-offs with TEC thickness
- Thicker TECs are not always better, especially at higher heat densities

$$COP = \frac{Q_c}{P_{TEC}}$$





How we develop TECs

////////////////////////

Requirements Recap

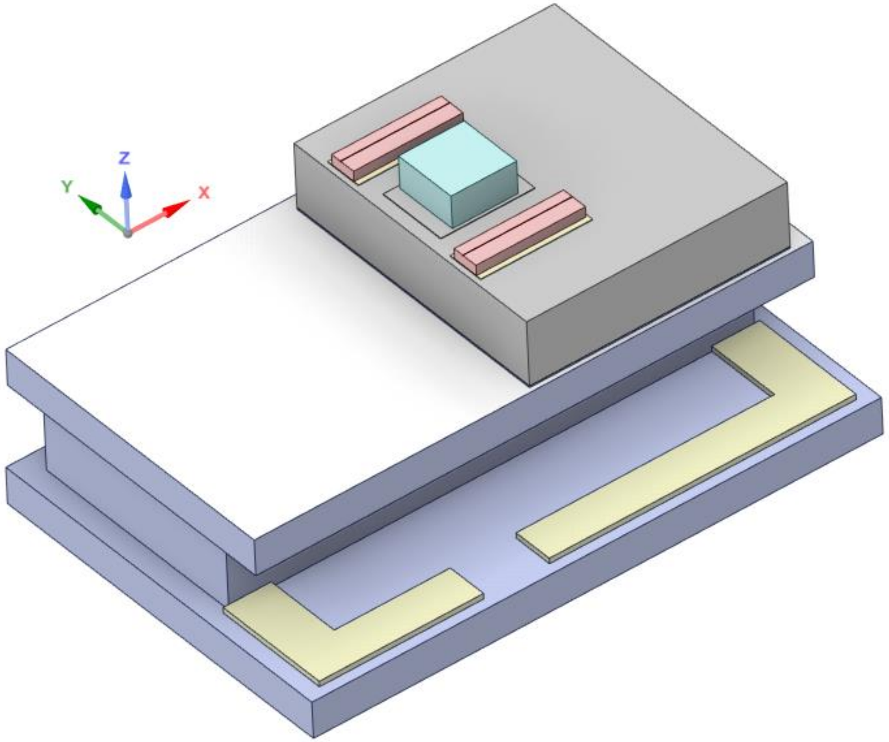
Documentation:
- Customer Provided

Thermal Requirements
- Hot Side Temperature
- Thermistor Temperature
- Total Heat Load

Electrical Requirements
- TEC Voltage
- TEC Current

Mechanical Requirements
- Cold Side
- Thickness

Cost and Performance Considerations



Thermal Model

T_H [°C]	$T_{THERMISTOR}$ [°C]	Hot Side Thermal Resistance [°C/W]	Cold Side Thermal Resistance [°C/W]	Active Heat Load [W]	Passive Heat Load [W]	Total Heat Load [W]
120	50	-	3.2	0.67	0.03	0.7

No Considerations for additional package electrical resistance

Thermal Resistances:

- Hot side ignored (consistent with SOA previous thermal model)
- Cold side impacts simulated by Phononic and presented as shown

Passive Heat Load:

- As provided

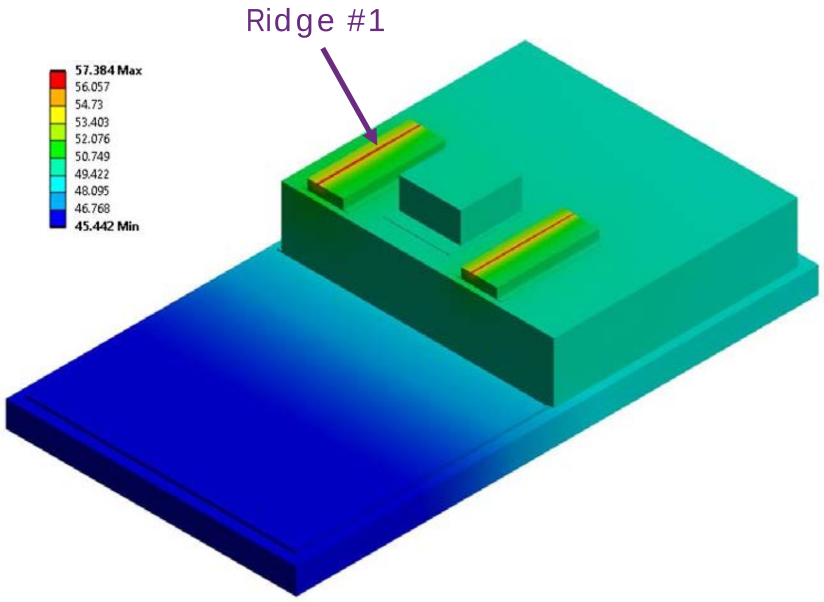
**Thermal model can be updated based on feedback and/or system details updated*
Other conditions can be evaluated upon request

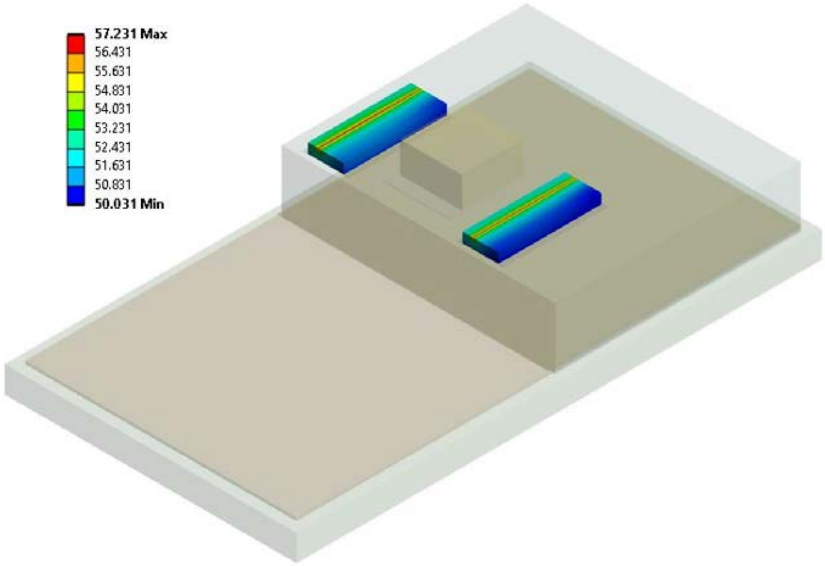
Phononic Simulation Comparison

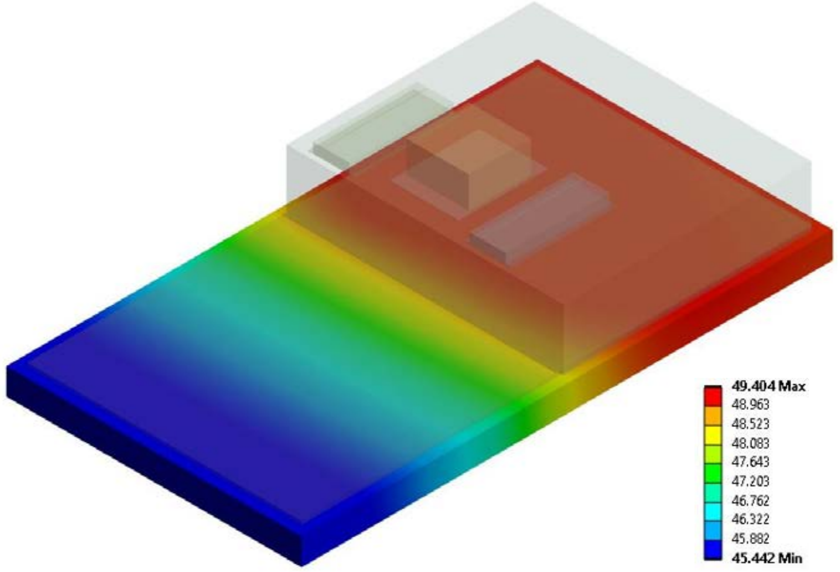
- Geometry and materials per provided 3D CAD
- Ridge heat load applied to body
- TEC Cold Side ceramic modeled to act as a boundary condition for the Phononic TEC performance model
- No powered applied to the thermistor
- Ridge to Thermistor offset at this condition is ~6.3°C

	Temperature [°C]
Ridge #1	56.5
Ridge #2	56.1
Thermistor	50.0
TEC Cold Side	47.7

Cold Side Thermal Resistance [C/W]	3.2





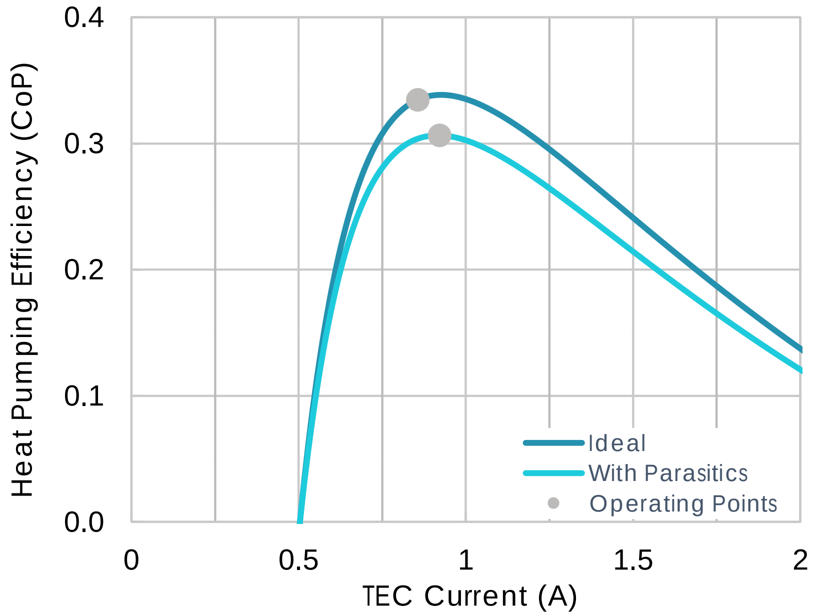


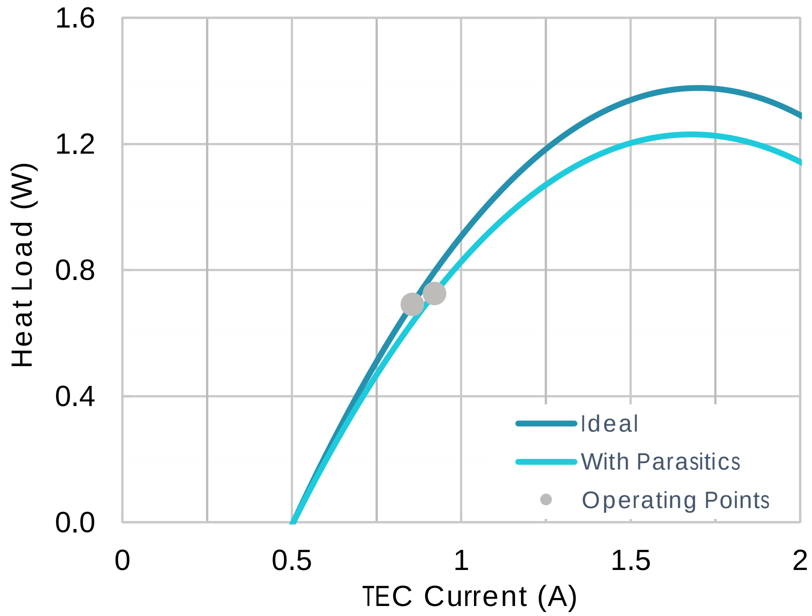
Performance Graphs

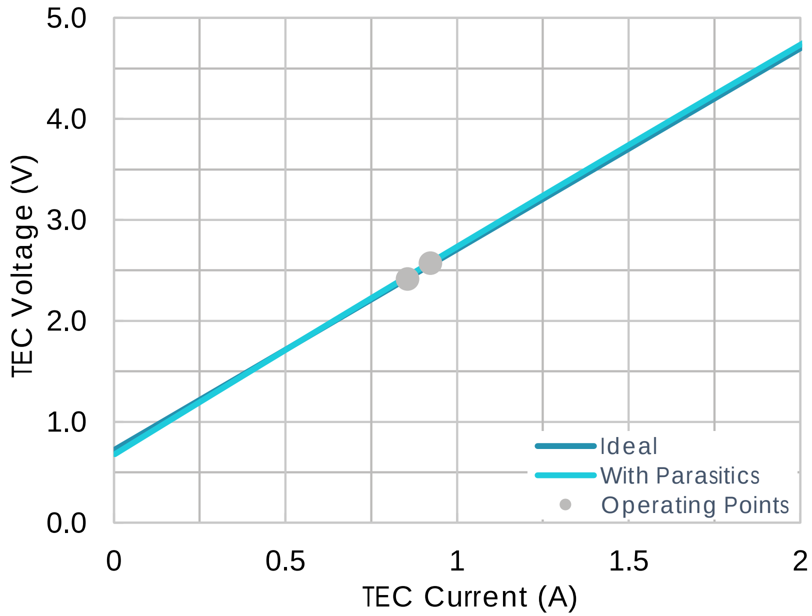
New Design

- Ideal data does not include thermal resistances or passive heat load
- Design operates at peak efficiency and is optimized for the conditions shown
- Voltage and current operate well within specified limits
- Design has been changed from previous proposals and Cost should land between the previously provided pricing
- Standard performance graphs shown; additional graphs and/or heating mode available upon request

Operating Points		
	Ideal	With Parasitics
Total Heat Load [W]		
T_H / $T_{THERMISTOR}$ [°C]	120 / 50	
TEC Power [Watts]		
TEC Voltage [Volts]		
TEC Current [Amps]		







Reliability Overview

Focus:

Device Test

- CSAM
- ACR
- ZT
- Automated Optical Inspection (AOI)
- Seebeck, Electrical/ Thermal Conductivity
- DTmax
- CoP

Reliability

In-house

- Power Cycling
- High Temp Storage
- Bias/Humidity
- Temp Cycling
- Temp Humidity Bias
- Low Temp Storage
- Die Shear Strength

External

- Shock/Vibration
- Lead Integrity
- UHAST
- Heat Resistance
- Fire Hazard

Tests performed on sampling basis

- Factory-wide Control Plans using Statistical Process Control defined by product
- Comprehensive reliability testing in accordance with JEDEC, Telcordia, and Mil Spec standards
- Flexibility to adjust reliability tests based on customer need

Optoelectronic Standard-Based Test Method

- Optoelectronic standard-based testing is based on the Telcordia GR-468-CORE test standard, Section 7
- Telcordia address primary failure modes
- Passing this standard optoelectronic qualification suite of tests indicates that a device will perform well under customer use profiles
- The standard-based test plan for optoelectronic TECs is shown below

Table 7-1 Physical Characteristics and Stress Tests for TECs

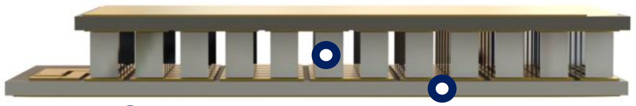
Category	Test	Ref.	Level	Sampling			Additional Information[1, 2]
				LTPD	SS	C	
Physical Characteristics	Die Shear Strength	3.2.10.4	**R**	20	11	0	Applicable to all relevant connections (e.g., TEC/heat sink)
Mechanical Integrity[3]	Mechanical Shock	3.3.1.1	**R**	10	22	0	Condition A (500 g, 1.0 ms), 5 times/direction
	Vibration	3.3.1.1	**R**	10	22	0	Condition A (20 g), 20 to 2000 to 20 Hz, 4 min/cy, 4 cy/axis
Non-Powered Environmental Stress	High Temp. Storage	3.3.2.1	**R**	10	22	0	85°C, 2000 hours
	Temp. Cycling[4]	3.3.2.2	**R**	10	22	0	–40°C/+85°C, 100 cycles
			O	10	22	0	–40°C/+85°C, 500 cycles
Powered Environmental Stress	Power Cycling (On/Off)	7.1.1.2	**R**	10	22	0	Hot-side T ≥ max. op. T, 5000 cycles

Who We Are

Solid State Cooling Platform

High Performance Devices

Advanced Materials
Vertically integrated w/high performance ΔT

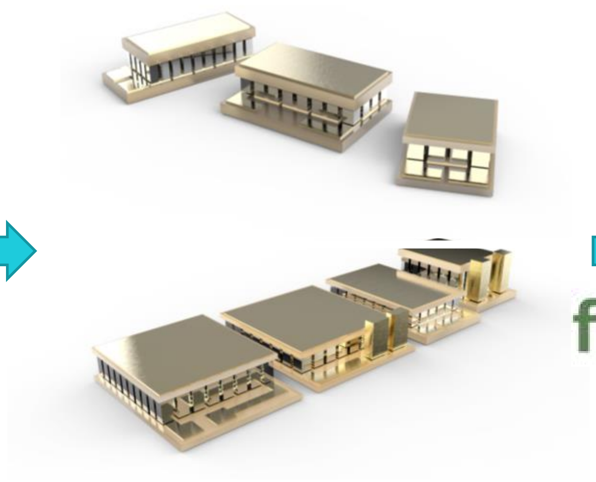


Global IP Portfolio
>85 patents & 40+ trade secrets cover[1]

Wafer Level Process/Package
Compact form factor

Foundational Building Block

Application Specific



Modular Output

Quality Manufacturing

fabrinet

Drives Product Adoption

Proven Industry Leader

ISO & IATF Certified

>25M Devices in Use

Trusted Partner

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[1]Select Patents: Devices: US 8,563,844, US 8,901,612, US 9,218,979; Components/PHP: US 8,564,129, US 9,144,180; Systems: US 8,893,513, US 8,991,194, US 9,103,572, US 9,234,682, US 9,310,111; Products: US, 9,341,394, US 9,581,362, US 9,593,871, US 9,683,752, US 9,746,247

Phononic Active Cooling Solutions

Superior
TEC Modeling

Enabling New Technologies Around the Globe

25+ Million
TECs in Field

World class custom designs with industry leading manufacturing.

Zero
Recalls

Robust QMS & EMS certifications towards ISO 9001:2015 & 14001:2015

Unmatched Application Specific Design Expertise

Fast Turnaround for Production Quality Samples

Industry Leading High-Volume Manufacturing

Unparalleled Quality, Reliability & Performance

Thank You!

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