

# 2.5D Silicon Photonics Interposer Flip Chip Attach

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#### Speaker

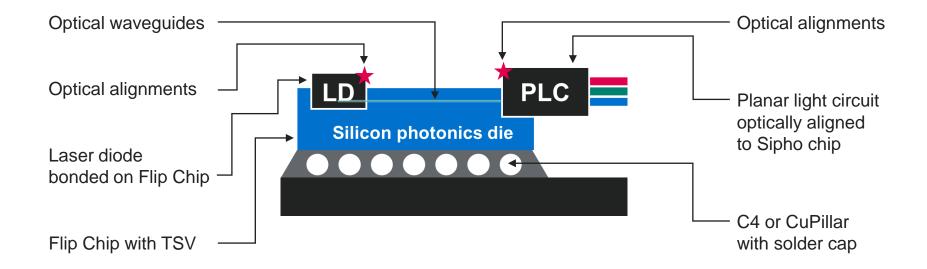


Pushkraj Tumne received his B.S. degree in mechanical engineering from the University of Mumbai in 2006. He went on to earn his Master's degree in 2009 and his Ph.D. in 2012, both in industrial and systems engineering from the State University of New York at Binghamton. Currently, he serves as the Principal Packaging Engineer at Marvell Semiconductors (formerly Inphi Corporation). With over 11 years of experience in IC package technology development, Pushkraj specializes in researching and integrating complex hybrid MCM packages and 2.5D silicon photonics modules.

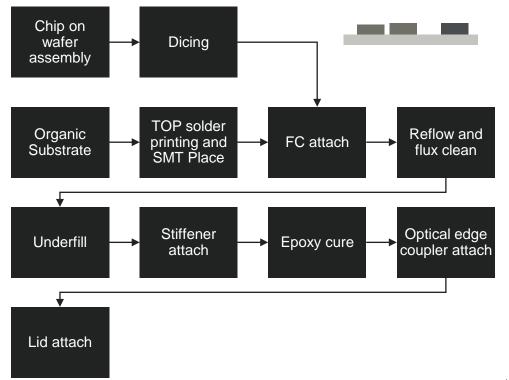
# Outline

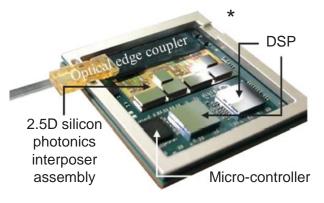
- 1. 2.5D silicon Flip Chip
- 2. 2.5D process flow
- 3. Assembly challenges
- 4. Silicon photonics die attach
  - TCB vs. mass reflow
- 5. Underfill
- 6. Findings and results

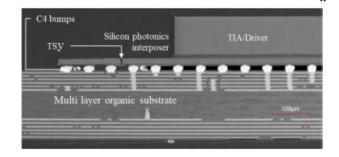
### 2.5D silicon photonics Flip Chip



### 2.5D FC typical process flow



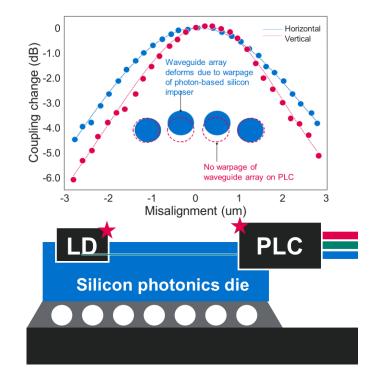




\*Radhakrishnan Nagarajan et al., "2.5D heterogeneous integration for silicon photonics engines in optical transceivers," IEEE Journal of Selected Topics in Quantum Electronics, vol. 29, no. 3, pp. 1-10, 2023. 5

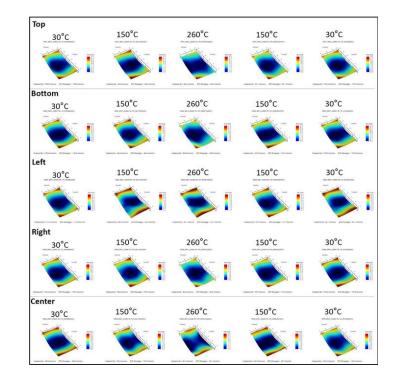
# 2.5D silicon photonics Flip Chip assembly challenges

- Maintain flatness through Pb free reflow (260°C),wash cycles and survive.
- High sensitivity of coupling efficiency (CE) to misalignment, i.e., more than 3dB loss when the horizontal and vertical misalignments are more than 1.5 to 2.0 microns
- Retain waveguide facets cleanliness, maximize underfill coverage and CE at optical interfaces

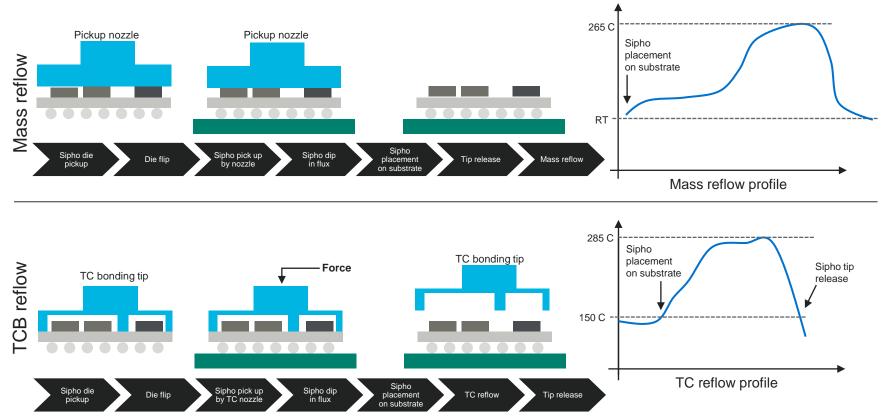


#### Silicon photonics die attach

- The temperature conditions were selected to simulate a typical lead (Pb) free reflow profile.
- Bare dies facing bumps side up. Dies selected from various locations on the wafer.
- The bare die height movement from room temperature to 260°C peak reflow temperature was in the range of 30um to 60um.

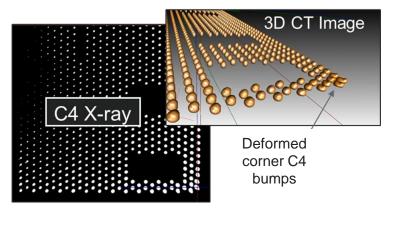


### TC bonding and mass reflow

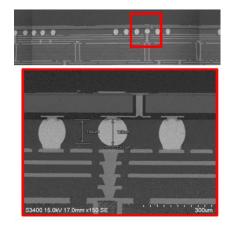


#### Silicon photonics die attach

# Both Mass Reflow (MR) and Thermocompression Bonding (TCB) showed defects

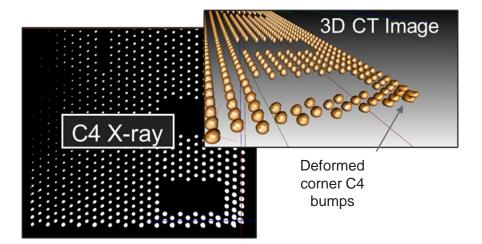


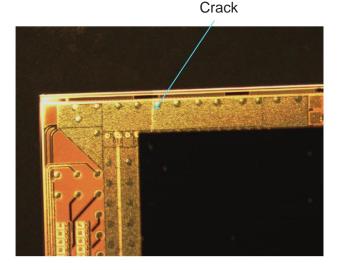
Deformed C4 bumps



Non-wet open defect in C4 joint

#### Thermocompression Bonding (TCB)

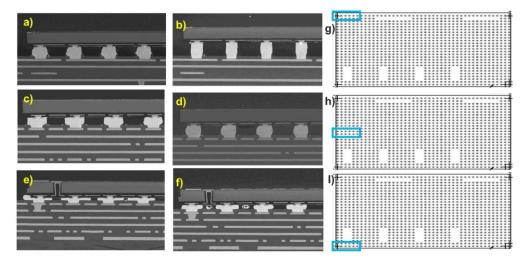




#### Deformed C4 bumps, and die crack

### Thermocompression Bonding (TCB)

TCB pick tool held the Flip Chip (CoW) from the top of the child dies, which increased flatness at the center but kept the outer edges of the OLE free floating



C4 solder joint shape variation across different location in the same die with TCB

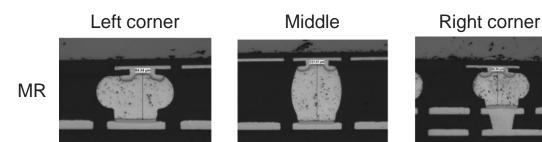
a, c, e are from the same die but different locations

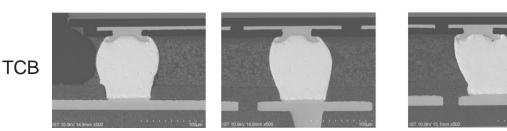
b, d, f are results from OLE bonded with an offset height during TCB process

### Thermocompression Bonding (TCB)

Optimized TCB by using a custom designed TCB tool tip.

The modified tool tip allowed for a better grip of the OLE and reduced temperature distribution across the OLE to less than 5°C.

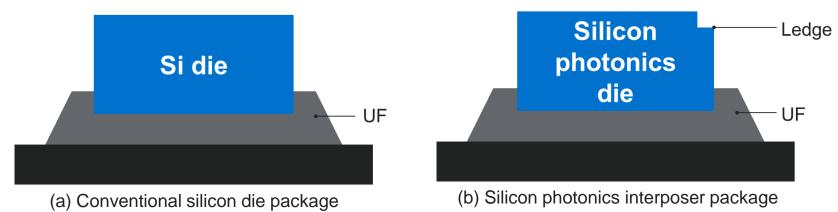




C4 height distribution across the chip

### Underfill

- In convention silicon die UF Filling does not require fillet control except UF creep on top of the die
- Unique challenge to retain waveguide facet cleanliness
- Incomplete underfill coverage can result in larger-than-expected CE variation



#### Underfill

#### **Excess underfill volume**

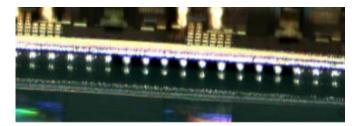
#### Good C4 coverage but underfill creeping to the ledge



Excess underfill across along the ledge

#### Inadequate underfill

Exposed C4 joints, high optical coupling sensitivity to temperature variation

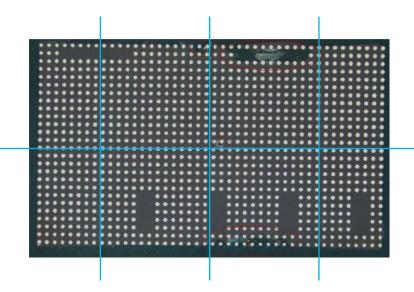


Incomplete underfill exposed solder joints

### **Underfill-optimization**

#### Weighted distribution method:

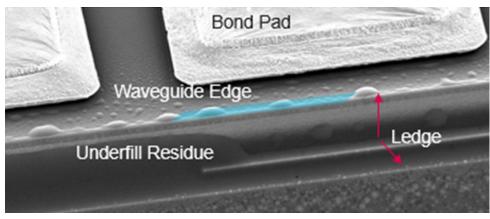
- 1. Divide the silicon photonics interposer into unique sections;
- 2. Measured standoff
- 3. Customize underfill volume dispense for each interposer



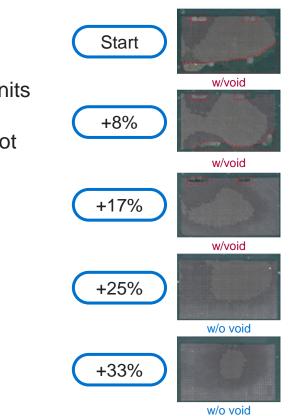
### Underfill-optimization

#### Range method:

- 1. Measure min. and max vertical standoff height for several units from the same lot
- 2. Setup the underfill volume and use for the entire assembly lot



Silicon photonics ledge inspection for UF residue



### Challenges of UF volume control

Excess UF volume			PLC coupler Max UF fillet
<ul> <li>UF on ledge</li> <li>UF dispense volume control challenge</li> </ul>	Good C4 coverage Post-assembly stability	(+) (+)	Max UF fillet height allowed
<ul> <li>Sensitive to thermal change</li> <li>Unstable post-assembly</li> <li>Exposed C4, reliability risk</li> </ul>	No UF on ledge Clear alignment path for PLC att	+ ach +	Goal Maximize C4 coverage under Sipho + No UF on ledge

#### - Limited UF volume



### Findings and results

- Mass reflow resulted in 30% higher Z height variation than TCB
- High variation of C4 height within die impacts optical CE and stability
- Achieved underfill coverage more than 95% using both methods while avoiding waveguide contamination
- Achieved stable CE with variation within +/-1.0dB with both TCB and mass reflow
- Need for optimization: further research is needed to improve the stability of the coupling efficiency

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## Thank You







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#### References

This Talk is based on - Published article -

P. Tumne, H. -C. Wang, D. R. Shirley and R. Coccioli, "2.5D Silicon Photonics Interposer Flip Chip Attach," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 1896-1902, doi: 10.1109/ECTC51909.2023.00325.

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