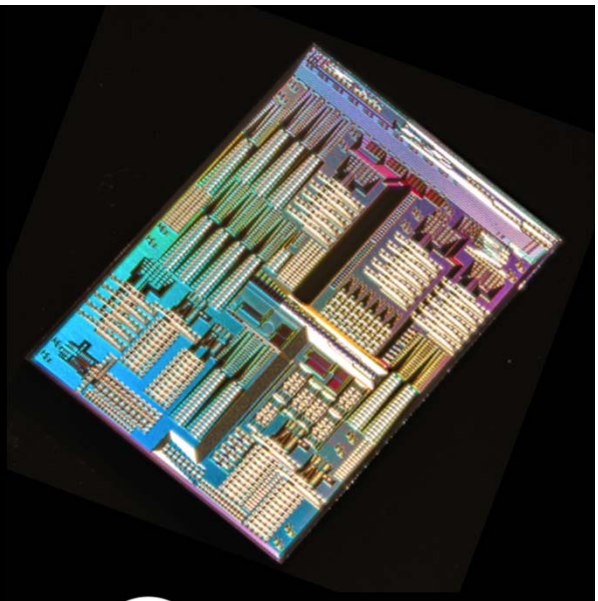
Photonic Wire Bond Packaging for Silicon Photonics, Optical Fibers and Laser Integration



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– Professor, Electrical and Computer Engineering, University of British Columbia
– Co-founder, Dream Photonics Inc.

October 19, 2023
IEEE EPS Bay Area Chapter

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Land Acknowledgement

The UBC Vancouver Point Grey campus is located on the traditional, ancestral, and unceded territory of the Musqueam and other Coast Salish people who have lived here for 10,000+ years.

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Abstract

Photonic integrated circuit technology (silicon photonics) is used for many applications including optical data communications, optical and quantum computing, and sensing including LiDAR, biomedical and environmental. A major packaging challenge facing the industry is optical coupling between multiple integrated photonic components together with low insertion loss, in a cost effective manner, into a package suitable for commercialization. A promising approach is to create “photonic wire bonds” (PWBs), namely optical waveguides that look similar to conventional electrical wire bonds. PWBs are a high-yield, low-insertion-loss, and high-throughput versatile method of packaging photonic components such as chip-to-fiber, laser-to-chip interconnects. Utilizing two-photon polymerization to fabricate freeform 3D polymer structures, PWBs can connect components with arbitrarily disparate mode field shapes and sizes. Capabilities and advantages of the PWB technique include: gain chip integration with existing ’known good die’, dense optical I/O connections to the chip, scalability from prototyping to high-volume, and interconnects that are not possible with other standard photonic packaging techniques.

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Outline

- Electrical wire bonding
- Challenges in packaging for photonics
- Silicon photonics introduction
- Photonic wire bonding
- Commercial availability

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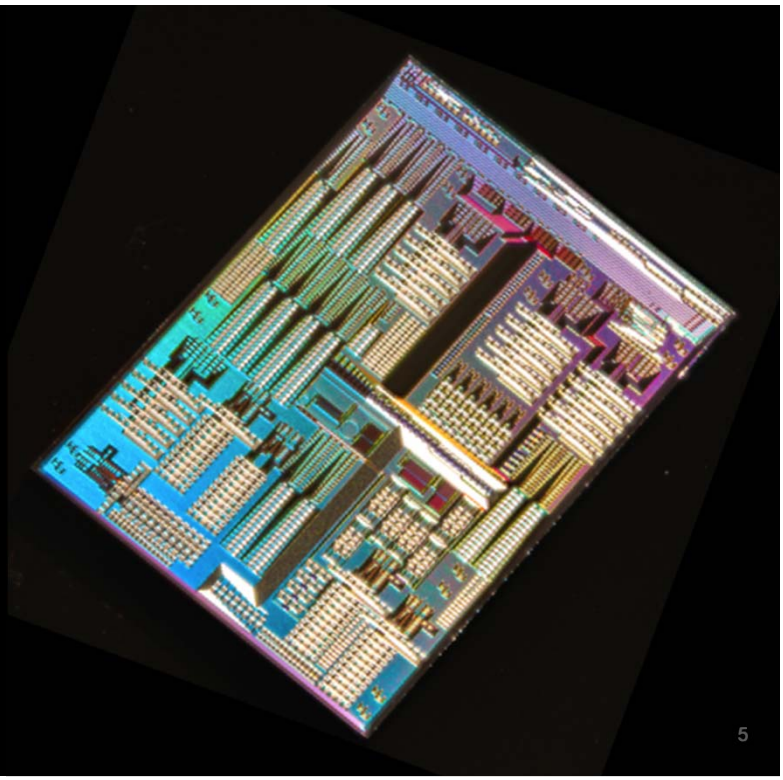
Electrical Wire Bonding



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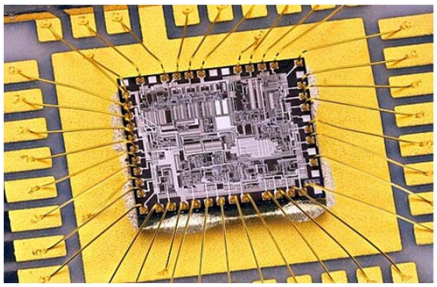
Electrical Wire Bonding – impact on CMOS industry

- Invented in 1957 at Bell Labs
  - Kulicke & Soffa (K&S) in 1959 developed the first commercial wire bonder
- Wire bonding fuelled the microelectronics revolution
  - Whatever was not available on a CMOS chip, one can hybrid integrate on a PCB
- Flexible
  - Type: Ball, wedge
  - Material: Copper, gold or silver
  - Bond pad pitch: from 30 to 100s µm
  - Number of bonds: e.g., 2, 50, 2000
- From Prototyping to Production
  - Manual R&D tools
  - High volume production lines with many wire bonders and robots, used for smartphones, etc.
- Advanced packaging was forecast to replace wire bonding
  - Flip-chip, TSV, Interposer, etc.
  - Yet, wire bonding continues to be a workhorse
  - And keeps improving: stacked die, multi-row connections



https://en.wikipedia.org/wiki/Wire_bonding

Source: K&S https://semiengineering.com/technology-advances-shortages-seen-for-wire-bonders

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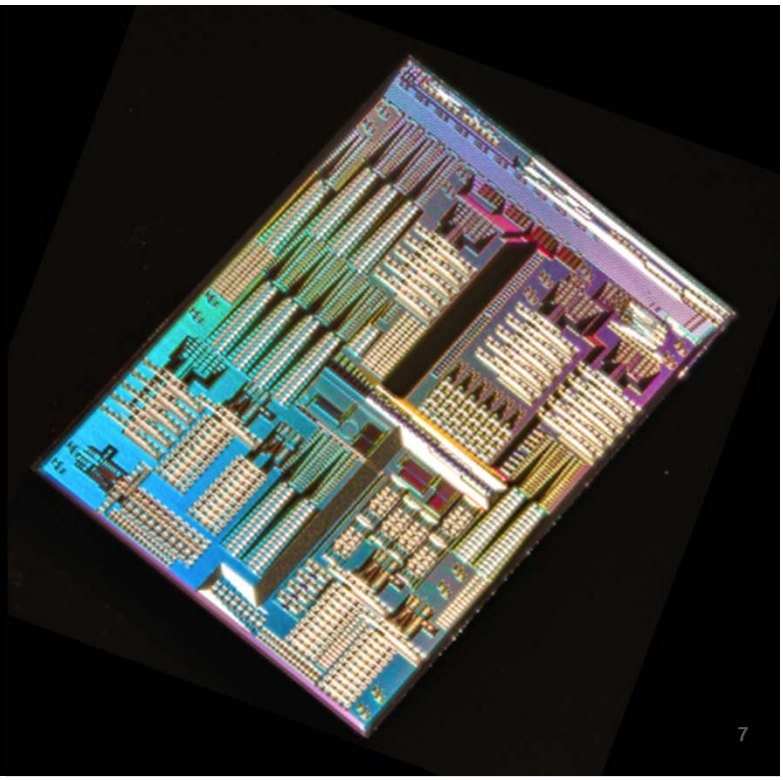
Challenges in Packaging for Optics and Photonics



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What is a Photon?

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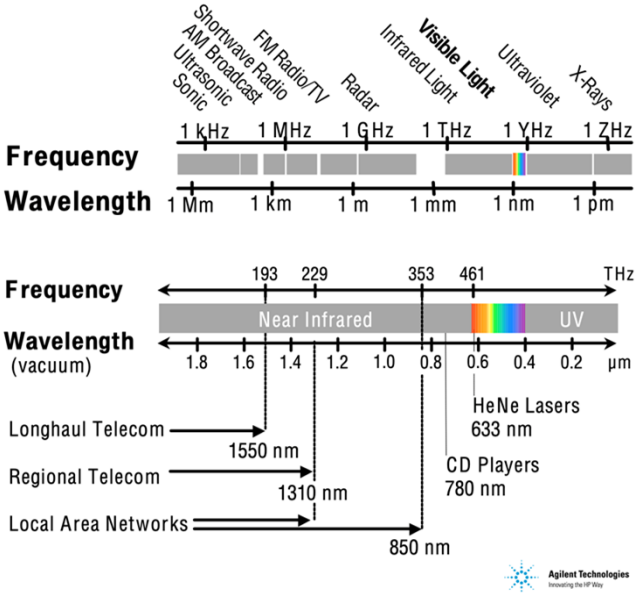
- Electrons vs Photons
  - Electricity “flows” anywhere there is a metallic contact
- A photon is a “wave”
  - Electromagnetic
- Properties
  - Wavelength
    - (or Frequency or Energy)
  - Waves are complex
    - Amplitude
    - Phase
  - Spatial distribution
    - **“Mode” in a waveguide**
  - Temporal distribution



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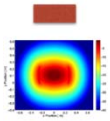
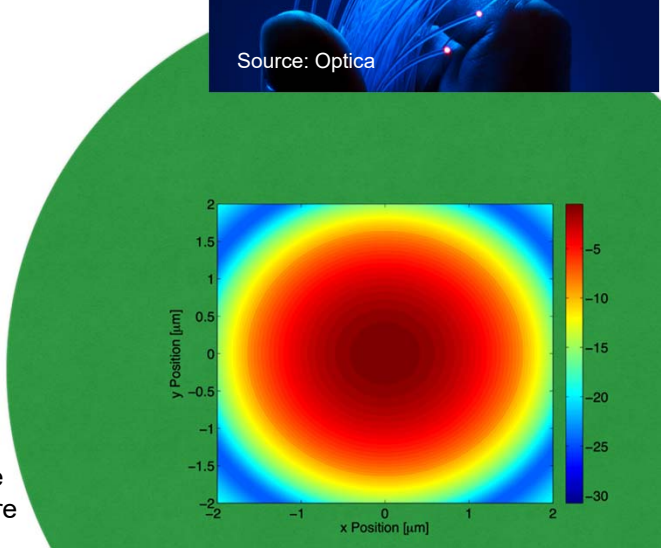
Packaging challenges in Optics & Photonics

- Mode area mismatch
  - The cross-sectional area of an optical fibre core is almost 600 times larger than that of a silicon waveguide!
  - We need mode-matching components
- Precision alignment
  - 6 degrees of freedom (to get profiles to match)
  - Typically < 1 µm accuracy is required

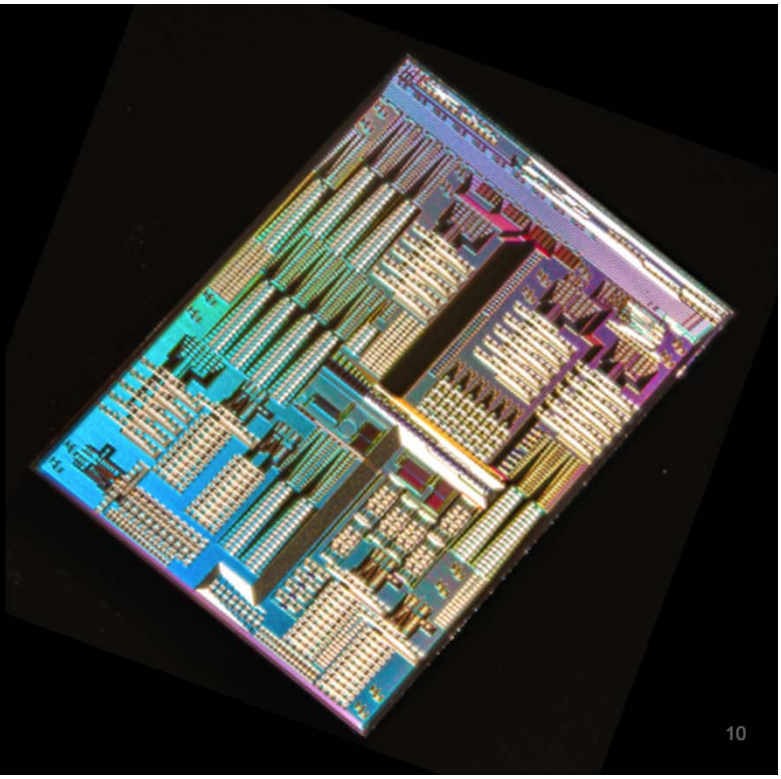
Silicon photonic strip waveguide 500 x 220 nm





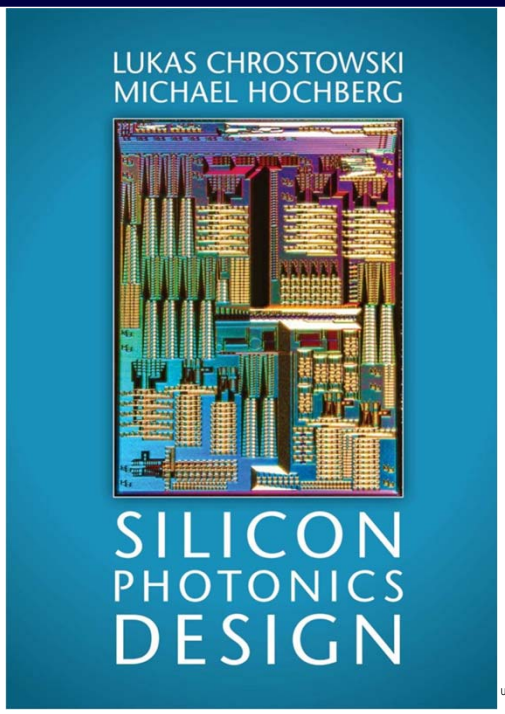
Single Mode Fibre 9 µm diameter core

Silicon Photonics Introduction



Silicon Photonics – Motivation

- Silicon electronics industry
  - $40+ Billion annual R&D investment*
  - Mature materials, **processing**, **design technologies**
  - Possibility of leveraging this technology for optics/photonics
- Silicon photonics
  - "integrated optics" and "photonic integrated circuits (PICs)" on silicon
  - use silicon for optical waveguides and for optical processing/switching
  - Small size, CMOS compatible
- Both electronics & photonics:
  - electronic and photonic integrated circuits (EPIC) in silicon
- Also need rapid prototyping
  - And novel functionality



* $53B in 2012. Source: IC Insight, and http://www.electroiq.com/articles/sst/203/02/semiconductor-rand-spending-rises-7percent-despite-weak-market.html

Updated: 2014/07/05

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Silicon Photonics Applications

Telecommunications
- High-speed networks (e.g. Cisco)
- Coherent (e.g., Ciena, Nokia)
- Fibre to the Home

Optical Interconnects
- Data-com / data centres (e.g. Intel, Cisco (Luxtera))
- Consumer electronics

Analog, RF, Microwave photonics
- Wireless access networks
- Radio over fibre
- Phased array antennas, LIDAR, etc.

Optical computing
- Neural networks
- Matrix multiplication

Quantum Information Processing
- Secure quantum communication
- Quantum computing
- Quantum transducers

Bio Photonics
- Research, Life Science and Clinical Diagnostic market
- Protein and nucleic acid testing (Genalyte)
- Medical diagnostics, blood (SiDx)
- Medical Imaging
- Food safety, Ecoli (NRC)

Environmental Sensing
- Oil & Gas (LuxMux)
- Water quality

Inertial sensors
- Gyroscopes, Accelerometers

Quantum Sensors
- Magnetometers, Electric field

Nano-Opto-Mechanical systems
- ...

Updated: 2014/

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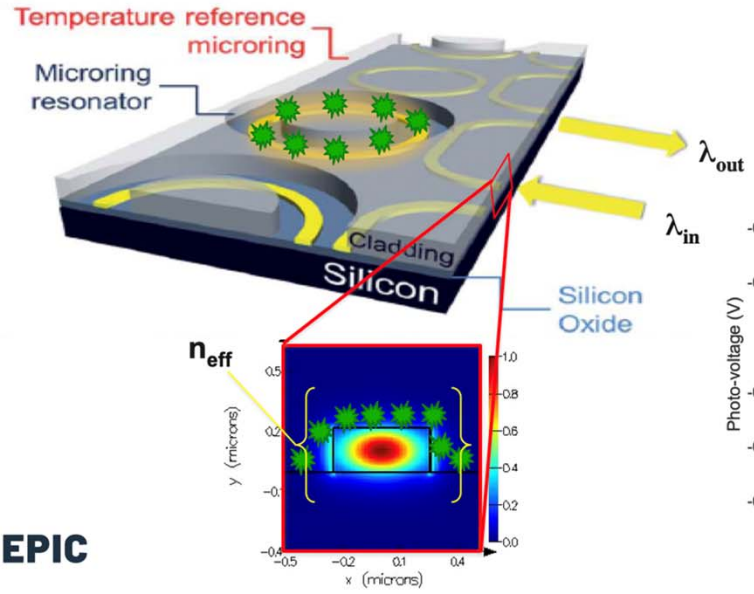
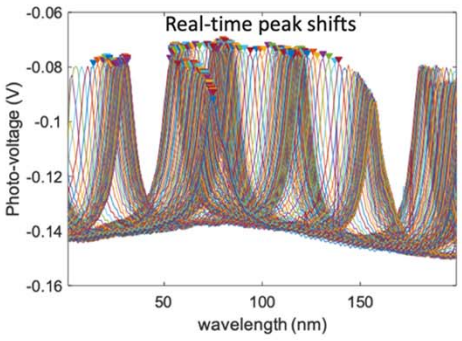
Application – Silicon photonic evanescent-field ring (bio) sensors

- Refractive index sensing using resonators
  - track resonance frequency changes





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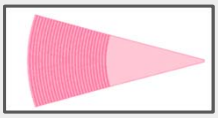
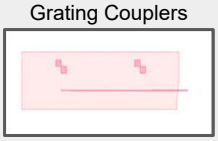
Application – Photonic Quantum Computing (e.g., Xanadu, PsiQuantum)

INPUTS

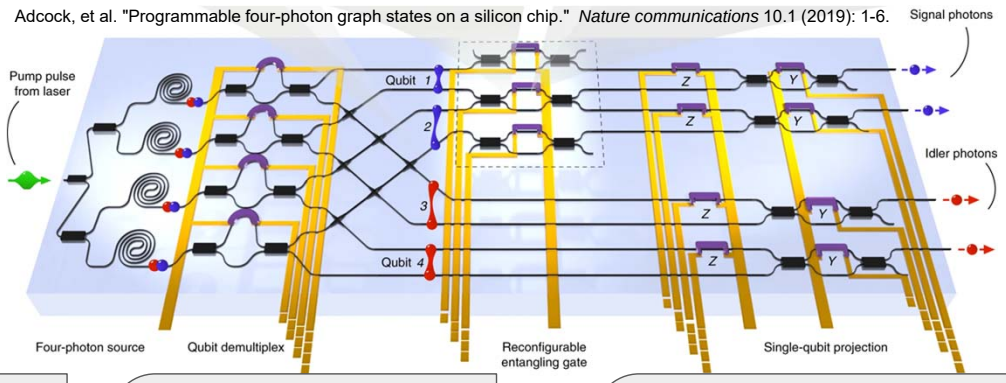


Grating Couplers

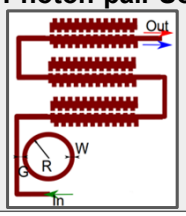


Photonic Wirebonds

Adcock, et al. "Programmable four-photon graph states on a silicon chip." *Nature communications* 10.1 (2019): 1-6.

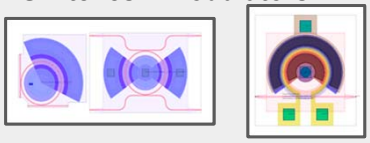


Photon-pair Sources



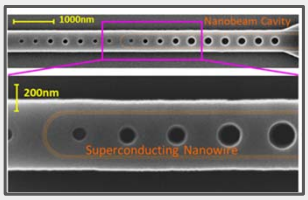
SFWM MRR + CDC pump reject filters

Switches + Modulators



- IRPH Modulators
- Polymer/Graphene Modulators
- PN Junction Modulators

On-chip Single-photon Counting



PhC Cavities + SNSPD integration

Akhlaghi, et al. *Nature communications* 6.1 (2015): 1-8.

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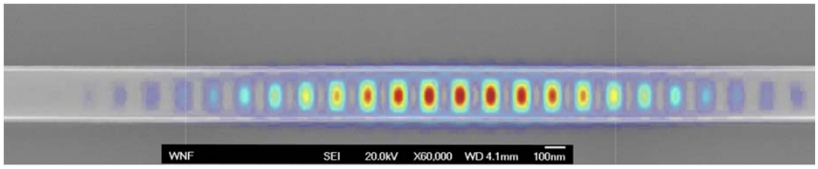
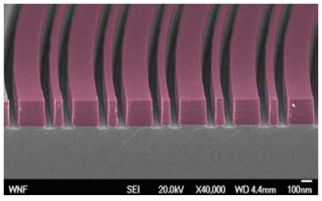
Devices

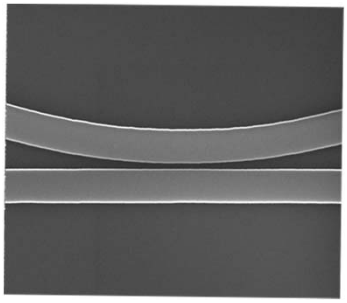


Optical Waveguides

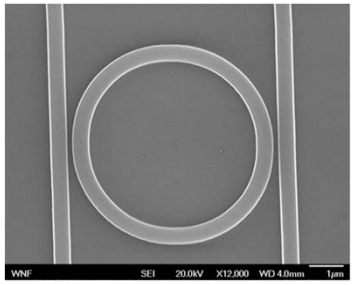


Optical coupling in/out of chip

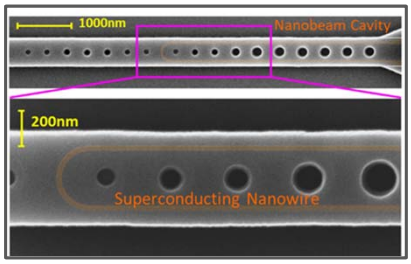
2x2 Splitters



Photon Pair Sources



Superconducting Nanowire Single Photodetector (SNSPD)



Akhlaghi, et al. *Nature communications* 6.1 (2015): 1-8.

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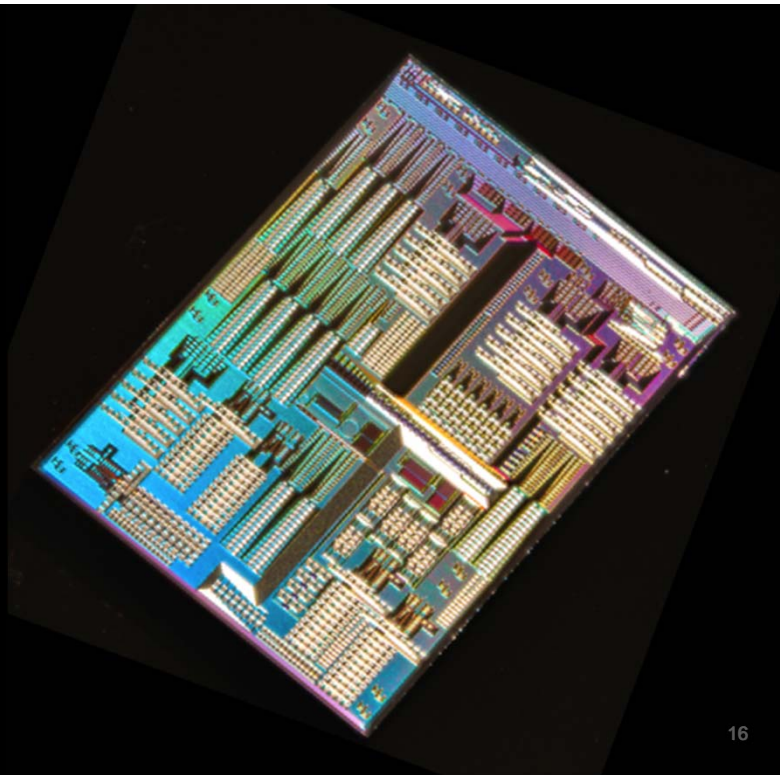
Challenges in Packaging for Optics and Photonics



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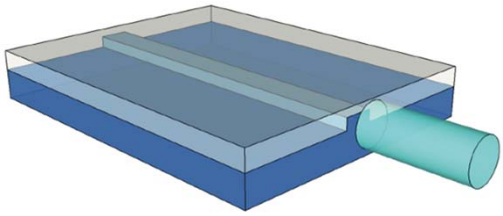
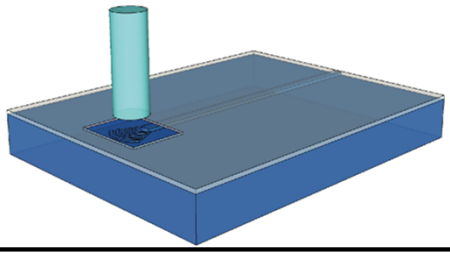
Packaging challenges in Optics & Photonics





	Edge Coupling	Surface Grating Coupling
Pros	• Wide optical bandwidth • Support for both TE/TM polarization • Similar to existing laser & modulator edge packaging techniques • **High-efficiency**	• Easy alignment • Cost-effective – no post process • Location flexibility in the designs; compact • **Chip/wafer scale automated measurement** • High-efficiency
Cons	• **Challenging alignment (smaller mode size)** • More complicated fabrication (e.g., edge facet polishing, tapers for mode expansion, access to edge of chip)	• Limited optical bandwidth • **Challenge in obtaining good coupling efficiency (typically 3 dB or more)** • Normal-incidence challenging for packaging

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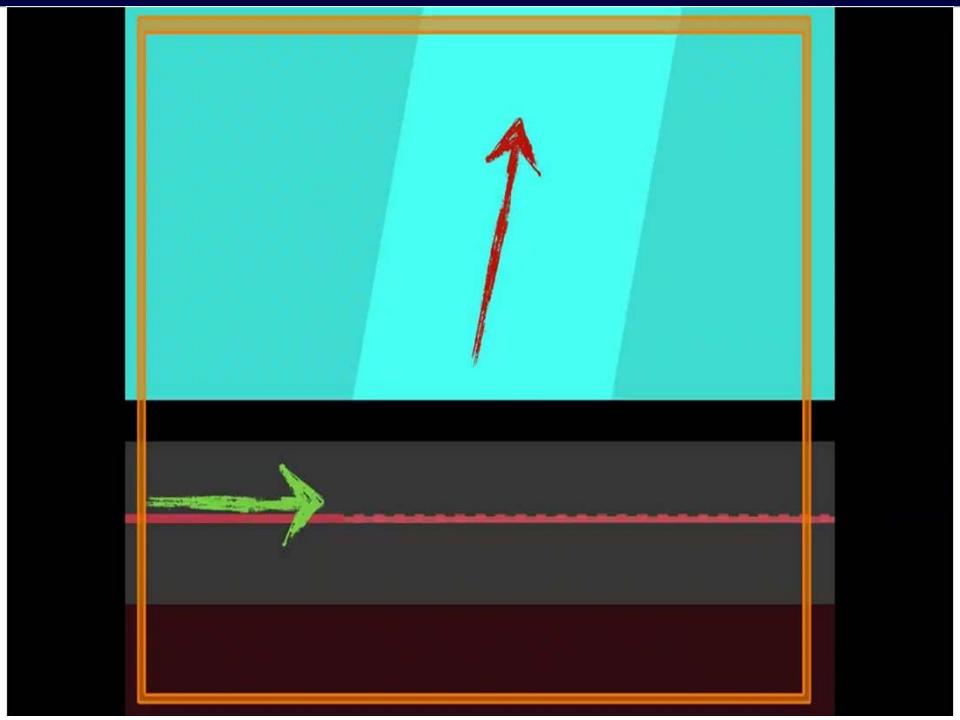
Fiber to Surface grating coupler



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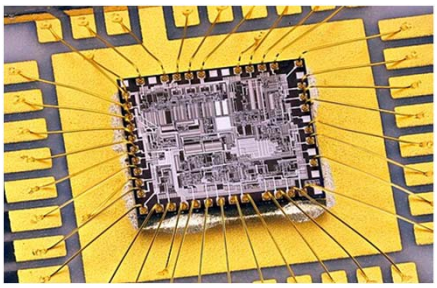
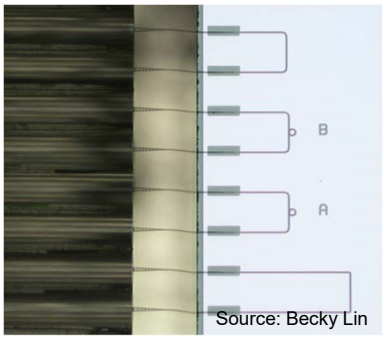
Packaging challenges in Optics & Photonics

- Desirable attributes for a photonic packaging solution:
  - Whatever is not available on a silicon photonics chip, one can hybrid integrate
  - Flexible
    - Type: single mode, multi mode
    - Pitch: from 30 to 100s µm
    - Number of connections: e.g., 2, 50, 2000
    - Works for a broad range of wavelengths
    - Works for different types of chips (e.g., lasers)
    - Temperature, Humidity, Shock, Reliability…
  - Known-good die compatibility
  - From Prototyping to Production
    - Manual R&D tools
    - High volume production lines with many wire bonders and robots, etc.
- Solution – Photonic Wire Bonding



https://en.wikipedia.org/wiki/Wire_bonding



Source: Becky Lin

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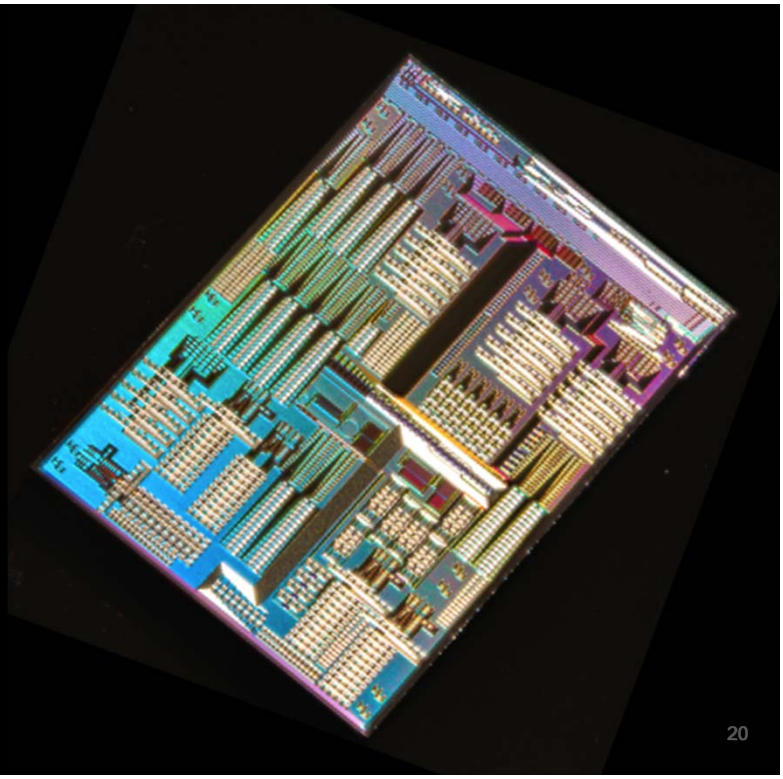
Photonic Wire Bonding



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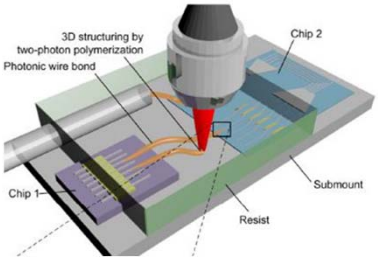
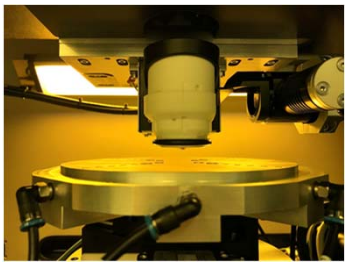
Photonic Wire Bonding (PWB)

Packaging solution:

- Fast 3D fabrication of optical connection (30 to 120 seconds per bond)
- Low optical insertion loss (< 3 dB per bond)
- High placement and optical misalignment tolerance (30 µm)
- Compact and mechanically stable (demonstrated down to 4 K)
- Flexible - can accommodate components with disparate mode field size/shape
- Low-volume prototyping, and potential for up to million units production



Vanguard Automation GmbH tool



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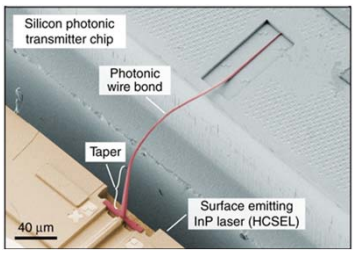
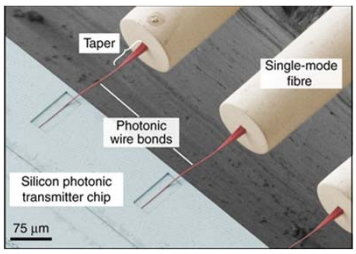
Menagerie of photonic wire bond connections

DFB to SiP

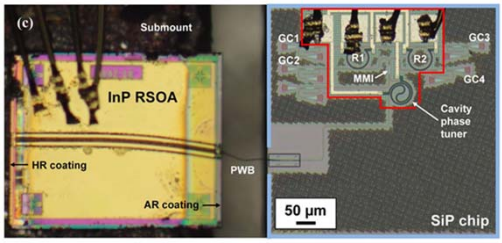


SiP to SMF fibre



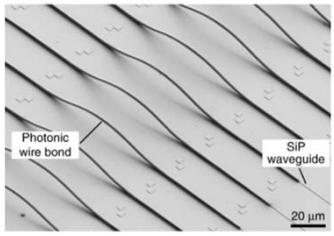
Blaicher, M., et al., *Light Sci Appl* 9, 71 (2020).

SOA to SiP – External Cavity Laser



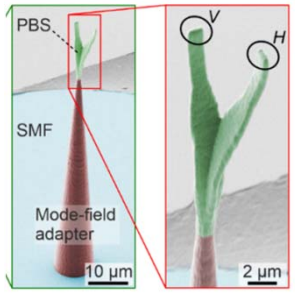
Xu, Y., et al., *Scientific Reports* 11, 1 (2021).

SiP to SiP (reliable)



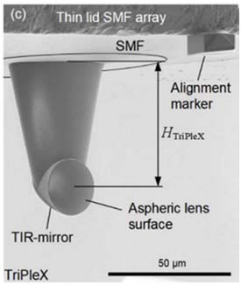
Blaicher, M., *et al., Light Sci Appl* 9, 71 (2020).

Polarization BS/Rot



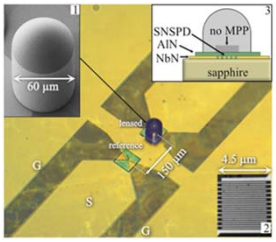
A. Nesic et al., *arXiv* 2107.12282 (2021)

Lens on SMF fibre



M.Trappen, et al., *Opt. Express* 28, 37996-38007 (2020)

Lens on SNSPD



Y. Xu, et al., *Opt. Express* 29, 27708-27731 (2021)

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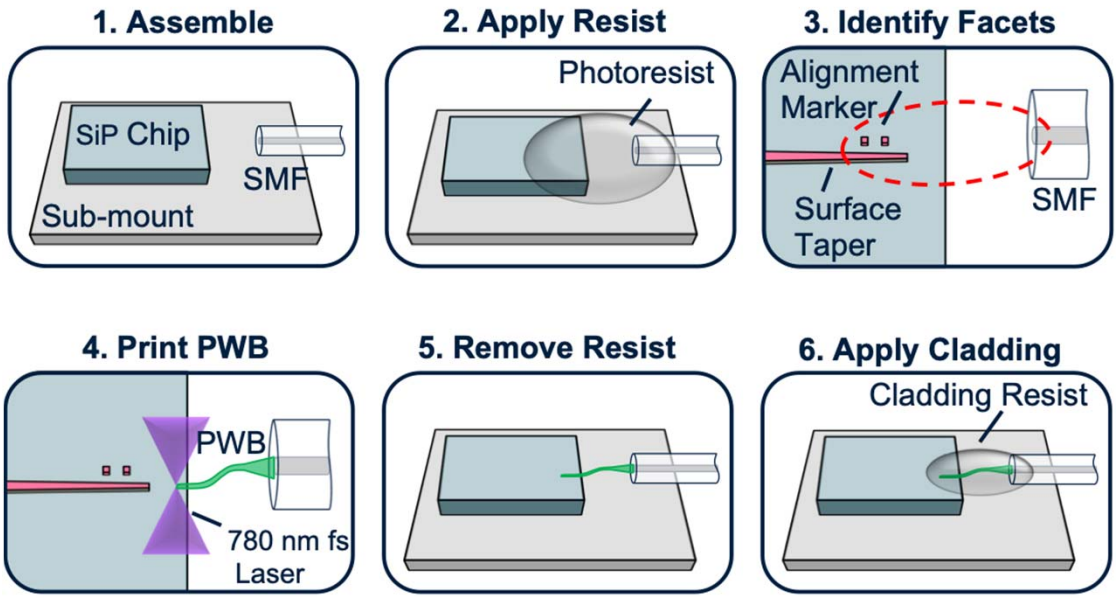
PWB 3D printing process



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Source: Becky Lin

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Fiber-to-chip packaging of AMF chips with photonic wire bonds (PWB)

Advantages of photonic wire bonds

- Fast 3D fabrication of optical connection (30 to 120 seconds per bond)
- Low optical insertion loss (< 3 dB per bond)
- High placement and optical misalignment tolerance (< 30 µm)
- Compact and mechanically stable
- Flexible - can accommodate components with disparate mode field size/shape
- Low-volume prototyping, and potential for up to million units production

Contact AMF and/or Dream Photonics for more information (PWB cell, PDK documentation), custom solutions, and costs

amf ADVANCED MICRO FOUNDRY sales@amf.com

dreamphotonics.com

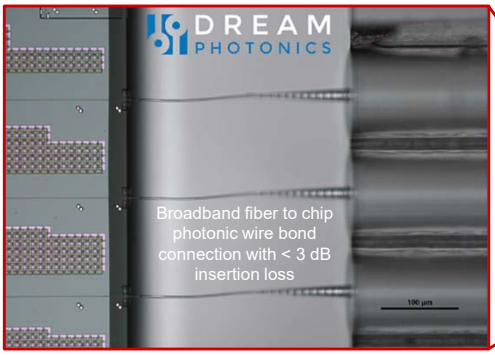
pwb@dreamphotonics.com

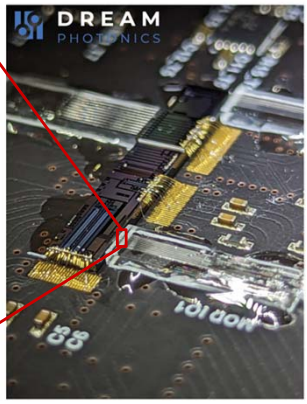
DREAM PHOTONICS

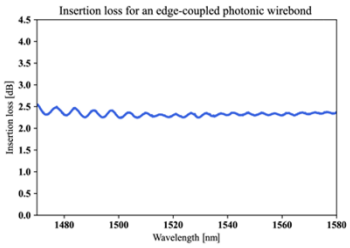
Fiber-to-chip packaging of AMF chips with photonic wire bonds (PWB)

Advantages of photonic wire bonds

- High placement and optical misalignment tolerance (< 30 µm)
- Low optical insertion loss (< 3 dB per bond)
- Fast 3D fabrication of optical connection (30 to 120 seconds per bond)
- Compact and mechanically stable
- Flexible - can accommodate components with disparate mode field size/shape
- Flexible choice of substrate for higher degree of integration (PCBs, interposers, etc.)
- Low-volume prototyping, and potential for up to million units production





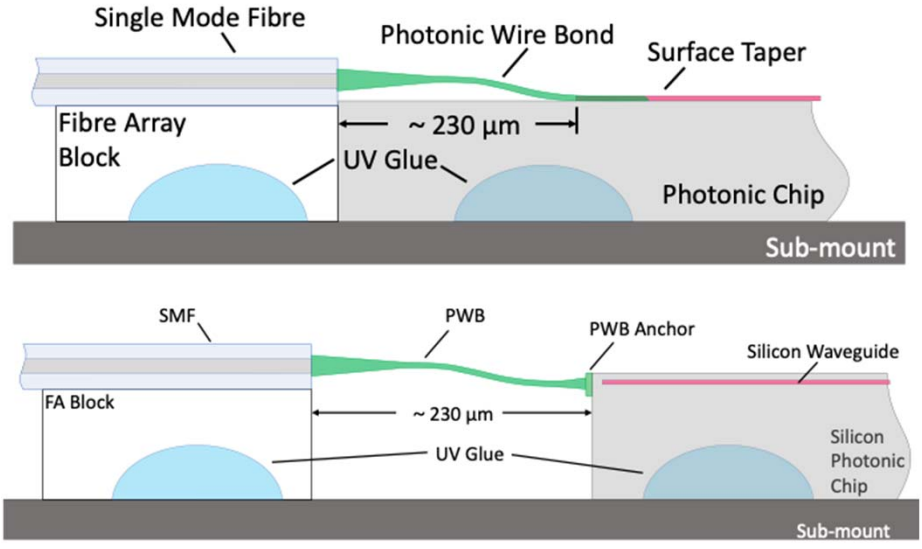


Contact AMF and/or Dream Photonics for more information (PWB cell, PDK documentation), custom solutions, and costs

amf ADVANCED MICRO FOUNDRY sales@amf.com dreamphotonics.com pwb@dreamphotonics.com DREAM PHOTONICS

Surface or Edge PWBs

- PWBs can be attached to either the surface or the edge of a chip



Source: Becky Lin

SiEPIC FAB

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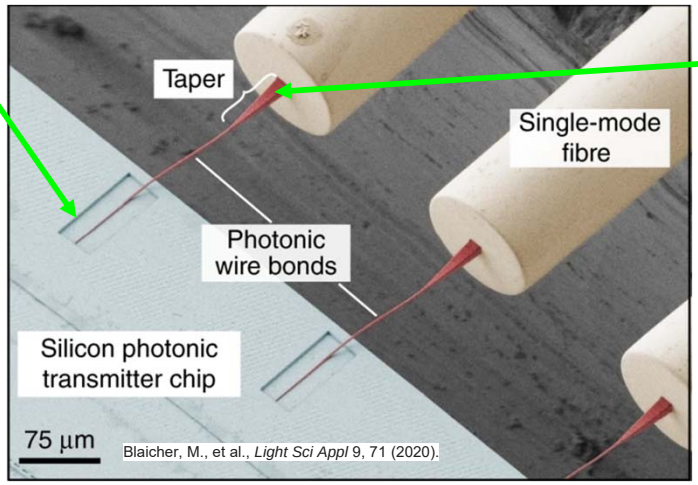
Surface or Edge PWBs

- Surface couplers require access to the optical waveguide
  - Achieved using an oxide open process step
- Edge coupling requires a clean facet (etched or polished)
- Both interfaces have been shown for Si, SiN, and other materials

Surface evanescent-field adiabatic coupler

Edge / "butt" coupler



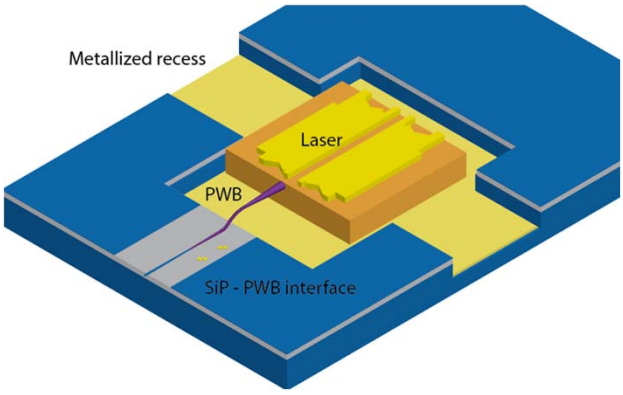
Blaicher, M., et al., *Light Sci Appl* 9, 71 (2020).

27

PWB interfaces - DFB laser to chip/fiber

- Distributed feedback (DFB) laser placed in recess on the SiP chip, integrated via a PWB

US Patent Application 17969709



Ref: "SiEPICfab: the Canadian silicon photonics rapid-prototyping foundry for integrated optics and quantum computing" SPIE 2021
https://www.dropbox.com/s/jutwul04a0zfl24/2021_SPIE_PW_SiEPICfab.pdf?dl=1
https://www.dropbox.com/s/2xvgjixu0ccghfs/SPIE_PW_2021_SiEPICfab_v2.mp4?dl=0

28

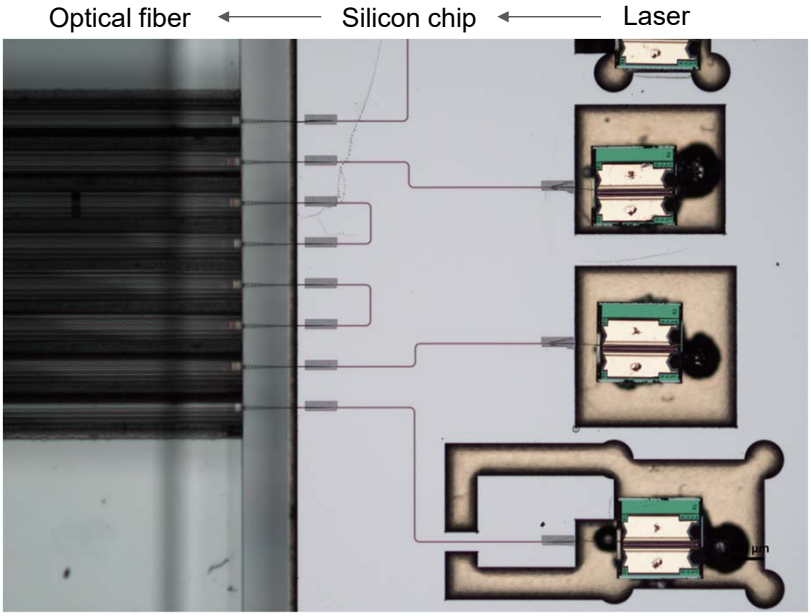
Integrating a Laser on a Silicon Photonics Chip

In-house chip fabrication

- EBL + ICP-RIE for photonic layer
- Maskless lithography + DRIE for laser recess
- Ti/Au metallization of deep trench for probing/electrical wire bonding

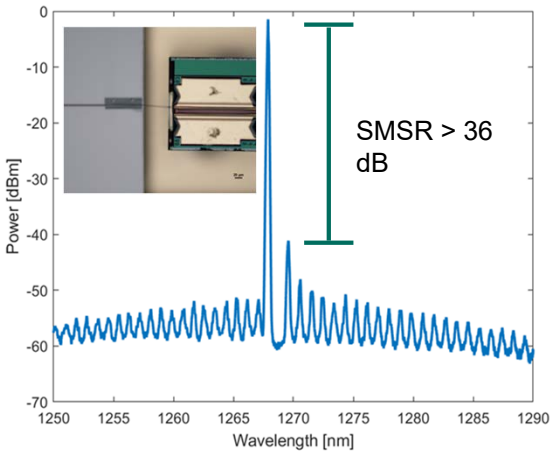
Laser attach

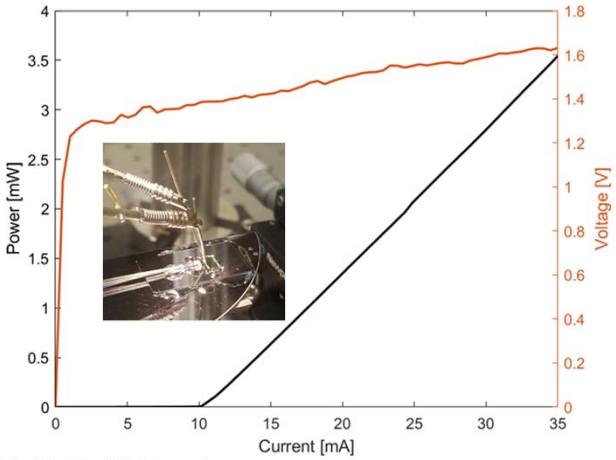
- Reflow soldering, laser placement with flip chip die bonder tool (~5 µm placement accuracy)



29

Integrating a Laser on a Silicon Photonics Chip





- Correcting for insertion loss of chip to fiber PWB (-2.25 dB @ 1270 nm):
  - Power coupled to the chip = 5.8 mW @ 35 mA, 59% ± 5% coupling efficiency - laser to chip
- Good side-mode suppression ratio
- Excellent heat sinking to silicon substrate: current tuning coefficient 10 pm/mA
- Risk: No isolator – optical feedback may degrade (or **improve**!) laser performance (linewidth, RIN)

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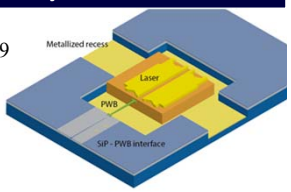
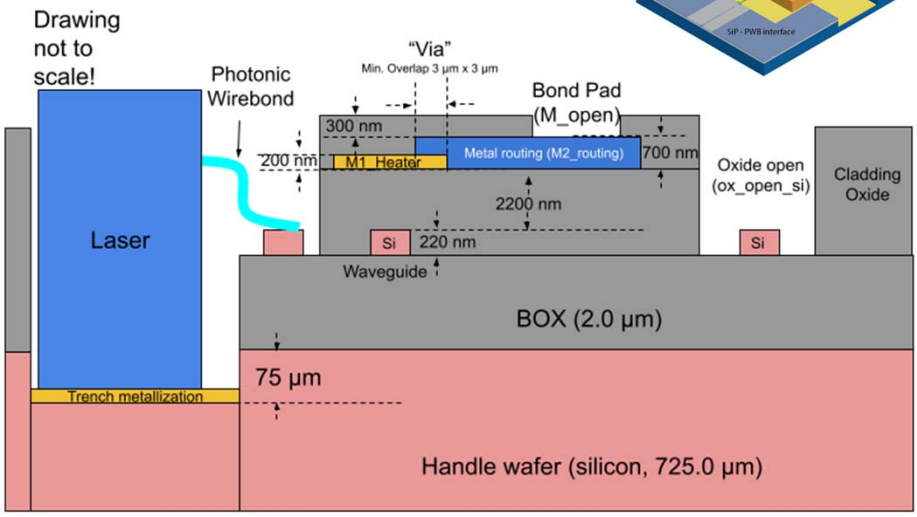
SiEPICfab Shuksan – Process Development Kit Overview: Layer Stack

- Single silicon etch process, electron-beam lithography
- Metal heaters for thermo-optic phase shifters
- Open-oxide regions
- Laser attach

US Patent Application 17969709



Layer name	Layer/datatype	Description
Si	1/0	Silicon full etch
Ox_open_Si	6/0	Oxide etch to expose the Si waveguide; used for photonic wire bonds, sensors, and depositing materials such as polymer for modulators, phase change materials, chalcogenide glasses
M1_heater	11/0	Layer to draw a heater element, Tri-layer metal: TiW alloy
M2_router	12/0	Layer to draw routing and bond pads for elements defined on layer 11/0 Tri-layer metal: TiW/Al Bilayer
M_Open	13/0	Layer to draw oxide openings. Tri-layer metal: Oxide windows
Floor Plan	99/0	Virtual Layer to define layout design area.
SEM imaging	200/0	Virtual Layer to define areas to be SEM imaged. $25 per image. The SEM site must be a 4:3 ratio rectangle. SEMs are not allowed over blackbox devices.
Text	10/0	Virtual Layer to define measurement labels on.
DevRec	68/0	Virtual Device recognition layer for DRC.
PinRec	1/10	Virtual Port/pins recognition layer for snapping and connectivity checks.
Waveguide	1/99	Virtual layer to draw waveguide paths



SiEPICfab Shuksan PDK: https://github.com/SiEPIC/SiEPICfab_Shuksan_PDK

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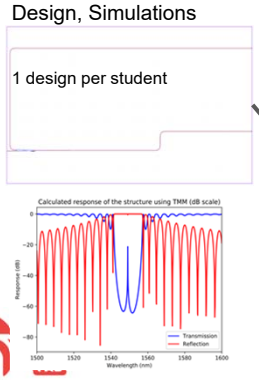
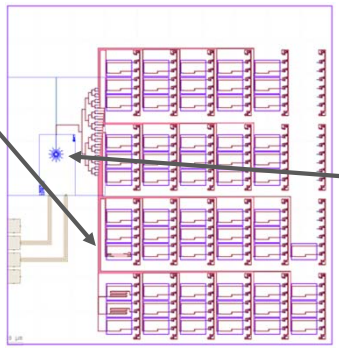
Training on laser integration

- Offered the world's first undergraduate course (UBC ELEC 413) that featured a design-fabricate-test cycle with laser integration to silicon photonics.
- Less than 6 weeks! Student design submission Feb 18, 2023. Fabrication in Feb-March. Testing March 31, 2023.
- Goal: Design, simulate and layout a photonic integrated circuit containing a 1310 nm DFB laser attached to your own circuit, such as a resonator. Use the laser to characterize the circuit.
- *Planning for a new online course "AIM Photonics-SiEPICfab: Semiconductor Laser Integration with Silicon Photonic Integrated Circuits". Target launch January 2025.*

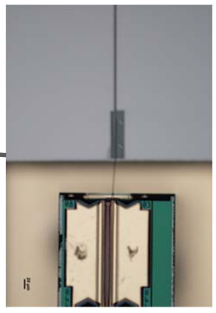
Design, Simulations

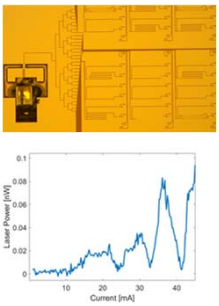


Merge, Fabrication



Experiments using laser integrated on the silicon chip





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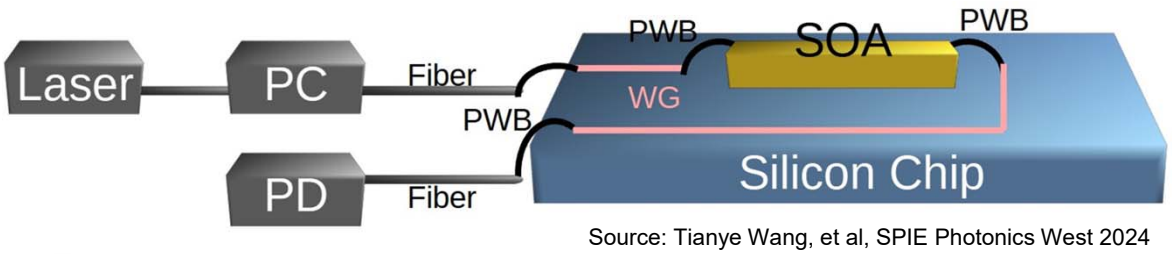
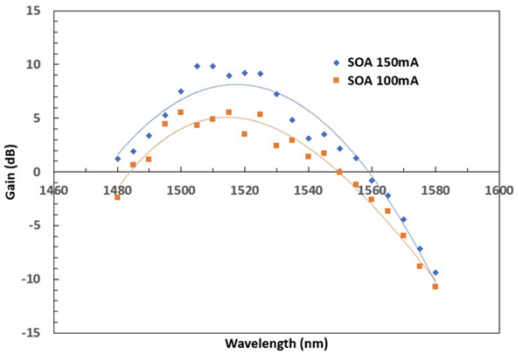
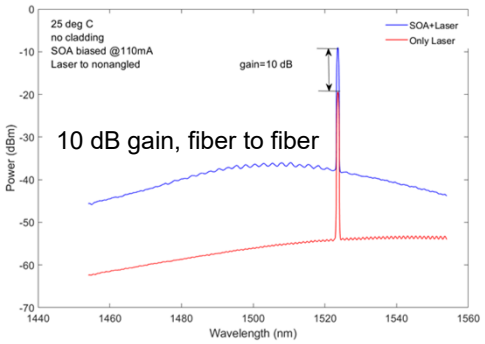
Optical Amplifier (SOA) Integration



Source: Tianye Wang, et al, SPIE Photonics West 2024





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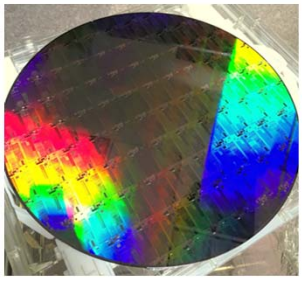
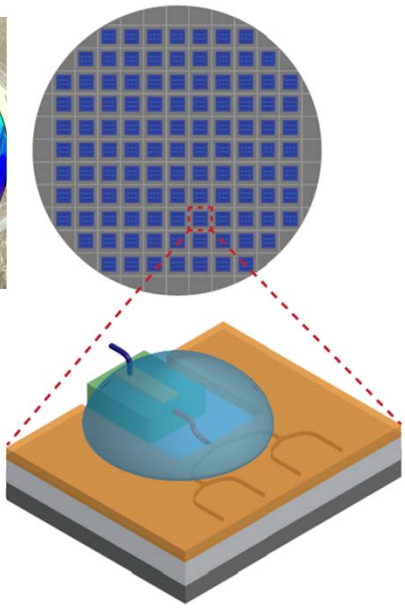
Towards wafer-scale laser integration with foundries

Anticipated process steps

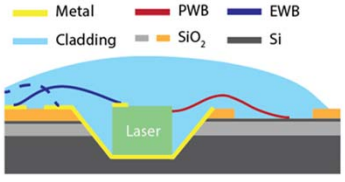
1. SiP wafer with metalized deep trenches
2. Pick and place lasers into trenches
3. EWB laser die to chip bond pads
4. PWB laser to PIC
5. Clad PWB and EWB
6. Dice
7. Follow with remaining required packaging steps (Fiber array to chip assembly, EWB to PCB, etc.)





Writing speed

- 30 seconds per laser to chip bond
- 1000 lasers in ~8 hours



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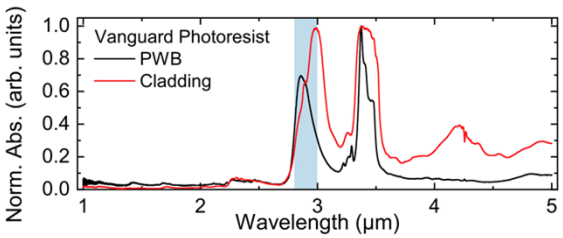
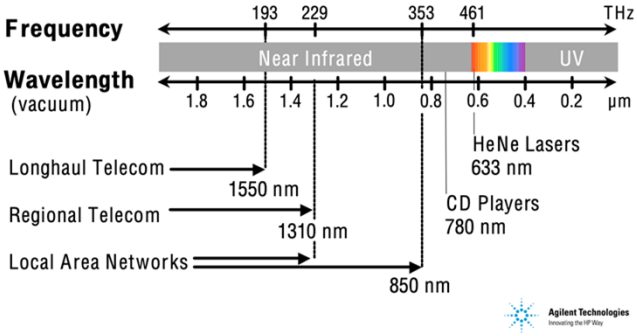
Wavelength

- PWB polymer material is transparent for green, red, infrared
  - Limit for visible applications: polymer starts absorbing ~ 450 nm
- VCSELs: 850 nm, 980, 1310, 1550 nm, etc
- DFBs for datacom/telecom: 1310, 1550 nm



Xiruo Yan, et al., APL Photonics 6, 070901 (2021); https://doi.org/10.1063/5.0049372

PWB: suitable from ~0.5 μm to 2.7 μm



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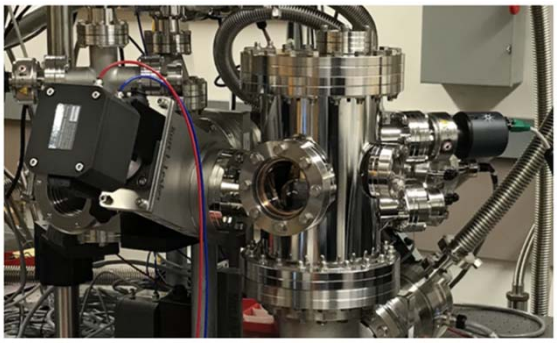
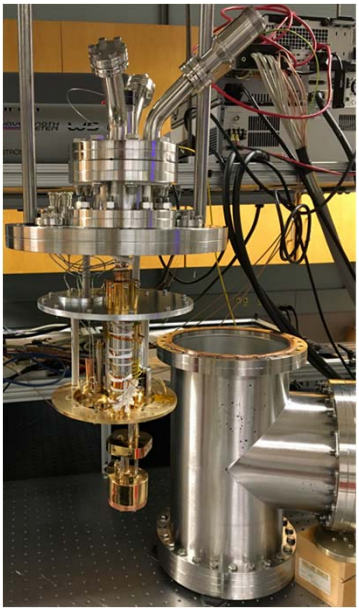
Cryo testing – using automated fibre array or photonic wire bonds

For Quantum applications





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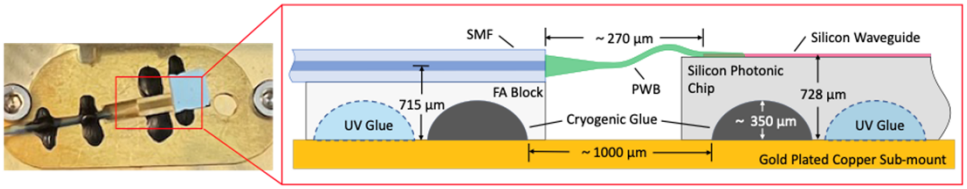
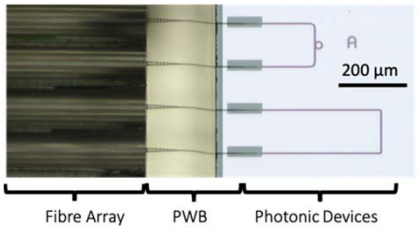
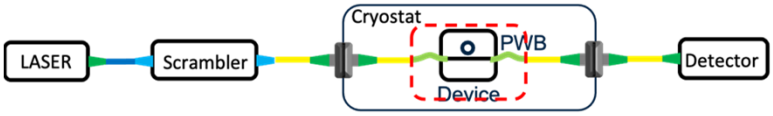
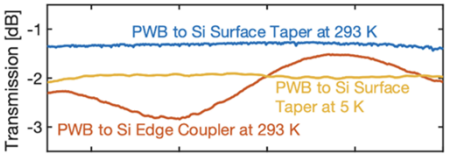
Cryo testing – using automated fibre array or photonic wire bonds

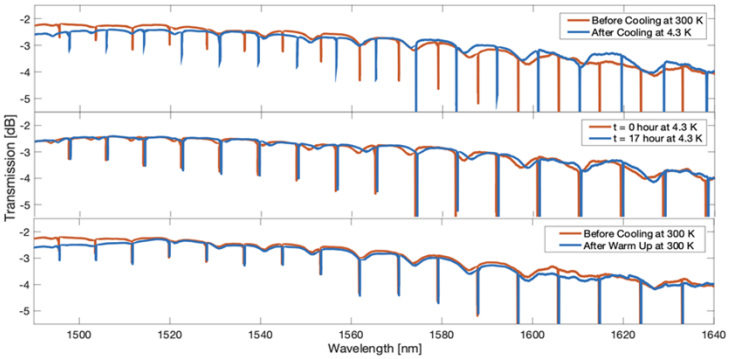


Becky Lin, et al., "Cryogenic Optical Packaging Using Photonic Wire Bonds", arXiv:2307.07496
5 K and 470 mK









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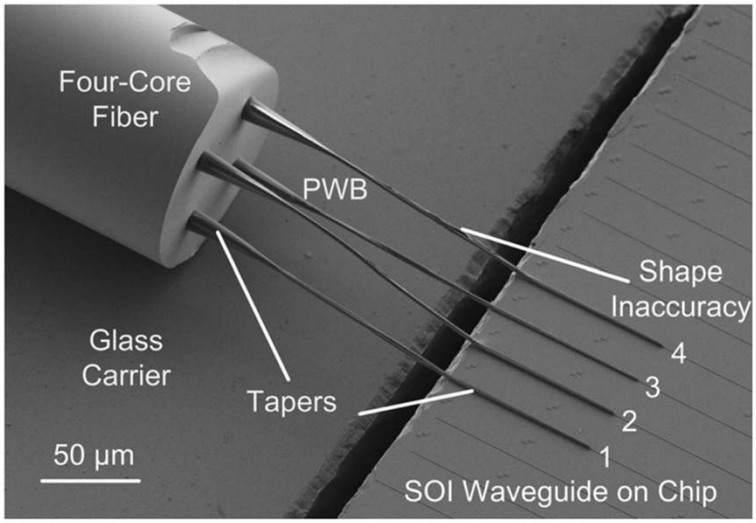
Multi-core Fibers

- Multi-core fibers are being considered for future high-density datacomm
- Demonstrated 1.7 dB coupling efficiency



Ref: N. Lindenmann, "Connecting Silicon Photonic Circuits to Multicore Fibers by Photonic Wire Bonding" IEEE JLT, 2015

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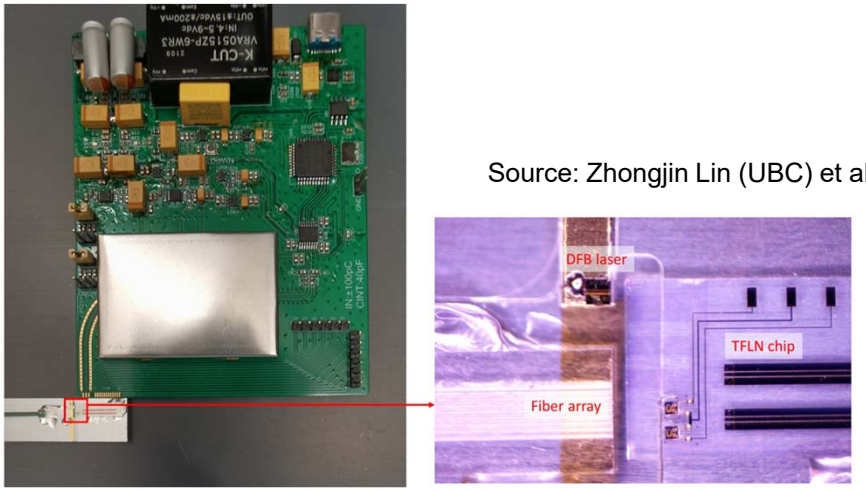
Integration of multiple chips

- No single material platform offers all functionality. Can integrate:
  - III-V lasers, SiP, thin-film Lithium Niobate, detectors, optical fibres…
- Example optical computing system, TFLN (Thin-Film Lithium Niobate) tested up to 65 GSa/s, with laser and detectors



Source: Zhongjin Lin (UBC) et al.

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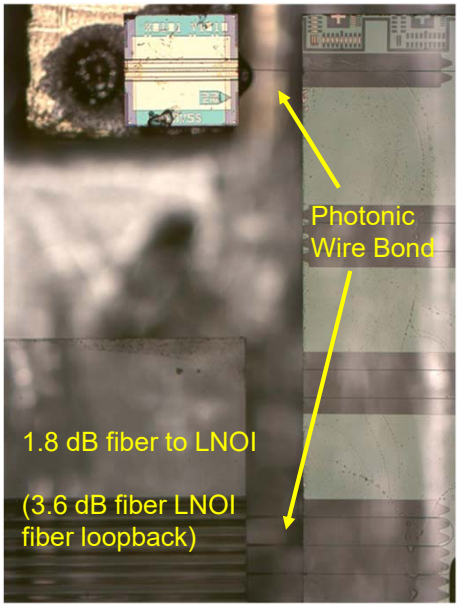
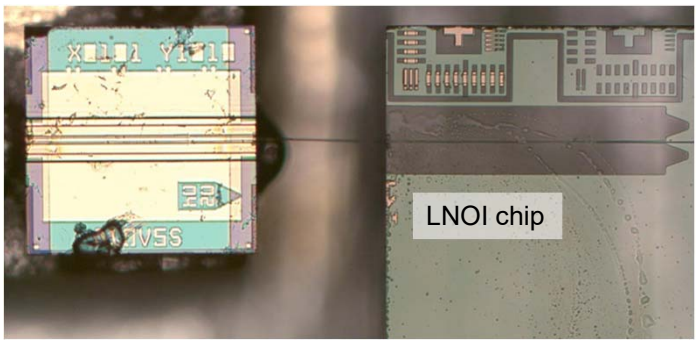
Integrating a Laser with a LNOI chip (preliminary results)





Source: Zhongjin Lin (UBC) et al.

- Height matching fiber array to chip using etched shims
- Fiber array lateral alignment performed manually
- Air-clad samples
- 1.8 dB coupling efficiency from fiber to TFLN

SiEPIC FAB UBC

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EWB vs PWB

	Electrical Wire Bond	**Photonic Wire Bond**
Data signal bandwidth	Limited, typically tens GHz	Potentially very large with multiplexing (WDM), N x tens of GHz
Flexibility	Pad pitch, >30 µm	Coupler pitch, >30 µm
Pad design	Different sizes, different metals, ESD protection	Optimal surface or edge coupler cells
Number of bonds	1 to thousands	1 to tens to hundreds (largest fiber array is 256 on 127 µm pitch)
Speed	~1 s per bond	30 s to 90 s (anticipate it will go down in next generation of tool)
Volume	Prototype to High Volume	Prototype to High Volume (not yet demonstrated)

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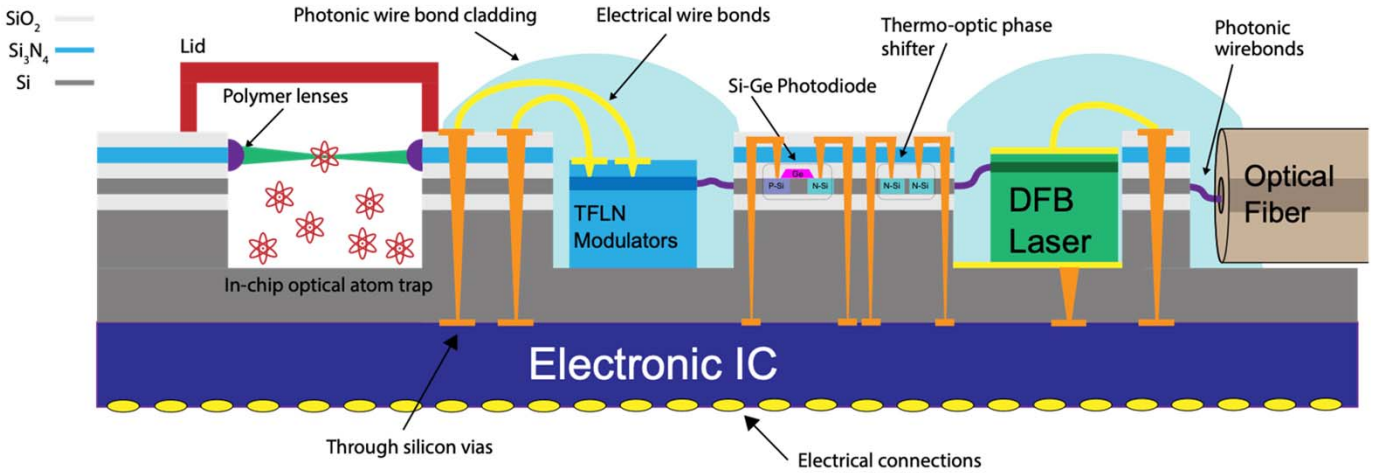
Hybrid Integrated Photonics

Long term vision: photonics integration platform for various applications, mixing different types of materials



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Conclusions

- Photonic Wire Bonds have similar strengths as Electrical Wire Bonds
- First commercial PWB tool delivered in 2020 and most activities are in prototyping. Customers are interested in getting to high volume.
- PWB as a solution for optical fiber attach
- Opportunities for multi-chip hybrid integration
  - Silicon photonics
  - III-V compound semiconductors
  - Thin-film Lithium Niobate, BTO, other platforms

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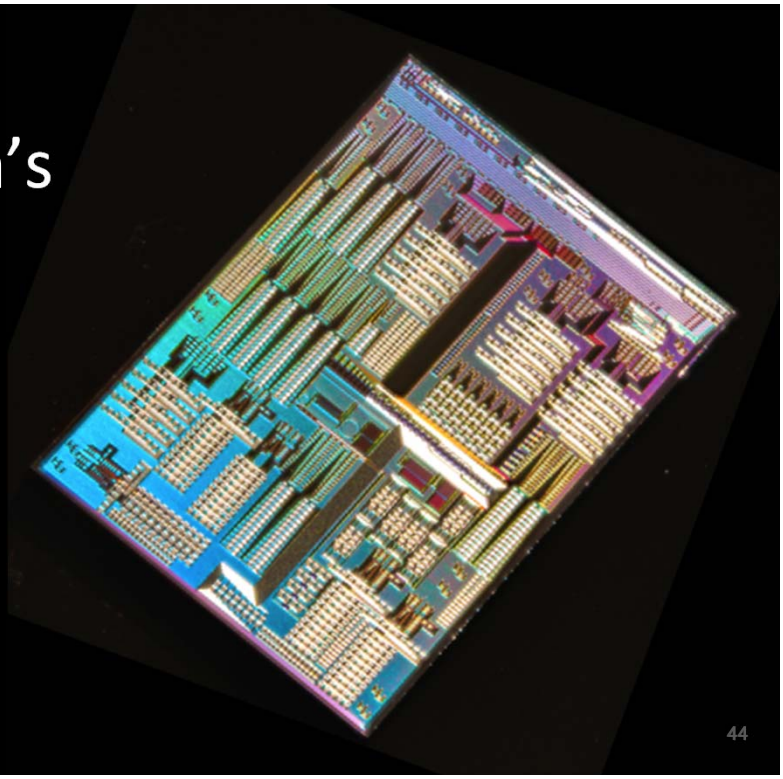
SiEPICfab – Canada's silicon photonics fabrication consortium



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SiEPIC – the Silicon Electronic Photonic Integrated Circuits program

Education – SiEPIC

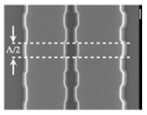
Since 2008, we have offered courses with design–fabricate–test cycles (workshop format):

- SiEPIC-Passives, SiEPIC-Actives
- 28 SiEPIC workshops so far
- Workshops have trained 596 students, from 50 universities (total of 123 groups), from 32 companies or gov't labs
- Delivered by universities and CMC
- Online course on edX.org, includes fabrication & test; Next run in Jan 2024

Fabrication – SiEPICfab

Canada's silicon photonics fabrication consortium

- University researchers, government funding
- Partners offering design tools, fabrication and MPW runs, test, packaging, incubation
- End users with applications
- Accelerate silicon photonics development cycle

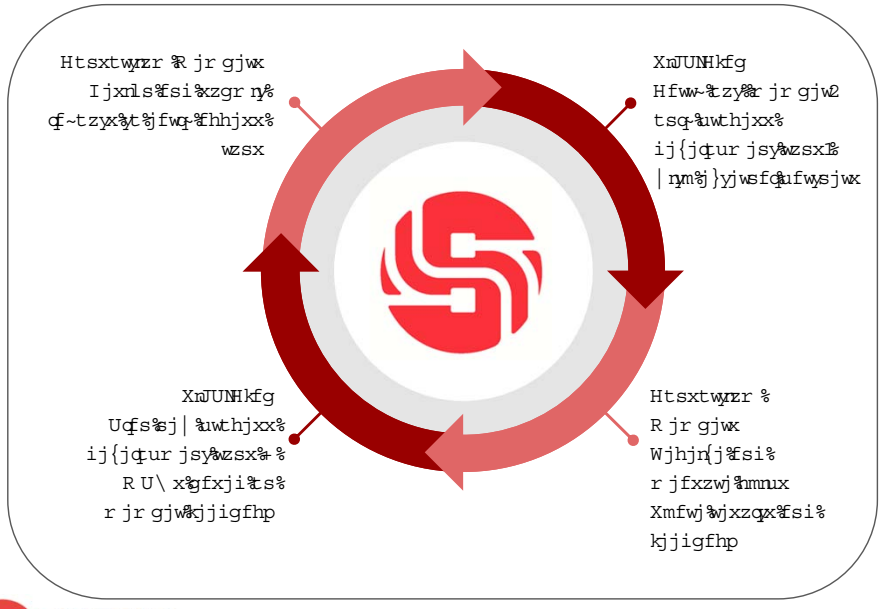


Using Electron Beam Lithography
Ref: L. Chrostowski, et al., IEEE JSTQE 2019

SiEPIC FAB

http://siepic.ca

SiEPICfab Process Development EcoSystem



Mature Processes

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APPLIED NANOTOOLS INC.

SiEPIC FAB

UBC Nanofabrication Facility - Silicon Photonics Infrastructure

- Electron beam lithography cleanroom ($0.6M)
  - Electron beam lithography, Jeol JBX-8100FS ($3M) – operational since 2018
  - 100 kV, 125 MHz, Write-field up to 1 mm x 1 mm
  - Overlay accuracy +/- 20 nm (< 10 nm typical)
  - Small pieces to full wafers up to 200 mm
- New cleanroom, Nanofab ($5M) – opened 2020; new equipment:
  - AJA sputtering / evaporator – 2018
  - Contact mask aligner – 2018
  - Heidelberg MLA150 Maskless Lithography System – 2020
  - Inductively Coupled Plasma (ICP) etcher, dedicated for Silicon – 2020
  - Vanguard 3D Laser Printer for Photonic Wire Bonds – 2020
  - Tresky Die Bonder and Component Placer, TPT Automatic Wire bonder - 2021
  - New RIE for ashing and NbTiN – 2022
  - Planning for a new PECVD for oxide and nitride

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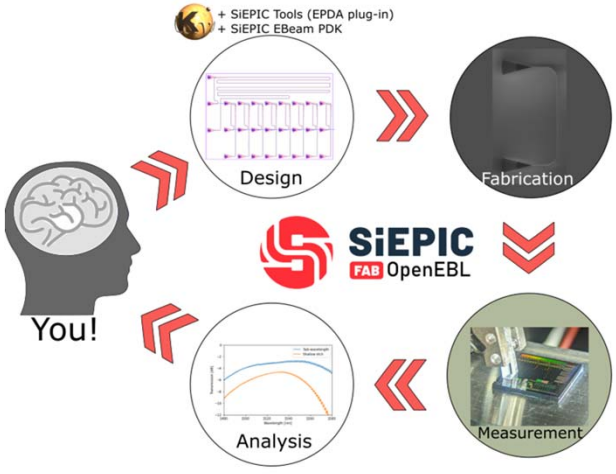
openEBL – free educational fabrication & test SiEPICfab OpenEBL

- Free fabrication and testing through the OpenEBL program.
- Limited fabrication process, single etch EBL layer, no metals or other process steps.
- Testing at UBC, and designers will be provided with results, will not receive chips.
- Primary purpose is to act as an educational platform, but may be useful for testing new designs.
- More information on OpenEBL can be found here: https://siepic.ca/openebl/



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Contributing Organizations to Photonic Wire Bonding at UBC

Equipment and Infrastructure

UBC
INNOVATION Canada Foundation for Innovation / Fondation canadienne pour l'innovation
Stewart Blusson Quantum Matter Institute, THE UNIVERSITY OF BRITISH COLUMBIA

PDK and MPW:

CMC MICROSYSTEMS
Ansys / LUMERICAL
cadence
LUCEDA PHOTONICS

Research and Development

REMAP Refined Manufacturing Acceleration Process
AAPF Accélération de l'amélioration des processus de fabrication
Celestica
AEPONYX PHOTONICS IN MOTION
vanguard AUTOMATION
UBC
SiEPIC FAB
DREAM PHOTONICS
ANT APPLIED NANOTOOLS INC.

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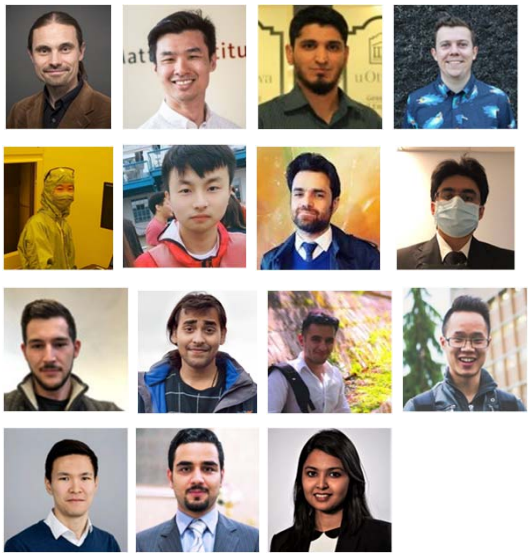
Contributors to the Photonic Wire Bond MPW project

- Lukas Chrostowski, Professor, SiEPICfab PI/UBC/Dream Photonics
- Serge Khorev, Steve Gou, Project Manager, Project management
- Kashif Awan, Research Associate, UBC: EBeam lithography development
- Matthew Mitchell, Postdoctoral Fellow, Dream Photonics/UBC: Photonic wirebond development, SiP chip fabrication and laser integration
- Becky Lin, MASc student, UBC: Photonic wirebond development and cryogenic experiments
- Shangxuan Yu, MASc student, UBC: PWB Laser integration
- Iman Taghavi, PhD student, UBC: SOA integration, polymer modulators
- Naman Pant, Dream Photonics: Photonic wirebond development
- Alexander Tofini, MASc student, UBC: Simulation and modeling
- Colin Parkyn, coop, UWaterloo: Photonic wirebond development
- Davin Birdi, coop, UBC: Photonic wirebond development
- Sheri Jahan Chowdhury, MASc student: SiP chip fabrication, laser test
- Jaspreet Jhoja, PDK development, SiEPICfab: PDK Development
- Mustafa Hammood, PhD student, UBC/Dream Photonics: PDK Dev
- Sean Lam, MASc student, UBC: PDK Development
- Dias Azhihulov, MASc student, UBC: PDK Development
- Omid Esmaeeli, PhD student, UBC: PDK Development
- Applied Nanotools: SiP chip fabrication and process development
- CMC Microsystems: Aggregation and invoicing



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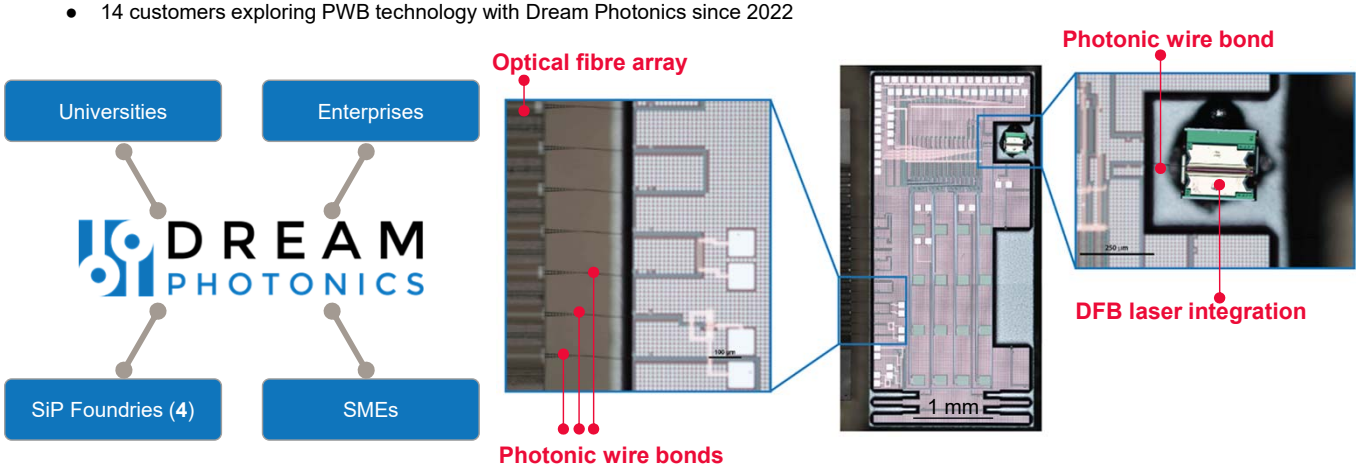
Dream Photonics — Building the photonic ecosystem

- Spin-out of UBC utilizing the PWB tool for hybrid integration and packaging
- >10 employees - building advanced manufacturing capabilities
- 14 customers exploring PWB technology with Dream Photonics since 2022



Hybrid integration as a service using photonic wire bonding and lens printing – see more at dreamphotonics.com

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Thank you

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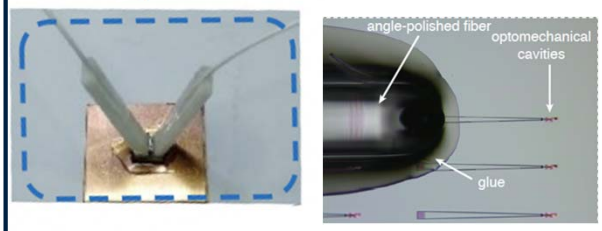
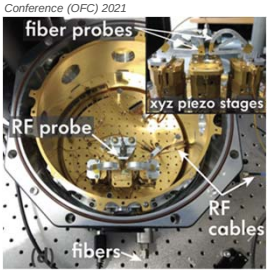
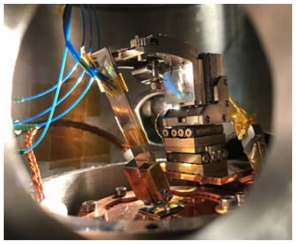
Cryo testing – using automated fibre array or photonic wire bonds

Fixed Coupling via Glued Fibre(s)	Flexible Coupling via Piezo Stages
Minmin You, Zude Lin, Xiuyan Li, and Jingquan Liu, "Chip-Scale Silicon Ring Resonators for Cryogenic Temperature Sensing," J. Lightwave Technol. 38, 5768-5773 (2020) 	H. Gevorgyan, A. Khilo, D. Van Orden, D. Onural, B. Yin, M. T. Wade, V. M. Stojanović, and M. A. Popović, "Cryo-Compatible, Silicon Spoked-Ring Modulator in a 45nm CMOS Platform for 4K-to-Room-Temperature Optical Links," in *Optical Fiber Communication Conference (OFC) 2021*   Prof. Jeff Young's Lab (AMPEL 347)
[+] Compact integration, small footprint, low heat load [+] Low cost [+] No extra electrical/software controls needed	[+] Measure multiple devices at cryogenic temperature [+] Reuse chip
[-] Require individual active alignment during assembling [-] Prone to breakage from thermal mechanical stress [-] Low optical bandwidth, high insertion loss [-] Spectral shift during cooldown	[-] High cost [-] Require additional electrical and software controls [-] Misalignments during cooldown due to thermal induced movement cause signal lost [-] Require large footprint

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Photonic wire bonding FAQs

- What is the maximum power the PWB can tolerate?
  - Vanguard has shown no degradation for a fiber-to-fiber PWB up to 29 dBm at 1540 nm
- Electrical wire bonding or photonic wire bonding first?
  - Depends on the assembly, but the recommendation is that electrical wire bonding should be performed last.
- Are the PWBs polarization maintaining?
  - Yes - the PWBs we are currently using have rectangular or elliptical cross-sections.
  - You can even build polarization rotators/splitters out of them
- Can PWBs be operated at visible wavelengths
  - Samples have been fabricated, waiting for test results
  - 780 nm – similar insertion losses
- How mechanically stable are the PWBs?
  - Vibration tests have shown no difference in reliability between clad and un-clad PWBs.
  - Mass and forces are so low on these structures which makes them resilient
- Does oxide need to be removed for PWB?
  - For surface tapers, yes, but not for edge coupler interfaces.

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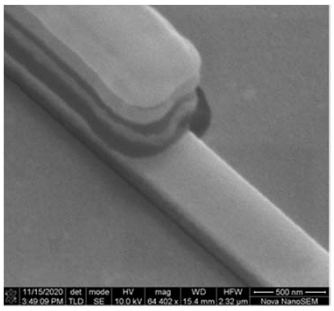
Photonic wire bonding FAQs

- Do you have any data on the reflections caused by the PWBs?
  - -30 dB return loss
- How long does it take to write a single PWB?
  - Depends on the size, but on the order of 30 - 120 seconds
- Is there any data on PWB performance in cryogenic conditions?
  - Ref: Becky Lin, arXiv:2307.07496
- Is there any long term reliability data on the PWBs?
  - Demonstrated for waveguide-to-waveguide bonds on the same SiP chip:
    - Telcordia Ref. 3.3.2.2: 225 cycles of -40 °C to +85 °C (> 200 h)
    - Telcordia Ref. 3.3.2.3: 85°C / 85% humidity, 3500 h

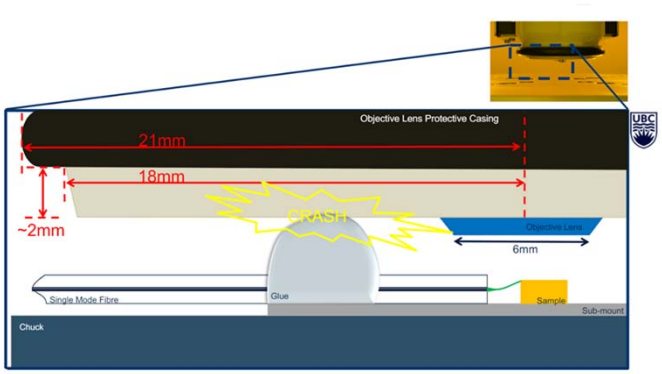
Photonic wire bonding FAQs

- What are the main sources of loss in the PWB?
  - Under investigation.
    - Bend loss due to radiation
      - negligible for bends with radius > 100 μm
    - Roughness of PWB (it is written layer by layer)
    - Placement accuracy (~30 nm)
    - PWB interface design versus what is fabricated
    - Mode and index matching
- How far apart can components be for PWB, and what is the alignment tolerance?
  - The writefield is ~ 350 μm x 350 μm, which limits maximum distance between components.
  - Absolute maximum vertical offset between components is 250 μm. However, for a low loss bond, alignment accuracy of components should be kept <30 μm as a general rule.



Assembly Design Kit

- Assembly Design Kit
  - Documentation on building assemblies, rules for chip designers, GDS cells for fiber/laser coupling
- Some considerations
  - Sample height: limit of 250 µm above the PWB
  - Order of operation of electrical wire bonding (EWB), and photonic wire bonding (PWB) + cladding:
    - EWB → PWB → PWB Cladding
    - PWB → EWB → PWB Cladding
    - PWB → PWB Cladding → EWB
  - Component misalignment < 30 µm



Source: Becky Lin

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