Using Glass Carriers for Precision Wafer Thinning and Warpage Control

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Semiconductor Technologies and Solutions
Corning Incorporated

IEEE ELECTRONICS PACKAGING SOCIETY

Outline

- Introduction
- Wafter ultra-thinning
  - Ultra-low-TTV glass carrier
  - ALoT – advanced lift-off technology
  - Results
- Warp control for buildup structures
  - Fundamentals
  - Simulation examples
- Conclusions

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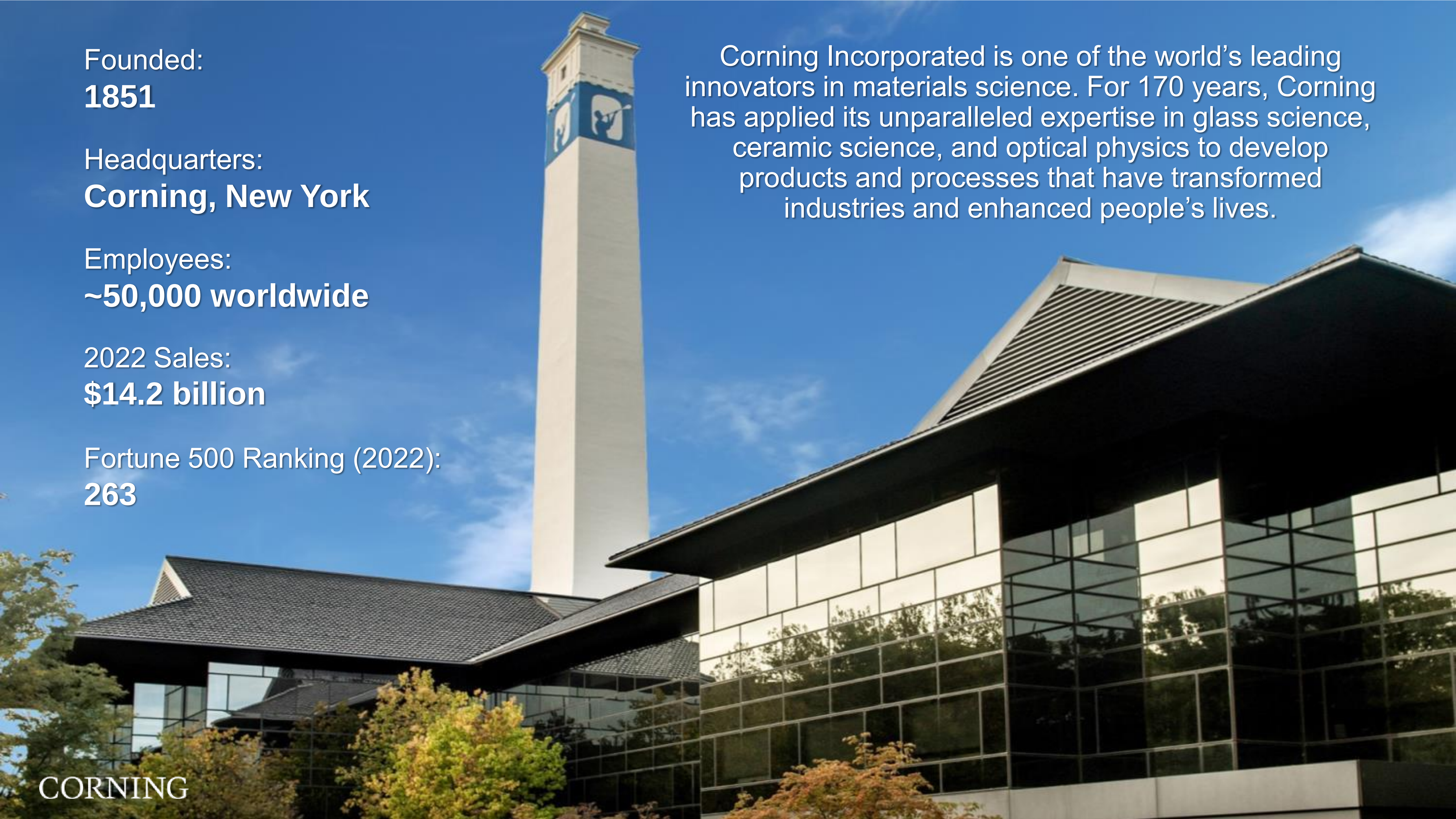


Founded:
1851

Headquarters:
Corning, New York

Employees:
~50,000 worldwide

2022 Sales:
$14.2 billion

Fortune 500 Ranking (2022):
263

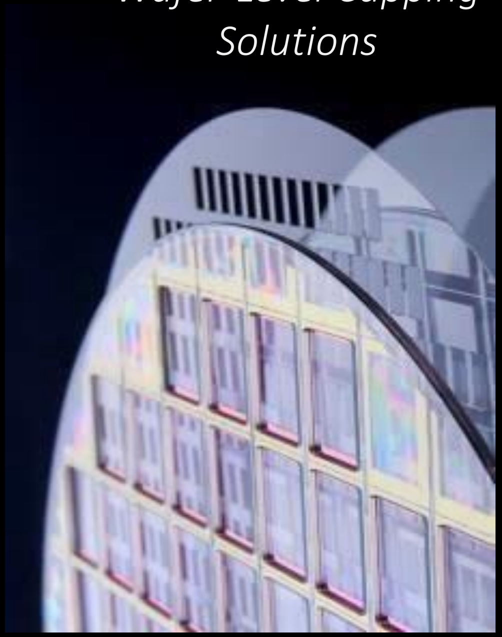
Corning Incorporated is one of the world’s leading innovators in materials science. For 170 years, Corning has applied its unparalleled expertise in glass science, ceramic science, and optical physics to develop products and processes that have transformed industries and enhanced people’s lives.

CORNING

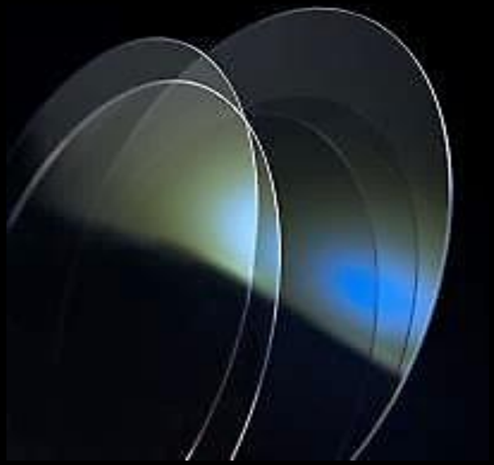
Corning's *Packaging & Wafer Business as part of Semiconductor Technologies & Solutions (STS)* offers industry-leading wafer and panel format glass-based substrates into the market

Our products help customers deliver increasingly demanding functionality and form factor requirements in consumer devices and Internet of Things (IoT) applications.

Wafer-Level Capping Solutions



Wafer-Level Optic Solutions



Carrier Solutions

Custom Glass Solutions

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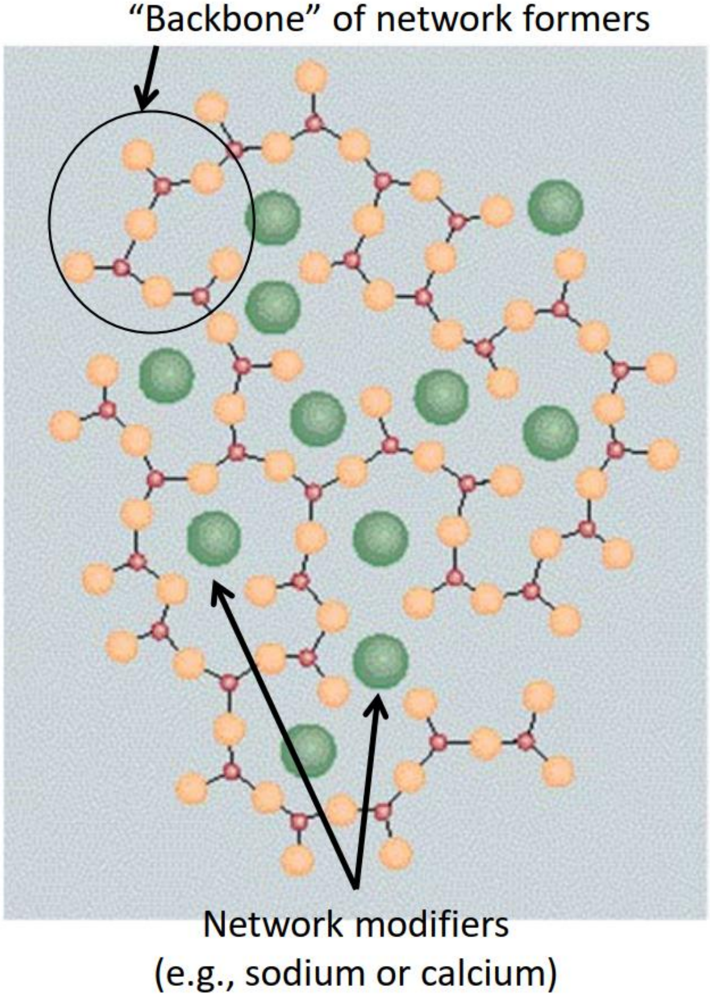
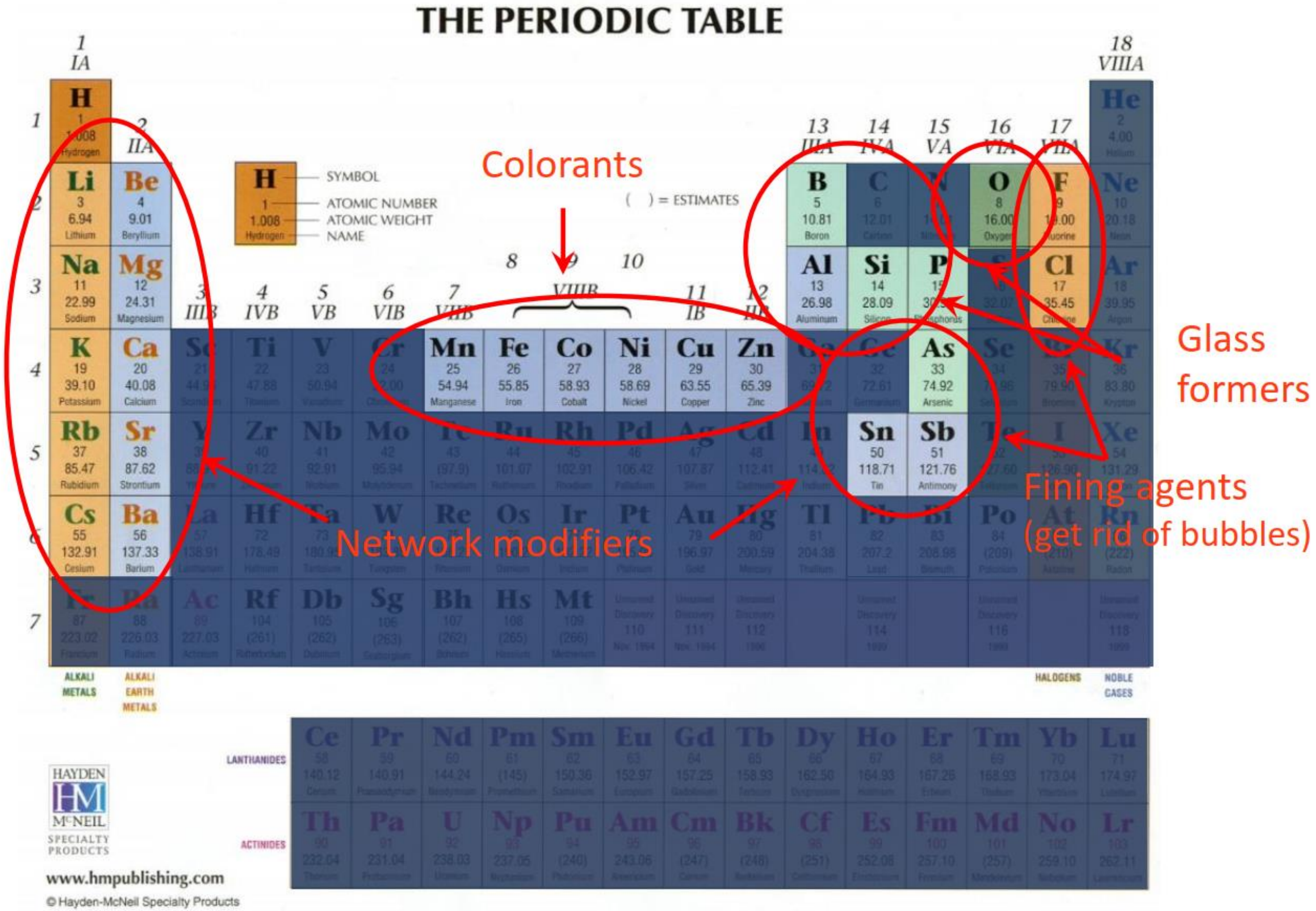
Glass is made up of key ingredients of the periodic table





THE PERIODIC TABLE

	1 IA	2 IIA	3 IIIB	4 IVB	5 VB	6 VIB	7 VIIB	8	9 VIIIB	10	11 IB	12 IIB	13 IIIA	14 IVA	15 VA	16 VIA	17 VIIA	18 VIIIA
1	H 1 1.008 Hydrogen																	He 2 4.00 Helium
2	Li 3 6.94 Lithium	Be 4 9.01 Beryllium											B 5 10.81 Boron	C 6 12.01 Carbon	N 7 14.01 Nitrogen	O 8 16.00 Oxygen	F 9 19.00 Fluorine	Ne 10 20.18 Neon
3	Na 11 22.99 Sodium	Mg 12 24.31 Magnesium											Al 13 26.98 Aluminum	Si 14 28.09 Silicon	P 15 30.97 Phosphorus	S 16 32.07 Sulfur	Cl 17 35.45 Chlorine	Ar 18 39.95 Argon
4	K 19 39.10 Potassium	Ca 20 40.08 Calcium	Sc 21 44.96 Scandium	Ti 22 47.88 Titanium	V 23 50.94 Vanadium	Cr 24 52.00 Chromium	Mn 25 54.94 Manganese	Fe 26 55.85 Iron	Co 27 58.93 Cobalt	Ni 28 58.69 Nickel	Cu 29 63.55 Copper	Zn 30 65.39 Zinc	Ga 31 69.72 Gallium	Ge 32 72.61 Germanium	As 33 74.92 Arsenic	Se 34 78.96 Selenium	Br 35 79.90 Bromine	Kr 36 83.80 Krypton
5	Rb 37 85.47 Rubidium	Sr 38 87.62 Strontium	Y 39 88.91 Yttrium	Zr 40 91.22 Zirconium	Nb 41 92.91 Niobium	Mo 42 95.94 Molybdenum	Tc 43 (97.9) Technetium	Ru 44 101.07 Ruthenium	Rh 45 102.91 Rhodium	Pd 46 106.42 Palladium	Ag 47 107.87 Silver	Cd 48 112.41 Cadmium	In 49 114.82 Indium	Sn 50 118.71 Tin	Sb 51 121.76 Antimony	Te 52 127.60 Tellurium	I 53 126.90 Iodine	Xe 54 131.29 Xenon
6	Cs 55 132.91 Cesium	Ba 56 137.33 Barium	La 57 138.91 Lanthanum	Hf 72 178.49 Hafnium	Ta 73 180.95 Tantalum	W 74 183.84 Tungsten	Re 75 186.21 Rhenium	Os 76 190.23 Osmium	Ir 77 192.22 Iridium	Pt 78 195.08 Platinum	Au 79 196.97 Gold	Hg 80 200.59 Mercury	Tl 81 204.38 Thallium	Pb 82 207.2 Lead	Bi 83 208.98 Bismuth	Po 84 (209) Polonium	At 85 (210) Astatine	Rn 86 (222) Radon
7	Fr 87 223.02 Francium	Ra 88 226.03 Radium	Ac 89 227.03 Actinium	Rf 104 (261) Rutherfordium	Db 105 (262) Dubnium	Sg 106 (263) Seaborgium	Bh 107 (262) Bohrium	Hs 108 (265) Hassium	Mt 109 (266) Meitnerium	Unnamed Discovery 110 Nov. 1994	Unnamed Discovery 111 Nov. 1994	Unnamed Discovery 112 1996		Unnamed Discovery 114 1999		Unnamed Discovery 116 1999		Unnamed Discovery 118 1999
	ALKALI METALS	ALKALI EARTH METALS															HALOGENS	NOBLE CASES

LANTHANIDES	Ce 58 140.12 Cerium	Pr 59 140.91 Praseodymium	Nd 60 144.24 Neodymium	Pm 61 (145) Promethium	Sm 62 150.36 Samarium	Eu 63 152.97 Europium	Gd 64 157.25 Gadolinium	Tb 65 158.93 Terbium	Dy 66 162.50 Dysprosium	Ho 67 164.93 Holmium	Er 68 167.26 Erbium	Tm 69 168.93 Thulium	Yb 70 173.04 Ytterbium	Lu 71 174.97 Lutetium
ACTINIDES	Th 90 232.04 Thorium	Pa 91 231.04 Protactinium	U 92 238.03 Uranium	Np 93 237.05 Neptunium	Pu 94 (240) Plutonium	Am 95 243.06 Americium	Cm 96 (247) Curium	Bk 97 (248) Berkelium	Cf 98 (251) Californium	Es 99 252.08 Einsteinium	Fm 100 257.10 Fermium	Md 101 (257) Mendelevium	No 102 259.10 Nobelium	Lr 103 262.11 Lawrencium

H — SYMBOL
1 — ATOMIC NUMBER
1.008 — ATOMIC WEIGHT
Hydrogen — NAME

( ) = ESTIMATES

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Glass properties are tailorable using well-known relationships

Component	Role	Expansion	Density	Modulus	Hardness	Durability	Transmission
SiO_2	NF	-	-	-	-	+	
Al_2O_3	NF	-	+	+	+	+	
B_2O_3	NF	-	-	-	-	+	
Li_2O	M	+		-	-	-	
Na_2O	M	+		-	-	-	
K_2O	M	+	+	-	-	-	
MgO	M			+	+	+	
CaO	M			+	+	+	
TiO_2	C		+	+	+	+	-
ZrO_2	NF/M		+	+	+	+	
Sb_2O_3	F	+	+	-	-	+	
SnO_2	F			+	+	+	

Key

+ = Component increases this property

- = Component decreases this property

= Component has little effect on this property

NF: Network Former
M: Modifier
C: Colorant
F: Finer

Glass scientists tailor chemical compositions to customers requirements

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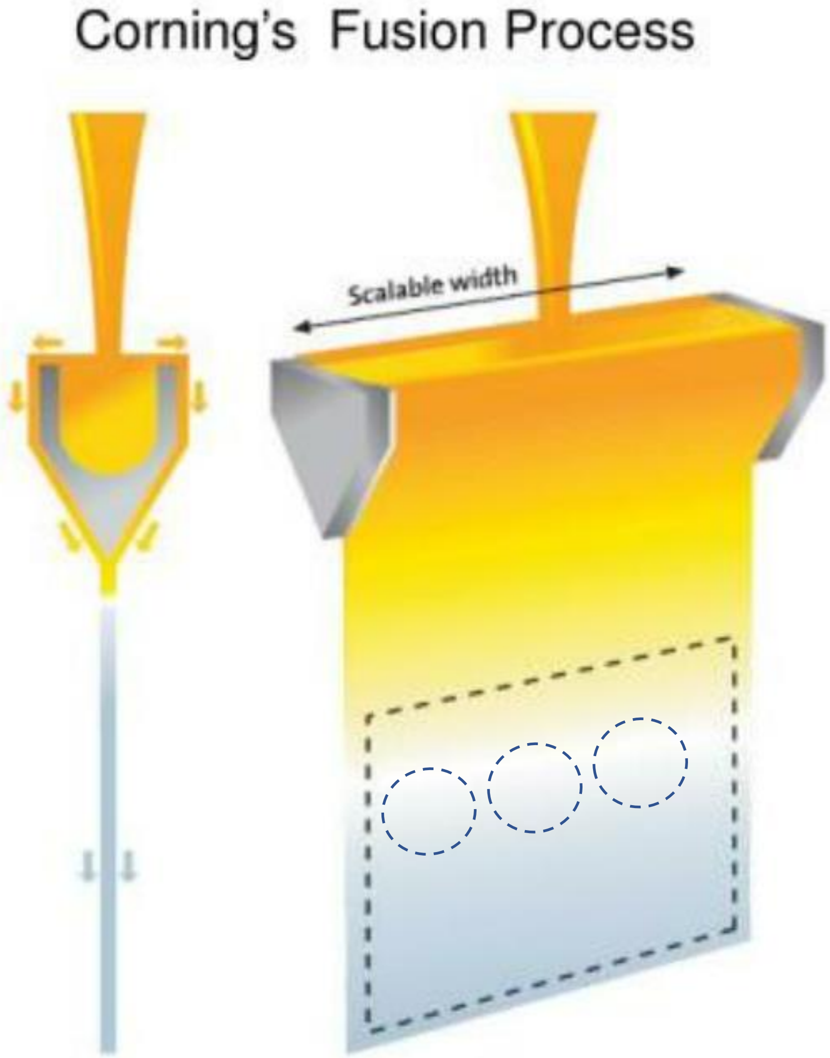
Fusion is a highly capable sheet forming technology



- Many different compositions
- Typical thickness 0.1-3.0mm
- Width as large as 3m
- Flat: low warp as-made
- Uniform thickness: low TTV
- Pristine surfaces

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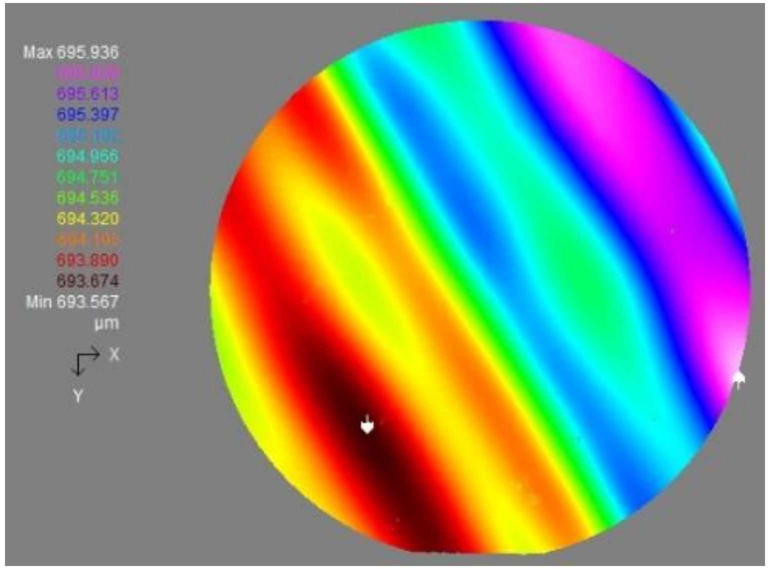
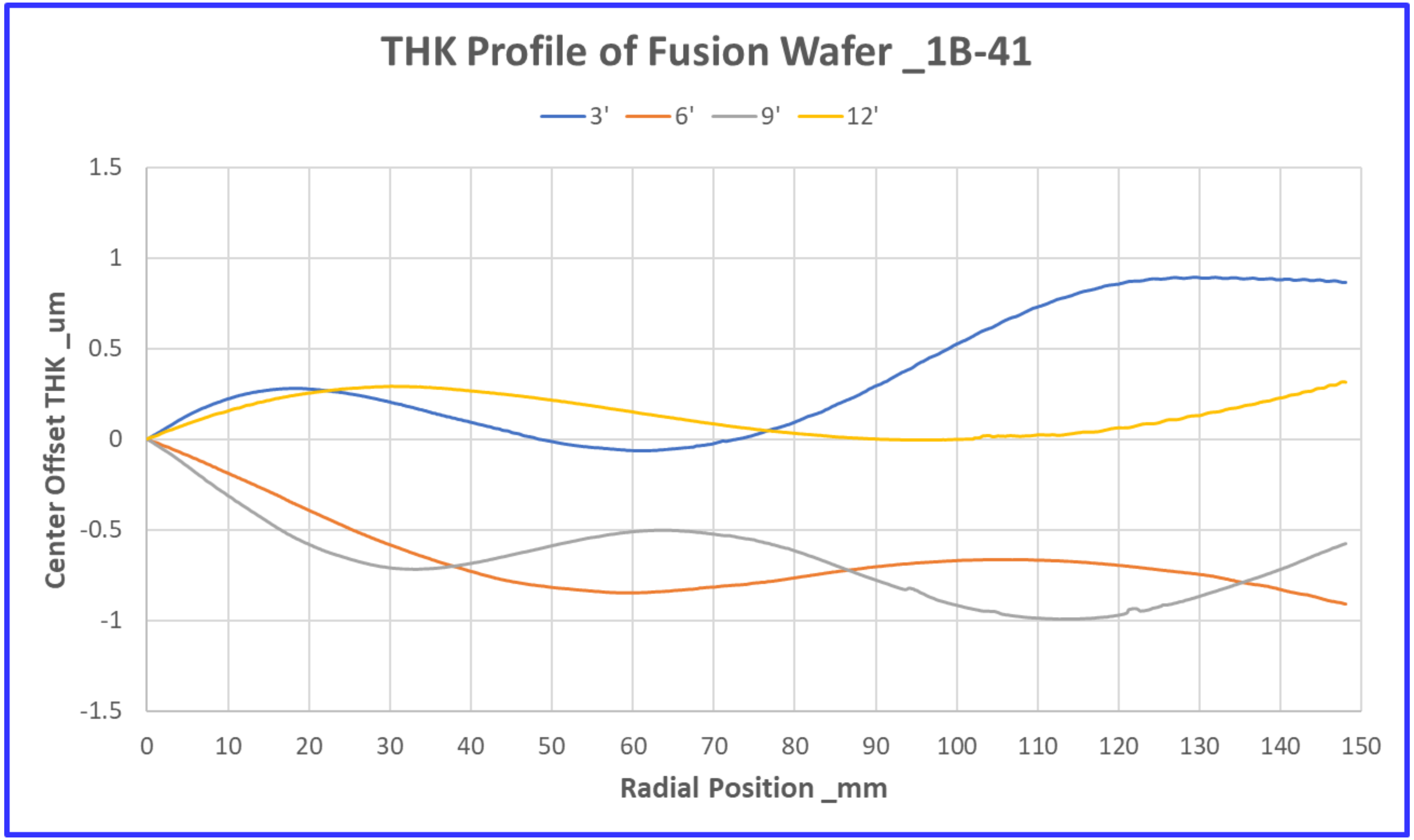
Fusion surface profile

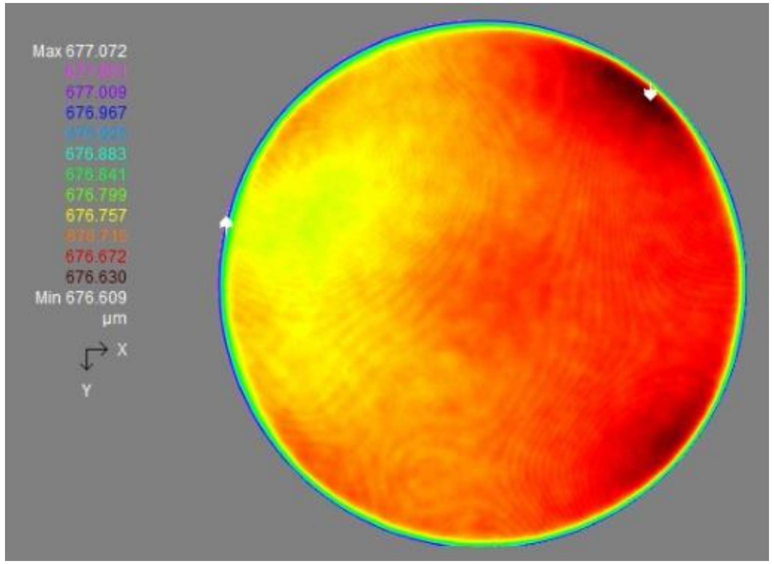
draw direction

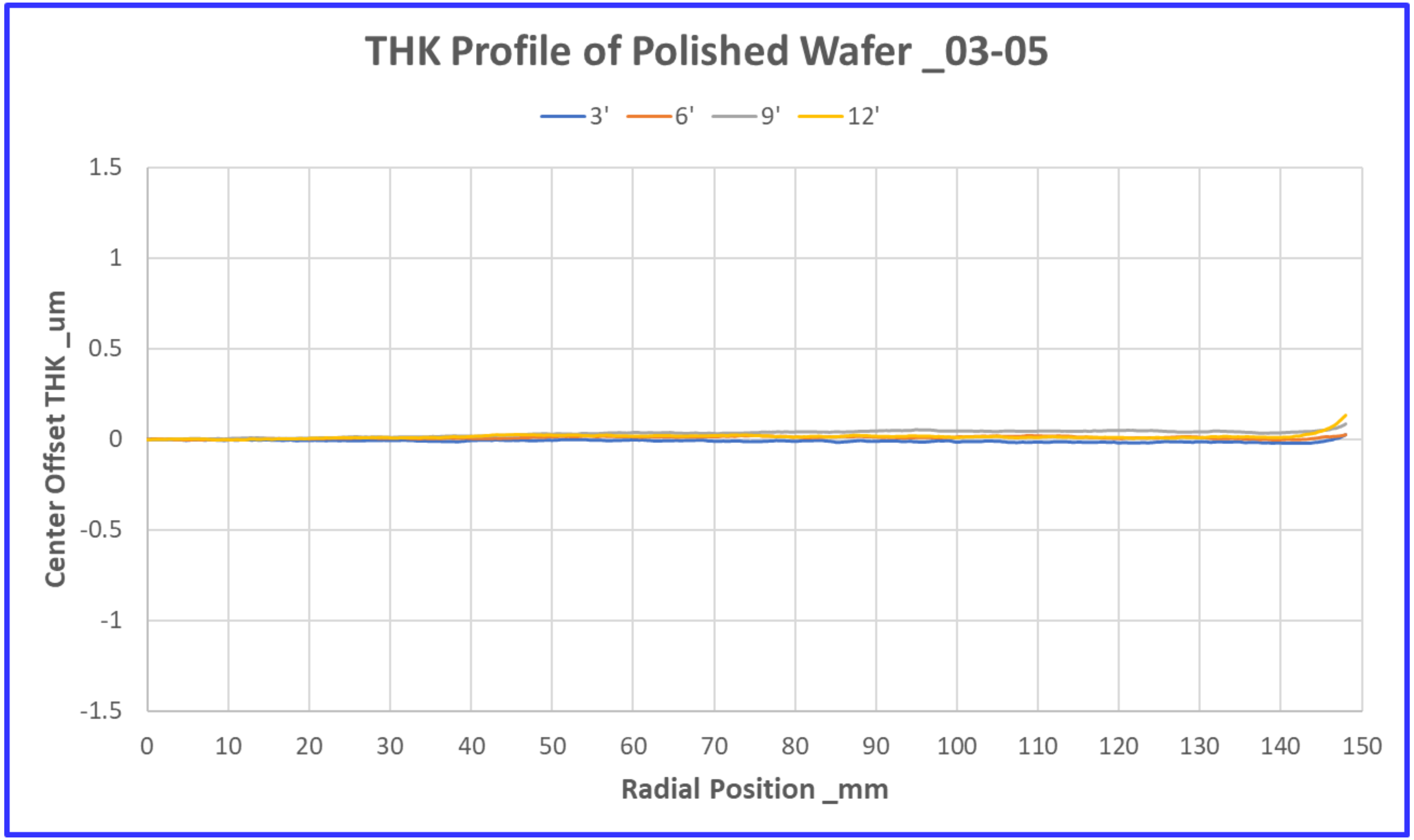




Data based on results of internal Corning studies

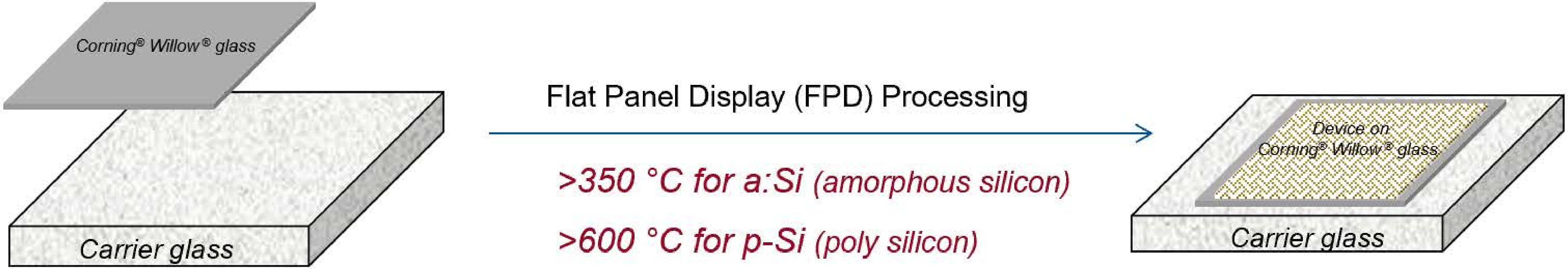
Polished surface profile





Data based on results of internal Corning studies

ALoT *(Advanced Liftoff Technology)* Introduction



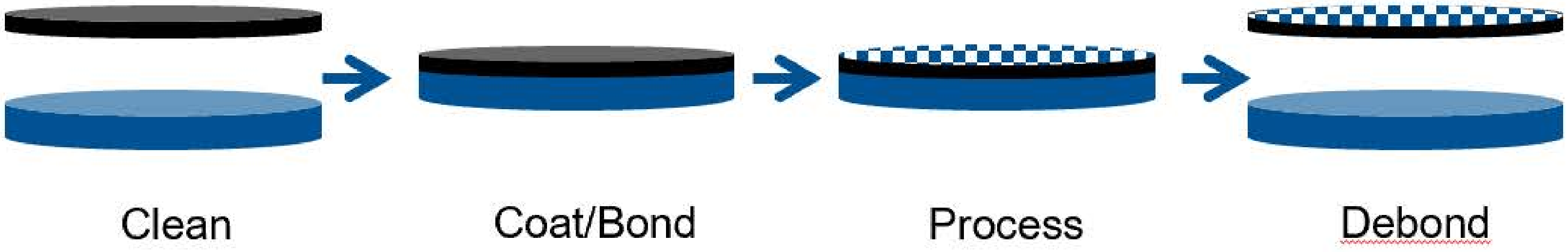
Flat Panel Display (FPD) Processing

>350 °C for a:Si (amorphous silicon)

>600 °C for p-Si (poly silicon)

From display panels

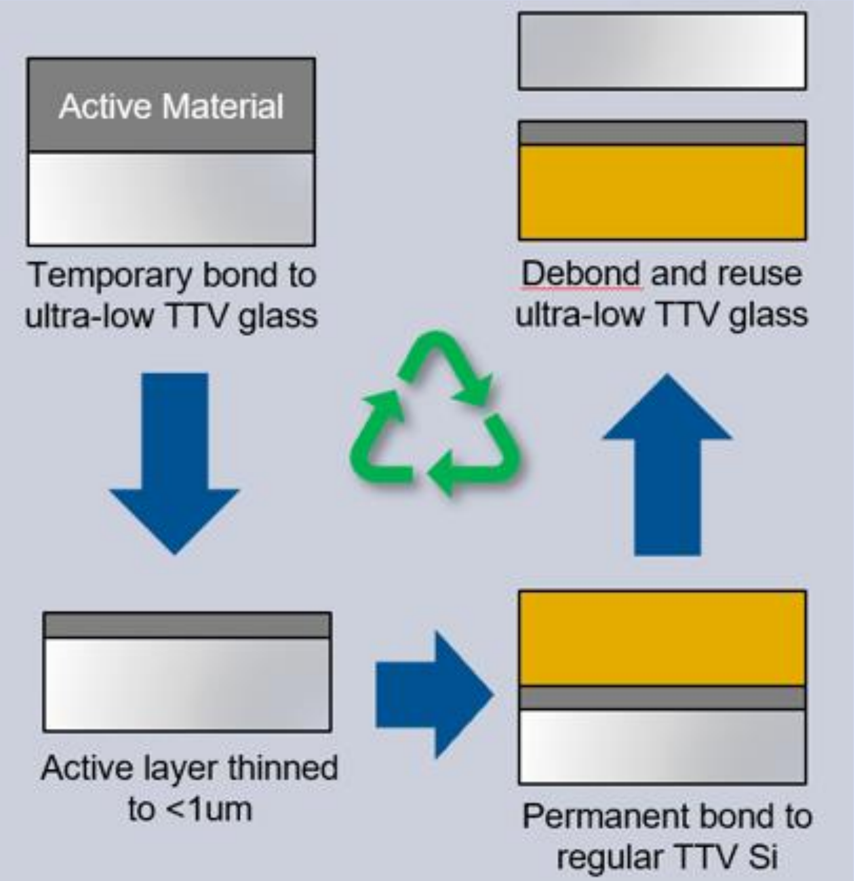
To semiconductor wafers



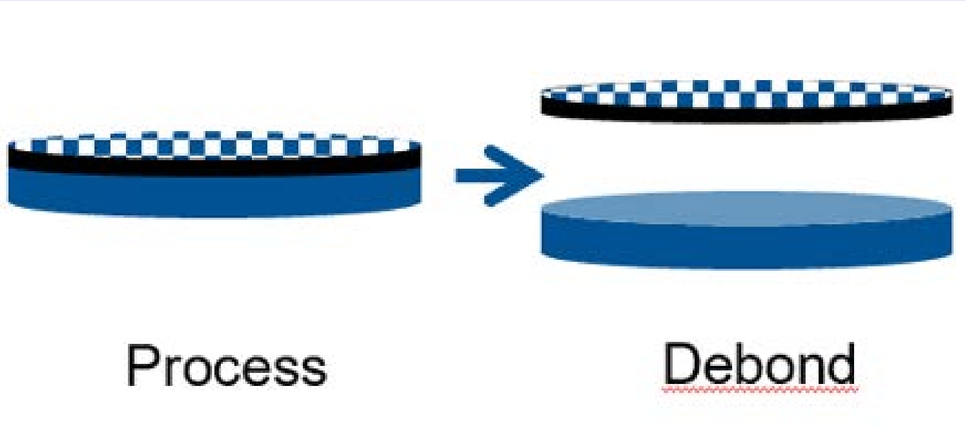
Key benefits: high temperature and near-zero-TTV

Near-zero TTV	High Temperature

Near-zero TTV

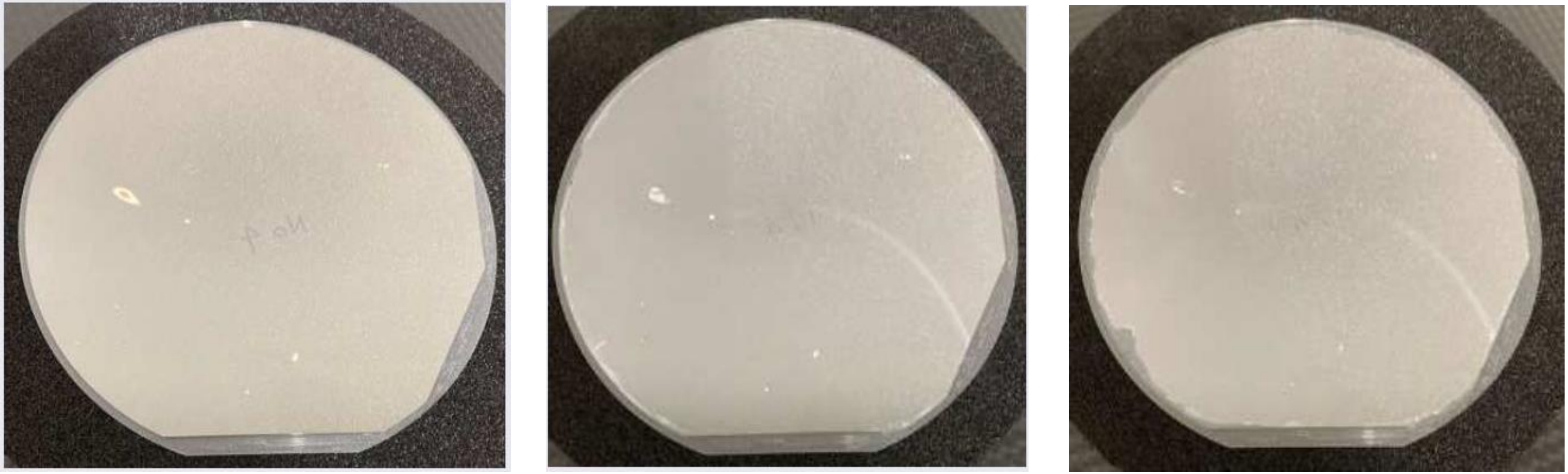


High Temperature



- Commercial adhesives < 350C
- Many semicon processes need >400C

Thinning down to 5um has been demonstrated



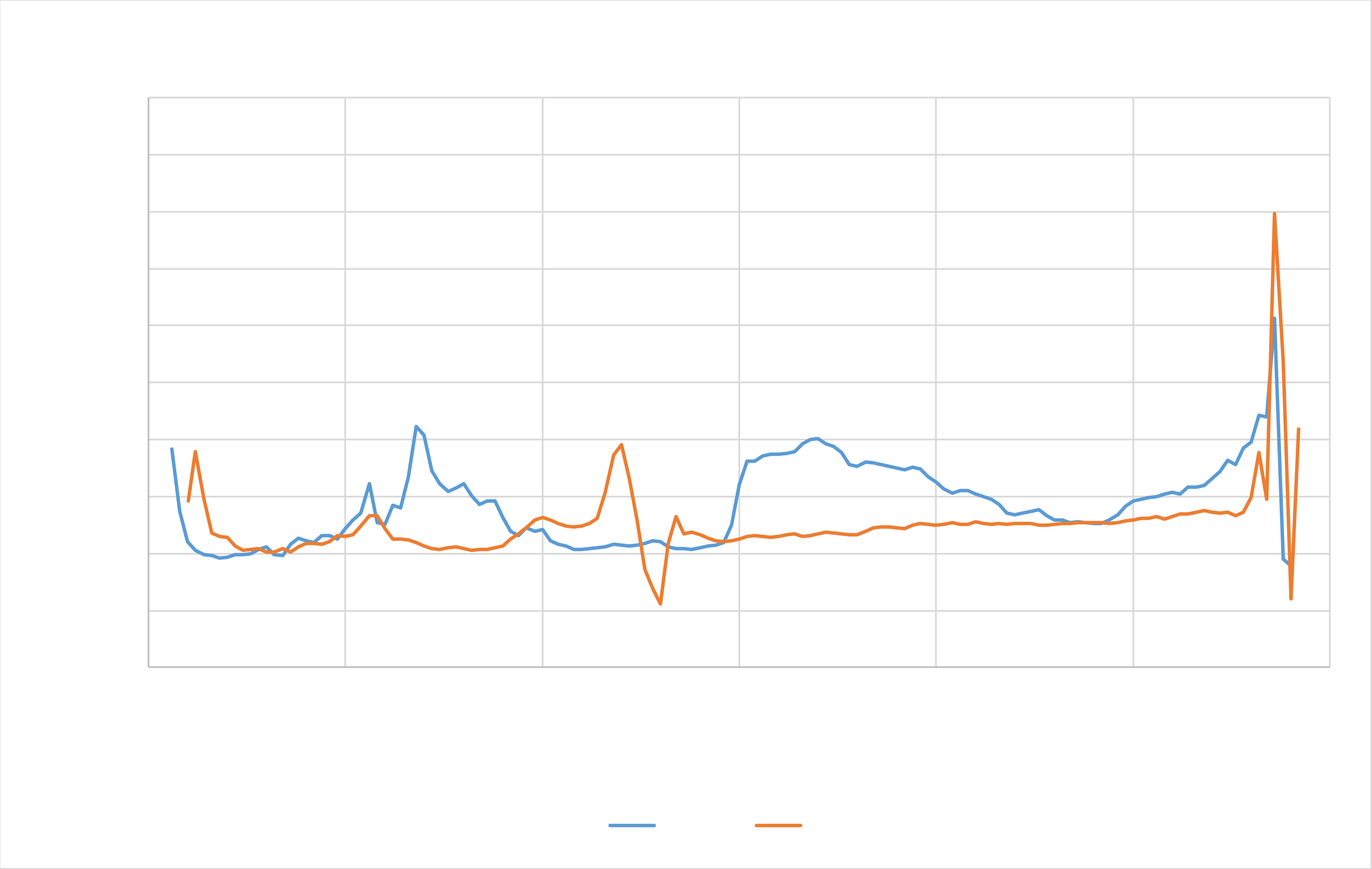
LT @350um

LT @15um

LT @<5um

Credit: DISCO

TTV of thinned LT ~2X carrier TTV



Credit: DISCO

Successful mechanical debonding at EVG

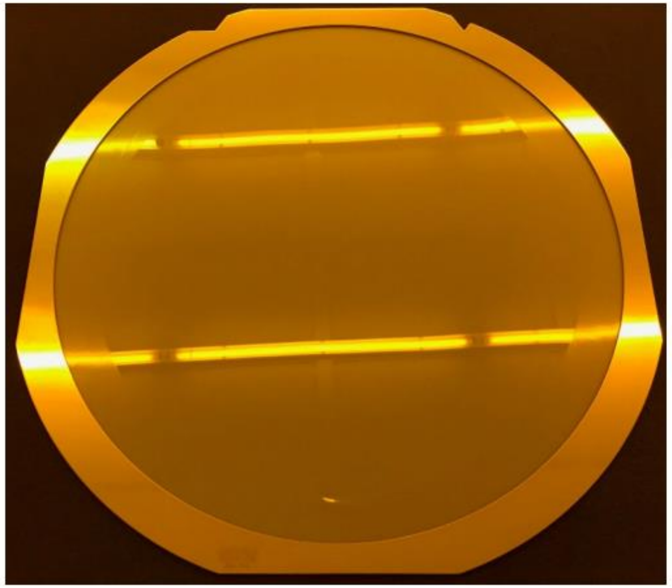
Substrate 1 Thickness	Substrate 2 Thickness
100 µm	700 µm

No separation could be succeeded without a blade initiation ✗
→ Vacuum loss

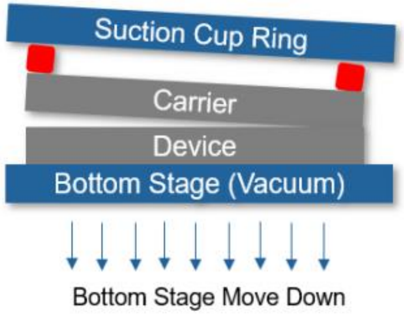
A proper initiation could be achieved with a stainless steel and a low abrasion plastic initator ✓

The wafer stack could be successfully separated (carrier peel off) after initiation ✓
→ Pull force (~10N)

300 mm thin wafer on FilmFrame
Post debond inspection



Method A



Credit: EVG

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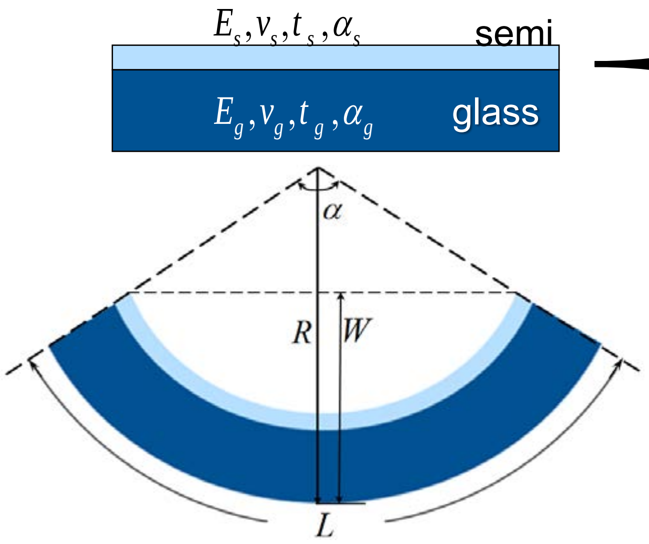
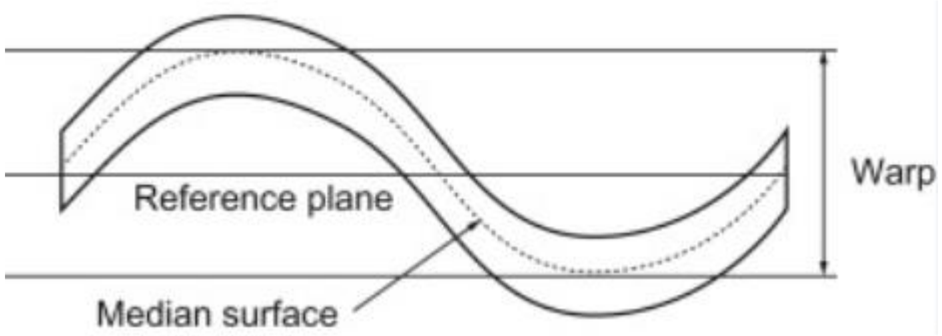
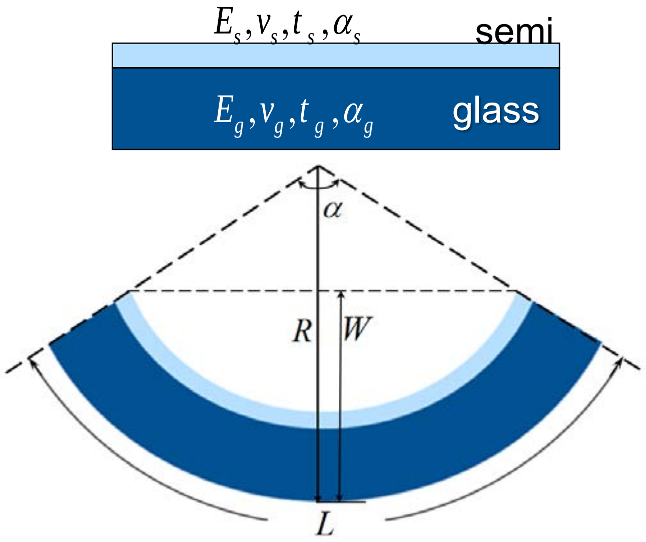
Definition of a buildup structure and warp



- Buildup structure on glass
  - Laminate of metal and dielectric
  - Epoxy molding compound w/ Si
  - Adhesive layer
  - Any combination of the above



CTE mismatch causes in-process warp



Under typical buildup conditions, in-process warp follows a simplified formula showing its dependence on:

1. CTE mismatch between glass & the composite semi material
2. Inverse of glass Young's modulus
3. Inverse of square of glass thickness

(2 and 3:) *Both deliver "Stiffness"*

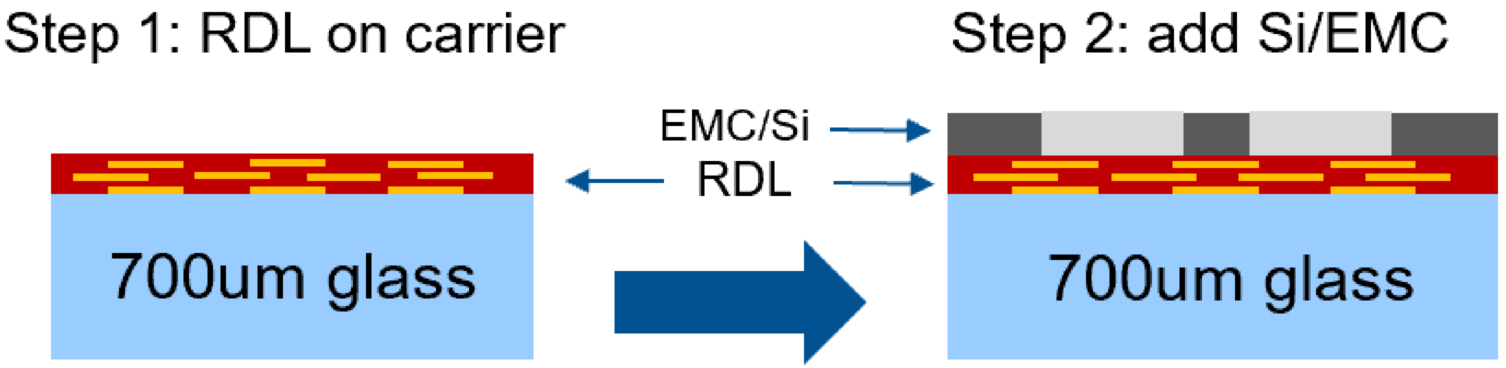
$$\approx 0.75 L^2 \Delta\alpha \Delta T \, \frac{E_s(1-v_g)}{\mathbf{E_g}(1-v_s)} \, \frac{t_s}{\mathbf{t_g}^2}$$

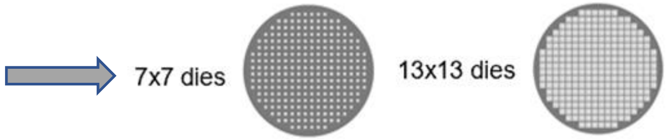
E : Young's modulus; ν : Poisson's ratio; t: Glass thickness;

α : Coefficient of thermal expansion; T : Temperature.

g: glass; s: semiconductor layers (MC + redistribution layers + die)

Simulation case 1: RDL-first fanout in two FO ratio scenarios





	Glass	Dielectric	Copper	EMC	Si
Young's modulus (GPa)	80.0	0.9	117.0	18.5	Anisotropic
CTE (ppm/K)	4.0/8.0/12.6	80.0	17.0	9.0	2.6
Poisson's ratio	0.22	0.30	0.34	0.30	Anisotropic
Density (g/cc)	2.4	1.0	9.0	1.0	2.3

Scenario 1:
- 15mm x 15mm package size
- 7mm x7mm die size

Scenario 2:
- 15mm x 15mm package size
- 13mm x 13mm die size

Reference: Z. Chen et al, "Package Level Warpage Simulation of Fan-out Wafer Level Package (FOWLP) Considering Viscoelastic Material Properties", EPTC, 2018

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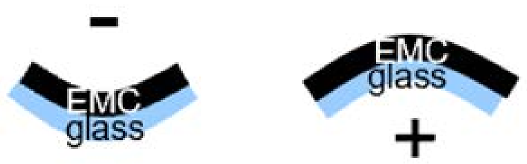
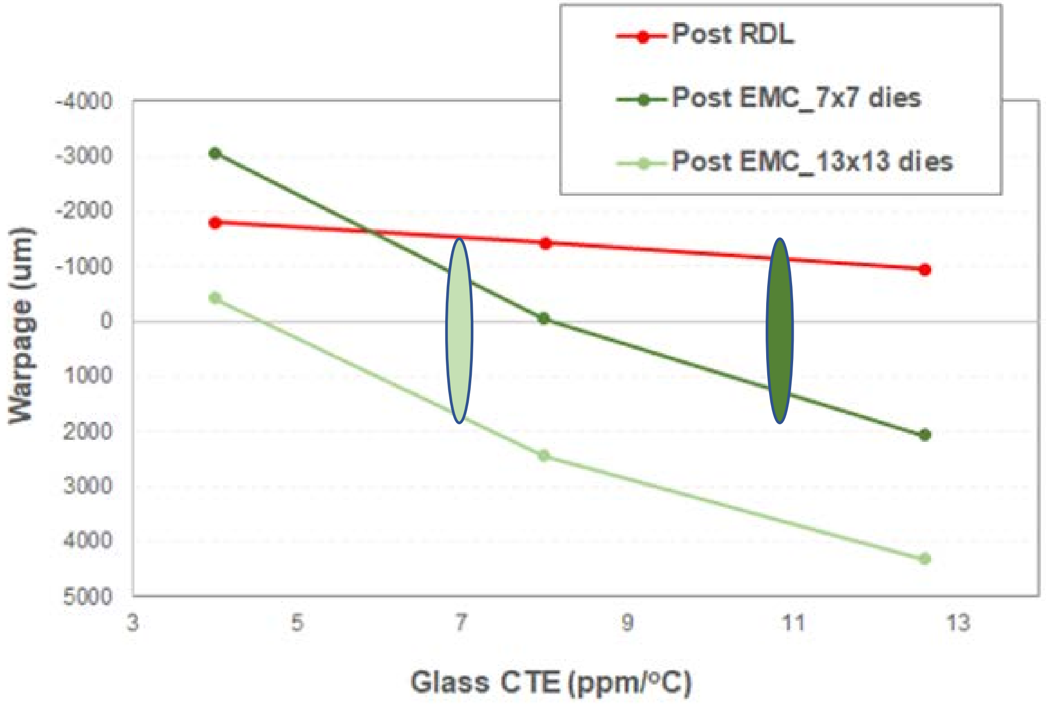
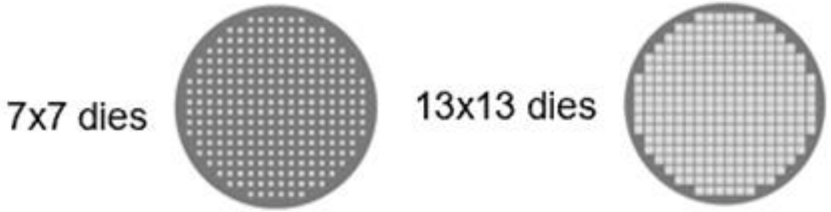
Simulation case 1: RDL-first fanout in two FO ratio scenarios

Warpage sign convention



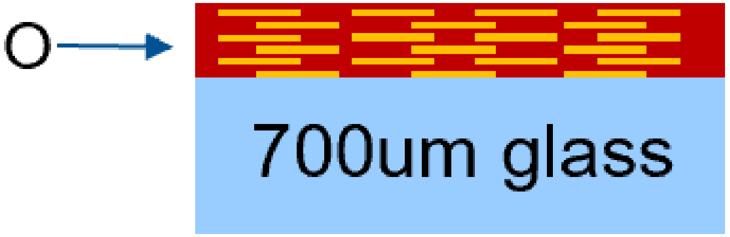




- Post RDL shows smiley face bow due to higher Cu and PI CTE than carrier
- Adding Si and EMC flips bow direction due to lower CTE of Si and EMC
- Single carrier CTE choice should keep maximum bow within equipment tolerance: ~11 ppm/C for high FO ratio and ~7 ppm/C for low FO ratio

Simulation case 2: multilayer organic (MLO)

MLO built on carrier

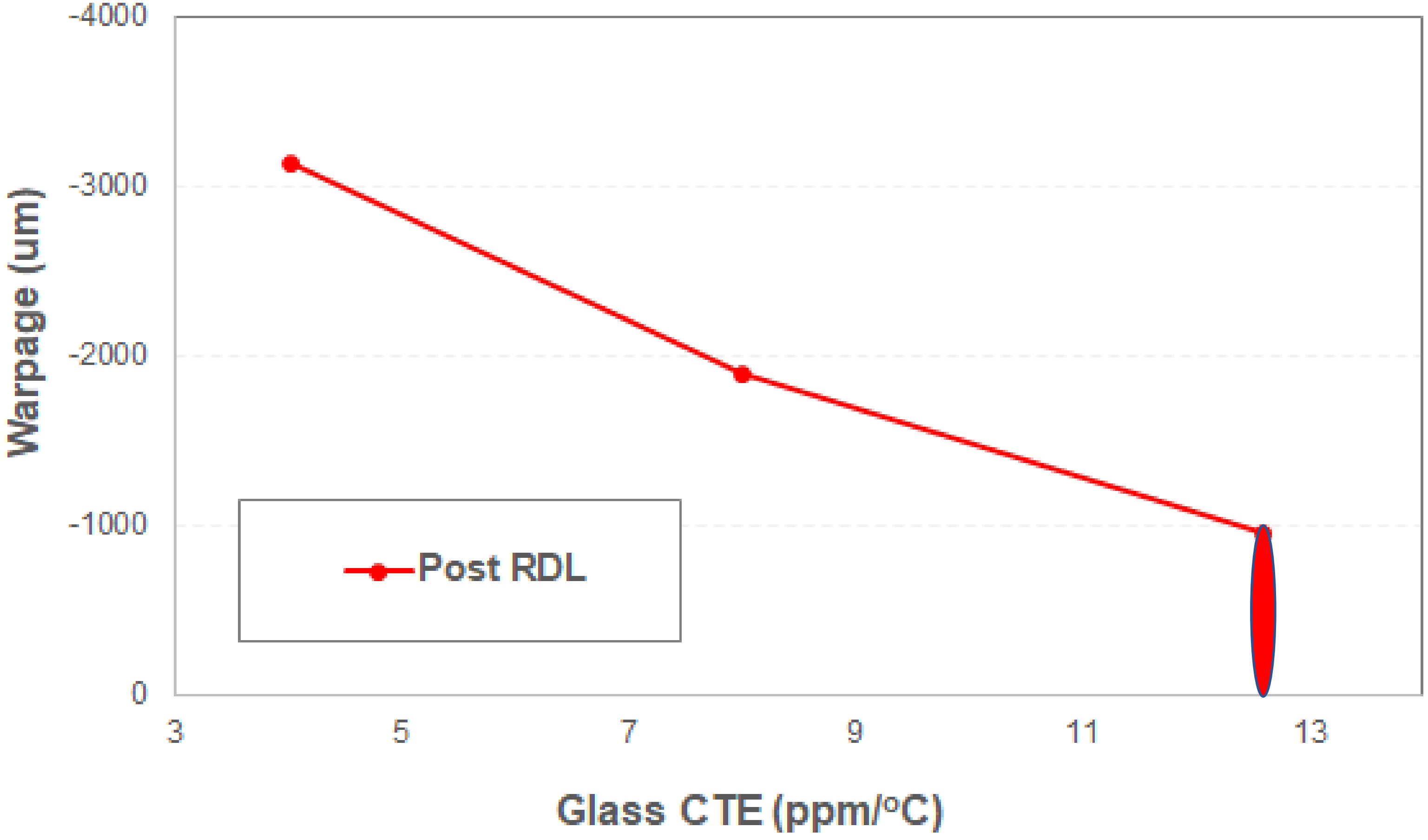

6-layer Cu/PI MLO

700um glass

	Glass	Dielectric	Copper
Young's modulus (GPa)	80.0	8.5	117
CTE (ppm/K)	4.0/8.0/12.6	3.0	17.0
Poisson's ratio	0.22	0.30	0.34
Density (g/cc)	2.4	1.4	9.0

Source: HD MicroSystems PI-2600 product bulletin

Simulation case 2: multilayer organic (MLO)



- Bow is smiley face because Cu has high CTE and high Young’s modulus
- Low CTE PI plays a minor role due to low Young’s modulus
- CTE @12.6 ppm/C brings bow < 1mm

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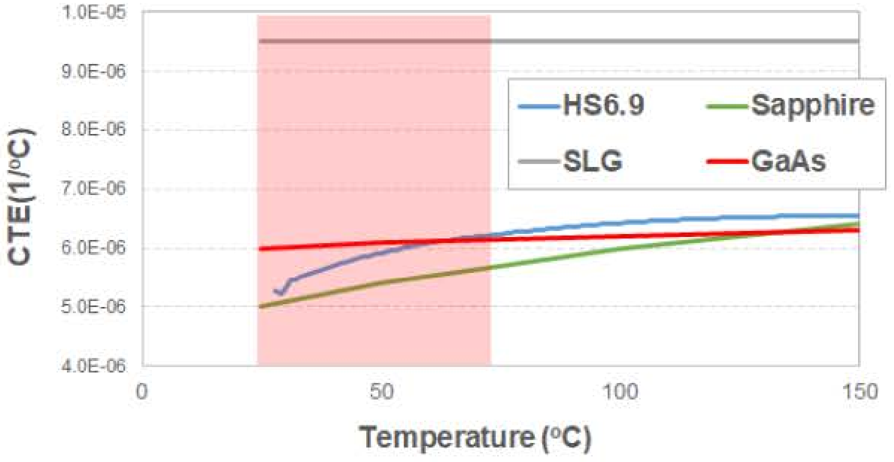
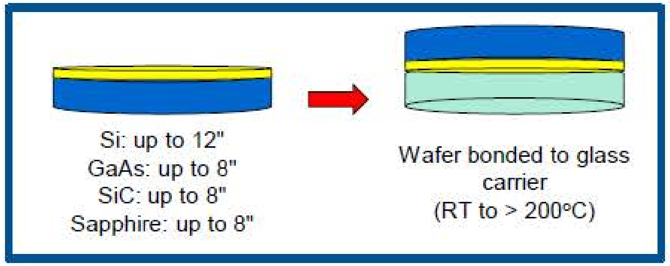
Wafer Warp During Bonding Process

ΔCTE of glass substrate, device wafer and adhesive: modeling & experimental data

Minimizing *Δ* CTE between carrier substrate and wafer at processing temperature is important

Glass CTE is not a constant value.
It changes as a function of temperature.

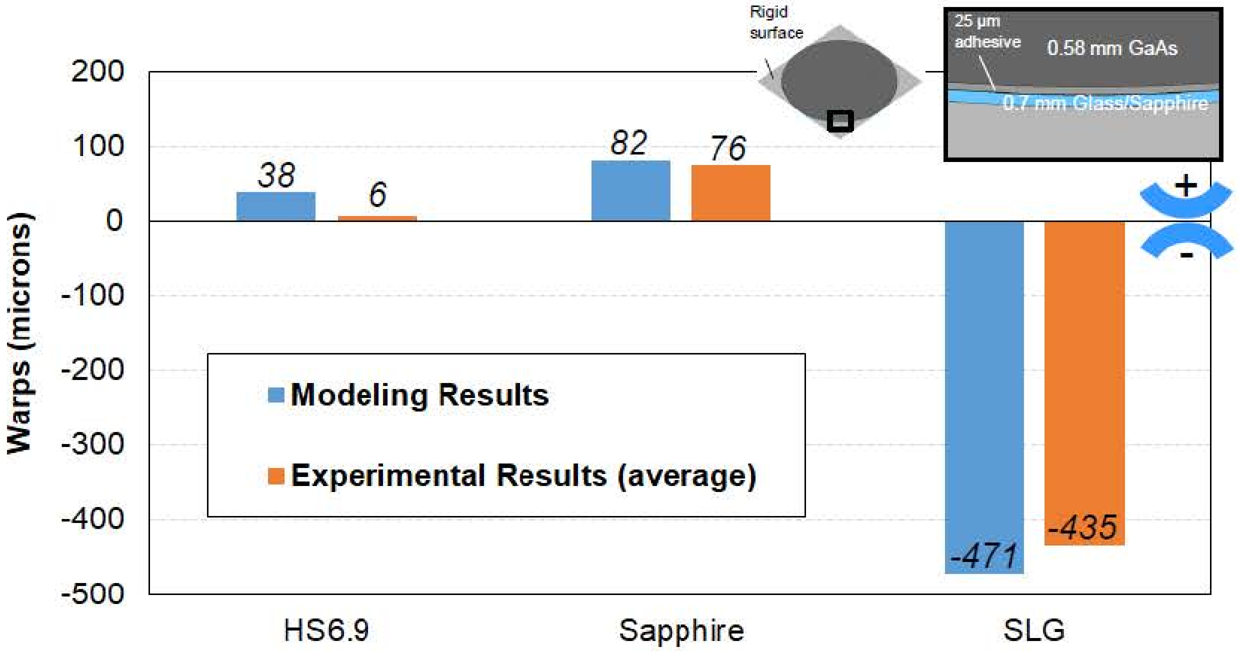



Si: up to 12"
GaAs: up to 8"
SiC: up to 8"
Sapphire: up to 8"

Wafer bonded to glass carrier
(RT to > 200°C)

In-process warp of bonded GaAs wafers: Modeling and experimental data

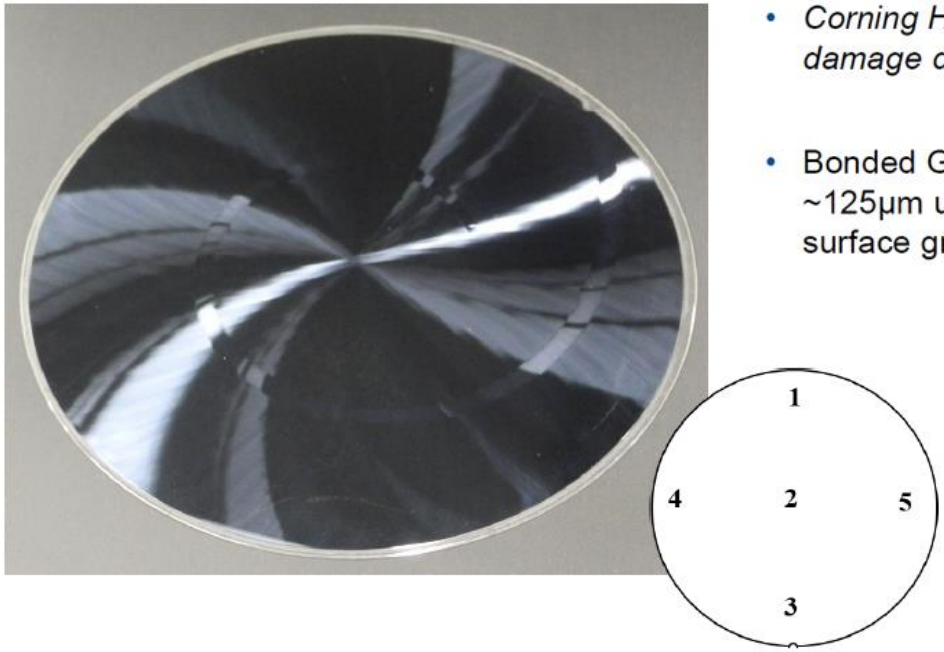
Modelling assumption:
- high temperature GaAs wafer bonding with different substrate
- Substrate thickness 0.7mm and adhesive thickness 25um
- Intial GaAs wafer thickness 580µm
- Wafer diameter 150mm (6")
- Stress-free temp: 70°C (adhesive Tg)



Bonded Wafer after Back Grinding

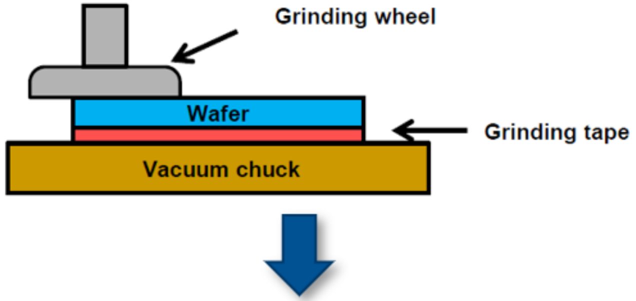
HS6.9 successfully supports wafer thinning: experimental result

Bonded GaAs on HS6.9 after back grinding

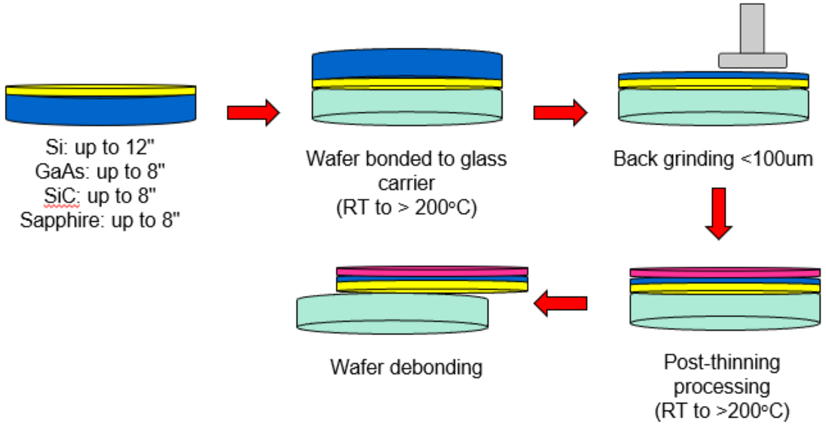


- *Corning HS6.9 showed no process damage during thinning process*
- Bonded GaAs wafer was ground to ~125µm using Disco DAG810 automatic surface grinder

Carrier		Org.	Final Thickness (um) (Measurement points)						
Material	Thickness (um)	thickness	1	2	3	4	5	Ave	TTV
HS6.9	700	1383	824.8	825.3	824.9	824.7	825.0	824.9	0.6



Typical Wafer Thinning and Processing Flow



Si: up to 12"
GaAs: up to 8"
SiC: up to 8"
Sapphire: up to 8"

Wafer bonded to glass carrier
(RT to > 200°C)

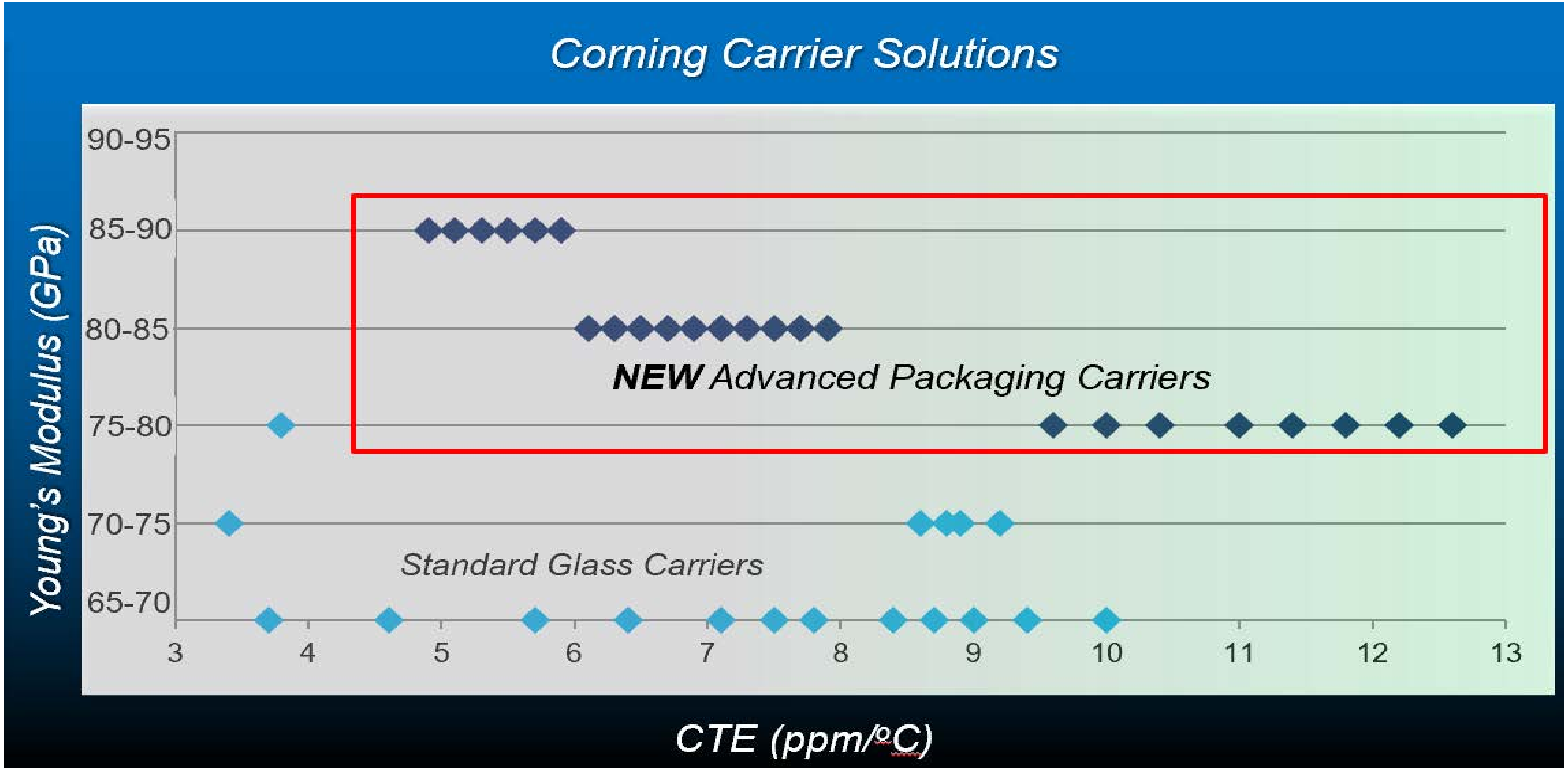
Back grinding <100um

Post-thinning processing
(RT to >200°C)

Wafer debonding

Custom CTE carrier for ANY device wafer thinning: GaAs, SiC...

Corning glass covers broad CTE range and fine granularity



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Conclusions

- Glass is a highly versatile class of material. Glass properties can be widely tuned to meet a diverse range of applications
- Corning's ultra-low-TTV carrier and "near-zero-TTV" temporary bonding solutions (ALoT) deliver <<1um stack TTV, enabling extreme wafer thinning
- Glass carrier wafers can effectively help control warp in many buildup processes as well as substrate thinning through CTE engineering, Young's modulus enhancement, and thickness customization
- Corning's advanced packaging carrier (APC) product line now covers wide range of CTE with fine granularity, high Young's modulus and thickness flexibility to deliver on this promise
- Corning welcomes applications inquiries and joint development opportunities with customers

Acknowledgments

- Corning Incorporated: Jay Zhang, Andy Teng, Christina Yu, Erica Chang, Chris Kuo, Andy Kuo, Julie Tseng, Gwako Liang, Prantik Mazumder, Bo-kyung Kong, Robert Manley, Han-hee Jo, and Kuniaki Yamazaki
- DISCO Corporation in Japan for wafer thinning as well as insightful discussions with Dr. Frank Wei of DISCO Hi-Tec America
- EVG in Austria for mechanical debonding

Thank you for listening and please reach out with questions:
BrueckneJ@Corning.com