Acronyms

- **ASIC** – American Semiconductor Innovation Coalition
- **COE** – Coalition of Excellence
- **IDM** – Integrated Device Manufacturer
- **NAPMP** –National Advanced Packaging Manufacturing Program
- **NSTC** – National Semiconductor Technology Center
- **OSAT** – Outsourced Semiconductor Assembly and Test
- **UFC** – University Focus Center

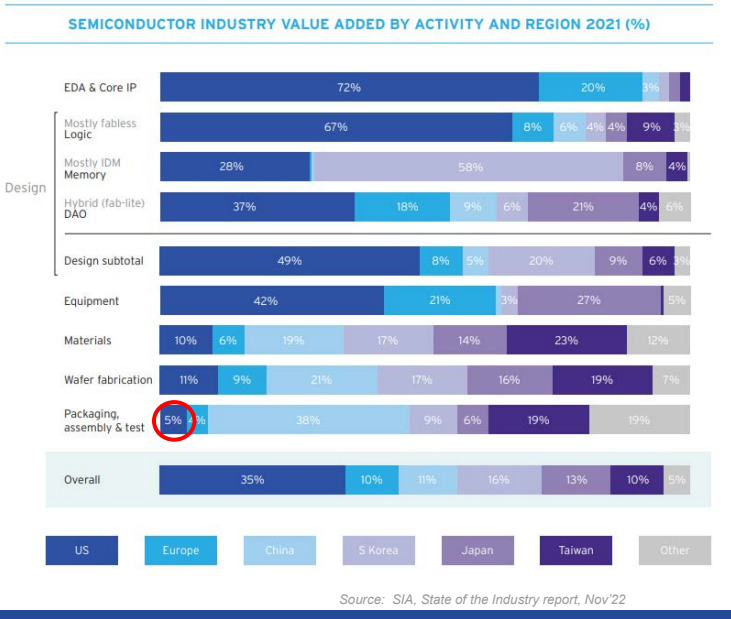
Contents

- **Problem Statement** – very limited US self-sufficiency in Semiconductor Packaging
- **Solution: CHIPS Act** – $52B over 5 years for Semiconductor and Packaging R&D
- **ASIC** – American Semiconductor Innovation Coalition
- **NAPMP** – Proposed ASIC Framework for the National Advanced Packaging Manufacturing Program

The US Houses only ~5% of the Packaging Industry (by Value Added)

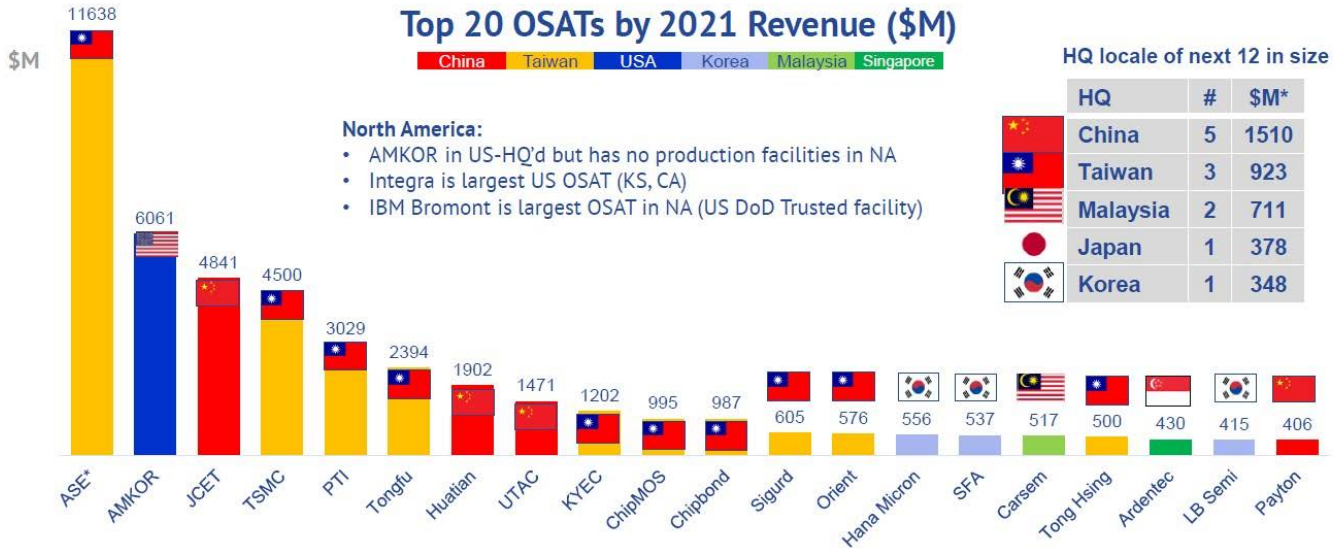
Negative Implication:
- Surety of Supply

Packaging Assembly & Test is the weakest link in the Supply Chain for the United States.



Source: SIA, State of the Industry report, Nov'22

China & Taiwan Dominate the OSAT Landscape



North America:

- AMKOR in US-HQ'd but has no production facilities in NA
- Integra is largest US OSAT (KS, CA)
- IBM Bromont is largest OSAT in NA (US DoD Trusted facility)

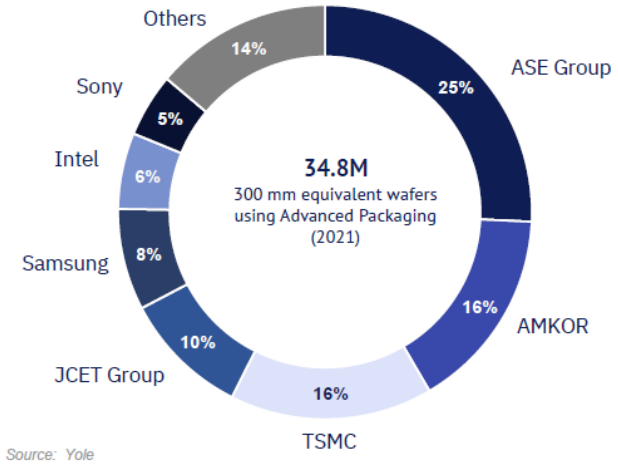
HQ locale of next 12 in size

HQ	#	$M*
China	5	1510
Taiwan	3	923
Malaysia	2	711
Japan	1	378
Korea	1	348

Source: Yole

6 Companies Package 80% of wafers using Advanced Packaging

Top Providers of Advanced Packaging*



Source: Yole

Company	HQ	Advanced Packaging Main Factory Location(s)
ASE Group		
AMKOR		
TSMC		
JCET Group		
Samsung		
Intel		Vietnam, Malaysia

Advanced Packaging includes: all flip chip, all wafer level packaging technologies, and all 2.x and 3D technologies.

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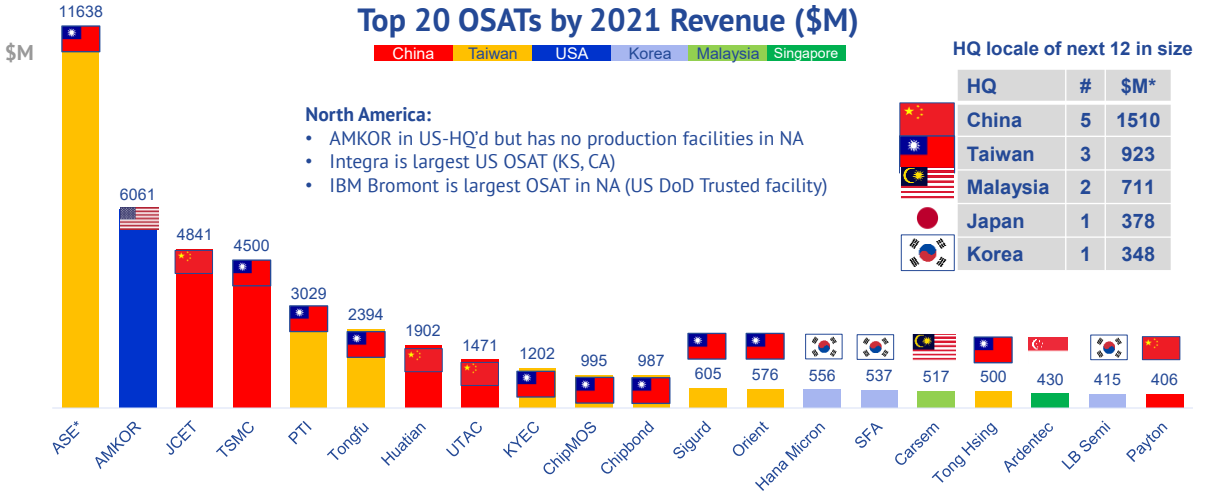

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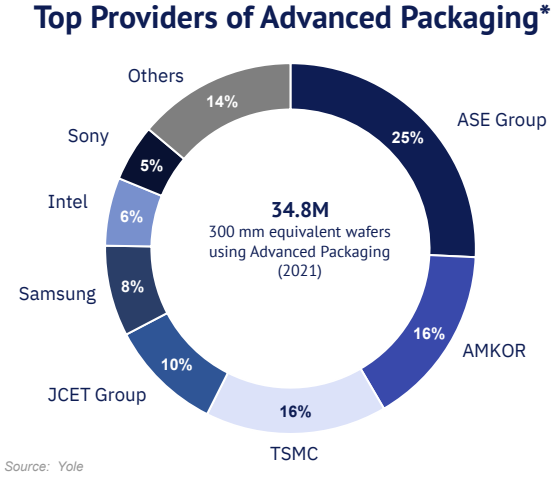

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>50% of the World's Packaging Facilities are in China + Taiwan

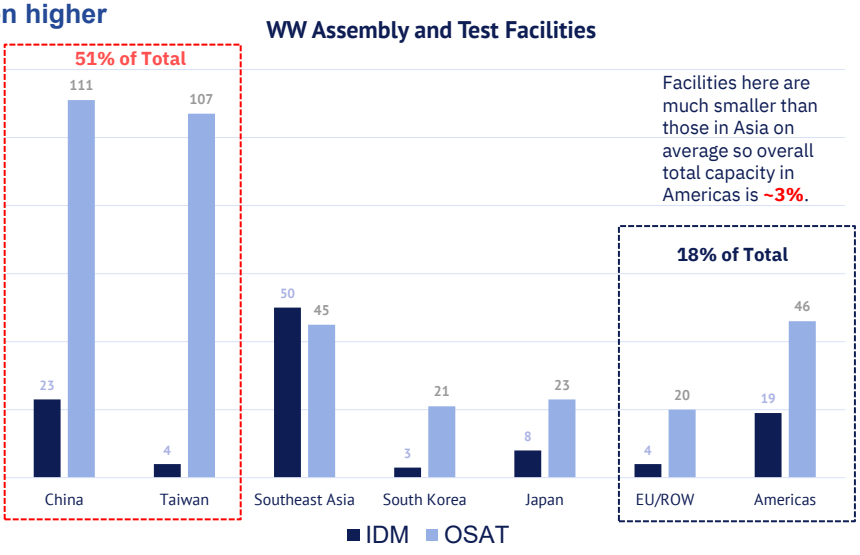
Implied Capacity is even higher

Global Packaging Facilities:

- 373 OSAT (77%)
- 111 IDM (23%)

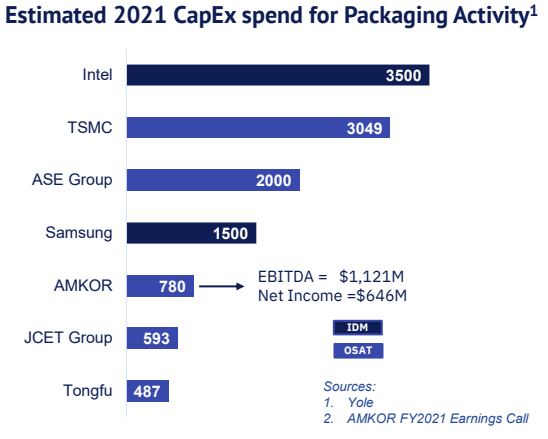
The majority are focused on legacy packaging technology (e.g. >100 facilities offering QFN)

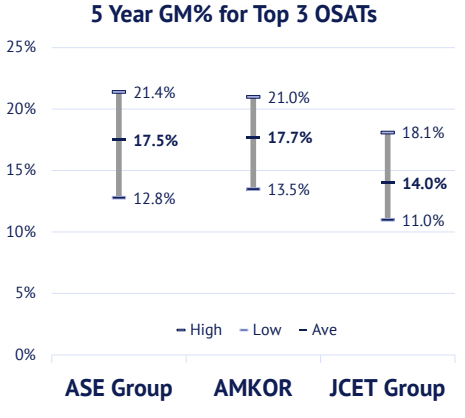
Source: SEMI, OSAT Database



Facilities here are much smaller than those in Asia on average so overall total capacity in Americas is **~3%**.

OSAT Manufacturing in US has two Major Barriers to Entry





. . . and this with all major manufacturing operations being in Asia.

Financial sustainability is a problem even if you have the initial CAPEX to launch.

CHIPS Act Funding Status

NIST

Proposed $52B in appropriations

Several cross-NIST, DOC, Interagency and White House Teams are developing plans for implementation when funds are appropriated for the implementation of the CHIPS Act R&D Programs

Section	CHIPS Act	Proposed appropriations FY 2022 $ B	2023 $ B	2024 $ B	2025 $ B	2026 $ B
9902	**Semiconductor incentives**					
9902	Incentives Program	**19**	**5**	**5**	**5**	**5**
9906	**Advanced microelectronics R & D**					
9906 **c**	National Semiconductor Technology Center	**2**	**2**	**1.3**	**1.1**	**1.6**
9906 **d**	Nat. Advanced Packaging Manufacturing Prog.	**2.5**				
9906 **e**	Microelectronics Research at NIST	**0.5**				
9906 **f**	Manufacturing USA Institute					

ASIC

Source: Robert Rudnitsky, NIST

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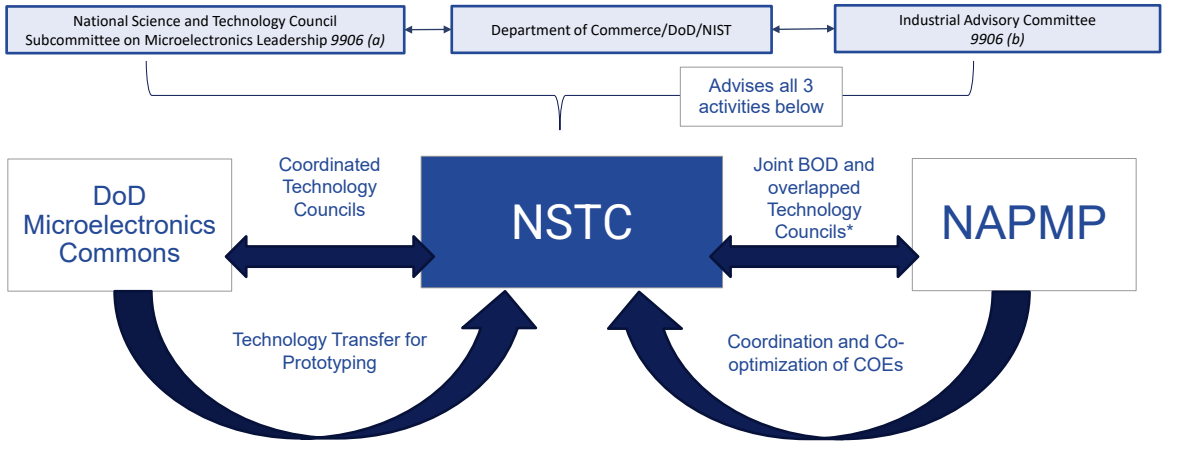
ASIC Notional Structure of Authorized Programs in CHIPS Act



+ up to 3 Manufacturing USA Institutes and NIST Metrology

*If legal or possible

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American Semiconductor Innovation Coalition (ASIC)

Who we are:

The American Semiconductor Innovation Coalition (ASIC) represents more than 175 businesses, startups, universities, national labs, and nonprofits dedicated to bringing the best research and development to The National Semiconductor Technology Center (NSTC) and The National Advanced Packaging Manufacturing Program (NAPMP).

Our approach:

Broad Representation

Robust governance model with diverse representation from industry, government, academia, national labs and small businesses to define and implement an ambitious technical agenda and roadmap

Coalitions of Excellence

Network of core research centers across the U.S. with key infrastructure to execute research agenda, facilitating technology development, maturation and translation from 'lab to fab'

Investment Fund and Start-up Support

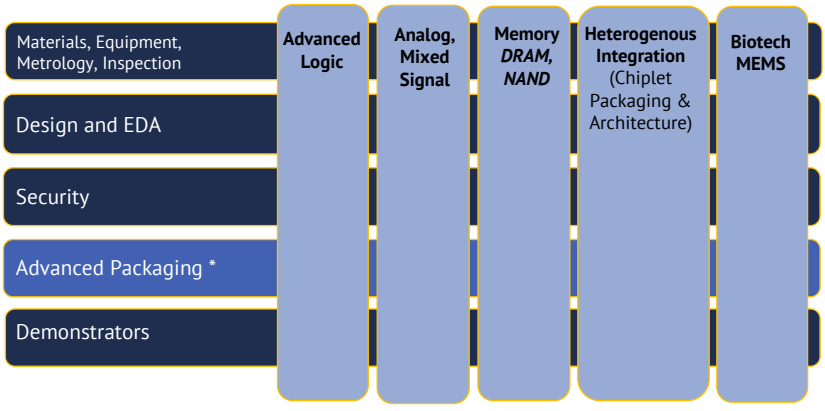
Funding opportunities for new ventures, in addition to support for early-stage start-ups; leveraging resources across Coalitions of Excellence to provide start-ups with access to expertise, facilities and equipment

Education & Workforce Development

A nation-wide program to develop and rapidly adopt educational content, investing in and supporting equitable education and training programs and facilities accessible to a broad range of institutions

ASIC Technical Team

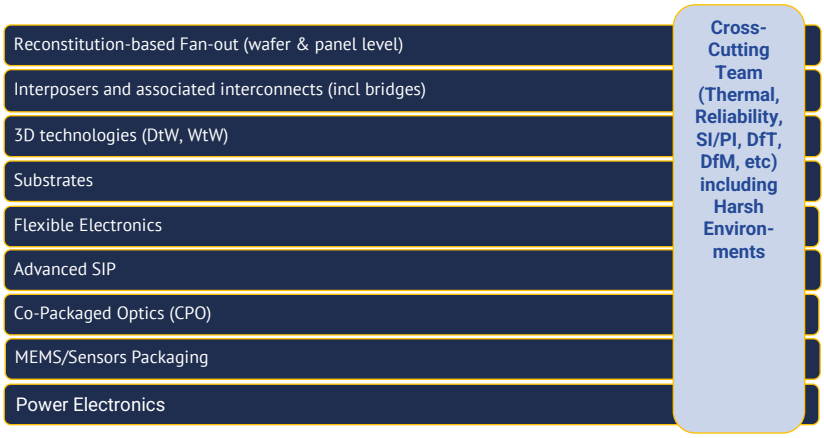
300+ participants across 10 Work Groups



* Denotes NSTC, NAPMP scope

Advanced Packaging Workstream Sub-Team Organization

9 horizontal teams and 1 cross-cutting vertical team



ASIC Advanced Packaging Team

Who are we? 138 members from across 79 entities

19 Universities
37 members

BU
Cornell
GaTech
MIT
Penn State
Princeton
Purdue
RPI
SUNY
U Binghamton
U Delaware
U Illinois
U Michigan
U Minnesota
U Puerto Rico
U Vermont
UCLA
UIUC
USC(ISI)

48 Companies
87 members

3D Glass
ADI
Advantest
AMAT
AMD
Analog Photonics
ASPDL
AT&S
Atomica
Canon Nano
DECA
Dupont
FormFactor
GE Research
Global Foundries
Green Source
Hyperion
i3 Micro
IBM
Integra
Jabil
Resonac
JSR Micro
Keysight
KLA
LAM
Marvell
Mercury
Mosaic
NANTERO
nepes
NGC
Nhanced
WDC
Novami
NXP
Siemens
Skywater
Sunray
TEL
Teledyne
TI
TTM
UI Corp
ULVAC
Veeco
WDC

3 Industry Assoc
3 members

iNEMI
IPC
SEMI

2 MIIs
4 members

AIM Photonics
NextFlex

3 Analysts
3 members

TechCet
TechSearch
Yole Dev

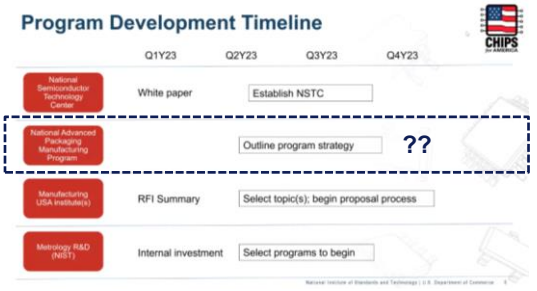
3 National Labs
3 members

ANL
CEA-LETI
Fraunhofer

NYCreates

NAPMP Direction

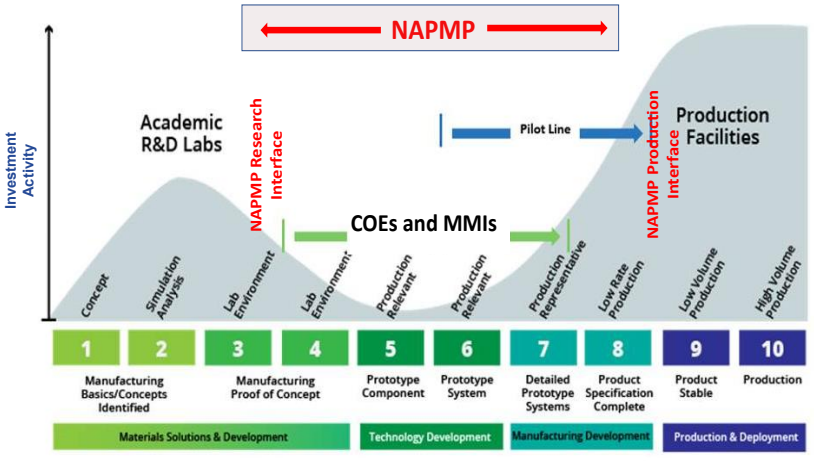
- **NIST/DOC direction for the NAPMP has been sparse despite $2.5B allocated in first year**



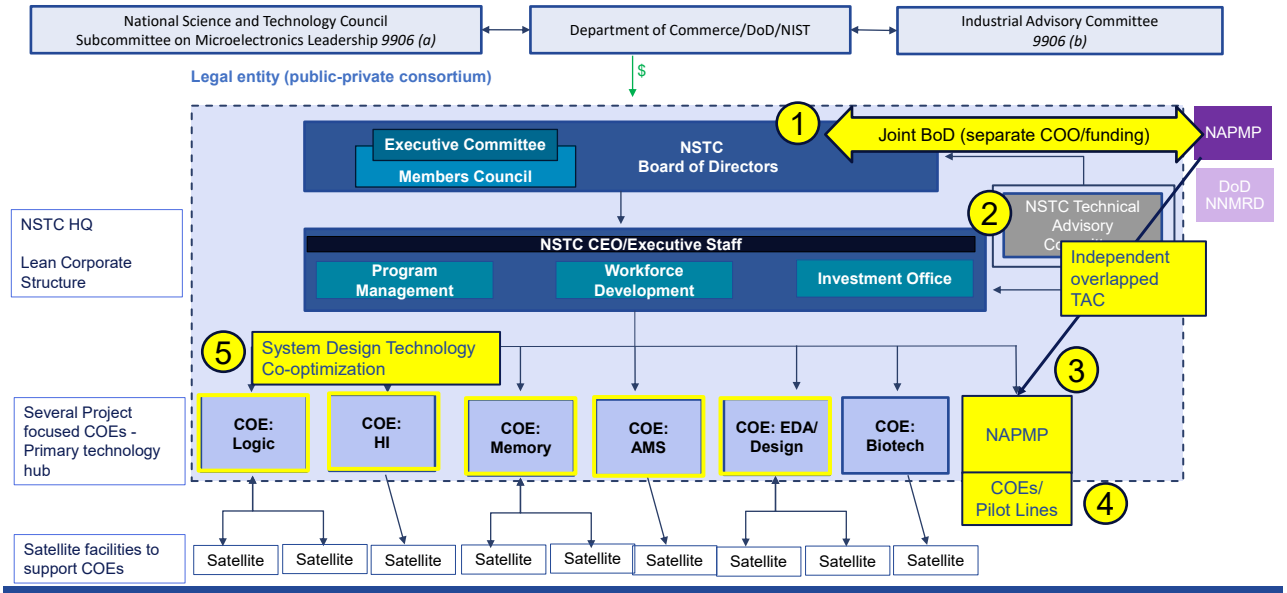
- **Nevertheless, the ASIC Advanced Packaging Teams have been active in planning**

ASIC NAPMP Objectives

- Encourage and support advanced research to create totally new technologies, designs and products.
- Accelerate technology development
- Transfer new technology to US commercial production
- Support workforce development
- Maintain close links with the NSTC



NSTC proposed structure – NAPMP Connection



NSTC/NAPMP Relationship

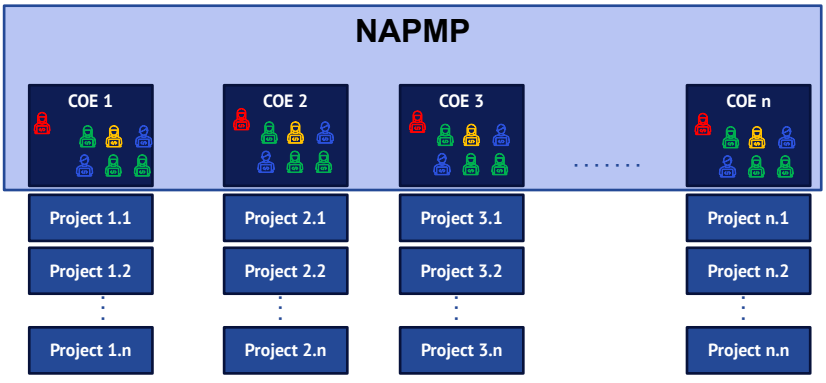
- To avoid duplicate overhead costs and to ensure strategic alignment, we recommend that the NSTC and the NAPMP share:
  - Board of Directors
  - CEO
  - Workforce Development
  - Support Staff where possible
- To ensure appropriate governance and funding, we recommend that the NSTC and NAPMP have separate:
  - COEs
  - COO
  - Budget / Financial Management
  - Program Management
  - Technical Advisory Committees

Proposed NAPMP COE Structure

As a "Manufacturing Program", we assume the NAPMP COEs will be program focused and will not typically have their own facilities

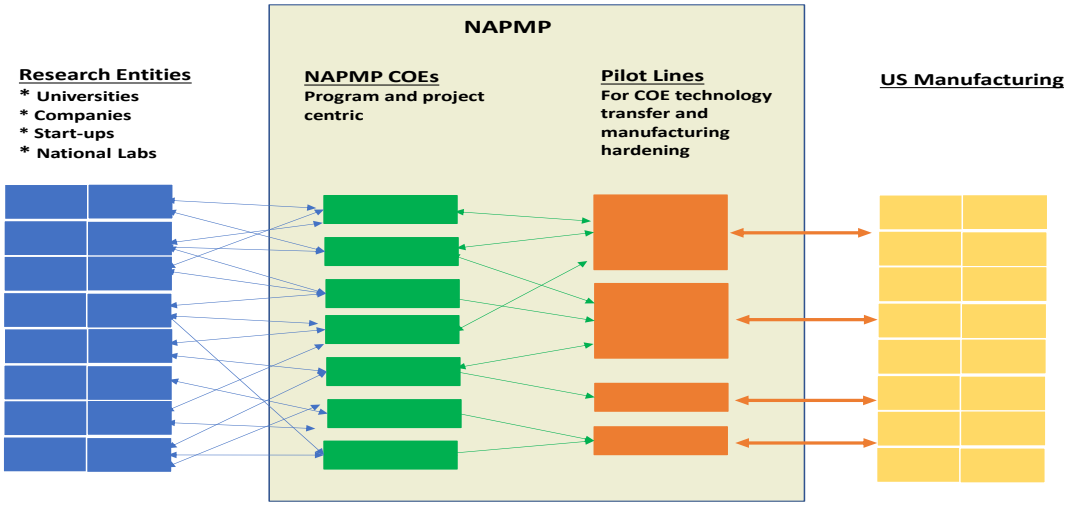
Major tasks would be;

- Research interface
- Road mapping
- Program selection, funding, objectives, monitoring to accelerate technology development
- Transfer of technology to pilot lines



- Each COE has a specific technology theme
- COE should have industry/university inputs, along with NIST inputs, into decision making

Conceptual Schematic of the NAPMP



Major Markets Enabled By Advanced Packaging

- High performance computing (including AI) with reduced energy consumption (3DHI, Co-Packaged Optics)
- Memory centric computing (3DHI)
- Defense, 6G, autonomous driving (>60GHz packaging)
- EVs, renewable energy (high voltage/power packaging)
- Data communications, AR headsets, autonomous driving LIDAR (3DHI, Co-Packed Optics)
- Wearable medical devices (MEMS, low power, size, flexible electronics)
- Aerospace and Defense (all of the above)

NAPMP Coalitions of Excellence (COEs)

The COEs would focus on accelerating technology development in the NAPMP, each with a particular technology theme. Ten proposed:

- 3D heterogeneous integration
- Copackaged optics (CPO)
- Advanced SIP
- High voltage/high power
- FO-WLP (reconstituted)
- Interposers/Bridges
- Substrates
- MEMS
- Flexible Hybrid & Additive
- Cross cutting (eg thermal, reliability, DFM, etc)

Each COE would have sub-COEs to drive subsets of the technology.

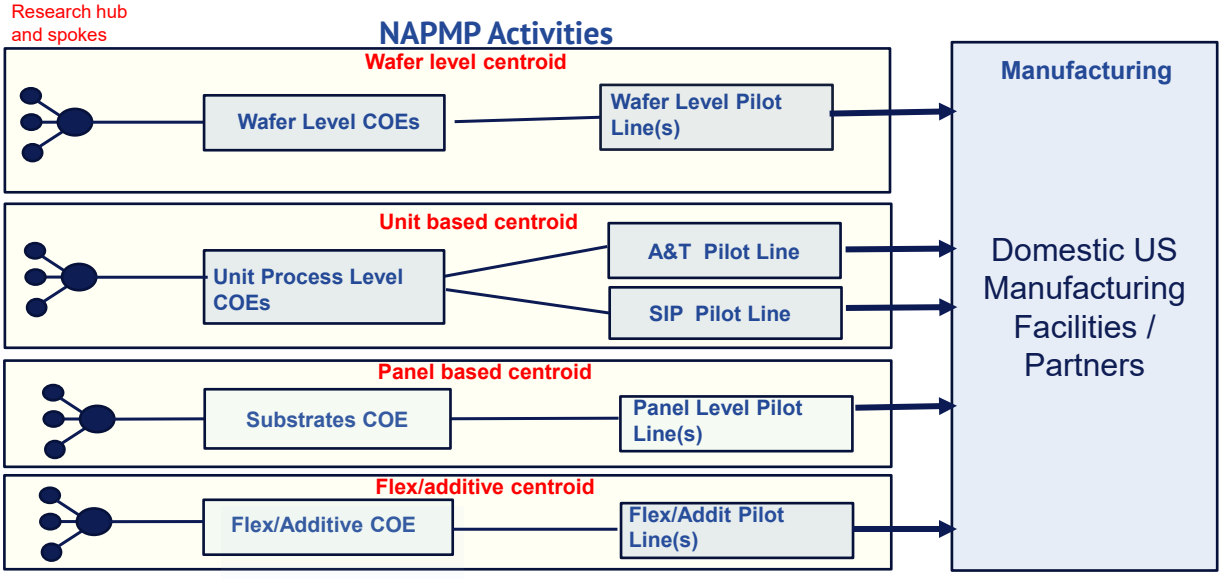
Example: 3D HI

- Co-design EDA for design and test
- Hybrid bonding *[example Projects]*
  - *Bonding down to 2um bond pitch plus improved wafer finishing*
  - *Alignment to 100nm*
  - *Higher throughput tools with die speed binning capability*
  - *New materials to reduce anneal temperature*
  - *Data management for increased yield and traceability*
- Thermal dissipation
- Below surface metrology
- Reliability

Research – University Focus Centers

- Research and innovation is a great strength for the United States. Large research universities are very hard to replicate, and we need to leverage this advantage we have.
- Each NAPMP COE should be linked to a lead university with expertise in its technology and other universities in a hub and spoke structure.
- The NAPMP should support both capital and operating cost for funded projects.
- The COE and the universities should collaborate on road mapping and areas for research, with some funding for theme-based undirected research

Proposed COE/Pilot Line Approach



NSTC/NAPMP EWD – Key Components & Program Strategy

Developed by 80+ Person EWD Team from 65 ASIC Universities, Comm. Colleges, Companies & Industry Orgs

EWD = Education & Workforce Development

- NSTC/NAPMP National Microelectronics Outreach and Awareness Initiative
- NSTC/NAPMP National Diversity, Equity, Inclusion, Belonging and Underserved Communities Thrust
- NSTC/NAPMP National Experiential Learning Network Universities, Colleges, Community Colleges, Apprentice Programs, Veterans Training, SkillBridge
- NSTC/NAPMP National and Regional EWD Needs Roadmap & Impacts

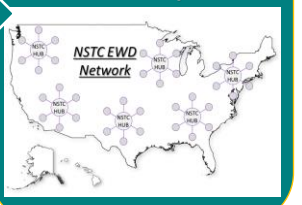
NSTC/NAPMP Incentives Crosscut: (Nat'l Fellowship & Training Support)

- Nat'l University Network
- Nat'l Comm. Coll. Network
- Training Programs (Incumbent, Vets/Military, Construction Trades, Facilities support)

Coalition of Excellence (COE) & EWD Crosscut:

- Knowledge, Skills, Abilities (KSAs)
- Experiential Learning Program
- COE-centric initiatives, e.g. NSTC Design Education & Training Initiative

NSTC Regional EWD Cluster Network: On-the-ground programs, regional workforce support, content development and dissemination, interface with UFC campuses



UFC = University Focus Center

- ASIC's EWD Team is assembling an adaptive ***National EWD Platform*** to engage NSTC COE's, industry, academia and WFD organizations from across the U.S. to expand and elevate the national microelectronics workforce
- ASIC's National EWD Platform will enable ***broad national participation, scale and sustain successful EWD programs, promote DEIB, and engage underserved communities*** across the U.S. in semiconductor careers.

Proposed NAPMP Success Metrics

The NAPMP needs to monitor a broad set of success metrics, both leading and trailing, covering four areas:

- Operations
- Technical
- Economic
- Workforce Development

Area	ASIC Proposed NAPMP Metrics	
Operations	▪ # of NAPMP projects taken to production in USA ▪ # of members and dues paid ▪ # of projects delivered on schedule ▪ # of projects transfer to manufacturing	▪ Budget control ▪ # of research partnerships (academic and commercial) ▪ Progress towards industry self sufficiency for the NAPMP ▪ Assess performance of each NAPMP COE
Technical	▪ Roadmap acceleration versus prior expectations ▪ US technical leadership ▪ # of technologies/processes/products transferred to manufacturing ▪ Reduced environmental footprint for packaging technologies	▪ # of breakthrough challenges supported by NAPMP developed technologies ▪ # of projects terminated for technical reasons ▪ # of patents and license revenue ▪ # of peer reviewed papers and conference presentations
Economic	▪ US production market share in semi packaging (advanced and mature) ▪ # of new jobs created in US packaging facilities ▪ Growth of new industries supported by the NAPMP (eg EV, medical etc) ▪ Growth of US based packaging foundry	▪ # of start-up companies supported by NAPMP ▪ # of packaging related start-ups reaching successful exit ▪ National security support ▪ # of projects terminated for market reasons ▪ Improved supply chain resilience (less dependence on Taiwan)
Workforce	▪ # of students in training versus goals (AA, BS, MS, PhD) ▪ % minority and retrained students (eg military) ▪ # of students hired by semiconductor packaging industry ▪ # of semi packaging centric locations, courses and programs ▪ Geographic diversity of training	▪ % students graduating in 2 years (CC) and 4 years (BS) ▪ # students hired by semi-industry ▪ Number of CCs, colleges, and universities offering courses. ▪ # of student internships (at multiple levels: 2-year, 4-year, post-grad)

Summary

- The ASIC NAPMP team has developed an organization and structure for the NAPMP built around:
  - Ten Coalitions of Excellence for accelerated technology development
  - Five Pilot Lines for economic and sustainable manufacturing hardening
  - University Focus Centers leading the university research efforts
- The NAPMP objectives are:
  - Support research activities in advanced packaging
  - Accelerate technology development
  - Develop and harden economically and sustainable manufacturable processes
  - Transfer technology for manufacture to support multiple new market opportunities
- The NAPMP will collaborate with multiple organization including the NSTC, companies, universities and other government programs

To Learn more about ASIC

- **Website:** https://asicoalition.org/about
- **Twitter:** https://twitter.com/asicoalition
- **Linkedin:** https://www.linkedin.com/company/american-semiconductor-innovation-coalition/

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