SRC ® Semiconductor Research Corporation

MAPT: From Decadal Plan to actionable all-industry Roadmap

Victor Zhirnov
Chief Scientist
Victor.Zhirnov@src.org

Victor Zhirnov

Semiconductor Research Corporation

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Acronym Definitions

- CCG – Crosscut Group
- MAPT – Microelectronic and Advanced Packaging Technology
- MMI – Microelectronics Manufacturing USA Institute
- REXCOM – Roadmap Executive Committee
- TWG – Technical Working Group
- WFD – Workforce Development

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Outline

- Genesis of MAPT
  - Decadal Plan for Semiconductors
    - Five Seismic Shifts
- MAPT Roadmap mission and organization
- MAPT Roadmap in the context of related roadmaps & roadmapping activities

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3

Decadal Plan for Semiconductors
FULL REPORT

https://www.src.org/about/decadal-plan/

Ilyh#Vhlvp lf#Vkliw¶#Uhvhdufk#SulruWhv

- The Analog Data Deluge
- The Growth of Memory and Storage Demands
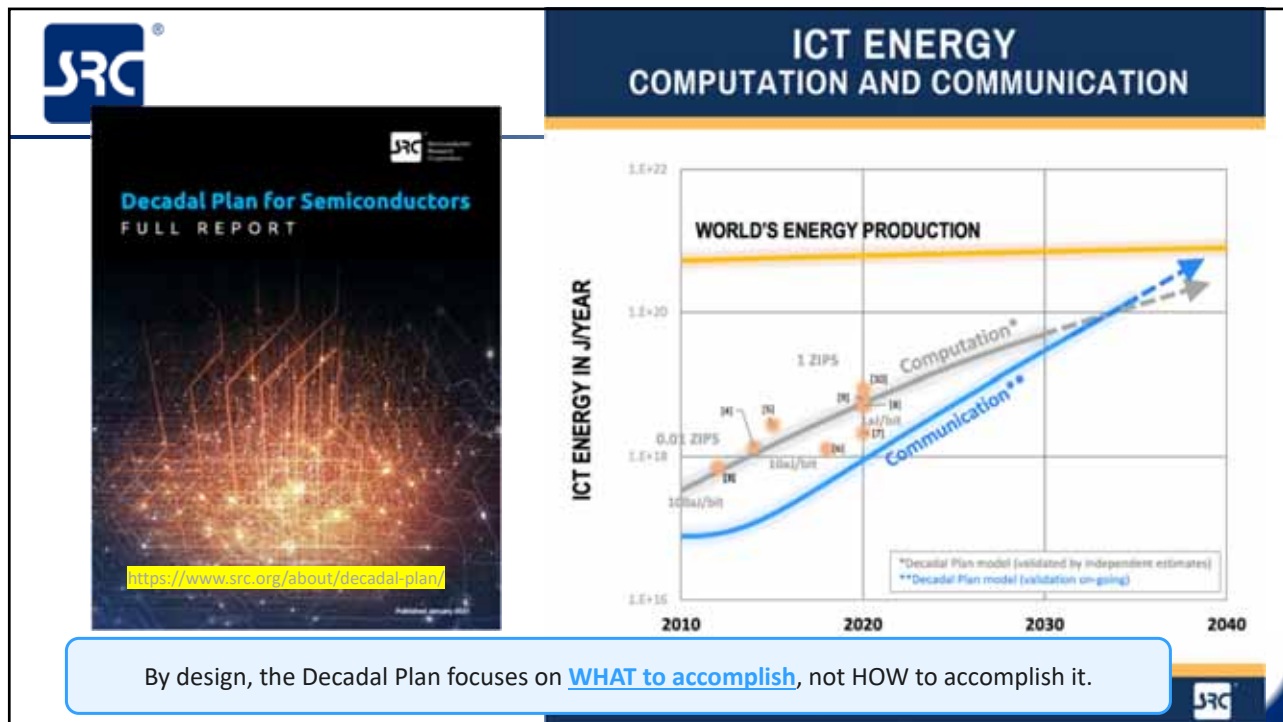- Communication Capacity vs. Data Generation
- ICT Security Challenges
- Compute Energy vs. Global Energy Production

Year 2022:Triumphal March of Decadal Plan

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By design, the Decadal Plan focuses on **WHAT to accomplish**, not HOW to accomplish it.

https://www.nextplatform.com/2022/01/04/the-five-horsemen-of-the-data-apocalypse/

THE FIVE HORSEMEN OF THE DATA APOCALYPSE

January 4, 2022   Nicole Hemsoth

Semiconductor Research Corporation (SRC) has issued a decade-spanning plan to identify and with partner DARPA, fund efforts those critical areas. Those five most pressing challenge areas SRC identifies (and which DARPA plans to back with its new **JUMP 2.0** funding effort) are the following:

The growth of memory demands will outstrip silicon supply presenting opportunities for radically new memory and storage solutions.

Always available communication requires new research directions that address the imbalance of communication capacity vs. data generation rates.

Fundamental breakthroughs in analog hardware are required to generate smarter world-machine interfaces that can sense, perceive, and reason.

Ever rising energy demands for computing vs. global energy production is creating new risk, and new computing paradigms offer opportunities with dramatically improved energy efficiency.

Breakthroughs in hardware research are needed to address emerging security challenges in highly interconnected systems and AI.
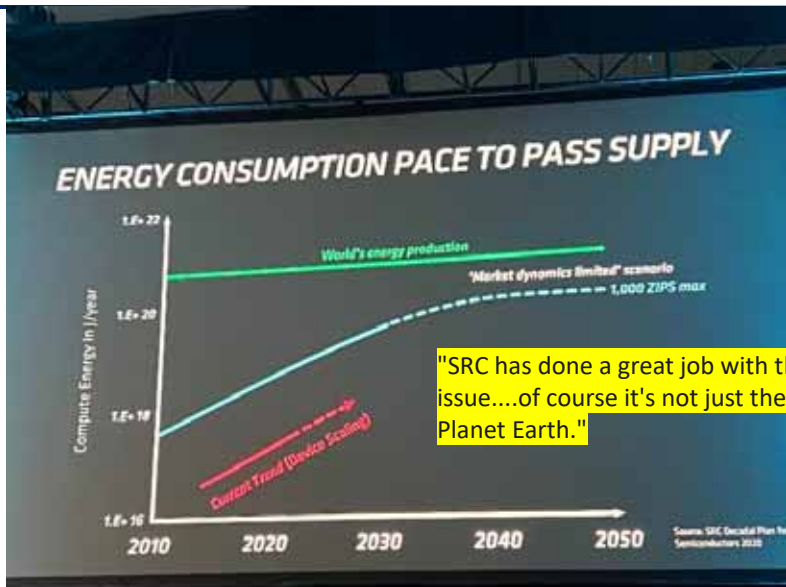
Opening keynote talk at DAC 2022 (by Mark Papermaster, AMD CTO)

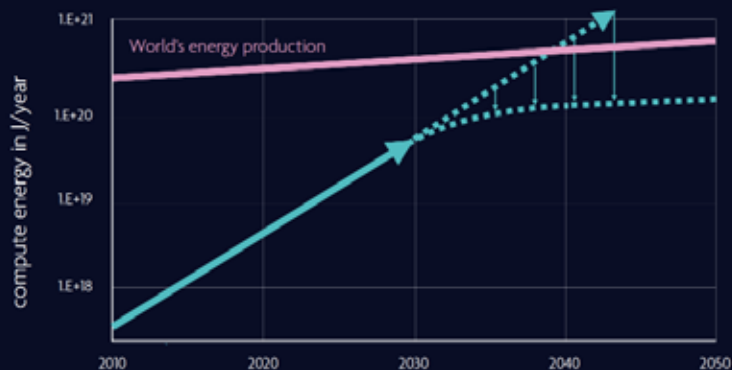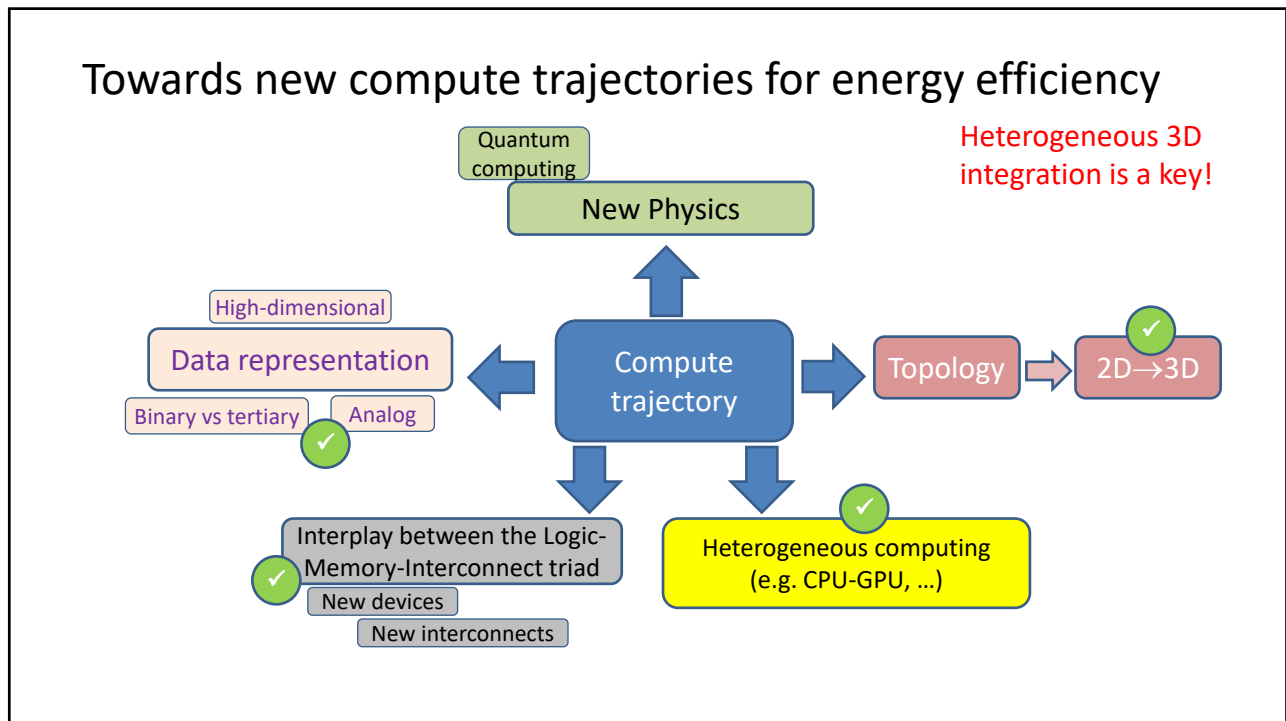Semi Engineering - What Future Processors Will Look Like, Mark Papermaster (AMD)

"SRC has done a great job with their Decadal Plan to highlight this issue....of course it's not just the energy used, it's the impact on Planet Earth."

Luc Van den Hove's presentation slides 16-17

Towards new compute trajectories for energy efficiency

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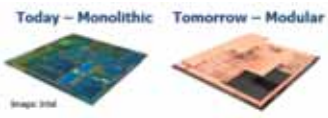# Next microelectronic revolution
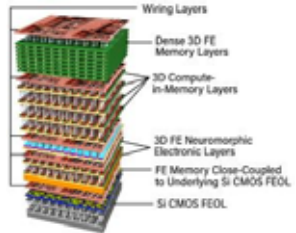
We must evaluate market-driven opportunities "side-by-side" to realize lasting innovations

Today – Monolithic   Tomorrow – Modular

Image: Intel

Wiring Layers
Dense 3D FE Memory Layers
3D Compute-in-Memory Layers
3D FE Neuromorphic Electronic Layers
FE Memory Close-Coupled to Underlying Si CMOS FEOL
Si CMOS FEOL

Priority 1	Priority 2	Priority 3
2.5D and 3D Advanced Packaging	**3D Super Chips**	**Hardware for New Paradigms**
Image: DARPA/Intel https://www.darpa.mil/program/common-heterogeneous-integration-and-ip-reuse-strategies	Image: SIRO, Penn State, Prof. Vijay Narayanan https://news.psu.edu/story/625834/2020/07/15/research/over-10-million-awarded-penn-state-energy-center	Image: IBM Q system displayed at CES 2020 https://www.fierceelectronics.com/electronics/what-quantum-computing

Advanced Packaging, along with 3D monolithic and 2.5D/3D heterogeneous integration, will be the key enabler of the next microelectronic revolution. <u>In fact, advanced packaging+3D is becoming the equivalent of transistor of the Moore's Law and ITRS era.</u>

11

MAPT: A natural next step for Decadal Plan

Microelectronics and Advanced Packaging Technology (MAPT) Roadmap

Decadal Plan for Semiconductors
FULL REPORT

Who/When/Where?

Systems   Hardware   Support

Decadal Plan
defines **WHAT** is needed
- Plan for 10 years

$$MIPS = k\left(BITS\right)^{p}$$

MAPT Roadmap
defines **HOW** to accomplish

MAPT team is developing the first industry-wide 3D semiconductor roadmap to guide the forthcoming microelectronic revolution

CHIPS Funding
implementation plan
- Industry, academia, gov. labs
- NSTC, NAPMP
- Manufacturing USA Inst.

12

Dave Seiler"(NIST): "Charge" to the MAPT team

- Accelerate innovation
- Collapse the timescale
- Foster high risk / high reward
- Change competitors to collaborators

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Mission

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- SRC received an award from NIST Advanced Manufacturing Program for MAPT Roadmap Development

- Goal: Enable the United States to lead in the microelectronic industry through advanced chip making and chip packaging efforts as well as creating a sustainable supply chain

- The Roadmap is
  - identifying technology targets/goals,
  - assessing the state of each technology area,
  - identifying challenges and barriers to advanced manufacturing,
  - defining quantitative objectives and metrics of progress,
  - prioritizing research needs

16

MAPT* Roadmap Will Work to Fill the R&D Pipeline

Sandia Nat Labs - AICoM Workshop - 4/6/2022

Innovation pipeline can be divided into 4 segments:
a) Basis Research
b) Applied Research
c) Development
d) Demo & Scale

Applied Research has reasonable Microelectronics infrastructure but limited for APT, needs 10- 100X growth

Development infrastructure also has limited APT infrastructure, needs 10- 100X growth

*Microelectronics and Advanced Packaging Technologies

Roadmap Executive Committee (REXCOM)

	Primary	Alternate
• **SRC:**	Victor Zhirnov	David Henshall
• **Purdue U:**	Ganesh Subbarayan	Carol Handwerker
• **Georgia Tech:**	Muhannad Bakir	George White
• **SUNY Binghamton:**	Kanad Ghose	Bahgat Sammakia
• **Texas Instruments:**	Jim Wieser	Timothy Rost
• **Intel:**	Henning Braunisch	Johanna Swan
• **AMD:**	Mike Ignatowski	Mark Fuselier
• **IBM**	Timothy Chainer	Dale McHerron
• **NIST**	David Gundlach	Jason Campbell

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MAPT Summary

Total Organizations 102

- SRC Members
- Universities
- Government
- Other Industry
- Trade Org/Society

TWGs by numbers

- TWG A: Workforce Development
- TWG B: Application Drivers & System Requirements
- TWG C: Advanced Packaging & Heterogeneous Integration
- TWG D: Digital Processing
- TWG E: AMS Processing
- TWG F: Photonics & MEMS

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MAPT Summary

University (US) - 29	Industry - SRC Member - 22	Industry - Other - 31
Arizona State University	ASM	3D Glass Solutions
Binghamton University	Advanced Micro Devices, Inc.	Ansys
Clarkson University	Analog Devices, Inc.	Amazon
Darthmouth college	Applied Materials, Inc.	Bosch
Duke University	Arm	Broadcom
Georgia Institute of Technology	Boeing	Cadence
Howard University	GlobalFoundries Inc.	Cardea Bio
Iowa State University	IBM Corporation	Cirrus Logic
Mass. Institute of Technology	Intel Corporation	Cisco Systems, Inc.
Morgan State University	MediaTek, Inc.	eFabless
NC A&T State Univesity	Micron Technology, Inc.	Google
North Carolina State University	Mubadala Technology	Hewlett Packard Enterprise
Oregon State University	Northrop Grumman	Kepler Computing
Pennsylvania State University	Qualcomm	Lumoniq
Purdue University	NXP Semiconductors	Memcus
Rochester Institute of Technology	Raytheon Technologies	Microsoft
Stanford University	Samsung Electronics Co., Ltd.	MITRE
SUNY Polytechnic Institute	Siemens EDA	Nokia
University of California, San Diego	SK hynix Inc.	Rigaku
University of California, Irvine	Texas Instruments Incorporated	Silicon Intervention Inc.
UCSB	Tokyo Electron Limited (TEL)	Si Ware Systems
UCF	TSMC	Skywater Technologies
University of Florida		Softmems
U Illinois, Urbana-Champaign	**University (Int'l) - 5**	Synopsys, Inc.
University of Michigan	Indian Inst. of Tech./Kanpur	Tower Semiconductor
University of Minnesota	KAUST	Twist Bioscience
University of Notre Dame	Khalifa University	Uhnder
University of Texas, Dallas	University of Guelph	Western Digital Corporation
Washington State University	University of Toronto	X-Celeprint
		Zero Asic

Government (Agencies/National Labs) - 7
DARPA
Los Alamos National Laboratory
NIST
Oak Ridge National Laboratory
Pacific Northwest National Laboratory
Sandia National Laboratories
SLAC

Associations/Societies - 8
America's Frontier Fund
IMEC
Innovation Impact Partners
IPC
Materials Research Society
Razdan Research Institute
SEMI
Semiconductor Research Corporation

Total Organizations: 102

20

MAPT Roadmap
Organization Structure

→ Specs
← Requirements

Needed: 3D-IC platform for multi-chiplet system design and advanced packaging

TWG A: Workforce Development
- Pipeline
- Inclusion
- Curriculum
- KSAs
- Experiential Learning
- Internships
- Hiring

System Specification & Application Layer
TWG B: Application Drivers & System Requirements
- Auto
- DC/HPC
- Mobile, Comms and Infra
- Bio-applications and Health
- Edge / IoT
- Defense and Harsh Environments
- EDA (C)
- AI/ML (C)

Foundational Microelectronics Layer
TWG D: Digital Processing
- Logic & Memory Devices
- Nanomaterials & Processes
- Interconnects
- Processors/Accelerators

TWG E: AMS Processing
- Analog & Mixed-Signal
- Power Conversion & Mgt
- Intelligent Sensors
- RF to THz

TWG F: Photonics & MEMS
- Sensors & Actuators
- Communication
- Memory & Computing
- Materials & Processing
- Design & Modeling Enablement

System Integration Layer
TWG C: Advanced Packaging & Heterogeneous Integration
- Chip-package architecture and co-design
- Next-gen interconnects
- Materials
- Substrates
- Assembly & Test
- Performance and process modeling and model validation
- Power Delivery and Thermal Management
- Reliability

Crosscuts (Common to all)
- I: Manufacturing and Process Metrology
- II: Sustainability & Energy Efficiency
- III: Design, Modeling, Test, and Standards
- IV: Supply Chain: Materials, Chemicals, Substrates
- V: Security and Privacy

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2020–2022 global chip shortage

> *This is not a bubble. This is the oil crisis of 1973, but with chips*

Peter Wennink – Topman ASML

in order to grow the capacity the size of the workforce must be increased

22

Forthcoming "workforce crisis"?

- There is already a visible lack of the skilled workforce in semiconductors and now the question is if this will cause another "oil crisis" in the middle term?
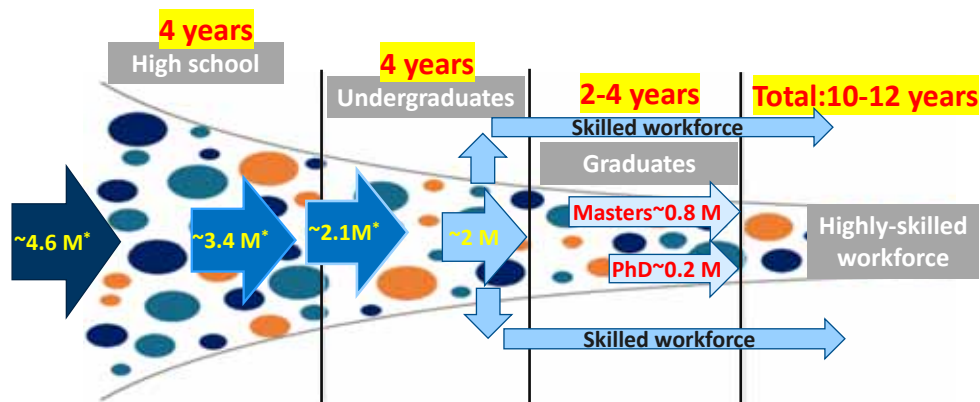- Thus, the semiconductor WFD becomes not just important, but mission-critical.
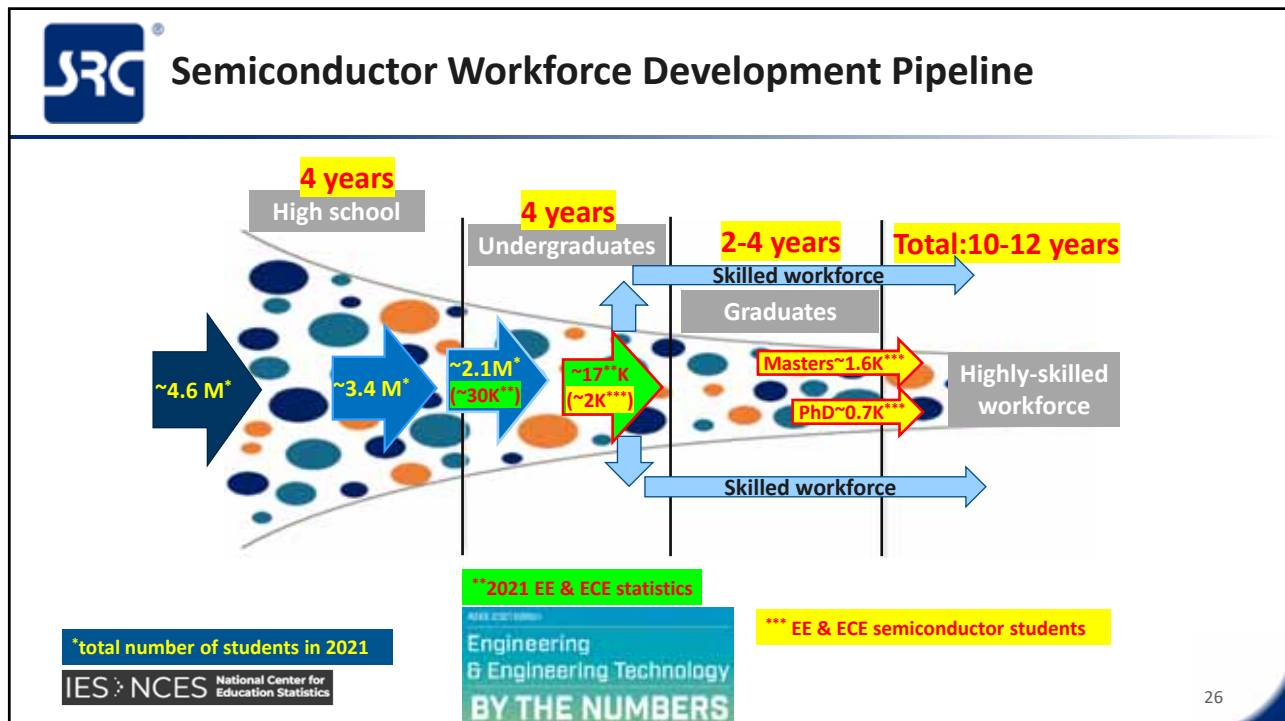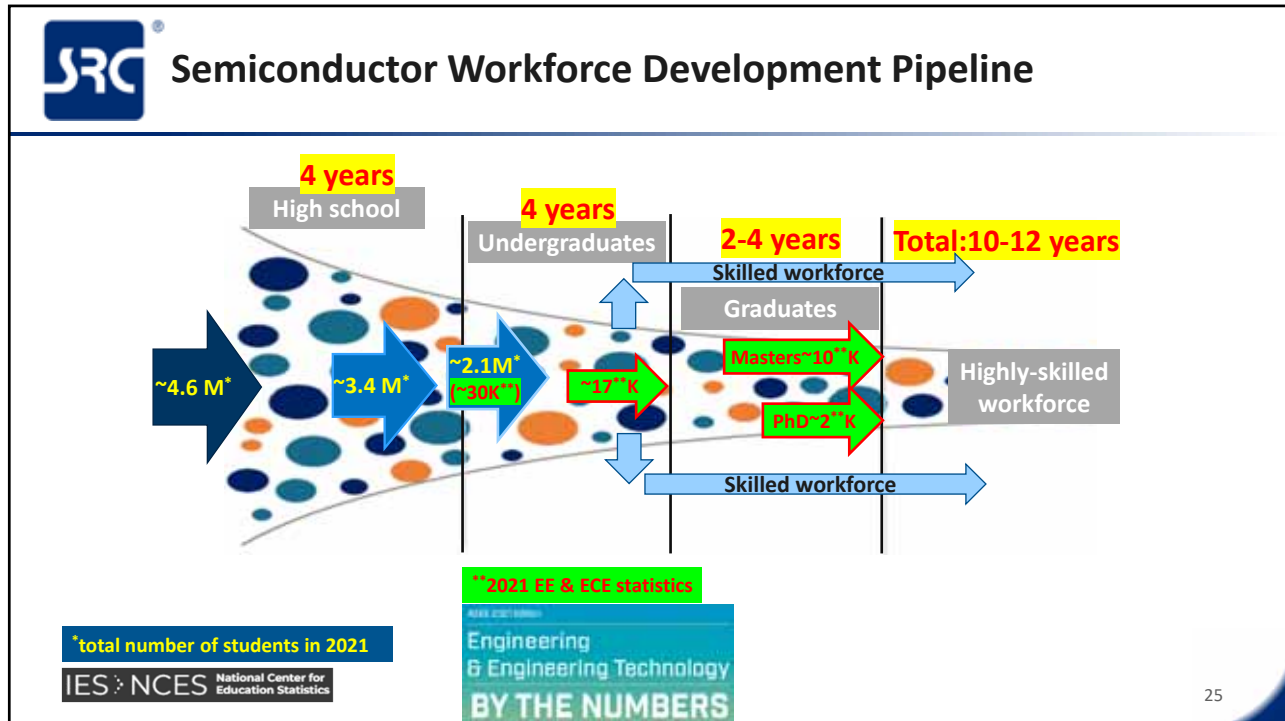
The Five Horsemen Timeline

23

Semiconductor Workforce Development Pipeline

*total number of students in 2021

24

MAPT Roadmap in the context of related roadmaps & roadmapping activities

Two major documents we are building on

HI for Market Applications	HI Components
HPC and Data Centers	Single Chip and Multi Chip
IoT	Integrated Photonics
Medical, Health and Wearables	Integrated Power Electronics
Automotive	MEMS and Sensor Integration
Aerospace & Defense	RF and AMS
Mobile	

We don't want to recreate these documents
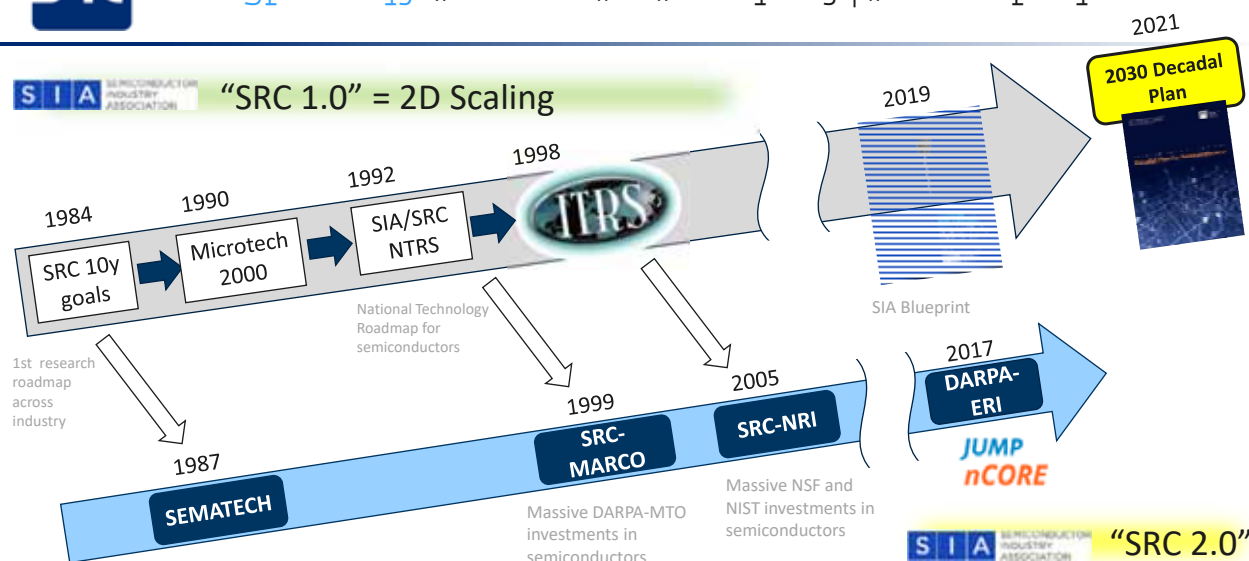
Taxonomy and Terminology

- **Problem Statement/Grand Challenge**
  - Example– "Moon shot", SRC Decadal Plan
- **"RADAR" Screen**   MAPT
  - Broad list of promising technologies (also in SRC Decadal Plan . . .)
- **Roadmap**
  - Significant down-selection from radar screen (funnel model) Where? When?
  - Time as the x-axis– a path to the grand challenge destination
- **Plan/Strategic Plan**
  - More specific still – not just Where? When? But also Who? How?
- **Blueprint/Statement of Work**
 - Very specific– budgets, deliverables, contracts . . .

31

MAPT: Charge to Work

- Make the MAPT roadmap very comprehensive so it will be adopted by global microelectronic community
  - Will enable a new Microelectronic Manufacturing USA Institute

- Establish quantitative metrics to develop the roadmap, so all TWGs can use it.

MAPT team is developing the first industry-wide 3D semiconductor roadmap to guide the forthcoming microelectronic revolution

32

MAPT Roadmap Timeline
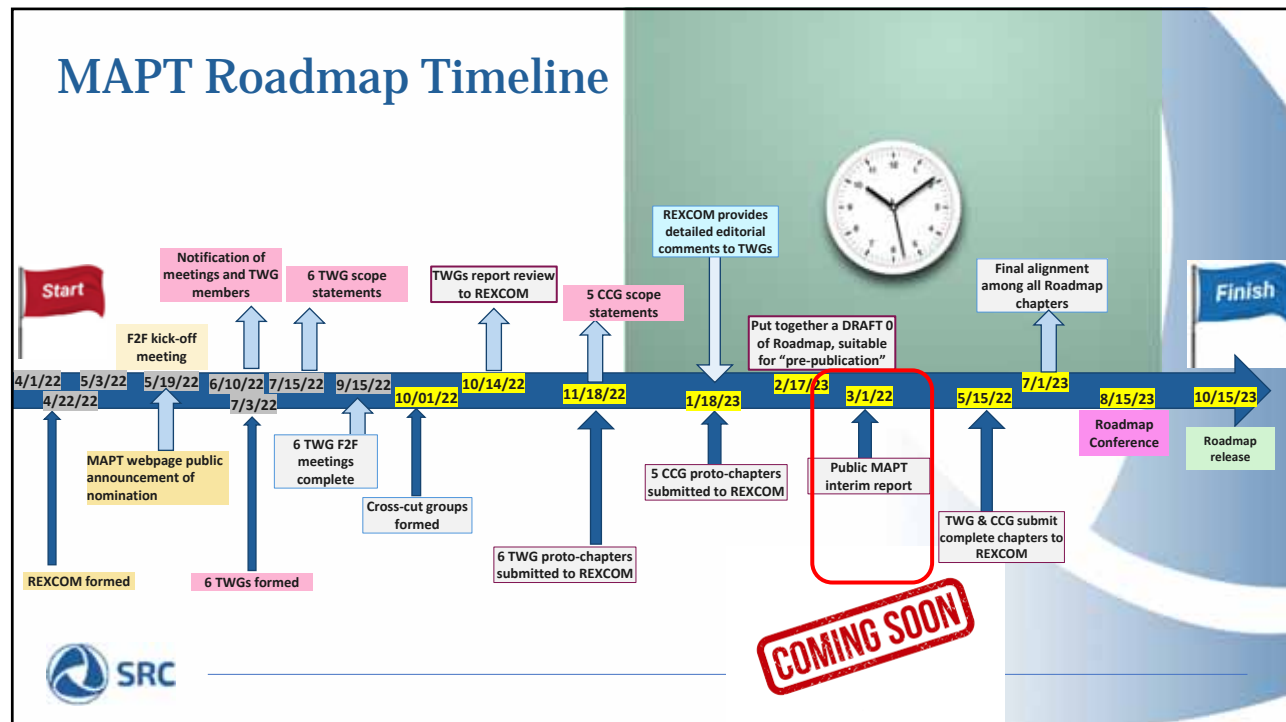
Public MAPT Interim Report

- NIST request for an early complete version
- Important for CHIPS planning
- Collect feedback sooner

- Release date: 3/1/2023

Summary

- On March 1st, we will release the Interim Report for the Microelectronic and Advanced Packaging Technologies Roadmap (MAPT)
  - an industry-wide initiative of major impact on the semiconductor industry
  - introduces a new comprehensive Roadmap to guide the forthcoming microelectronic revolution, like the ITRS has served in the past.
- The MAPT Roadmap manifests the transition from
  - a two-dimensional (2D), smaller-transistor-centric paradigm to
  - a universal 3D and heterogeneous integration microelectronics platform
    - seamless integration of multiple electronic, photonic, micromechanical, etc. chiplets
- Advanced packaging is critical to the future of microelectronics!
- The MAPT Roadmap supports the 2030 Decadal Planfor Semiconductors
  - projects 10-15 year targets and timelines highlighting possible solutions for the identified targets including
    - Semiconductor Manufacturing Technologies
    - Workforce Development

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35

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Thank You

Victor Zhirnov, Chief Scientist: victor.zhirnov@src.org

David Henshall, Director of Business Development and Government Relations: david.henshall@src.org

Todd Younkin, President and CEO: todd.younkin@src.org

36