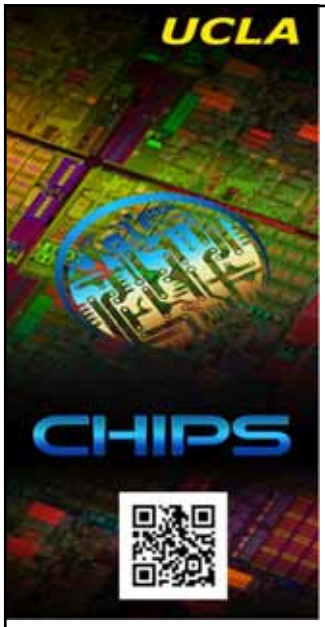

A Manufacturing Roadmap for Heterogeneous Integration and Electronics Packaging (MRHIEP)

Presentation to HIR annual Meeting Feb 2023

Steering Committee

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Background

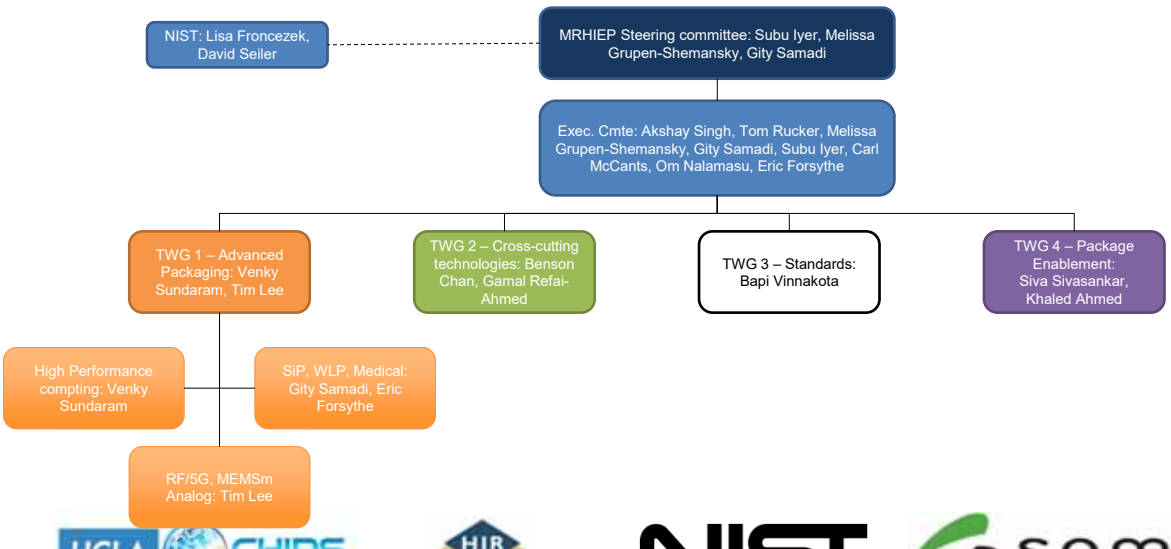
- Translate the HIR roadmap into a simple manufacturing roadmap for advanced packaging
  - Tools, processes, enablement standards and interdependencies
- Individual working group reports
  - 1. Technology - Venky Sundaram (3D system Scaling)
  - 2. Cross cutting issues – Gemal Refai-ahmed, Benson Chan
  - 3. Standards: Bapi Vinnakota - (ODSA)
  - 4. Supply chain – Siva Sivashankar

Goals

- Translate the HIR into a blueprint for on-shore manufacturing that can drive materials, equipment, manufacturing processes, the supply chain, and product manufacturing with a trained workforce in the USA
- Duration 18 months – trying to accelerate

- In plain English: A Quick Start guide for an advanced packaging manufacturing facility in the US:
  - tools (hardware and software),
  - Processes
  - Supplier infrastructure

Organization



Approach

- As appropriate add sections each of the chapters in the HIR roadmap that focus on translation of the roadmap elements into actional manufacturing options
- Draw extensively on the existing HIR working groups based in the US to translate the chapter content into manufacturing roadmaps
- Work closely with other allied groups that are also part of the NIST effort such as SRC,
- Co-opt industry associations such as iNEMI, iMAPS, SIA, ODSA …..
- Work closely with other NIST sponsored Institutes such as the Smart Manufacturing Innovation Institutes eg. CESMII in SoCal
- Additional information available here and here

UCLA CHIPS HIR NIST semi

Working from the HIR roadmap 2021 edition

- Application Driven Chapters
  - e.g.: chapters 1-7, 12
- Technology Driven Chapters
  - e.g.: chapters 8-11, 15,16, 20-24
- Design Driven Chapters
  - e.g.: chapters 13,14
- Eco system driven Chapters
  - e.g. Chapters 18, 19

UCLA CHIPS HIR NIST semi

Aditional Topics to include

- Sustainable Manufacturing (Melissa Grupen-Shemansky/Gity Samadi)
- Standards
  - Electrical
  - Mechanical
  - Equipment, data management security, traceability
- Workforce development (high schools, Vocational Schools, 2-year colleges, 4-year colleges, Graduate Schools, on-the-job learning)

TWG groups

- TWG 1: Advanced Packaging (3 subgroups)
  - Ch 8. Single and multi chip
  - Ch 9. photonics
  - Ch 22. Interconnects for 2D and 3D
  - Ch 10. power electronics
  - Ch 11. MEMS
  - Ch 12+. RF mm wave and THz
  - Ch 15. Emerging material
  - Ch 21. SiP and module
  - Ch 23. Wafer-level packaging (WLP) including FHE & medical electronics)
- TWG 2: Cross cutting issues
  - Ch 13. package-signal Co-design
  - Ch 14. Modeling and simulation
  - Ch 17. Test
  - Ch 20. Thermal
  - Ch 24. Reliability
- TWG 3: Standards
  - Mechanical Standards
  - Electrical Standards
- TWG 4: packaging enablement
  - Ch 18. Supply chain
  - Ch 19. Cyber security
  - Smart Manufacturing

TWG1: Advanced Packaging & Heterogeneous Integration

- ***Goal:*** Create a manufacturing roadmap and generic blueprint for Advanced Packaging & Heterogeneous Integration in two key areas (a) AI and HPC, (b) Medical, wearable and hybrid electronics, building from the HIR Roadmap and other relevant industry roadmaps – focus on 5G/6G mm-wave will reference the iNEMI MAESTRO project
- ***Themes & Sub-Groups:***
  - AI and HPC sub-group focused on key platforms driving the advanced packaging roadmap - (i) Advanced substrates and interposers, (ii) fanout wafer and panel level packaging, (iii) hybrid bonding & 3D-IC, (iv) fine pitch bumping & assembly.
  - Medical, wearable and hybrid electronics sub-group focused on two major platforms (i) flexible substrates and integration, and (ii) rigid substrates and integration.
- ***Past Six Months Summary:***
  - Completed detailed reviews of relevant HIR roadmap chapters and created first-of-its-kind chapter summaries for broader dissemination.
  - Created unified outline for manufacturing blueprint – For each platform, (a) End User Parametric Targets (3, 5, 7 year), (b) Generic Mfg Process Flow, (c) Materials List and Top Suppliers by Geography, (d) Tools List and Top Suppliers by Geography, (e) Gaps and Challenges in Enabling Near and Mid Term Manufacturing Infrastructure, with potential solution pathways.
- ***Current Quarter Focus:*** Complete first draft of manufacturing blueprint with Process Flows, Materials List and Tools List. On track to complete first draft by the end of Q1
- ***Active Participants (in alphabetical order):*** 3D System Scaling, Ajinomoto, Applied Materials, Boeing, dPiX, EMD, Fujifilm, Intel, Micron, Northrop Grumman, Resonac (Showa Denko), SEMI, Tokyo Electron, UCLA, Ulvac, US Army.

TWG2: Cross Cutting Issues

- ***Goal:*** Create a manufacturing roadmap and generic blueprint for Advanced Packaging & Heterogeneous Integration in two key areas (a) AI and HPC, (b) Medical, wearable and hybrid electronics by understanding the packaging roadmap maybe affected by reliability issues, thermal trends and modeling / simulation methodologies that may need to be developed to support HIR
- ***Themes & Sub-Groups:***
  - Thermal trends are all pushing the needs for new and novel thermal management solutions to support higher power requirements (>1000 Watts), 2.5 and 3D solutions for high power stack dies, backside power delivery etc. HPC will drive much of this development, the use of large substrates, multiple chiplets, stacked high power and others. The drive to understand package warpage of very complex multiple chiplets in a large package will drive new thermal solutions
  - Increasing system complexity, functionality, diversity and density, as a result of the twin drivers of Heterogeneous Integration (HI) and miniaturization, involving multiple chiplets, will pose new challenges for meeting reliability targets. Modeling and Simulation sub group extended to cover more than packaging- added materials, devices, electronics, package, subsystem and others co-design. Also split and formed teams for Simulation and Modeling
- ***Past Six Months Summary:***
  - Completed detailed reviews of relevant HIR roadmap chapters and identified unique packaging needs to support HPC and wearable/flexible/medical packaging
- ***Current Quarter Focus:*** Continue identifying packaging trends and understand gaps in technologies and where research needs to be focused on.
- ***Active Participants (in alphabetical order):*** Ajinomoto, AMD, Analog Devices, Binghamton University, CMC, EMD Group, Google, Greenwich.AC, Lamar, MEPTEC, Meta, Soft MEMS, Microsoft, Qualcomm, Tesla

TWG3: Standards

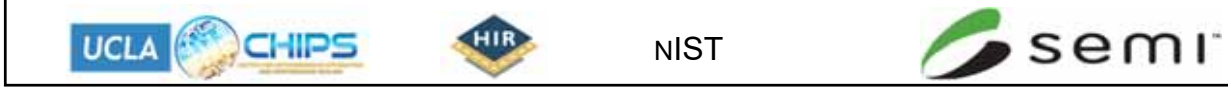
- ***Goal:*** As part of a Quick Start Guide to establishing a new economically viable Heterogeneous Integration and Electronic Packaging facility in the United States, identify the open standards relevant to packaging chiplet-based semiconductor products.
- ***Summary of work done:***
  - Identified products where packaging costs are a significant component of total product costs. That is, products that require advanced packaging technology.
  - Enable cost-efficient mass customization - recommend standards for (or identify new standards needed for) modularization, and thereby automation, to reduce costs compared to current packaging and assembly methods.
- ***Current quarter Goal:*** Focusing on defining a modular HPC architecture to demonstrate the potential benefit of modularity in assembly and packaging. Aim to finish a draft by the end of Q1.
- ***Active Participants:*** AMD, DOE, IBM, Intel, Meta, Microchip, Micron, OCP, UCLA

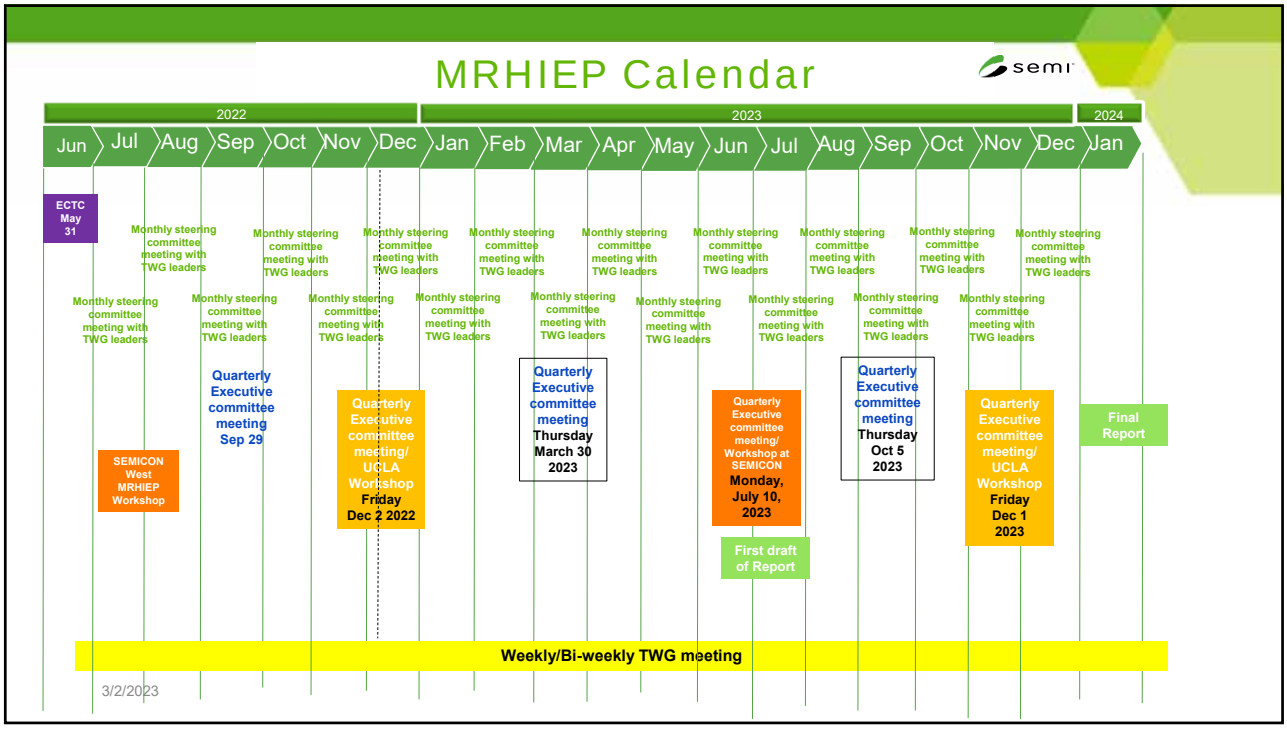
TWG 4: Manufacturing and Supply Chain

- ***Goal:*** TWG4 focus is Manufacturing & Supply Chain – manufacturing roadmap and execution blueprint in key areas of HPC & Medical Devices
- ***Theme based sub groups:*** Supply Chain, Security, Test and Smart Manufacturing
- ***Current progress:*** Each sub-team worked to expand on the sub-topics that will be addressed within and in-collaboration within WGs
  - Supply Chain - Focus to identify and define materials, equipment & processes, constraints, drivers, and proposed solutions
  - Security – Focus on Design-Time, Manufacturing environment and execution phase security along with future break through technology (e.g. Quantum, 6G etc) security considerations
  - Test – Focus on available test methods & techniques for a variety of HIR test areas (e.g. RF, Photonics etc.) and standards gaps and priorities.
  - Smart Manufacturing – Focus on identifying & deploying critical Industry4.0 technology for future cost-effective HI manufacturing lines
- ***Next Steps:***
  - TWG4 will continue to expand and elaborate on the 4 main sub-topics towards a clear actionable manufacturing roadmap with specific focus on HPC and Medical Devices
  - Clearly articulate gaps in future technologies (TSV, Interposers), material supply, equipment, and standards, and roadmap items to close these gaps.
- ***Active Participants:*** SEMI, Binghamton U, KnS, Google, EMD, DpiX, Applied Materials, LAM Research, Veeco, Advantest, UCLA, Intel

Interaction with other roadmap efforts

- We are interacting on monthly basis with INEMI and SRC on the roadmapping efforts to avoid duplication.
- Overlap is minimal as MRHIEP is focused specifically on Heterogeneous integration drives from HIR chapters





Summary

- Working groups have been constituted and are building the relevant roadmaps
- The next executive meeting is at March End
- The first draft will be released in July 2023
- The final report will be released in January 2024

Acknowledgements

- List of the TWG members

https://docs.google.com/document/d/1-4PjIe938j2NqaHm8cCzXCtMBkivJuA/edit