Heterogeneous Integration Roadmap 2023 Annual Workshop

HETEROGENEOUS INTEGRATION ROADMAP

HIR 2023 Annual Conference

WLP
TECHNICAL WORKING GROUP

Heterogeneous Integration Roadmap 2023 Annual Workshop

Presentation Outline

- WLP Technical Working Group
- Our Focus Area
- WLP Market Drivers
- Industry Trends
- Key Challenges
- Future work & Acknowledgements

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WLP TWG Team

New Members are Welcome!

- **Chairs:**
  - Rozalia Beica – AT&S
  - Tony Shao - TSMC
- **Team Members:**
  - CP Hung - ASE
  - Chuan Seng Tan – Nanjang University
  - Harry Shimamoto – AIST
  - Hiroyuki Shida – ShinEtsu
  - John Hunt – ASE
  - Kuldip Johal - Atotech
  - Li Li - Cisco
  - Michael Liu – JCET
  - Seung Wook Yoon – Samsung
  - Steffen Kroehnert – ESPAT
  - Suresh Ramalingam – Xilinx
  - Sze Pei Lim - Indium
  - Takeshi Wakabayashi – HTL
  - Tanja Braun – Fraunhofer IZM

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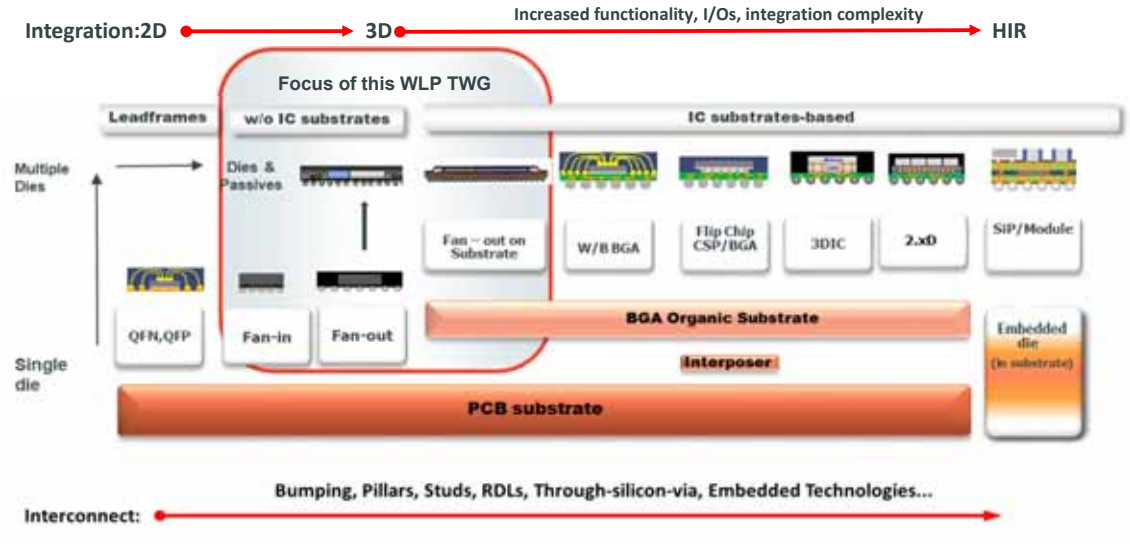
Wafer Level Packaging TWG



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Wafer and Panel Level Packaging

WLP – Wafer Level Package: **Includes all packages that are processed as packages while still in Silicon or molded wafer form, prior to singulation**

Wafer Level Chip Scale Package - WLCSP

- Since WLCSP by definition is "Chip Scale", there are a limited number of variations that lend themselves to Heterogeneous Integration (HI)

Wafer Level Fan-out Packaging – WLFOP & FOPLP

- Fan Out Packaging Technology was developed to expand this packaging capability beyond the limits of the die including Low to High Density formats
- While Fan Out has been processed in wafer format, nearly all suppliers are working to develop rectangular panel versions

The WLP TWG includes Fan Out packages that are manufactured on both wafer & panel level

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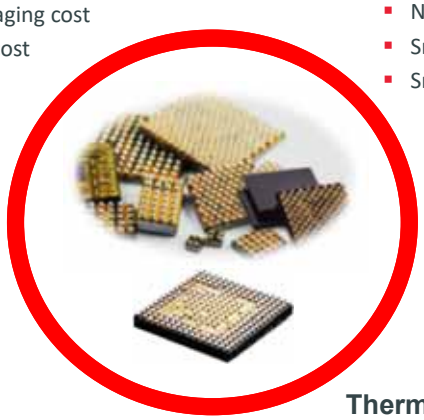
Market Drivers for WLP

Cost
- Lower packaging cost
- Lower test cost

Form-Factor
- No laminate substrate required
- Smaller thickness
- Smaller footprint



I/O Density
- Smaller pitches
- Smaller dies
- Higher density of I/Os

Electrical Performance
- Shorter interconnects
- Lower parasitics
- Higher package speed
- Higher frequencies

Integration
- IPD
- SiP
- 3D

Thermal Performance
- Lower power consumption
- Lower thermal resistance

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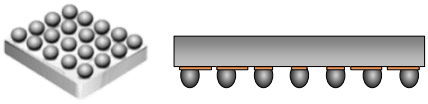
Fan in WLP: Market Drivers & Enabling Technologies

- **Main Markets**
  - Mobile (90% market)
- **Market Drivers & Capabilities**
  - Small footprint
  - Better electrical performance
  - Lower cost package
  - Thinner package
  - Lower thermal resistance

Applications of WLCSP Packaging Platform



- **Main Enabling Technologies:** wafer processing, bumping, thin film RDL

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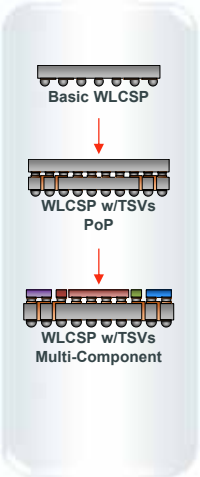
Heterogeneous Integration using WLCSP

WLCSP



- **2D – Die to Die face to face stacking**
  - Secondary die mounts on pads between solder balls on face of die
  - Can be active die or MEMS, or IPD die

- **3D – TSV through WLCSP – Die face to Die backside stacking**
  - Uses TSVs to allow secondary die to be mounted on backside of primary die

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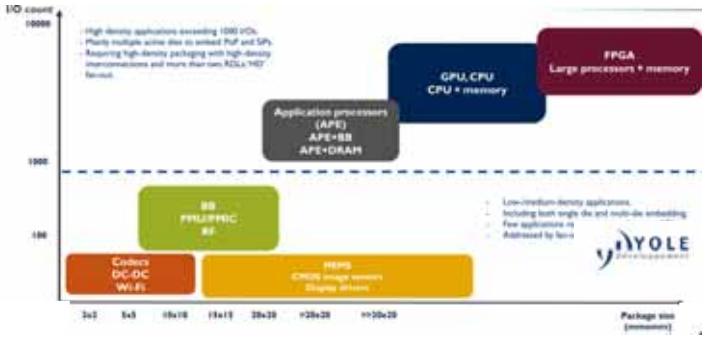
Fan-out: Market Drivers & Enabling Technologies

- **Main Markets**
  - Mobile (90% market) (LD & MD)
  - Networking (HD)
- **Market Drivers & Capabilities**
  - Small footprint
  - Better electrical & thermal performance
  - Lower power consumption
  - Lower cost package
  - Thinner package
  - Larger Package Size
  - Improved Reliability performance
  - PoP & SiP Package capability
  - An alternative to SoC
  - Finer L/S

Applications of Fan-Out Packaging Platform



- **Enabling Technologies:** wafer processing, bumping, thin film RDL

specific to Fan-out: wafer molding, low temperature cure RDL polymer, panel processing

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

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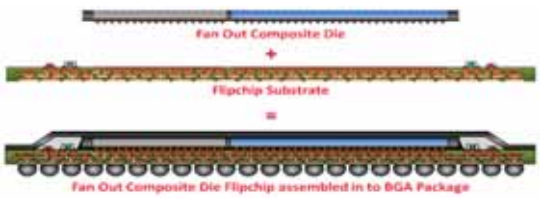
Heterogeneous Integration using Fan-out

2D Packaging

3D Packaging

Hybrid Fan-out



ASE GROUP

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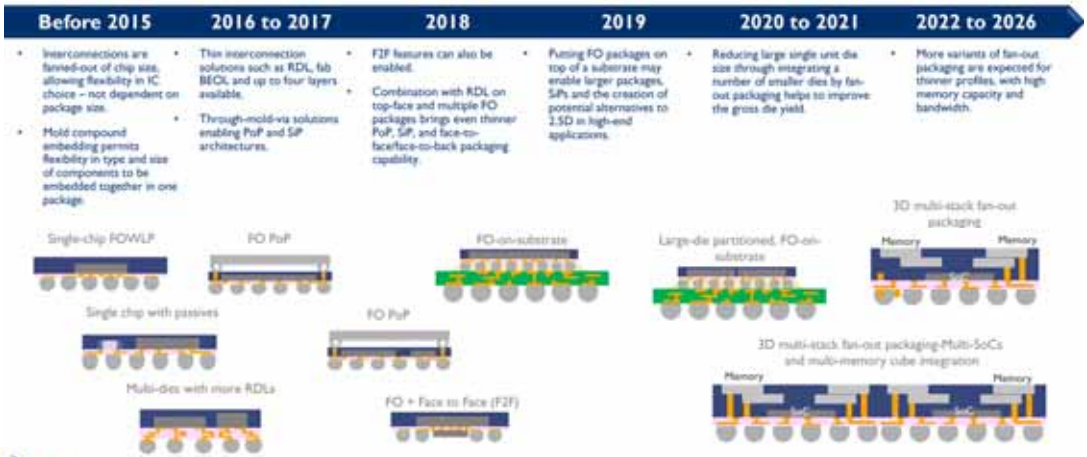
Fan-out Evolution: From Single Die FO to FO SIP



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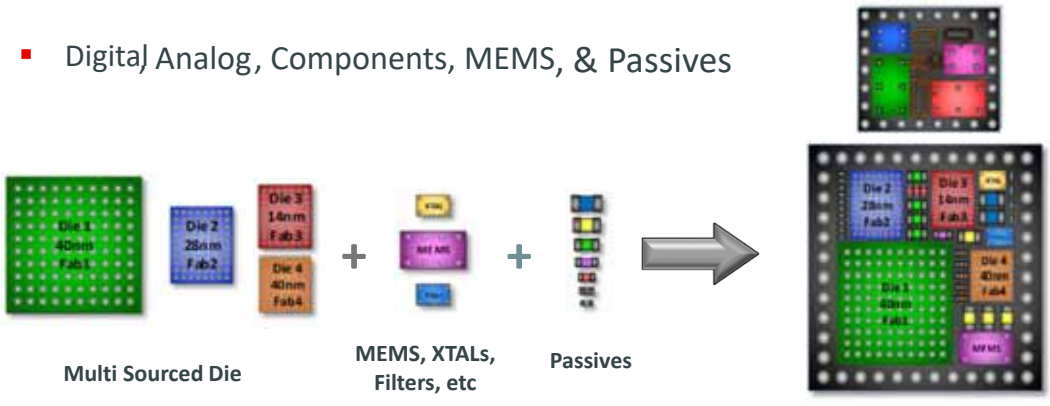
FO – Enabling Multi-Chip Heterogeneous Integration

- Fan out allows partitioning of functionality
  - Digital, Analog, Components, MEMS, & Passives



Source: ASE **Fan Out SiP**

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Key Challenges

Common challenges for WLP

- **Increasing package size due to reliability concerns**
- **Thin package profile using very thin silicon die** (wafer handling becomes increasingly difficult at lower thicknesses)
- **Heterogeneous integration of different materials (**CTE mismatch; dielectrics, conductors and semiconductor devices, interfacial adhesion, stress/warpage, etc.)
- **Cost Reduction**

Specific →

Fan-in

- **Increasing I/O count within small form factor**
- **Increased complexities with dies at more advanced nodes**

Fan-Out

- **Die shift during/after Molding**
- **Controlling levels of Warpage at each process stage**
- **Topography when using different device sizes**
- **Chip to mold non-planarity and RDL distortion**
- **Fine Line and Via capability for high density Fan Out package requirements**
- **Processes to allow inclusion of low cost passive components**
- **Development of Equipment, Materials & Processes suitable for Panel Production**

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Future Work

Included in current chapter

- **Markets and Applications**
- **Market drivers / benefits of WLP/PLP**
- **Industry activities overview**
- **Major challenges**
- **Discussions of key technical issues**
- **Roadmap**

Future work

- **Next Iteration of Chapter will expand on, and update all topics as applicable**
- **Expand on WLP integration technologies to various applications and alignment with other TWGs**
- **Feedback welcomed**

Acknowledgement

WLP TWG & Contributing Members

- David Butler – SPTS (UK)
- Douglas Yu – TSMC (TW)
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- Michael Liu – JCET (US)
- Monita Pau – DuPont (US)
- Rozalia Beica – AT&S (AT)
- Takeshi Wakabayashi – HTL (Japan)
- Tanja Braun – IZM Fraunhofer (Germany)
- Tom Buschor – Nuvotronics (US)

Interested in joining the WLP team? - Please send email to rbeica.semi@gmail.com