Heterogeneous Integration Roadmap for Aerospace and Defense (HIR-A/D)

Boeing Technical Fellow, BR&T
2022 IEEE Board of Directors
2022 IEEE Region 6 Director
IEEE Industry Engagement Committee
IEEE FNTC Vice-Chair
IEEE HIR TWG Co-Chair
Past President, IEEE MTT-S

Aerospace-Defense TWG Co-Chairs:
Tim Lee (The Boeing Company)
Dan Blass (Lockheed Martin)
February 2023

Timothy Lee, currently a Boeing Technical Fellow, is responsible for the development of RF and digital electronics for advanced communications networks and sensor systems. In the IEEE, Tim is promoting the use of technology to benefit humanity.

Summary of Topics Covered

- CHIPS Act – Department of Commerce
- EU CHIPS Act
- DoD Microelectronics Commons
- OSD/Crane SHIP, STEAM PIPE, STAMP
- DARPA ERI 2.0
  - NGMM
  - MiniTherm3D
- IBAS Cornerstone RESHAPE
- NDIA 3DHI Working Group

CHIPS for America Research and Development Program

CHIPS for America Incentives

$39 billion for manufacturing

Two component programs:
1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

$11 billion for R&D

- National Semiconductor Technology Center
- National Advanced Packaging Manufacturing Program
- Manufacturing USA institute(s)
- National Institute of Standards and Technology measurement science

Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

Workforce development

IEEE USA in 2021-2022 let the way to inform Congress on the importance of the CHIPS Act

3

National Semiconductor Technology Center

Vision: Will serve as the **focal point** for research and engineering throughout the semiconductor ecosystem, advancing and enabling disruptive innovation to provide U.S. leadership in the industries of the future.

Structure: A public-private consortium as an independent entity with a governing board informed and advised by industry, academia, government, and key stakeholders.

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National Advanced Packaging Manufacturing Program
CHIPS for AMERICA
• Strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem
• Leverage public-private partnerships, that can include support for facilities managed by the NSTC and MUSA
• Broad range of technologies:
• Heterogeneous integration
• Wafer and panel-based approaches
• Tooling and automation
• Substrate technology
5

NAPMP Target Areas
CHIPS for AMERICA
Technology innovation
Create an R&D environment advancing the state-of-the art in advanced packaging.
Ecosystem support
Investments to bolster the growth in domestic capacity and enhance capabilities for competitive edge.
Co-design and simulation
Chiplets
Pilot packaging facilities
Tooling and automation
Materials and substrates
6

TSMC Building Advanced Node Fabs in Arizona

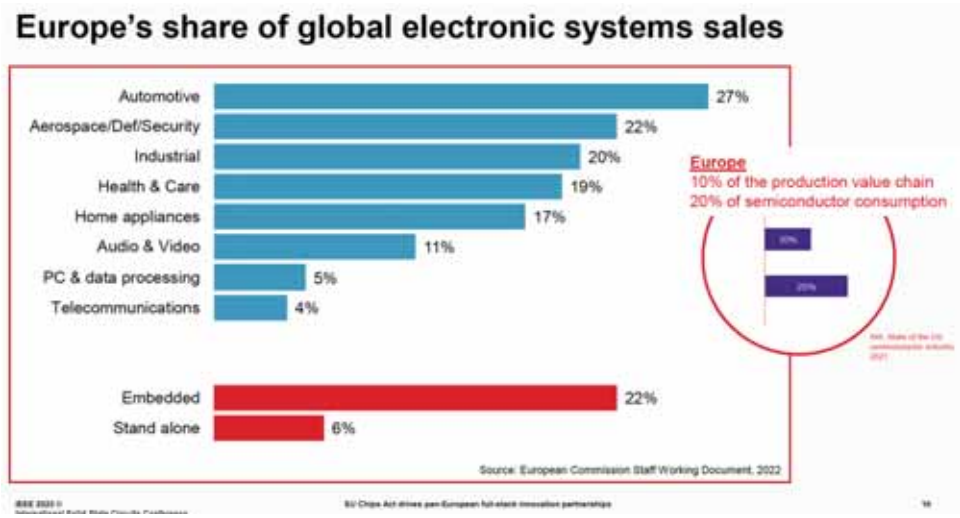
- NYTIMES: 22 February 2023
  - "Taiwan Semiconductor Manufacturing Company, the world's biggest maker of advanced computer chips, is upgrading and expanding a new factory in Arizona that promises to help move the United States toward a more self-reliant technological future."
  - "But to some at the company, the $40 billion project is something else: a bad business decision."
  - "Caught in a deepening battle between the United States and China over technological leadership, TSMC has tried to hedge its bets — only to find that its actions are creating new kinds of tensions"
- The political capital and goodwill arrived at building this FAB beachhead in the United States in addition to the CAPEX and tax incentives arrived at from the CHIPs Act, passed at 2022, are well worth the additional pressure on TSMC.

https://www.nytimes.com/2023/02/22/technology/tsmc-arizona-factory-tensions.html

EU CHIPS Act

https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

Europe's Strength is in Automotive and A/D Electronics



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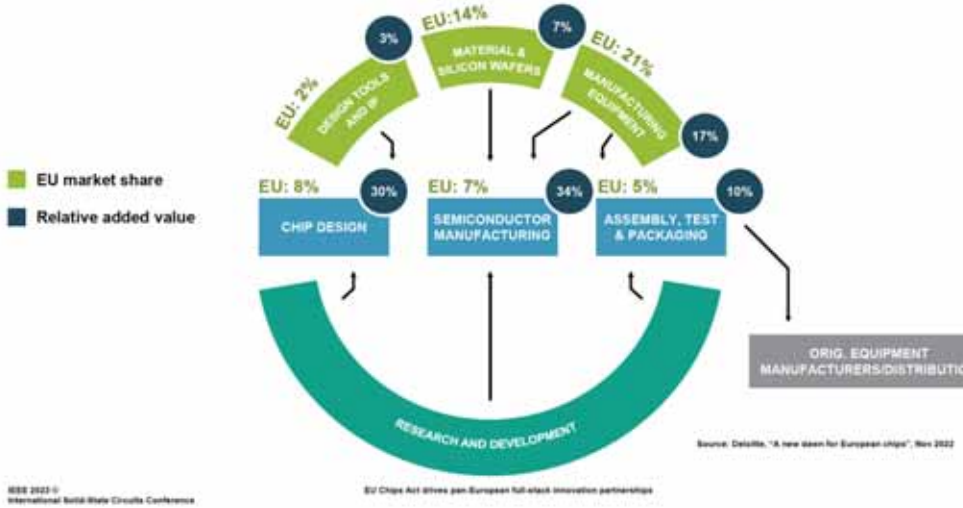
Europe's presence in the semiconductor supply chain



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European Chips Act

As announced by the EC on 8 February 2022:

"With the European Chips Act, the EU will address semiconductor shortages and strengthen Europe's ***technological leadership****.*

It will mobilise ***more than € 43 billion of public and private investments*** *and set measures to prepare, anticipate and swiftly respond to any future supply chain disruptions, together with* ***Member States*** *and our* ***international partners****."*

European Chips Act

Strengthen Europe's research and technology leadership towards smaller and faster chips

Build and reinforce capacity to innovate in the design, manufacturing and packaging of advanced chips

Put in place a framework to increase production capacity to 20% of the global market by 2030

Address the skills shortage, attract new talent and support the emergence of a skilled workforce

Develop an in-depth understanding of the global semiconductor supply chains

J. De Boeck, "EU Chips Act drives pan-European full-stack innovation partnerships," imec, ISSCC 2023 Plenary

European Chips Act focuses on five specific areas

- ***Research and Development*:** Calls for further allocations of funds for research and development (R&D) to keep up with global competitors.
  - Further invest €3.3 billion in two current programs: €1.65 billion to the "Horizon Europe" program and €1.65 billion to the "Digital Europe" program.
  - The "Horizon Europe" program focuses on pre-competitive research, development, and innovation in the area of semiconductors
  - "The Digital Europe" program looks to make digital domains and technology widely available for all businesses and the general public to maximize performance in key industries.
- ***"From the lab to the fab":*** Effective translation research into industrial innovation and market-feasible products. Europe must bridge the gap between excellence in laboratory research and onshore manufacturing to sustain leadership in semiconductors and other advanced technologies.
- ***Industry Production*:** Europe is looking to host "first of its kind" facilities through the creation of Integrated Production Facilities, which are factories that design and produce semiconductor components that serve the European market and through Open EU Foundries for chip design, which are facilities that design and produce components for other industrial actors such as medical devices and computer programming.
- ***Local Support*:** Support the workforce development - local skill base and the network of smaller, innovative companies and start-ups as a part of their strategy to grow their semiconductor and high technology ecosystems. The "EU Chips Fund" which will contribute €2 billion to create a more competitive market for semiconductor start-ups to participate in and address skill shortages. Additionally, the Commission wants to help in the retention of employees that have the skills that these start-ups need to be successful and to find industrial partners for these start-ups to collaborate with.
- ***Overhaul the European Supply Chain*:** EU Commission wants to encourage Member States and industry stakeholders to coordinate efforts towards an improved European supply chain for semiconductors.. To enable a rapid response to the current shortages, the Commission has created a list of recommendations to the Member States. Along with streamlining policies of member states, Europe is also looking to build partnerships with the United States and other nations to create a more resilient global semiconductor network.

https://www.csis.org/blogs/perspectives-innovation/european-chips-act-strategy-expand-semiconductor-production

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EU CHIPS Act Proposals

- Ministers of European Parament (MEPs) has voted to back the Chips Joint Undertaking proposal, implementing most of the measures put forward under a "Chips for Europe" initiative, as part of the wider Horizon Europe program, the stated aims of which are to support large-scale capacity building through investment in EU-wide research and development infrastructure.
- This will initially pool together about €11 billion ($11.78 billion) drawn from EU central funding, EU countries, and the private sector. The Chips Act aims to eventually unlock €43 billion (£46 billion) in funding for the European semiconductor sector.
- Rapporteur for the Chips Act, MEP Dan Nica said in a statement: "The EU Chips Act should establish Europe as a key player in the global semiconductors arena. Not only does the budget need to be commensurate with the challenges and funded through fresh money, but the EU should lead in research and innovation, have a business-friendly environment, a fast permitting process and invest in a skilled work force for the semiconductor sector."

https://www.theregister.com/2023/02/16/eu_chips_act_bills/

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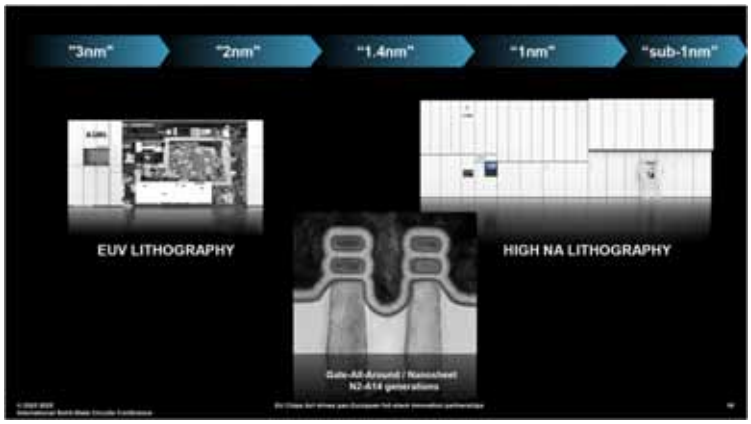
EU is Strong in Advanced Lithography



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EU: Leader in FD-SOI

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Intel Investments in EU Semiconductor Centers

- Pat Gelsinger, CEO of Intel:

  "Our planned investments are a major step both for Intel and for Europe. The EU Chips Act will empower private companies and governments to work together to drastically advance Europe's position in the semiconductor sector. This broad initiative will boost Europe's R&D innovation and bring leading-edge manufacturing to the region for the benefit of our customers and partners around the world. We are committed to playing an essential role in shaping Europe's digital future for decades to come."

- Intel announces building new fabs in the EU ($88B investments)
  - Magdeburg (Eastern Germany) as the site for its new €17B mega chip manufacturing complex – "Silicon Junction"
  - Other countries including Italy also courting Intel for a new factory
- Intel wants €10B in EU subsidies

https://www.intel.com/content/www/us/en/newsroom/news/eu-news-2022-release.html

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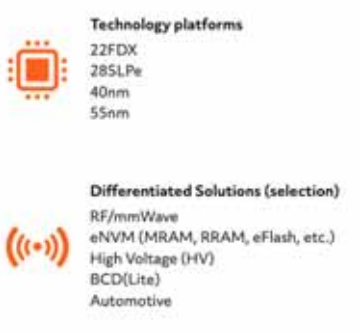
Other Fabs in EU

- GlobalFoundries – Dresden, Germany, 850,000 wafers/year
- Infineon has the green light for €5B Dresden chip fab, secured €1B in subsidies; total site cost: €20B



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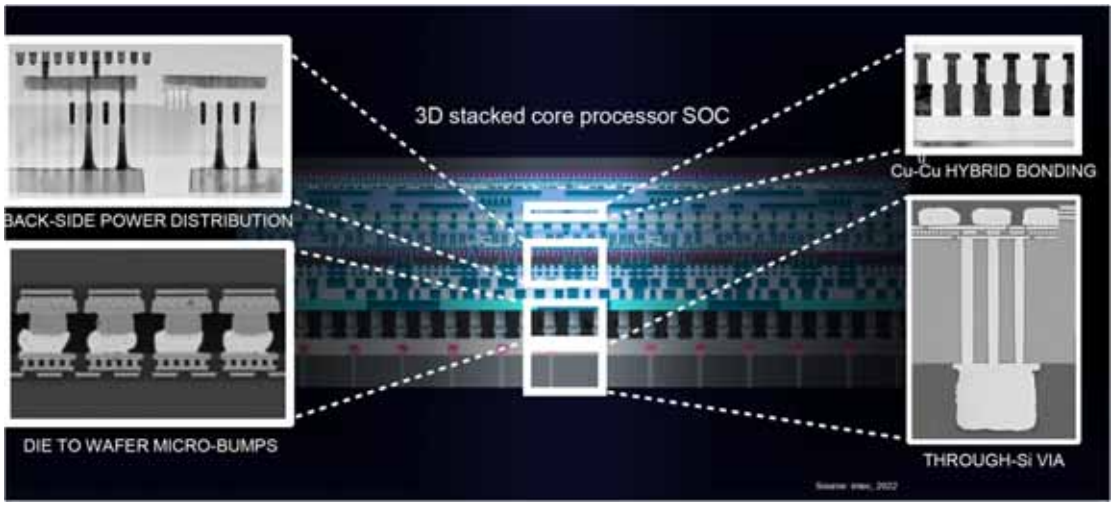
Imec: 3D Stacked ICs



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DoD Microelectronics Commons

https://nstxl.org/opportunity/microelectronics-me-commons/

Lab-to-Fab Transition of Microelectronics Technologies

Research Universities, Start-ups have facilities for Lab prototyping but face barriers to demonstrating manufacturability in a Fab.

Core Facilities or Foundries/Fabs provide access to early stage Fab prototyping.

Microelectronics Commons aims to enable lab-to-fab prototyping– evolve microelectronics laboratory prototyping to foundry/fab prototyping – in domestic facilities.

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www.slido.com Event Code: #meodc2022

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The Microelectronics Commons: Innovation from Lab-to-Fab

Innovation Barriers

- Lack of access to existing fabs for lab-to-fab prototyping
- High capital costs for process and metrology tooling to support manufacturing of microelectronics technologies
- High Intellectual Property (IP) and Electronic Design Automation (EDA) design license costs
- Lack of domestic access to chip carriers, and packaging materials to support integration of electronics
- Lack of workforce talent and expertise to support technology transition

End State

- **Sustained partnerships** between emerging technology sources, manufacturing facilities, and interagency partners
- **Rapid transition** of early-stage microelectronics research to proven technology in domestic foundries
- Expand **domestic** microelectronics fabrication capability
- Enhance microelectronics **education** to bolster the microelectronics engineering workforce
- Develop a **pipeline of talent** to bolster local semiconductor economies and grow the domestic semiconductor workforce

Democratize access to capabilities needed for lab-to-fab prototyping

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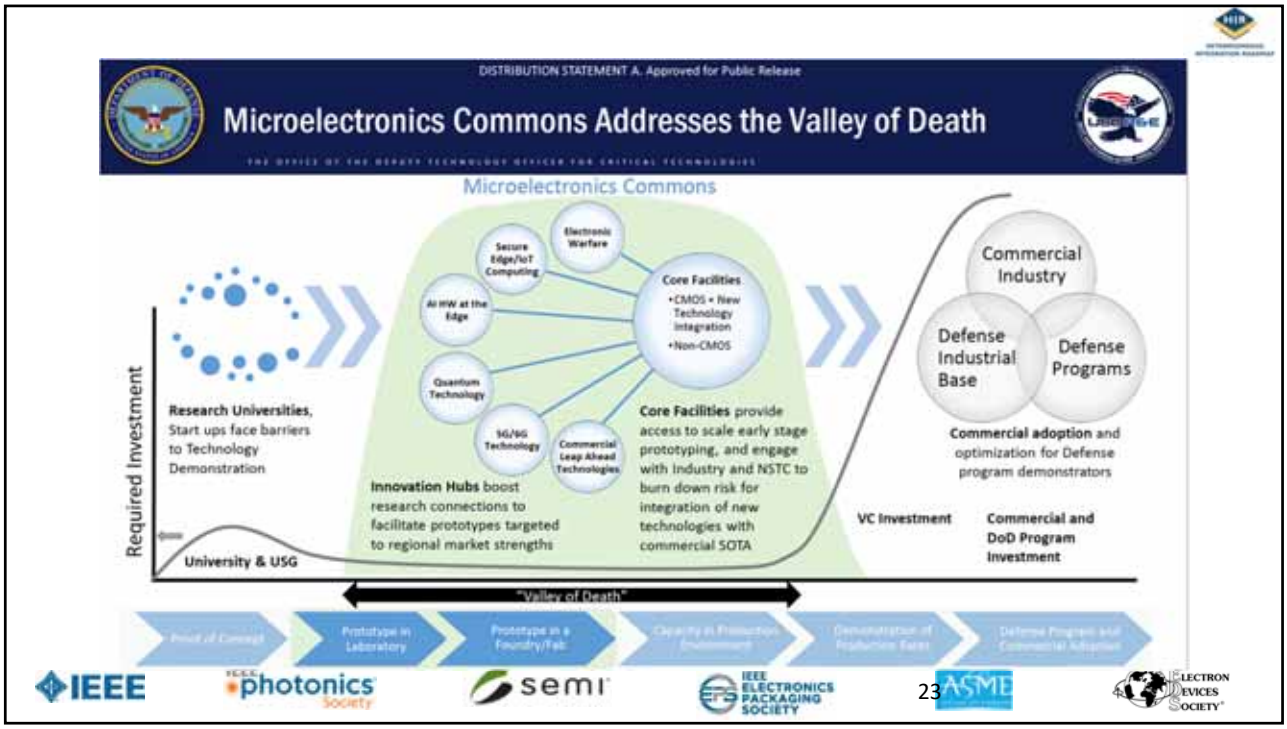


Comparison between DOC and DOC Programs

DOC Programs	DOD Microelectronic Commons
Support growth of domestic capacity, capability for US commercial market	Ensure that growth supports, and takes advantage of, national defense technologies
CHIPS for America R&D	**Regional Hubs**
• NSTC - Supports the future market for, leading edge, heterogeneous integration, non-CMOS • NAPMP – Supports the future market for heterogeneous integration, advanced packaging • Mfg USA, NIST Metrology - Support the industry with manufacturing solutions and characterization methods	• Distributed network of technology-focused hubs that build on regional strengths • Support prototyping, leverage unique capabilities • Guided by national defense needs, projects proposed by hubs foster the best solutions
Incentives	**Cores**
Expanded capability and capacity to support high TRL / MRL development • High-TRL prototyping • Pilot, manufacturing processes • Test and assembly	• Commercial fabs and foundries • Mid-TRL prototyping, pilot, test and assembly through Commons • High TRL production and commercialization for DIB, services & others

Shared resources, network access, coordination, and planning

CHIPS for AMERICA

OSD/Crane State-of-the-Art Heterogeneous Integration Packaging (SHIP), STEAM PIPE and STAMP

State-of-the-Art Heterogenous Integrated Packaging (SHIP) Program

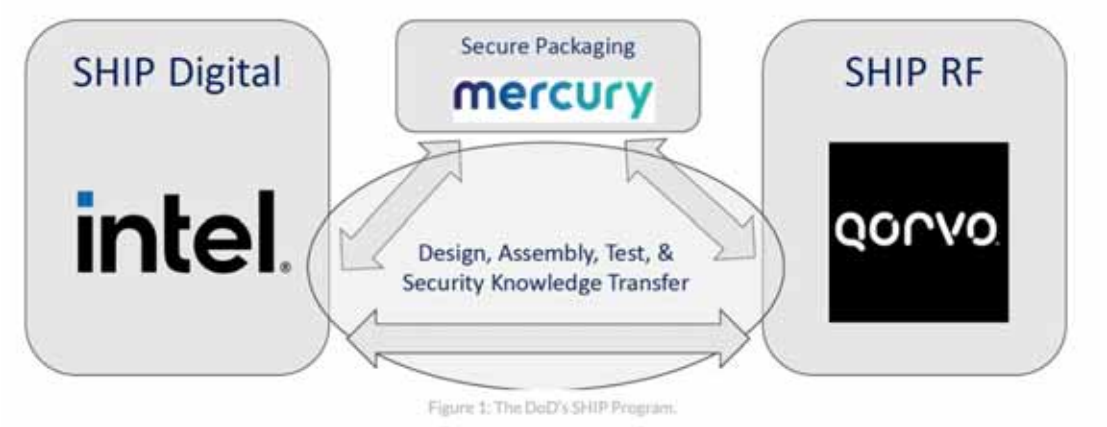


Figure 1: The DoD's SHIP Program.

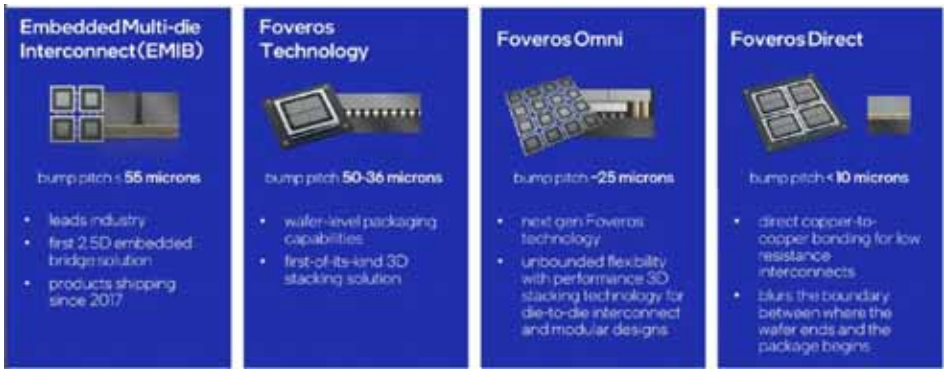
OSD SHIP Program (Dr. Darren Crum)

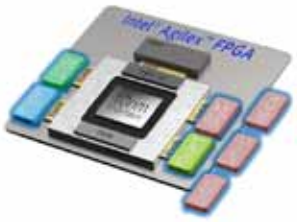
- SHIP Program Manager: Dr. Darren Crum
  - Develop an economically viable, SOTA heterogeneous integration and packaging capability for DoD system performance enhancement and assurance/security applications, which currently do not exist.
  - Provide sustainable, quantifiably assured SOTA advanced packaging access to the DoD and defense industrial base (DIB).
- The SHIP program specifically addresses both digital and RF packaging technologies through the program leads Intel and Qorvo, respectively.
- The key focus of the SHIP digital program includes:
  - Multichip packaging products utilizing Intel's commercial packaging, assembly, and test
  - Create a catalog of available designs, die, chiplets, package types etc.
  - Reuse and standardization
  - Creation of demonstrators that use the SOTA technology
  - **Adoption and use in military systems (transition the technology into actual products)**

The key focus of the SHIP Rf program led by Qorvo includes:

- Design, packaging, and assembly as an onshore service
- Reshoring mature manufacturing, assembly, and test such as the high-volume flip-chip capability
- Enable access to advanced Rf packages by providing a full suite of design tools, advanced packaging platforms, and a wide selection of materials choices
- **Allow DoD and DIB access to this commercial design flow through PDKs and ADK to design custom devices**

Intel – SHIP Digital (John Sotir)

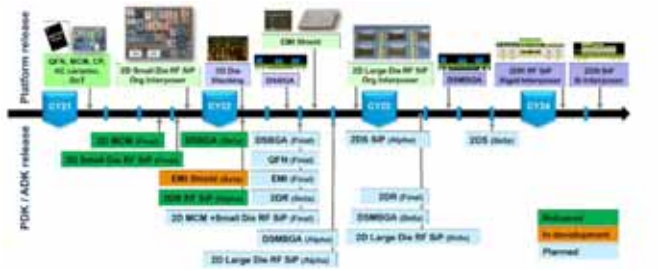




https://www.3dincites.com/2022/06/iftle-524-imaps-examines-the-dept-of-defense-ship-program/

Qorvo – SHIP RF (Ted Jones)

- The Qorvo ATC will be a US-based assembly and test factory offering access to SOTA manufacturing technologies at commercially competitive pricing. It will be based on Qorvo-proven commercial SOTA packaging technologies running at high volume manufacturing (HVM) rates offshore.



https://www.3dincites.com/2022/06/iftle-524-imaps-examines-the-dept-of-defense-ship-program/

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Stimulating Transition for Advanced Microelectronics Packaging (STAMP)

- Leveraging alignment to existing DoD Programs to transition the MCP technology to a program of record system. Advantages for military system developers and integrators include:
- Access to processing devices specifically designed in collaboration with DoD to meet DoD computing needs
- Access to next-generation at-the-edge sensor computing designed in collaboration DoD
- SOTA technologies will provide your systems with cutting-edge technology improvements – dramatically accelerating your technology roadmap of processing/computing devices with significantly reduced SWAP and increased performance

https://nstxl.org/opportunity/stimulating-transition-for-advanced-microelectronics-packaging-stamp/

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Stimulating Transition for Advanced Microelectronics Packaging (STAMP)

SHIP MCPs 1 and 2

Multi-chip package (MCP)

- MCPs 1 and 2 contain SOTA chiplets with advanced functionality, low power, smaller size, and cutting-edge performance along with Intel® Agilex™ advanced Field Programmable Gate Array (FPGA) technology
- The chiplets are Intel A-Tile Direct RF data converter tiles and Intel F-Tile advanced Serial/Deserial tiles
- These chiplets are connected to Intel® Agilex™ FPGAs with SOTA low power, low latency, Enhanced Multi-Die Interconnect Bridge (EMIB) parallel bus interconnect technology offered by Intel

MCP-1: Belmont Bay	MCP-2: Laguna Bay
Lead DIB Partner: BAE Systems **Use Case:** Small Form Factor EW System **Expected SWaP Savings:** 8x **Product Release:** Expected April 2023	**Lead DIB Partner:** Lockheed Martin **Use Case:** EW System **Expected SWaP Savings:** 8x **Product Release:** Expected December 2023

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https://nstxl.org/opportunity/stimulating-transition-for-advanced-microelectronics-packaging-stamp/

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Strategic Transition of Microelectronics to Accelerate Modernization by Prototyping and Innovating in the Packaging Ecosystem (STEAM PIPE)

Motivation

- Support the SHIP program goals to develop a US-based SOTA packaging capability for the DoD
- Enable system performance enhancement through the development of advanced prototypes and transition to military systems
- Emphasize transition strategy

Requirements

- Credible strategy to transition, including productization, qualification, and use
- Encouraged use of cost sharing and teaming
- Finalized third-party IP agreements, subcontracts, and purchase agreements according to originally proposed timeline
- Advanced packaging technologies and processes with a clear path to support DoD volume production

Current SHIP performer (Intel, Qorvo, Mercury) processes and products are not required.

STEAM PIPE can award prototypes with different product and process access models

Model 1	Model 2	Model 3
New devices and/or processes that will be made available across the DIB.	New capability of packaging technology or process made available to the DIB. Demonstrator devices may not be made available.	Devices that may be shared on a case-by-case basis with certain DIB members. If the prototype and process will not be shared with the entire DIB, a significant cost share is required.

https://nstxl.org/opportunity/strategic-transition-of-microelectronics-to-accelerate-modernization-by-prototyping-and-innovating-in-the-packaging-ecosystem-steampipe/

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https://www.3dincites.com/2023/02/iftle-548-tsmcs-off-shore-production-steam-pipe/

https://www.3dincites.com/2023/02/iftle-548-tsmcs-off-shore-production-steam-pipe/

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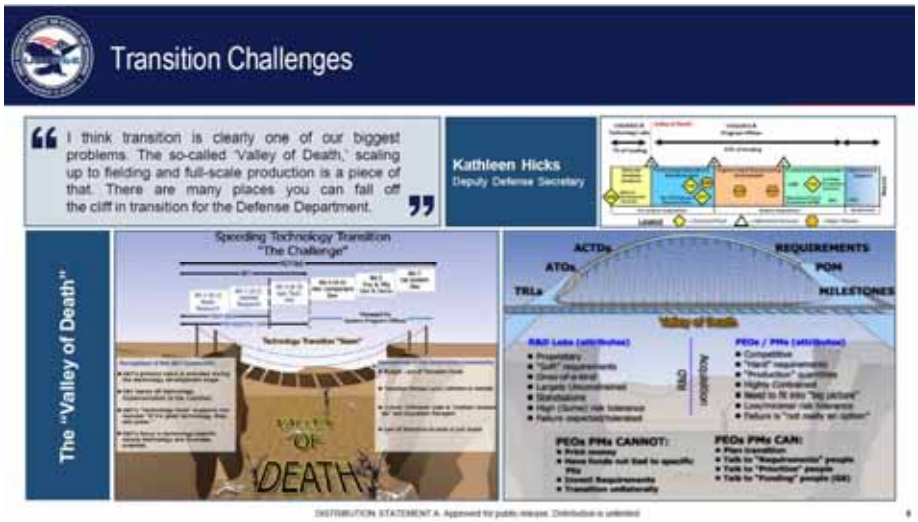
STAMP Objectives: Bridging the Technology Valley of Death



https://nstxl.org/opportunity/stimulating-transition-for-advanced-microelectronics-packaging-stamp/

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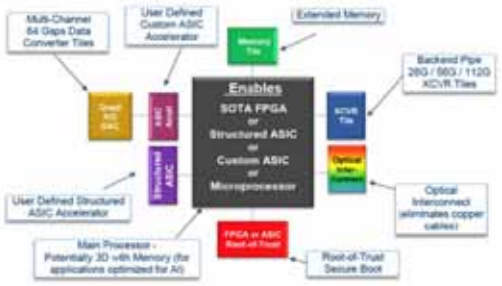
STEAM PIPE Intended Outcomes

Goals and Intended Outcomes

- New heterogeneously integrated packaged prototypes that achieve less power consumption and latency, reduced physical size, and improved system performance and reliability than current packaging methods.
- Address technology adoption risks and barriers resulting in follow-on Government sponsor funding.
- Unique and secure design tools and IP for multi-die heterogeneous integration of SOTA microelectronics.
- Strengthen the domestic advanced packaging ecosystem through the maturation of manufacturing processes and addition of SOTA devices.



Potential configurations for HI-enabled SOTA devices

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https://nstxl.org/opportunity/strategic-transition-of-microelectronics-to-accelerate-modernization-by-prototyping-and-innovating-in-the-packaging-ecosystem-steampipe/

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DARPA
MTO
High-performance, intelligent microsystems and next-generation components
C4ISR
Directed Energy
Electronic Warfare
PNT
Disruptive Microsystems
Local Processing
Microsystems Manufacture
Spectrum Dominance
35

DARPA
Microsystems Manufacture: Key challenges
Realizing heterogeneous 3D electronics
Optimizing design and test for complex circuits and prototypes
Overcoming security threats across the entire hardware lifecycle
Developing electronics for extreme environments
2D electronic interconnects limit throughput, functionality, miniaturization, and efficiency
Increasingly complex circuits and assembly stretch the limits of current design, packaging, and test capabilities
Persistent hardware threats limit the ability to access and utilize advanced electronics technology
Electronics performance and reliability are limited by extreme temperature, voltage, current, and radiation
https://www.darpa.mil/work-with-us/opportunities
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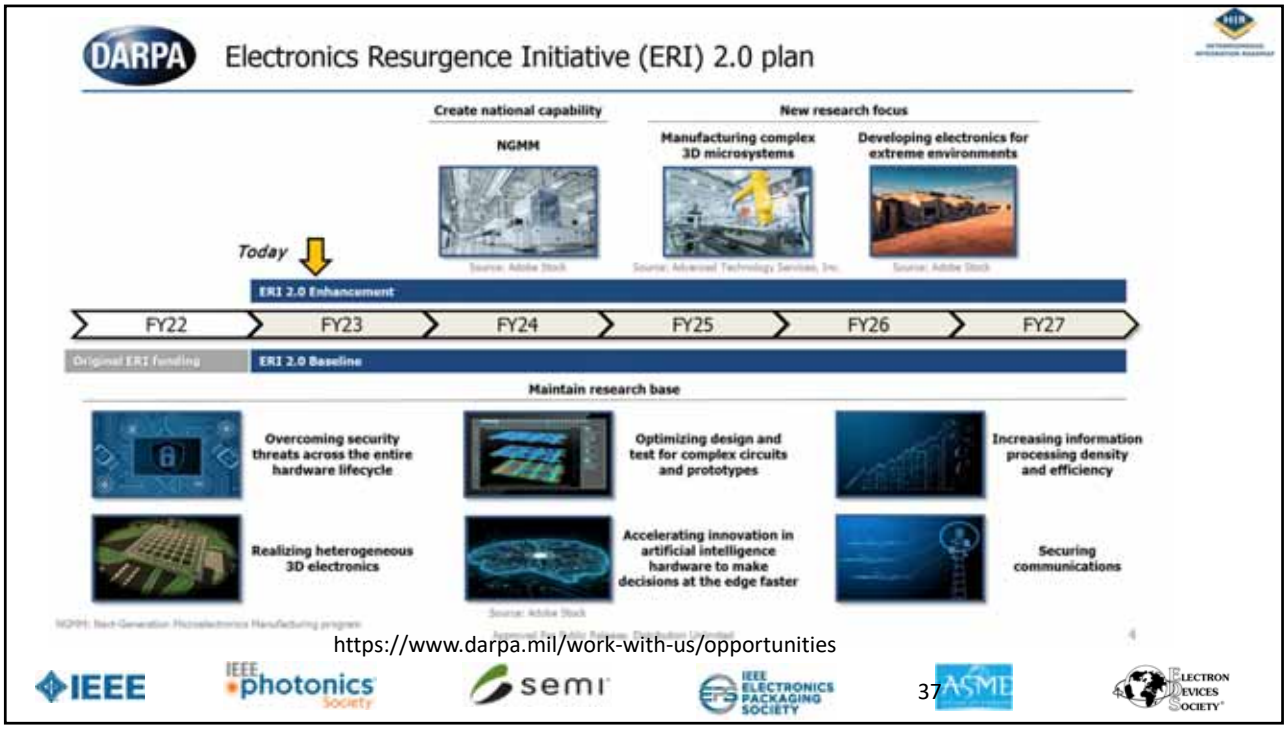

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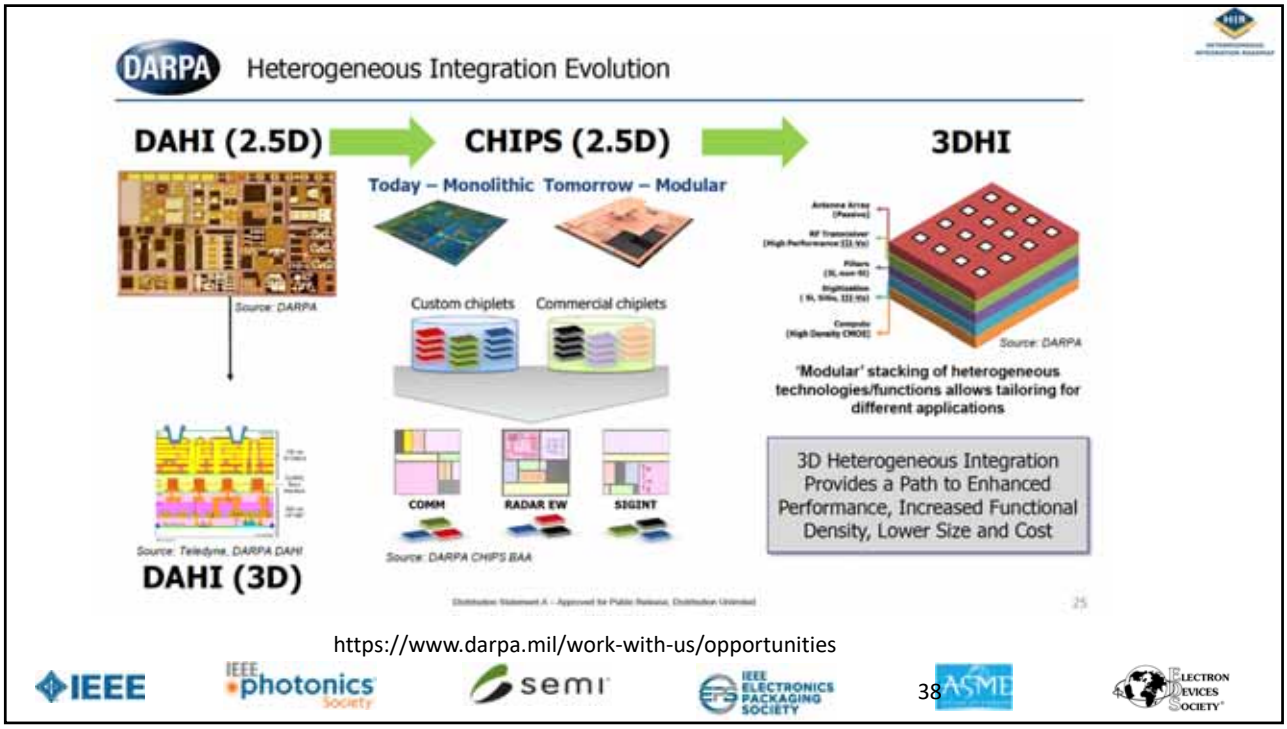

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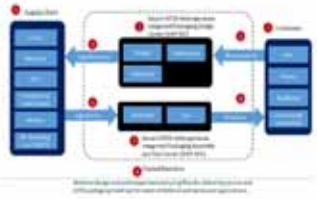
Can it be Manufactured

OSD SHIP (2.5D)



Source: OSD SHIP RFS

Sustainable, quantifiably assured SOTA advanced packaging for DoD and defense industrial base

NGMM (3D)
(Next Generation Microelectronics Manufacturing)

Manufacturing process

3DHI assembly design kit

National facility
3DHI R&D and low-volume manufacturing

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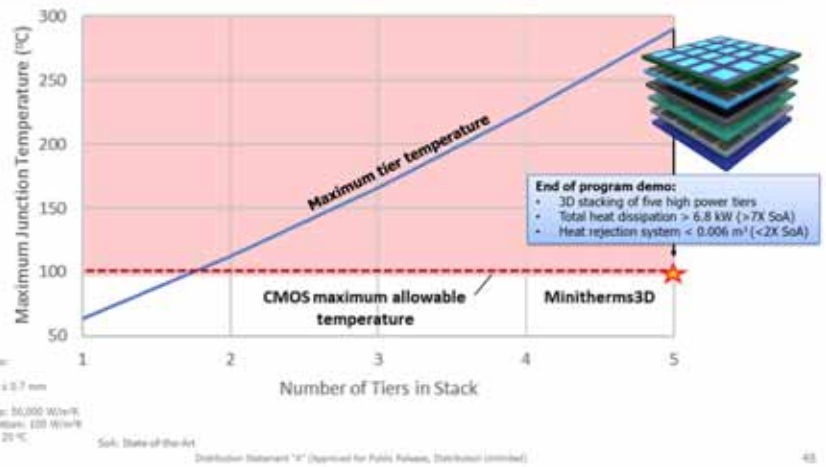
Minitherms3D Goal:
Compact thermal management to enable a scalable number of high power tiers



https://www.darpa.mil/work-with-us/opportunities

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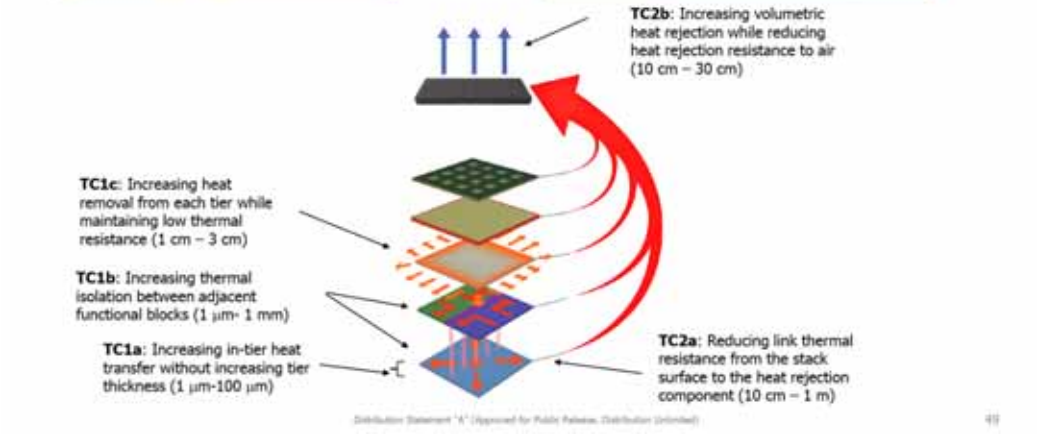
DARPA Technical challenges

MiniTherms3D Technical Challenges

TC1: Reducing thermal resistance within the 3D stack

TC2: Reducing thermal resistance outside the 3D stack



https://www.darpa.mil/work-with-us/opportunities

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Industrial Base Analysis and Sustainment Program (IBAS) RESHAPE is Onshoring Advanced Microelectronic Packaging

- Cornerstone OTA: CIR for Advanced Packaging known as RESHAPE (Reshore Ecosystem for Secure Heterogeneous Advanced Packaging Electronics)
- Foreign participation, access, transfers, and permit participation for this CIR are restricted and will be approved on a case-by-case basis, and only when in the best interest of the U.S. Government.
- Areas of Interest:
  - State-of-the-art (SOTA) wafer preparation techniques
  - copper-based silicon and III/V interposers
  - fan-out wafer-level packaging (FO-WLP)
  - silicon bridges
  - high-density build-up (HDBU) substrates
  - high-density interconnects (HDI)
  - assembly design kits (ADKs) for SOTA computer-aided design (CAD) tools

https://www.3dincites.com/2023/02/iftle-547-ibas-reshape-is-onshoring-advanced-microelectronic-packaging/?cn-reloaded=1

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Likely Semiconductor Hubs

- Arizona – Silicon Desert (Intel, NXP, TSMC, ASU, ACA)
- California – Silicon Valley (Intel, Nvidia, Skyworks, Maim, AMD, Stanford, Berkeley)
- Idaho - Silicon Spuds (Micron)
- Indiana and Ohio – Silicon Heartland (SkyWater, Intel, OSU, Purdue, Midwest Regional Hub)
- Minnesota – Silicon Prairie (Skywater)
- NY – Albany Corridor (GF, IBM, AIM)
- Oregon – Silicon Forest (Intel)
- Texas – Silicon Hills (MXP, TI, Samsung)
- Mid-Atlantic – (VA, PA, MD)

https://www.semi.org/en/blogs/semi/technology-and-trends/10-likely-locations-for-chips-act-innovation-hubs

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NDIA 3DHI Working Group

- Organized by NDIA Electronics Division, held 8 Feb 2023 at ASU
- Speakers: Darren Crum (Navy), Matt Walsh, (NSWC), Carl McKants (DARPA), SungKyu Lim (DARPA)
- Scope: Develop a Working Group to address 3DHI challenges
- Host: Professor Hongbin Yu, Arizona State University
- Themes:
  - Re-shoring of Microelectronics and Advanced Packaging Technologies and Capabilities
  - State-of-the-Art
  - Open Standards
  - Cornerstone RESHAPE

https://www.ndia.org/divisions/electronics/upcoming-events

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Next Steps

- Monitor on-going and new programs
  - CHIPS Act appropriations and NIST White Paper
  - National Advanced Packaging Manufacturing Program
  - DoD / OSD
  - DARPA
  - EU CHIPS Act
- Expand coverage for other activities
  - Bring HIR members into discussion for their perspectives
  - MAPT Roadmap
    - https://www.src.org/about/nist-mapt-roadmap/
  - UCLA/SEMI Roadmap
    - https://samueli.ucla.edu/ucla-chips-and-semi-win-300k-in-nist-funding-to-create-heterogeneous-integration-roadmap/
  - EU CHIPS Act
    - https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

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Thank You!

https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html