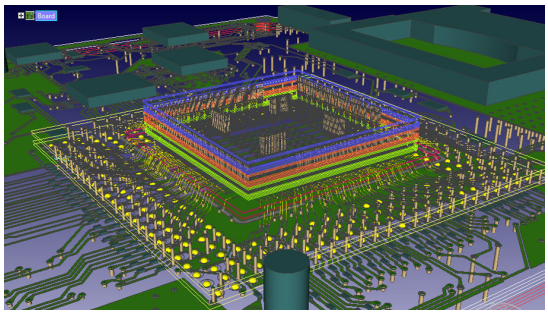
Co-Design for Heterogeneous Integration

Jose Schutt-Aine

Co-Chair: Chris Bailey

Co-Design for HI

- Focus on minimizing energy and delay
- Identify and address conflicting requirements,
- Take advantage of novel interconnect technologies
- Leverage from AI methodologies
- Address design and computational complexity



Courtesy of Zuken

Research Needs

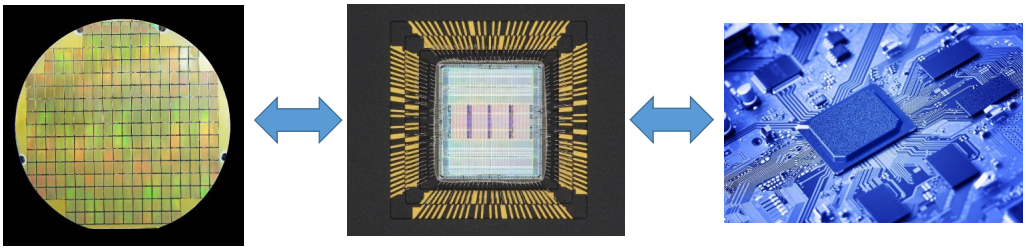
HETEROGENEOUS INTEGRATION ROADMAP

- **Co-Design for HI Challenges**
  - Chiplet-based design
  - Interconnection schemes, D2D Interfaces
  - Brain-inspired architecture
  - Multiphysics modeling and simulation
  - AI/ML design approach

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | IEEE ELECTRON DEVICES SOCIETY

Traditional Co-Design

HETEROGENEOUS INTEGRATION ROADMAP



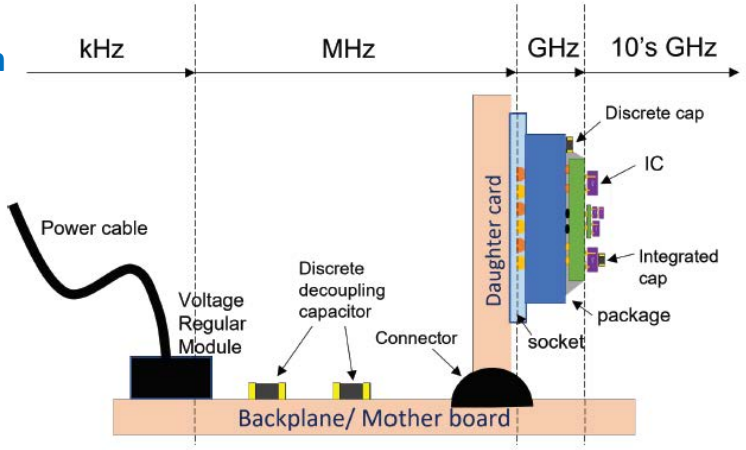
CHIP	PACKAGE	BOARD
- Transistors	- Interconnects	- Transmission lines, sensors
- Nonlinear	- Linear	- Linear+Nonlinear
- SPICE	- EM Tools	- EM Extraction, SPICE, IBIS,…
- Scaling with tech	- Scaling with λ	- Scaling with λ

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | IEEE ELECTRON DEVICES SOCIETY

4/20

Chiplets and HI

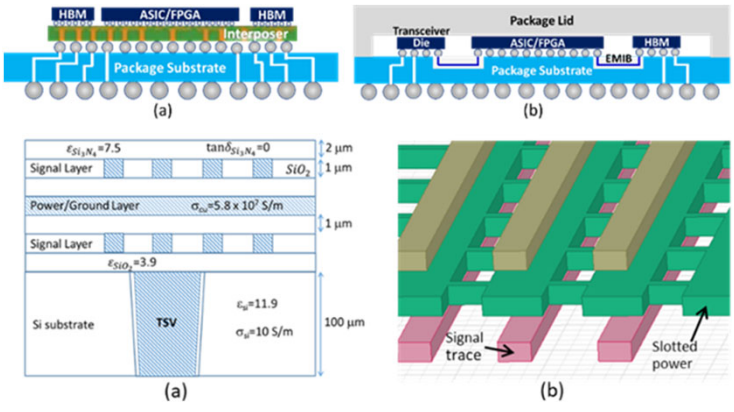
- **Multilevel Power Distribution**
  - Chiplets advantageous
  - Boundary between chip and package is blurred
  - Concurrent design is necessity
  - SI/PI, multilevel frequencies
  - System-level verification challenging



5/20

HI – The Interconnect Challenge

"There are many solutions and techniques for improving transistors; options for improving interconnects are very few…"



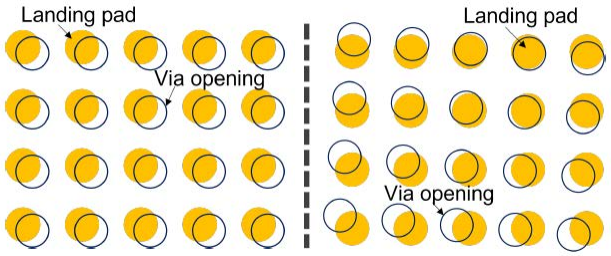
Challenges

- Signal/power integrity
- Thermal effects
- IR Drop
- Power dissipation
- High I/O count
- Reliability
- Security
- Environment
- Architecture

Chiplet-Based Assembly - Uncertainty

HETEROGENEOUS INTEGRATION ROADMAP

- SI/PI Under Uncertainty
  - Dice shifted and rotated
  - Can be tolerated to increase yield
  - Misalignment can cause failure
  - Multiphysics modeling and simulation
  - Random and stochastic



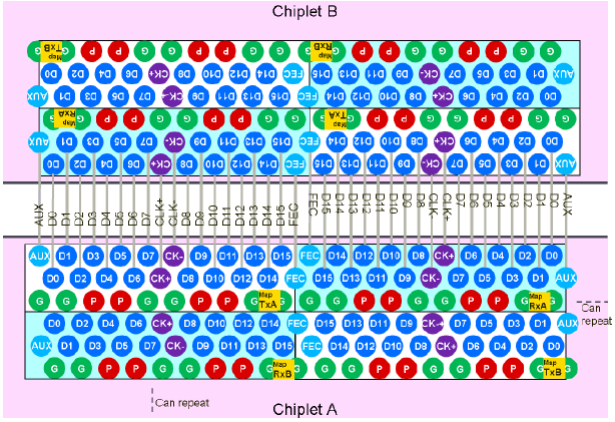
IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

7/20

I/O Channel Design

HETEROGENEOUS INTEGRATION ROADMAP

- D2D Interfaces
  - Bunch of Wires (BoW)
  - Universal Chiplet Interconnect Express (UCIe)
  - Initial specifications released
  - Development still under way
  - Focus on best practices for SI/PI



BOW Slice – Source: [1]

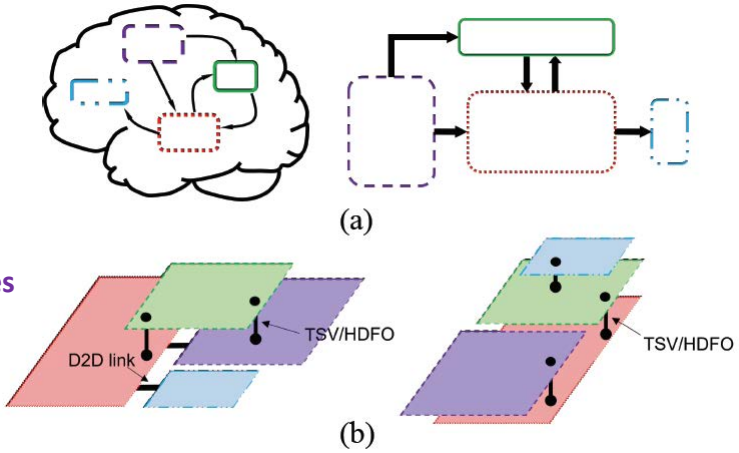
[1] Shahab Ardalan, Ramin Farjadrad,Mark Kuemerle,Ken Poulton,Suresh Subramaniam, Bapiraju Vinnakota, "Chiplet Communication Link: Bunch of Wires (BoW)", IEEE Micro, Jan/Feb 2021

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

Brain-Inspired Computing

HETEROGENEOUS INTEGRATION ROADMAP

- New Architecture
  - Near/In-memory computing
  - Architectural motifs
  - Breakup functional circuits into tiles
  - Speed and energy advantages



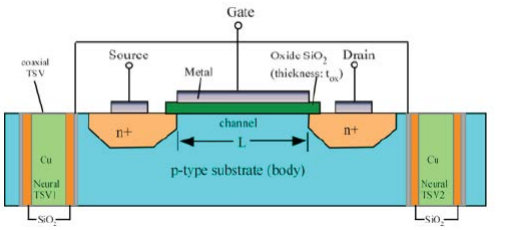
IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

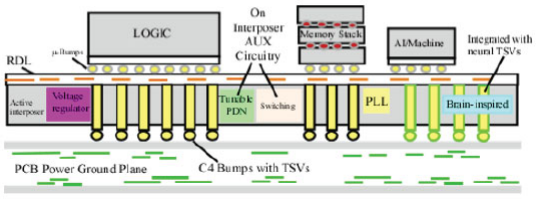
9/20

Intelligent/Active Interposers

HETEROGENEOUS INTEGRATION ROADMAP

- Components
  - Neural TSVs
  - Neuroprimitives
  - Smart materials
  - Reconfigurable devices
- Viable Platforms for
  - Tunable PDN
  - HI of logic, memory
  - PLL, equalizers





IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

10/20

Multi-Physics Co-Design

HETEROGENEOUS INTEGRATION ROADMAP

Enablers
- TSV
- Interposers
- BGA
- EMIB
- Chiplets

Architecture
- Logic
- Memory
- Analog
- RF

Driver/Application
- Multicore
- Accelerators

Constraints
- Bandwidth
- Thermal
- Power
- Signal Integrity
- I/O
- Security
- Reliability
- Environment

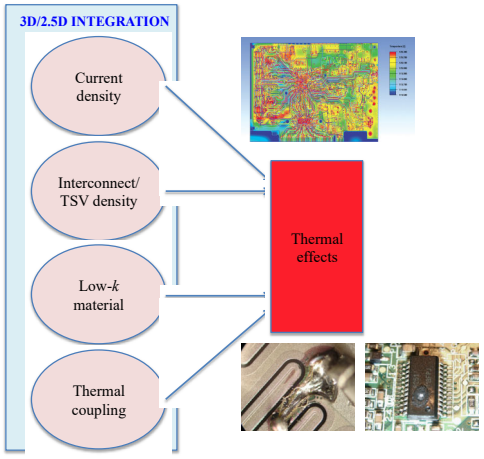
Design Optimizer
- 3D Design Flow
- Multiphysics Algorithms
- Multidomain Algorithms
- Interface/Integrator

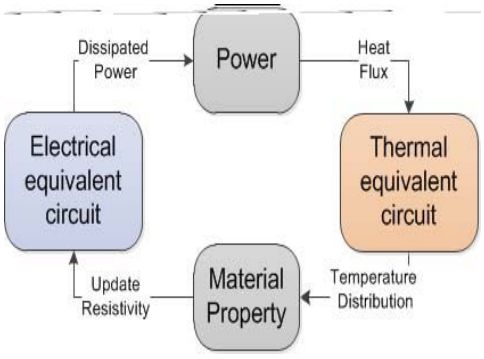
IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

11/20

Thermal-Aware Co-Design

HETEROGENEOUS INTEGRATION ROADMAP

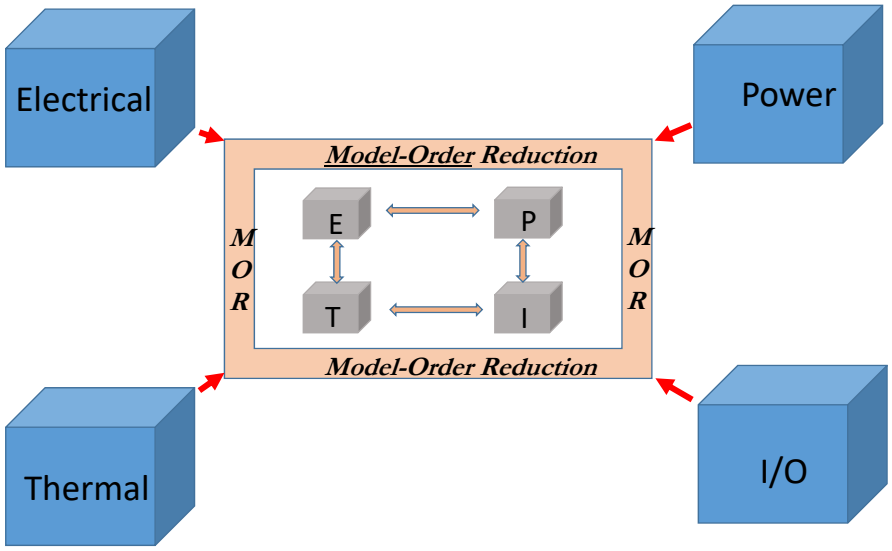




IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

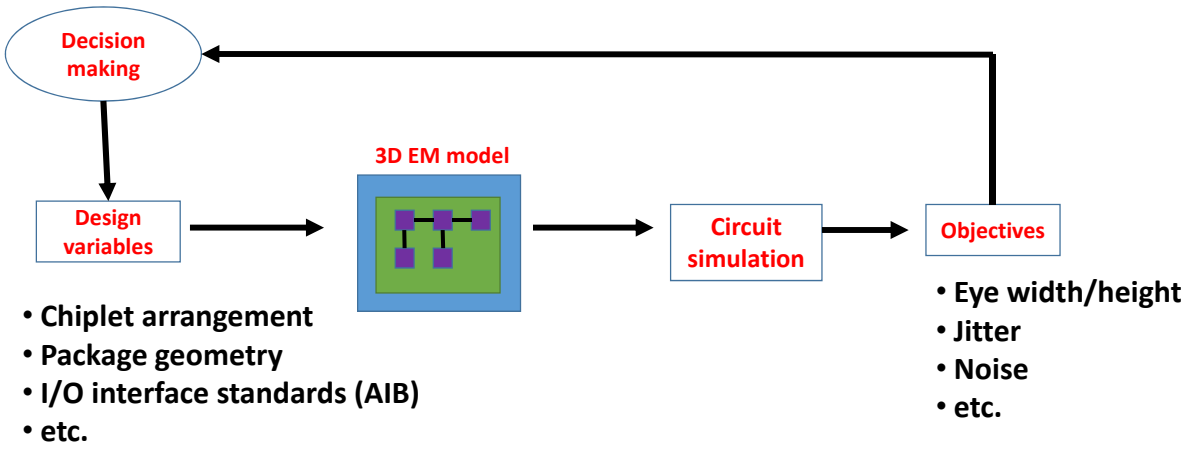
12/20

Multiphysics & MOR



13/20

AI/ML for System-Level



- Chiplet arrangement
- Package geometry
- I/O interface standards (AIB)
- etc.

- Eye width/height
- Jitter
- Noise
- etc.

14/20

Conclusions

HETEROGENEOUS INTEGRATION ROADMAP

- Chiplet PDN - Higher level of complexity
- Can only be resolved by Co-design
- Novel technologies will enable inception
- Make use of AI and ML techniques
- Will help achieve performance
- Faster time-to-market

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

15/20