




HIR Test Chapter




Dave Armstrong



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Ken Butler




- Co-chaired for many years by Dave Armstrong and Ken Lanier
 - Many thanks to Dave and Ken for their leadership, big shoes to fill
- Last year passed responsibilities to George Hurtarte (Teradyne, Lam) and Ken Butler (TI, Advantest)






HIR
HETEROGENEOUS
INTEGRATION ROADMAP

Sections and Leaders

Section	Leader(s)
Executive summary	Ken Butler, George Hurtarte
RF Test	George Hurtarte
Photonics	Dave Armstrong
Logic Test	Marc Hutner
Specialty Test	Wendy Chen
Memory Test	Jerry McBride
Analog	Rich Dumene
Probe, handlers	TBD
System level test	Harry Chen
Data analytics	Ira Leventhal
2.5D/3D Test	Morten Jensen, Boris Vaisband
Test cost	Ken Lanier









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2023 HIR Test Chapter Update

- Cross-cut topic with many overlaps with the rest of HIR
- Test chapter leadership team met monthly in 2022
- Full update on test chapter wrapping up now
- Multiple new section leaders, 110+ contributors, thank you!
- 2023 revision aimed at focusing on test trends and needs - less on providing extensive market context commentaries.



HIR
HETEROGENEOUS
INTEGRATION ROADMAP

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Executive Summary and Scope

The 2023 revision of the HIR test chapter aimed at focusing on test trends resulting from semiconductor market and technologies inflection points and emerging use cases, and less on providing extensive market context commentaries.

Sections Updated in 2023 Revision

Below we provide a high-level summary of the key test challenges and needs for each of the device types addressed in the test sections that were updated in this 2023 test chapter revision.

RF Test: Need 1) Non-frequency-gapped ATE RF test capability in the 0-100 GHz frequency, either for characterization, quality assurance, and/or high-volume production testing; 2) Higher ATE RF bandwidth production test capability up to 400 MHz for Wi-Fi 7 (with EVM in the 48+ dB range) and satellite; and up to 2 GHz to support 5G mmWave, UWB, and 6G THz; and 3) High-volume over-the-air (OTA) handler-based testing for mmWave and THz, and possibly automotive radar, will become increasingly relevant as DIB cabling for increased site count becomes cost-prohibitive.

Photonics Test: Need 1) novel test approaches for testing optics in co-packaged heterogeneous devices in high volume; and 2) Emphasis on test time containment and test time reduction as the number of lanes and wavelengths per fiber increase.

Logic Test: 1) Need new test methods for testing chiplet devices with mixed technologies (for example, need for retargetable test IP for next level of integration into SIP or system); and 2) test methodologies using Silent Data Corruption (SDC) logic testing methods.

Specialty Test: Need 1) higher test parallelism to reduce cost of test; and 2) multi-functional and cost-effective test capabilities as specialty devices become part of heterogeneous packages.

Memory Test: 1) Need test capabilities for addressing higher interface speed, power, and thermal management requirements; 2) Test capabilities for overcoming the challenges of electro-mechanical interface capability of wafer and component test as NAND memory density increases due to vertical scaling; and 3) Testing of higher DRAM bandwidth requirements.

Analog/Mixed Signal Test: Need 1) High speed instrumentation that can accept, force, and tolerate higher voltages and currents, driven by wide bandgap materials; 2) DC accuracy below 50 uV over the entire temperature range; 3) Closed-loop temperature forcing test capability at final test; 4) Test capabilities for AMS devices housed in heterogeneous packages; 5) Novel test solutions for overcoming the inherent physics of high voltage test at very high multistate testing; 6) High density floating resources with high accuracy, medium current capability, and large isolation voltages; and 7) Need for fully floating low-speed digital instrumentation for testing chip-to-chip communications devices which are shifted by tens to hundreds of volts above or below system ground.

System Level Test: Need 1) Flexible DFT architectures for both structural and functional test content; 2) Effective SW/HW system failure diagnosis methods; and 3) Deep component parametric data extraction to Data Analytics.

Data Analytics: 1) Need for advanced and comprehensive data analytics solutions that take full advantage of data from across the entire value chain; 2) Significant improvements in the development and adoption of key enablers such as communications infrastructure, data interchange formats, traceability, data


security, and advanced data analytics algorithms; 3) Need efficient methods for accessing, curating, managing, and analyzing data from on-chip sensors IP, equipment sensors, and test results.

2.5D/3D Test: Need 1) known-good-die DFT test methods that enable high quality wafer probe test – thus reducing fallout at final test; 2) Faster die-to-die communication standards that enable thorough testing at final test; 3) Standardized test and repair methodologies that considers new trends in 3D interconnects; 4) Yield prediction and analysis methods that ensure fallout at all levels of testing are understood; and 5) End-to-End data analytics capability that applies to all dies on the package.







Test Cost: 1) Need new probing technology which allows testing of singulated die; 2) Need new PCB and interposer technology to lower the cost and complexity of consumable material; 3) Need improvements in the test process by increased use of data analysis and machine learning based on measured data; and 4) Cost reduction of system-level testing.

Test Technology Working Group, Heterogeneous Integration Roadmap Leadership Team

Co-Chairs:	Ken Butler George Hurtarte		
RF Test:	George Hurtarte	Analog/Mixed Signal Test:	Rich Dumene
Photonics Test:	Dave Armstrong	System Level Test:	Harry Chen
Logic Test:	Marc Hutter	Data Analytics:	Ira Leventhal
Specialty Test:	Wendy Chen	Test Cost:	Ken Lanier
Memory Test:	Jerry McBride		
2.5D/3D Test:	Morten Jensen and Boris Vaisband		




2023 Test Chapter Edition Executive Summary














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HIR Test: A Few Examples of Key Needs and Trends

- Need: High-volume over-the-air (OTA) handler-based testing for mmWave and THz
- Need: Known Good Die (KGD) design for test for 2.5D/3D enabling high quality wafer probe
- Need: Probe technology for testing singulated die
- Need Efficient methods for accessing, curating, managing, and analyzing data from on-chip sensors IP, equipment sensors, and test results
- Trend: Increases in photonic lane counts, frequencies – need to contain test cost
- Need: Test methods for chiplet-based designs with mixed technologies



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How can we encourage more working collaboration between HIR chapters?

For example, across-chapters leadership quarterly meetings
(not just once per year)

