Heterogeneous Integration Roadmap Workshop

Heterogeneous Integration Roadmap
Thermal Technical Working Group (TWG)

Presented by
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On behalf of the Thermal TWG
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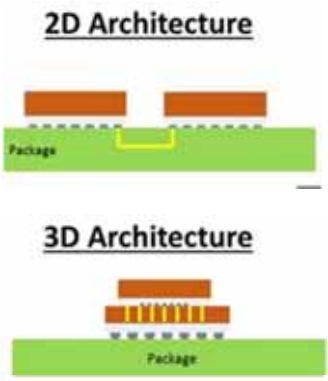


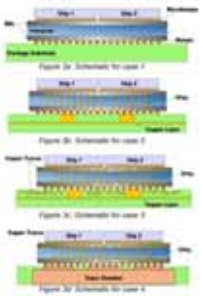
IEEE HIR Thermal Chapter

Thermal TWG will consider three areas:
- (a) Die level.
- (b) Package integration/SIP/module Level.
- (c) System Level (limited to board level).

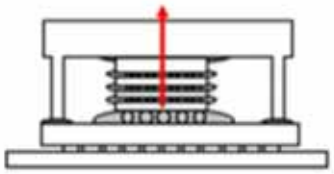
Thermal TWG will focus on articulating the following in quantitative and qualitative terms:
- (i) Canonical problems with thermal challenges;
- (ii) Cooling limits for known solutions;
- (iii) Advanced concepts and research.

Years 1-3 (2019-2021)
- Thermal effort kicked off in 2018.
- ~50 industry & university experts
- 2019-2022 chapters published
- Past focus
  - Canonical industry problems
  - Research advances

2022 focus
- Quantum Computing cooling
- Advanced thermal modeling
- Immersion cooling
- Stacked die thermal enhancements
- Back side power delivery
- Transient thermals in die
- Silicon micro-channels mfg
- Summary of world's top supercomputer cooling

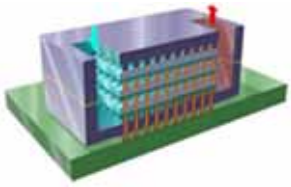


1. 2D chip with stacked memory on a silicon/glass interposer

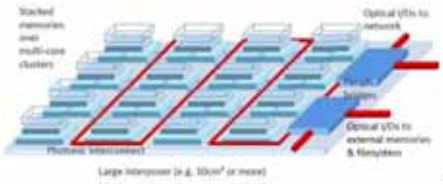


2. 3D stacked die with conduction interfaces

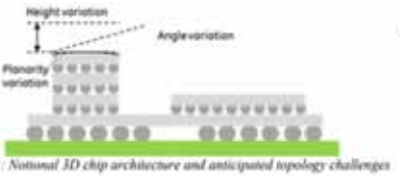
Canonical Thermal Heterogeneous Integration Problems



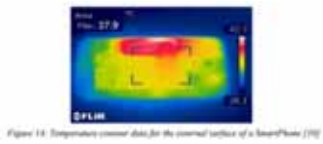
3. 3D stacked die with embedded liquid cooling



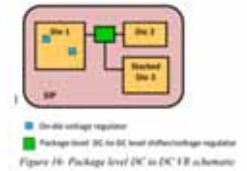
4. Optics/photonics based Heterogeneous package



5. Harsh environment (military, aerospace, automobile)

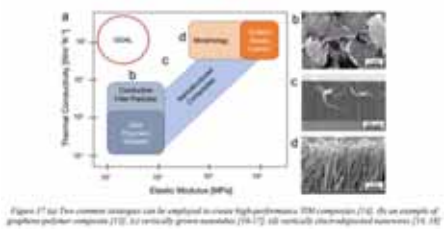


6. Mobile application chipset (package on package, fan out, bridge)



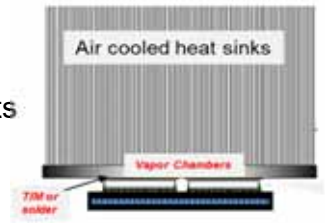
7. Voltage Regulators in a Heterogenous Package

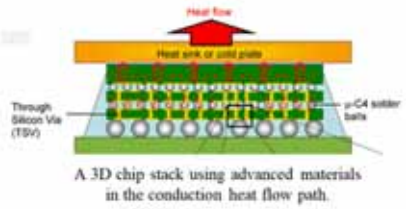
Advanced Thermal Technologies & Research



[A] Thermal Interface Materials

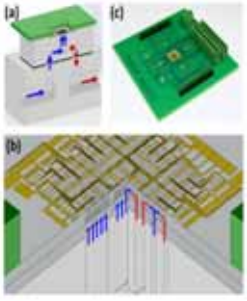
[B] System thermal limits for HPC multi-chip modules





A 3D chip stack using advanced materials in the conduction heat flow path.

[D] Advanced Thermal Materials for Thermal Management



[C] Embedded liquid cooling of chip and chip stacks

[E] Thermomechanical Modeling for Heterogeneous Integration

2023 and beyond, TWG continuing to work on

Htsyxsszj%yt%fiiwjxx%ymj%canonical problems with thermal challenges, cooling limits for known solutions; and advanced concepts and research

Linkage: Quantum computing, 3D IC, IVR (Integrated power electronics)

Explore the future collaborations with other TWGs. Please reach out us if your group have specific needs on the thermal investigation. Happy to collaborate.

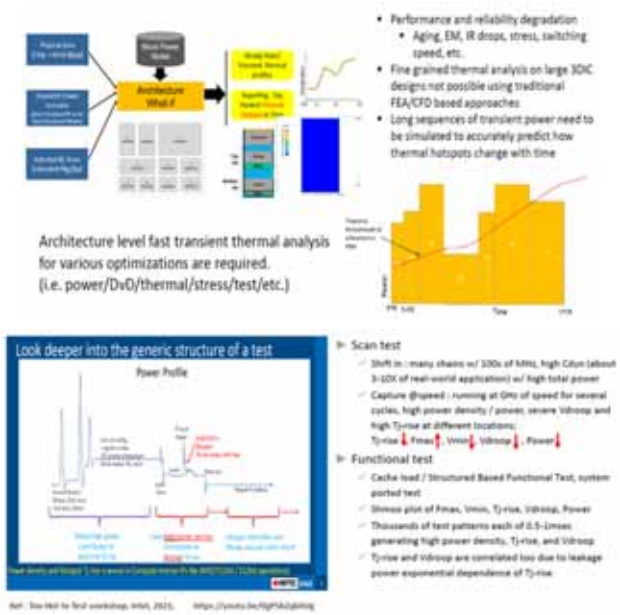
New additions in 2022 Chapter (published)

- Emerging challenges and opportunities on thermal modeling for advanced 3D IC system
- Challenges and characterization of hotspots modeling
- Thermal modeling on the High Bandwidth Memory (HBM)
- Thermal challenges related to the integrated voltage regulators (IVR)
- Advanced Liquid Cooling for next Generation data center integrated circuits
- Innovative method for manufacturing silicon microchannel

Select topics to present

- **Emerging challenges and opportunities on thermal modeling for advanced 3D IC system**
- Challenges and characterization of hotspots modeling
- **Thermal modeling on the High Bandwidth Memory (HBM)**
- Thermal challenges related to the integrated voltage regulators (IVR)
- **Advanced Liquid Cooling for next Generation data center integrated circuits**
- **Innovative method for manufacturing silicon microchannel**

Emerging challenges and opportunities on thermal modeling and simulation for advanced 3DIC system



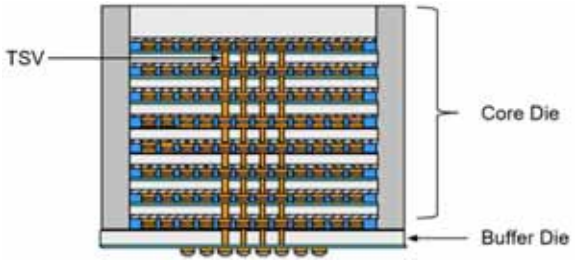
Challenges and opportunities on thermal modeling and simulation for advanced 3DIC systems:

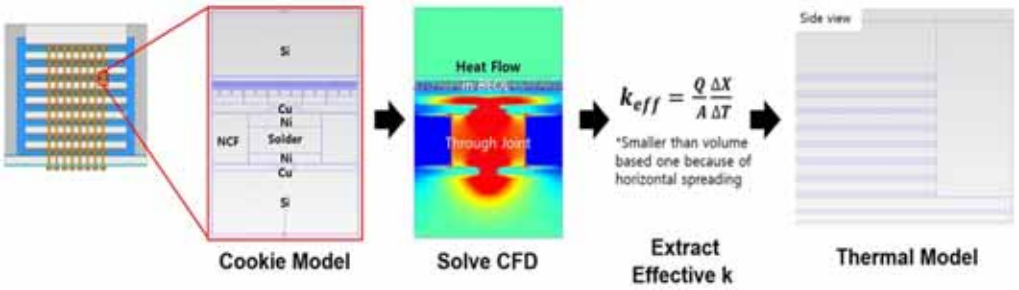
- Performing fine-grained static and transient thermal analysis on large 3DIC designs is required and demand adaptive meshing or machine-learning technology to overcome the limitation using traditional CFD/FEA based solvers.
- Architecture-level thermal and thermal-induced stress analysis are required due to the thermal coupling from cross-die horizontally and vertically with transient-based power profile among chiplets in 3DIC.
- Heterogeneous Integration 3DICs may consist of analog/mixed-signal and digital designs which have very different thermal and stress requirements that need to be co-optimized among chiplets and package in 3DIC.
- For Silicon Photonics 3DICs, accurate thermal gradient analysis is required for the co-optimization of 3DIC package and required thermal heater for PIC design.
- Testing of large 3DIC consisting of CPU/GPUs, etc. presents a major challenge due to multiple localized thermal hotspots and dynamic voltage drop affecting yield. Co-optimization of test techniques and localized thermal hotspots and Vdroop on 3DIC should be considered.

Thermal modeling on the High Bandwidth Memory (HBM)

HBMs have thermal challenges due to the large stack thermal resistance and thermal coupling from adjacent higher power logic dies.

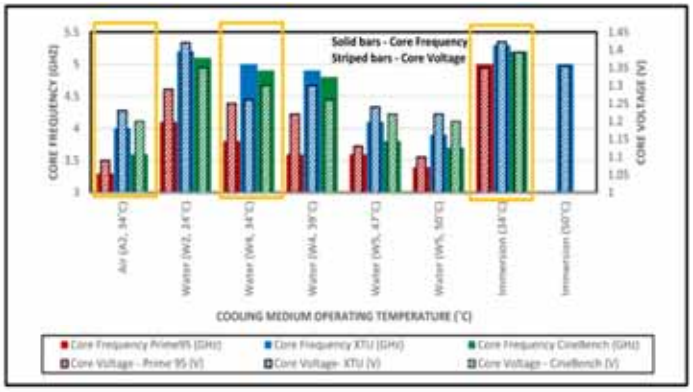
HBM is also not easy to simulate and provide accurate temperature predictions due to its complicated stacking structure.

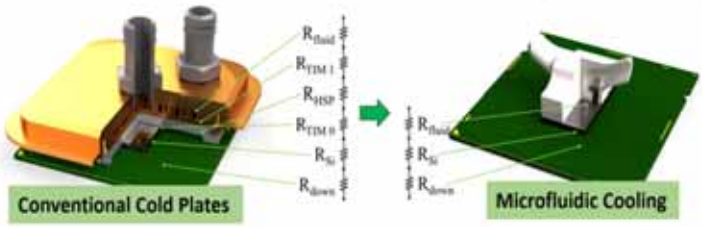




Advanced Liquid Cooling for next Generation data center integrated circuits

When it comes to cooling high density electronic devices including CPUs, GPUs, and FPGAs employed in a data center (DC) server HW infrastructure, two phase (2P) immersion cooling using boiler plates (aka evaporators) and direct contact liquid Cooling using cold plates (aka water cooled microchannel heat sinks) outperform traditional air-cooling techniques.

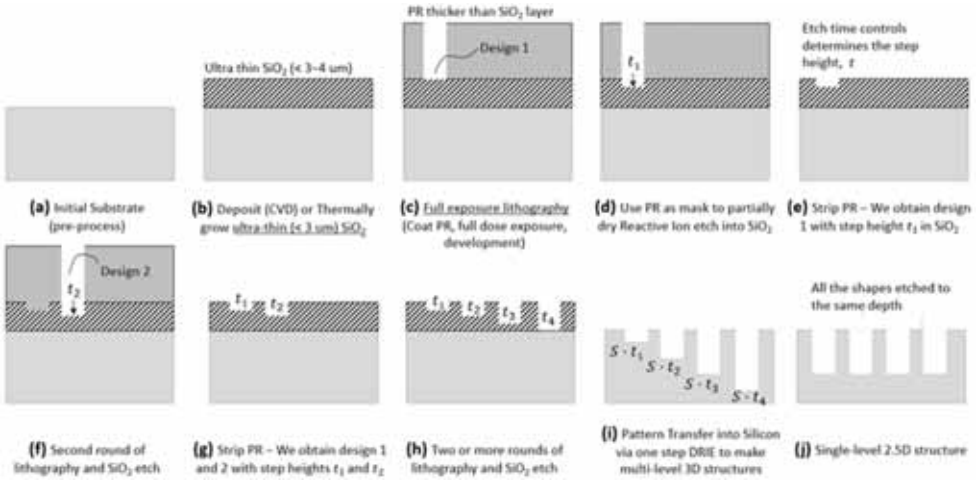




Demonstrated up to *44.4% reduction in junction-to-inlet thermal resistance* while using only *0.3× of volumetric coolant flow per Watt* of power dissipated in the CPU compared to a conventional cold-plate.

Manufacturing innovative method for the silicon microchannel cooling technology

Cold plate requires 10um to 500-600um depth channel, the traditional etching method creates challenges to make multi-depth, hierarchical, 3D structures in the substrate of height more than a few microns, and also PR spinging on larger step heights (more than 5-10um) lead to unsatisfactory coating.



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