Heterogeneous Integration Roadmap Workshop

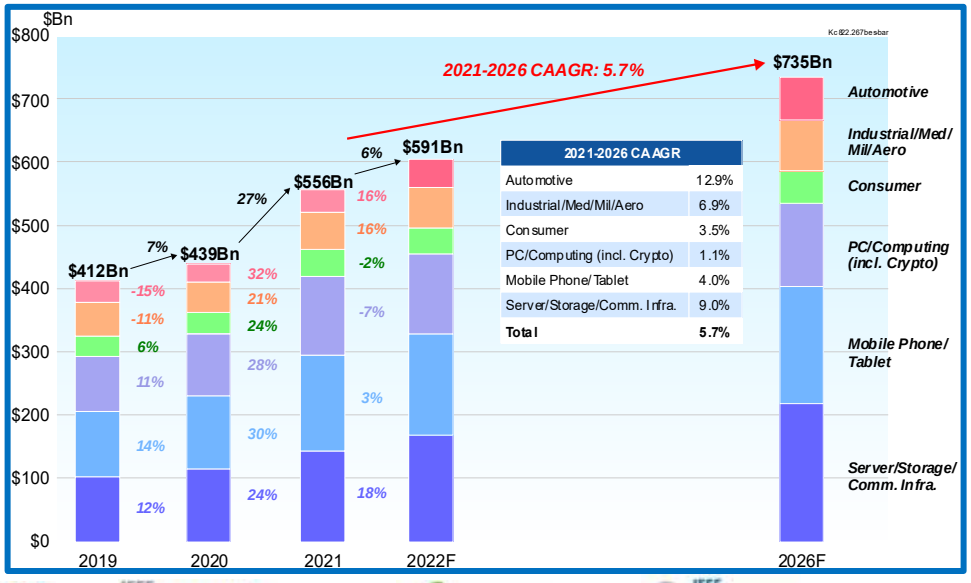
MobileTWG

TWG Chair & Co-Chair
William (Bill) Chen & Benson Chan

Agenda

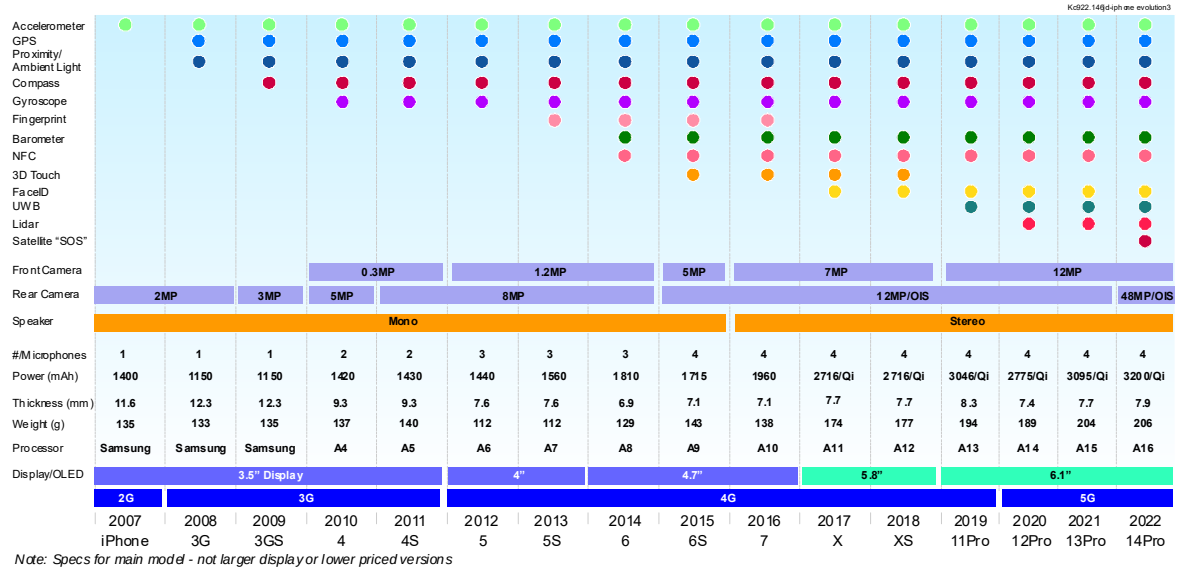
- Mobile is essential tool for consumers for daily lives
- Smart Phone growth in capabilities & features
- 5G mmWave a technology disruption
- Battery
- Collaboration across Technical Working Groups
- Summary

Electronics Industry Forecast is Bright



2021-2026 CAAGR	
Automotive	12.9%
Industrial/Med/Mil/Aero	6.9%
Consumer	3.5%
PC/Computing (incl. Crypto)	1.1%
Mobile Phone/Tablet	4.0%
Server/Storage/Comm. Infra.	9.0%
Total	**5.7%**

APPLE IPHONE EVOLUTION



	2007 iPhone	2008 3G	2009 3GS	2010 4	2011 4S	2012 5	2013 5S	2014 6	2015 6S	2016 7	2017 X	2018 XS	2019 11Pro	2020 12Pro	2021 13Pro	2022 14Pro
Front Camera				0.3MP		1.2MP			5MP	7MP			12MP			
Rear Camera	2MP		3MP	5MP		8MP			12MP/OIS							48MP/OIS
Speaker	Mono									Stereo						
#/Microphones	1	1	1	2	2	3	3	3	4	4	4	4	4	4	4	4
Power (mAh)	1400	1150	1150	1420	1430	1440	1560	1810	1715	1960	2716/Qi	2716/Qi	3046/Qi	2775/Qi	3095/Qi	3200/Qi
Thickness (mm)	11.6	12.3	12.3	9.3	9.3	7.6	7.6	6.9	7.1	7.1	7.7	7.7	8.3	7.4	7.7	7.9
Weight (g)	135	133	135	137	140	112	112	129	143	138	174	177	194	189	204	206
Processor	Samsung	Samsung	Samsung	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16
Display/OLED	3.5" Display					4"		4.7"			5.8"		6.1"			

Note: Specs for main model - not larger display or lower priced versions

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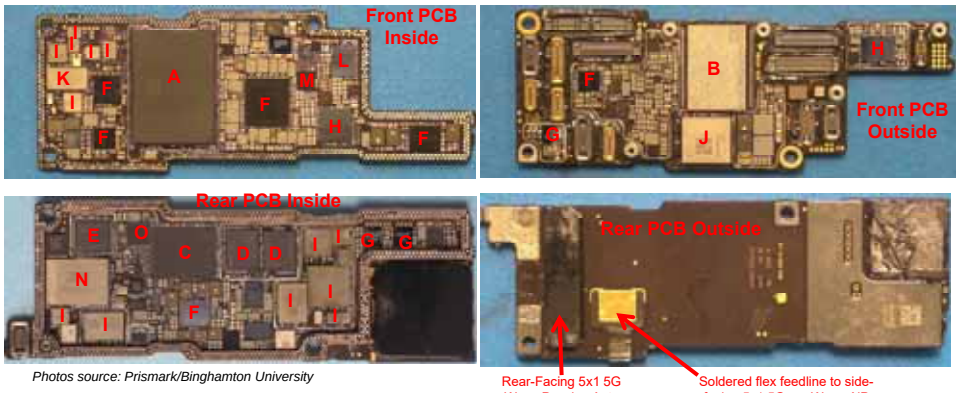
APPLE IPHONE 14 PRO MAIN BOARD ASSEMBLY



Photos source: Prismark/Binghamton University

A. Apple A16 Applications Processor
B. Flash Memory
C. Qualcomm SDX65M 2G-5G Baseband
D. Qualcomm SDR735 2G-5G TRx (sub-6GHz), 2x
E. Qualcomm SMR546 5G IF TRx (mmWave)
F. Power Manger (Apple, Qualcomm, etc)
G. Apple/Cirrus Logic Audio Amplifier
H. Apple/Cirrus Logic Audio Codec
I. FEM (Broadcom, Skyworks, etc.)
J. Wi-Fi Module
K. USI UWB Module
L. Broadcom Wireless Charging
M. NXP Display Manager
N. 5G mmWave Module
O. NXP NFC Controller

Note: Front board is 10L any-layer HDI, rear board is 8L any-layer HDI

922.432mvc

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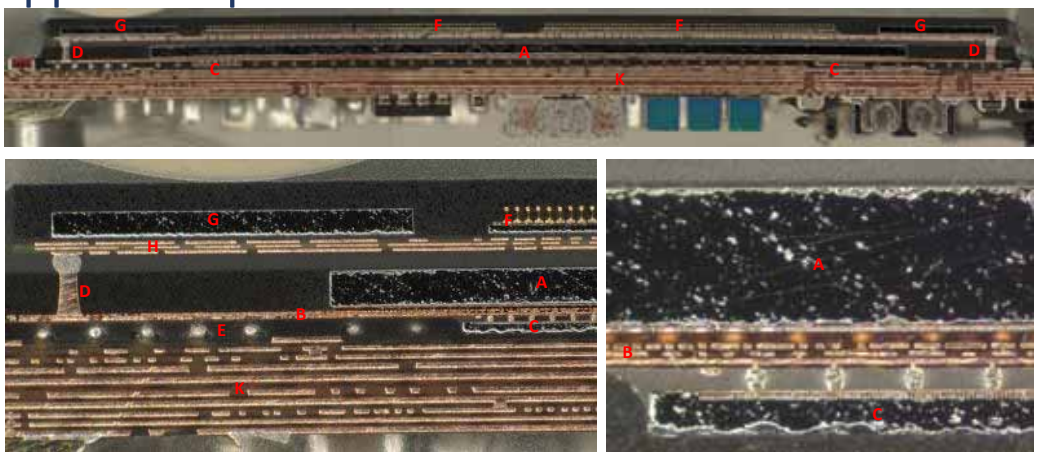
Apple A16 processor



A16 in FOWLP (A) as bottom package
5 RDL layers (B)
Capacitor die (C) on underside of FOWLP
Peripheral TMV (D) for top package interconnect
0.3mm ball pitch (E)
0.4mm collapsed height

0.9mm total collapsed height
10L Anylayer digital main board (K)

Memory (F) and dummy die (G) in top package
Wirebonded memory die
3L HDI (H)
0.3mm ball pitch (not shown)
0.5mm collapsed height

Photos source: Prismark/Binghamton University

Smart Phones Lead in SiP Implementation

Apple A12 Processor

WLP Fan-Out Apple

Samsung EXYNOS 9810

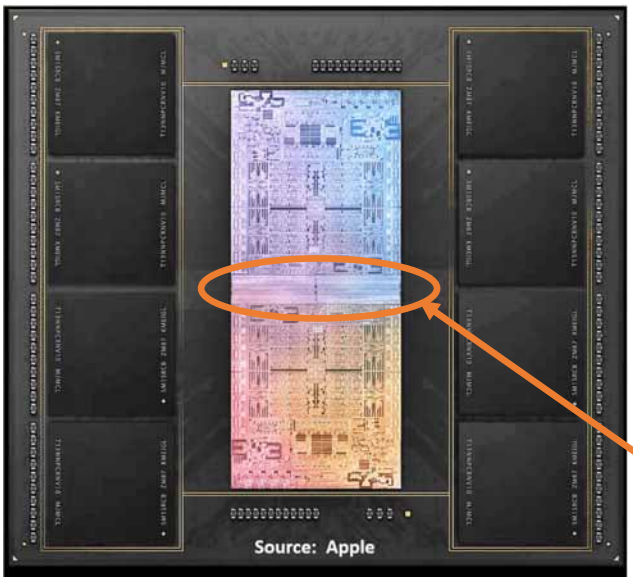
Advanced PoP
Samsung

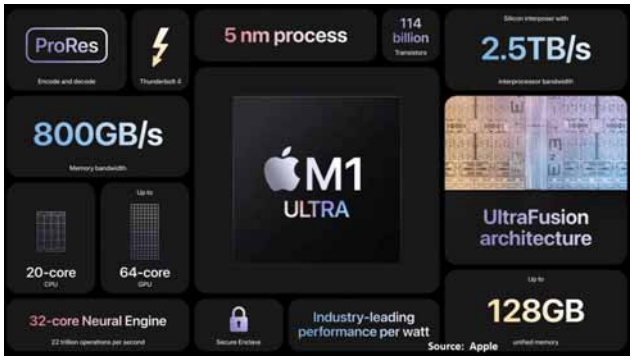
Huawei HiSilicon Kirin 980

Advanced PoP
Huawei

Source: Prismark Partners & Binghamton University

Apple Mac Studio Ultra

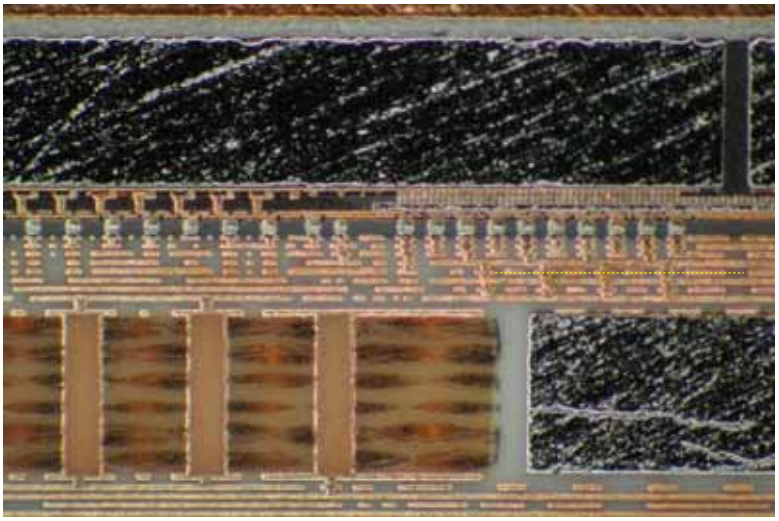




Silicon bridge connection

70mm Package

Joining metallurgy between Apple Ultra M1 logic chip and Si bridge



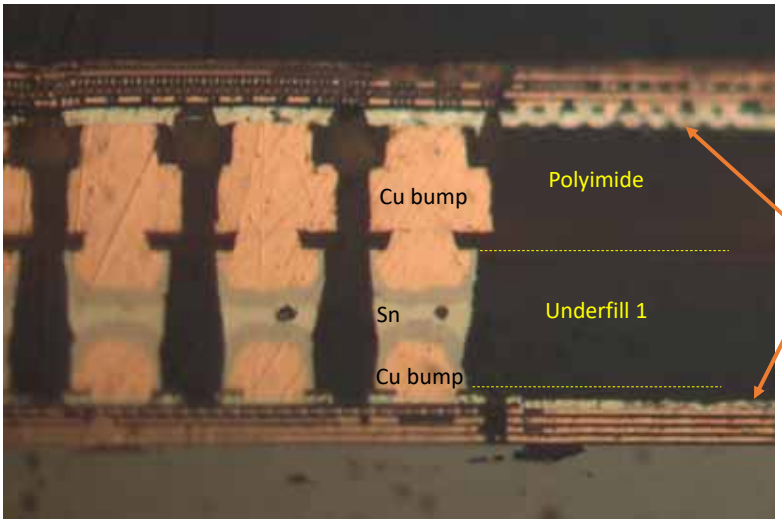
M1 chip circuits

Si bridge circuits

Core Substrate w/ embedded device

Photos source: Prismark/Binghamton University

Joining metallurgy between Apple Ultra M1 logic chip and Si bridge



M1 chip circuits

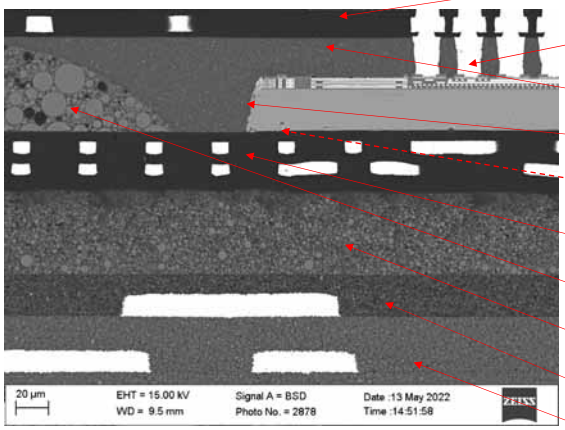
25 micron pitch

Aluminum final metallization

Si bridge circuits

Photos source: Prismark/Binghamton University

A cross section of Si Bridge and substrate Interface



PSPI and wiring

Micro bump joining for M1 and Si bridge

C4 (flip chip joining, not shown here)

Underfill 1 (for micro joining)

Si bridge diced edge

Backside grinding plane

PSPI and wiring levels formed after backside grinding (RDL)

Molding compound

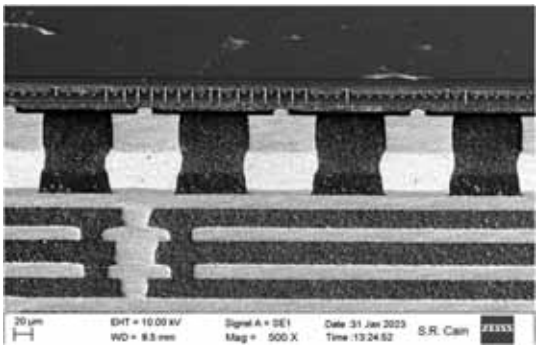
Underfill 2

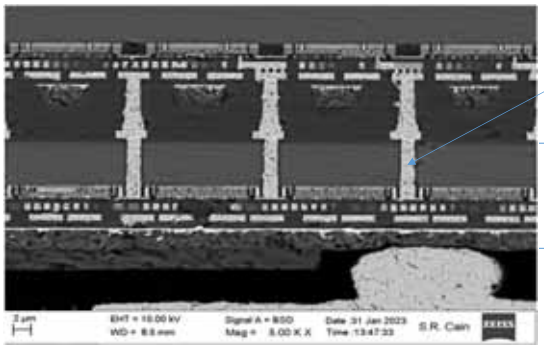
Solder mask

Substrate cross section

Photos source: Prismark/Binghamton University

Die Stacking in AMD Ryzen 7 5800X3D



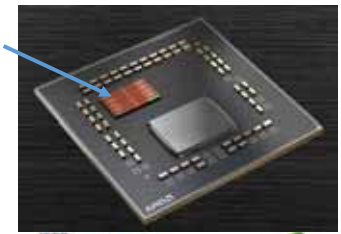


1.6 um dia

16 um

Source: Binghamton University & Prismark Partners

Stacked L3 cache

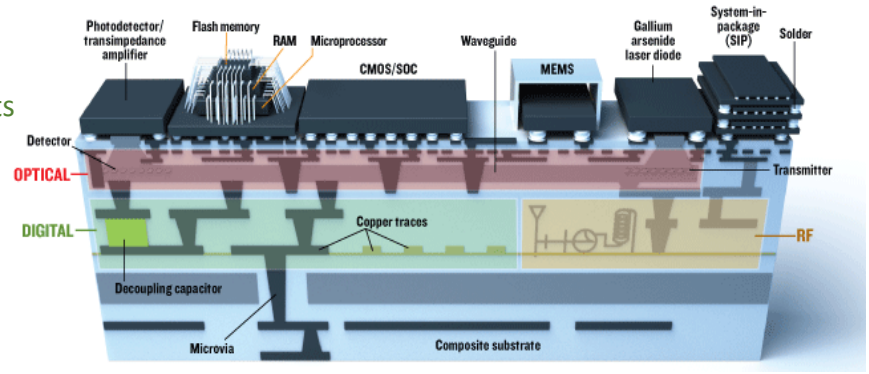


Source: AMD

Die to die interconnect: ~1.6 um dia columns on 15.5 um pitch

SOLUTION

- Smaller nodes
- 2.5 & 3D
- Smaller interconnects
- Smaller Line/space
- Shorter distances
- TSV & Bridges
- Embedded
- Co-packaging



Press Release October 9th , 2019
The Royal Swedish Academy of Sciences
awards the Nobel Prize in Chemistry 2019 to

- **John B. Goodenough**
  The University of Texas at Austin, USA
- **M. Stanley Whittingham**
  Binghamton University, State University of New York, USA
- **Akira Yoshino**
  Asahi Kasei Corporation, Tokyo, JapanMeijo University, Nagoya, Japan

"for the development of lithium-ion batteries"

"They created a rechargeable world"

The Nobel Prize in Chemistry 2019 rewards the development of the lithium-ion battery. This lightweight, rechargeable and powerful battery is now used in everything from mobile phones to laptops and electric vehicles. It can also store significant amounts of energy from solar and wind power, making possible a fossil fuel-free society. Press Release October 9th , 2019

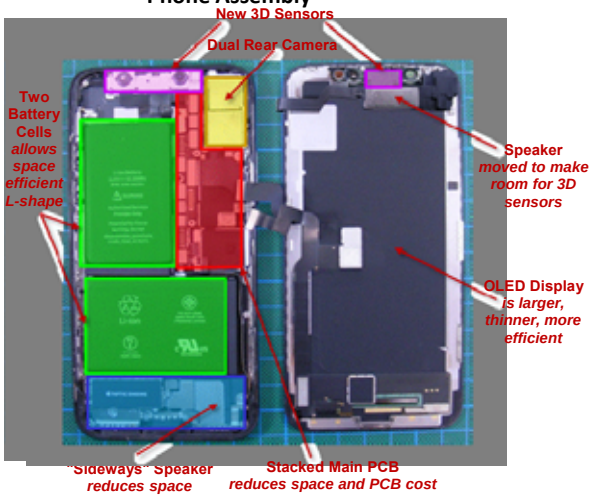
The Royal Swedish Academy of Sciences

How much space does the battery occupy?

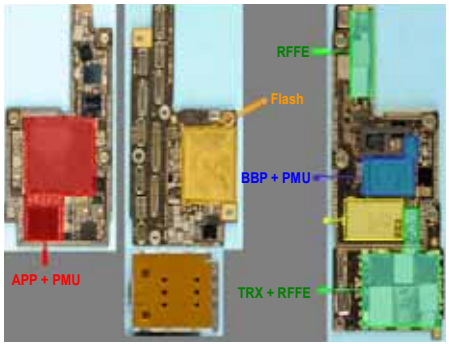
Example from Apple IPhone X

Source: Prismark Partners

Phone Assembly

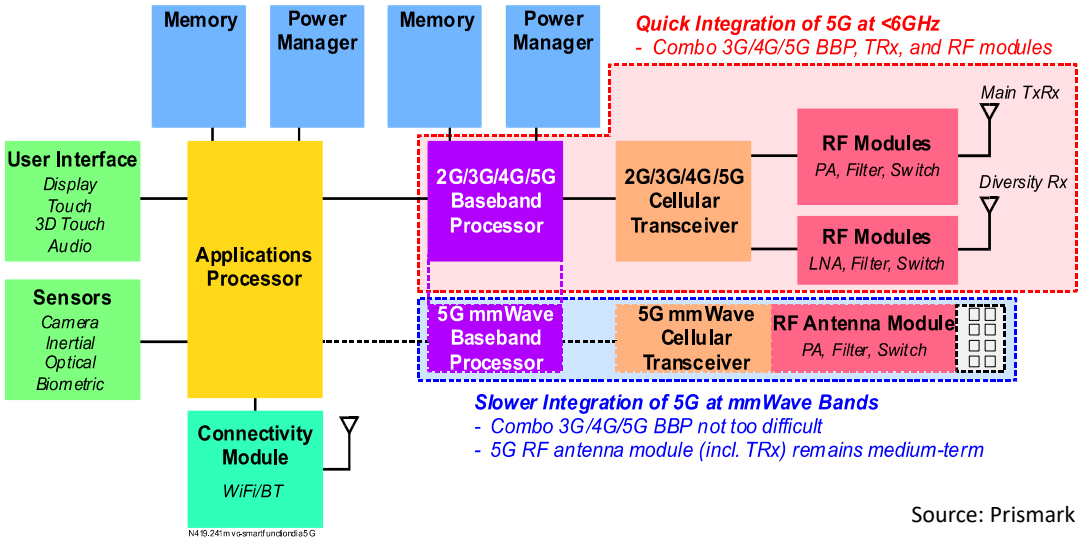


Stacked Main PCB Board



PCB Footprint (1553 sq mm – 14% of the bottom frame area

Impact of 5G on Packaging



Source: Prismark

TWGs Collaboration

MEMS & Sensor Integration
5G & 6G
Supply Chain
SIP & Module
Emerging Materials
Single & Multichip Integration
Reliability
Additive Manufacturing

Low warpage Low Dielectric -ABF

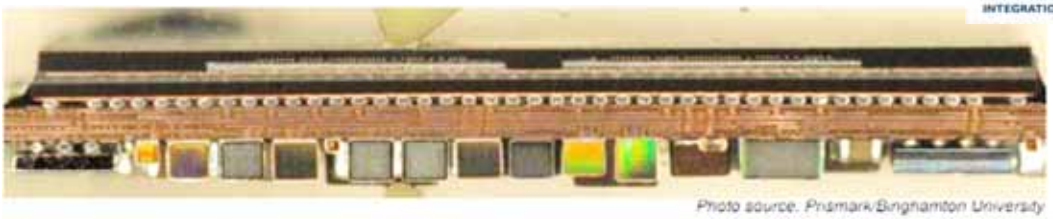
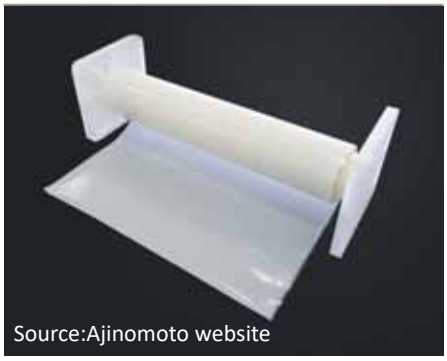
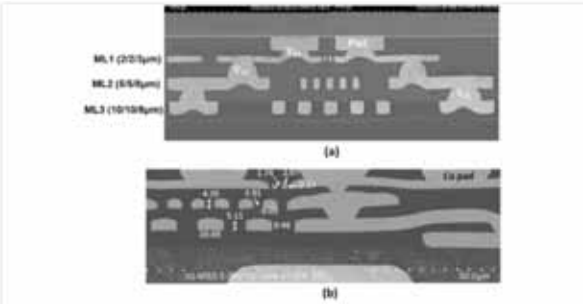


Photo source. Prismark/Binghamton University

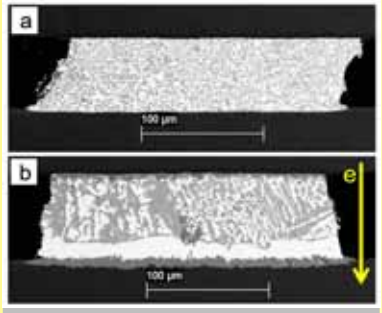


Source:Ajinomoto website



G.C.F Chen et al., "2.3D Hybrid substrate with Ajinomoto build-up film for Heterogenous Integration" May 2022, pp 30-37 (Unimicron)

ELECTROMIGRATION

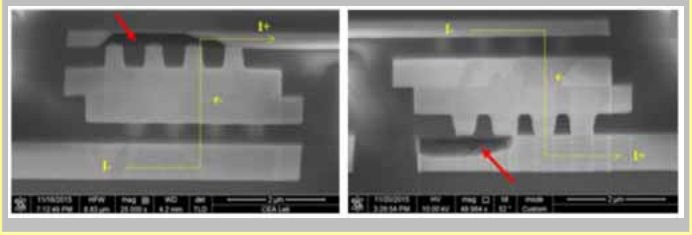


EM behavior of Bi-Sn solder as potential lower process temp material.

Source: E Cotts, BU

EM is Major concern
-Joule heating and hot spot due to thin layers
-higher current density
-Software and physics based models are used to predict and mitigate Void formation

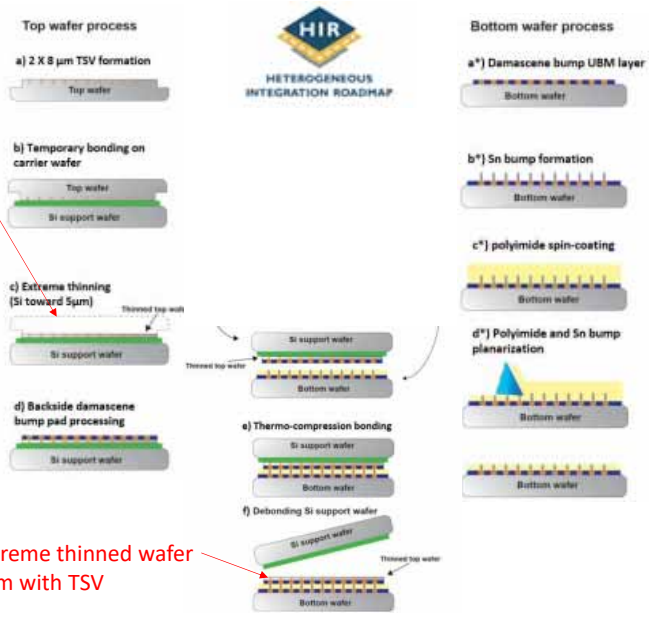
Source: P. Ho (UT)



EXTREME THIN DIES

Carrier bonding
Thinning
CMP-TSV reveal
TCB (thermal compression Bonding)
Debond/Lift off

Reference: Julien Bertheau, et al (imec) & Atsushi Nakamura (Fujifilm Electronic Materials), "Extreme Thinned-Wafer Bonding Using Low Temperature Curable Polyimide for Advanced Wafer Level Integrations" in *IEEE 68th Electronic Components and Technology Conference, San Diego*



Extreme thinned wafer 5um with TSV