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Heterogeneous Integration Roadmap

Integrated Power Electronics (IPE) Chapter 10



Chapter 10 Outline

Section I: Embedded Integrated Voltage Regulators

- I.1. Summary
- I.2. Requirements
- I.3. Existing Solutions and Challenges
- I.4. Potential Solutions
- I.5. Required R&D

Section II: Power System-In-Package (SIP) Modules

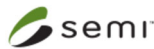
- II.1. Power Module Topologies
- II.2. SIP Power Module Integration
- II.3. Potential Solutions and Required R&D
- II.4. Passive Components
- II.5. Roadmap

Section III: Integrated High-Power Systems

- III.1. Introduction
- III.2. Challenges in Circuit Architectures
- III.3. Challenges and Existing Solutions
- III.4. Power Module (High Voltage)

Section IV: Energy Harvesting

- IV.1. Introduction
- IV.2. Energy Harvester Related Integration Challenges
- IV.3. Power Management ICs (PMICs) for Energy Harvesting
- IV.4. Challenges and Solutions Roadmap





 HETEROGENEOUS
 INTEGRATION ROADMAP

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Chapter 10 Contributors








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 INTEGRATION ROADMAP

Graphic Description of Chapter Contents

PART-I Inside SiP

Type C) In substrate

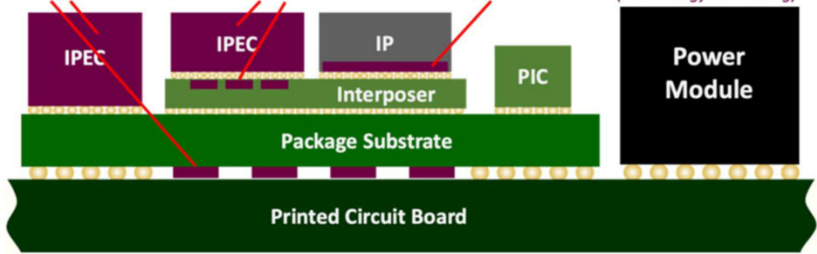
- On top side
- On land side

Type B) In interposer

- On top side
- Integrated in active interposer
- Embedded in organic interposer


Type A) In load

- (Ex. IP, HBM, PIC)
- Monolithic integration
- Hybrid bonding








PART-II & -IV Board-Mount & Standalone
(Incl. Energy Harvesting)


Power Module



PART-III Higher Power Modules
(Ex. Integrated Power Modules)

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Integration with Load and/or Interposer

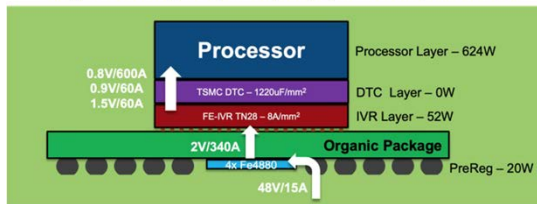


Hybrid Bonding

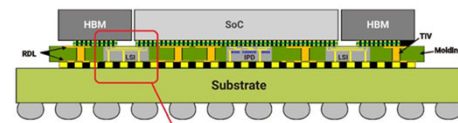
Integrate a hybrid converter topology:

1st stage: 48V-to-2V converter on landside of package

2nd stage: hybrid-bond deep trench capacitor (DTC) and integrated voltage regulator (IVR) layers to the processor dies

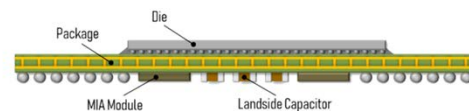


IEEE Power Electronics Society October 22, 2020,
Integrated Power – A Virtual Panel Session

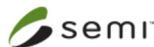


CoWoS-L, with embedded Local Silicon Interconnect bridge
"BEOL" chip-last assembly

Highlights of the TSMC Technology Symposium Part 2



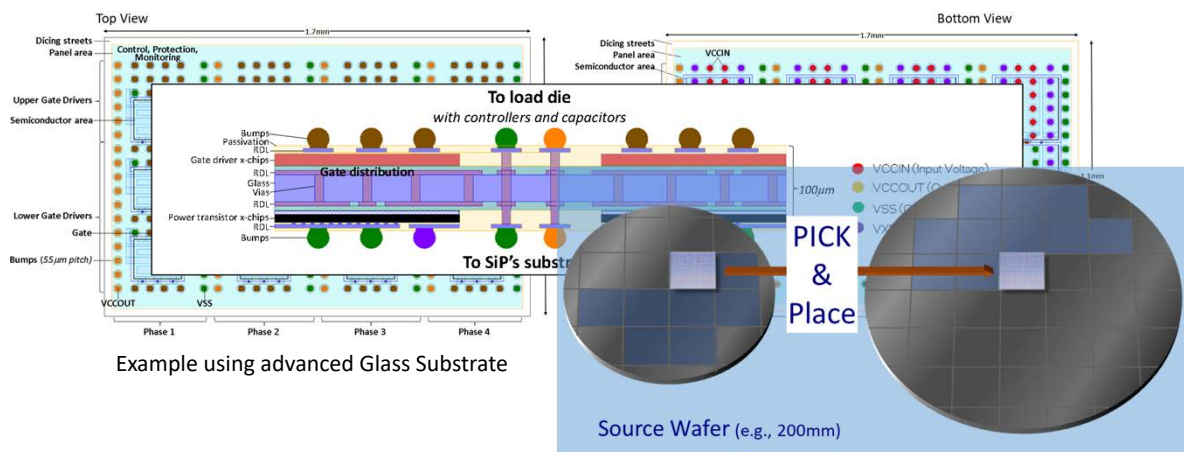
Magnetic Inductor Arrays for Intel® Fully Integrated Voltage Regulator (FIVR) on 10th generation Intel® Core™ SoCs



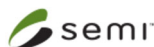
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HI of III-V chips and other processes via Micro-Transfer Printing (μ TP)



Example using advanced Glass Substrate



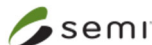
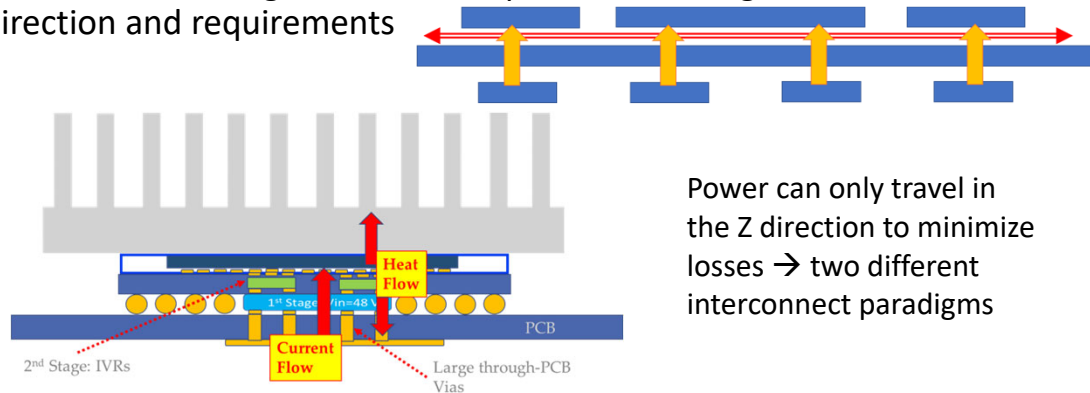
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In HPC, Signal Interconnect Requirements Are at Odds with Power Integrity



- In the substrate, Signal and Power paths are orthogonal both in direction and requirements



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IVR Requirements

Metric	Target	
Input Voltage	> 5 V	Reduce routing loss
Output Voltage	0.6 – 1.2 V	
Current Density	> 10 A/sqmm	
Target Efficiency	> 90 %	Minimize power loss
Switching Freq	10-25 MHz	Shrink passives Increase transient response

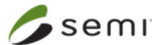
Source: K. Radhakrishnan

Additional requirements

Facilitates use in SiPs & SAP

- Modular building blocks
- Minimal z-height
- Known good “die” (KGD)
- Tested / binned prior to integration in SiP
- Low cost
- High reliability
- Ultra low thermal resistance

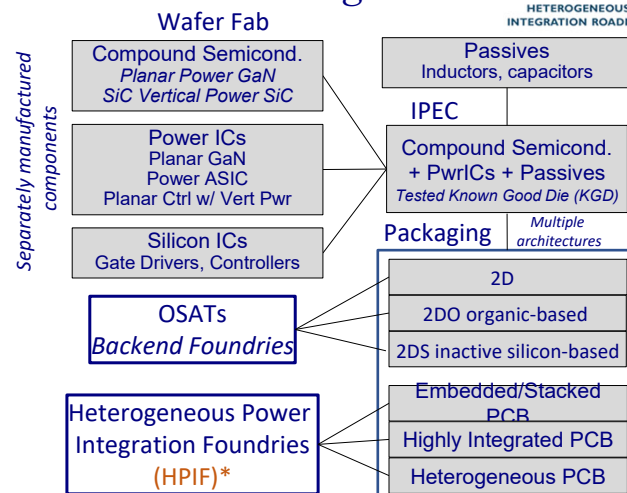
Source: K. Radhakrishnan, Challenges and Innovations in Microprocessor Power Delivery, IEEE Electronics Packaging Society Silicon Valley Area Chapter webinar, June 22, 2002.
SAP: Stand Alone Power



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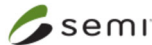


IPEC Integration



* HPIF Concept: National network of flexible-packaging foundries with Pwr Pkg PDKs (P³DKs)

Source: K. Radhakrishnan, Challenges and Innovations in Microprocessor Power Delivery, IEEE Electronics Packaging Society Silicon Valley Area Chapter webinar, June 22, 2002.
SAP: Stand Alone Power



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A sub-group of HIR Chapter 10 has engaged in projects funded by CHIPS Act



- DARPA NGMM Phase 0 Proposal has been accepted:
 - “Requirements for a 3DHI Power Microsystem (3DHIP) and Manufacturing Center”
- Participation to Manufacturing USA “Semiconductor Institute” RFI



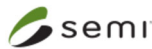
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Focus on Section IV for 2023 update: Energy Harvesting



- Challenges:
 - Multi-science simulation requirements (electrical, packaging, etc.)
 - Flexible, conformal components, substrates and packaging
 - Materials for Biodegradable Sensors



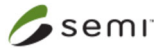
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Potential for Cross TWGs Collaborations

- Energy efficiency is job one for all products, both to improve performance and to satisfy the sustainability objectives.
- Power management is a critical aspects of all applications, thus relevant collaboration can be established with many HIR Chapters.
- Closer integration with the IEEE EPS Power and Energy Technical Committee is ongoing.



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