HIR 6th Annual Conference (2023)

Heterogeneous Integration Roadmap Updates

Single & Multichip Integration (CHAPTER 8)

TWG Chair & Co-Chair
William (Bill) Chen & Annette Teng
Lei Shan (speaker)
And the Single & Multichip Integration Technical Working Group

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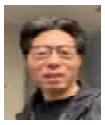
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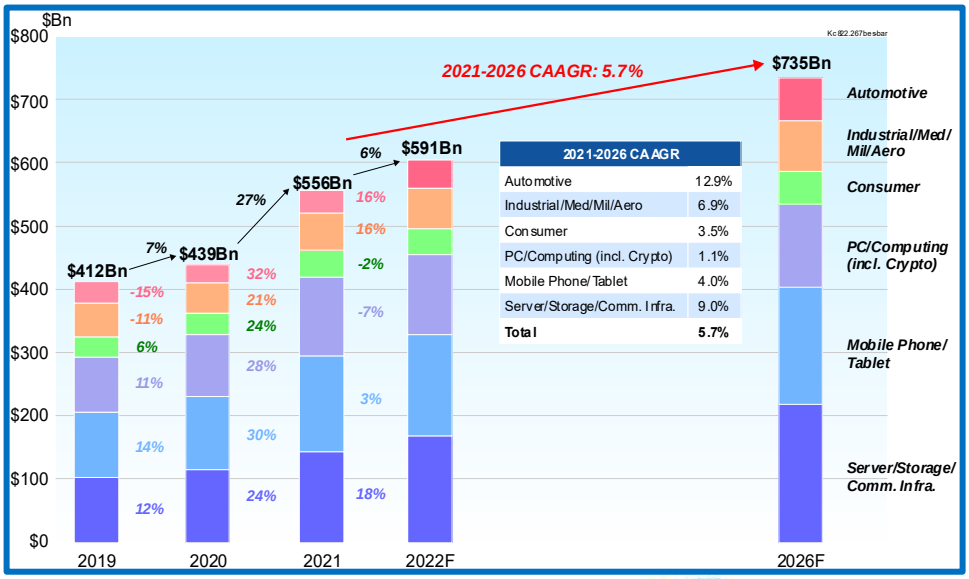
Electronics Industry Forecast is Bright



MAJOR MARKETS DRIVING GROWTH

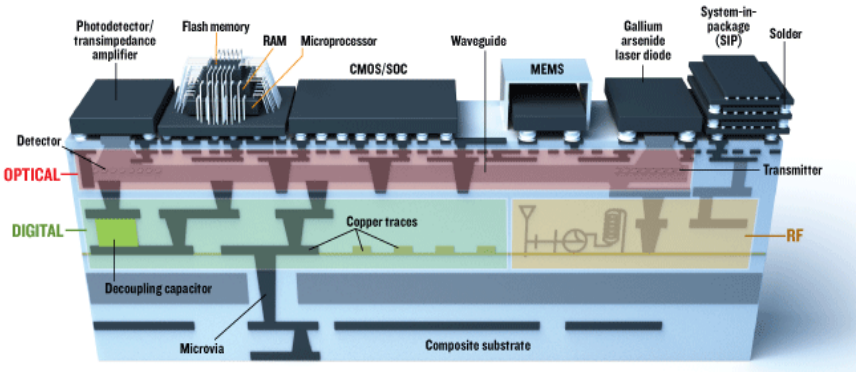
IoT to IoE	Smart Mobile Everywhere	Data to the Cloud & Data Centers	Autonomous Vehicles	Wearables & Health	Aerospace & Defense

MARKET DEMANDS

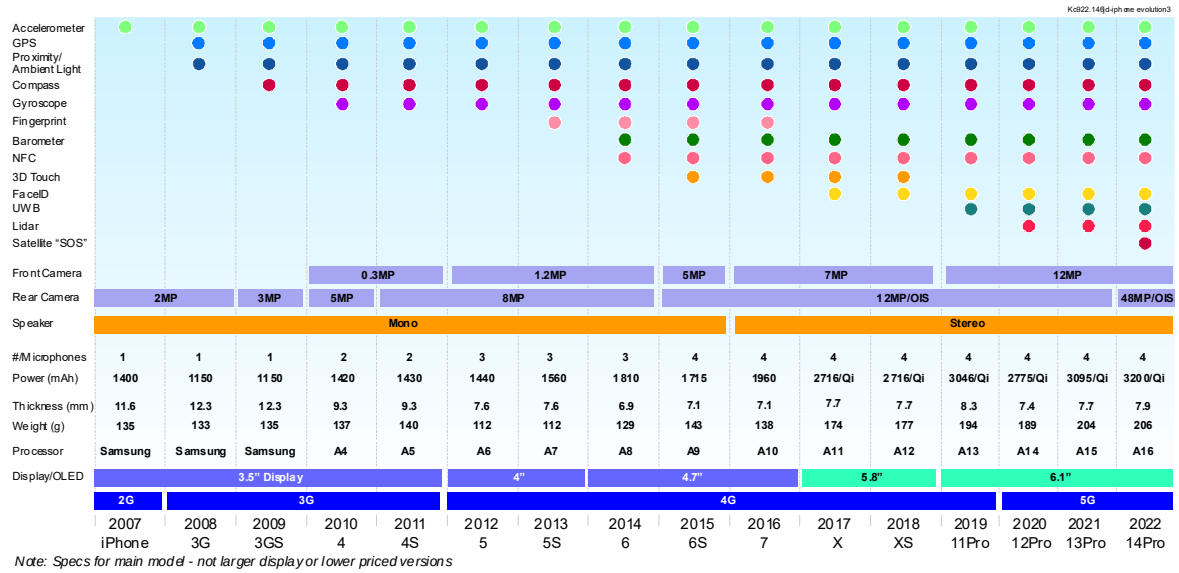
- More Compute Capability
- Compute Faster
- Less power
- Cooler
- Signal Integrity (SI)
- Power Integrity (PI)
- High bandwidth memory
- Photonics
- Low cost
- Reliable
- Miniature
- Cleaner/healthier

SOLUTION

- Chiplet
- 2.5D & 3D
- Low-power I/O
- Fine Line/space
- Proximity
- Embedded
- Clean power
- Adaptive cooling
- Heterogeneous



APPLE IPHONE EVOLUTION



Note: Specs for main model - not larger display or lower priced versions

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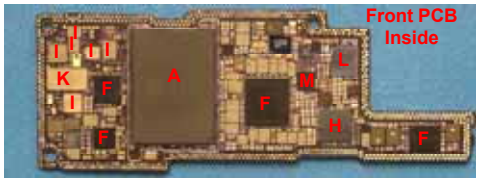
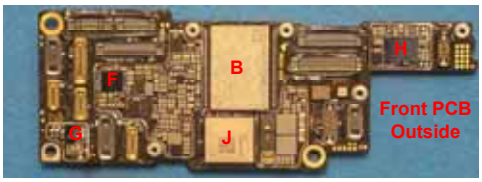
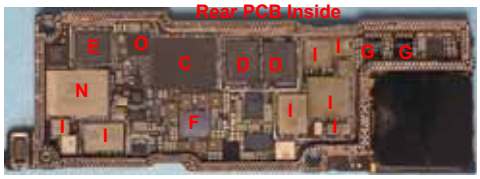
APPLE IPHONE 14 PRO MAIN BOARD ASSEMBLY







Photos source: Prismark/Binghamton University

A. Apple A16 Applications Processor
B. Flash Memory
C. Qualcomm SDX65M 2G-5G Baseband
D. Qualcomm SDR735 2G-5G TRx (sub-6GHz), 2x
E. Qualcomm SMR546 5G IF TRx (mmWave)
F. Power Manger (Apple, Qualcomm, etc)
G. Apple/Cirrus Logic Audio Amplifier
H. Apple/Cirrus Logic Audio Codec
I. FEM (Broadcom, Skyworks, etc.)
J. Wi-Fi Module
K. USI UWB Module
L. Broadcom Wireless Charging
M. NXP Display Manager
N. 5G mmWave Module
O. NXP NFC Controller

Note: Front board is 10L any-layer HDI, rear board is 8L any-layer HDI

922.432mvc

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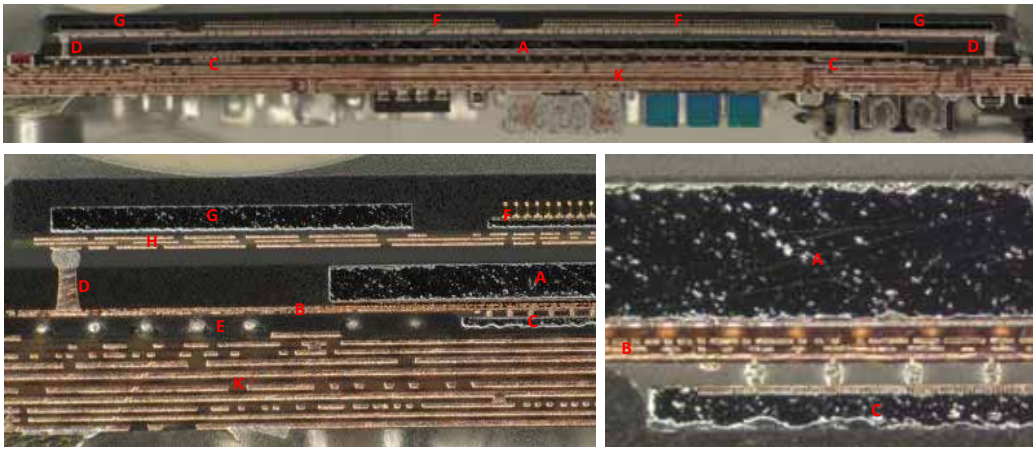
Apple A16 Processor



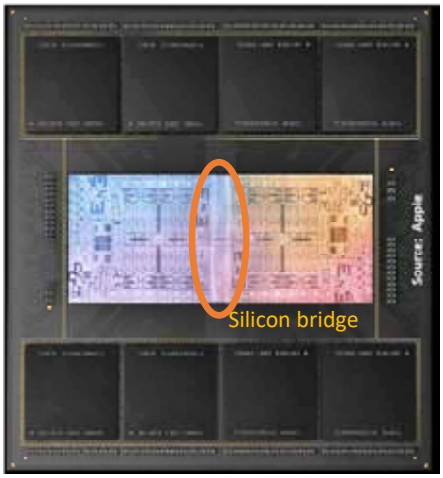
Photos source: Prismark/Binghamton University

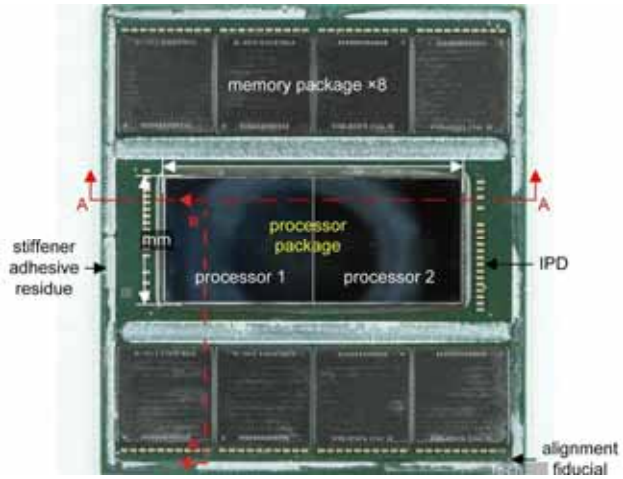
A16 in FOWLP (A) as bottom package
5 RDL layers (B)
Capacitor die (C) on underside of FOWLP
Peripheral TMV (D) for top package interconnect
0.3mm ball pitch (E)
0.4mm collapsed height

0.9mm total collapsed height
10L Anylayer digital main board (K)

Memory (F) and dummy die (G) in top package
Wirebonded memory die
3L HDI (H)
0.3mm ball pitch (not shown)
0.5mm collapsed height

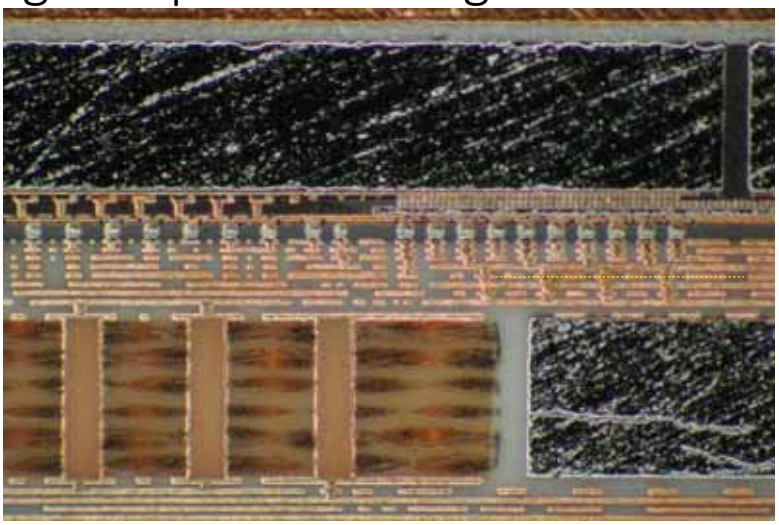
Apple Mac Studio Ultra (70mm), 20-core CPU, 64-core GPU, 800GB/s BW





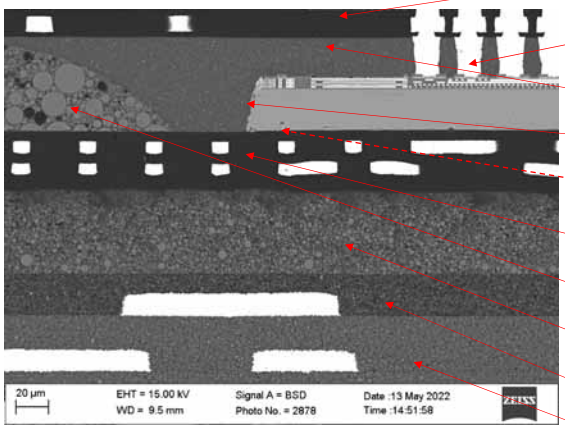
Photos source: Tech Insights

Joining metallurgy between Apple M1 Ultra logic chip and Si bridge



Photos source: Prismark/Binghamton University

A cross section of Si Bridge and substrate Interface



PSPI and wiring
Micro bump joining for M1 and Si bridge
C4 (flip chip joining, not shown here)
Underfill 1 (for micro joining)
Si bridge diced edge
Backside grinding plane
PSPI and wiring levels formed after backside grinding (RDL)
Molding compound
Underfill 2
Solder mask
Substrate cross section

Photos source: Prismark/Binghamton University

SINGLE & MULTICHIP ROADMAP METRICS

Year of Production	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*
On-chip feature size (nm)							
Memory (DDR/HBM)	10	7	7	5	5	3	3
Smart Phone / Laptop	5	5	3	3	2	2	2
High-performance (note1), chiplet/monolithic	7	5	5	3	3	2	2
Maximum Average Power Density (W/mm^2)							
Memory (DDR/HBM) (note2)	0.06/0.12	0.05/0.11	0.05/0.11	0.04/0.1	0.04/0.09	0.04/0.08	0.04/0.07
Smart Phone / Laptop	0.5	0.5	0.55	0.55	0.6	0.6	0.65
High-performance	0.9	0.95	0.95	1	1	1.05	1.05
Core Voltage (Minimum Volts)							
Memory (DDR/HBM)	1.2	1.1	1.1	1	1	0.9	0.9
Smart Phone / Laptop	0.75	0.75	0.75	0.75	0.7	0.7	0.7
High-performance	0.8	0.75	0.75	0.75	0.75	0.7	0.7
Package Pin count Maximum							
Memory (DDR/HBM)	288/3200	288/3200	288/3200	326/4100	326/4100	350/4700	350/4700
Smart Phone / Laptop	1212/7000	1212/7000	1275/7600	1275/7600	1396/8400	1396/8400	1396/8400
High performance (note3)	6400	7800	7800	9600	9600	11200	11200
Minimum Package Dimension (mm)							
Memory (DDR/HBM)	133	133	133	133	133	133	133
Smart Phone / Laptop	50	50	55	55	60	60	60
High-performance	79	87	87	95	95	103	103

ADVANCE SUBSTRATE ROADMAP METRICS

	Year of Production		2018	2019	2020	2021	2022	2025	2028	2031	2034
Technology	Parameter	Units									
FCBGA substrate	Maximum layer Count	N/A	20	20	20	20	22	24	24	26	26
	Maximum body size	mm2	3000	3500	4000	4500	5000	6500	8000	9000	>10000
	Minimum Bump Pitch	µm	110	110	100	100	100	90	90	80	80
	Copper roughness	nm	500	300	300	300	150	150	100	<100	<100
	Dielectric loss tangent (Df)		0.007	0.007	0.007	0.007	0.004	0.004	0.002	0.002	0.002
Chiplet (Fan-out, Organic interposer)	Min. Bump Pitch (um)	µm	50	50	50	45	45	40	40	30	30
	Min Line width (um)	µm	2.0	2.0	2.0	1.5	1.5	1.0	1.0	0.5	0.5/0.5
	Min. uVia diameter (um)	µm	30	30	30	20	20	10	10	5	5
Chiplet (Si Interposer) solder based	Min. Bump Pitch (um)	µm	40.0	40.0	40.0	35.0	30.0	22.0	16.0	13.0	10.0
	Min Line width (um)	µm	0.6	0.6	0.6	0.6	0.6	0.5	0.4	0.3	0.2
	Min. uVia diameter (um)	µm	0.6	0.6	0.6	0.6	0.6	0.5	0.4	0.3	0.2
Chiplet (Si Interposer) hybrid bonding	Min. Bump Pitch (um)	µm				9.0	9.0	6.0	6.0	3.0	3.0

WARPAGE REDUCTION ROADMAP

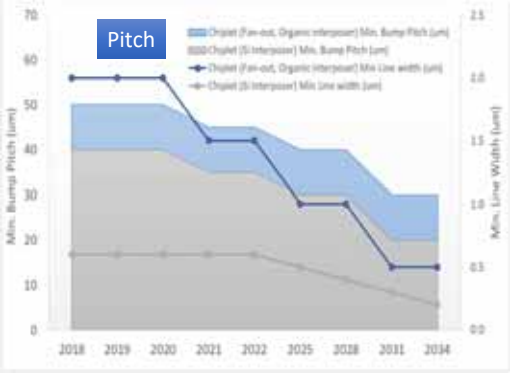
Table 2: Warpage Allowance across two market segments

	Year of Production	2018	2019	2020	2023	2026	2029	2030
	Pitch (mm)							
HPC	1.0	-0.13, +0.21	-0.11, +0.18	-0.11, +0.18	-0.11, +0.18	-0.10, +0.16	-0.08,+0.16	-0.08,+0.17
		-0.13, +0.20	-0.11, +0.18	-0.11, +0.18	-0.11, +0.18	-0.10, +0.15	-0.08,+0.15	-0.08,+0.16
	0.8	-0.13, +0.21	-0.11, +0.18	-0.11, +0.18	-0.11, +0.18	-0.10, +0.16	-0.08,+0.16	-0.08,+0.17
		-0.10, +0.10	-0.09, +0.09	-0.09, +0.09	-0.09, +0.09	-0.08, +0.08	-0.07, +0.07	-0.07, +0.07
	0.65	-0.10, +0.10	-0.09, +0.09	-0.09, +0.09	-0.09, +0.09	-0.08, +0.08	-0.07, +0.07	-0.07, +0.07
		-0.09, +0.09	-0.08, +0.08	-0.08, +0.08	-0.08, +0.08	-0.07, +0.07	-0.065, +0.065	-0.065, +0.065
Mbile	0.5	-0.09, +0.09	-0.08, +0.08	-0.08, +0.08	-0.08, +0.08	-0.07, +0.07	-0.065, +0.065	-0.065, +0.065
		-0.08, +0.08	-0.07, +0.07	-0.07, +0.07	-0.07, +0.07	-0.065, +0.065	-0.06, +0.06	-0.06, +0.06
	0.4	-0.08, +0.08	-0.07, +0.07	-0.07, +0.07	-0.07, +0.07	-0.065, +0.065	-0.06, +0.06	-0.06, +0.06
		-0.07, +0.07	-0.065, +0.065	-0.065, +0.065	-0.065, +0.065	-0.06, +0.06	-0.055, +0.055	-0.055, +0.055
	0.3	-0.07, +0.07	-0.065, +0.065	-0.065, +0.065	-0.065, +0.065	-0.06, +0.06	-0.055, +0.055	-0.055, +0.055
		-0.06, +0.06	-0.055, +0.055	-0.055, +0.055	-0.055, +0.055	-0.05, +0.05	-0.045,+0.045	-0.045,+0.045
	0.25		-0.055, +0.055	-0.055, +0.055	-0.055, +0.055	-0.05, +0.05	-0.045,+0.045	-0.045,+0.045
				-0.055, +0.055	-0.055, +0.055	-0.05, +0.05	-0.045,+0.045	-0.045,+0.045
	0.2			-0.055, +0.055	-0.055, +0.055	-0.05, +0.05	-0.045,+0.045	-0.045,+0.045
					-0.045,+0.045	-0.045,+0.045	-0.045,+0.045	-0.045,+0.045
	0.15				-0.045,+0.045	-0.045,+0.045	-0.045,+0.045	-0.045,+0.045
					-0.025,+0.025	-0.025,+0.025	-0.025,+0.025	-0.025,+0.025
	0.1				-0.025,+0.025	-0.025,+0.025	-0.025,+0.025	-0.025,+0.025
						-0.020,+0.020	-0.020,+0.020	-0.020,+0.020

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

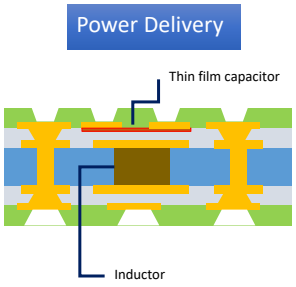
SUBSTRATE KEY DRIVERS AND BUILDING BLOCKS

source: K Lee, Intel



- High resolution litho & laser process
- Photoimagible dielectric materials CTE <3ppm
- Panel Level Dry seed, etching process and tool.
- Fine pitch bumping technology
- Low warpage BU/Core materials for large form factor substrate

- Low copper roughness
- Low dielectric constant BU material
- Pure chemical assisted adhesion promoter



- High capacitance thin film capacitor
- High inductance inductor compatible to embedding in substrate

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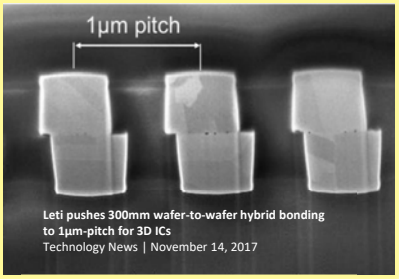
CHIP ASSEMBLY KEY CHALLENGES

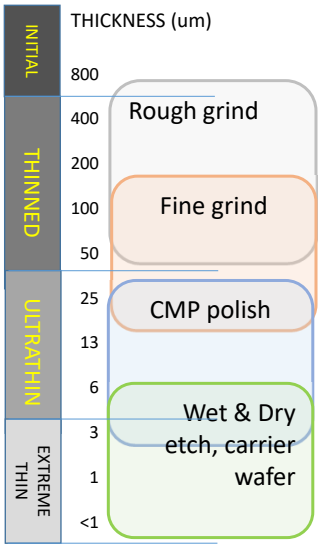
chip size, chip thickness, process thermal budget, metal density, warpage control, dicing quality, surface treatment conditions, bond tool accuracy, and particle control

S. W. Liang, Gene C. Y. Wu, K. C. Yee, C. T. Wang, Ji James Cui, and Douglas C. H. Yu

"High Performance and Energy Efficient Computing with Advanced SoIC™ Scaling"
2022 ECTC, Taiwan Semiconductor Manufacturing Company



WAFER THINNING



WAFER SINGULATION

1. Mechanical Dicing Saw
- High RPM Blade
- Wet process
- Silicon wafer all thicknesses

2. Laser Dicing

3. Plasma Dicing
- Very small dies
- Smooth finish

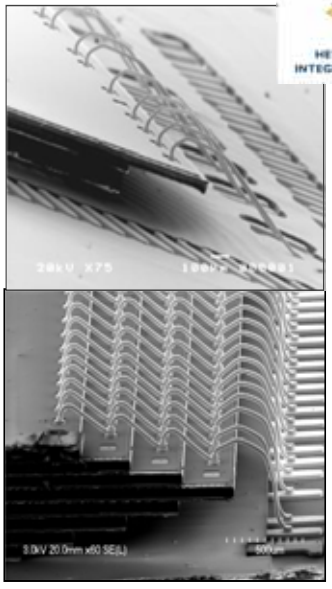
WIREBOND

Source: Ivy Qin KnS

Table 1: Wire Bond Interconnects

Year	2018	2019	2020	2021	2022	2025	2028	2031	2034
Wire Type									
Au ↓	38%	35%	31%	28%	24%	23%	22%	21%	20%
Ag ↑	3%	4%	5%	6%	7%	8%	8%	9%	10%
PdCu ↑	30%	32%	34%	36%	38%	38%	38%	38%	38%
Cu →	29%	29%	30%	30%	31%	31%	32%	32%	32%
Single In Line Pitch (µm)									
Au (Forward)	40	35	35	30	30	30	30	30	30
Au (SSB*)	45	40	38	33	33	33	33	33	33
Ag (Forward)	40	35	35	30	30	30	30	30	30
Ag (SSB)	45	40	38	33	33	33	33	33	33
PdCu (Forward)	40	35	35	30	30	30	30	30	30
PdCu (SSB)	45	40	38	33	33	33	33	33	33
Number of Pad/Loop Tiers (in HVM)									
Au	3	4	4	5	5	5	5	5	5
Cu	6	7	8	9	10	10	10	10	10
Cu (SSB)	4	5	6	7	8	9	10	10	10
Overhang Capability									
30um Die	0.5	0.6	0.7	0.8	0.9	0.9	1.0	1.0	1.0
20um Die	0.15	0.2	0.25	0.3	0.35	0.35	0.35	0.35	0.35
Low Loop Capability for Forward Bonding Wires (µm)									
Au and Ag wire	45	40	35	30	28	28	26	26	25

* -- SSB stands for Stand-Off Stitch Bond. It is widely used in SiP and Stack Die packages where die-to-die bonding is required.



SUMMARY

- The mega monolithic silicon chip is giving way to mega packages requiring mega integration of chiplets
- The Single & Multichip Integration Chapter covers the building block technology base for heterogeneous integration from architecture & design to assembly & manufacturing.
- You are Welcome to join our TWG

Backup

FLIPCHIP ROADMAP METRICS

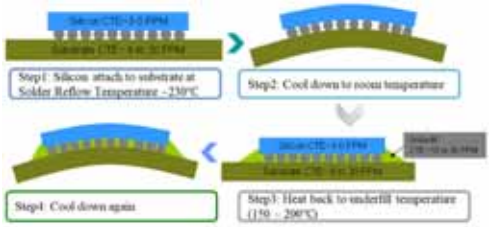
Source: M. Gerber, ASE

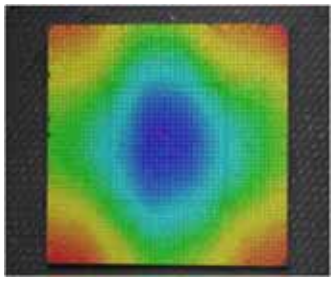
HETEROGENEOUS INTEGRATION ROADMAP

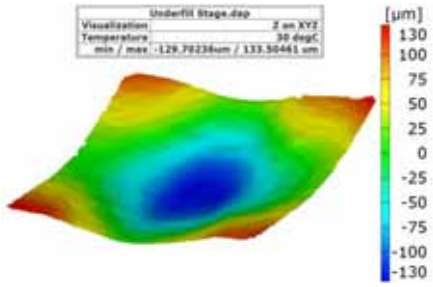
Year of Production	*2019*	*2020*	*2021*	*2022*	*2025*	*2028*	*2031*	*2034*
Flip Chip Pitch								
Flip Chip- Large Body Solder >12mm Sq Die	**130**	**130**	**130**	**130**	**130**	**130**	**130**	**130**
Flip Chip- Small Body Solder <12mm Sq Die	**130**	**130**	**130**	**130**	**130**	**130**	**130**	**130**
Flip Chip - Cu Pillar Small Body <12mm Sq Die (Periphery Staggered, Inline Same as large Body Cu Pillar)	**30/60**	**30/60**	**30/60**	**30/60**	**20/40**	**20/40**	**20/40**	**20/40**
Flip Chip- Cu Pillar Large Body >12mm Sq Die	**115**	**115**	**110**	**110**	**100**	**90**	**90**	**80**
Flip Chip Solder - COW	**50**	**50**	**50**	**50**	**50**	**50**	**50**	**50**
Flip Chip Cu Pillar -COW (Chiplets)	**40**	**40**	**35**	**30**	**25**	**25**	**25**	**25**
Flip Chip Cu Nano Particles	**30**	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Wafer to Wafer Cu to Cu Interconnect	***5***	***5***	***2***	***2***	***2***	***1***	***1***	***1***
Die to Wafer Cu to Cu Interconnect (Hybrid)	**30**	**30**	**30**	**30**	**20**	**20**	**20**	**20**
Embedded Die In Substrate Interconnect Pitch	**120**	**120**	**120**	**90**	**90**	**70**	**70**	**70**

2.5D Warpage Studies

- In most packaging architectures, manufacturing steps occur at elevated temperatures when the assembly is nearly plat. As cooling takes place, out-of plane deformation can occur due to CTE mismatches.
  - Non-uniform expansion/contraction of die and substrate in temperature cycle.
  - Results in warpage of the package which is major reliability concern.

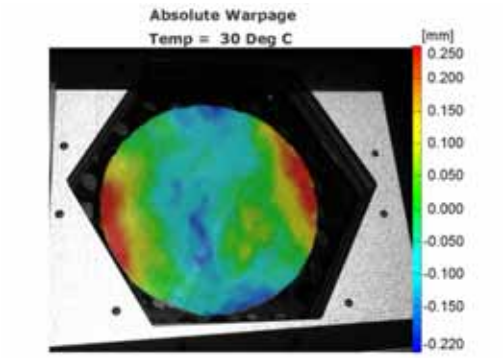


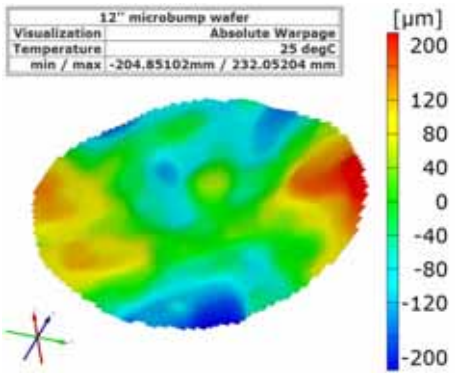




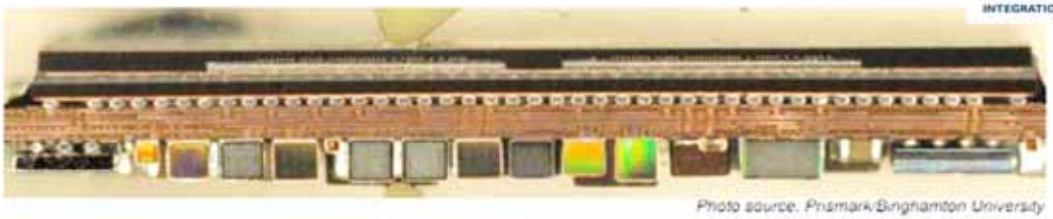
Wafer Warpage During Reflow

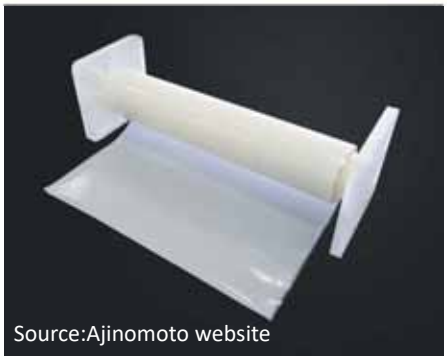
- 300 mm fully defined and back ground wafer processed in a reflow cycle from 25 °C to 240 °C
- Digital Image Correlation (DIC) warpage measurement was measured through the simulated reflow temperature cycling

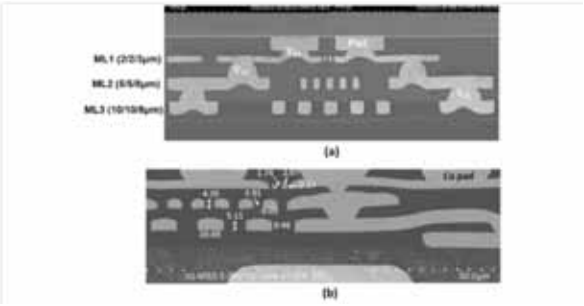




Low warpage Low Dielectric -ABF

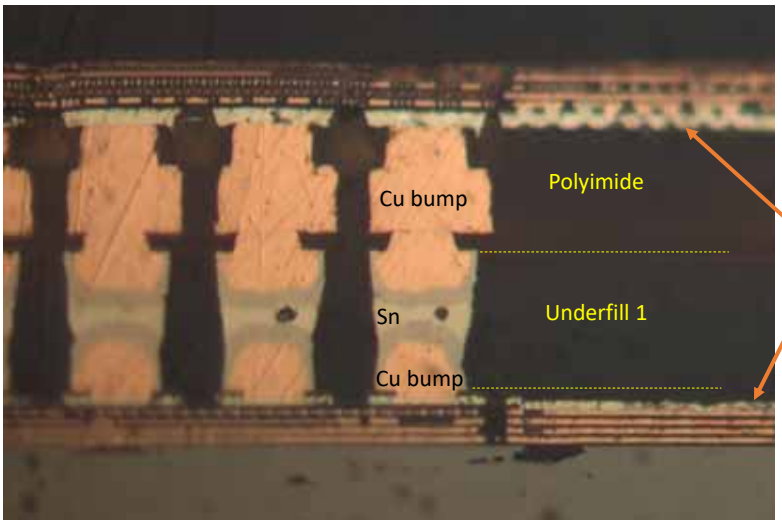






G.C.F Chen et al., "2.3D Hybrid substrate with Ajinomoto build-up film for Heterogenous Integration" May 2022, pp 30-37 (Unimicron)

Joining metallurgy between Apple M1 Ultra logic chip and Si bridge



M1 chip circuits

25 micron pitch

Aluminum final metallization

Si bridge circuits

Photos source: Prismark/Binghamton University

EXTREME THIN DICE

Carrier bonding

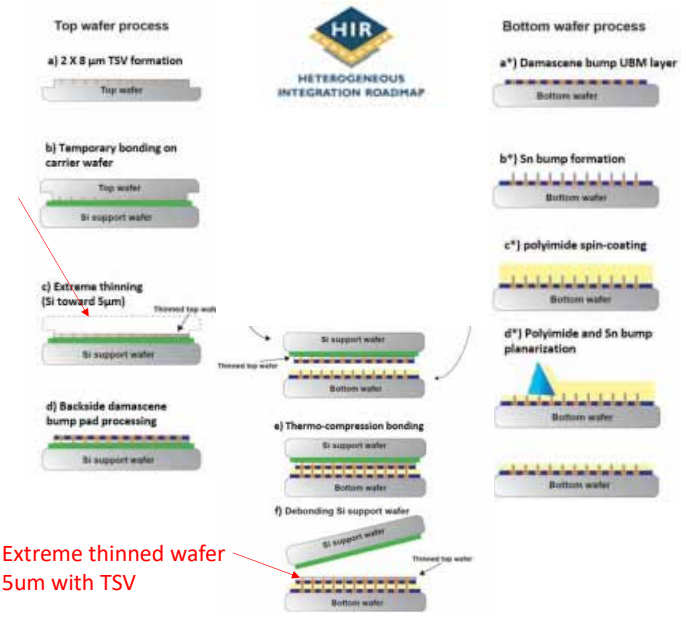
Thinning

CMP-TSV reveal

TCB (thermal compression Bonding)

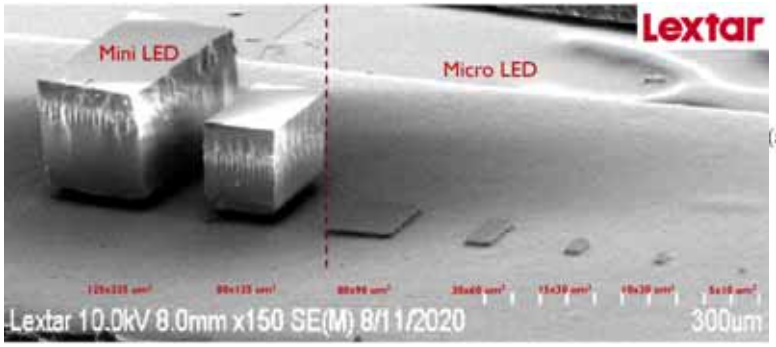
Debond/Lift off

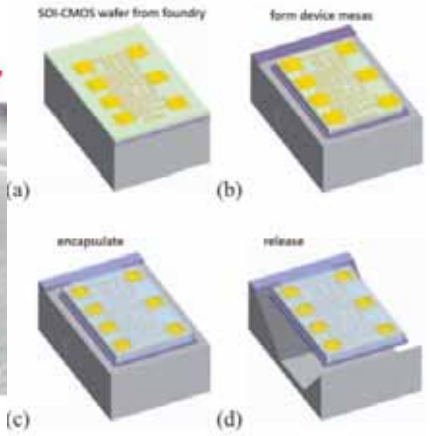
Reference: Julien Bertheau, et al (imec) & Atsushi Nakamura (Fujifilm Electronic Materials), "Extreme Thinned-Wafer Bonding Using Low Temperature Curable Polyimide for Advanced Wafer Level Integrations" in *IEEE 68th Electronic Components and Technology Conference, San Diego*



Extreme thinned wafer
5um with TSV

SINGULATION BY ETCHING

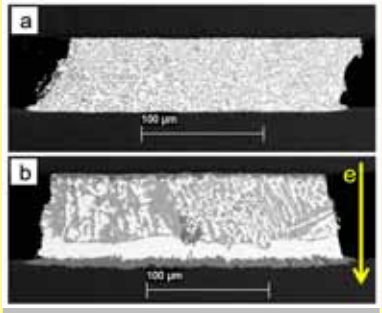




XCeleprint

Reliability: Multiscale and Multiphysics Modes/Mechanisms/Models for Degradation and Failure

ELECTROMIGRATION



EM behavior of Bi-Sn solder as potential lower process temp material.

Source: E Cotts, BU

EM is Major concern
-Joule heating and hot spot due to thin layers
-higher current density
-Software and physics based models are used to predict and mitigate Void formation

Source: P. Ho (UT)