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Heterogeneous Integration Platform for Next Generation Computing

“Road to Beyond Moore”

Moonsoo Kang, Ph.D.

EVP, Advanced Package(AVP) Business
Samsung Electronics

Samsung Proprietary

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Samsung AVP's Beyond Moore Platform

- HI Platform Overview
- Platform's Value and Roadmap

Technical Challenges

Heterogeneous Integration Eco System

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Introduction

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Why We Need "Beyond Moore"

Increased need for new solutions due to slowdown of Moore's Law and the computing power solutions

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3 Challenges

Cost

Moore's law slowdown caused by technical difficulty while cost continue to increase

Performance

Power efficiency and bandwidth are limited by physical constraint of chiplets

Memory BW

Bottle-neck of System Performance is Memory Bandwidth

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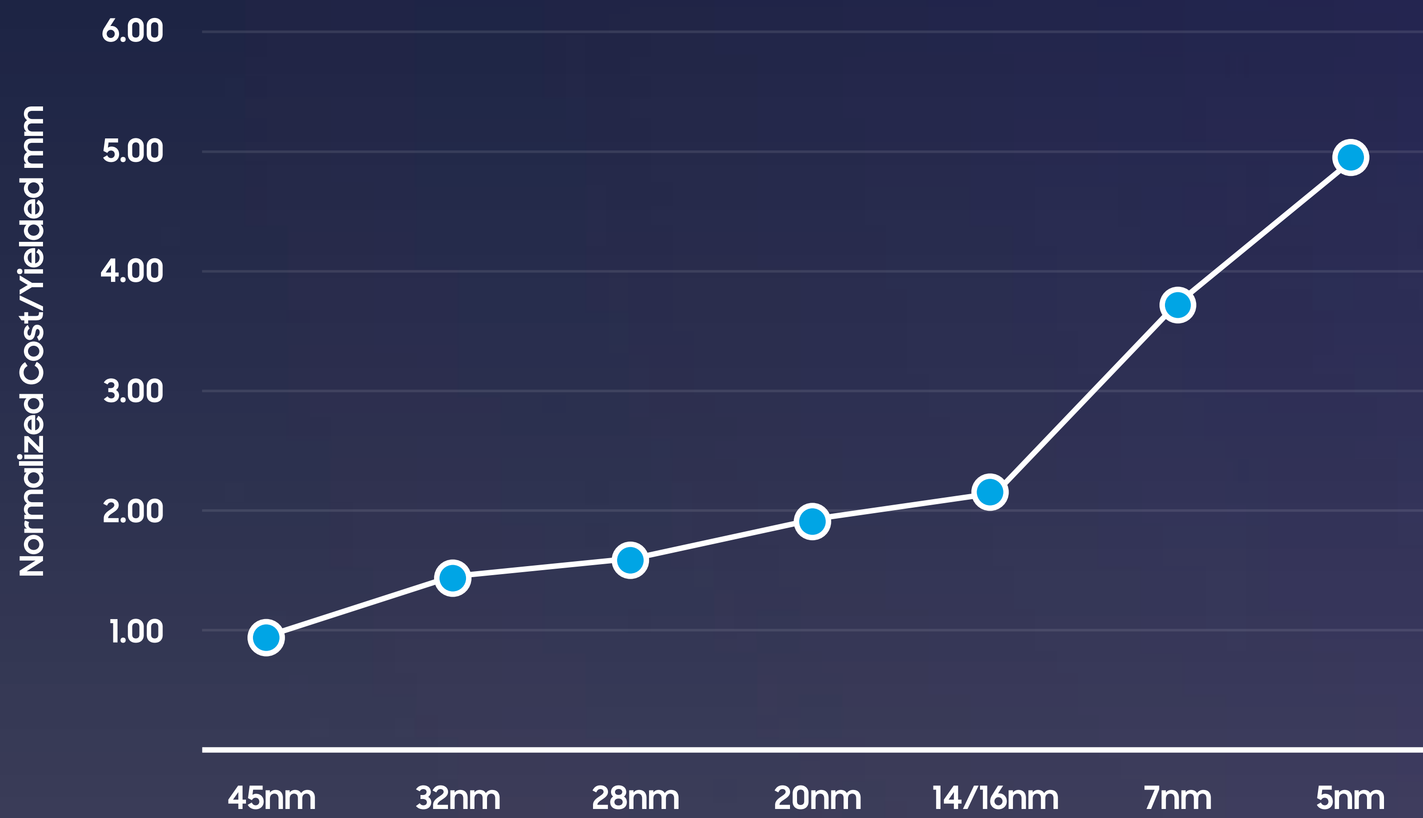
Why We Need "Beyond Moore"

- Heterogeneous integration to mitigate development cost and to improve performance

Cost Challenge

Moore's law slowdown caused by technical difficulty while cost continue to increase

Cost Per Yielded mm² for a 250mm² Die

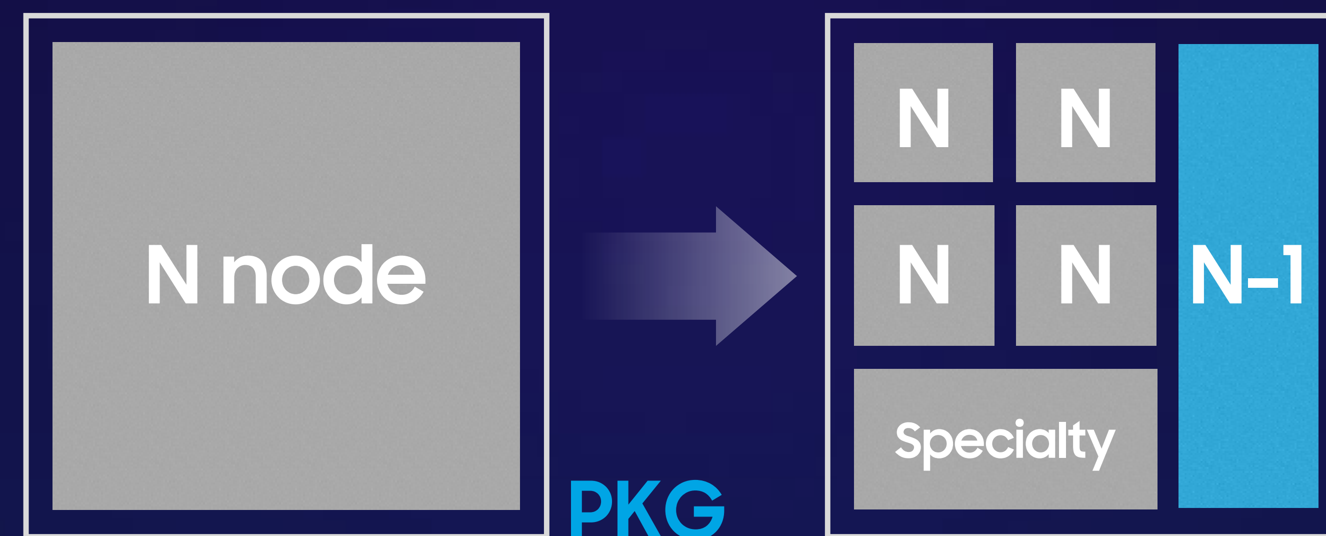


Increasing Die Sizes are Economically Problematic

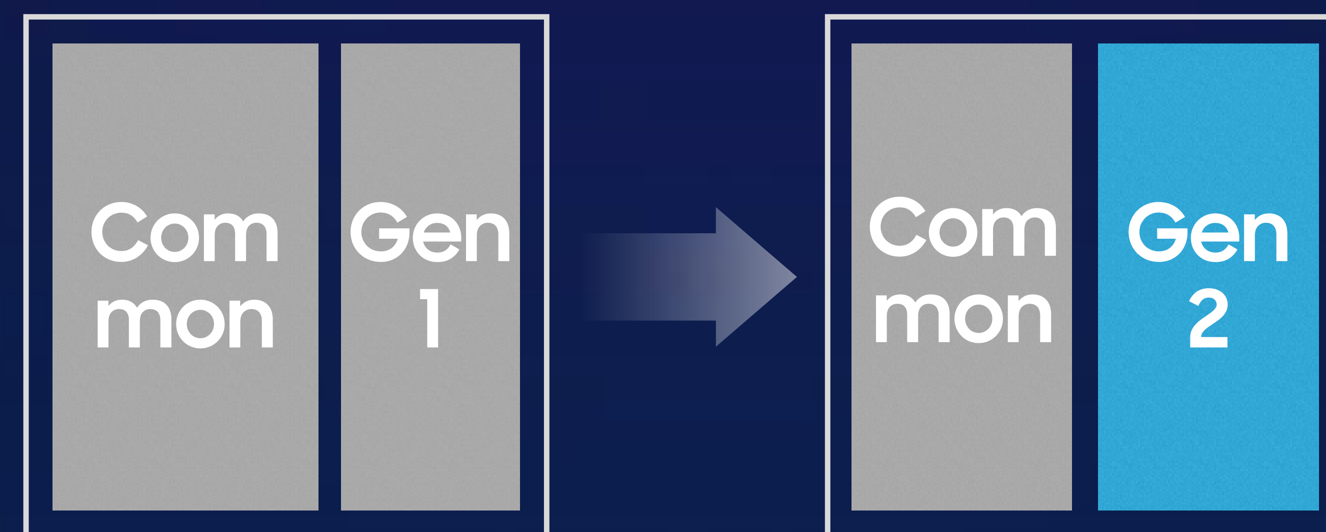
(AMD, Hotchips 2019)

Cost Reduction

High yielding smaller chips & optimal process selection



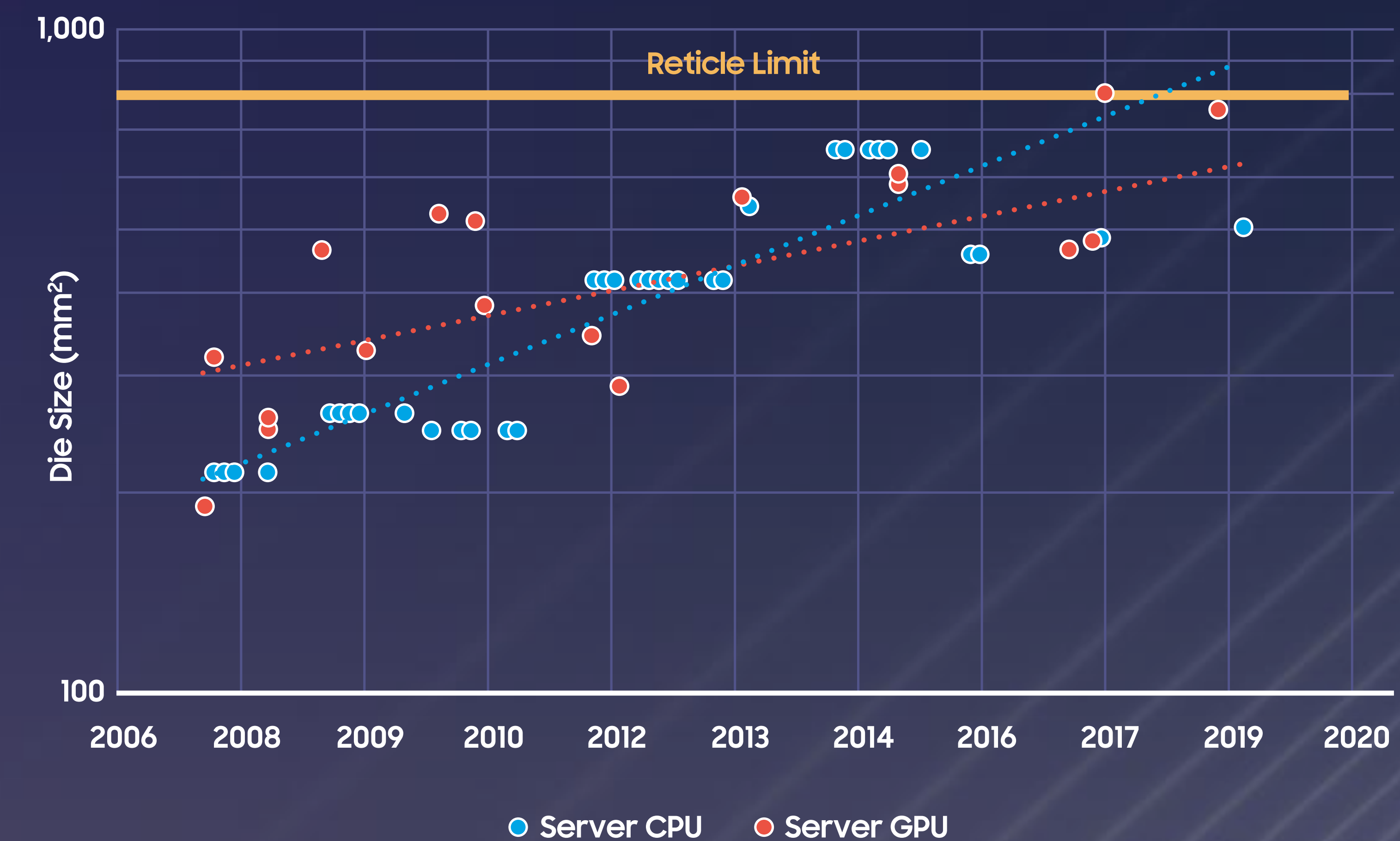
Modular design, design reuse and mix & match



Die Size Challenge

Increases of Die Size due to needs for high performance

Die Size Increases Over Time in Server CPUs and GPUs



Die Size Increasing at an Unsustainable Rate

(AMD, Hotchips 2019)

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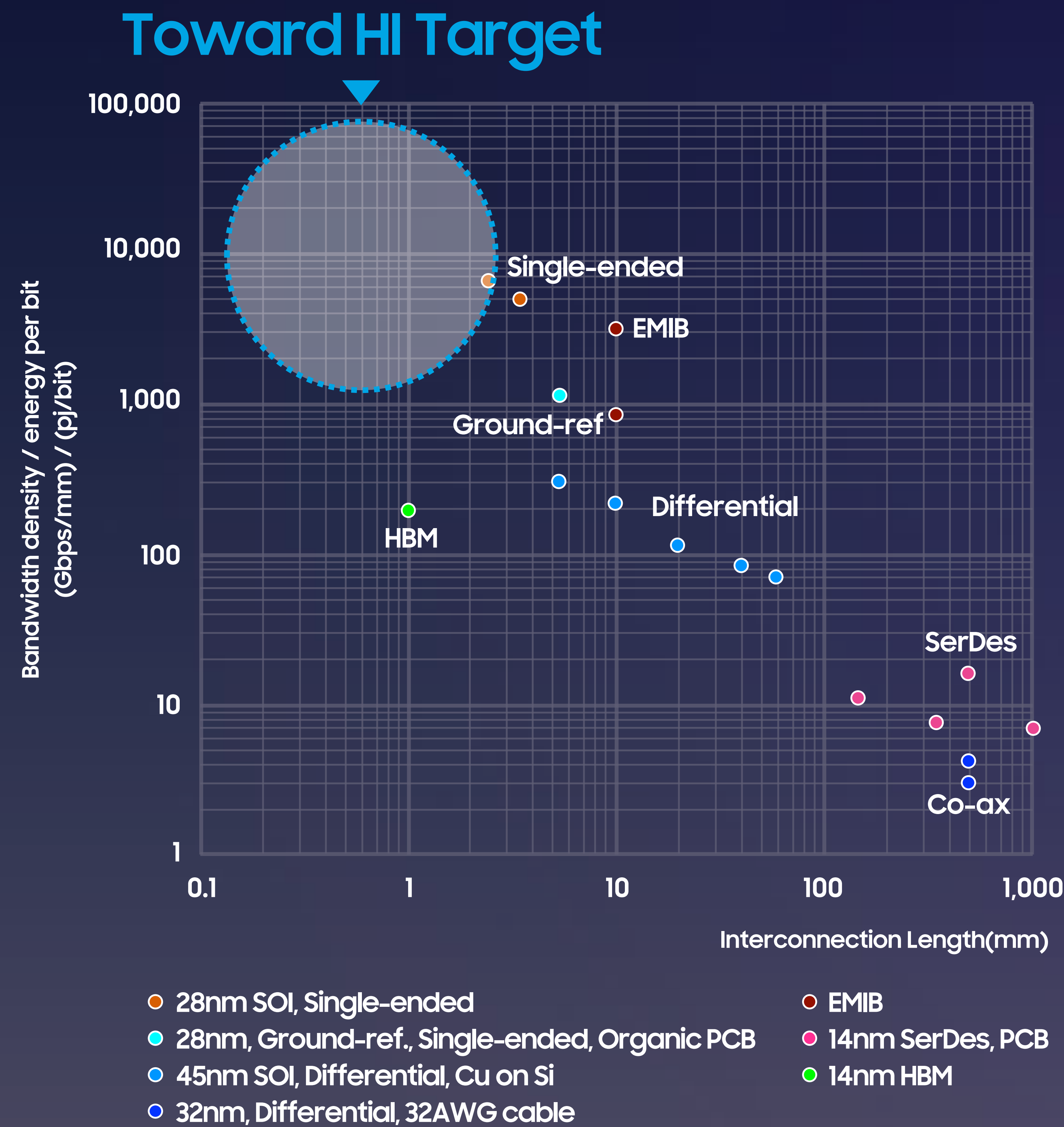
How "Beyond Moore" Can Make it Better

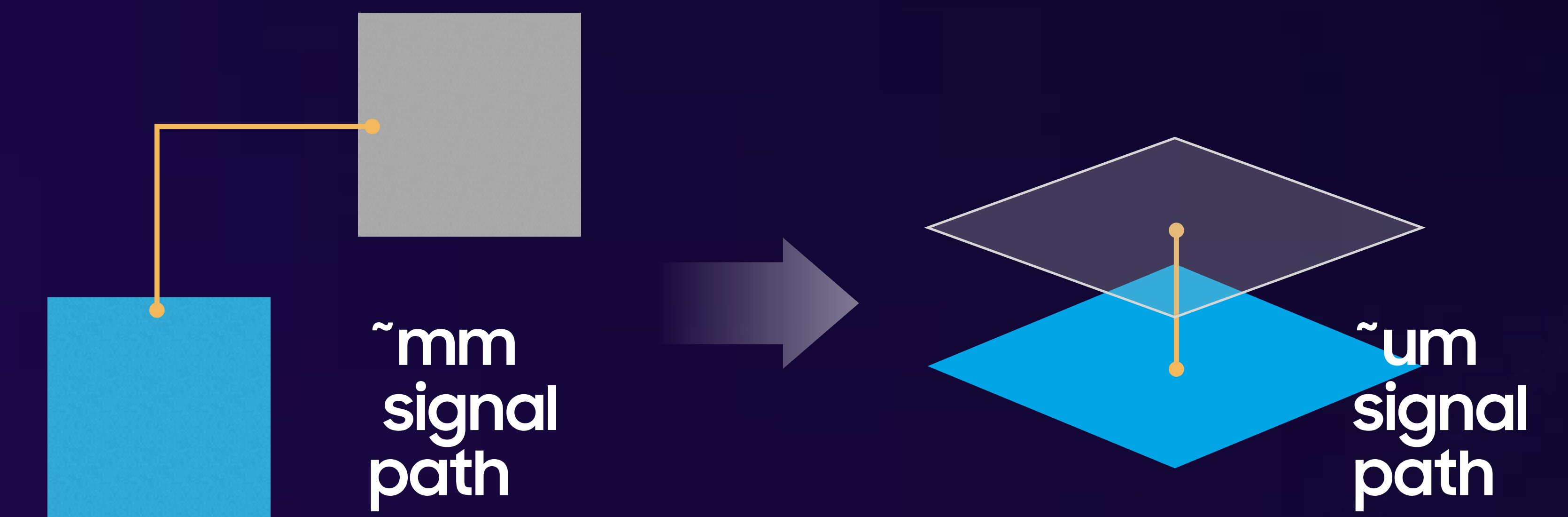
- Heterogeneous integration to mitigate development cost and to improve performance

Inter Chiplets Challenge

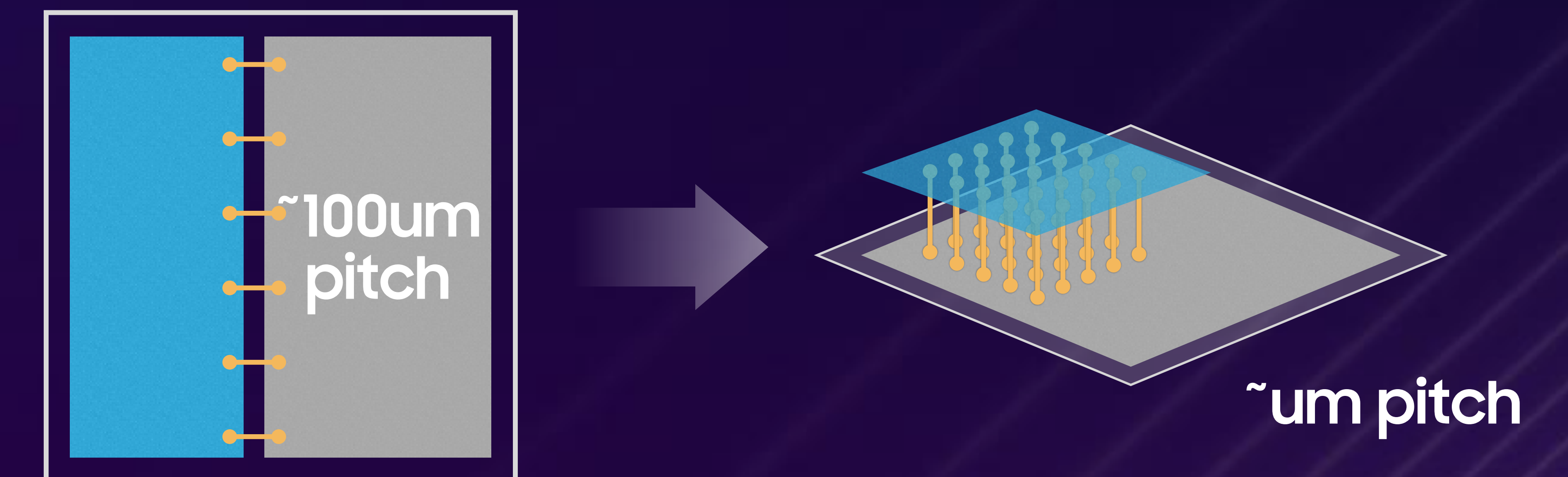


Performance Enhancement

Interconnect path reduction



Fine pitch & massive interconnect



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How "Beyond Moore" Can Make it Better

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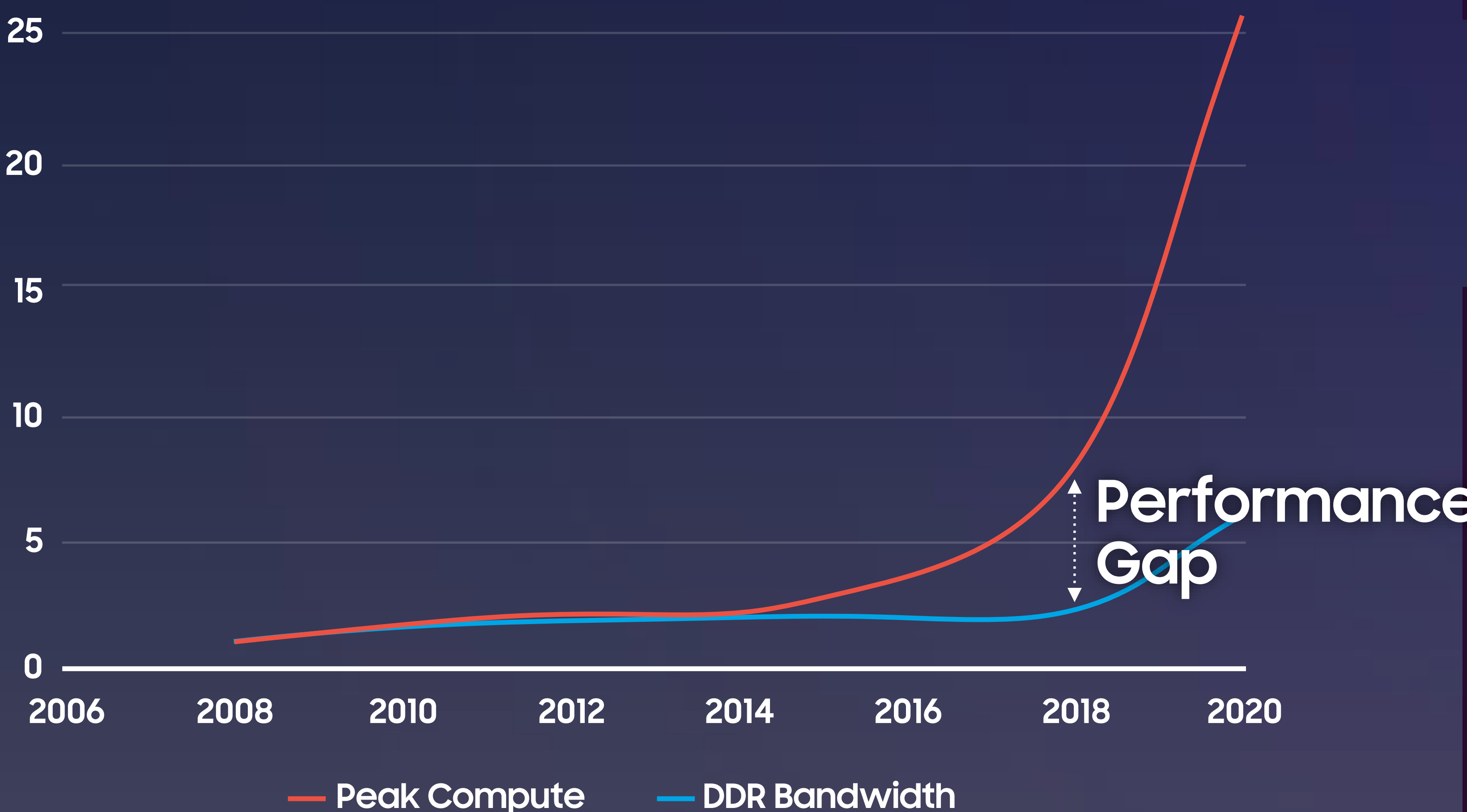
- Heterogeneous integration to mitigate development cost and to improve performance

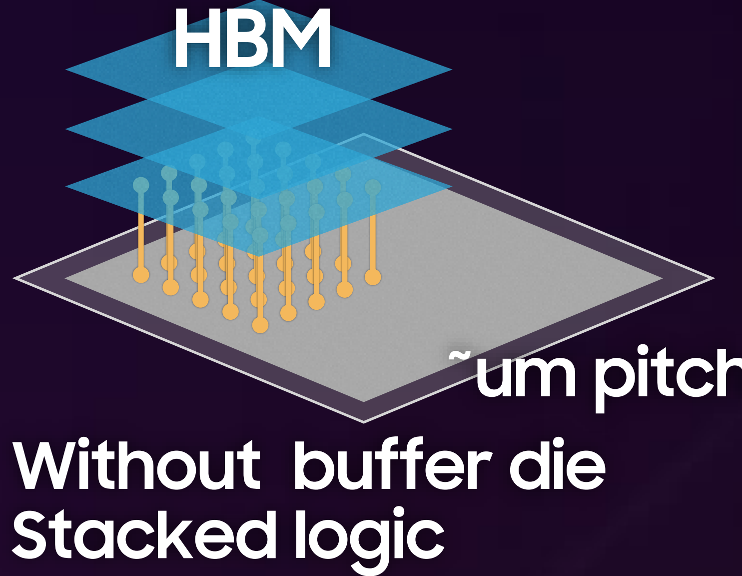
Memory BW Challenge

Bottle-neck of System Performance is Memory Bandwidth



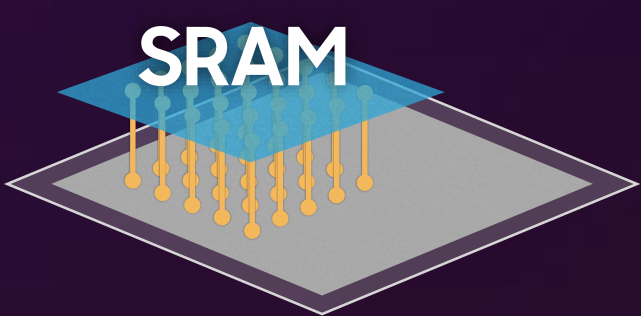
Bandwidth Improvement

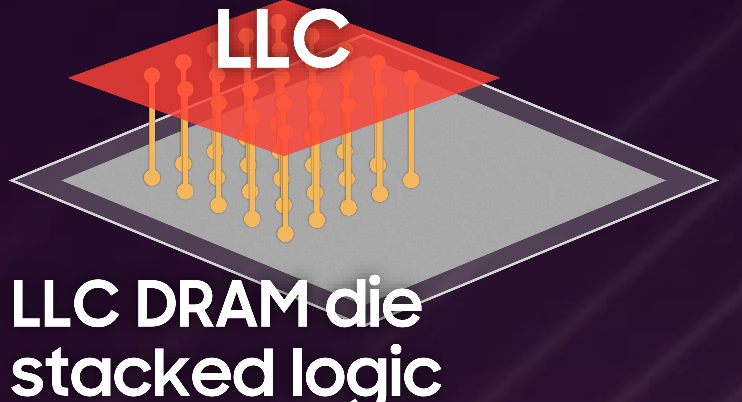
HBM stack on Logic



Without buffer die Stacked logic

High Volume Memory stack





LLC DRAM die stacked logic

* LLC : Last Level Cache design by Samsung

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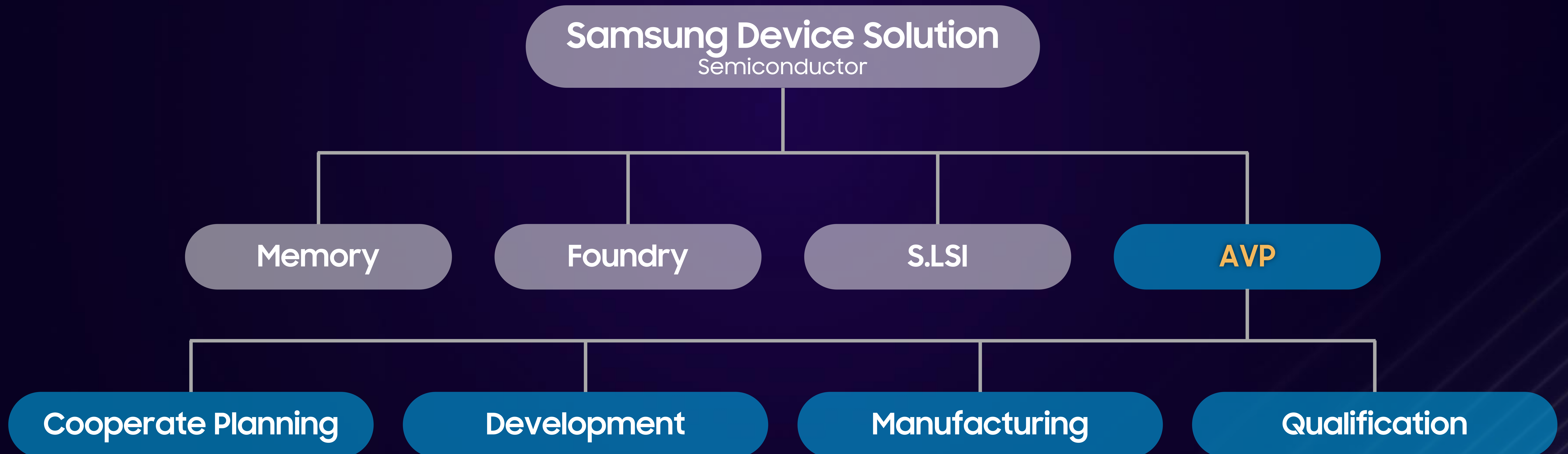
AVP Business Launched

- Launching a new advanced package(AVP) business unit for the increasing importance of Advanced Packaging
- Provides flexible services to customers leveraging Samsung semiconductor's synergy platform



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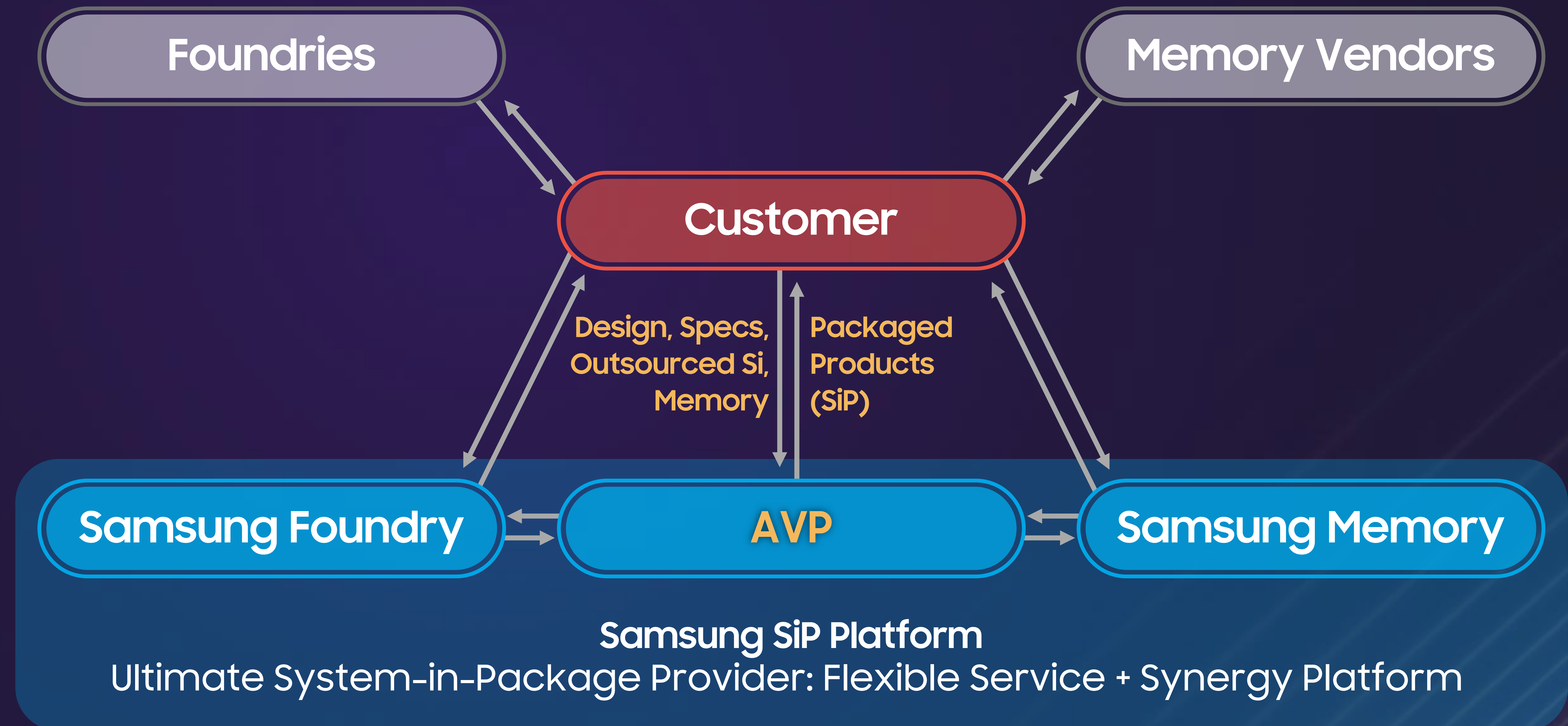
AVP Business Model



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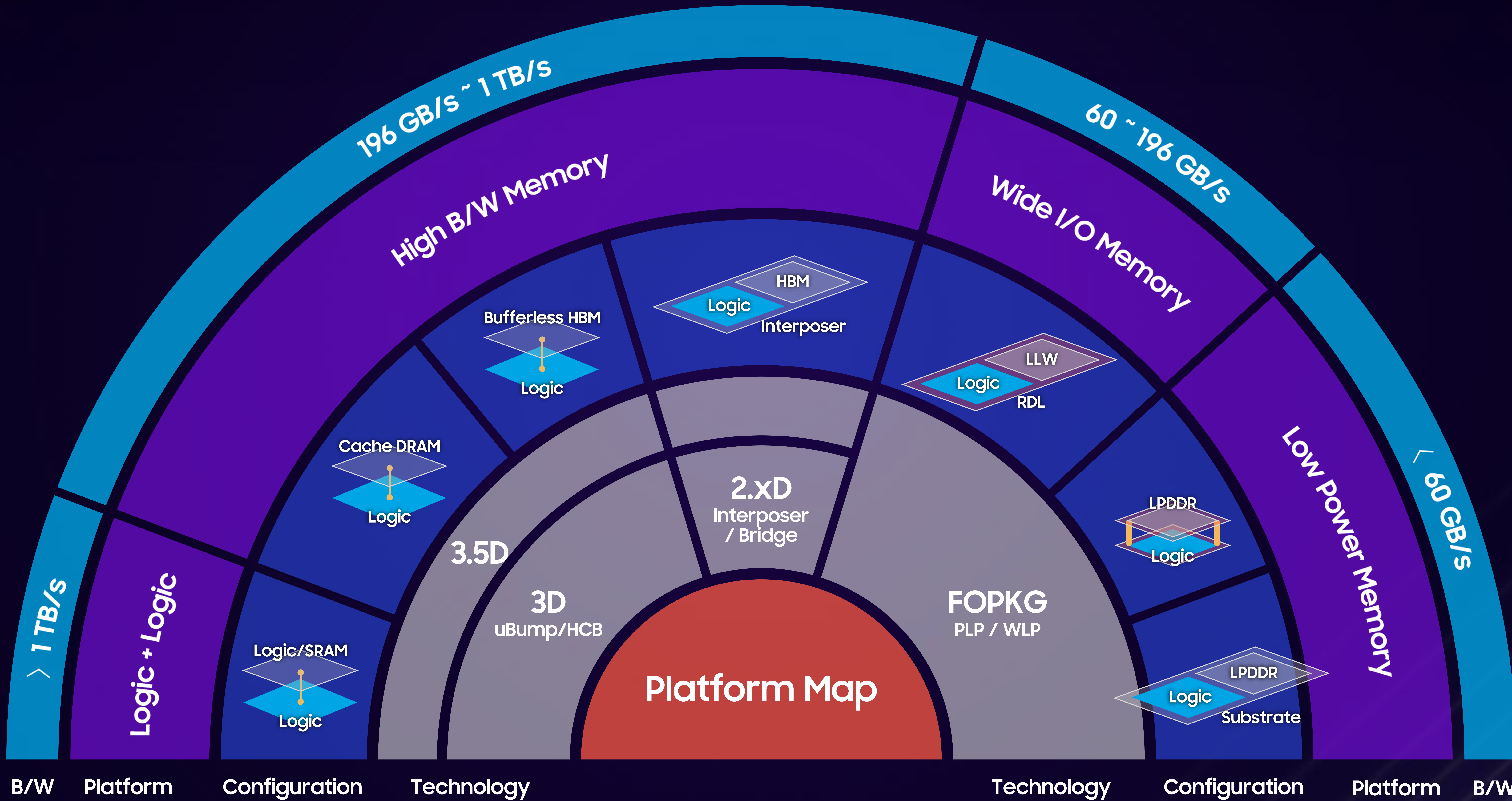
Samsung AVP's Beyond Moore Platform

Samsung AVP Heterogeneous Integration Platform



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Low Power Memory Integration Platform

- Fan-Out Package provides size, thickness and thermal performance benefits

FOPLP

- Enabling smaller form factor with fine pitch interconnection
- Minimizing PKG thickness without substrate
- Enhancing thermal performance with thicker die

FOWLP

Size

Thickness

Thermal Performance

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Low Power Memory Integration Platform Roadmap

- Samsung provides panel and wafer level Fan-Out package solutions

FOPLP

FOWLP

- FOPLP : In Mass Production(Since 2018)
  - PKG Size :14.6 x 14.1mm2 , PKG Height : 0.58mm, Chip T : 0.25mm, L/S : 5/5um, Bump Pitch : 90um
  - Status : Wearable AP(w PMIC, `18~), Premium AP(`22~)
- FOWLP : In Mass Production(`23.4Q)
  - PKG Size : 14.0 x 15.4 mm^2 , PKG Height : 0.47mm, Chip T : 0.21mm
- Technical Roadmap

		Current →			
FO WLP	RDL L/S	2/2um		1/1um	→
	Bump Pitch	90um	≤75um	→	
	PKG Thickness	0.35mm	0.33mm	→	

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Wide I/O Memory Integration Platform

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- LLW DRAM Application : Low Latency, High Bandwidth, and High Power Efficiency Benefits
- RDL based lateral multi-chiplet integration
  - Higher I/O population
    - ▶ **more bandwidth** * 128GB/s(2.0Gbps/pin)
  - TSV-less solution
    - ▶ **Cost competitiveness** * From Si interposer to RDL Interposer or Substrate replace

I/O number

Bandwidth

PKG cost

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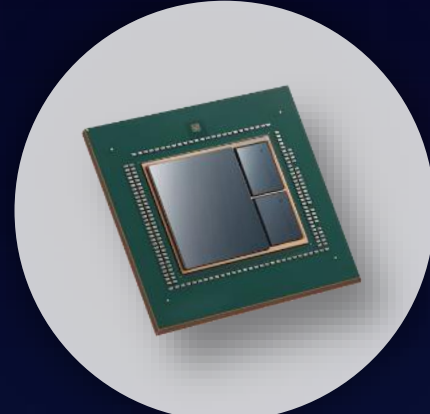
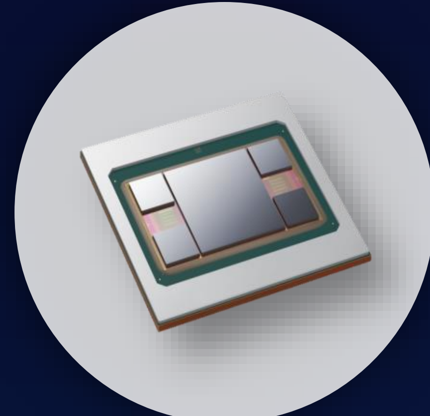
High B/W Memory Integration Platform I

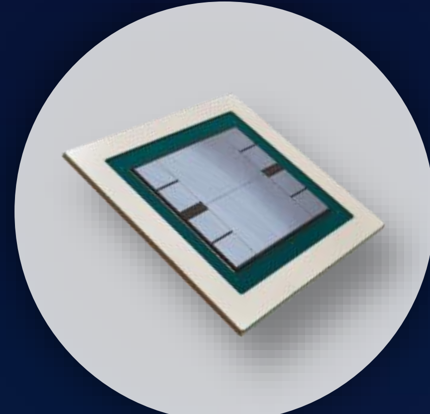
- I-CubeS (Si-Interposer)



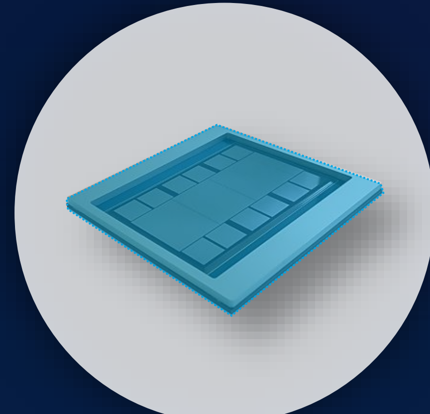
I-Cube2 (2x HBM)



I-Cube4 (4x HBM)



I-Cube8 (8x HBM)



I-Cube12 (12x HBM)*

*To be qualified in 4Q'24

- Horizontal multi-die integration
  - Largest (85x85mm^2) package size
- Ultra high routing & I/O density
  - Fine pitch routing (0.4um/0.4um) & I/O (40um) scalability
- Interposer capable of Integrated Silicon Capacitor (ISC)
  - High power support

Capacity

I/O Density

Bandwidth

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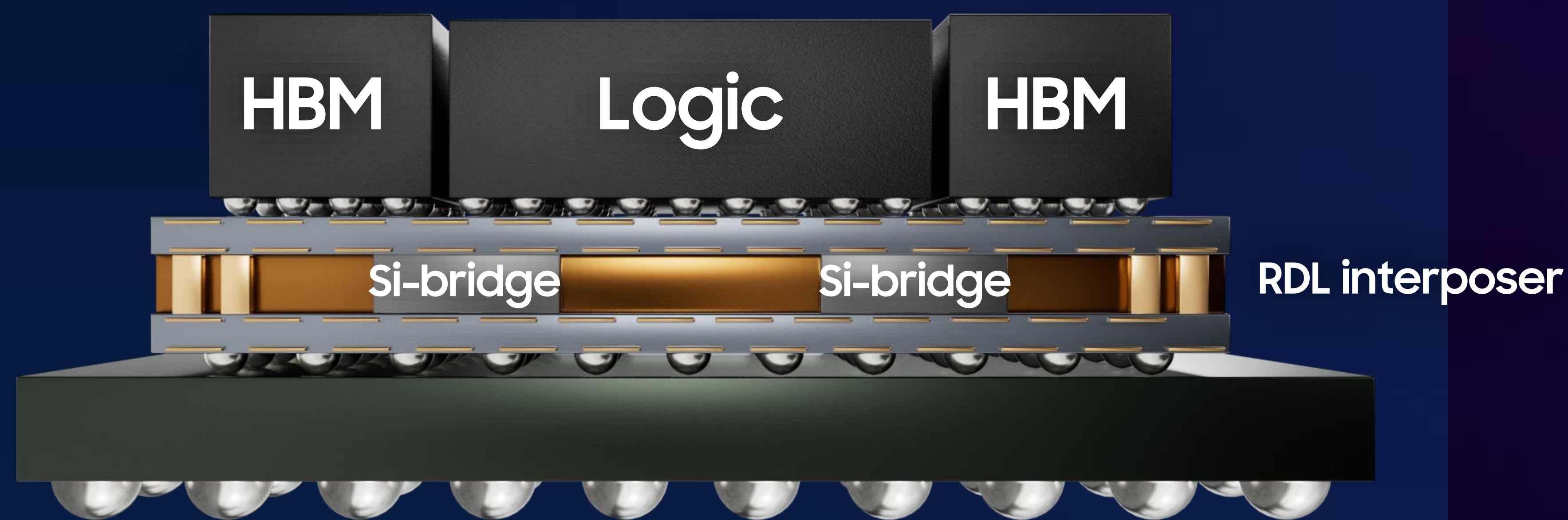
High B/W Memory Integration Platform II

- I-CubeE (Embedded Si-bridge RDL Interposer)



- Cost effective solution
- Enabling larger interposer size
  - Size scalability
- Fine Line/Space by Si-bridge die within RDL interposer
  - Line/Space: 0.4/0.4um(Si-bridge), 5/5um(RDL)

Up to **22%** vs Si-interposer (12x HBM)

Package cost

≥ 4x Reticle

Size expansion

Same vs Si-interposer

Signal/Power Integrity

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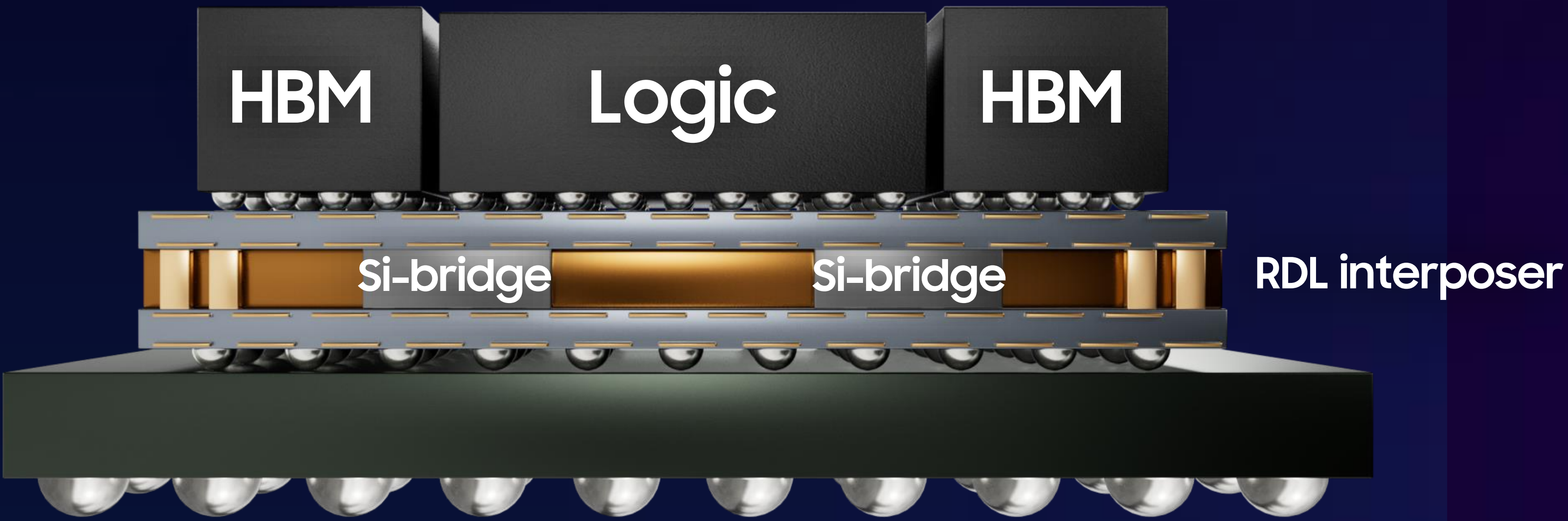
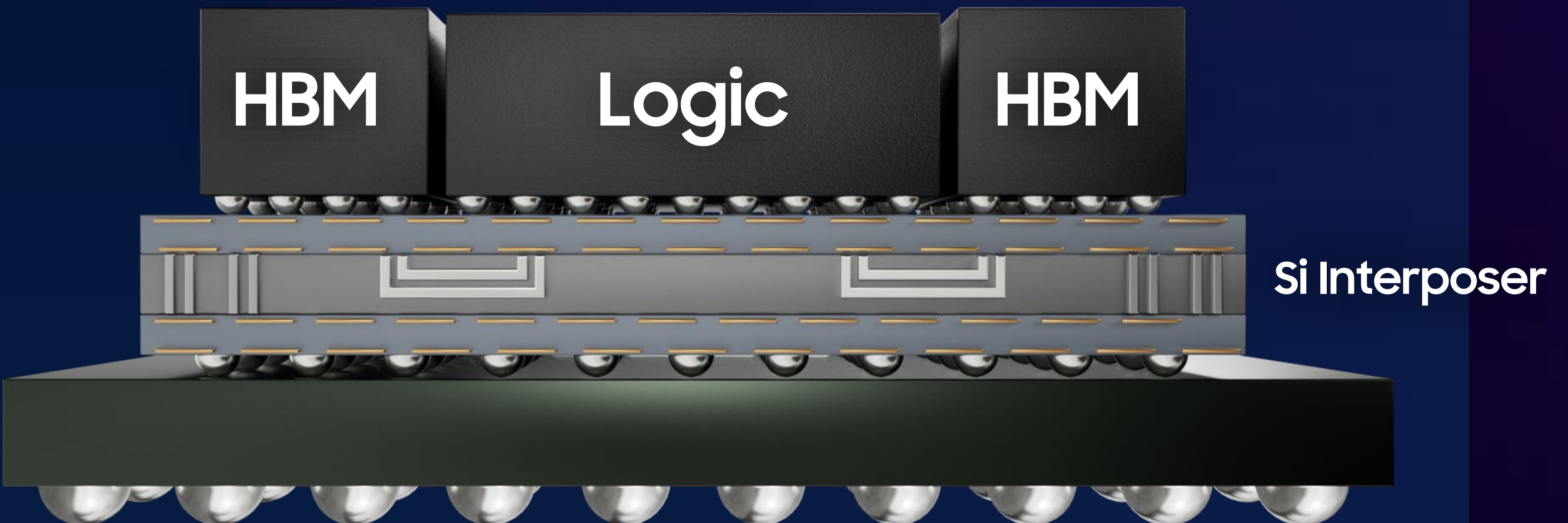
High B/W Memory Integration Platform Roadmap

- I-Cube enables larger interposer, more HBMs and multi-die for AI/Date center applications





		Current		
2.xD	uBump pitch	40um	25um	→
	Interposer size	3x	4x reticle size	→
	Interposer C4 pitch	150um	125um	→
	#of HBM	8x HBM	SOC+12xHBM	→
	Package size	85x85 mm^2	100x100 mm^2	130x130 mm^2

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ISC Solution (Integrated Silicon Capacitor)

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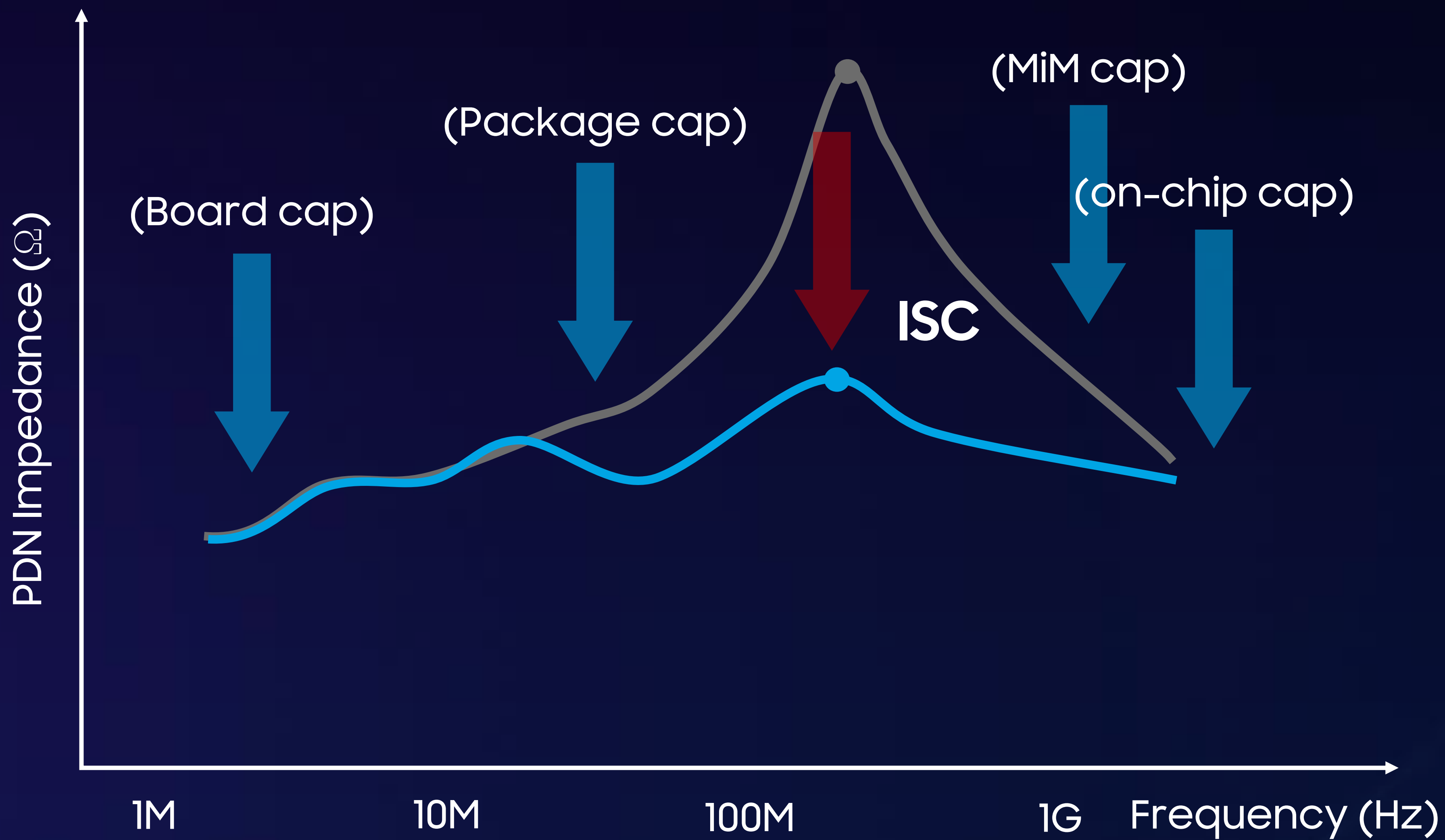
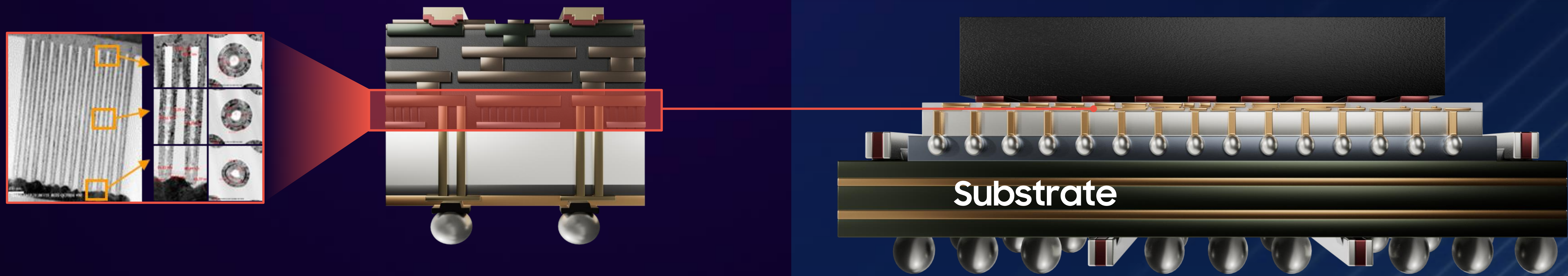
- ISC leads to Decoupling Cap competitiveness in component level
  - PDN improvement : More power noise reduction is possible
  - Low ESL&ESR
  - High Insertion Ratio
- ISC Production ramp-up with Cap density(1,350nF/mm²) in '24 3Q
  - ISC Interposer can be powerful decap solution for 2.5D customers

	Current				
ISC Cap density (nF/mm²)	1,350 ①	2,200 ②	2,750	→	→

① EOT Reduction ② Pitch Reduction





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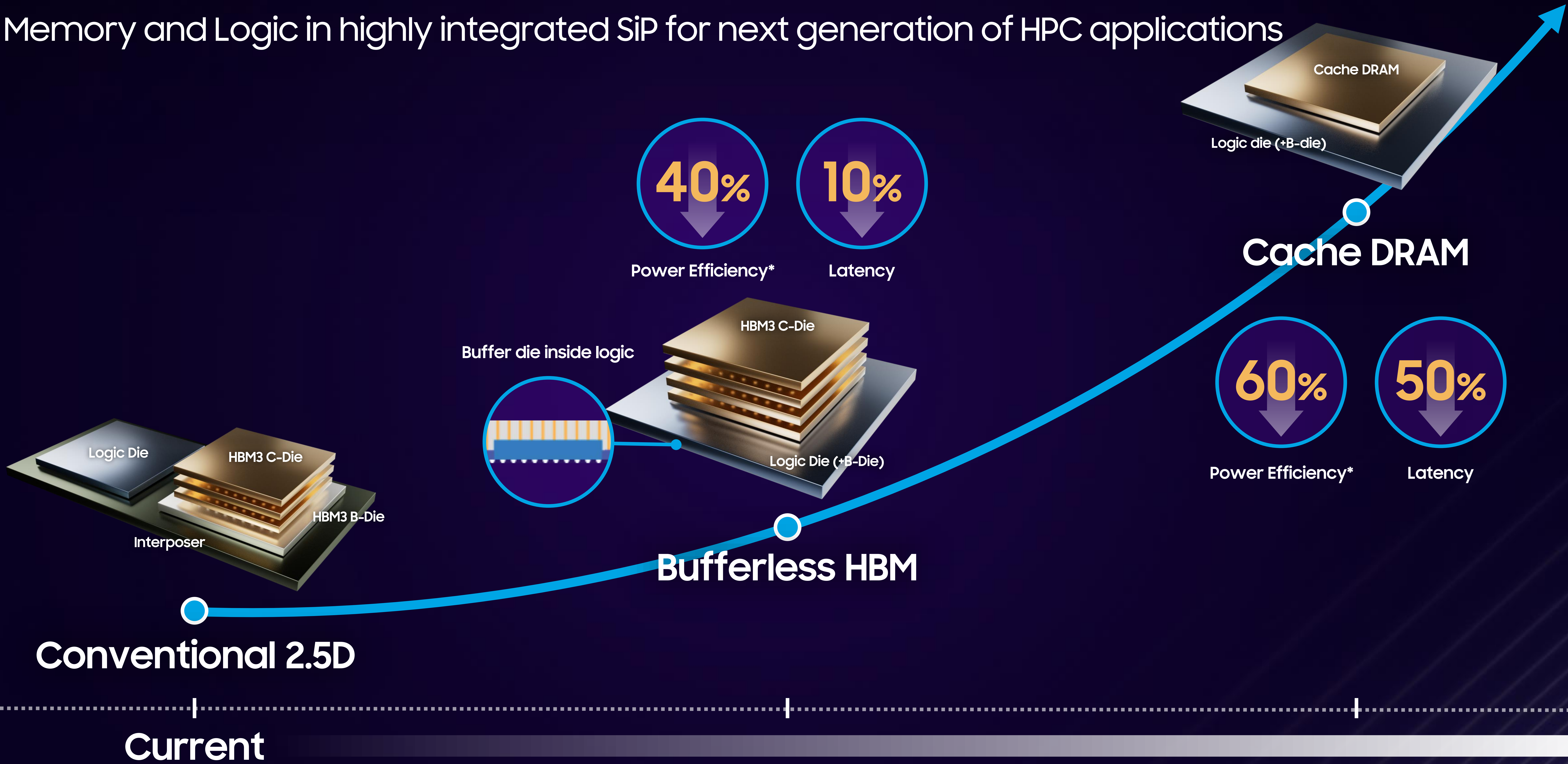
Future High B/W Memory Integration Platform

- Memory and Logic in highly integrated SiP for next generation of HPC applications



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Logic 3D IC Platform

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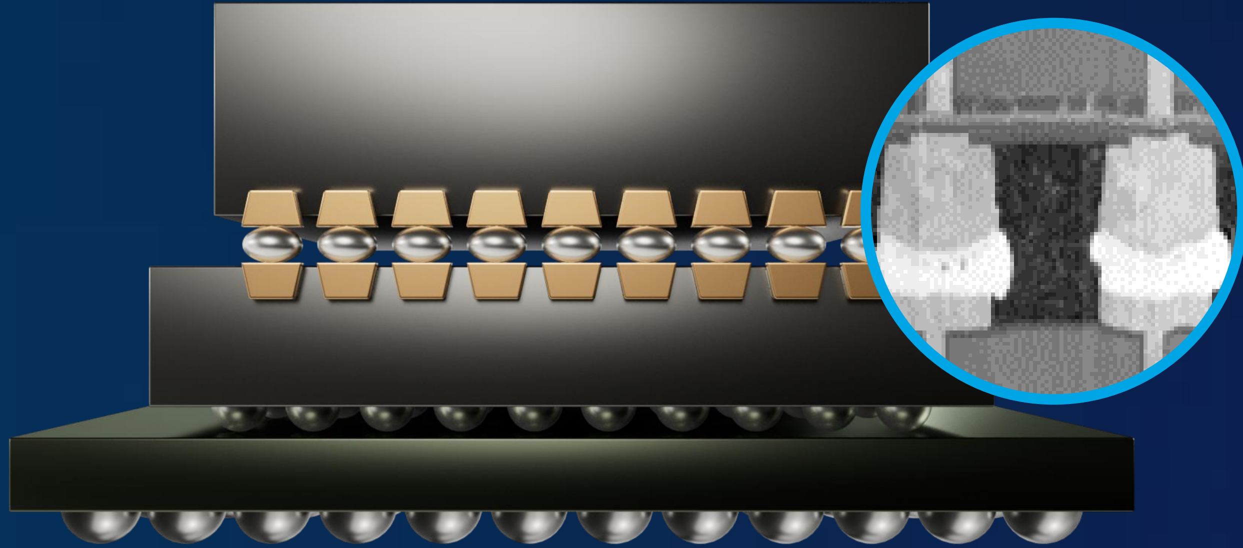
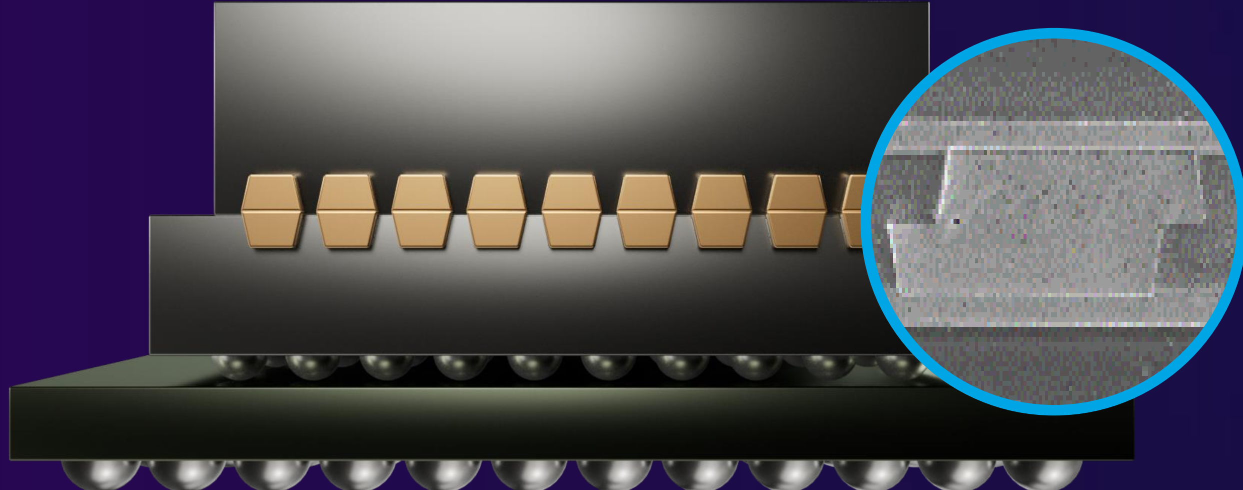
µBump(TCB)

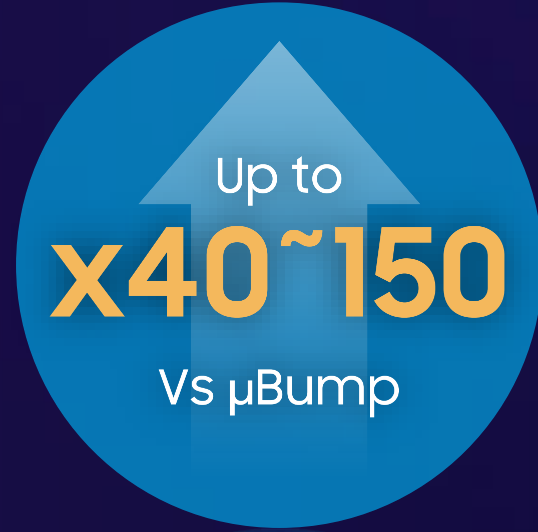


- In Mass Production (Since 2016)
  - A few tens of millions(HBM)
- Lower cost than HCB

Bumpless(HCB)



- Higher interconnection density (Bumpless HCB)
  - Bandwidth & Thermal gains



Bandwidth

Allowable Power

- Vertical stacking format (Die disaggregation)
  - Smaller Footprint (Die placement area)

Foot Print

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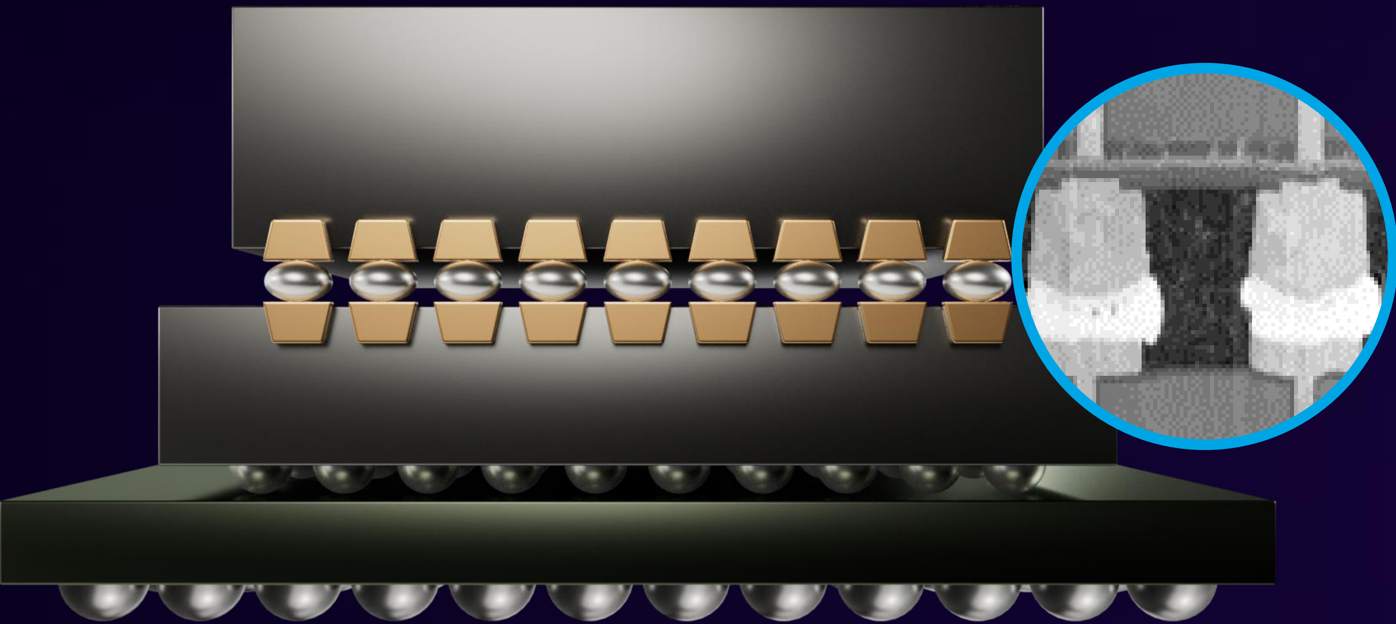
Logic 3D IC Platform Roadmap

- X-cube can integrate any configurations of logic-logic stacking optimized for performance

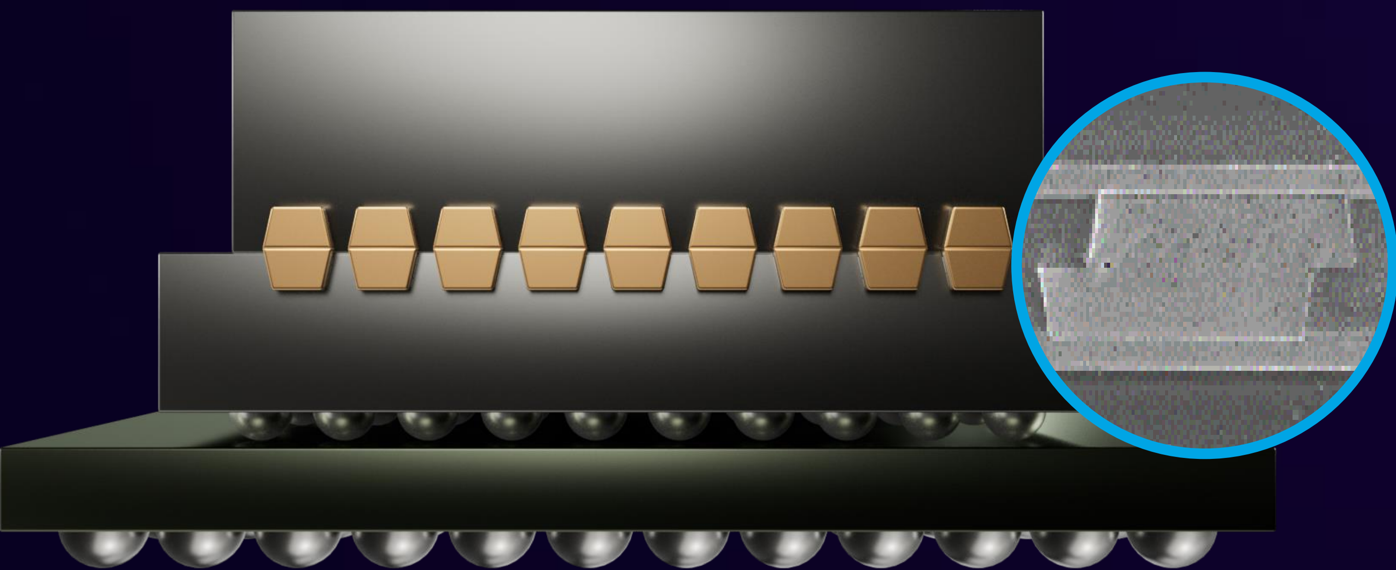
µBump(TCB)



		Current →		
TCB	Bump Pitch	25 um	21 um	<21um
	IO density	1,600 Bump/mm^2	2,260 Bump/mm^2	>2,260 Bump/mm^2
	Silicon Thickness	40um	<40um	
	Mass Product.		AP, XR	TBD

※ '16, HBM2 & '18, CIS-3Stack MP

Bumpless(HCB)



		Current →		
HCB	PAD Pitch	4um	3um	≤ 2um
	IO density	62,5K PAD/mm^2	110K	>250K
	Silicon Thickness	10um	<10um	
	Mass Product.		HBM4	AP

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Technical Challenges

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Technical Challenges, PSI(Power and Signal Integrity)

- PSI Challenges in Heterogeneous Integration

1 IR Drop

V_{dd}

IR drop allowed level

Excessive drop

2 Jitter Noise by Power Noise

V_{ddq}

w/o power noise

w/ power noise

3 Signal Degradation

S21

Signal loss

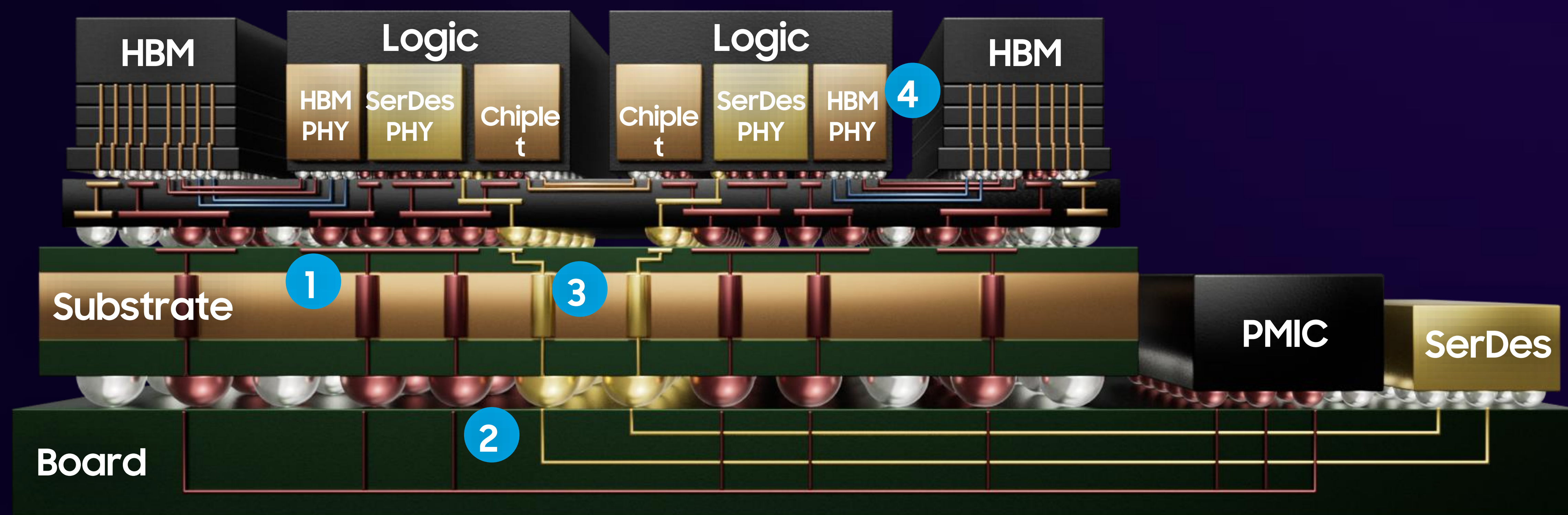
Freq

4 Crosstalk Noise

Aggressors

Xtalk

Victims



Power Integrity Challenges

- IR Drop by High-Power Logic Operation(>1kW)
- Jitter Noise due to Power Coupling Noise
  - ▶ Solution: Integrated Silicon Cap, Integrated VR

Signal Integrity Challenges

- Signal Degradation for Higher Speed IP (SerDes 112Gbps)
- Crosstalk Noise by Design Complexity
  - ▶ Solution: Design Methodology, Low-loss Material

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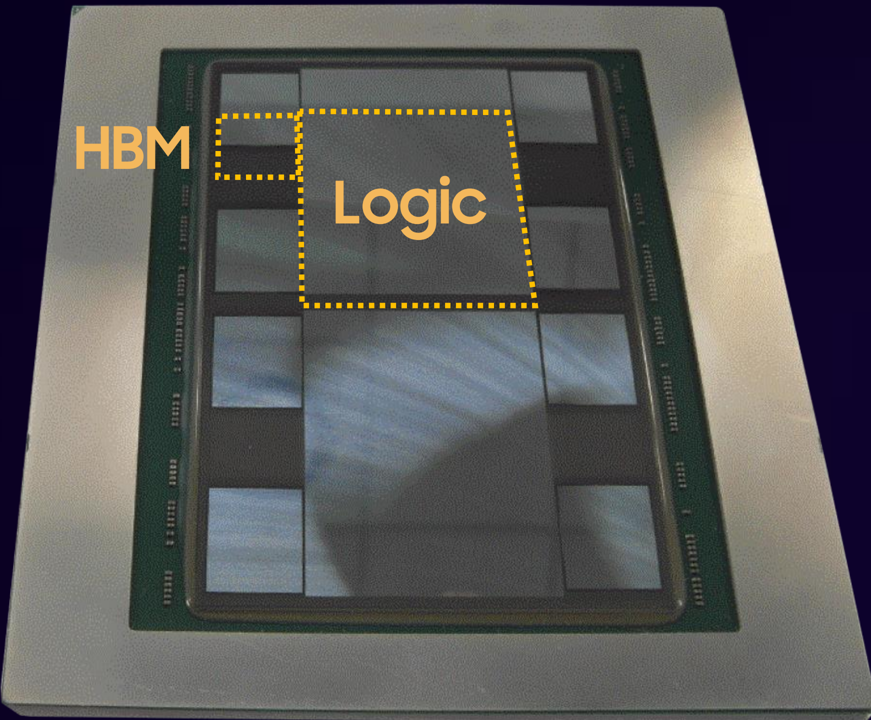
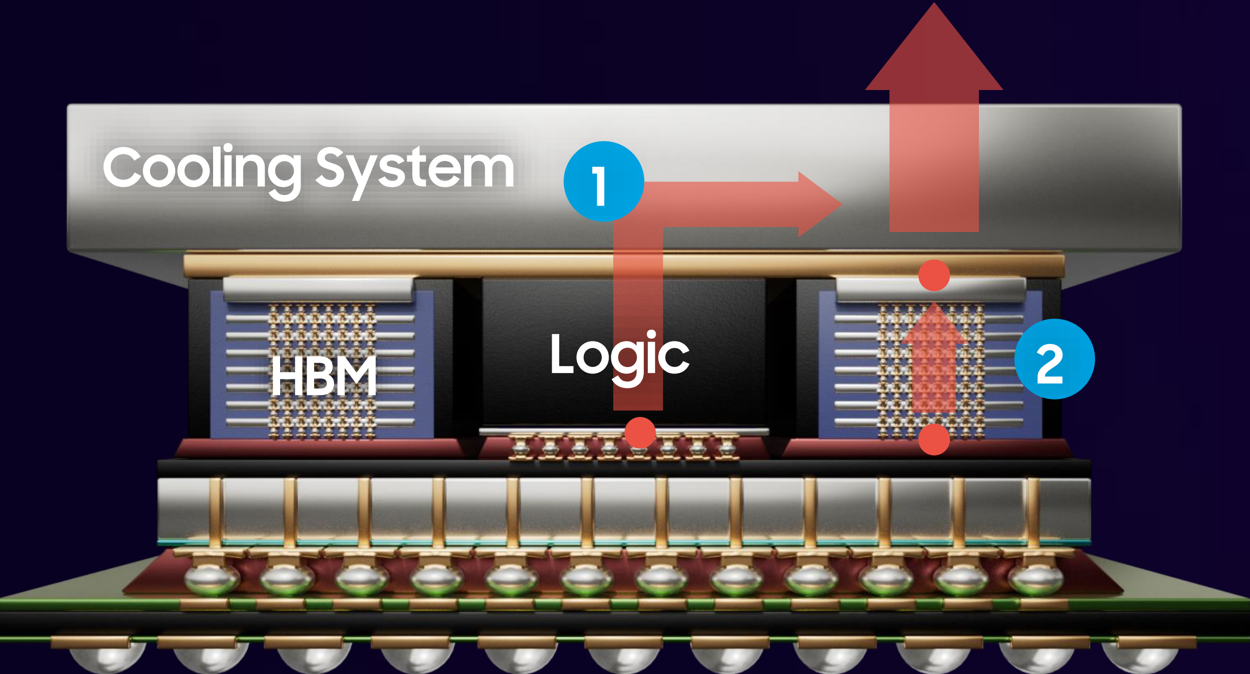
Technical Challenges, Thermal Congestion Issue

- Thermal Management Challenges in Heterogeneous Integration



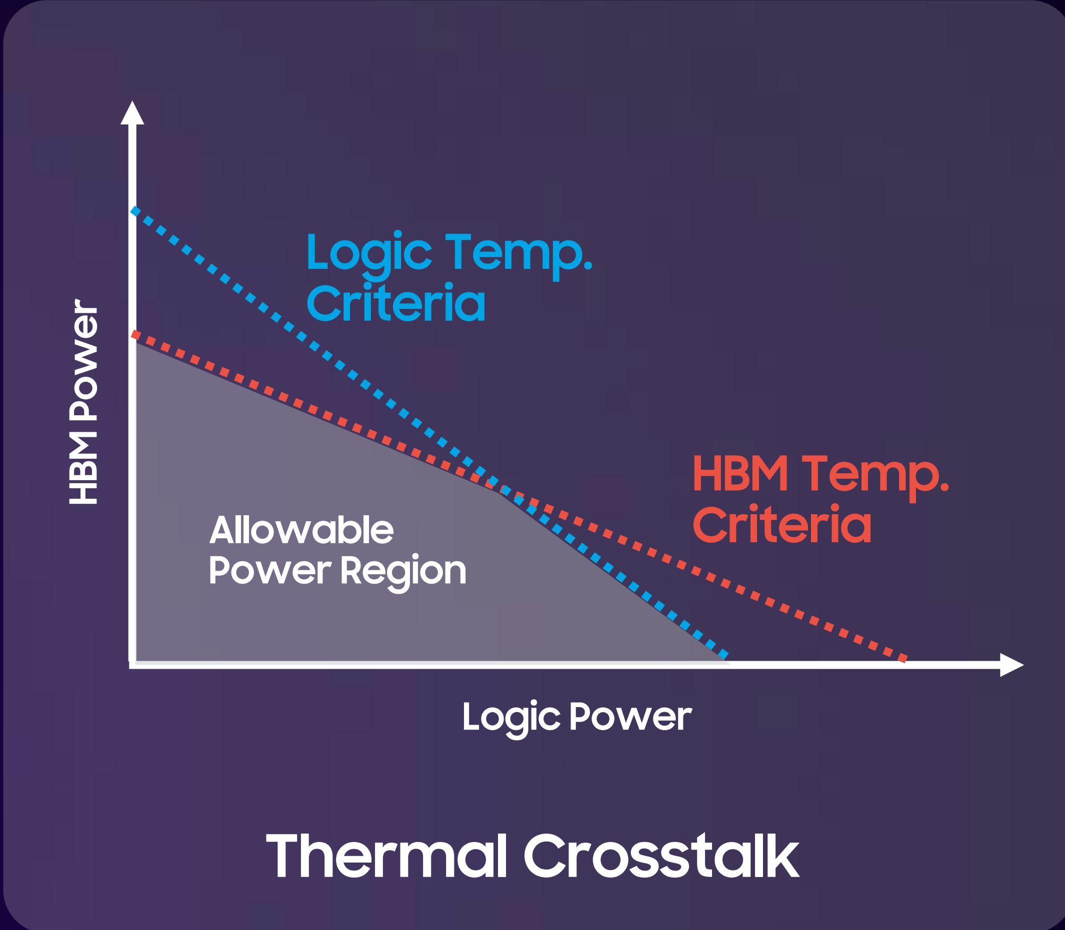
2.5D PKG



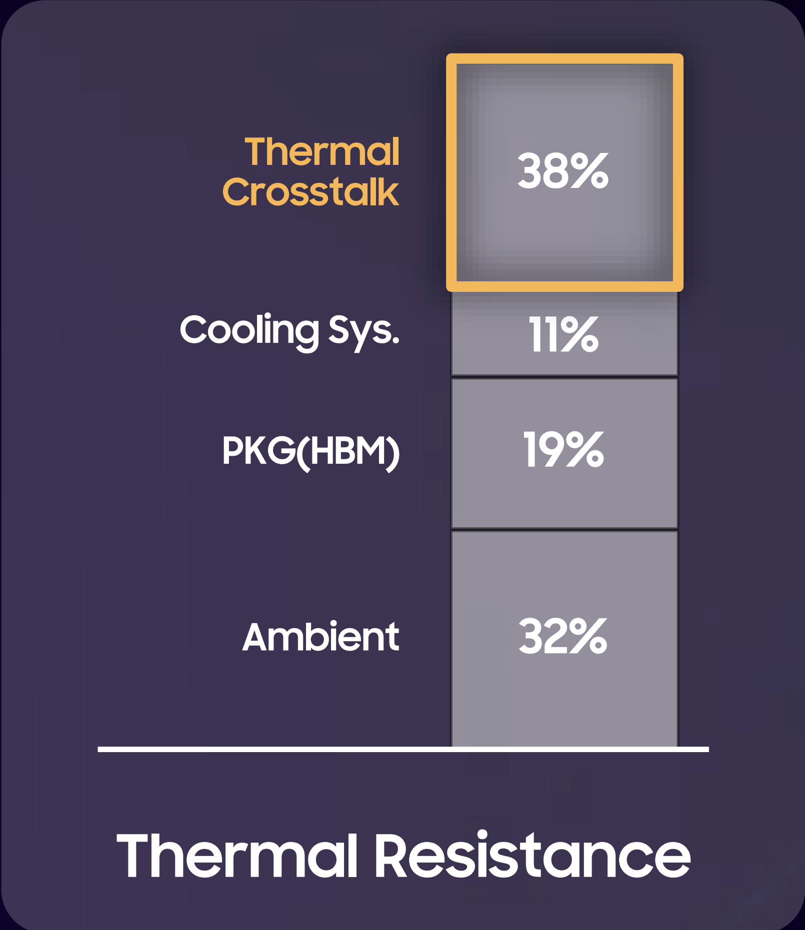
1. Thermal Crosstalk
2. Accumulated Heat Flow in 3D-IC

Multi-Chip Implementation

- Different Thermal Limits
  : Logic Die vs Memory Die
- Thermal Crosstalk
  - ▶ Solution: Thermal Aware Design



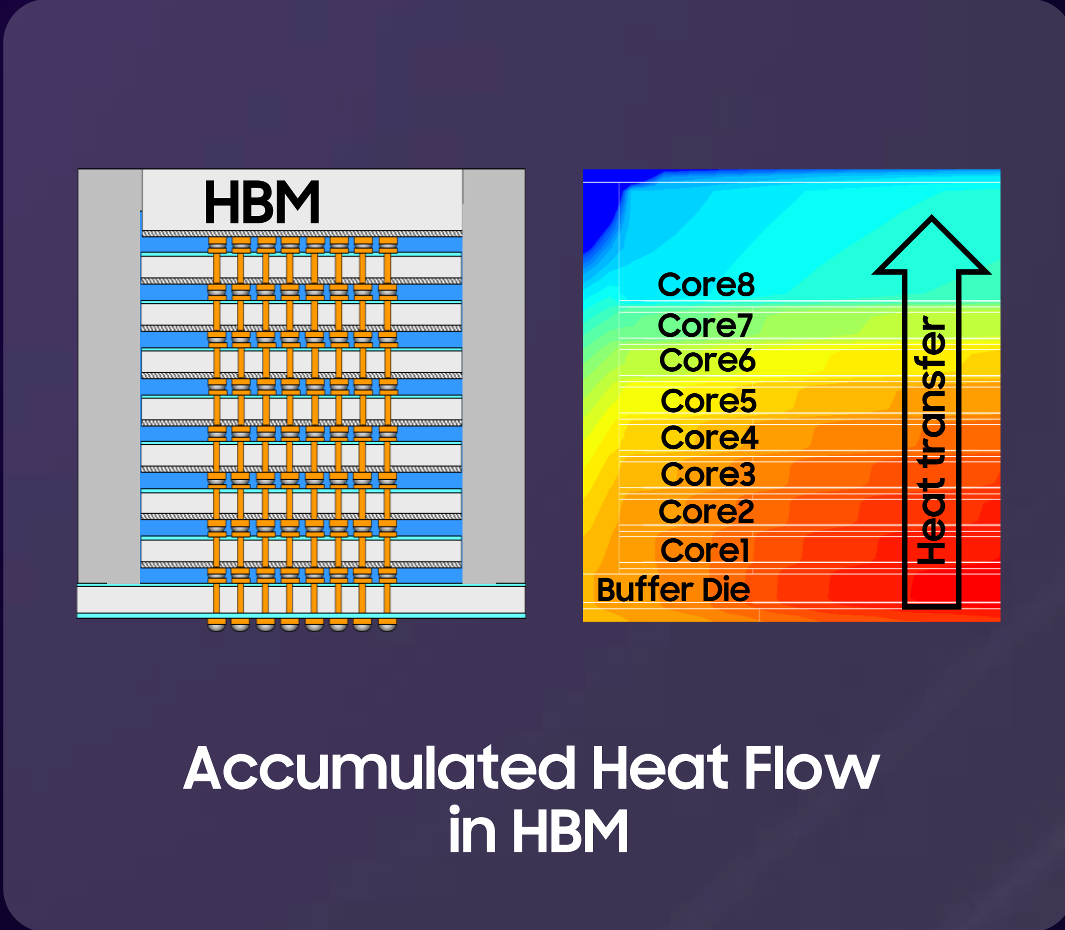
Thermal Crosstalk



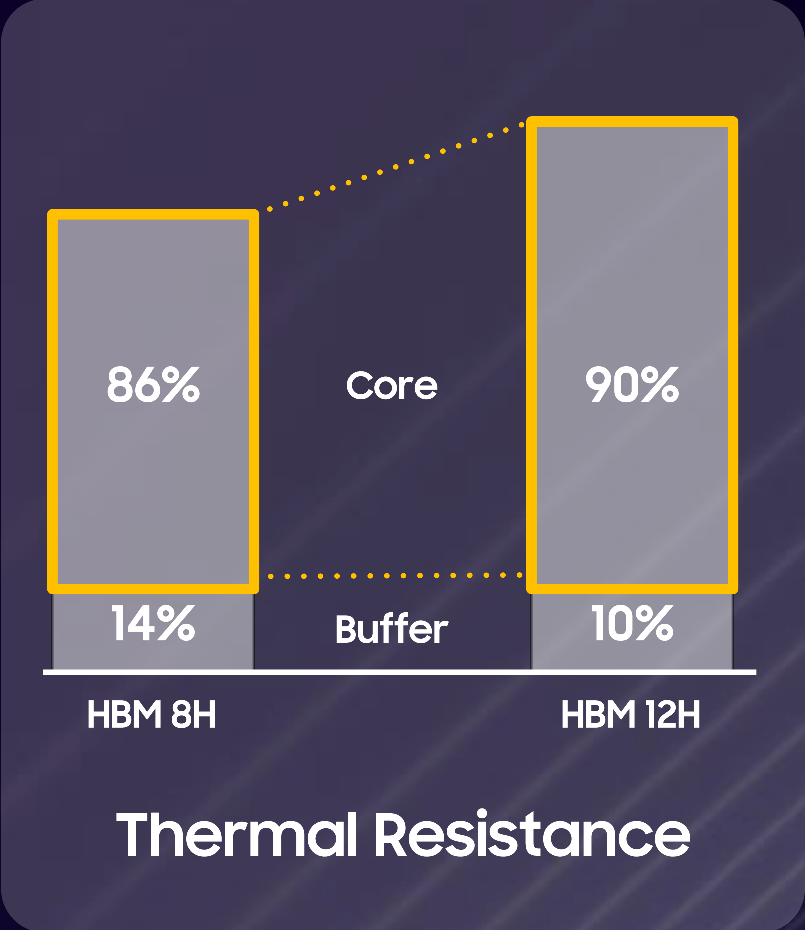
Thermal Resistance

3D Multi Stack Implementation

- Accumulated Resistance
- Accumulated Heat
  - ▶ Solution: Joint Thermal Enhancement, Thermal Aware Design



Accumulated Heat Flow in HBM



Thermal Resistance

Heterogeneous Integration Eco System

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Heterogeneous Integration Eco System

- Collaboration between Partners' Specialty & Samsung AVP's HI Platform to overcome the rising challenges of semiconductor

EDA Design methodology

cadence, SYNOPSYS

P&R, PEX, PSI, STA, DFT

ANSYS — IR-Drop, EM

SIEMENS — Verification

Chiplet IF Including memory

UCIe, JEDEC, SAMSUNG Foundry, cadence, SYNOPSYS

OSAT Cooperation

Amkor Technology, ASE GROUP, JCET, nepes

PCB & More Supply Chain

IBIDEN, KYOCERA, SAMSUNG ELECTRO-MECHANICS, SHINKO, TOPPAN

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Thank you

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