Hetero Integration Development - Interdisciplinary Innovations

Xin Wu, Corporate Vice President, Silicon Technology
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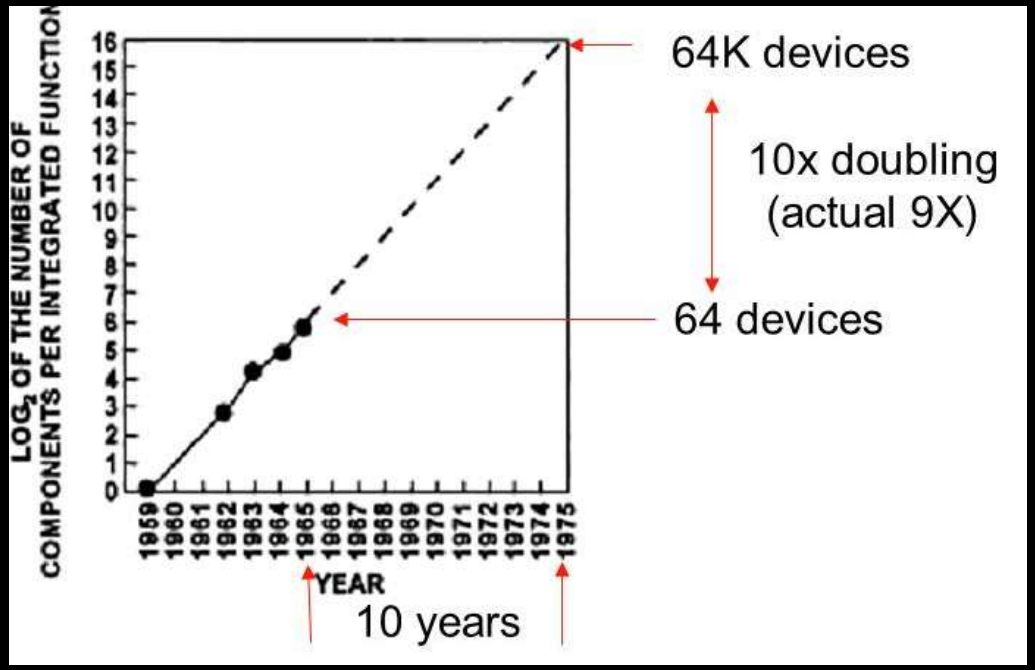
AMD
together we advance_

Moore's Law

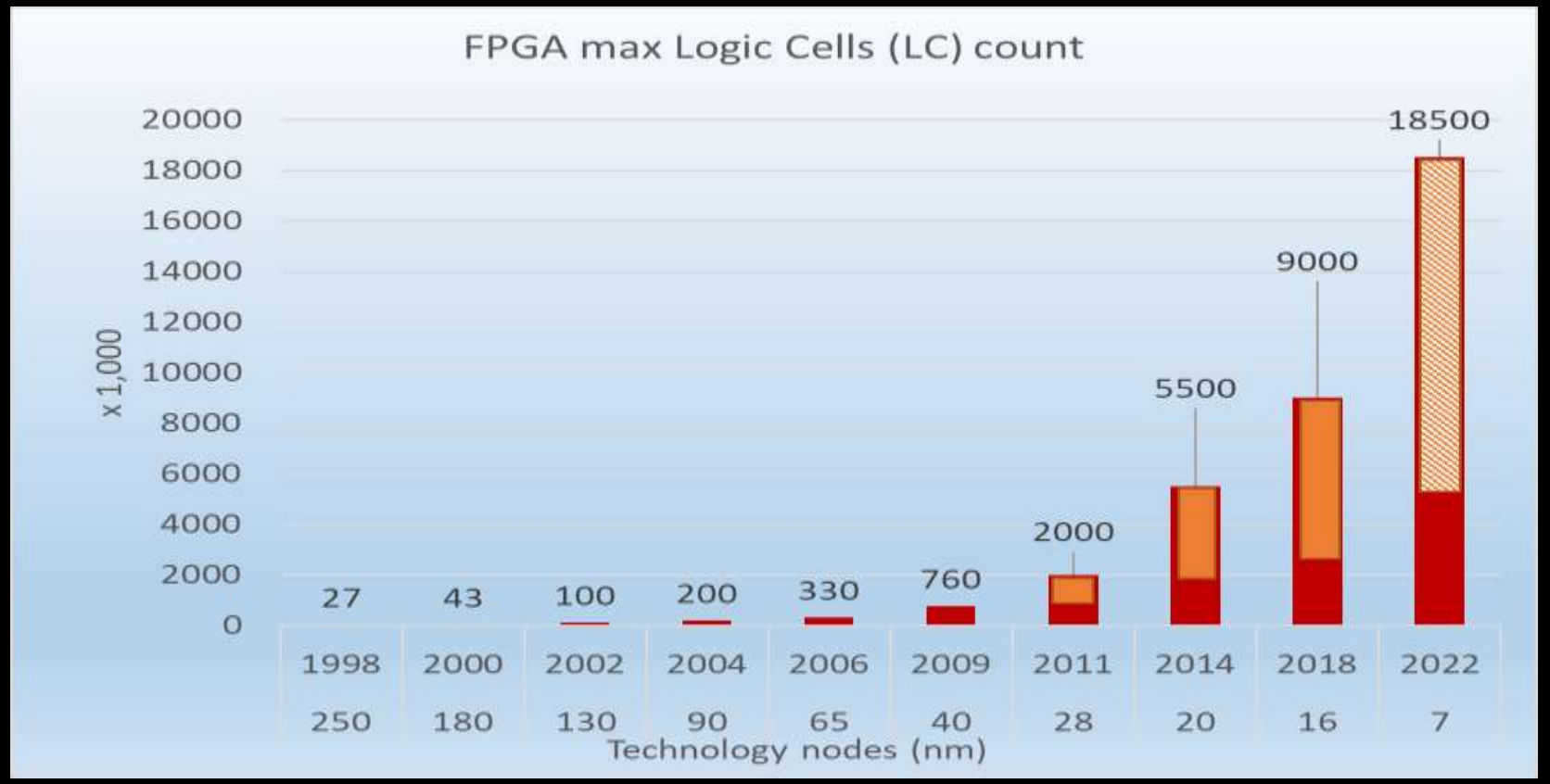
- In 1965, Moore observed that transistor density doubles every year
- Revised in 1975: transistor density doubles every two years



Source: "Cramming more components onto integrated circuits"
Gordon Moore, Electronics, Volume 38, Number 8, April 1965

Moore's Law was designed to rebut contemporary claims that integrated circuits were *expensive* and *unreliable*

FPGAs Then and Now

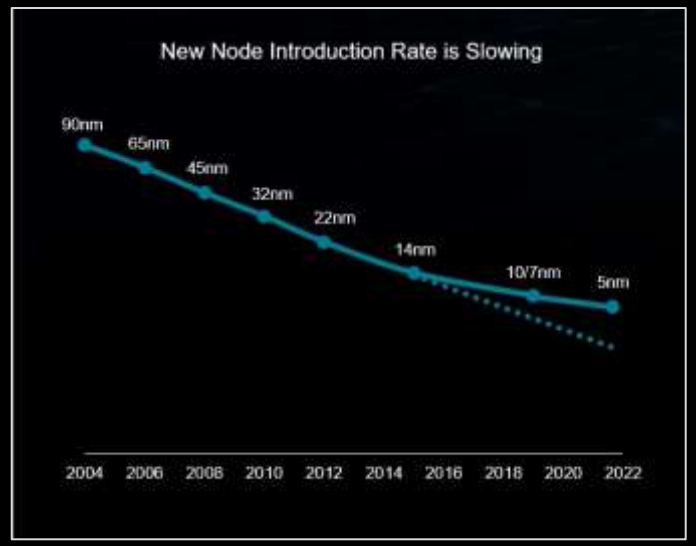


FPGA capacity grew ~680x in 10 nodes, benefiting from Moore's Law, hetero-integration, packaging and many new technologies

Source: H. Liu (AMD), "Challenges for Next Gen Advanced Packaging and Heterogeneous Integration," Annual EPoSS Forum, Oct. 2022

CMOS Technology Roadmap

- Moore's law has slowed down significantly
- Need expensive solutions to keep Moore's law alive
  - Gate-All-Around, EUV double patterning, SiGe channel, etc.
  - Node-to-node mask/wafer cost increase can be > 30%
  - High design cost for new technology nodes
- Advanced packaging & 3D integration can provide new opportunities



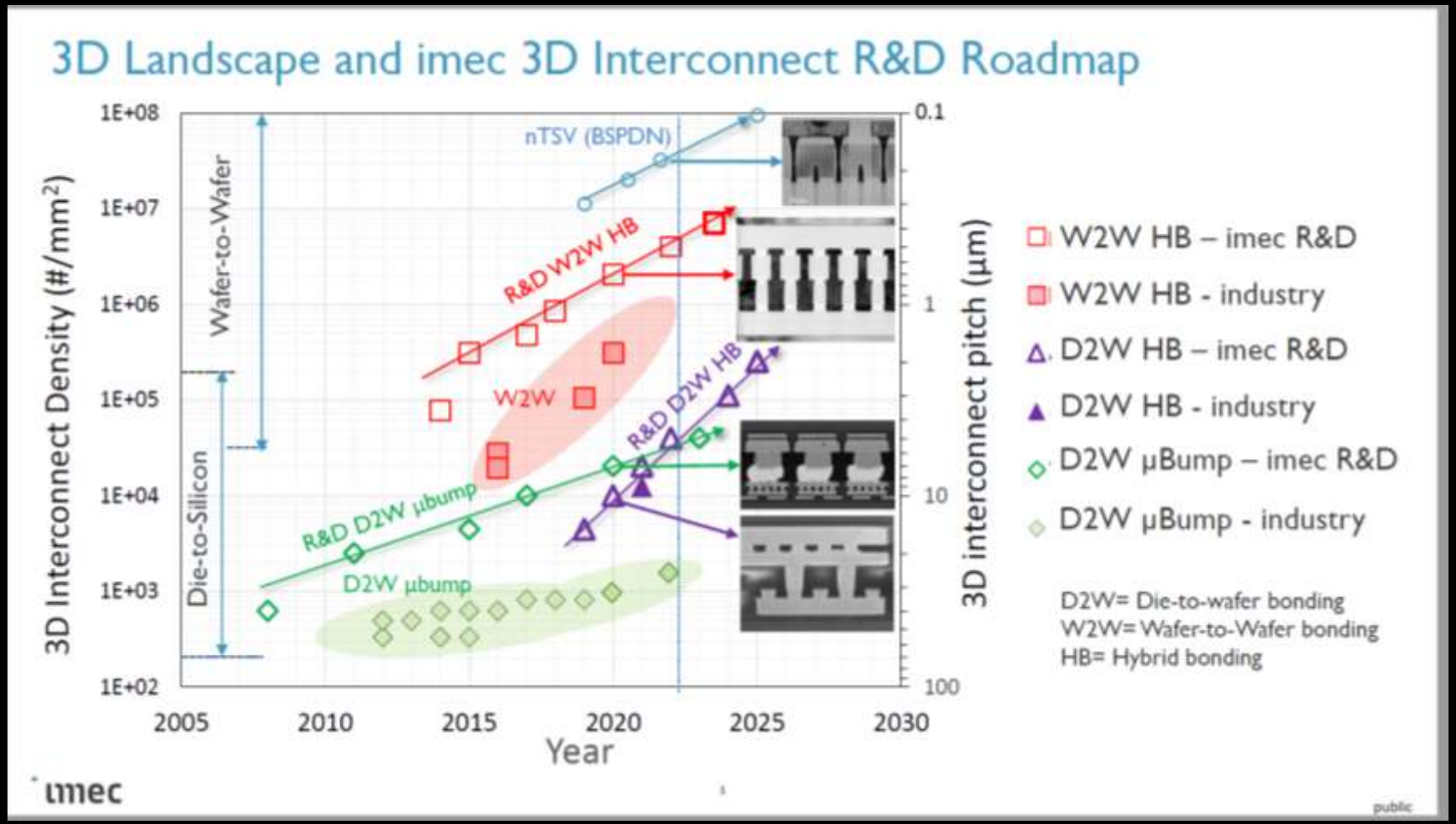
YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4	G38M16/T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
LOGIC TECHNOLOGY ANCHORS						
Device technology inflection	Taller fin	LGAA	CFET-SRAM	Low-Temp Device	Low-Temp Device	Low-Temp Device
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV
Beyond-CMOS as complimentary to platform CMOS	-	-	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	SiGe50%	SiGe60%	SiGe70%	SiGe70%, Ge	2D Mat	2D Mat
Local interconnect inflection	Self-Aligned Vias	Backside Rail	Backside Rail	Tier-to-tier Via	Tier-to-tier Via	Tier-to-tier Via
Process technology inflection	Channel, RMG	Lateral/AtomicEtch	P-over-N N-over-P	3DVLSI	3DVLSI	3DVLSI
Stacking generation inflection	3D-stacking, Mem-on-Logic	3D-stacking, Mem-on-Logic	3D-stacking, CFET, Mem-on-Logic	3D-stacking, CFET, 3DVLSI	3D-stacking, CFET, 3DVLSI	3D-stacking, CFET, 3DVLSI

Source: International Roadmap of Devices and Systems, 2022 Update, More Moore

Semiconductor Technology Today

- Although silicon node advances continue, scaling has slowed down
  - Standard-cell-based library design kept (almost kept) node scaling
  - SRAM and customized design scaling reduced to about half (or less) per node
  - Economic benefit of Moore's Law was reduced significantly - cost of manufacture and design increased from node to node
- Hetero-integrations (HI) provide a chance to advance the semiconductor industry further for certain products and applications
  - Unlike Moore's Law, HI provides many varieties of technology, each associated with its cost and suitable to certain kinds of applications
  - HI development requires multi-disciplinary innovations

Hetero-Integration & 3D Interconnect Roadmap

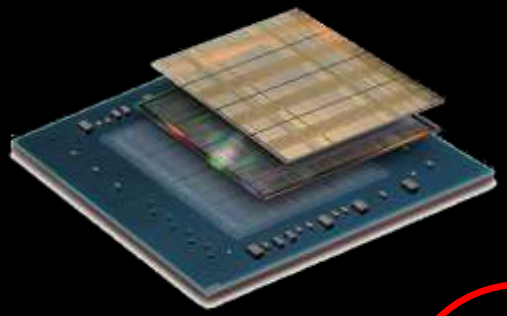


Source: IMEC public (https://www.imec-int.com/en/articles/view-3d-technology-landscape)

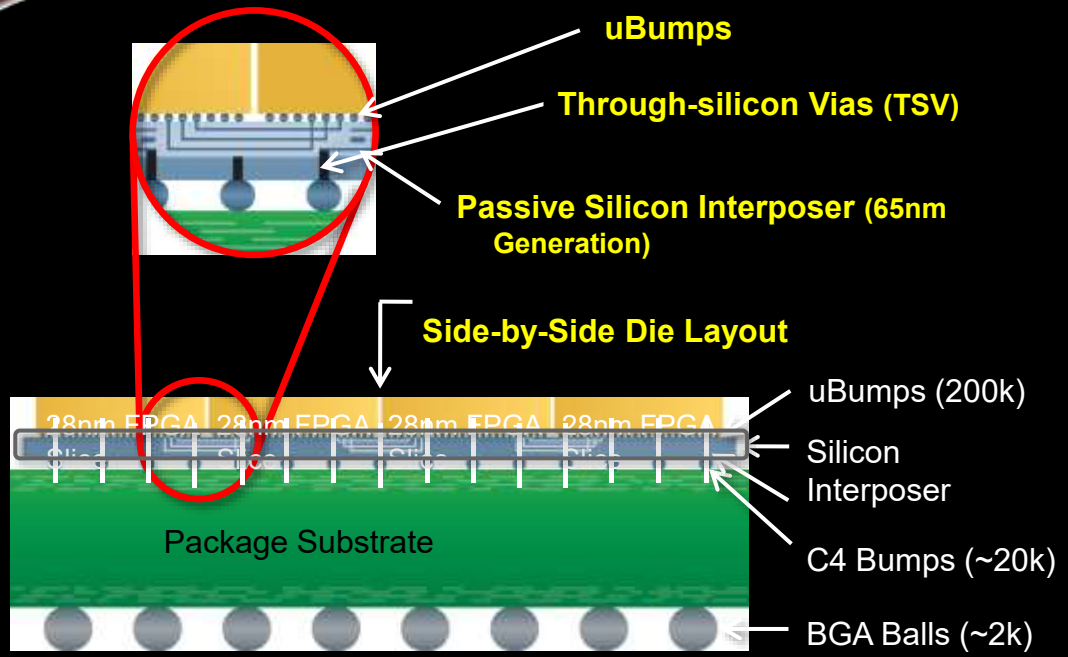
Key Challenges of Hetero Integration (HI) Product

- 3D stack technology itself
- Architecture that benefited from HI connections and mitigates
- HI design, CAD, simulation flow and PDKs (including 3D modeling)
- Software
- Pkg (I/Os) routability, signal and power integrity (SIPI), and power delivery
- Thermal solutions
- Multi-chip production flow and testing
- Reliability
- Etc.

The First Hetero-integrated FPGAs

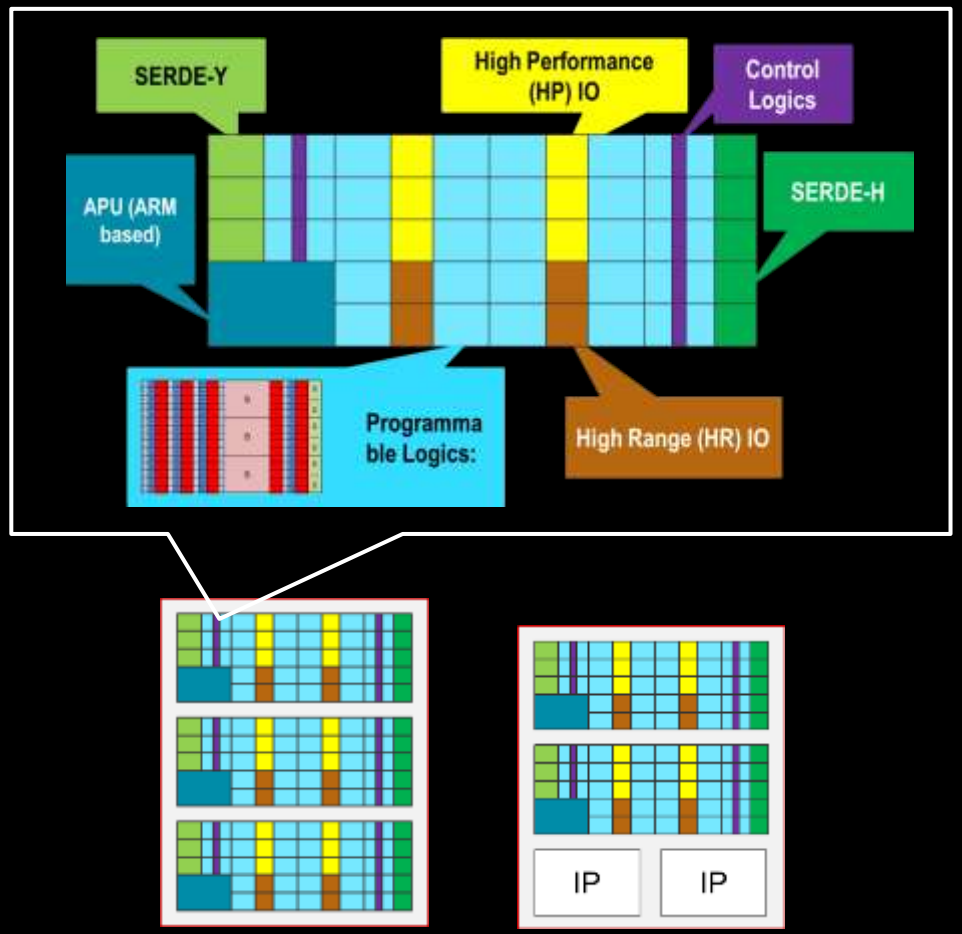


XCV2000T (2011)



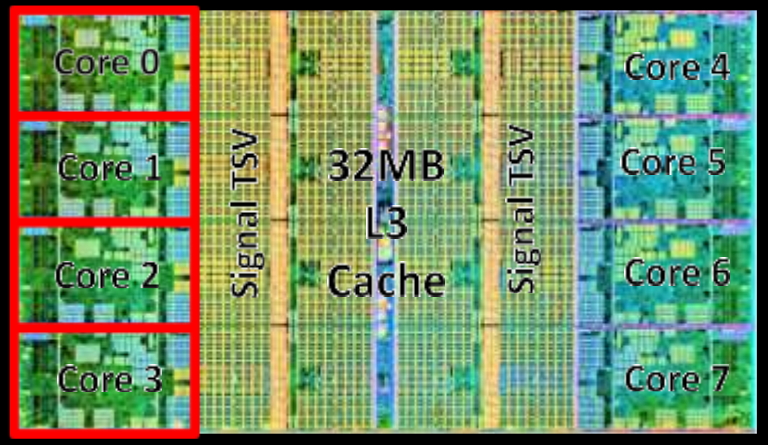
Sources: "3D TSV interconnects in digital applications based on "2.5D" silicon interposer", Xilinx, Inc. Oct. 2010

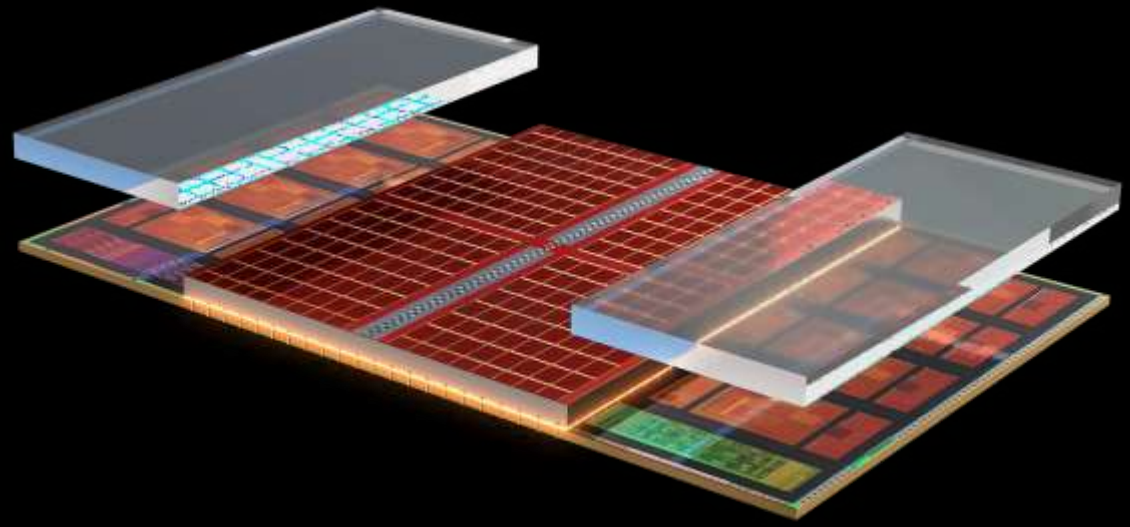
Architectural illustration of HI FPGAs

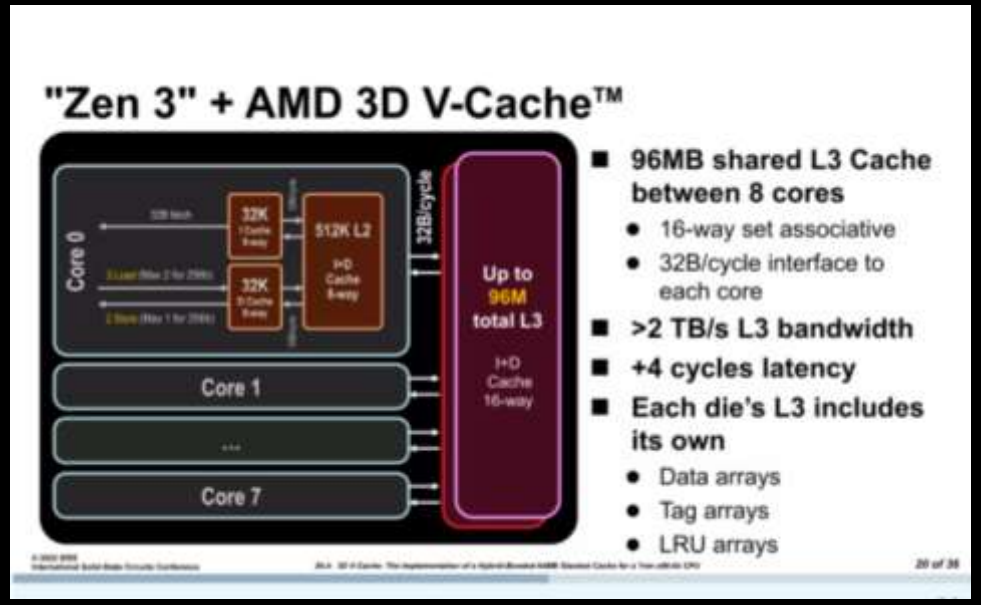


Sources: Technologies needed for FPGA, VLSI Conf short course June 2014

AMD CPU with 3D V-Cache Using Hybrid Bond Stacking







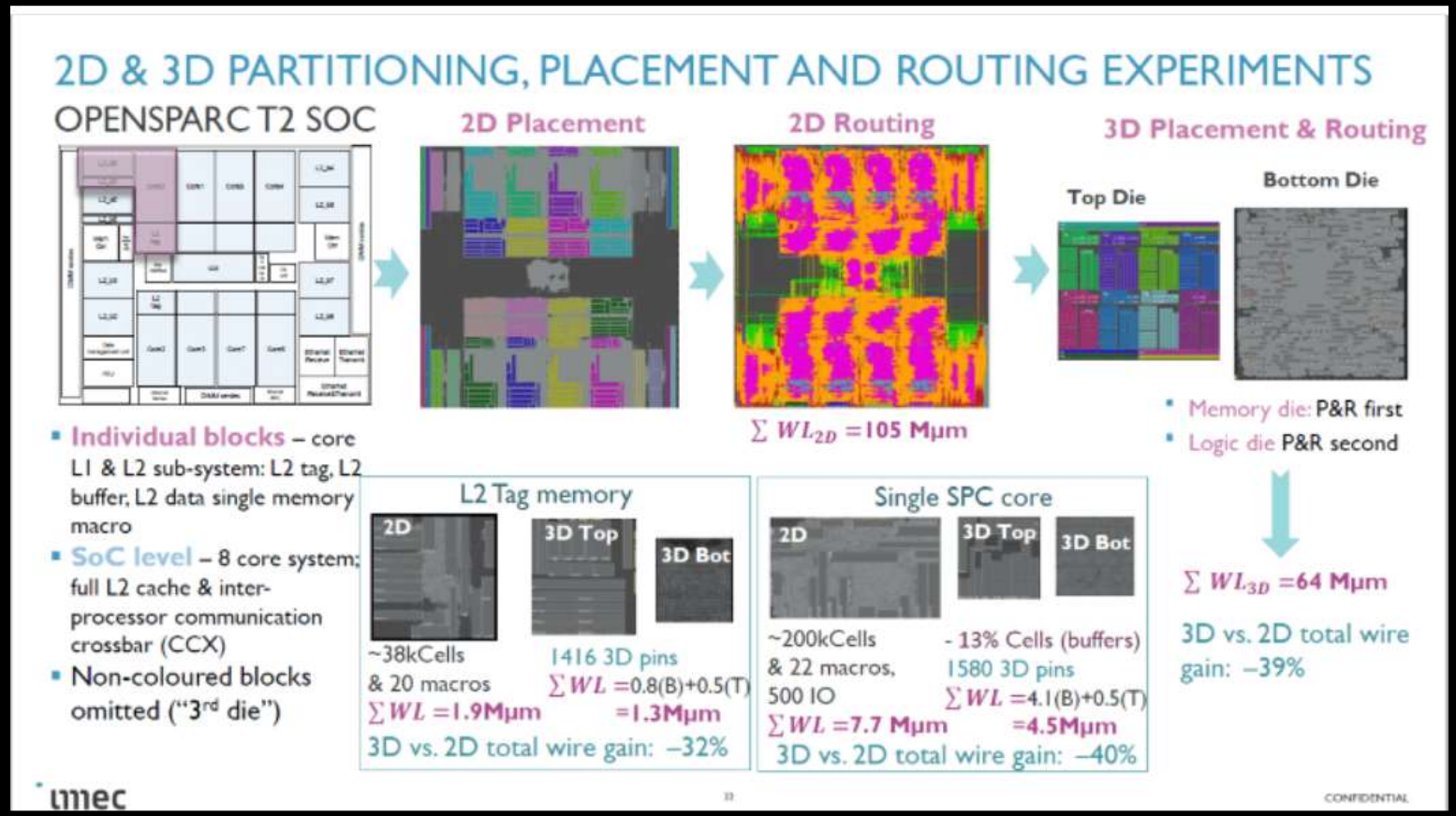
Vertical die stacking increases L3 cache from 32MB to 96MB

- 9um pitch hybrid bonding
- Improves effective memory latency
- Reduces long data path and I/O's dynamic powers
- Fits more transistors within a given package cavity size

Source: Wuu et al. (AMD), "The Implementation of a Hybrid-Bonded 64MB Stacked Cache for a 7nm x86-64 CPU, 3D V-Cache," IEEE ISSCC Feb. 2022

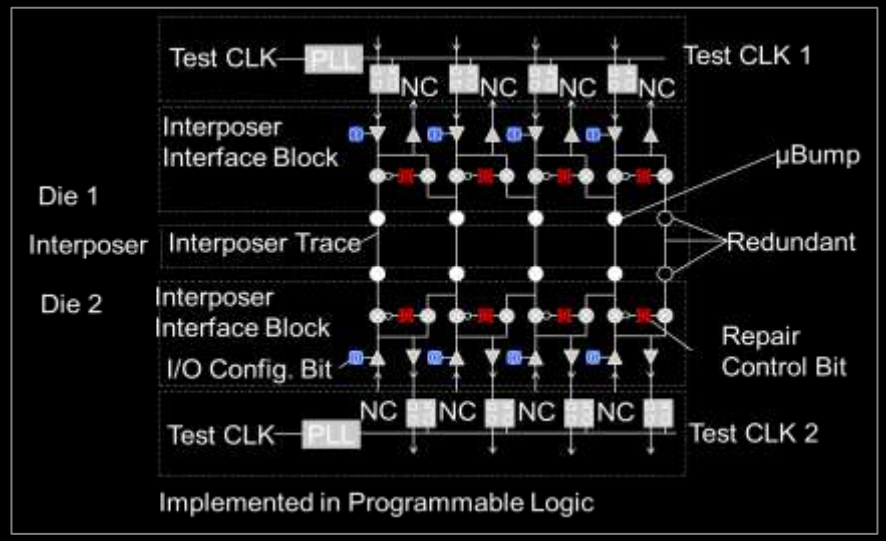
Hetero Integration (HI) Design and CAD Flows

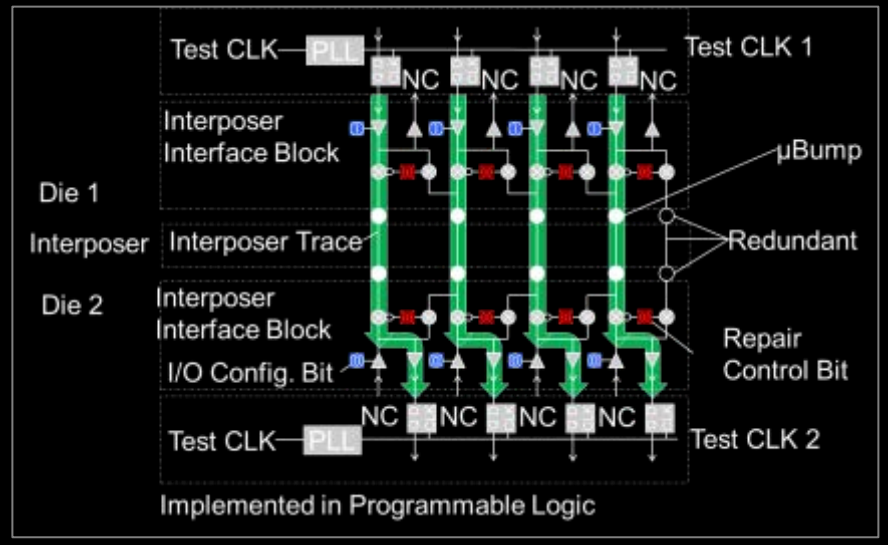
- Design innovations and CAD flow for HI have continually progressed but still have a long way to go

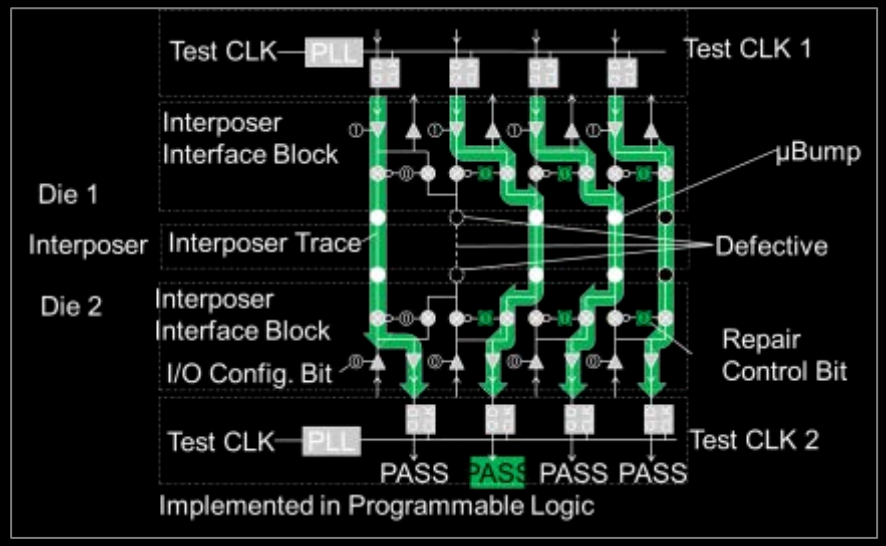


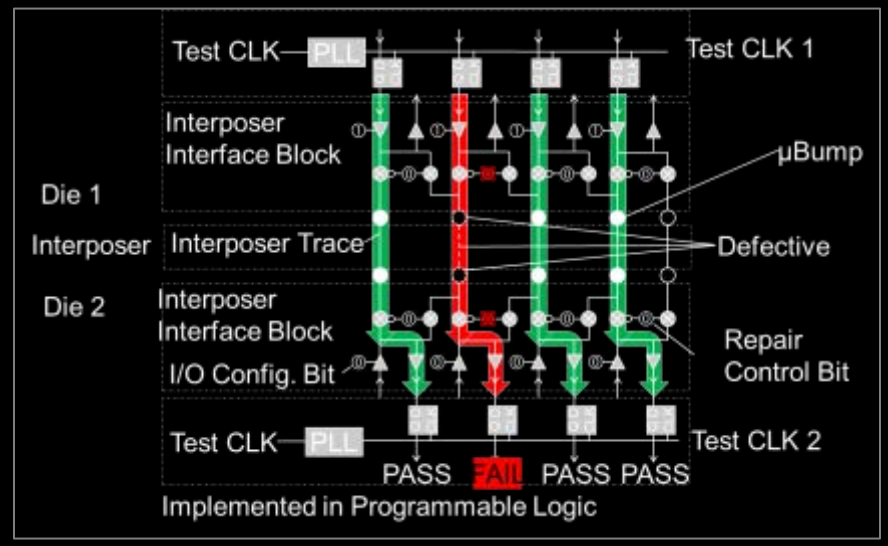
Source: E Beyne (IMEC, public) EETimes "Examples of partitioning, placement and routing," Feb. 2019

Hetero Integration (HI) Design (example)





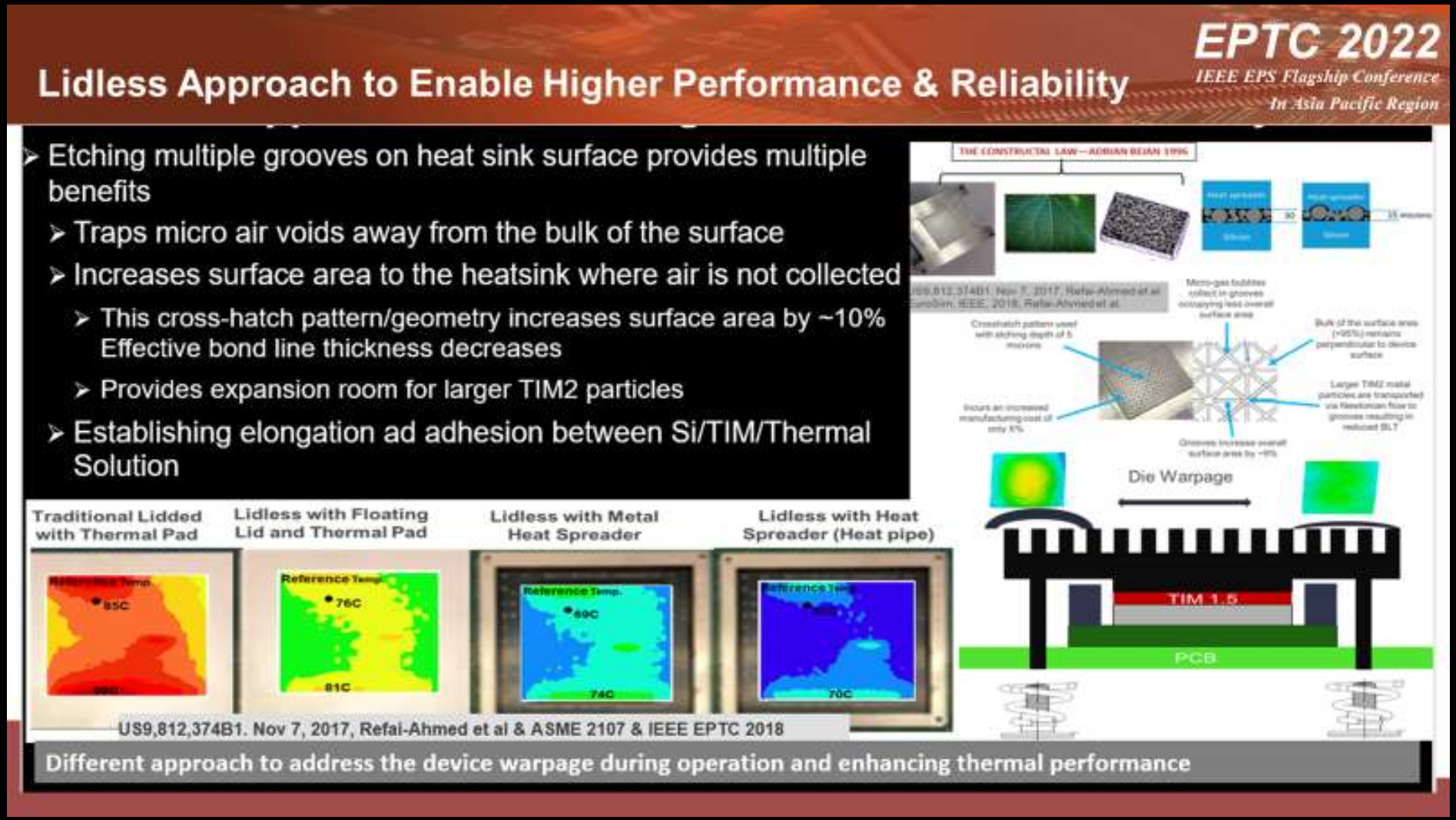




Sources: R Camarota (Xilinx) “Applying a Redundancy Scheme to Address Post-assembly Yield Loss in 3D FPGAs,” VLSI Conf Jun. 2014

Thermo-mechanical Engineering: a Critical Part of HI

- Power consumption is a top cost factor in data centers
- Thermal and mechanical solutions directly affect both performance and power efficiency
- This is one of the key STCOs



Sources: G Refai-Ahmed (AMD), “Pathfinding to Maximization of AI/HPC/GPC System Performance,” EPTC Dec. 2022

Summary

- Silicon scaling has been slowing, and costs continually increase from node to node
- Hetero-integrations (HI) provide new opportunities
- HI is not another Moore's Law - they fit distinct applications differently and come with a cost
- IC industry will continue to grow, especially in data processing areas (datacenters, auto drive, 5G, AI, etc.)
- Those who can target these areas to specific customers and applications and can provide these solutions at a better cost will fare better
- Future success requires more interdisciplinary knowledge and engineering

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