Moore’s Law

- In 1965, Moore observed that transistor density doubles every year.
- Revised in 1975: transistor density doubles every two years.

Source: “Cramming more components onto integrated circuits”
Gordon Moore, Electronics, Volume 38, Number 8, April 1965

Moore’s Law was designed to rebut contemporary claims that integrated circuits were expensive and unreliable.
FPGA capacity grew ~680x in 10 nodes, benefiting from Moore’s Law, hetero-integration, packaging and many new technologies

CMOS Technology Roadmap

- Moore’s law has slowed down significantly
- Need expensive solutions to keep Moore’s law alive
  - Gate-All-Around, EUV double patterning, SiGe channel, etc.
  - Node-to-node mask/wafer cost increase can be > 30%
  - High design cost for new technology nodes
- Advanced packaging & 3D integration can provide new opportunities

<table>
<thead>
<tr>
<th>YEAR OF PRODUCTION</th>
<th>Logic industry “Node Range” Labeling</th>
<th>Fine-pitch 3D integration scheme</th>
<th>Logic device structure options</th>
<th>Platform device for logic</th>
<th>LOGIC TECHNOLOGY ANCHORS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&quot;3nm&quot;</td>
<td>Stacking</td>
<td>finFET, LGAA</td>
<td>finFET, LGAA</td>
<td>Device technology inflection</td>
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<td>&quot;2nm&quot;</td>
<td>Stacking</td>
<td>LGAA, CFET-SRAM</td>
<td>LGAA, CFET-SRAM</td>
<td>Taller fin</td>
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<td>2022</td>
<td>&quot;1.5nm&quot;</td>
<td>Stacking</td>
<td>LGAA, CFET-SRAM</td>
<td>LGAA, CFET-SRAM</td>
<td>1931, EUV DP</td>
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<tr>
<td>2025</td>
<td>&quot;1.0nm eg&quot;</td>
<td>3DVL SI</td>
<td>LGAA, CFET-SRAM, 3DVL SI</td>
<td>LGAA, CFET-SRAM, 3DVL SI</td>
<td>1931, EUV DP</td>
</tr>
<tr>
<td>2028</td>
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<td>3DVL SI</td>
<td>LGAA-3D, CFET-SRAM, 3DVL SI</td>
<td>LGAA-3D, CFET-SRAM, 3DVL SI</td>
<td>1931, EUV DP</td>
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<tr>
<td>2031</td>
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<td>2034</td>
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<td>1931, EUV DP</td>
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<tr>
<td>2037</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1931, EUV DP</td>
</tr>
</tbody>
</table>

Source: International Roadmap of Devices and Systems, 2022 Update, More Moore
Semiconductor Technology Today

• Although silicon node advances continue, scaling has slowed down
  • Standard-cell-based library design kept (almost kept) node scaling
  • SRAM and customized design scaling reduced to about half (or less) per node
  • Economic benefit of Moore’s Law was reduced significantly - cost of manufacture and design increased from node to node

• Hetero-integrations (HI) provide a chance to advance the semiconductor industry further for certain products and applications
  • Unlike Moore’s Law, HI provides many varieties of technology, each associated with its cost and suitable to certain kinds of applications
  • HI development requires multi-disciplinary innovations
Hetero-Integration & 3D Interconnect Roadmap

Key Challenges of Hetero Integration (HI) Product

- 3D stack technology itself
- Architecture that benefited from HI connections and mitigates
- HI design, CAD, simulation flow and PDKs (including 3D modeling)
- Software
- Pkg (I/Os) routability, signal and power integrity (SIPI), and power delivery
- Thermal solutions
- Multi-chip production flow and testing
- Reliability
- Etc.
The First Hetero-integrated FPGAs

**XCV2000T (2011)**

- **uBumps**
- **Through-silicon Vias (TSV)**
- **Passive Silicon Interposer (65nm Generation)**
- **Side-by-Side Die Layout**
  - **uBumps (200k)**
  - **Silicon Interposer**
  - **C4 Bumps (~20k)**
  - **BGA Balls (~2k)**

Sources: “3D TSV interconnects in digital applications based on “2.5D” silicon interposer”, Xilinx, Inc. Oct. 2010

Sources: Technologies needed for FPGA, VLSI Conf short course June 2014
AMD CPU with 3D V-Cache Using Hybrid Bond Stacking

Vertical die stacking increases L3 cache from 32MB to 96MB

- 9um pitch hybrid bonding
- Improves effective memory latency
- Reduces long data path and I/O’s dynamic powers
- Fits more transistors within a given package cavity size

Hetero Integration (HI) Design and CAD Flows

- Design innovations and CAD flow for HI have continually progressed but still have a long way to go.

Source: E Beyne (IMEC, public) EETimes “Examples of partitioning, placement and routing,” Feb. 2019
Hetero Integration (HI) Design (example)

Sources: R Camarota (Xilinx) "Applying a Redundancy Scheme to Address Post-assembly Yield Loss in 3D FPGAs," VLSI Conf Jun. 2014
Thermo-mechanical Engineering: a Critical Part of HI

- Power consumption is a top cost factor in data centers
- Thermal and mechanical solutions directly affect both performance and power efficiency
- This is one of the key STCOs

Lidless Approach to Enable Higher Performance & Reliability

- Etching multiple grooves on heat sink surface provides multiple benefits
  - Traps micro air voids away from the bulk of the surface
  - Increases surface area to the heatsink where air is not collected
  - This cross-hatch pattern/geometry increases surface area by ~10%
  - Effective bond line thickness decreases
  - Provides expansion room for larger TIM2 particles
  - Establishing elongation adhesion between Si/TIM/Thermal Solution

Summary

- Silicon scaling has been slowing, and costs continually increase from node to node
- Hetero-integrations (HI) provide new opportunities
- HI is not another Moore’s Law - they fit distinct applications differently and come with a cost
- IC industry will continue to grow, especially in data processing areas (datacenters, auto drive, 5G, AI, etc.)
- Those who can target these areas to specific customers and applications and can provide these solutions at a better cost will fare better
- Future success requires more interdisciplinary knowledge and engineering
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