SiP and Module

(Heterogeneous Integration Roadmap (HIR) Annual Meeting 2023, Milpitas)

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Erik Jung is with the Fraunhofer IZM, serving as Business Developer for Advanced System Integration Solutions. He is Member of IEEE and has long standing activities within the IEEE community

Supported among others by: Harrison Chang (ASE), Hannes Stahr (AT&S),Key Chung (SPIL), Peter Machiels (Philips), Thomas Zerna (TU Dresden), Hugo Pristauz (BESI)

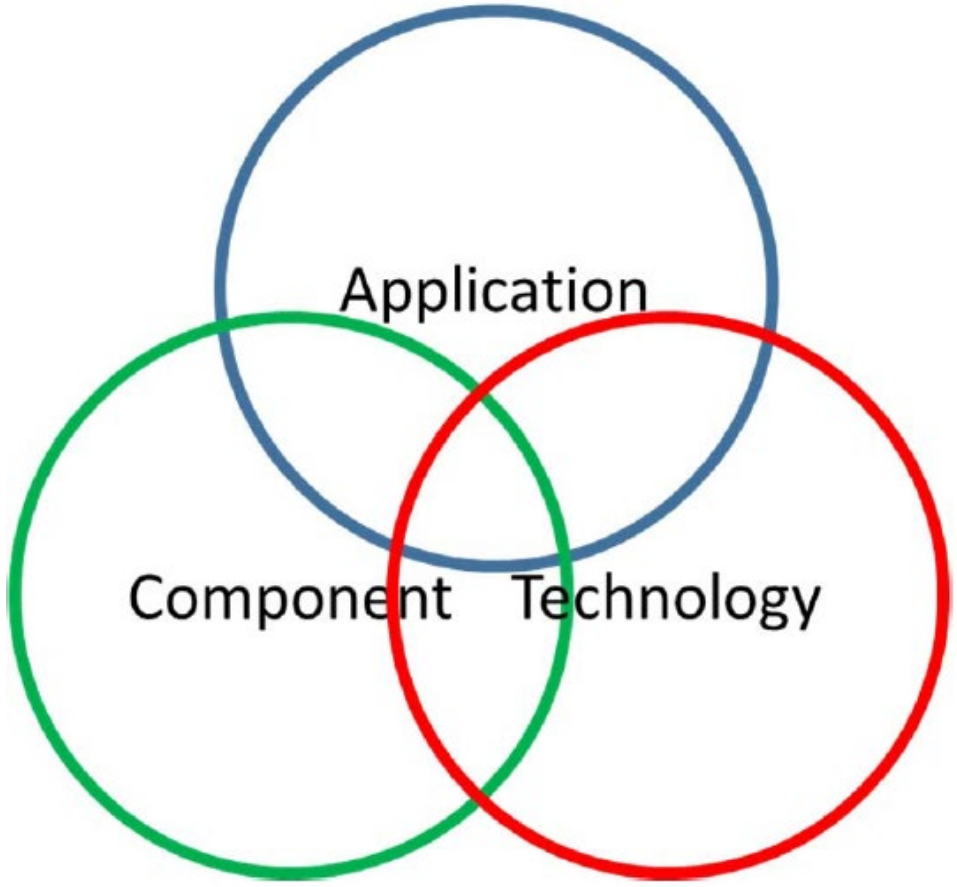
Outline

Definitions and Classification

Toolbox for SiP

Challenges

Outlook



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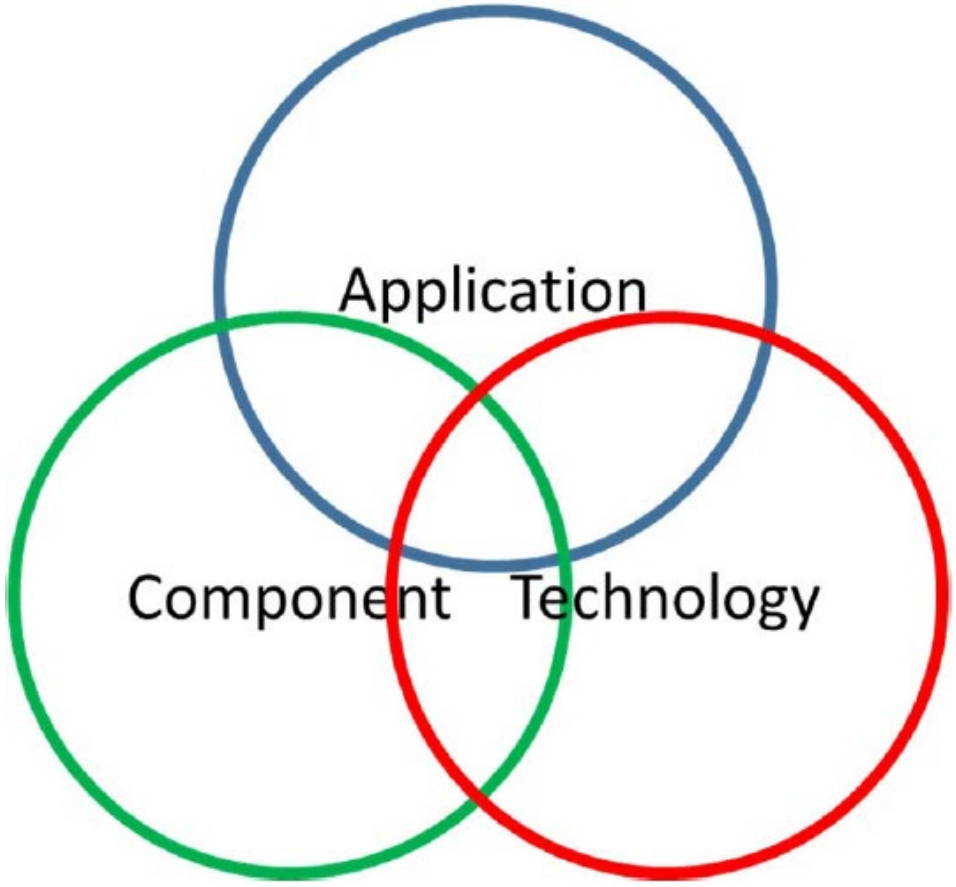
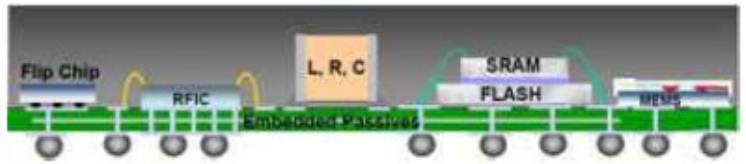
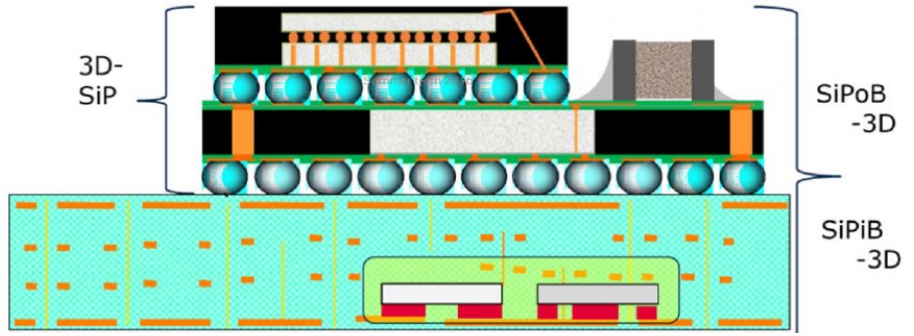
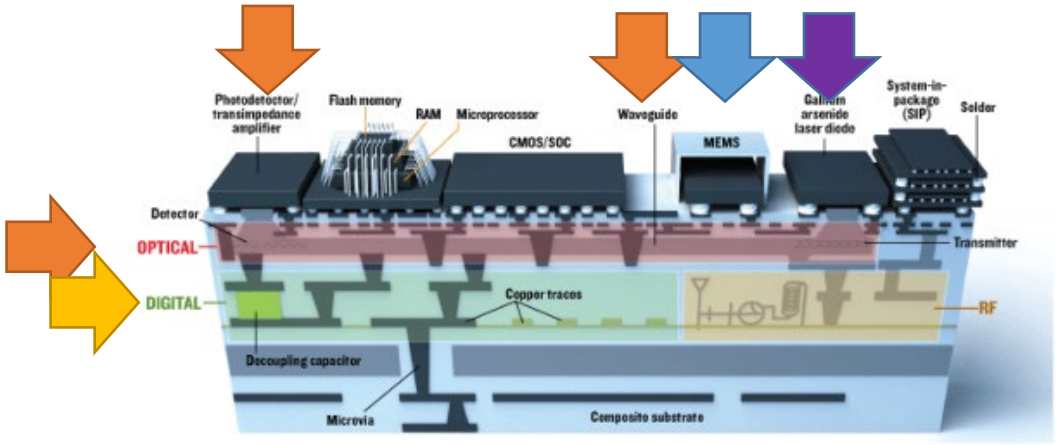






Definition of SiP

"SiP, or System-in-Package, refers to a package (such as SO, QFP, BGA, CSP,LGA) that has multiple die (Si, GaAs, SiGe, and or SOI) plus optional passives integrated together. The package is typically surface mounted to the main board."



Multi-

-Die
-Domain
-Function

Functionality

Components

Si, SiGe
SiC
III-V (GaN, GaAs)
MEMS
Optical (active, passive)
Passives
…

UseCase

Application

Power
MEMS
IoT
AI
Consumer
Automotive
Communication
Medical
…

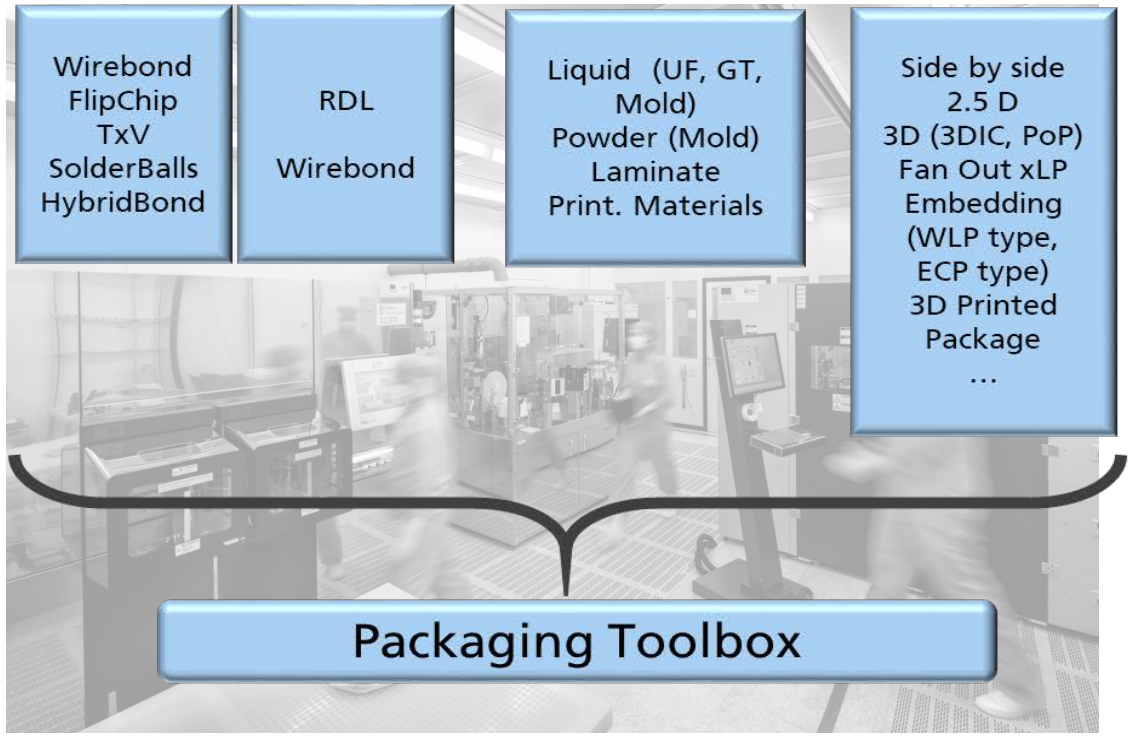
Interconnecting Functions

Material Focus

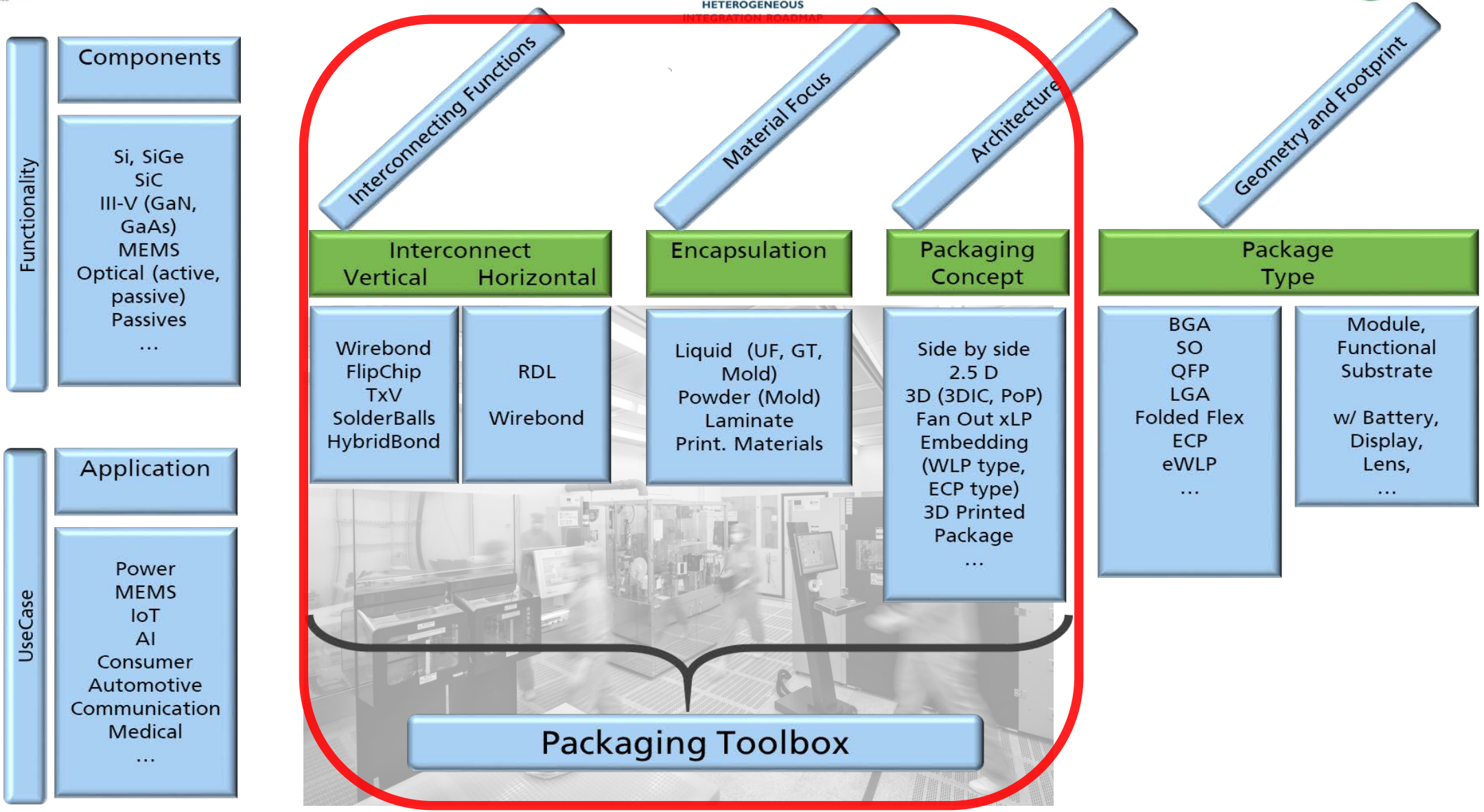
Architecture

Geometry and Footprint

Interconnect Vertical	Interconnect Horizontal	Encapsulation	Packaging Concept	Package Type	
Wirebond FlipChip TxV SolderBalls HybridBond	RDL Wirebond	Liquid (UF, GT, Mold) Powder (Mold) Laminate Print. Materials	Side by side 2.5 D 3D (3DIC, PoP) Fan Out xLP Embedding (WLP type, ECP type) 3D Printed Package …	BGA SO QFP LGA Folded Flex ECP eWLP …	Module, Functional Substrate w/ Battery, Display, Lens, …



Packaging Toolbox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Interconnect
Vertical
Horizontal
Encapsulation
Packaging Concept
Package Type
Wirebond
FlipChip
TxV
SolderBalls
HybridBond
RDL
Wirebond
Liquid (UF, GT, Mold)
Powder (Mold)
Laminate
Print. Materials
Side by side
2.5 D
3D (3DIC, PoP)
Fan Out xLP
Embedding (WLP type, ECP type)
3D Printed Package
…
BGA
SO
QFP
LGA
Folded Flex
ECP
eWLP
…
Module, Functional Substrate
w/ Battery, Display, Lens,
…
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Vertical | Horizontal

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FlipChip
TxV
SolderBalls
HybridBond

RDL

Wirebond

Material Focus

Encapsulation

Liquid (UF, GT, Mold)
Powder (Mold)
Laminate
Print. Materials

Architecture

Packaging Concept

Side by side
2.5 D
3D (3DIC, PoP)
Fan Out xLP
Embedding (WLP type, ECP type)
3D Printed Package
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Geometry and Footprint

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Module, Functional Substrate

w/ Battery, Display, Lens,
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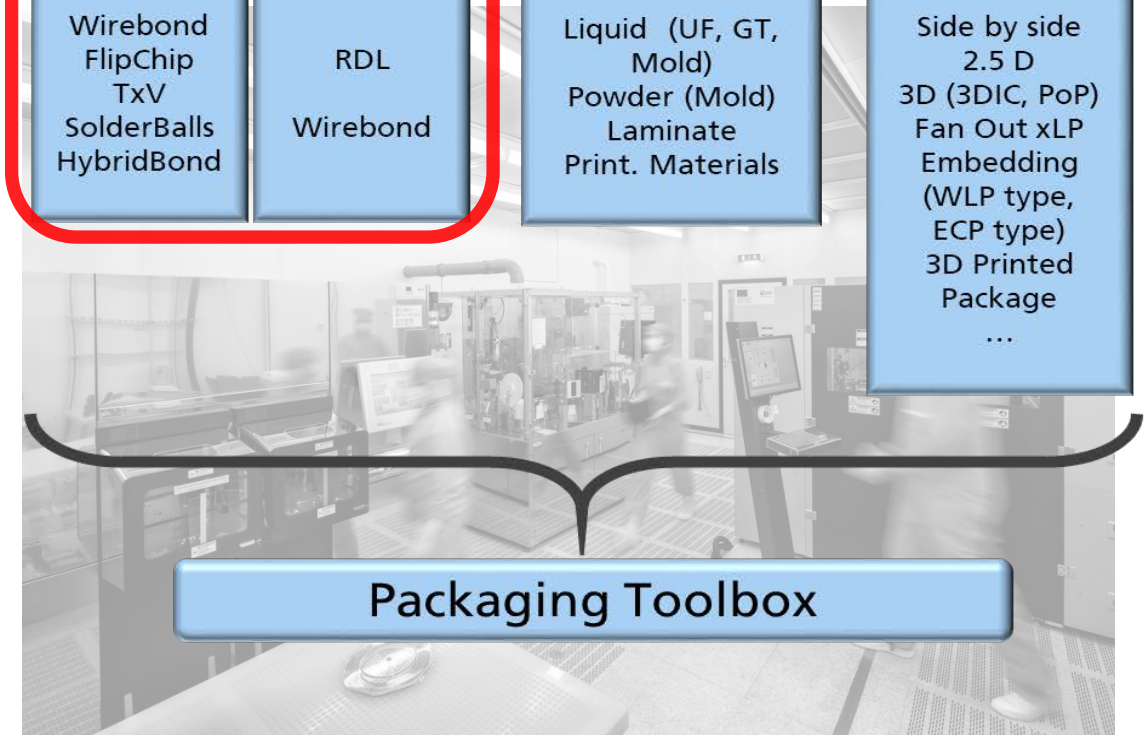
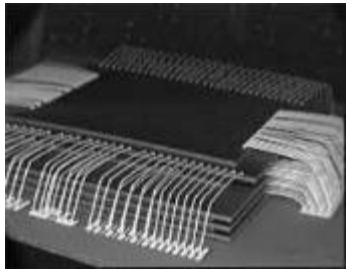
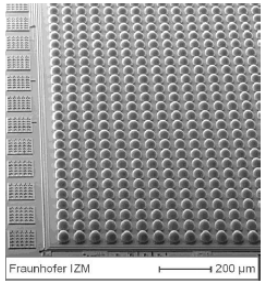
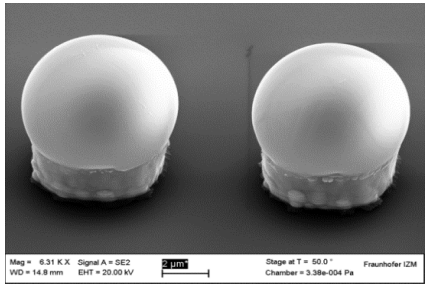


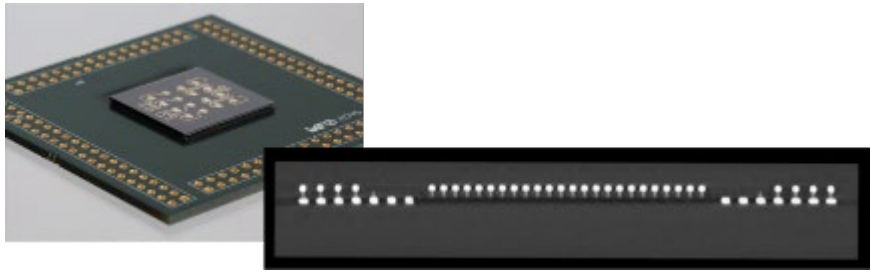
Packaging Toolbox

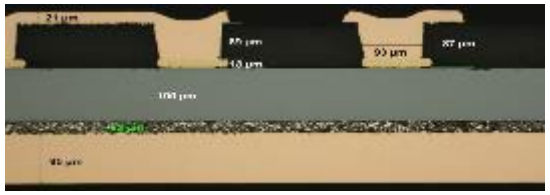
SiP Packaging Toolbox: *Interconnect*











Evolution of standard interconnect

- *Wirebond* and stacked wirebonds incl. copper wire
- *Flip Chips* and stacked flip chips (w/ TSV)
- Package on Package (PoP) bump bonding

Challenges

- More IO/area, size of microbumps
- Thin chips for thinner stacks
- Warp and I/O arrangement for *More than Moore* SiP

New: Embedding Technology – *Interconnect by Electroplating*

- Embedding of thin active chips into the dielectric layers
- Embedding of passive components together with chips
- Embedding of SMD components for low volume and SME´s

Challenges:

- Remaining dielectric thickness decreasing
- Lines/spaces and via Ø @ HDI substrates, by shrinking the chip pitch
- Multi material challenge (Si, dielectric, EMC, underfill, die attach …)

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Interconnecting Functions

Interconnect
Vertical | Horizontal

Wirebond
FlipChip
TxV
SolderBalls
HybridBond

RDL

Wirebond

Material Focus

Encapsulation

Liquid (UF, GT, Mold)
Powder (Mold)
Laminate
Print. Materials

Architecture

Packaging Concept

Side by side
2.5 D
3D (3DIC, PoP)
Fan Out xLP
Embedding (WLP type, ECP type)
3D Printed Package
…

Geometry and Footprint

Package Type

BGA
SO
QFP
LGA
Folded Flex
ECP
eWLP
…

Module, Functional Substrate

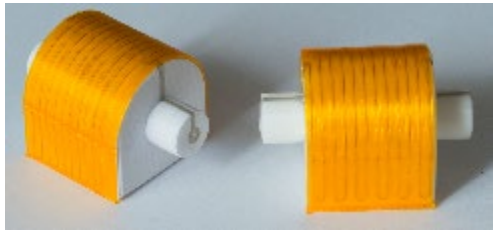
w/ Battery, Display, Lens,
…

Packaging Toolbox

SiP Packaging Toolbox: *Encapsulation*





Workhorses:

Molding (Pellet)

Glob Top (Dispense)

UnderFill (Dispense)

Established:

Molding (Liquid, Compression)

Glob Top (Jet and Print)

UnderFill (Jet)

To Come:

Lamination for thin/flat assemblies

3D Additive as „Structurally Integrated“

Material innovations, process innovations, conceptual innovations drive these advancements

Images: KCC, HybridCH, Finetech, Polymer Innovations, Neotech

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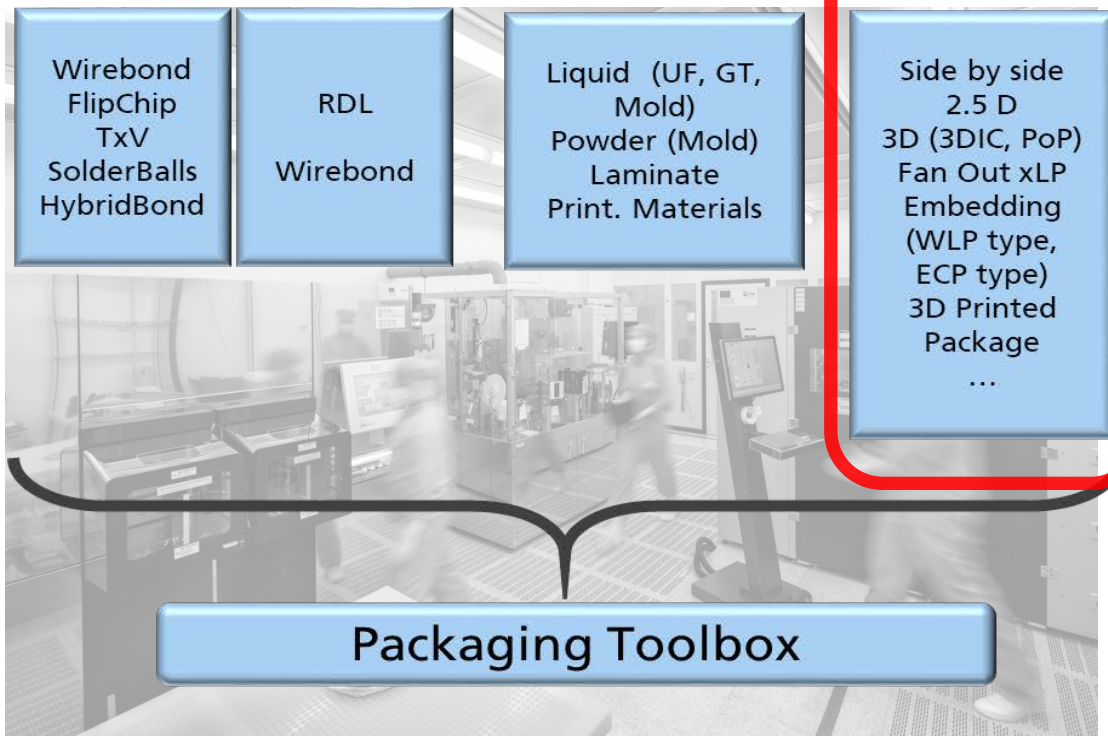
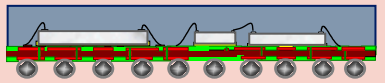
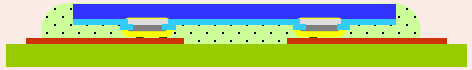
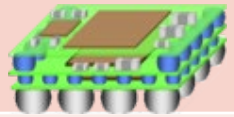
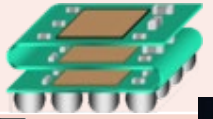
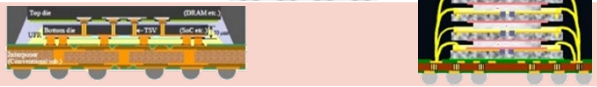


Packaging Toolbox

SiP Packaging Toolbox

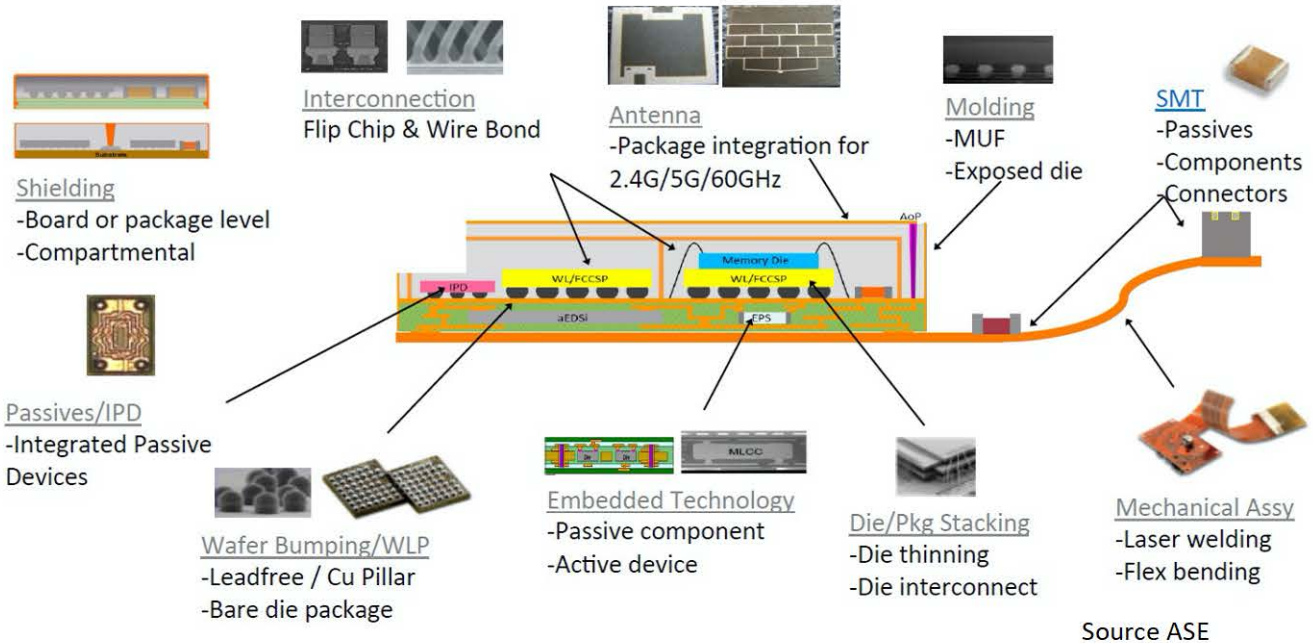
Packaging Concept

Concept	Material	Interconnection	
Side by Side	PCB	Solder Adhesive Wire bond	
	Flex Silicon	Solder Adhesive Wire bond	
Stacked / Folded	PCB	Solder Adhesive Wire bond	
	Flex	Solder Adhesive	
	Silicon	Solder Wire bond	
Embedding	PCB	Solder Electroplated	
	Flex	Solder Adhesive Electroplated	
	Thin film (Wafer Level)	Electroplated	
Fan Out Wafer/Panel Level	Mold compound	Solder Adhesive Electroplated	
Module	PCB Flex	Solder Adhesive Electroplated	

New Processes

- Wafer and Panel Level Packaging
- Reconstituted Wafers
- TSV´s for Silicon Interposer
- µ-Bumps
- Wafer Thinning and Handling
- Low *k* Polymers for RDL
- Merge of Front-end and Back-end

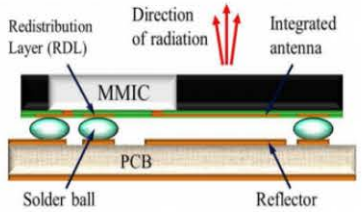
SiP Packaging Toolbox –> "new functional blocks"



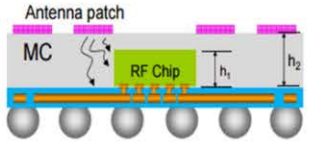
Source ASE

Example: Antenna Integration for FO

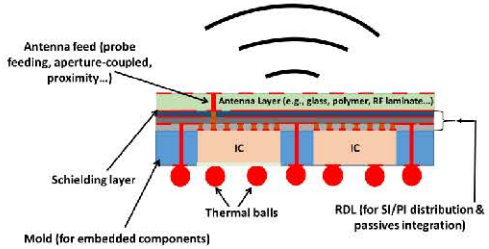
eWLB Infineon



Integrated FO TSMC



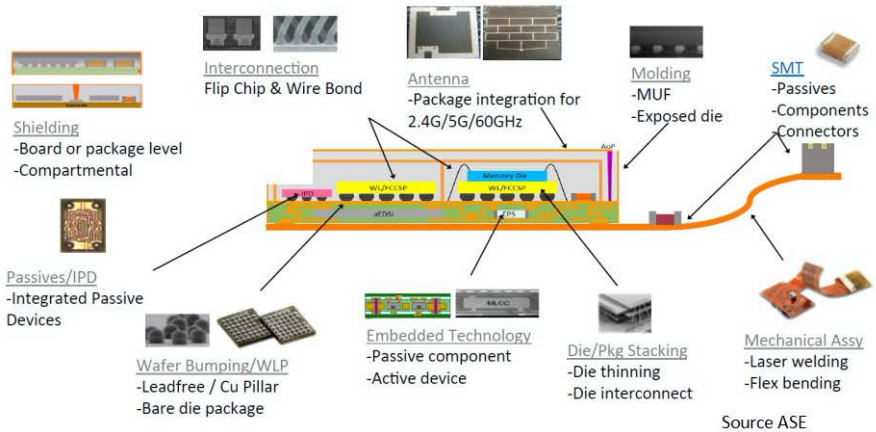
Panel FO FhG-IZM



Aside from the **electrical domain**, also **multiple additional functionalities will emerge** for the SiP packaging toolbox.

IEEE
IEEE photonics Society
semi
IEEE ELECTRONICS PACKAGING SOCIETY
ASME
ELECTRON DEVICES SOCIETY

SiP Packaging Toolbox –> "new functional blocks"



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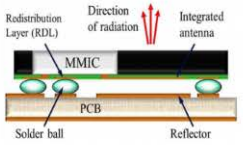

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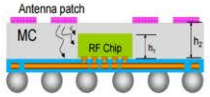

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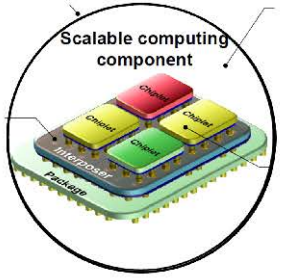
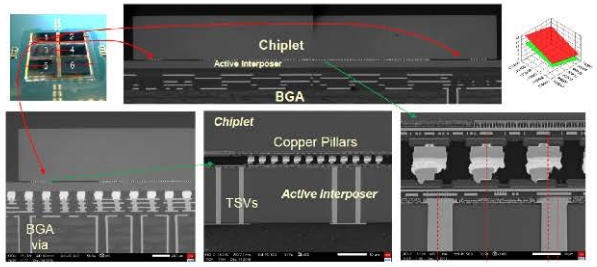
SiP Packaging Toolbox: Chiplet as a SiP momentum



- ***More Than Moore* and *More Moore* Integration in one SiP using Chiplet concept**
  - **Core technologies derived from previously mentioned tools**
  - **Active and passive interposer concept**
- **Electrical and optical interconnects „in SiP"**



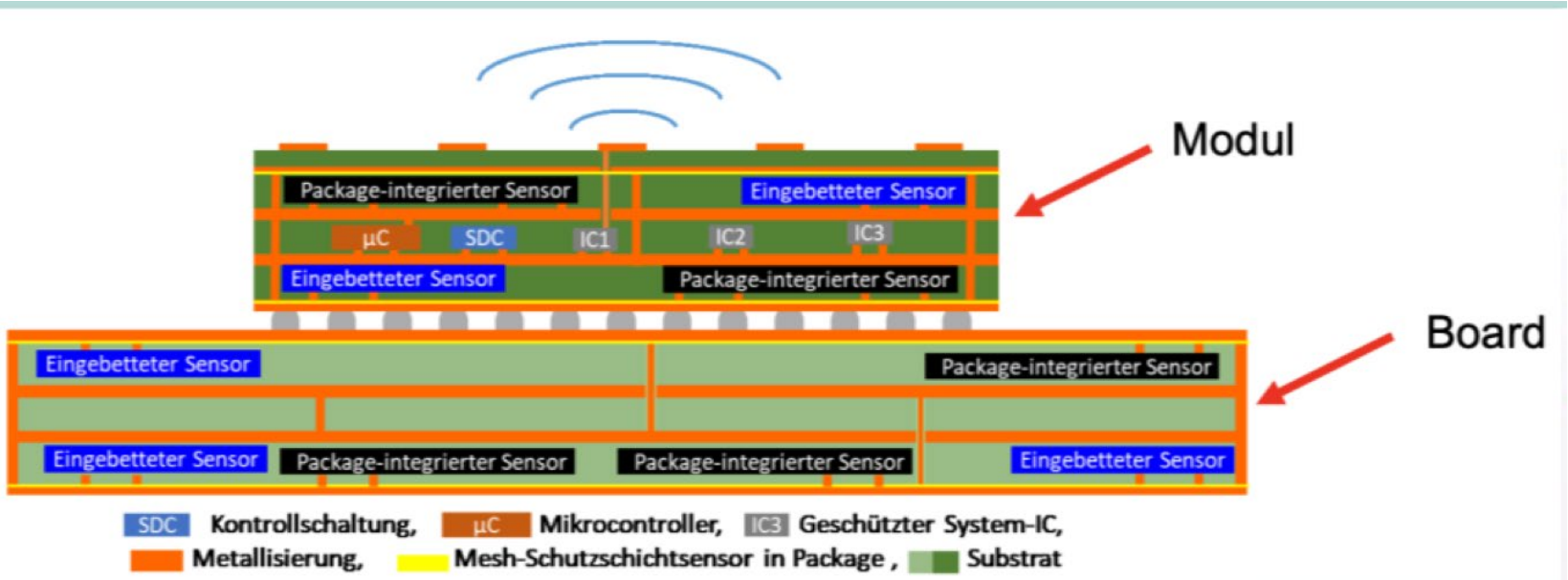
Issues to be adressed:

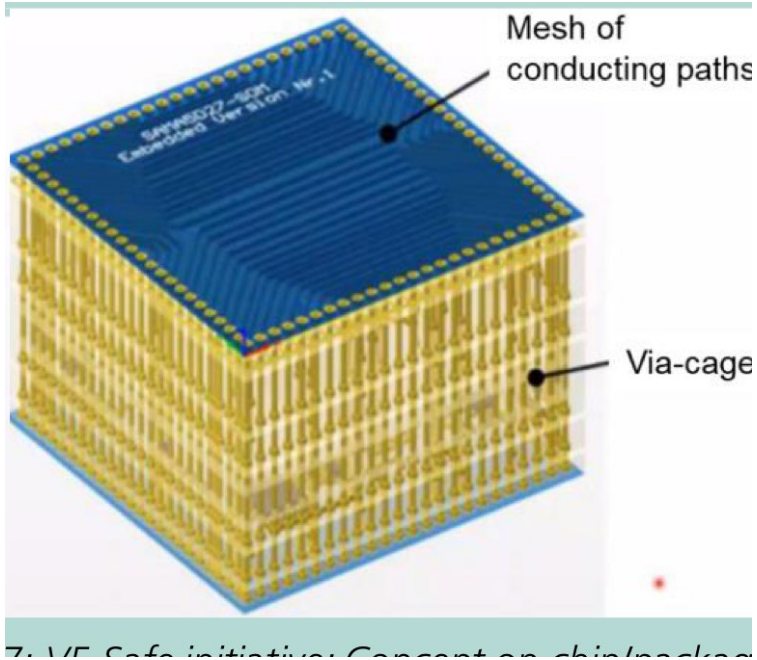
- KGD Issues
- EDA Issues
- Cost/Performance/Reliability considerations

Images from "Chiplet-based partitioning using Smart Interposer for High Performance Computing" by Patric Vivet, CEA Leti, 3D Summit, Dresden, Jan 2019

Chiplets supporting trusted computing concepts

- Critical functionalities can be sourced from trusted entities
- Non critical functionalities can be sourced from redundant suppliers and independently verified
- Integration by advanced packaging done by trusted entities
- Packaging to include tamper proofing technologies





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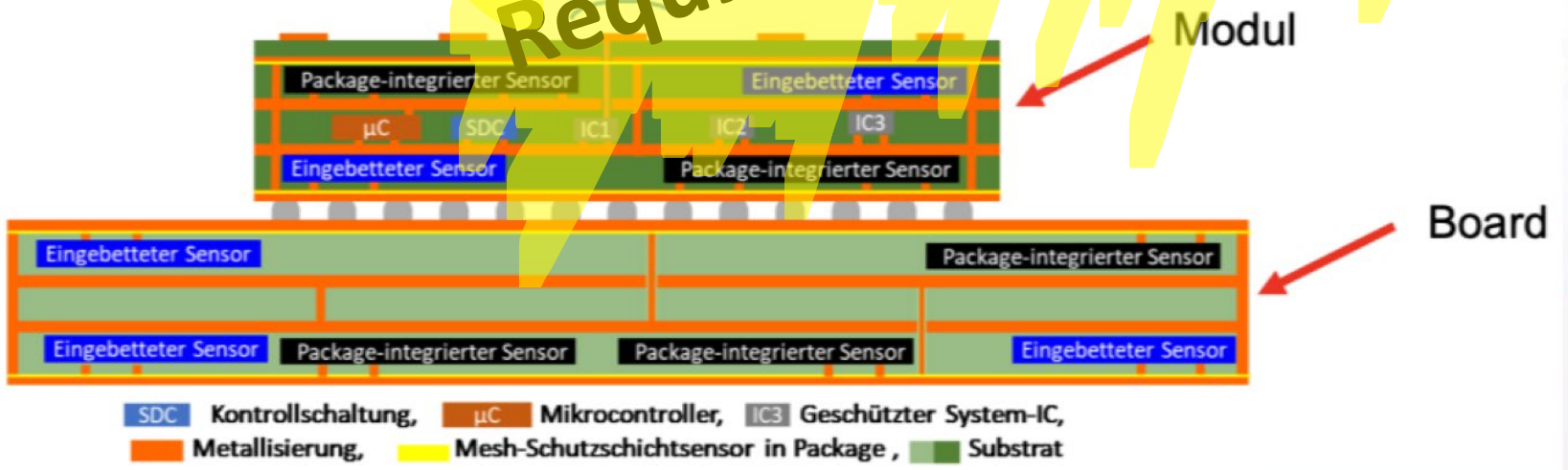
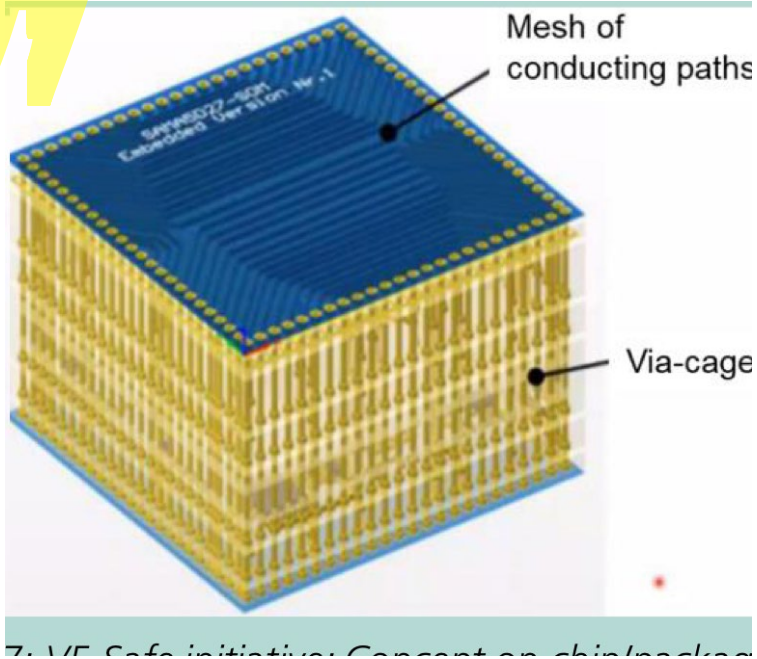
Requires SDKs, ADKs and PDKs





Outline

Definitions and Classification

Toolbox for SiP

Challenges

Outlook

New/future requirements derived from different application areas as indicators for roadmap targets
=> New challenges

Power

RF/THz

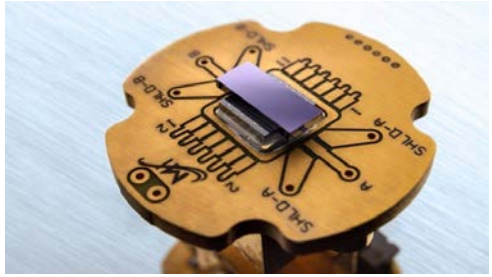
Autonomous Systems

IoT

Consumer

Wearables

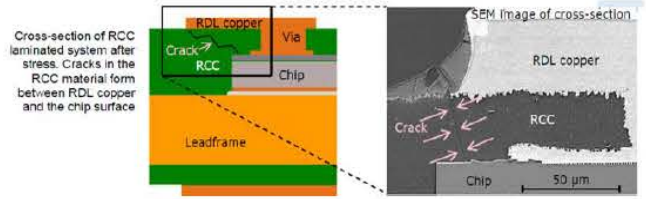
Quantum Devices



HETEROGENEOUS INTEGRATION ROADMAP

Difficult Challenges for Implementing SiP

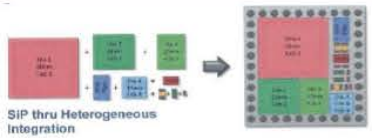
Materials
- New materials (HF materials)
- Material interactions
- Failure modes
- Thermal mismatch



Cost
- New package platform (FO, embedding)
- Complex Systems

Assembly
- Technology Diversity (Sensors, antenna, IC´s, passives
- Pitch, soldered and non-solderd components

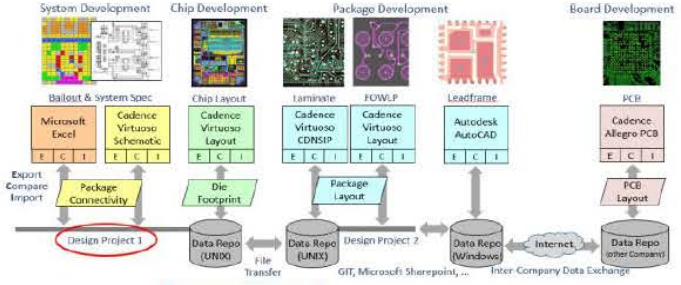
Standardization
common package type
- Footprint
- Dimensions
- Thickness



Customer Requirements
- Reliability and application specific requirements
- Temperature / cooling
- Performance
- Pitch, dimensions, thickness

Test
- Application specific (incl. mixed signal, media, etc.)
- Electrical, mechanical and thermal aspects
- Self testing, incl. BIST

Co-Design
- SiP Requiring a system <-> package co-design
- Different libraries in one project
- Multiple domains with different scaling properties
- Thermal, mechanical and electrical analysis



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Outline

Definitions and Classification

Toolbox for SiP

Challenges

Outlook

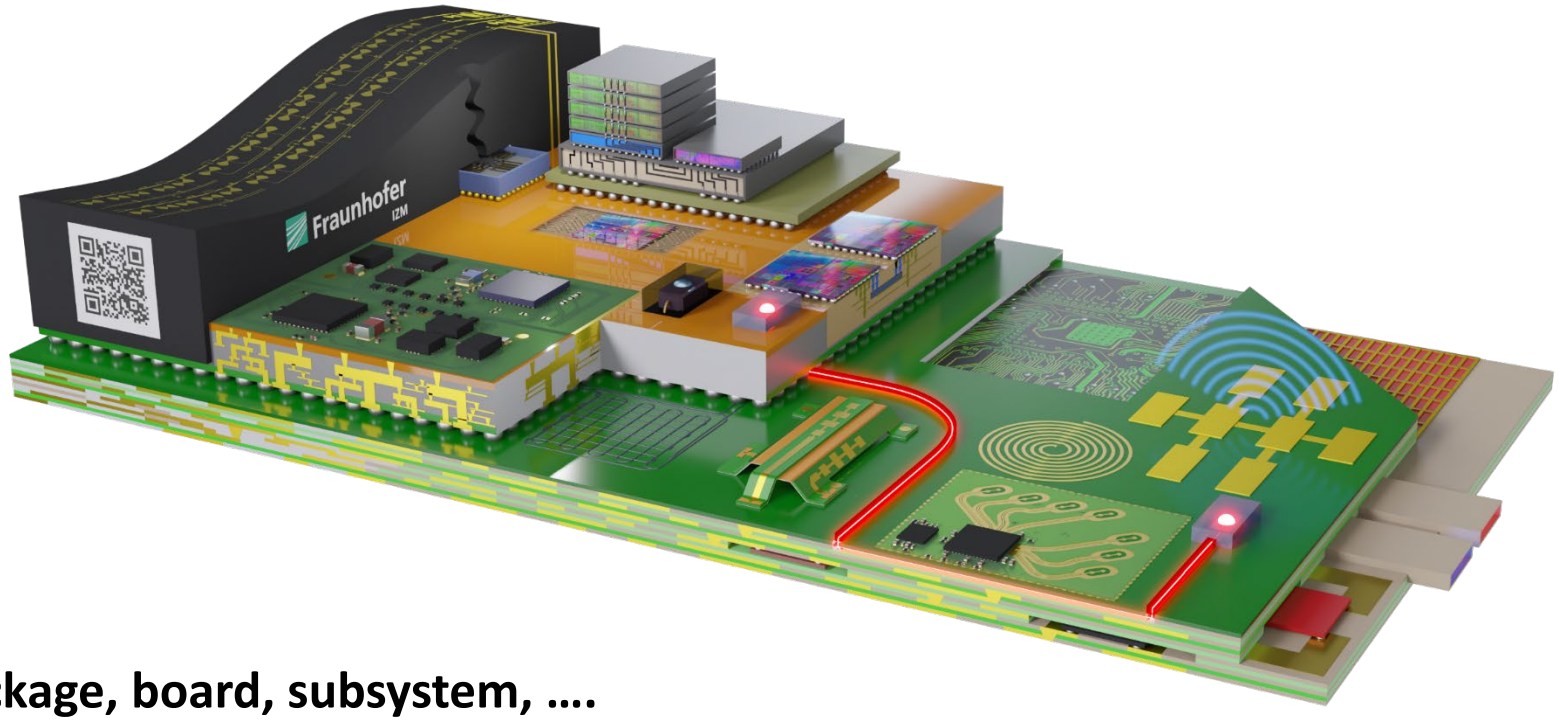
Outlook

-

SiP and Modules are major directions in future microelectronics

Managing complexity will be a major challenge:

- Functional increase
- Complex material mix on semiconductor, package and board level
- Reliability caused by new applications (in addition => impact on sustainability)
- Thermal management
- Complex testing
- Co-design over various domains chip, package, board, subsystem, ….
- Cost constraints



HIR 2023 Outlook

Refining quantitative details……Strengthen Cross TWG relations…… Assess new/emerging developments (PIC and Quantum….)

	Challenge	State of the Art	Future Perspective
		Application Related	
1	Functionality Increase	Single domain functionality	Multi domain functionality
2	Non-electric functions	Separate SiP approach, separated value chain segment	Integrated in one flow of value chain creation
3	Assembly	Single technology use	Choice from a technology menu built from a compatible tool box
4	Reliability	Standards derived from "typical applications" and adapted to actual use case	Novel applications driven by new business models may render current standards obsolete
		Material Related	
5	Material	Material evolution driven by integration requirements (e.g. high flow epoxies, CuPd wire)	Material revolution driving integration, disrupting industries' value chains
		Physics Related	
6	Thermal Management	passive and active cooling built after simulation/validation assessment	Thermal-Electric and Mechanical Co-Design including the SiP integration site via CAD Tool
7	Reliability	Empirically derived statistical models	Physics of Failure Modeling
8	Form Factor	SiP design targeting maximum package efficiency limited by physical geometry	SiP design with as-needed efficiency, limited by cross-cutting aspects, interdependencies
9	Signal Integrity	Individual design and test	Building blocks for S.I.
10	Power requirements	<50W/cm³	200W/cm³

		Cross Cutting Aspects	
11	Test	Single-domain testing, sequential test of multiple-domain functions	Simultaneous testing of multi-domain features to assess cross influences; testing specifically for target application
12	EDA assisted CoDesign	Different, incompatible EDA suites	EDA suites with a common referral language and APIs
13	WEEE	Electronics-only functionalities well addressed	Multi-domain functionalities difficult to address
14	Standardization	Standards in formfactor of individual packages	Platform technology with interface to EDA tools ("VHDL for SiP")
15	Security Aspects	No built-in security features	Depending on application, specific security features built into hardware may be needed
16	Cost Reduction	Cost challenges are addressed only on one level in the value chain	System level perspective to leverage synergies surpassing individual levels of value chain

High Attention

Midterm Attention

No immediate action needs foreseen

HETEROGENEOUS
INTEGRATION ROADMAP

Thank you for your attention!

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Images are referenced in the HIR – SiP&Module chapter, please see there