Agenda

- No Ordinary Times
- Transistor 75th Anniversary
- Heterogeneous Integration Roadmap
- Innovations & Microelectronics Resurgence
- Summary

No Ordinary Time

The World

- Climate Change
- War
- Geopolitical Conflict
- Economy – Inflation
- Covid 19 transitioning from pandemic to endemic
- Industry & Business: belt tightening & layoff

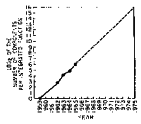
The Microelectronics World

- The United States CHIPS for America Act >>>> Investments in New Fabs & Packaging facilities, and talent workforce developments
- Similar scenario in Europe, Japan, Taiwan, India, Singapore, Malaysia, Vietnam …….
- New Fab/Facilities investment: $303 B - $464 B https://semiengineering.com/where-all-the-semiconductor-investments-are-going/
- Renaissance in microelectronics science & technology >>>>> Electronics Systems Resurgence for decades to come

75th Anniversary of the Transistor

December 16, 1947, John Bardeen and Walter Houser Brattain at Bell Labs NJ, demonstrated the first working transistor, now know as the point-contact. William Shockley, invented the the junction transistor in 1948. They initiated the first stone for the foundation of the Smart – Intelligent Society
NEXT are the inventions of Integrated Circuits (independently by Jack Kilby and Robert Noyce, 1958 & 1959). Moore's Law progress and fifty plus years of scientific and technological progress by scientists & technologists still going strong today. Semiconductor & Electronics are recognized as foundation pillars for digital transformation in service to society & humanity.

Moore's Law Paper



VII. Heat Problem

Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?

If we could shrink the volume of a standard high-speed digital computer to that required for the components themselves, we would expect it to glow brightly with present power dissipation. But it won't happen with integrated circuits. Since integrated electronic structures are two dimensional, they have a surface available for cooling close to each center of heat generation. In addition, power is needed primarily to drive the various lines and capacitances associated with the system. As long as a function is confined to a small area on a wafer, the amount of capacitance which must be driven is distinctly limited. In fact, shrinking dimensions on an integrated structure makes it possible to operate the structure at higher speed for the same power per unit area.

VIII. Day of Reckoning

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array. Perhaps newly devised design automation procedures could translate from logic diagram to technological realization without any special engineering.

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

IX. Linear Circuitry

Integration will not change linear systems as radically as digital systems. Still, a considerable degree of integration will be achieved with linear circuits. The lack of large-value capacitors and inductors is the greatest fundamental limitation to integrated electronics in the linear area.

By their very nature, such elements require the storage of energy in a volume. For high Q it is necessary that the volume be large. The incompatibility of large volume and integrated electronics is obvious from the terms themselves. Certain resonance phenomena, such as those in piezoelectric crystals, can be expected to have some applications for tuning functions, but inductors and capacitors will be with us for some time.

The integrated RF amplifier of the future might well consist of integrated stages of gain, giving high performance at minimum cost, interspersed with relatively large tuning elements.

Other linear functions will be changed considerably. The matching and tracking of similar components in integrated structures will allow the design of differential amplifiers of greatly improved performance. The use of thermal feedback effects to stabilize integrated structures to a small fraction of a degree will allow the construction of oscillators with crystal stability.

Even in the microwave area, structures included in the definition of integrated electronics will become increasingly important. The ability to make and assemble components small compared with the wavelengths involved will allow the use of lumped parameter design, at least at the lower frequencies. It is difficult to predict at the present time just how extensive the invasion of the microwave area by integrated electronics will be. The successful realization of such items as phased-array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar.

"Cramming More Components onto Integrated Circuits,"
Gordon Moore, *Electronics,* pp. 114–117, April 19, 1965

DAY OF RECKONING
"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."

A visionary statement for Heterogeneous Integration through Chiplets and SiP to continue Moore's Law 50 plus years Progress

Technology Roadmapping History

HIR HETEROGENEOUS INTEGRATION ROADMAP

1991

World's first Open Source Technology Roadmap, the National Technology Roadmap for Semiconductors (NTRS) sponsored by the US Semiconductor Industry Association (SIA).

1998

NTRS expanded forming the first Global Technology Roadmap. Europe, Japan, Taiwan, and Korea joined. It was renamed International Technology Roadmap for Semiconductors (ITRS).

2014

The benefits of Moore's Law scaling diminishing and decision was made to end ITRS.

2016

The last edition of the ITRS was published July 8, 2016

Heterogeneous Integration Roadmap (HIR)

Launched 10-10-2019
24 chapters
590 Pages
Free download
Download Link
https://eps.ieee.org/technology/heterogeneous-integration-roadmap

- **Sponsored by IEEE Electronics Packaging Society (EPS), SEMI, IEEE Electron Devices Society, IEEE Photonics Society and ASME Electronics & Photonics Division**
- **Comprehensively covers the complete microelectronics technology ecosystem: Industry, academia, and government organizations.**
- **Articulates state-of-the-art Advances in Technology & Science, Future directions, Significant roadblocks & Potential solutions**
- **Heterogeneous Integration Roadmap is the Roadmap for the Next Era of Moore's Law – Electronics Industry Resurgence- decades into the future.**

IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | IEEE ELECTRON DEVICES SOCIETY

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Heterogeneous Integration Roadmap Chapters

Covering the Microelectronics Systems Products & Technology Ecosystem

HIR HETEROGENEOUS INTEGRATION ROADMAP

HI Systems & Market Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Cross Cutting topics

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability (formed 2021)

Microelectronics Ecosystem
23 Technical Working Groups
Working in Collaboration

Heterogeneous Integration Components

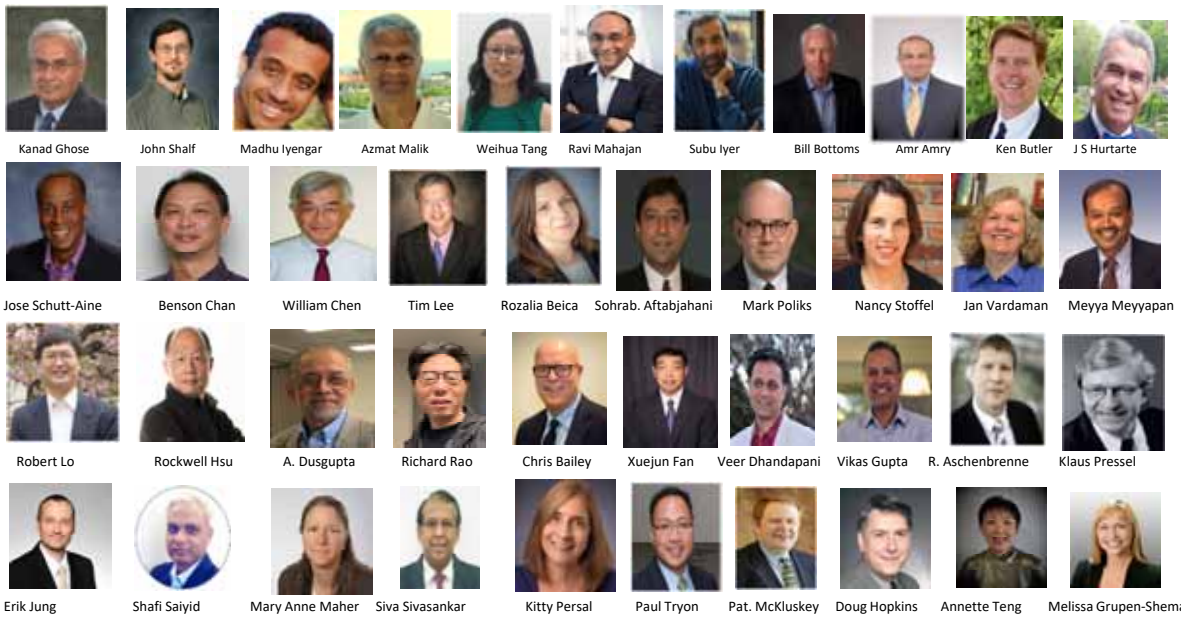
- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communication & Beyond

Integration Processes

- SiP & Module
- 3D +2D & Interconnect
- Wafer Level Packaging (fan in and fan out)

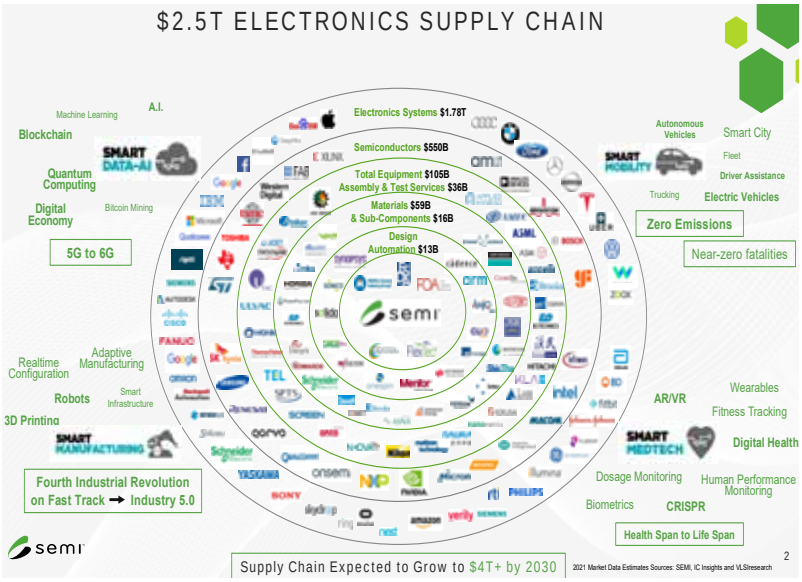
Co-Design + Simulation

- Co-Design
- Simulation



Heterogeneous Integration Roadmap Technical Working Groups Chairs & Co-Chairs

Electronics Products & Systems Supply Chain



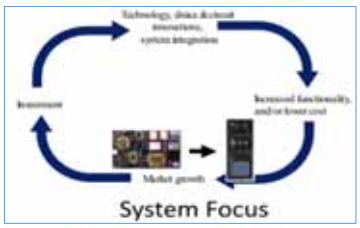
Acknowledgement: Tom Salmon (SEMI) & 2021 HIR Supply Chain Chapter TWG

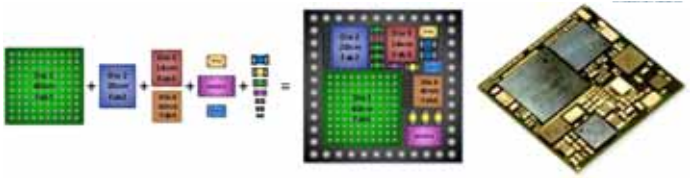
Looking Ahead – 2022 to 2026

- Total semiconductor market will grow almost 1.8x from 2019-2026
- Primarily fueled by Server / Storage / Comms Infra & Mobile Phone / Tablet segments
- Advanced nodes silicon
- **Chip architectures disaggregating** for cost & yield management
- Silicon **chiplet integration** enabled by **advanced packaging technology**

Source: Prismark 2022

Systems Focus in Heterogeneous Integration Roadmap





Heterogeneous Integration is defined as the integration of separately manufactured components into a higher-level assembly (Chiplets, SiPs, Modules) that, in the aggregate, provides enhanced functionality and improved operating characteristics

IEEE ELECTRONICS PACKAGING SOCIETY · ELECTRON DEVICES SOCIETY · IEEE Photonics Society · ASME · semi

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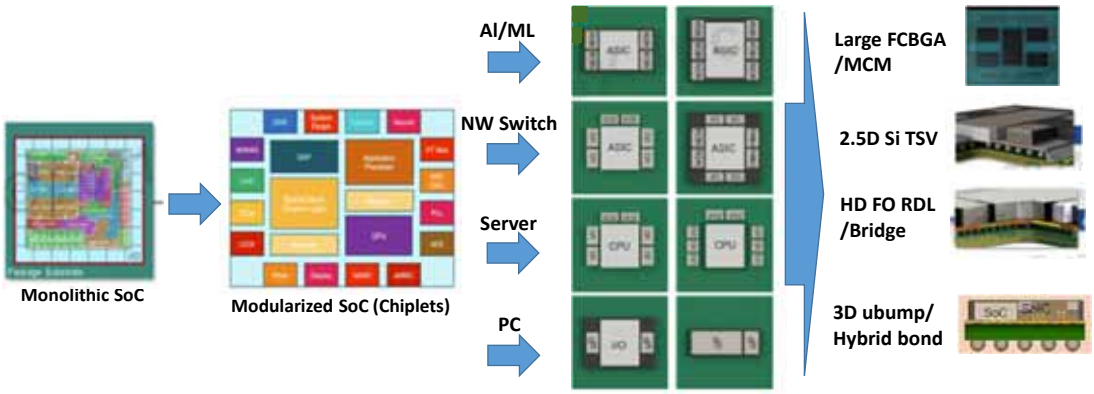
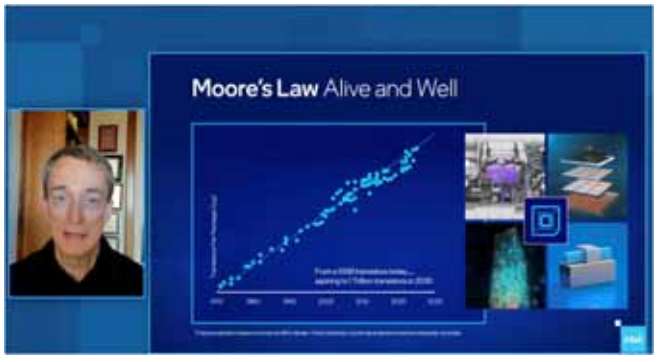
Chiplets – Heterogeneous Integration

Chiplet integration becoming mainstream for HPC through Advanced Packaging Platforms



Advanced packaging Heterogeneous Integration



IEEE Hot Chip 34 Conference August 21 - 24, 2022
Keynote One
"Semiconductors Runs the world"
Pat Gelsinger, Intel CEO.

In his talk Pat Gelsinger asserted that Moore's Law is alive & well. He articulated his vision for Intel and the crucial new role of advanced packaging in continuing the Moore's Law into the future.

He highlighted Intel packaging technology portfolio applied to chiplets in Intel component products including innovations in power delivery and advanced cooling technologies.

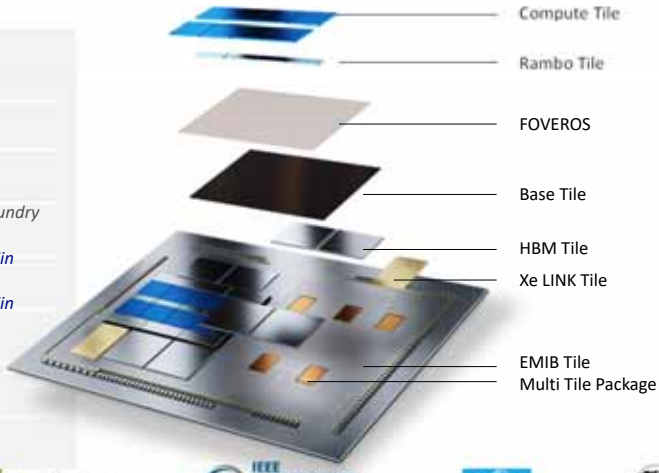
Intel Ponte Vecchio Chiplets Package for DOE Aurora Supercomputer

Blending Planar and 3D MCPs (EMIB + Foveros)

Reference: Sandeep Sane & Ravi Mahajan Advanced Packaging Technologies : Product Implementations at Hot Chip Conference August 21, 2021

Ponte Vecchio

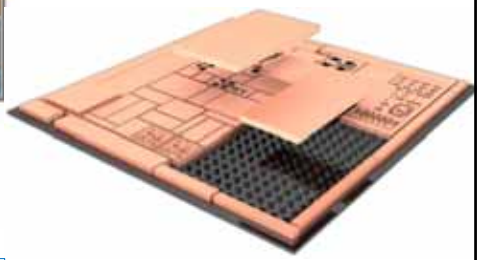
>100 Billion Transistors	
47 Active Tiles packaged on organic substrate	
16 Xe HPC Compute Tile	*Intel 7nm/External Foundry*
8 Rambo Tile	*Intel Enhanced SuperFin*
2 Xe Base Tile	*Intel Enhanced SuperFin*
11 EMIB Tile	*Intel Process*
2 Xe Link Tile	*External Foundry*
8 HBM Tile	*External Foundry*



Chiplets Technology & Products in AMD

Monolithic 32-core Chip
777mm² total area
1.0x Cost

4 x 8-core Chiplet, 213mm² per chiplet
852mm² total area (+9.7%)
0.59x Cost



Naffziger, S., Noah Beck, T. Burd, K. Lepak, Gabriel H. Loh, M. Subramony and Sean White. "Pioneering Chiplet Technology and Design for the AMD EPYC™ and Ryzen™ Processor Families : Industrial Product." 2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA) (2021): 57-70.

Many Thanks to John Shalf for sharing this slide

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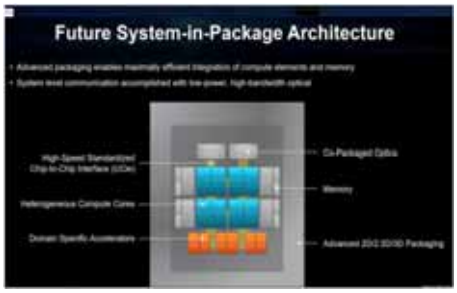
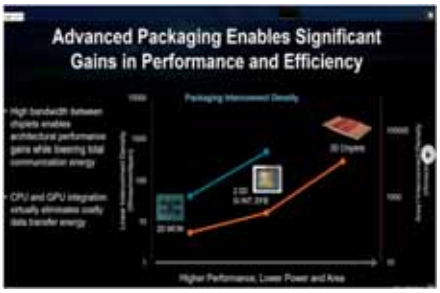
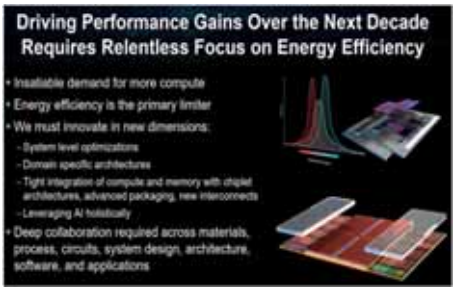


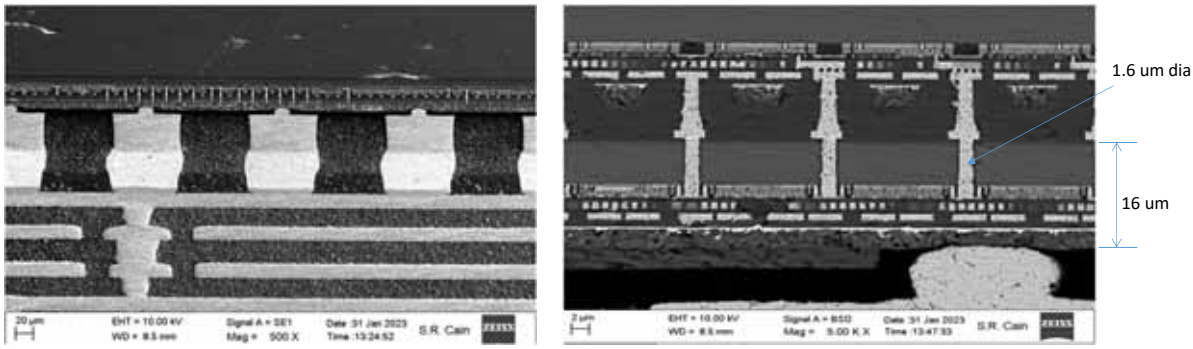




https://www.tomshardware.com/news/amd-puts-hopes-in-packaging-memory-on-logic-optical-comms-for-decade-ahead

Die Stacking in AMD Ryzen 7 5800X3D

Source: Binghamton University & Prismark Partners



Die to die interconnect: ~1.6 um dia columns on 15.5 um pitch

Summary

- **We are at a unique point in time when there is a global recognition on the critical roles of semiconductor and microelectronics as foundational pillars to nations economies.**
- **Heterogeneous Integration through Advanced Packaging for Chiplets & System-in Package is crucial to achieve best optimal systems: performance, power, cost, reliability, time to market and market penetration, paving the way for Microelectronics Resurgence for decades to come.**
- **HIR twenty-three technical working groups, represent the broad base ecosystem for advanced packaging innovations from package architecture & design, assembly, test, materials, equipment, tools, encompassing AI & ML.**
- **Basic research and collaboration across disciplines in Heterogeneous integration (e.g SiP & Chiplets & more) lays foundation for Renaissance in Science & Technology and Microelectronics Resurgence, in service to society and humanity.**

"For while we have our eyes on the future, history has its eyes on us"

Amanda Gorman, Poet Laureate