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Reliability Physics and Failure Mechanisms in Electronics Packaging

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Department of Mechanical Engineering

Course Organization

- **Module 1: Introduction**
- **Module 2: Thermal Stress-Induced Failures**
- **Module 3: Failure Analysis under Drop Test**
- **Module 4: Moisture-induced Reliability Issues**
- **Module 5: Electromigration**

Module 1

- **Module 1: Introduction**
- Module 2: Thermal Stresses-induced Failures
- Module 3: Failure Analysis under Drop Test
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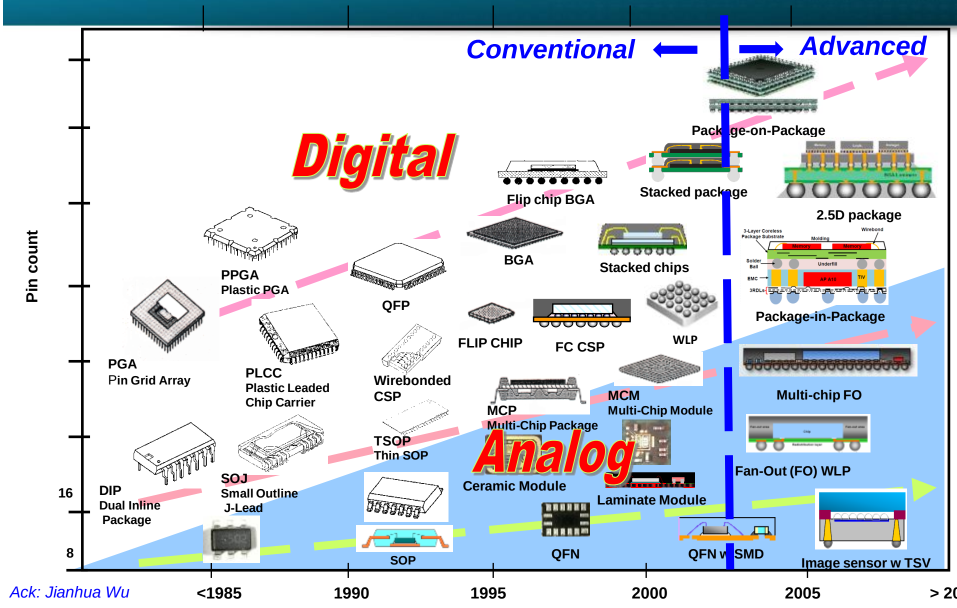
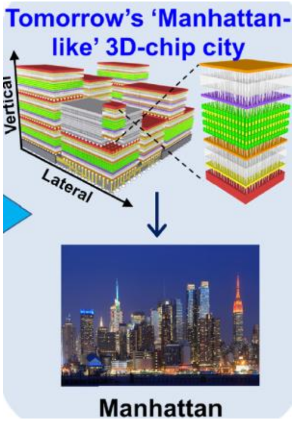
- Module 5: Electromigration

Electronics Packaging Evolution



Ack: Jianhua Wu

Through Hole → Surface Mount → Fine Pitch → Area Array (MCM) → Fan-Out WLP/TSV → 3D/heterogeneous integration



Ack: Kaustav Banerjee, UCSB ,Subhasish Mitra, Stanford

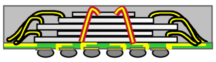
Conventional Electronics Packaging

wafer-level packaging

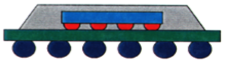
leadframe based

Quad Flat Leadless

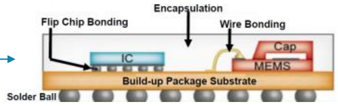
substrate based ball grid array (BGA)

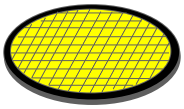


Stacked chip scale

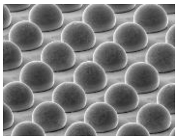


flip chip BGA

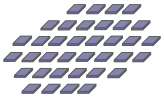




wafer



wafer bumping/RDL



dicing

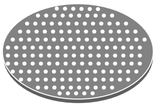
Fan-out (FO) Wafer Level Packaging (WLP)

- **Fan-out (FO) WLP: standard WLP on a plastic molded reconstituted wafer**

reconstituted wafer

“plastic molded” wafer

RDL/bumping



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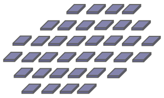
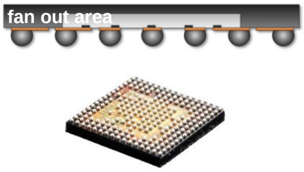
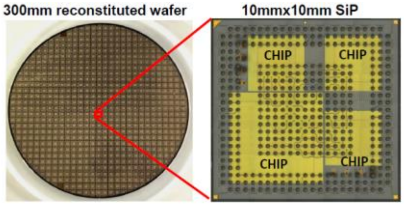
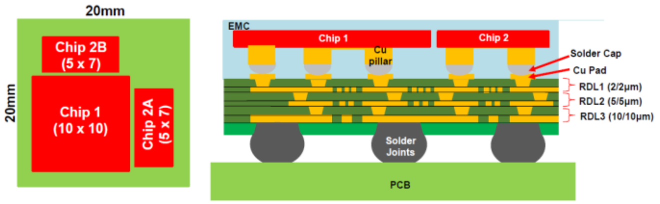






chip-first multi-chip FO

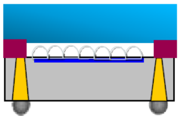


RDL-first multi-chip FO

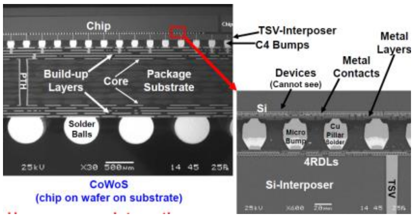
Fan XJ. Wafer level packaging (WLP): fan-in, fan-out and three-dimensional integration. 11th EuroSimE. April 25-18, 2010.

Enabling Interconnect Technologies for 3D Packaging

- **Through Silicon Via (TSV) Interposer**

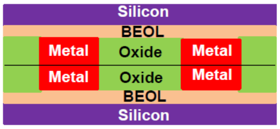


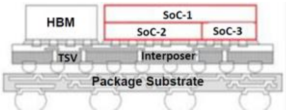
CMOS image sensor



CoWoS
(chip on wafer on substrate)

- **Hybrid bonding (Cu-Cu)**

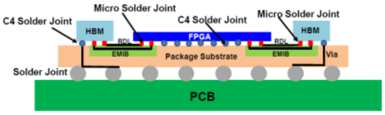




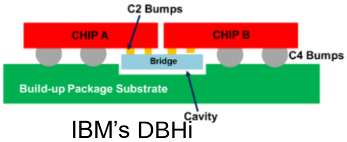
TSMC's SoC

Intel's Foveros

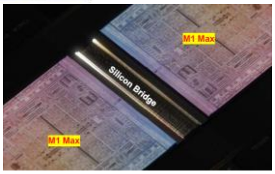
- **Bridge**



Intel's EMIB

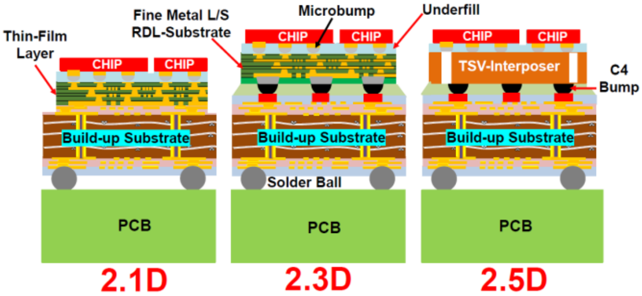


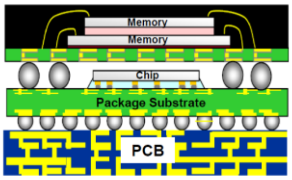
IBM's DBHi



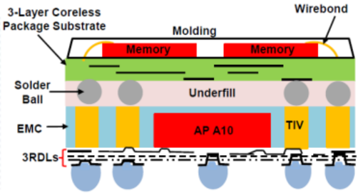
Apple's fusion

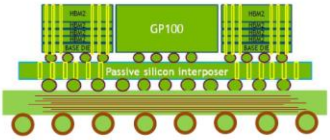
Heterogeneous Integration



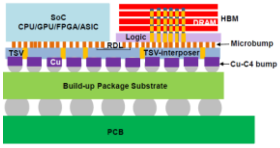


Package on package





NVidia's P100 with TSMC's CoWoS



Samsung's Interposer Cube-4

Apple/TSMC InFO (Integrated fan-out)

Lau, J.H., *Recent Advances and Trends in Advanced Packaging.* IEEE Transactions on Components, Packaging and Manufacturing Technology, 2022. **12**(2): p. 228-252.

Ack: John Lau, Unimicron

Advanced Packaging in "CHIPS and Science Act"

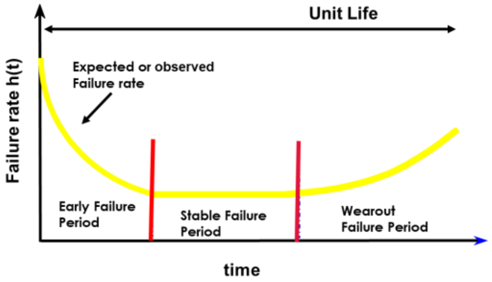
- **The next major wave of semiconductor innovation is expected to come from *heterogeneous integration* through advanced semiconductor packaging, as traditional silicon transistor scaling is unlikely to drive future long-term microelectronics innovation.**

-- White House: Report to President: Revitalizing the U.S. Semiconductor Ecosystem. (2022). The President's Council of Advisors on Science and Technology (PCAST)

- **One of the programs supported by CHIPS and Science Act is to create a National Advanced Packaging Manufacturing Program (NAPMP) to support and bolster semiconductor packaging R&D in the U.S.**
- **For the first time in history, electronics packaging is on the agenda on national stage.**

Reliability of Electronic Packages

- **Reliability describes the probability that a product will perform its intended function for a given time under specified operating (stress) conditions.**
- **The bathtub curve is a typical failure rate curve with three distinct parts to the failure rate.**
  - Early failure period.
  - Stable failure period.
  - Wear-out failure period.



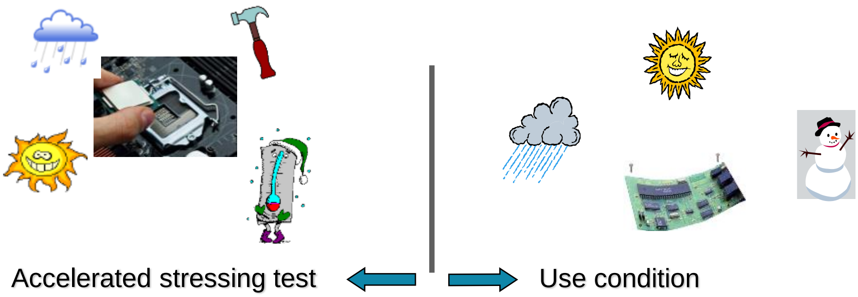
Zhang GQ, van Driel WD, Fan XJ. *Mechanics of Microelectronics.* Springer, 2006.

Reliability Physics and Failure Mechanisms

- **Reliability Physics uses the principles of physics to describe how physical, chemical, mechanical, thermal, or electrical failure mechanisms evolve over time and eventually induce failure.**
- **Ensuring the reliability of heterogeneously integrated semiconductor packaging imposes many new challenges that were never addressed in the past.**
- **Typical "stress" conditions**
  - Temperature (high, low, and **cyclic**)
  - Moisture
  - Voltage & current
  - Dynamic or static mechanical loads
  - Chemical exposure

Accelerated Stressing Test

- **How to determine whether a product will last 7 or 10 years in the field without taking 7 or 10 years to run reliability tests?**
  - Accelerate the time to failure by using stress test conditions that are more severe than field use.



Accelerated stressing test ⟵ | ⟶ Use condition

Typical Accelerated Stresses

Component Level Testing

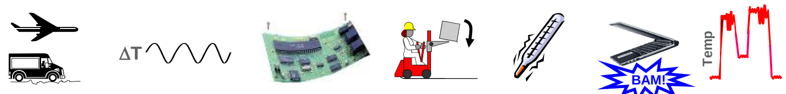
- **Preconditioning (Precon)**
  - Moisture + reflow temp
- **Bake**
  - High, Low temp bake
- **Temperature cycle**
  - Repeated high and low temp
- **Power cycle (Biased temp cycle)**
  - Repeated high and ambient temp
- **Burn-in**
  - High temp
  - Voltage & current
- **Steam or autoclave**
  - Elevated temp (121°C)
  - Moisture (100% RH)
- **THB (temp & humidity bias)**
  - Elevated temp (85°C)
  - Moisture (85 %RH)
  - Voltage & current (Bias)
- **HAST (Highly Accel'd Stress Test)**
  - High temp (130 °C)
  - Moisture (85% RH)
  - Voltage & current (Bias)
- **Mechanical shock/vibration**
  - Dynamic mechanical load

Board Level Testing

- **Temperature cycle**
  - Repeated high and low temp
- **Power cycle (Biased temp cycle)**
  - Repeated high and ambient temp
- **THB (temp & humidity bias)**
  - Elevated temp (85 °C)
  - Moisture (85%RH)
  - Voltage & current (Bias)
- **HAST (Highly Accel'd Stress Test)**
  - High temp (130°C)
  - Moisture (85% RH)
  - Voltage & current (Bias)
- **Bend/flex**
  - Dynamic mechanical load
- **Drop**
  - Dynamic mechanical load
- **Mechanical shock/vibration**
  - Dynamic mechanical load

Use Conditions

- **Use conditions are the environments that a product is exposed to throughout its lifetime, including**
  - Temperature (high, low, and cyclic)
  - Moisture
  - Voltage & current
  - Dynamic or static mechanical loads
  - Chemical exposure
- **Semiconductor packages' reliability is derived from the results of accelerated stress tests and relates to use conditions.**

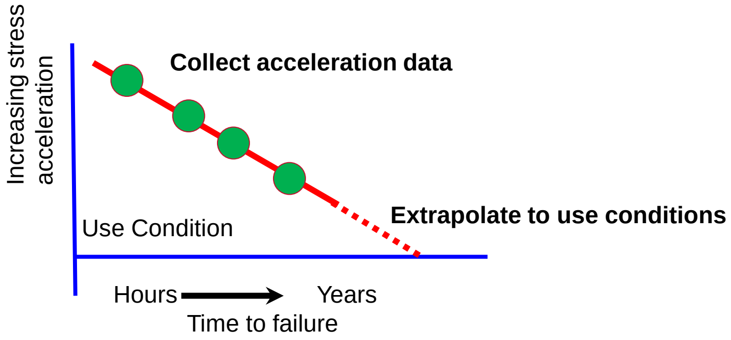


Shipping Shock   Temp Cycle   Bend   Reflow   Handling   Temp, RH   User Drop & Vibe   Power Cycle

Bent Pins, Singulation

Acceleration Models

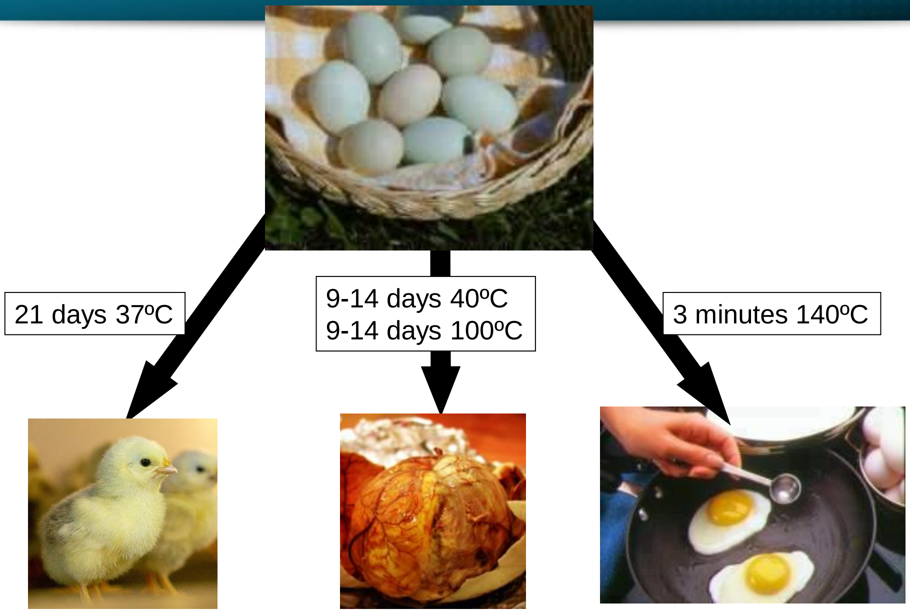
- **Acceleration models are usually based on the physics of failure underlying a particular failure mechanism.**
- **Acceleration factors (AFs) show how time-to-fail at an accelerated stress level (for one failure mode or mechanism) can be used to predict the time to fail at a use condition stress level.**



$$AF = \left(\frac{\Delta T_{stress}}{\Delta T_{use}}\right)^n$$

$$AF = \exp\left[\frac{E_{act}}{k_B}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

Risk of Acceleration



21 days 37ºC

9-14 days 40ºC
9-14 days 100ºC

3 minutes 140ºC

Course Organization

- Based on different stresses and failure mechanisms, this course is divided into 5 modules
- Module 1: Introduction
- Module 2: Thermal Stresses
- Module 3: Failure Analysis under Drop Test
- Module 4: Moisture-induced Reliability Issues
- Module 5: Electromigration

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End of Module 1

Thank you for your attention.

Questions?

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Reliability Physics and Failure Mechanisms in Electronics Packaging

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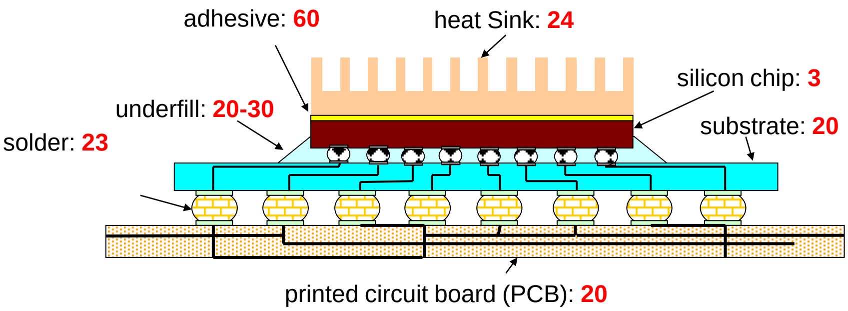
Module 2

- Module 1: Introduction
- **Module 2: Thermal Stress-induced Failures**
- Module 3: Failure Analysis under Drop Test
- Module 4: Moisture-induced Reliability Issues
- Module 5: Electromigration

Thermal Mismatch

- **Coefficient of Thermal Expansion (CTE): ppm/˚C**



adhesive: **60**

heat Sink: **24**

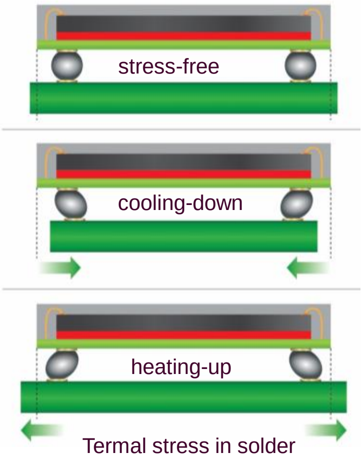
silicon chip: **3**

underfill: **20-30**

substrate: **20**

solder: **23**

printed circuit board (PCB): **20**

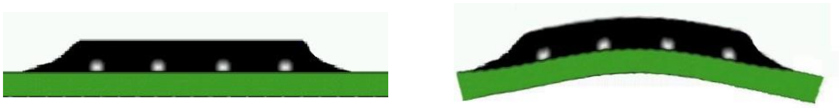


stress-free

cooling-down

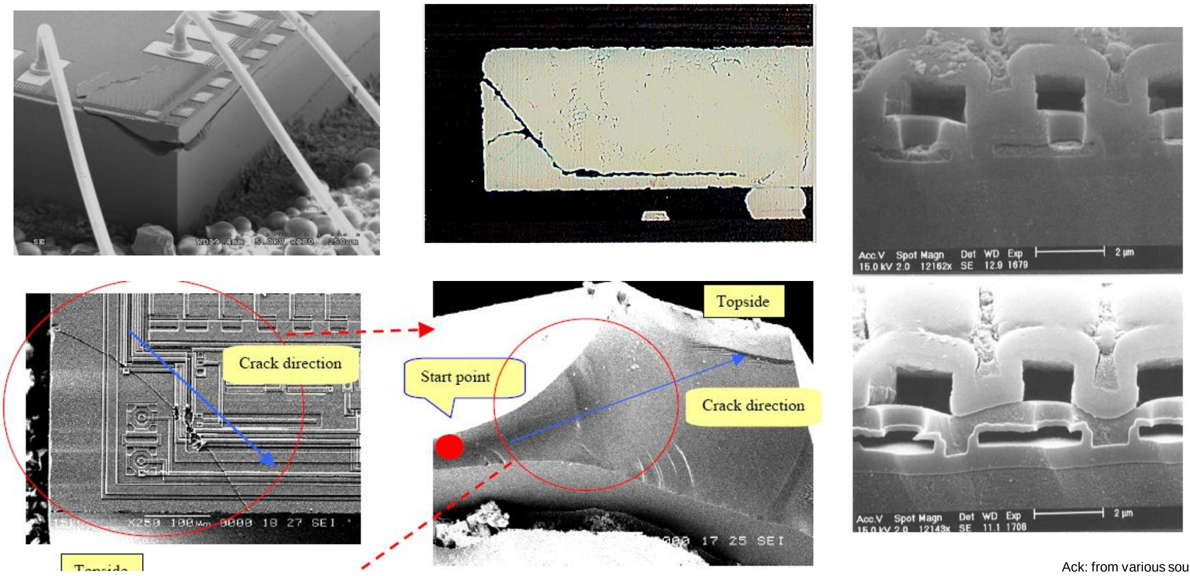
heating-up

Termal stress in solder



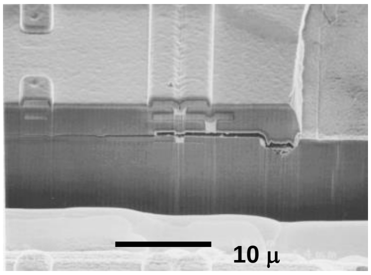
Package warpage during cooling down

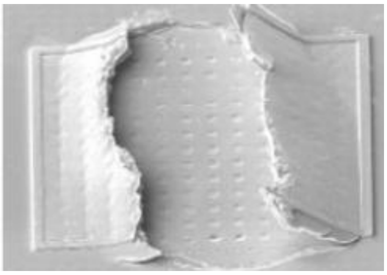
Die Cracking

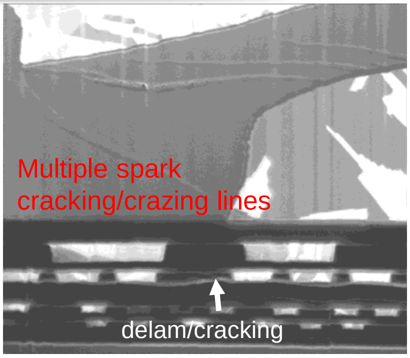


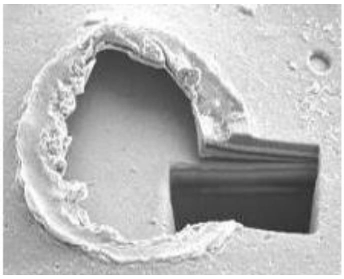
Ack: from various sources

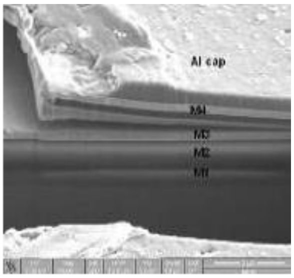
Thin-Film Cracking/Delamination

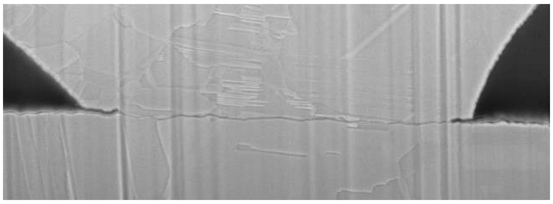






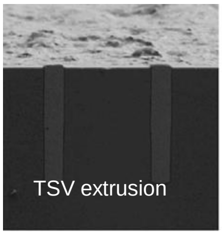


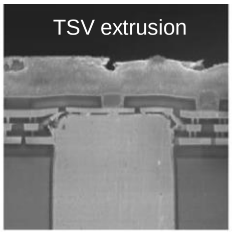


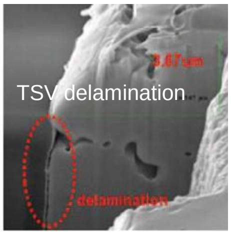


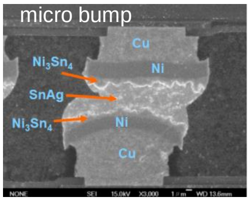
Ack: from various sources

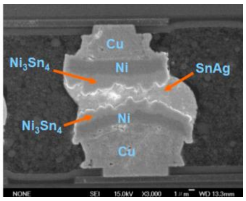
Interconnect Failure (TSV, micro bump, wire, RDL…)

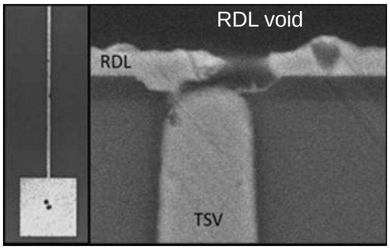






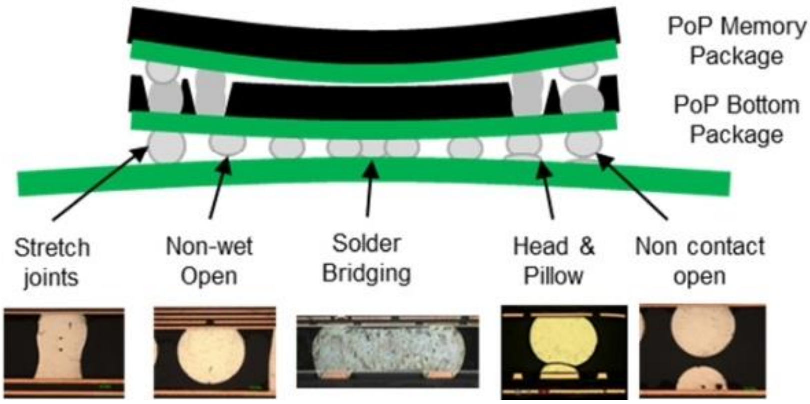






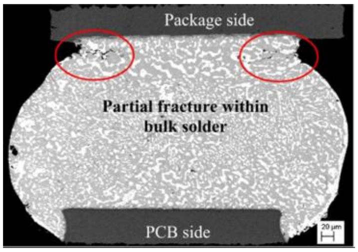
Ack: from various sources

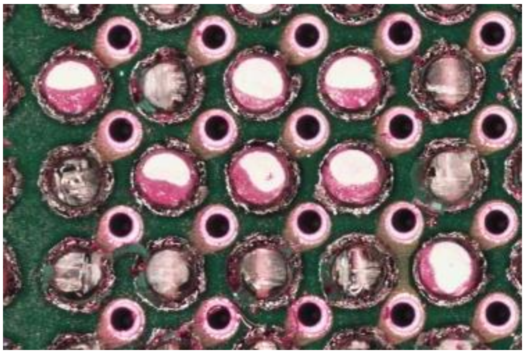
Warpage Issues

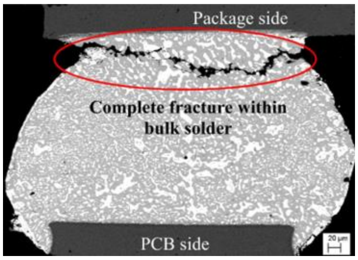


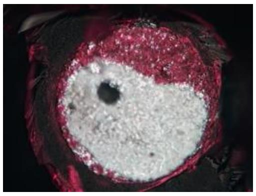
http://smt.iconnect007.com/index.php/article/98943/package-on-package-warpage-characteristics-and-requirements/98946/?skin=smt

Board Level Solder Ball Reliability



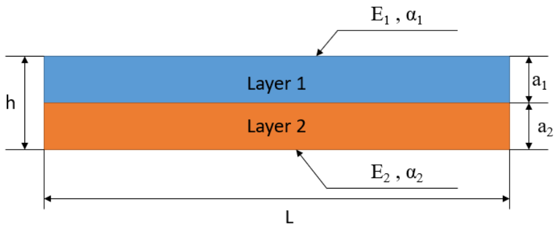


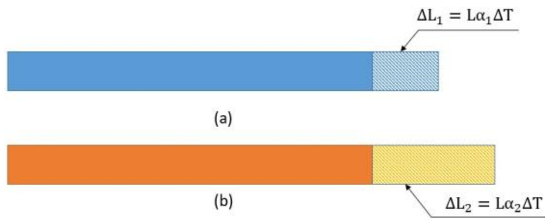


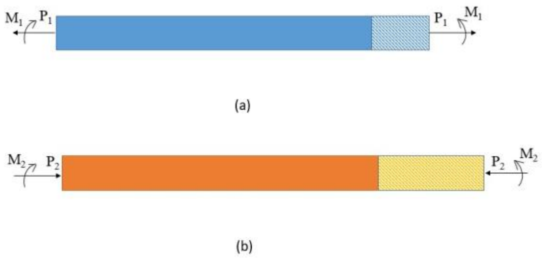


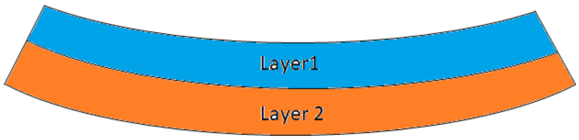
Ack: from various sources

Thermal Stress Analysis for Bi-layer Composite









Analytical Solution

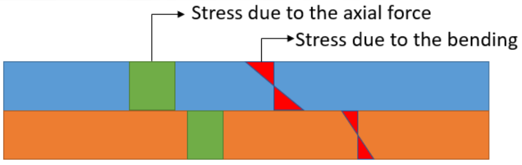
$$\sigma_x = \sigma_{axial} + \sigma_{bending}$$

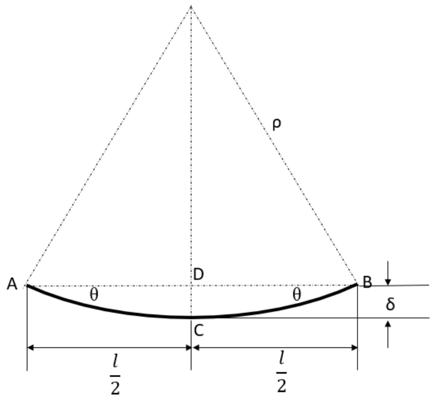
$$\sigma_{x1} = \frac{1}{\rho}\left(\frac{2}{ha_1}(E_1I_1 + E_2I_2) + \left(\frac{E_1a_1}{2}\right)\right)$$

$$\sigma_{x2} = -\frac{1}{\rho}\left(\frac{2}{ha_2}(E_1I_1 + E_2I_2) - \left(\frac{E_2a_2}{2}\right)\right)$$

$$k = \frac{1}{\rho} = \frac{(\alpha_2 - \alpha_1)\Delta T}{\frac{h}{2} + \frac{2}{h}(E_1I_1 + E_2I_2) * \left(\frac{1}{(E_1a_1} + \frac{1}{E_2a_2}\right)}$$

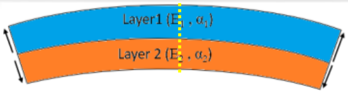
$$\delta = \frac{l^2}{8\rho}$$ warpage formula

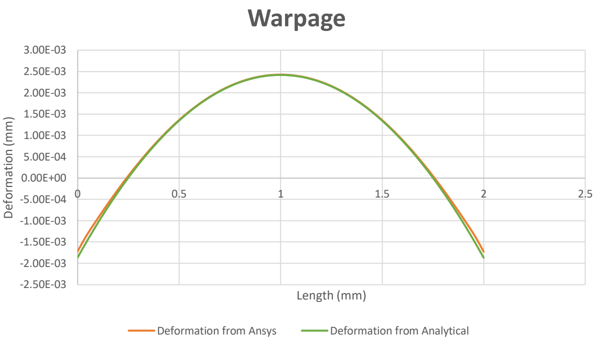


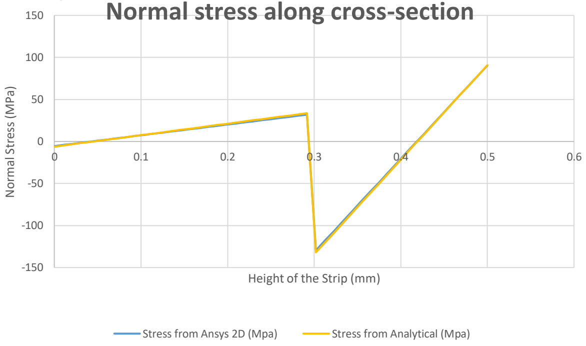


- **Package warpage can be obtained analytically.**

FEA vs. Analytical Solution

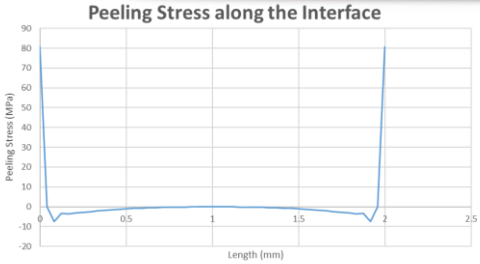


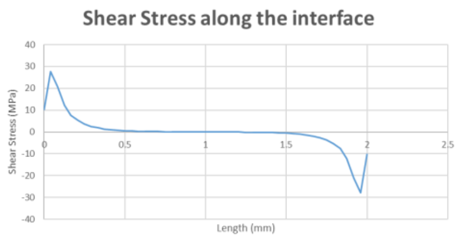


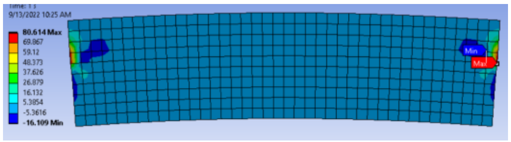


- **Analytical solutions provide excellent results compared to FEA results.**
- **However, peeling stress is completely neglected in the analytical solution.**

Peeling and Shear Stresses along the Interface





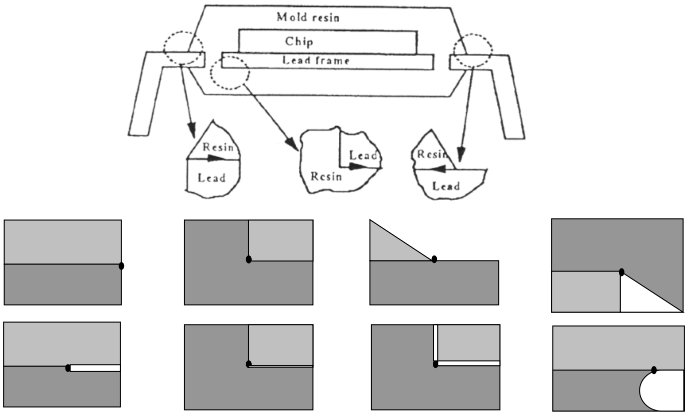


Mesh Size (mm)	Max Peeling Stress (MPa)
0.1	**58.5**
0.05	**80.6**
0.025	**106.9**
0.005	**183.9**

- Peeling stress at the interface is singular (theoretically infinity) at the free edge, thus mesh dependent.
- Both peeling and shear stresses are almost zero except near the free edges at both ends.

Ack: Mathews T Vellukunnel

Stress Singularity Issues



Fan XJ, Wang HB, Lim TB. Investigation of the underfill delamination and cracking for flip chip modules under temperature cyclic loading. *IEEE Transactions on Components, Manufacturing and Packaging Technologies*, 24(1), 84-91. 2001.

- Stresses are singular at the joints of dissimilar materials, crack tip, and free edge.
- Fracture mechanics deals with crack (or interface crack) only.

Take-Away Messages

- **The absolute value of the peeling stress components from FEA has no actual meaning due to stress singularity.**

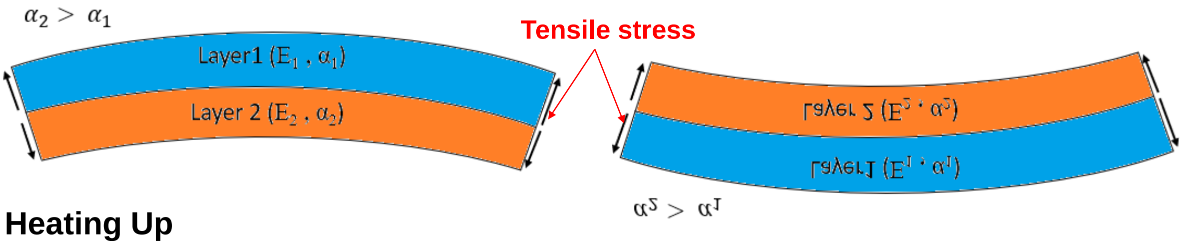
- **However, with the size and shape of the element fixed at the free edge, the stresses at free edge can still be used for a relative comparison among different design cases.**

- **The volume averaging method may be used to eliminate the mesh size dependence (to be discussed later).**

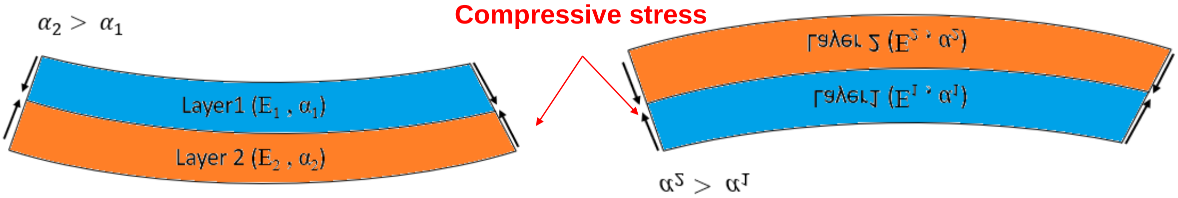
Ye G; Fan X; Zhang GQ; Practical aspects of thermomechanical modeling in electronics packaging: A case study with a SiC power package. *Microelectronics Reliability*, 132, 114514, 2022.

Tensile vs. Compressive Peeling Stress

- **Cooling Down**

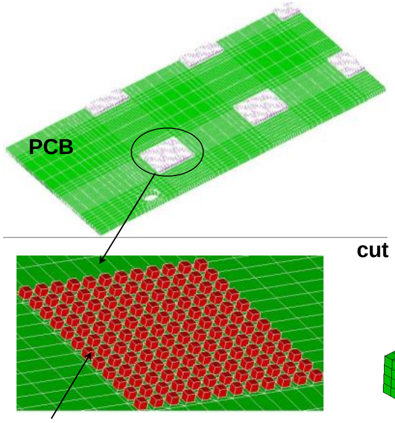


- **Heating Up**

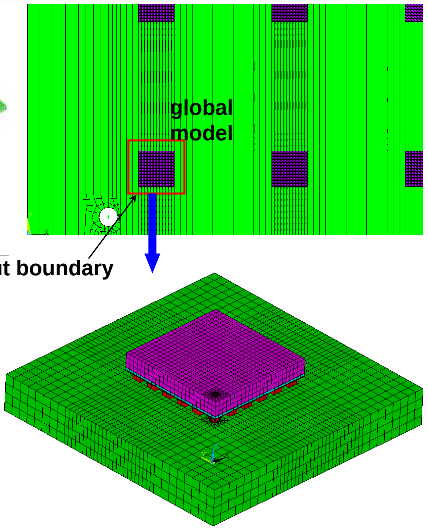


- Peeling stress is in tensile during cooling only, regardless of the warpage shape and materials' properties.

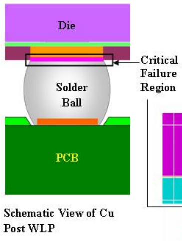
Global/Local Modeling



global model

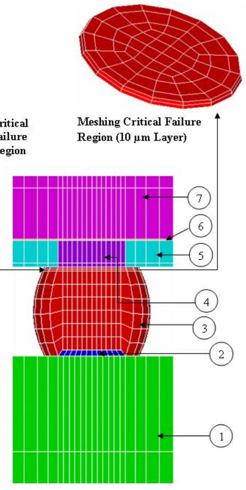


local model - level 1



Schematic View of Cu Post WLP

Part No.	Part Name
1	PCB
2	PCB Pad
3	Solder Ball
4	Copper Post
5	Epoxy
6	Passivation
7	Silicon Die

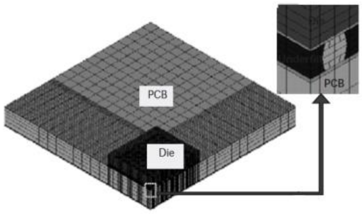


FE Model of Detailed Solder Ball

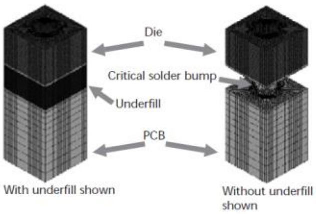
Local model – level 2

Fan XJ, Ranouta AS, Dhiman HS. Effects of package level structure and material properties on solder joint reliability under impact loading. *IEEE Transactions on Components, Packaging and Manufacturing Technology*. 3(1), 52-60. 2013.

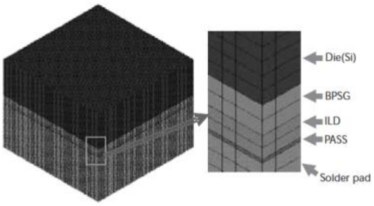
Global/Local Modeling (2)



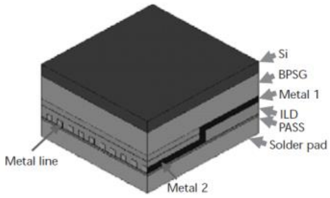
(a) package level



(b) critical solder level



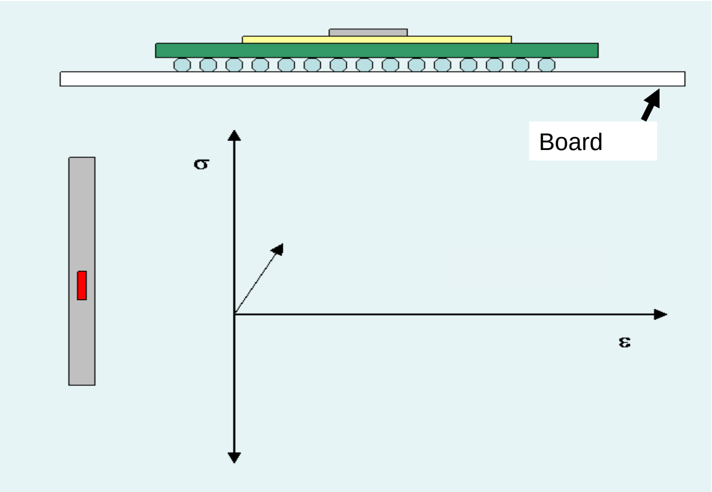
(c) die-solder interface level



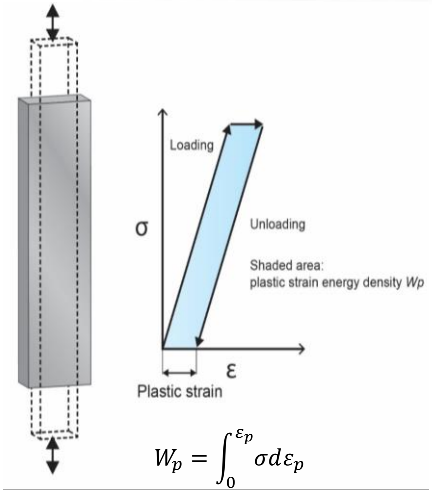
(d) interconnect level

Xuefeng Zhang, Se Hyuk Im, Rui Huang, and Paul S. Ho, Chip-Package Interaction and Reliability Impact on Cu/Low-k Interconnects, Chapter 2, UT Austin 2008/

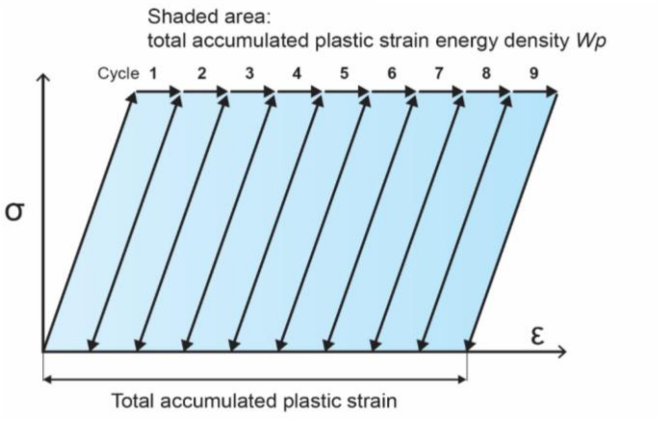
Temperature Cycling



Damage Accumulation during Cycling



$$W_p = \int_0^{\varepsilon_p} \sigma d\varepsilon_p$$

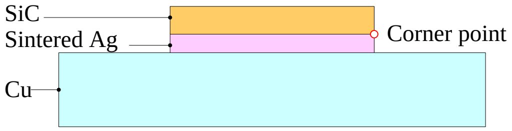


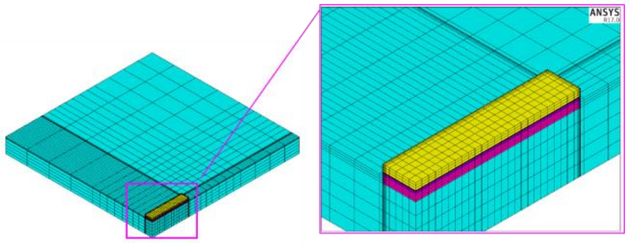
$$N_f = A\left(\Delta W_p\right)^{-n}$$

Coffin-Manson Equation

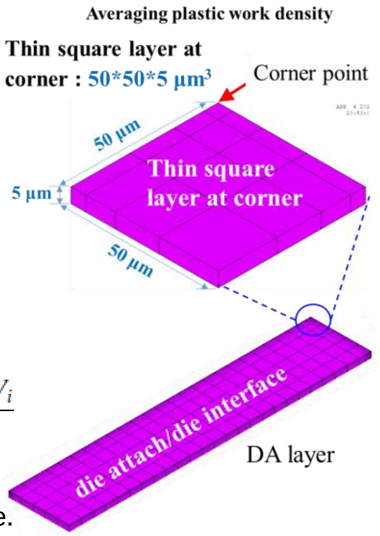
- Inelastic strain energy density W_p
- Inelastic strain energy density per cycle ΔW_p

ΔW_p : Volume Averaging





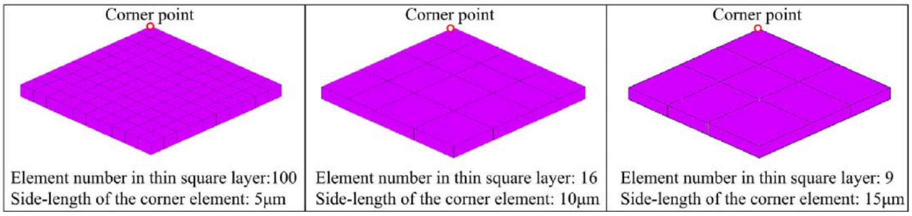
$$\Delta W_{\text{ave}} = \frac{\Sigma \Delta W_i V_i}{V}$$



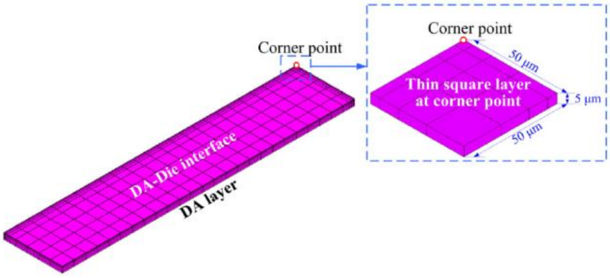
- Consider a power package with sintered-Ag as die-attach.
- Fracture always begins at the corners of the die-attach/die interface.
- Volume averaging is applied to obtain ΔW_p

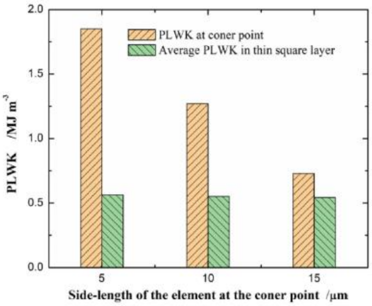
Ye G; Fan X; Zhang GQ; Practical aspects of thermomechanical modeling in electronics packaging: A case study with a SiC power package. *Microelectronics Reliability*, 132, 114514, 2022.

Mesh Independence



$$\Delta W_{\text{ave}} = \frac{\Sigma \Delta W_i V_i}{V}$$





- Mesh size dependence and stress singularity can be effectively eliminated.

Ye GG, Fan XJ, Zhang GQ, Practical aspects of thermomechanical modeling in electronics packaging: A case study with a SiC power package, Microelectronics Reliability 132 (2022) 114514.

Acceleration Models

- **Empirical models**
  - Temperature storage (Arrhenius equation-based)

$$AF = \exp\left[\frac{E_{act}}{k_B}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

- E_{act} Activation energy; failure mechanism dependent
- T_{stress} Temperature during stress test
- T_{use} Temperature during use
- k_B Boltzmann’s constant = 8.62 x 10-5 eV/K
- n exponent; failure mechanism dependent

Acceleration Models

- **Empirical models**
  - Temperature change

$$AF = \left(\frac{\Delta T_{stress}}{\Delta T_{use}}\right)^{n}$$

  - Temperature cycling for SAC

$$AF = \frac{N_0}{N_s} = \left(\frac{f_0}{f_s}\right)^{0.33}\left(\frac{\Delta T_s}{\Delta T_o}\right)^{1.8}\left(e^{1414\left(\frac{1}{T_{o\max}}-\frac{1}{T_{s\max}}\right)}\right)$$

  - ΔW_p-based

$$AF = \left(\frac{\Delta W_{stress}}{\Delta W_{use}}\right)^{n}$$

Vasudevan V, Fan XJ. An acceleration model for lead-free (SAC) solder joint reliability under thermal cycling, Proc of Electronic Components and Technology Conference (58th ECTC), 139-145. June 2008.

Summary

- Stresses singularity occurs at the free edge of bimaterial interface and corners/tips of dissimilar materials' joints. The absolute value of the stress components from finite element analysis has no actual meaning.
- Fracture mechanics deals with cracks (or interface cracks), but does not provide solutions without the presence of a crack.
- As a general practice for convenience, stresses at the singular points can still be used for a relative comparison among design cases, with the size and shape of the element fixed.
- Using the volume averaging method, the mesh size dependence can be effectively eliminated.
- Peeling stress at free-edge of biomaterial interface is always tensile during cooling, regardless of material properties.
- Global/local modeling in FEA provides a powerful approach to study chip-package interaction problems.

End of Module 2

Thank you for your attention.

Questions?

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Reliability Physics and Failure Mechanisms in Electronics Packaging

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Department of Mechanical Engineering

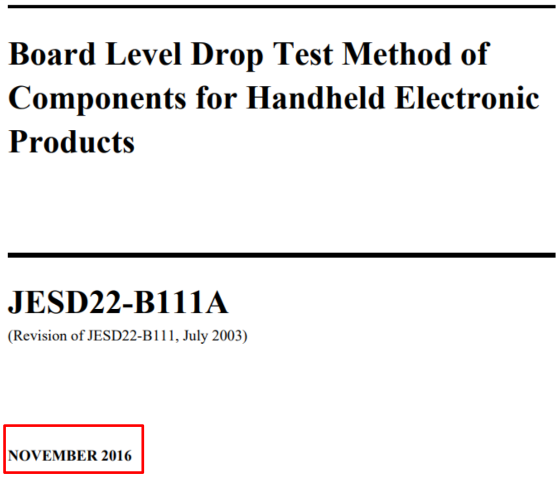
Module 3

- Module 1: Introduction
- Module 2: Thermal Stress-induced Failures
- **Module 3: Failure Analysis under Drop Test**
- Module 4: Moisture-induced Reliability Issues
- Module 5: Electromigration

ice Drop

- **Handheld electronic products are susceptible to drop impact failure.**
  - Frequently falls to rigid ground during transportation or usage.
  - Lead-free solder makes it worse.
- **The reliability performance of IC packages during drop impact has become a great concern.**

JEDEC Test Standard JESD22-B111A



Board Level Drop Test Method of Components for Handheld Electronic Products

JESD22-B111A

(Revision of JESD22-B111, July 2003)

NOVEMBER 2016

- **Board level drop test standard JESD22-B111A was released in 2003.**
- **Revision was made in 2016.**

Comparison of Two Versions of JESD22-B111A

2003 version

15 components

2016 version

four components or one component

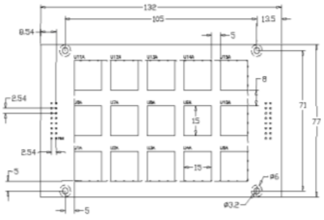
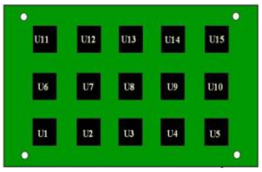
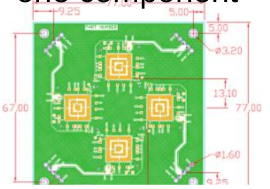
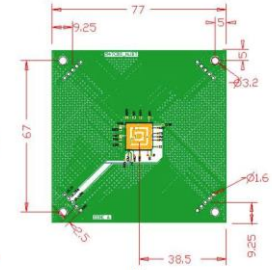


Figure 1. Test board size and layout.



Board and BGA Layout





(b)

Drop Test Table Setup

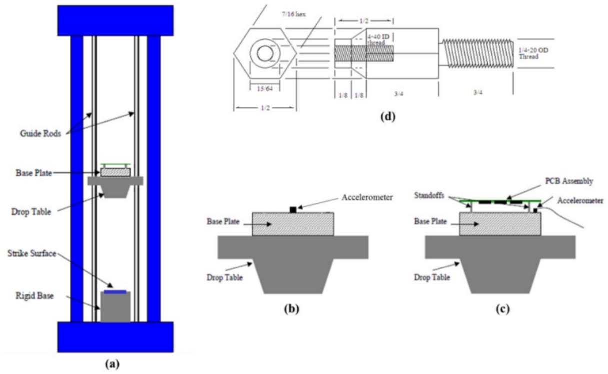
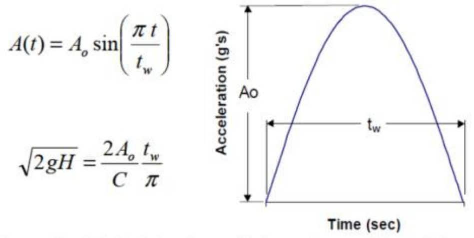


Figure 3 — (a) Typical drop test apparatus, (b) pre-characterization set up without test board, (c) assembly set up with board, and (d) a sample stand-off design.



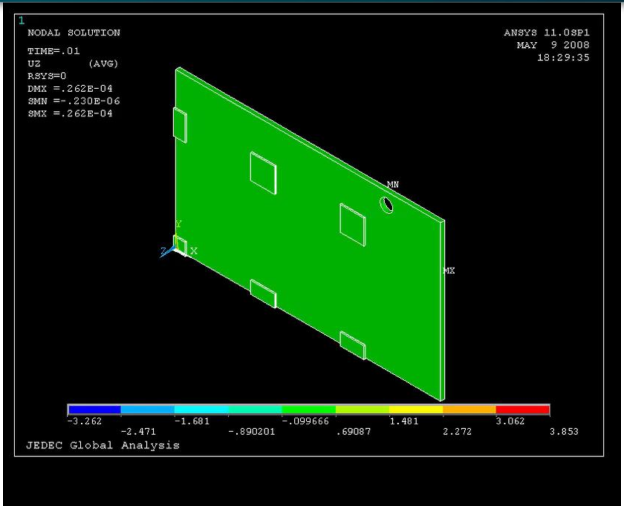
$$A(t) = A_o \sin\left(\frac{\pi t}{t_w}\right)$$

$$\sqrt{2gH} = \frac{2A_o}{C}\frac{t_w}{\pi}$$

Figure 5 — Typical shock test ½ sine pulse graphic and formulas

- Condition B: 1500g, 0.5-millisecond duration, half-sine pulse. Shock pulse applied to drop table measured close to support posts/spacers of PCB.
- Components face down.

Finite Element Analysis (FEA)



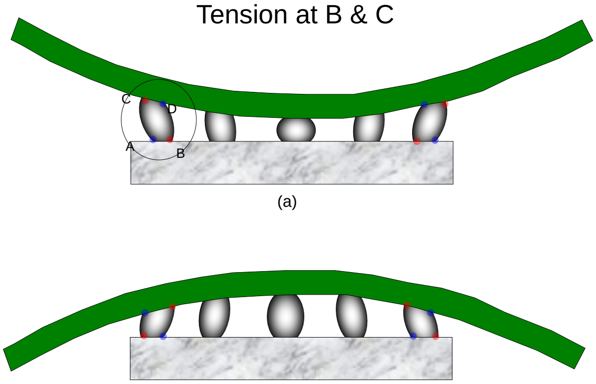
```
1
NODAL SOLUTION                                  ANSYS 11.0SP1
                                                MAY  9 2008
TIME=.01                                          18:29:35
UZ          (AVG)
RSYS=0
DMX =.262E-04
SMN =-.230E-06
SMX =.262E-04
```

- After the drop table hits the surface, the impact energy is converted to board vibration, causing components failure.

Fan XJ, Ranouta AS. Finite element modeling of system design and testing conditions for component solder ball reliability under impact. IEEE Transactions on Components, Packaging and Manufacturing Technology. 2(11), 1802-1810, 2012.

Illustration of Board Bend during Vibration

Tension at B & C



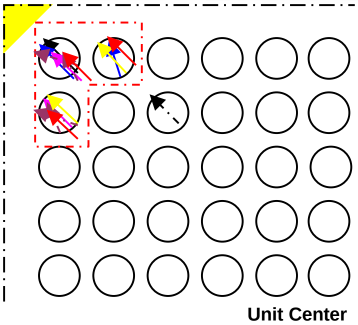
(a)

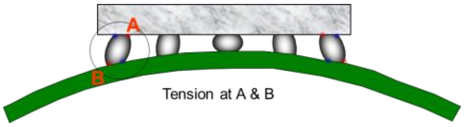
(b)

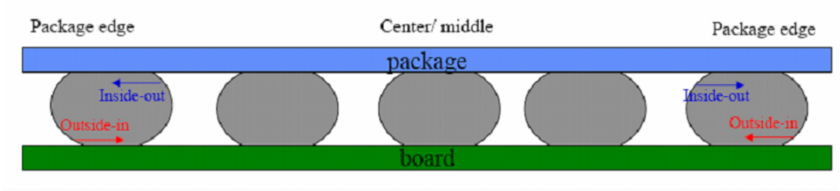
- During board vibration, solder balls inner side next to the package (Point B) and outer side next to the board (Point C) are in maximum tension.

Zhou T and Fan XJ. Effect of system design and test conditions on wafer level package drop test reliability. SMTA International. October 2013.

Crack Propagation Pattern





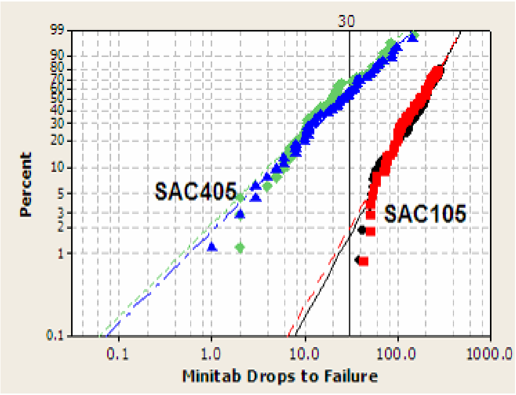


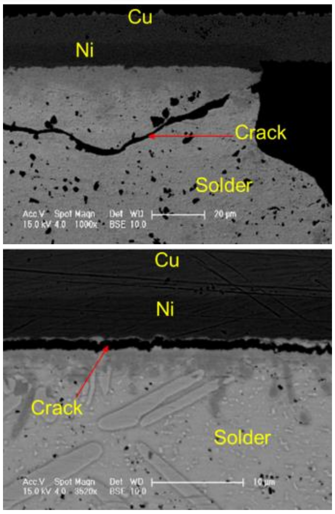
- **Failure occurs at the corner balls.**

Ack: from various sources

SAC405 vs. SAC105

SAC105/405 with NiAu



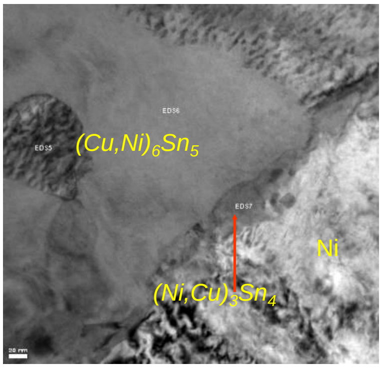


- SAC 105 (Sn1.0Ag0.5Cu) shows better drop performance that SAC 405; They have different failure mode.

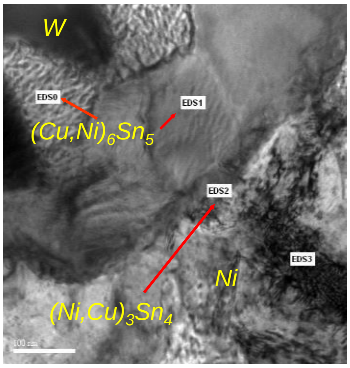
Ack: from various sources

IMC Microstructure

SAC105/NiAu



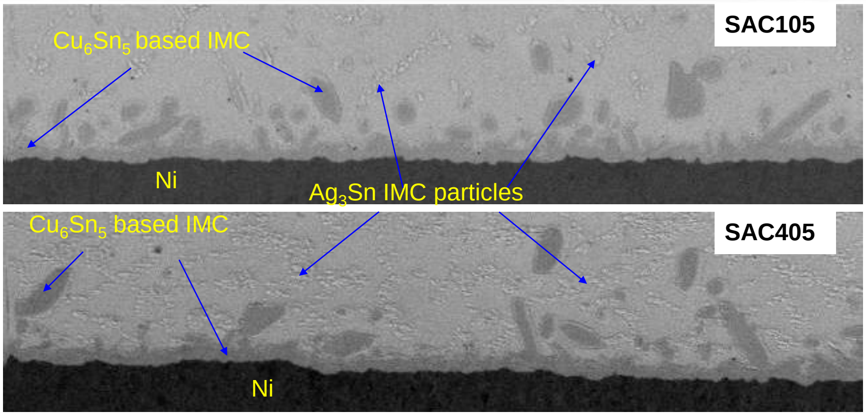
SAC405/NiAu



- SAC 105 and SAC 405 show same interfacial microstructure, Cu_6Sn_5 and Ni_3Sn_4 based IMCs were found in both alloy, indicating the drop performance difference was not due to IMC.

Ack: from various sources

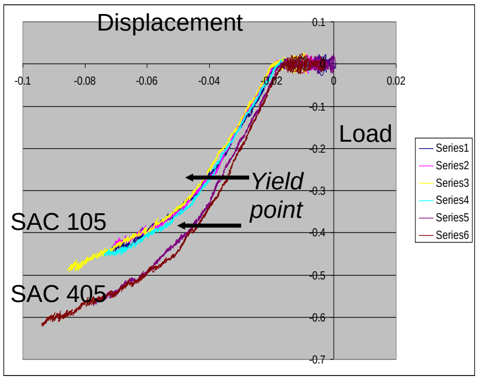
IMC Microstructure

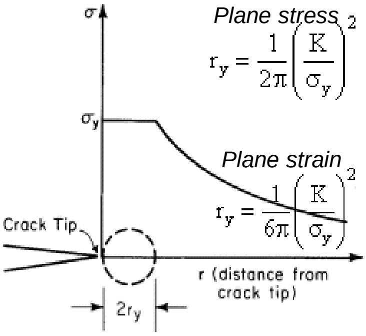


- **More Ag_3Sn IMC particles in SAC405.** More Ag_3Sn particles cause higher yield stress.

Ack: from various sources

Plastic Deformation vs. IMC Failure



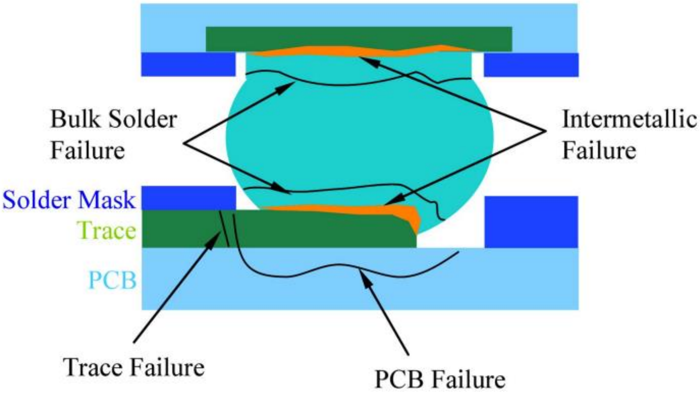


- **SAC 405 shows higher yield stress, meaning it has smaller plastic zone size, lower toughness, worse drop performance**

Ack: from various sources

Failure Mode during Drop Test

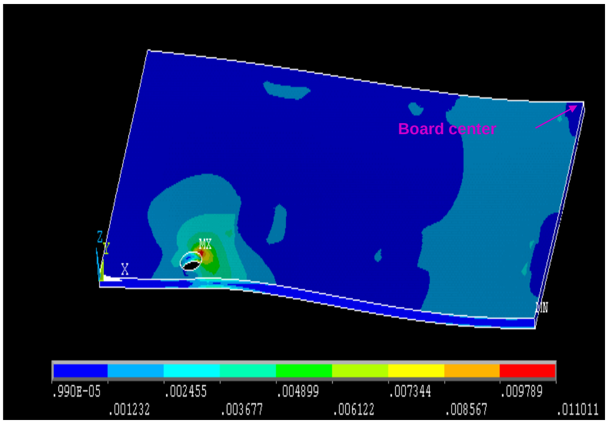
- IMC at package side
- IMC at board side
- Bulk solder at package side
- Bulk solder at board side
- Trace
- PCB failure (pad lift)



http://www.koreascience.or.kr/article/JAKO201106737200684.pdf

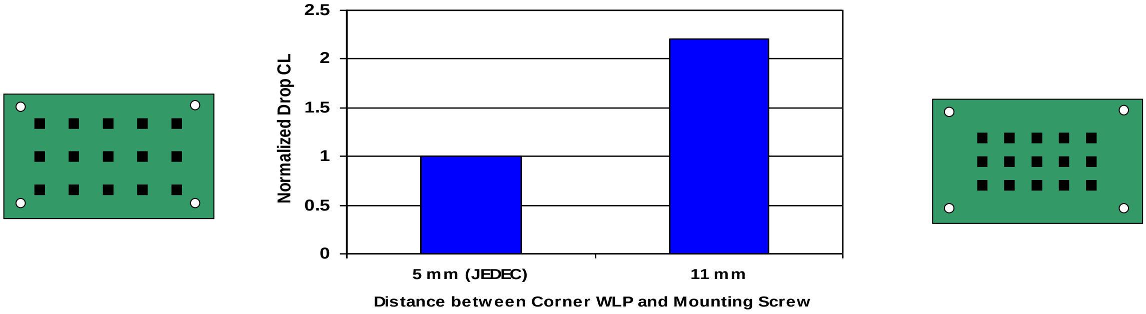
Board Deformation during Drop Test

- **There is high strain gradient next to mounting hole**



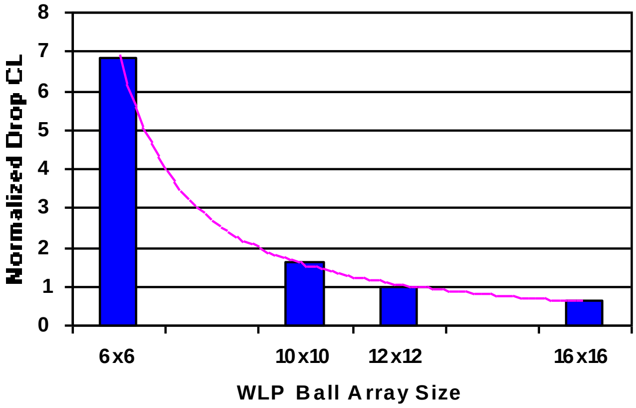
Fan XJ, Ranouta AS, Dhiman HS. Effects of package level structure and material properties on solder joint reliability under impact loading. *IEEE Transactions on Components, Packaging and Manufacturing Technology*. 3(1), 52-60. 2013.

Effect of Mounting Screw



- Corner component is sensitive to its distance to the mounting screws.

Package Size Effect



- Drop reliability sharply decrease with increased array size (power law).

Summary

- JEDEC test standard JESD22-B111A was updated in 2016 and adopted two different layouts of BGA components.
- The failure modes between SAC 405 and 105 were different.
- When a BGA component is close to the mounting screws, its drop performance is very sensitive to its distance from the mounting screws. Therefore, it is not appropriate to judge the BGA's drop test reliability in such a situation.
- Larger size of BGA packages are significantly worse in drop test performance.
- During drop test, crack propagation starts from the inner side of corner solder balls on package side, or the outer side on board side.
- Other failure modes may occur during drop test, such as pad crater or trace crack in PCB.

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End of Module 3

Thank you for your attention.

Questions?

Reliability Physics and Failure Mechanisms in Electronics Packaging

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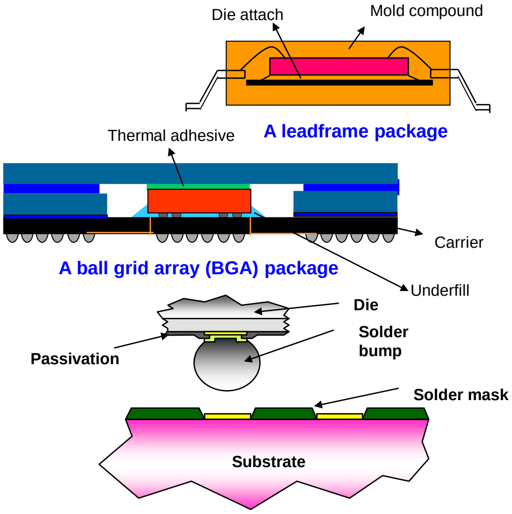
Module 4

- Module 1: Introduction
- Module 2: Thermal Stress-induced Failures
- Module 3: Failure Analysis under Drop Test
- **Module 4: Moisture-induced Reliability Issues**
- Module 5: Electromigration

Polymer Materials in Electronic Packaging

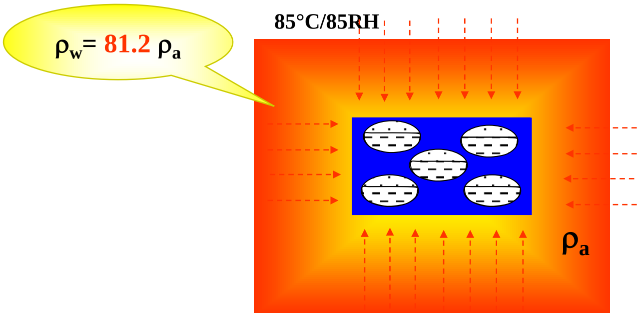
- **Bulk-form**
  - encapsulation (e.g. mold compound)
  - substrate …
- **Adhesives**
  - die-attach, underfill
  - thermal adhesives …
- **Thick- or thin- film**
  - solder mask
  - passivation



Fan XJ, Suhir, E. (eds.). *Moisture Sensitivity of Plastic Packages of IC Devices.* Springer, New York, 2010.

Moisture Absorption in Polymeric Materials

$\rho_{w:}$ moisture density in polymeric material
$\rho_{a:}$ ambient moisture density under 85°C/85%RH



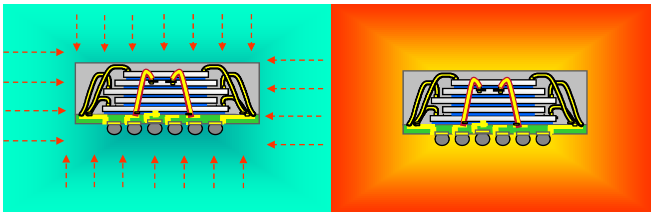
Moisture condensation in a typical underfill

- **Under 85°C/85%RH condition, ρ_w= Csat = 2.47e-2 g/cm^3 = 81.2 ρ_a (Csat: saturated moisture concentration)**
  - Moisture is condensed into liquid state and stays in micro/nano-pores or free volumes (in bulk or at interface).
  - Moisture density inside material is a few orders higher than ambient moisture density.
  - Moisture vaporizes at reflow, possibly still at mixed liquid/vapor phases.

Fan XJ, Lee SWR, Han Q. Experimental investigations and model study of moisture behaviors in polymeric materials. *Microelectronics Reliability* 49, 861–871. 2009.

Moisture Sensitivity Test

- **Moisture sensitivity test (precondition, or Precon) - IPC/JEDEC J-STD-020C**
  - Moisture absorption + reflow
  - Moisture absorption: hundred hours
  - Reflow: short time period (3 – 5 minutes)



Moisture absorption

Reflow process

MSL (Moisture Sensitivity Level) and Reflow Profiles

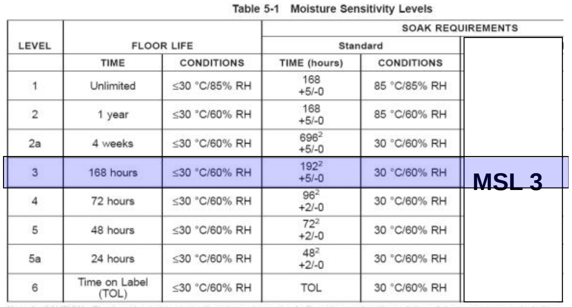


Table 5-1 Moisture Sensitivity Levels

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS	
			Standard	
	TIME	CONDITIONS	TIME (hours)	CONDITIONS
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH
2a	4 weeks	≤30 °C/60% RH	696^{2} +5/-0	30 °C/60% RH
3	168 hours	≤30 °C/60% RH	192^{2} +5/-0	30 °C/60% RH
4	72 hours	≤30 °C/60% RH	96^{2} +2/-0	30 °C/60% RH
5	48 hours	≤30 °C/60% RH	72^{2} +2/-0	30 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48^{2} +2/-0	30 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH

MSL 3

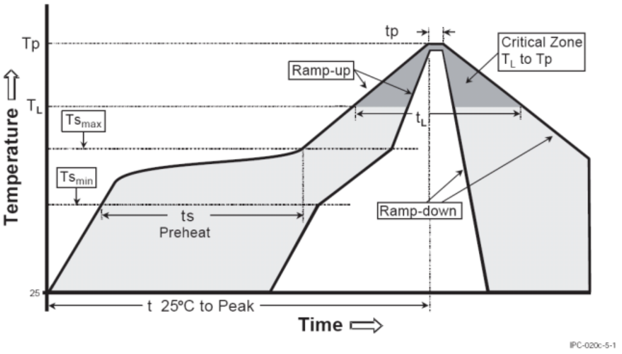
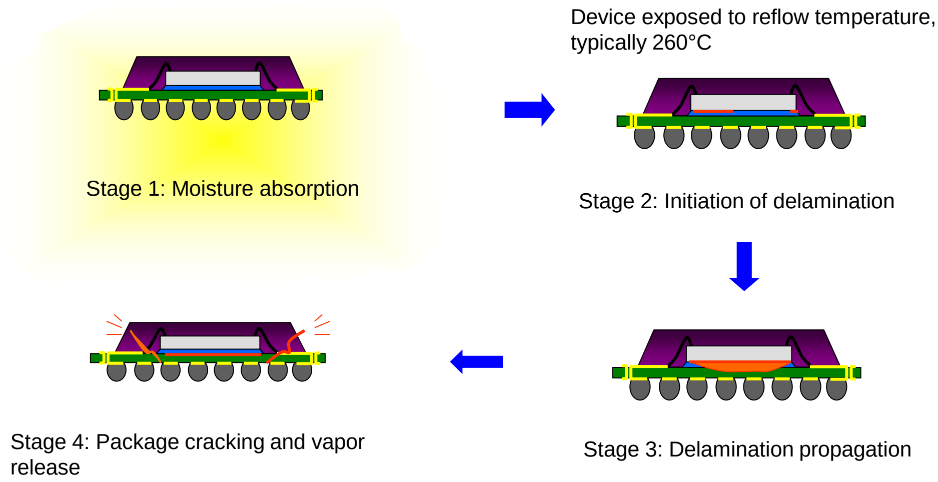


Illustration of Precon Test



Stage 1: Moisture absorption

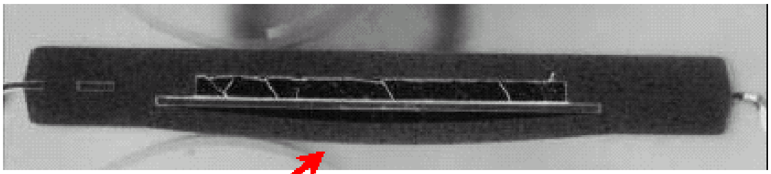
Device exposed to reflow temperature, typically 260°C

Stage 2: Initiation of delamination

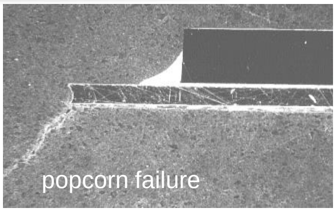
Stage 3: Delamination propagation

Stage 4: Package cracking and vapor release

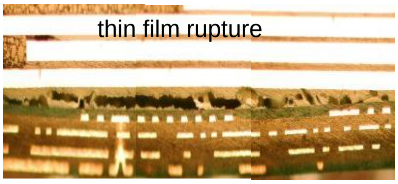
Failures at Precon Test



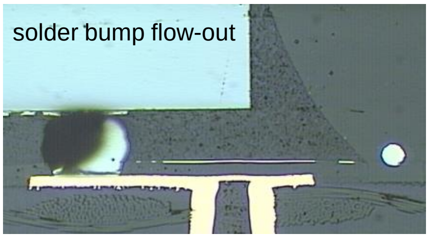
package bulging



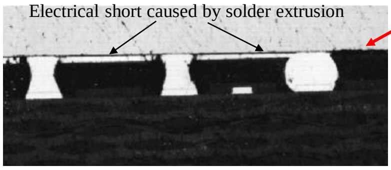
popcorn failure



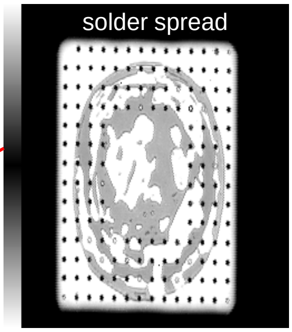
thin film rupture



solder bump flow-out



Electrical short caused by solder extrusion



solder spread

Ack: from various sources

Key Failure Mechanisms

- **Interface adhesion is reduced significantly, especially in the presence of moisture at high temperatures.**
- **Polymer materials become very compliant at reflow temperature.**
- **Absorbed moisture cannot be escaped sufficiently during reflow.**
- **High vapor pressure accelerates the failure.**

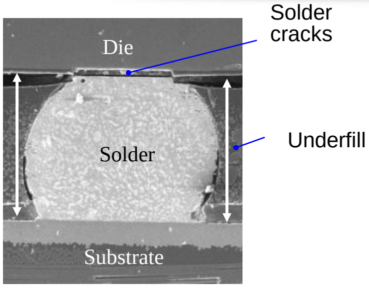
- **What is needed?**
  - Moisture diffusion
  - Integrated stress analysis
  - Vapor pressure analysis
  - Material properties at high temperatures, including adhesion.

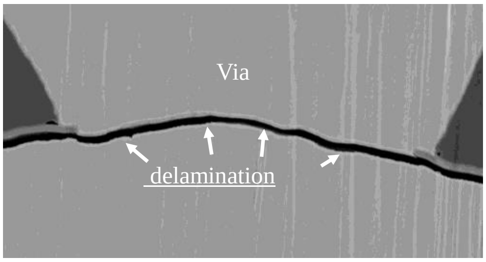
Fan XJ, Zhang GQ, van Driel WD, Ernst LJ. Interfacial delamination mechanisms during soldering reflow with moisture preconditioning, *IEEE Transactions on Components and Packaging Technologies* 31(2), 252-259, 2008.

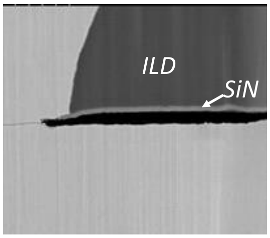
TH and HAST Condition (Unbiased)

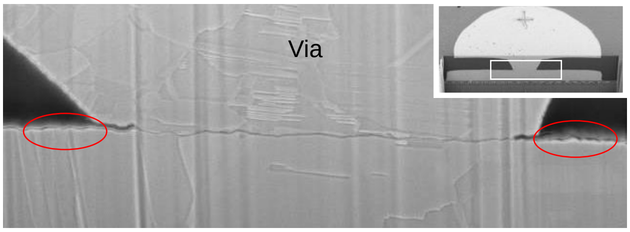
- **TH (temp & humidity)**
  - Elevated temp (85 °C) + moisture (85 %RH)
- **HAST (Highly Accelerated Stress Test)**
  - High temp (130 °C) + moisture (85% RH)
- **Steam or Autoclave**
  - Elevated temp (121 °C) + moisture (100% RH)

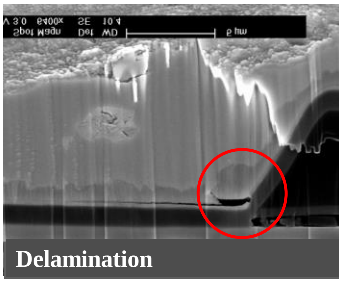
Failures during HAST or THB without Bias











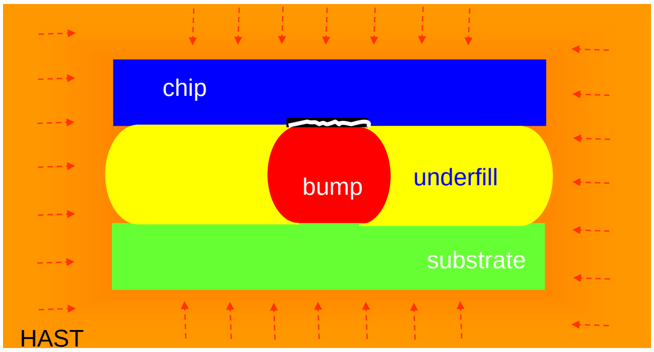
Ack: from various sources

Key Failure Mechanisms during Unbiased HAST

- **Interface adhesion is lost in the presence of moisture.**
- **Swelling of polymer materials.**

- **What is needed?**
  - Moisture diffusion
  - Swelling properties
  - Adhesion properties with moisture.

Illustration of Swelling-induced Failures during HAST

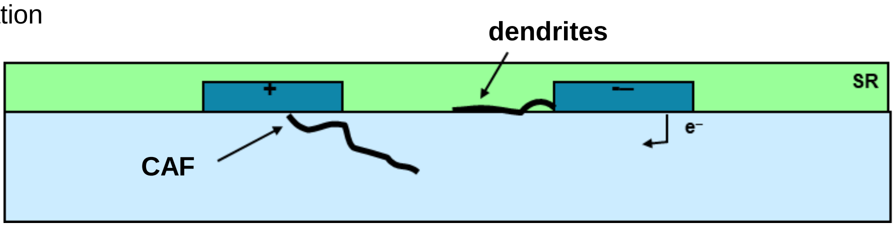


- Additional tensile stress/strain is generated in ILD layer due to swelling of underfill, causing delamination/cracking in bump region.

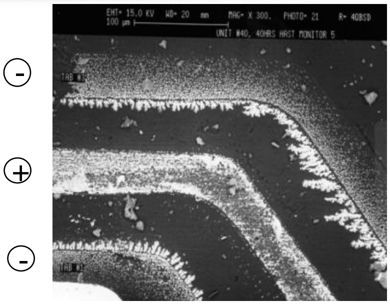
THB and Biased HAST Test

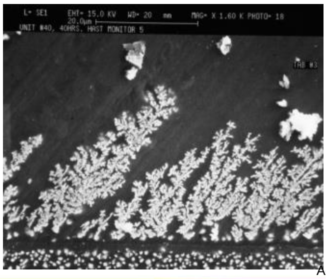
- **THB (temp & humidity biased)**
  - Elevated temp (85 °C) + moisture (85 %RH) + voltage/current
- **Biased HAST (Highly Accelerated Stress Test)**
  - High temp (130 °C) + moisture (85% RH) + voltage/current

- **Corrosion by electrochemical migration**
  - Moisture absorption/condensation
  - Voltage
  - Contamination



Dendritic Growth

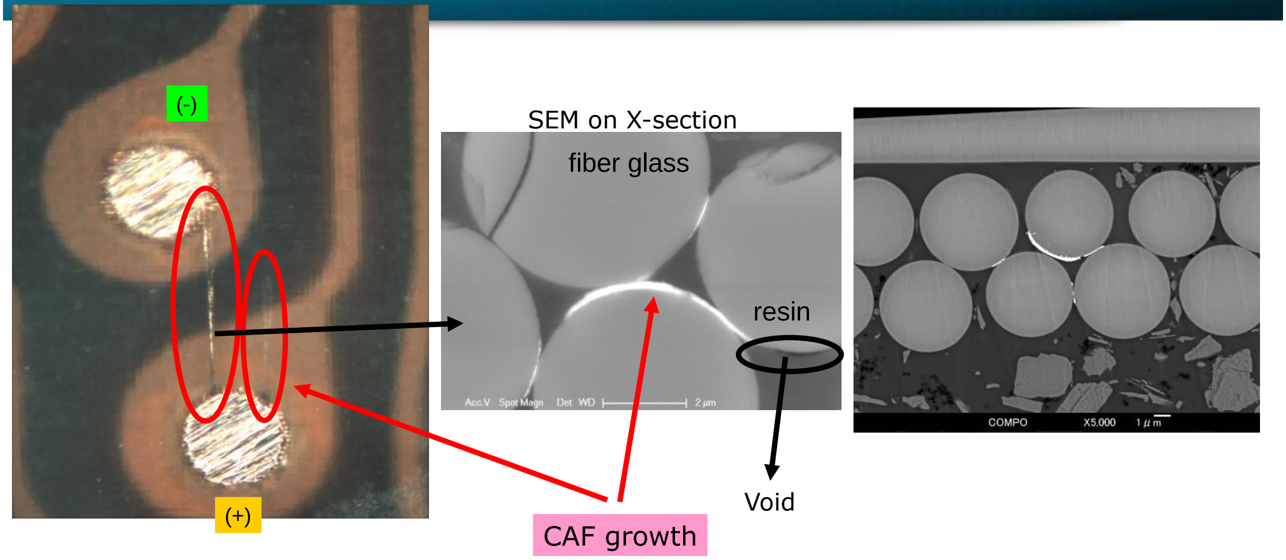




- Dendritic growth on surface - electrolytic dissolution of metal at anode followed by the reduction and deposition of metal ion at cathode.

Ack: from various sources

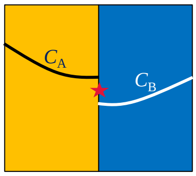
Conductive Anodic Filament (CAF) Failure



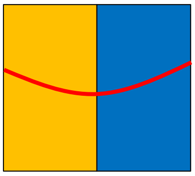
- Below surface, conductive anodic filament (CAF) growth initiates at anode and proceeds along separated fiber/epoxy interface.

Ack: from various sources

Moisture Diffusion Modeling



concentration discontinuity



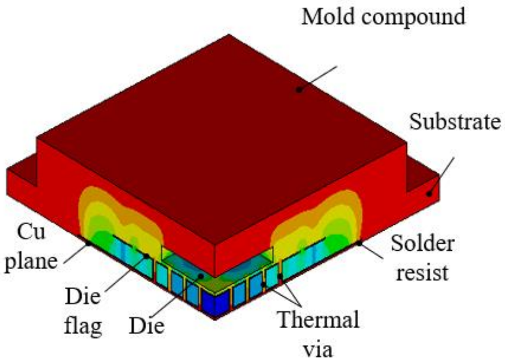
After normalization

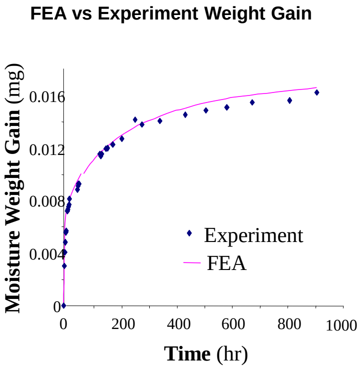
- Moisture concentration is discontinuous at multi-material interfaces.
- Such a discontinuity makes the problem unconventional in standard finite element modeling.
- A common practice is to adopt a continuous field variable through normalization.

Ma L, Joshi R, Newman K, Fan XJ. Improved Finite Element Modeling of Moisture Diffusion Considering Discontinuity at Material Interfaces in Electronic Packages. 2019 IEEE 69th Electronic Components and Technology Conference (ECTC). May 28 – 31, 2019, Las Vegas, 2019.

Moisture Diffusion Modeling: Validation

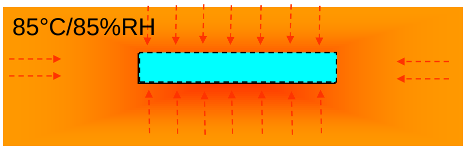
FEA moisture distribution (quarter model) after 168 hrs at 85^0C/85%RH for PBGA





- **35mmx35mm PBGA**

Coefficient of Swelling β



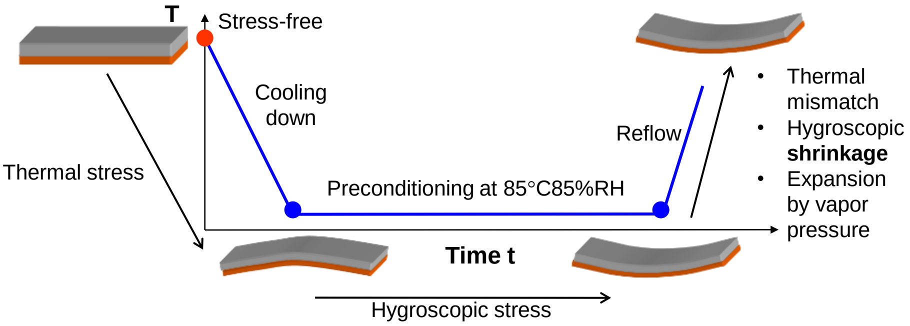
- Materials swell as moisture content changes.
- Hygroscopic swelling strain ε^{hygro} changes linearly with moisture concentration change ΔC

$$\varepsilon^{hygro}=\beta*(C-C_0) \qquad \varepsilon^{thermal}=\alpha*\Delta T$$

- β the coefficient of hygroscopic swelling.
- Unlike CTE (α), the coefficient of hygroscopic swelling is not available for most materials.

Fan XJ, Suhir, E. (eds.). *Moisture Sensitivity of Plastic Packages of IC Devices*. Springer, New York, 2010.

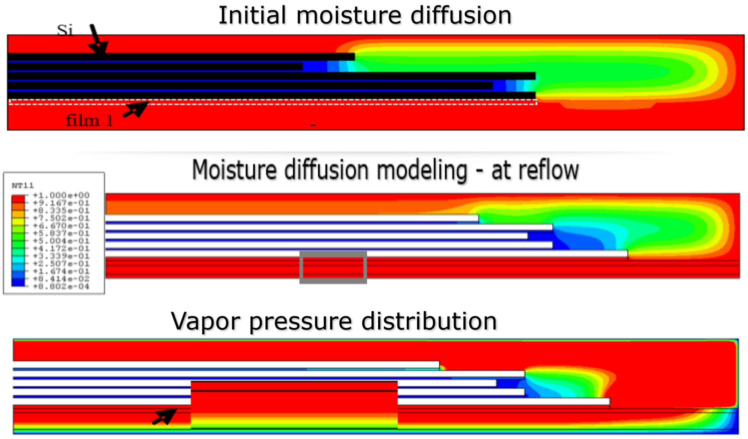
Integrated Stress Modeling



- We have developed an integrated stress modeling methodology considering thermal stress, vapor pressure, and swelling-induced stress.

Chen L, Fan XJ, Liu Y. A Direct Multi-Field Coupling Methodology for Modeling Moisture-Induced Stresses and Delamination in Electronic Packages. 2020 IEEE 70th Electronic Components and Technology Conference (ECTC).

Integrated Moisture Diffusion and Stress Modeling


Initial moisture diffusion

Moisture diffusion modeling - at reflow

Vapor pressure distribution

- Integrated moisture diffusion, stress, and vapor pressure modeling were performed for a stacked die CSP package.

Acceleration Models for HAST or THB Test

- **Empirical models**
  - Peck model

$$AF = f(V)\cdot\left(\frac{RH_{stress}}{RH_{use}}\right)^{n}\cdot\exp\left[\frac{E_{act}}{k_B}\left(\frac{1}{T_{use}}-\frac{1}{T_{stress}}\right)\right]$$

  - E_{act} Activation energy; failure mechanism dependent
  - T_{stress} Temperature during stress test
  - T_{use} Temperature during use
  - RH_{stress} Relative humidity during stress test
  - RH_{use} Relative humidity during use
  - k_B Boltzmann’s constant = 8.62 x 10-5 eV/K
  - n Peck exponent; failure mechanism dependent

Acceleration Models for HAST or THB Test

- **Empirical models**
  - Intel’s Peck model

$$AF = e^{-c\left(RH_{use\,env} - RH_{stress}\right)} \exp\left[\frac{Q}{k}\left(\frac{1}{T_{use\,env}} - \frac{1}{T_{stress}}\right)\right]$$

– Q	Activation energy; failure mechanism dependent
– T_{stress}	Temperature during stress test
– T_{use}	Temperature during use
– RH_{stress}	Relative humidity during stress test
– RH_{use}	Relative humidity during use
– k_B	Boltzmann’s constant = 8.62 x 10-5 eV/K
– c	Intel’s exponent; failure mechanism dependent

Summary

- **Moisture in IC packages will cause**
  - degradation in material strength/modulus, change in glass transition temperature, and reduction interfacial adhesion of polymer materials, especially at higher temperatures;
  - swelling and induce additional stresses;
  - moisture vaporization and induce vapor pressure, leading to popcorn cracking/delamination at reflow; and
  - electrochemical migration/corrosion.
- **Moisture diffusion and integrated stress modeling methodology have been developed.**
- **Interfacial adhesion in the presence of moisture at elevated temperatures and swelling properties are key moisture-related material properties.**

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End of Module 4

Thank you for your attention.

Questions?

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Reliability Physics and Failure Mechanisms in Electronics Packaging

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Department of Mechanical Engineering

1

Module 5

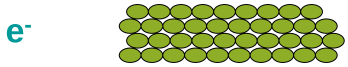
- Module 1: Introduction
- Module 2: Thermal Stress-induced Failures
- Module 3: Failure Analysis under Drop Test
- Module 4: Moisture-induced Reliability Issues
- **Module 5: Electromigration**

2

Acknowledgment

- **A team at Delft University of Technology**
    - Dr. Zhen Cui
    - Ms. Yaqian Zhang
    - Dr. Sten Vollebregt
    - Dr. Jiajie Fan
    - Dr. G.Q. Zhang
- **Dr. Kasemsak Kijkanjanapaiboon, Lamar University**

What is Electromigration (EM)?

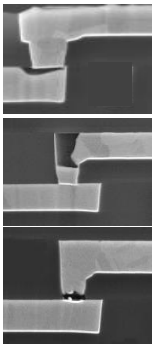


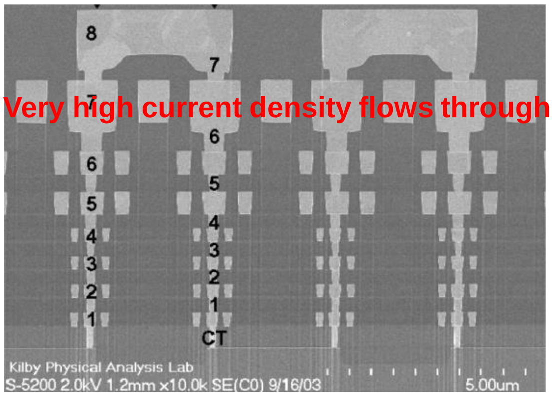
- Electromigration is a process of mass transport in the current-carrying metal under the driving forces generated by electric field.

K.N. Tu: EPTC 2008 short course

What Happens during EM?

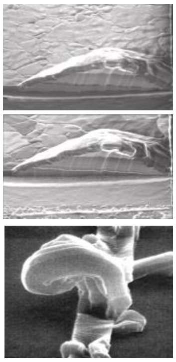
Void





Very high current density flows through

Hillock

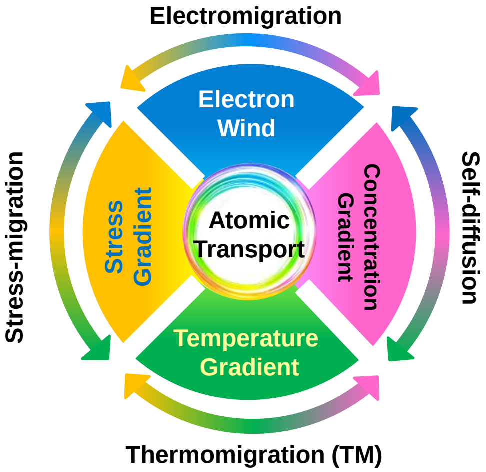


- Electromigration is one of the most persistent reliability problems in interconnect technology in semiconductor devices.

K.N. Tu: EPTC 2008 short course

Similar to River Flow…

EM – a Coupled Multi-Physics Problem

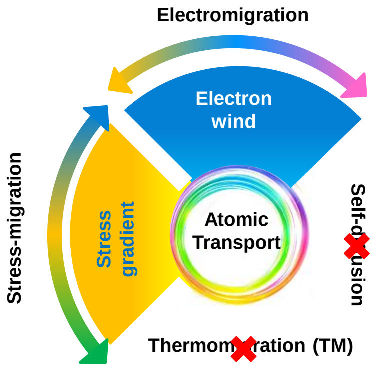


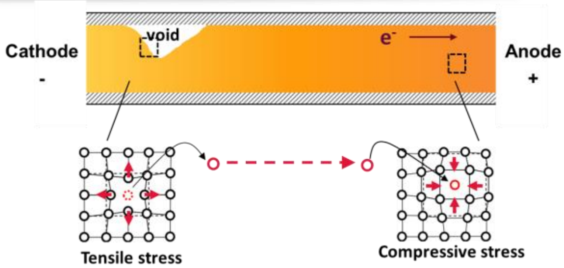
$$\boldsymbol{J}_a = -D_a \nabla C_a - D_a C_a \frac{Z^* e\rho \boldsymbol{j}}{k_B T} + D_a C_a \frac{\Omega \nabla \sigma}{k_B T} - D_a C_a \frac{Q^* \nabla T}{k_B T^2}$$

D_a : Atomic diffusivity
C_a: Atomic concentration (m^{-3})
Ω: Volume of per atom (m^3)
$\boldsymbol{j}$: current density (A/m^2)
k_B : Boltzmann's constant (J/K)
T: Temperature
e: elementary charge (C)
Z* : effective charge number(>0)
Q* : heat of transport (kJ/mol)
f : volume relaxation ratio

- EM is a multi-physics coupled field problem involved with electron wind, chemical potential, stress gradient and temperature gradient.

Blech's Theory (1976)





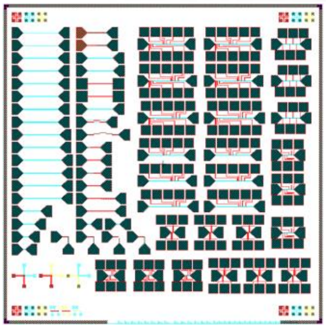
$$Z^* e\rho j + \Omega \frac{\partial \sigma}{\partial x} = 0$$

$$\boxed{jL = \frac{(\sigma_{max} - \sigma_{min})\Omega}{Z^* e\rho}}$$

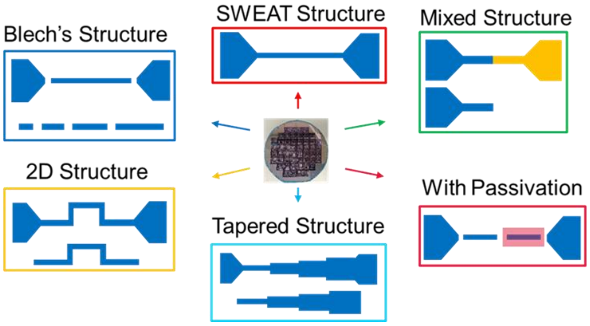
- EM flux is entirely balanced by the stress-induced counter flux.
- Blech Product, *jL*, provides a threshold condition of *maximum stress or stress gradient*, below which, electromigration failure will not occur - mechanical failure.

I. Blech and C. Herring, APL, 29, 131, 1976.

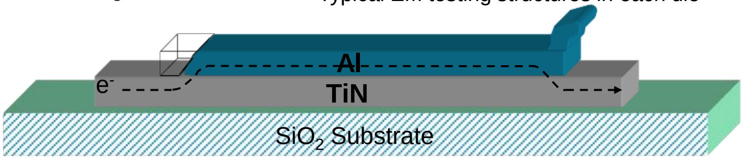
EM Testing Wafer & Die



Top view of mask design



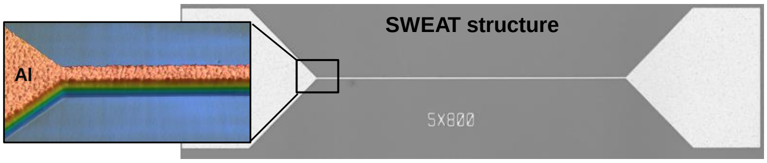
Typical EM testing structures in each die



Stacked-layer on wafer

Zhen Cui, PhD Dissertation Multi-Physics Driven Electromigration Study: Multi-Scale Modeling and Experiment, Delft University of Technology 2021.

Blech vs. SWEAT Test Structure



- **Blech structure** refers to a metal line non-contacted with pads, which has blocking conditions on both ends.
- **SWEAT** (standard wafer-level electromigration acceleration test) structure refers to a metal line connected with pads, which maintains constant atomic concentration at both ends.

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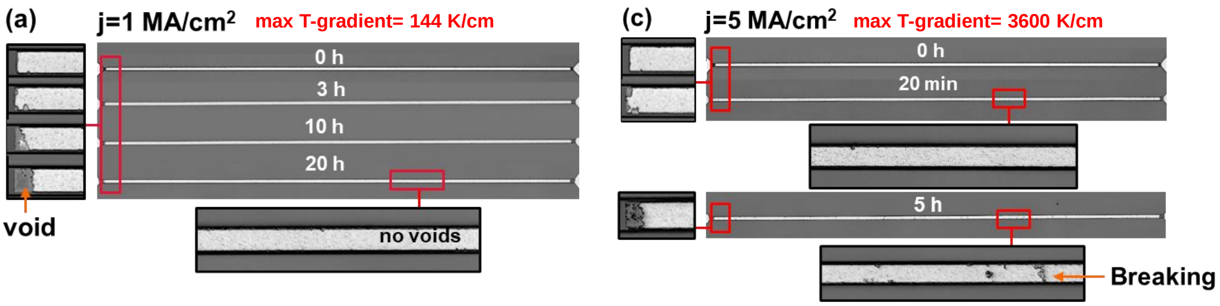
Experimental Results: Blech Structure

Aluminum line: 800 µm × 0.2 µm × 5 µm



- Void/hillock formations were observed first at the both ends in **an early stage**.
- However, with increasing current density, voids began to spread in the conductor.
- The void formation/spreading in the middle region of conductor lagged those at both the ends.
- Thermomigration is believed to be the primary cause for void formation in the middle region.

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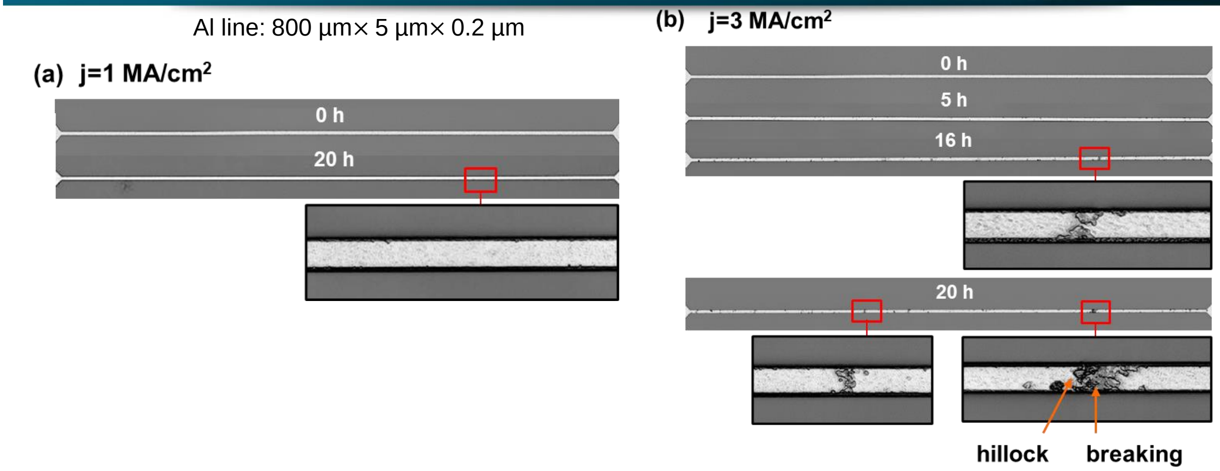
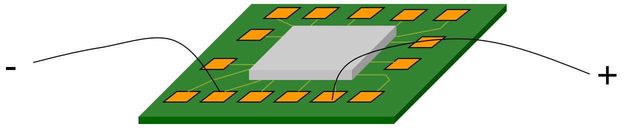
Experimental Results: SWEAT Structure

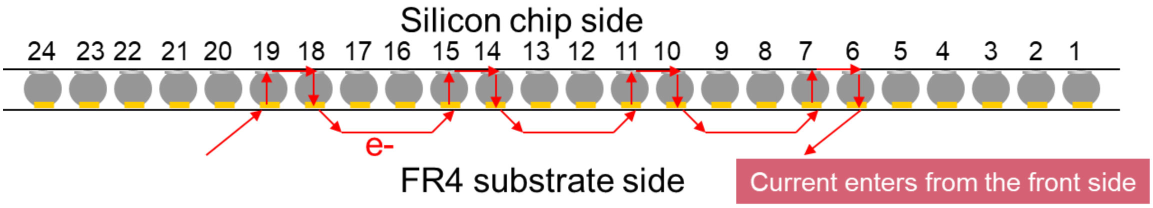
Al line: 800 µm× 5 µm× 0.2 µm



- No void/hillock formations at both ends in the SWEAT structure, regardless of current density and duration of test.
- With j = 1 MA/cm², no obvious voids were observed after 20 h.
- However, with j = 3 MA/cm², voids in the conductor were observed after 5 h.
- The metal line broke at 20 h, slightly off the center toward to the right, with j = 3 MA/cm²

EM and TM in Solder Joints

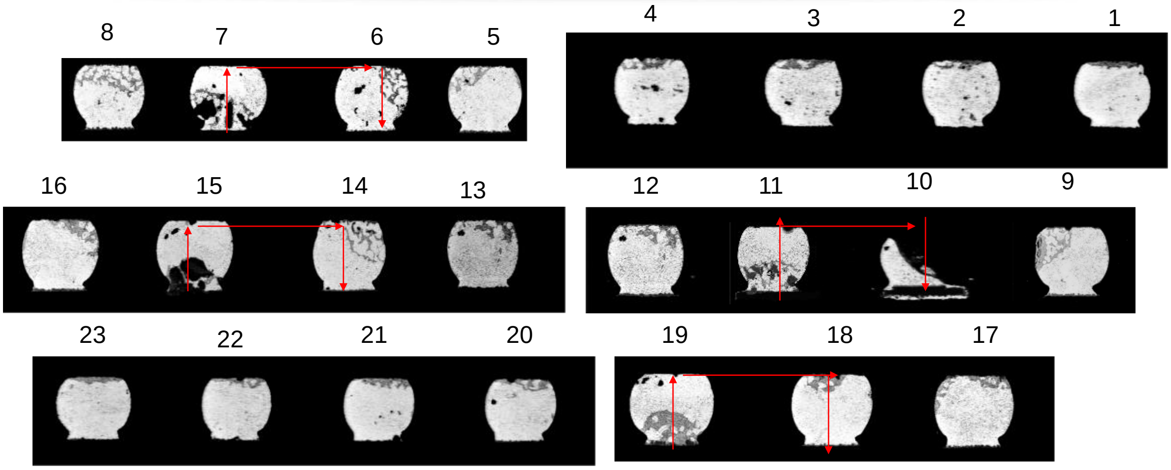




- Four pairs bump bumps are current stressed of 1A($1.57x10^4$A/cm^2) at 150^{o}C until failure.

Ack: K.N. Tu, EPTC PDC 2007

Test Results in Solder Joints



- The pairs of 6/7, 10/11, 14/15, 18/19 were stressd by current. The rest were not stressed, but thermomigration has occurred.

Ack: K.N. Tu, EPTC PDC 2007

Fully-Coupled Model of Electromigration

Mass conservation equation:

$$\frac{\partial\theta}{\partial t} = -\Omega\,\nabla\cdot\boldsymbol{J}_a$$

$$\boldsymbol{J}_a = -D_a\nabla C_a - D_aC_a\frac{Z^*e\rho\boldsymbol{j}}{k_BT} + D_aC_a\frac{\Omega\nabla\sigma}{k_BT} - D_aC_a\frac{Q^*\nabla T}{k_BT^2}$$

Constitutive equation:

$$\theta = \mathrm{tr}(\boldsymbol{\varepsilon}), \qquad \boldsymbol{\varepsilon} = \boldsymbol{\varepsilon}^{me} + \boldsymbol{\varepsilon}^{th} + \boldsymbol{\varepsilon}^{diff},$$

$$\boldsymbol{\varepsilon}^{th} = \alpha dT\mathbf{I}, \qquad d\boldsymbol{\varepsilon}^{diff} = \frac{1-f(C_a)}{3}\frac{dC_a}{C_a}\mathbf{I},$$

$$\boldsymbol{\sigma} = 2G\boldsymbol{\varepsilon} + \lambda\mathrm{tr}(\boldsymbol{\varepsilon})\mathbf{I} - B\mathrm{tr}\left(\boldsymbol{\varepsilon}^{th}\right)\mathbf{I} - B\mathrm{tr}(\boldsymbol{\varepsilon}^{diff})\mathbf{I}$$

$$\sigma = \mathrm{tr}(\boldsymbol{\sigma})/3$$

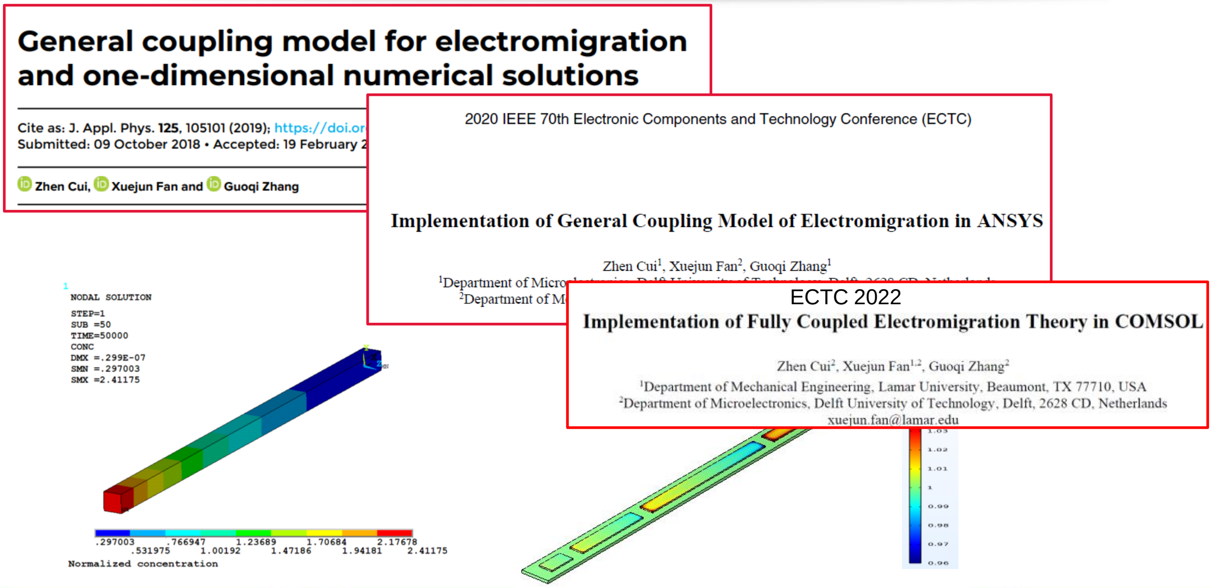
Field equations:

$$\nabla\cdot\boldsymbol{\sigma} + \boldsymbol{F} = 0, \qquad \boldsymbol{\varepsilon} = \frac{1}{2}(\nabla\boldsymbol{u} + \boldsymbol{u}\nabla)$$

$$\nabla\cdot\boldsymbol{j} = 0, \qquad \boldsymbol{j} = \frac{\boldsymbol{E}}{\rho} = -\frac{\nabla V}{\rho}$$

$$k\nabla^2T + \boldsymbol{j}\cdot\boldsymbol{E} = 0$$

Implementation in ANSYS and COMSOL



General coupling model for electromigration and one-dimensional numerical solutions

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Zhen Cui, Xuejun Fan and Guoqi Zhang

2020 IEEE 70th Electronic Components and Technology Conference (ECTC)

Implementation of General Coupling Model of Electromigration in ANSYS

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ECTC 2022

Implementation of Fully Coupled Electromigration Theory in COMSOL

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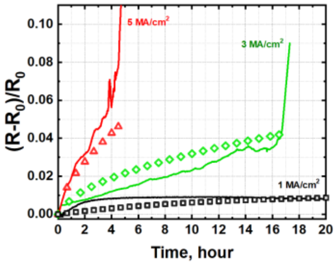
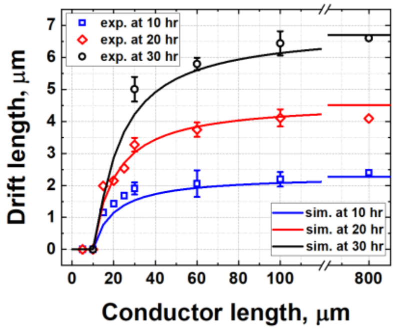
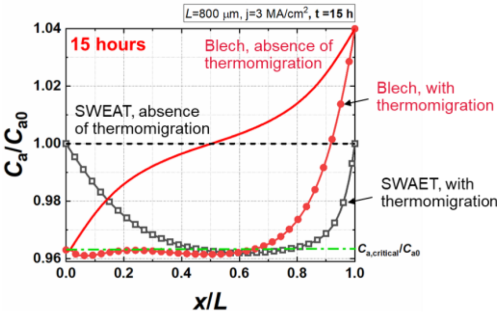
Simulation Results







- The simulation results agreed well with in-situ resistance measurement during EM.
- The predicted void growth has excellent agreement with the measurement.
- For both Blech and SWEAT test structures, the simulation results are consistent with the experimental observations for the effect of TM.

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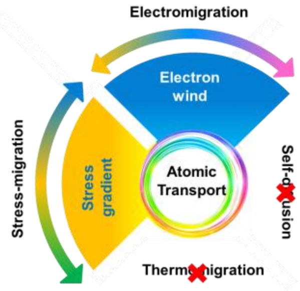
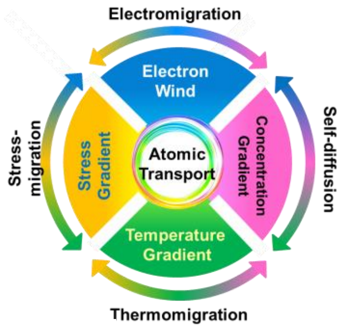
Revisit – Extension of Blech's Theory



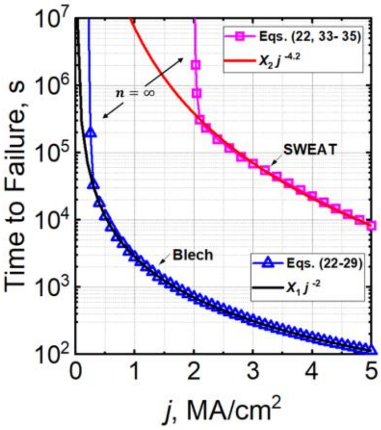


$$\begin{cases} jL = (jL)_c = C & , \quad \text{Blech} \\ jL^2 = (jL^2)_c = C' & , \quad \text{SWEAT} \end{cases}$$

- For Blech structures, the threshold condition was still the same as in the original Blech's theory but different constant.
- For the SWEAT structure, however, we found the threshold condition in the form of the product of the current density and the square of critical length (jL^2).

Z. Cui, et al, paper under review

Acceleration Models



$$AF = \left(\frac{j_{\text{stress}}}{j_{\text{use}}}\right)^{> 2 \to \infty}$$ when j_{use} in low range

Blech structure

$$AF = \left(\frac{j_{\text{stress}}}{j_{\text{use}}}\right)^{2}$$ when j_{use} in high range

$$AF = \left(\frac{j_{\text{stress}}}{j_{\text{use}}}\right)^{>4.2\ 2 \to \infty}$$ when j_{use} in low range

SEWAT structure

$$AF = \left(\frac{j_{\text{stress}}}{j_{\text{use}}}\right)^{4.2}$$ when j_{use} in high range

- For Blech structure, the exponent n maintained a value of 2 in the range of the current density from 0.2 to 5 MA/cm^2. The exponent then rapidly increased and approached infinity if the current density fell below the critical current density.
- For SWEAT structure, n fits a value of 4.2 in the range of the current density from 2 to 5 MA/cm^2. The exponent then rapidly increases and approaches infinity if the current density falls below the critical current density.

Z. Cui, et al, paper under review

Summary

- EM is a multi-physics coupled field problem involved with electron wind, chemical potential, stress gradient, and temperature gradient.
- We reported a new failure mode in Blech's structure: voids spreading in conductor, at a significantly delayed time after void/hillock formations at both ends.
- In SWEAT structure, despite of no-failures at both ends, we also observed voids spreading in conductor at higher current density.
- Thermomigration is believed to be the primary cause for void spreading in both Blech and SWEAT structures.
- The predicted time to failure, resistance change, and location agreed well with the experimental data.
- A fully coupled model has been implemented in ANSYS and COMSOL.
- An extension of Blech's threshold condition has been developed.
- Acceleration factors in different test structures have been determined.

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End of Module 5

Thank you for your attention.

Questions?

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