Reliability Testing And Design For Reliability of Packaging Interconnects (Solder Joints)

John H Lau
Unimicron Technology Corporation
John_lau@unimicron.com

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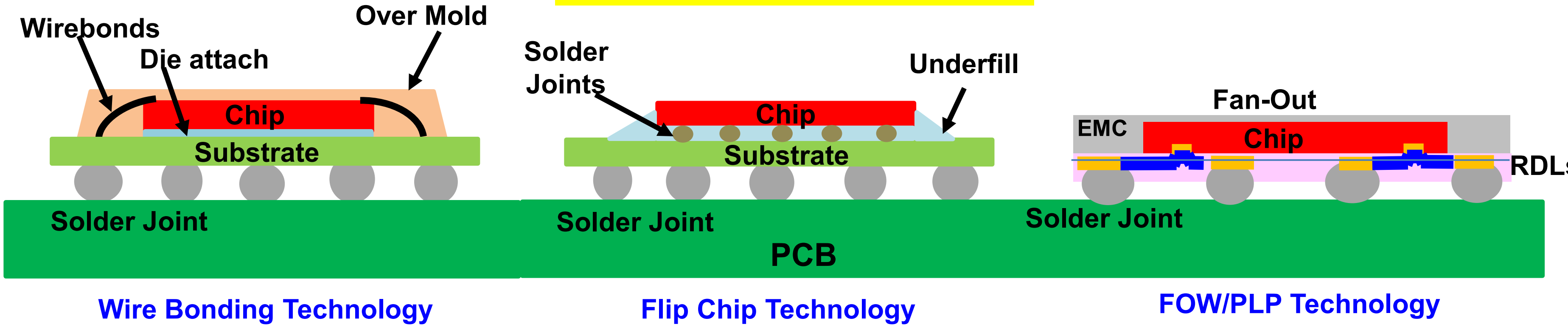
- **Solder Joints in Electronic Packaging**
- **Reliability Testing and Data Analysis of Lead-Free Solder Joints**
- **Design for Reliability of Lead-Free Solder Joints**

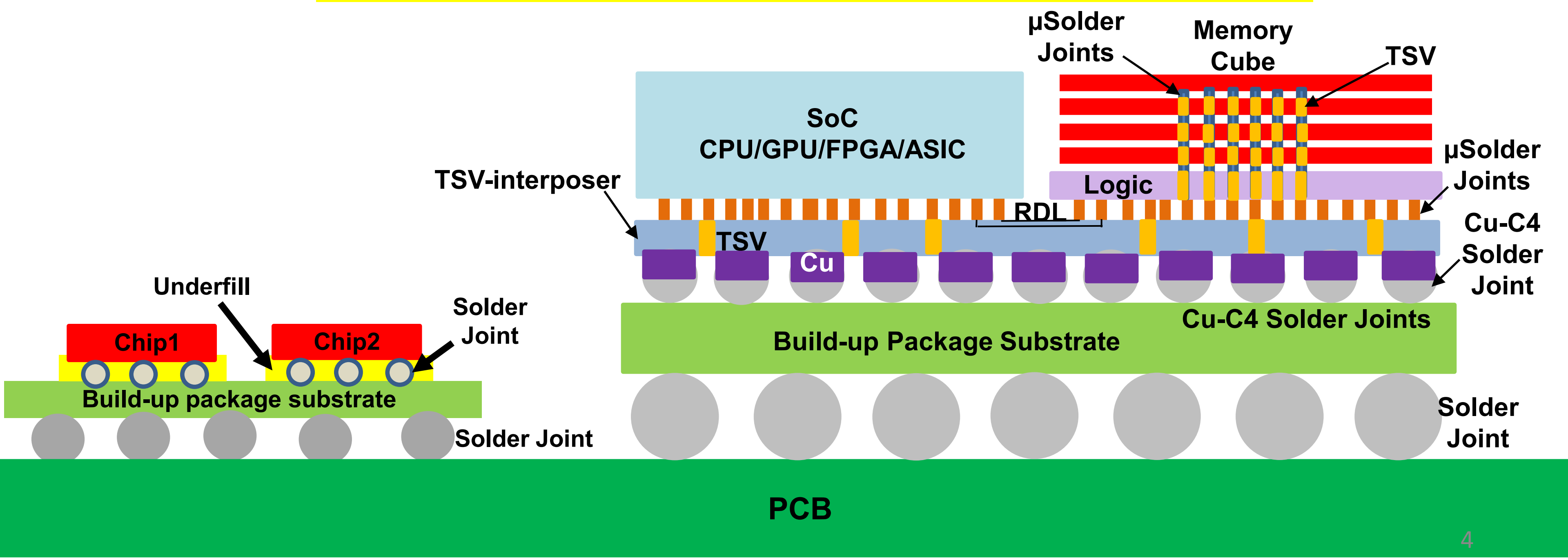
Solder Joints in Electronic Packaging

Solder Joints in Electronic Packaging

Single Chip Packaging



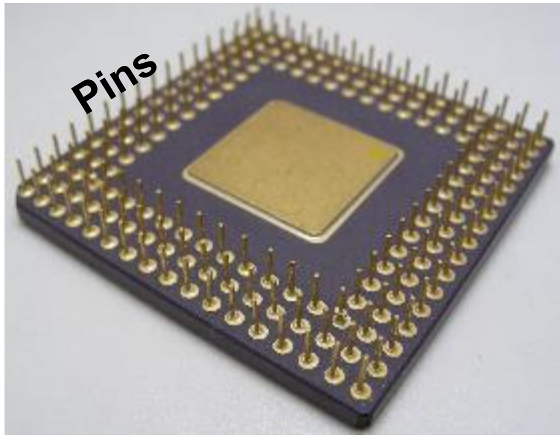
Multi-Chip (Heterogeneous Integration) Packaging



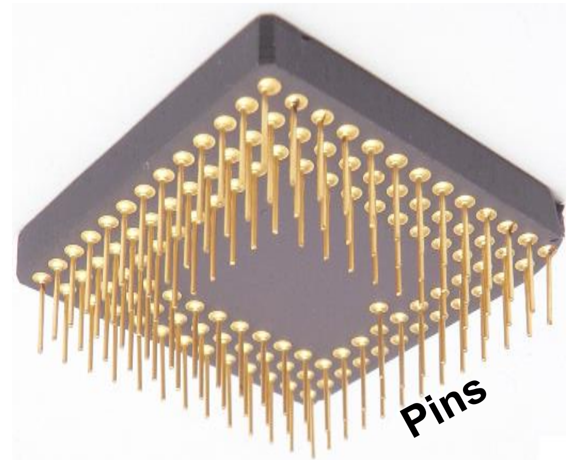
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

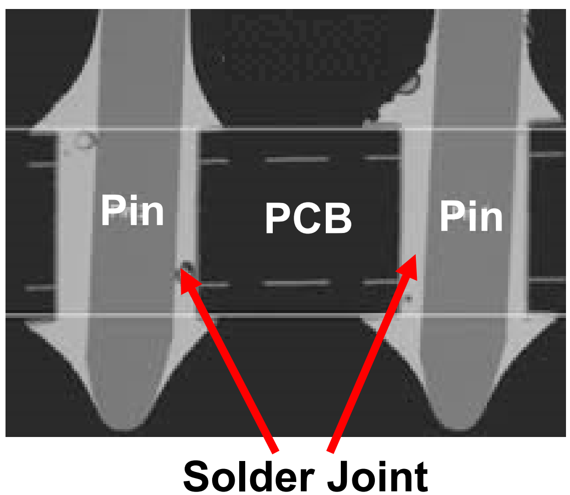
Solder Joints in PGA PCB Assembly

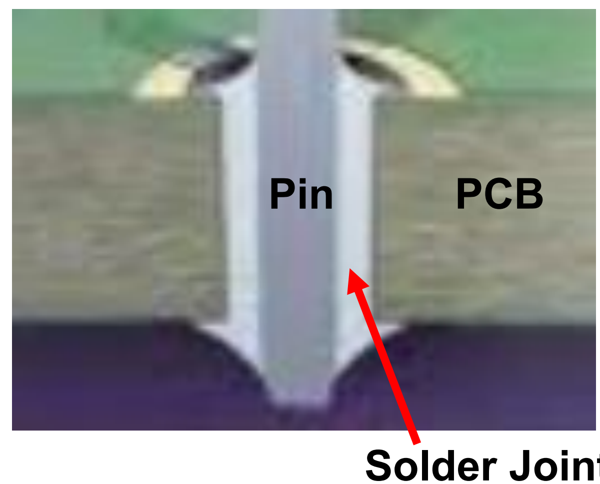
Pin-Grid Array (PGA)



Pin-Grid Array (PGA)

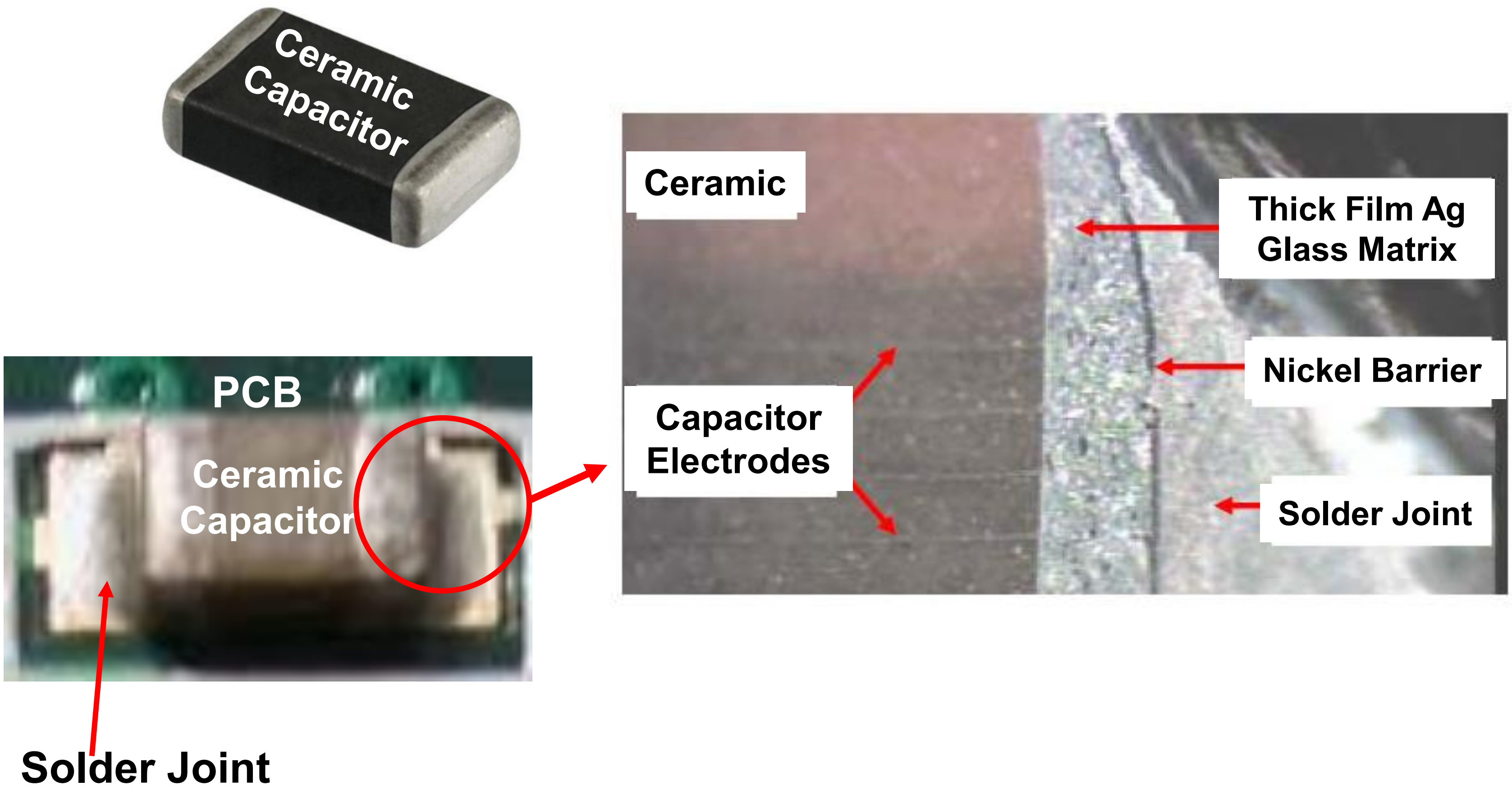






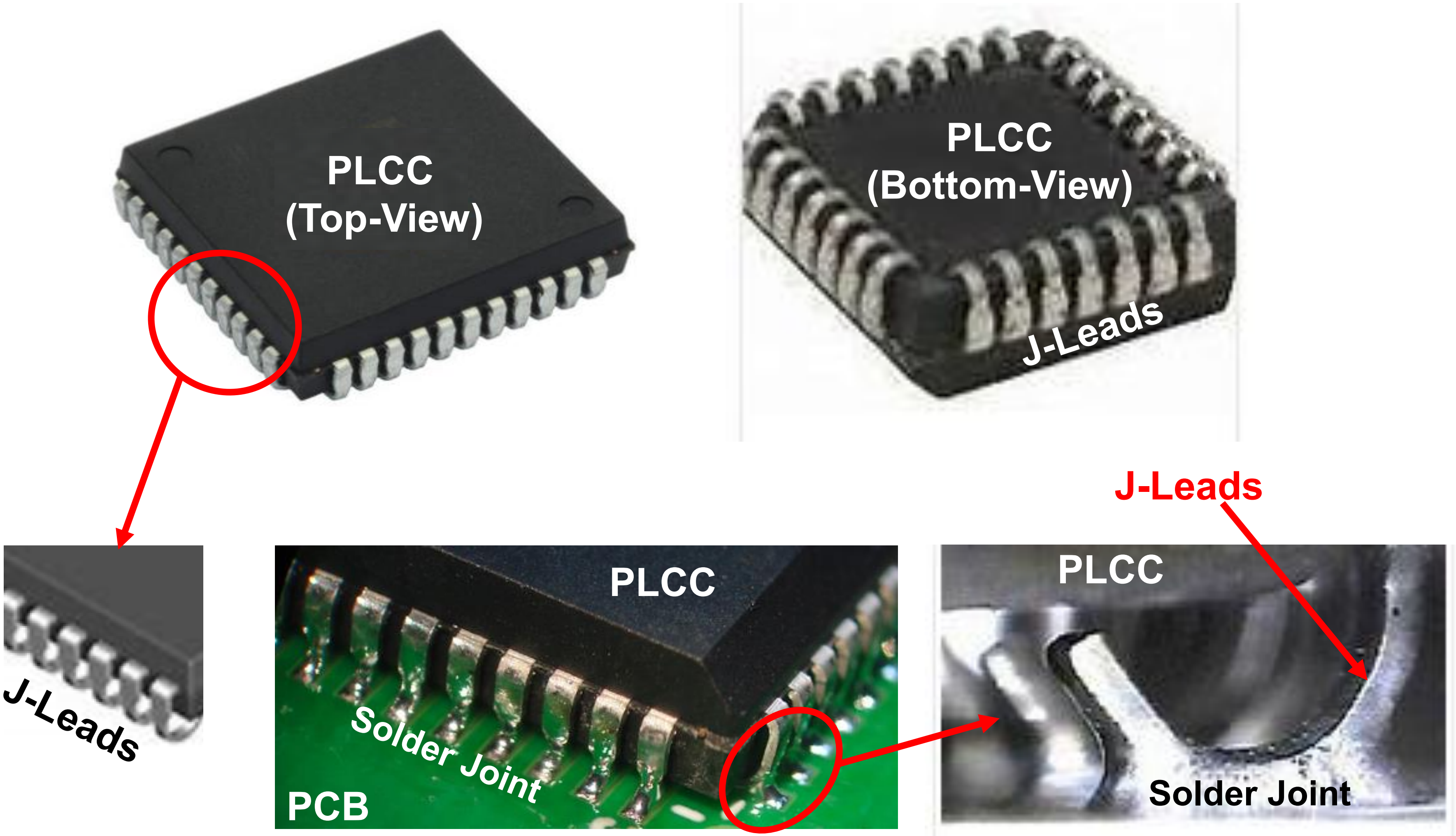
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Solder Joints in Ceramic Capacitor PCB assembly



Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

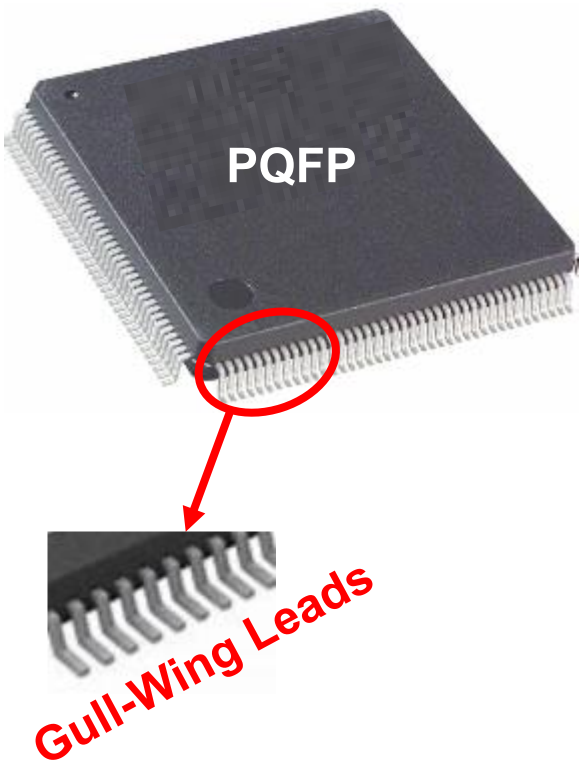
Solder Joints in PLCC PCB Assembly

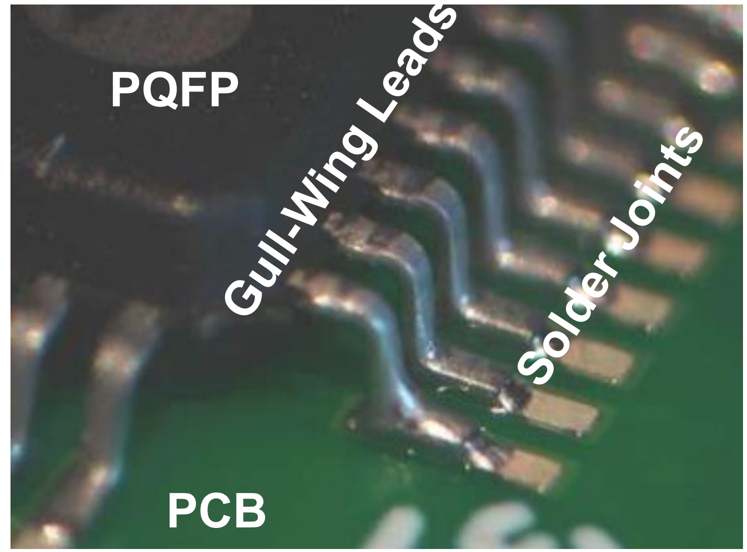


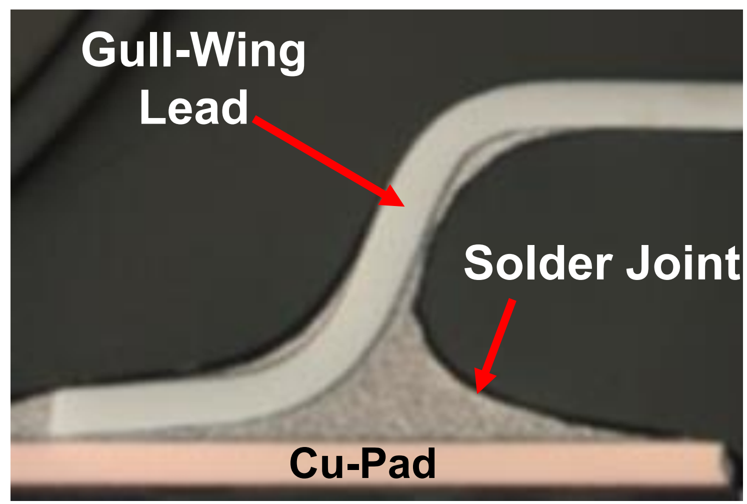
PLCC (Plastic Leaded Chip Carrier)

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Solder Joints in PQFP PCB Assembly



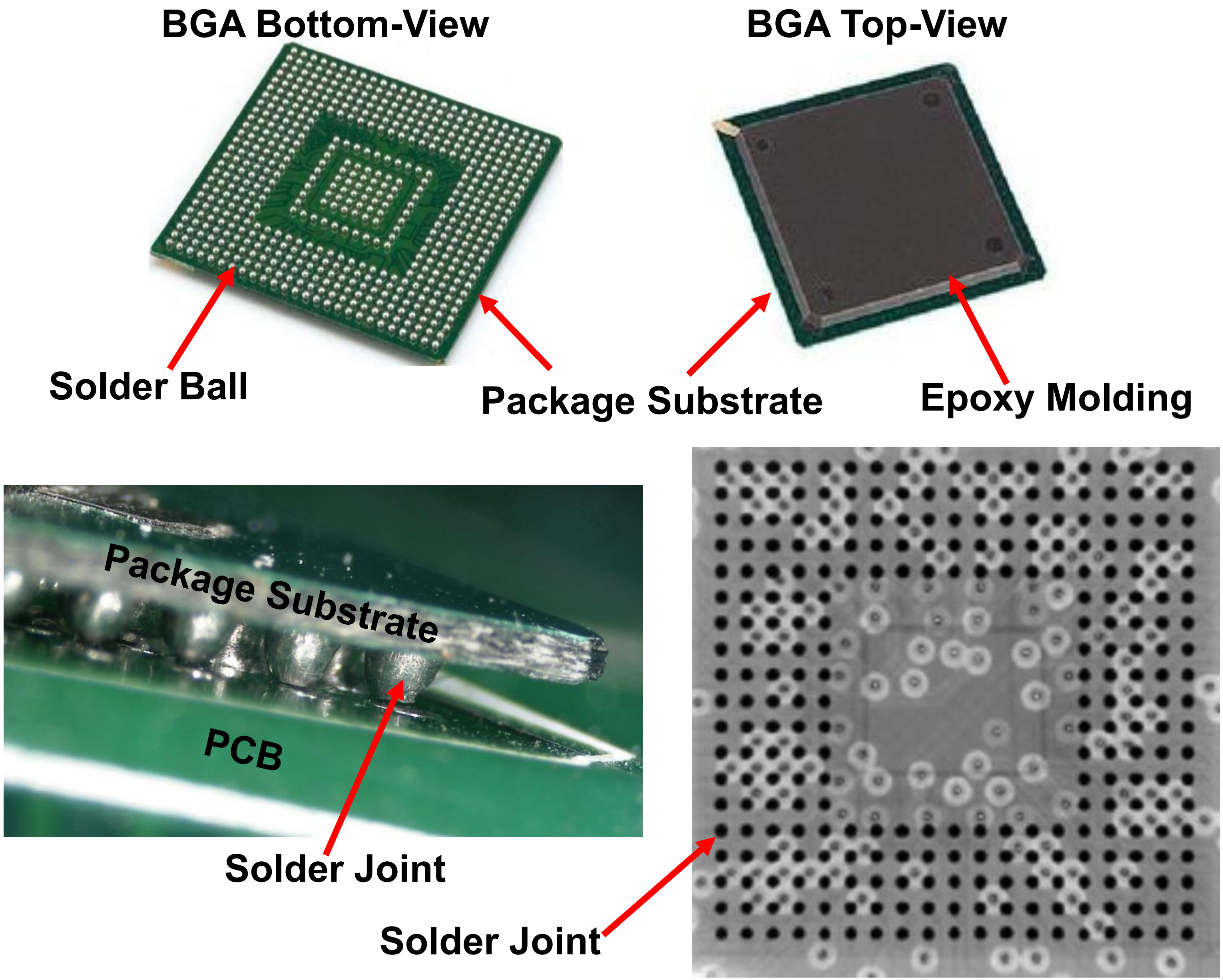




PQFP (Plastic Quad Flat Pack)

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

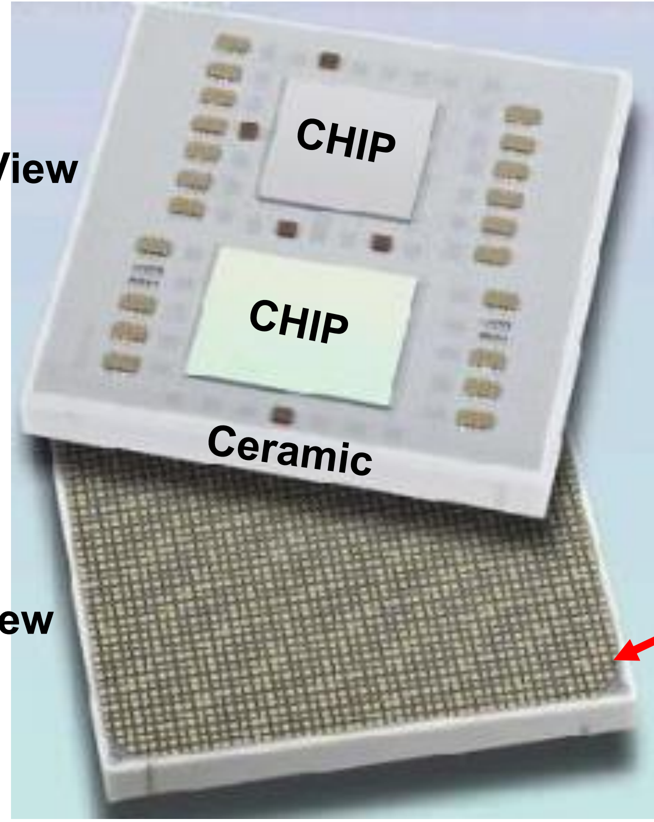
Solder Joints in PBGA PCB Assembly

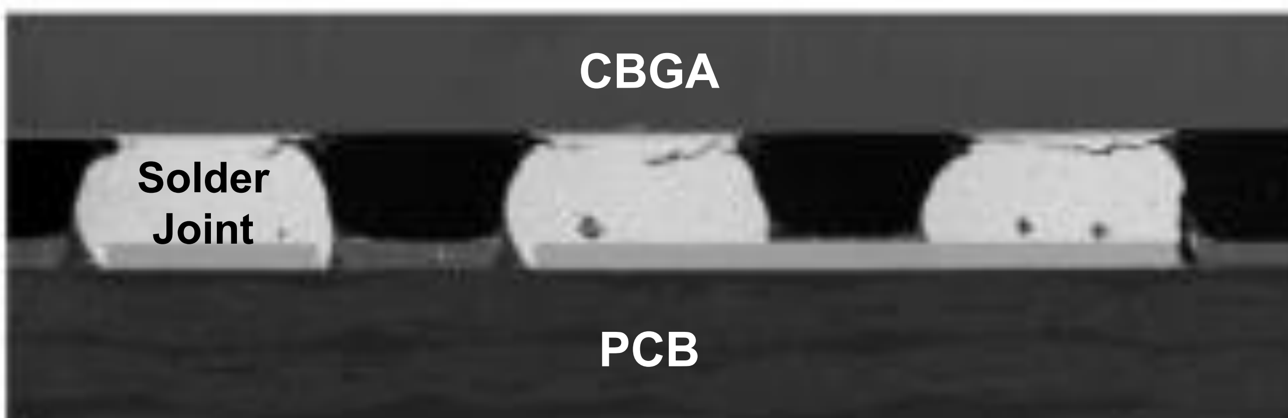


PBGA (Plastic Ball Grid Array)

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

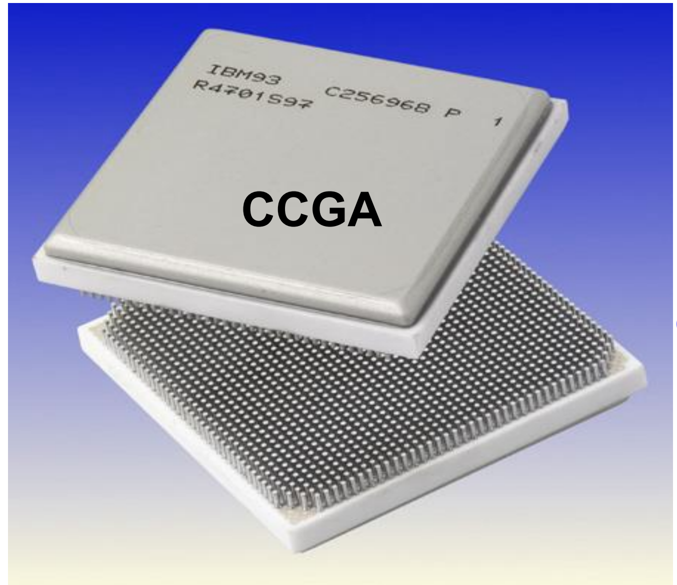
Solder Joints in CBGA PCB Assembly





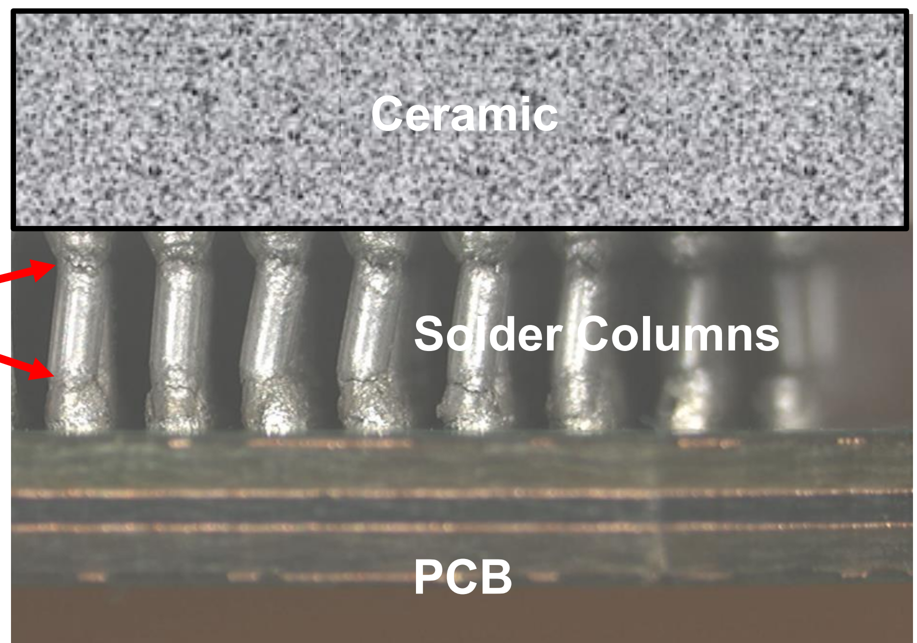
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Solder Joints in CCGA PCB Assembly



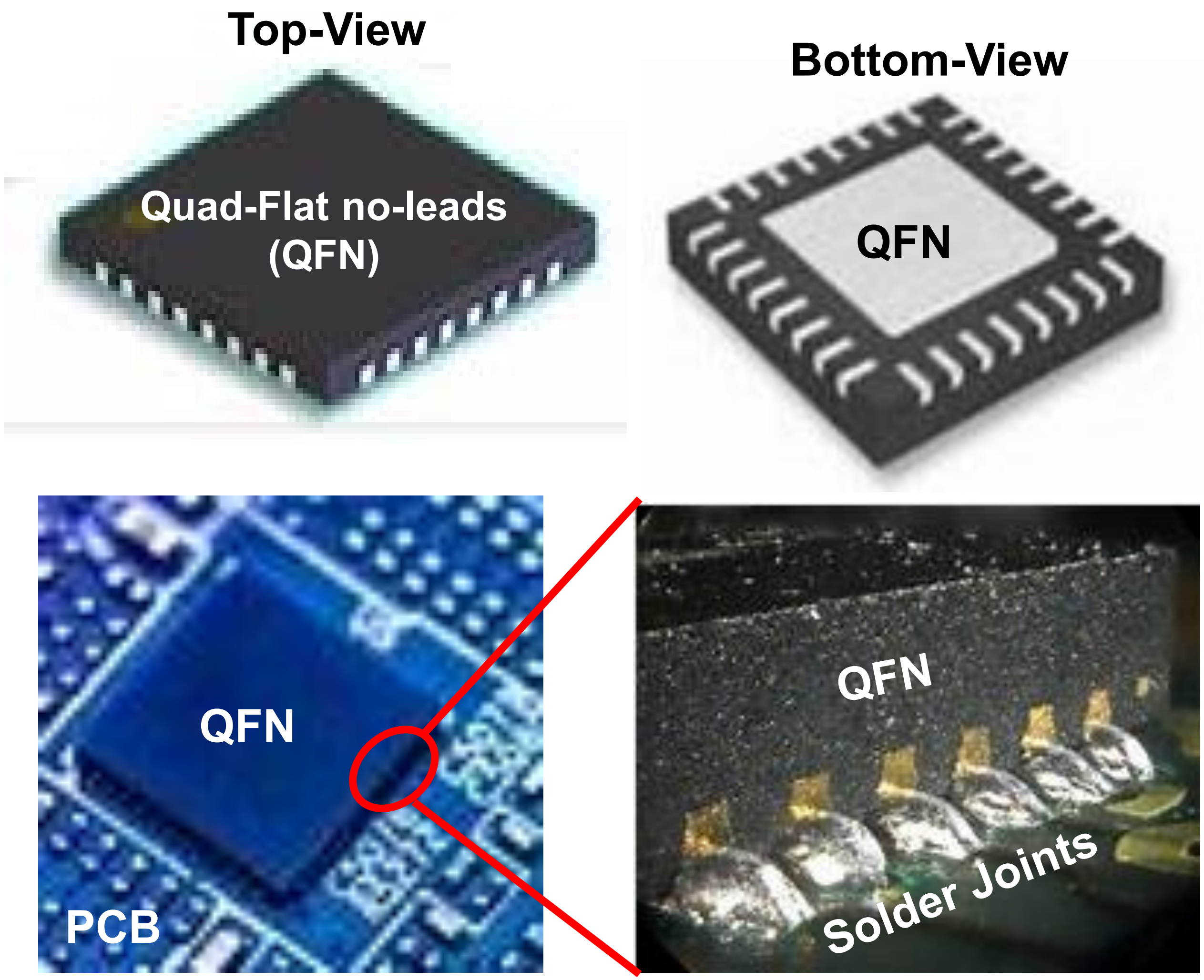
Ceramic Column Grid Array (CCGA)

Solder Joint

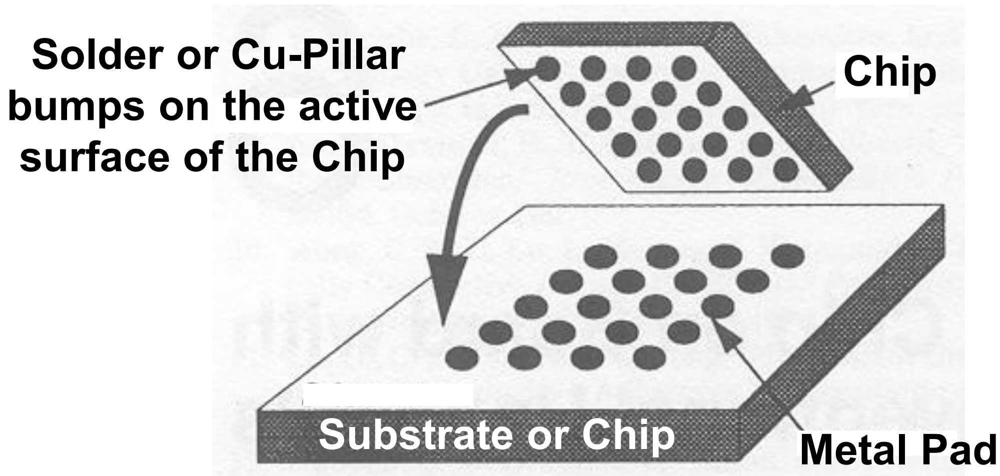


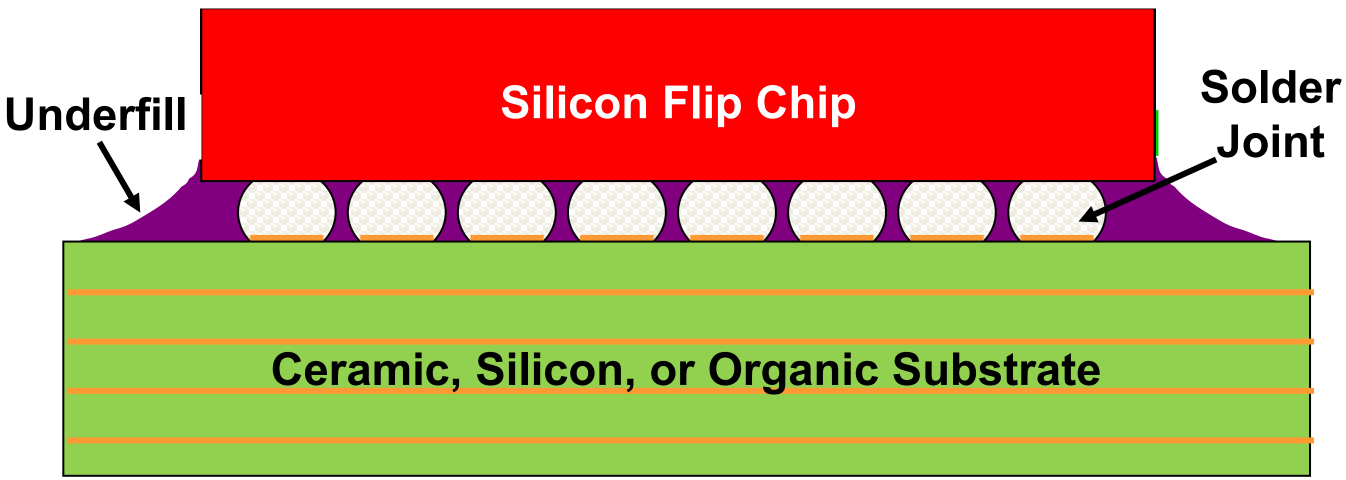
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Solder Joints in QFN PCB Assembly



Flip Chip Technology



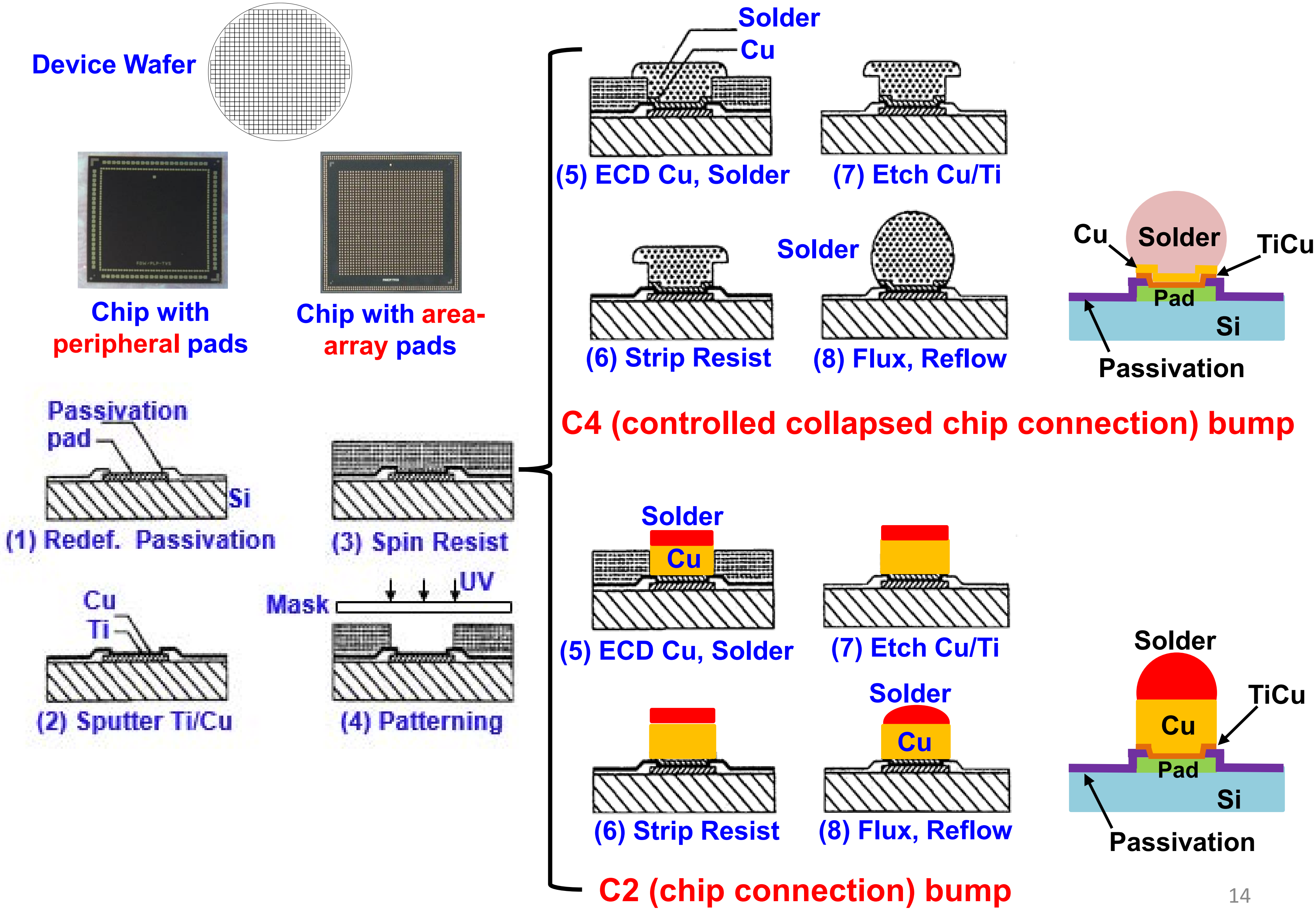


TCE of Ceramic = 5-6x10^{-6}/^{o}C; TCE of Organic = 15-18x10^{-6}/^{o}C

TCE of Silicon = 2.5x10^{-6}/^{o}C

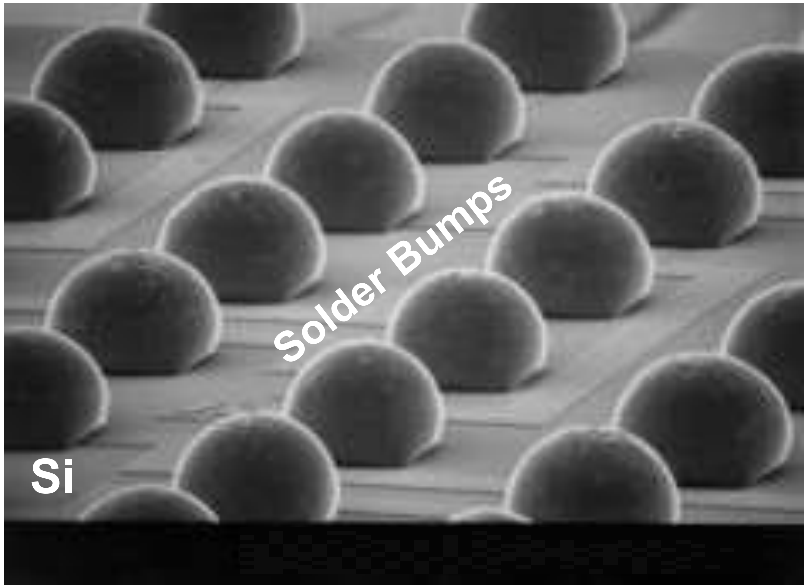
ASME Transactions, Journal of Electronic Packaging, 2021

Mother of Flip Chip Technology – Wafer Bumping

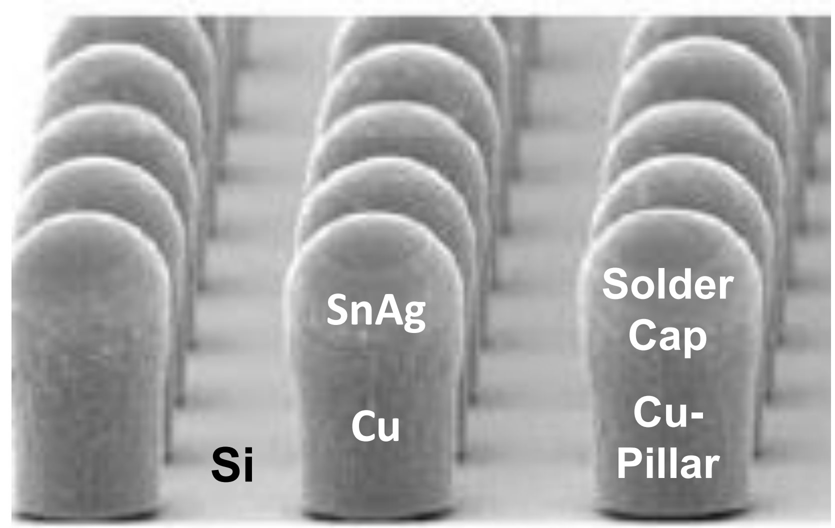


Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

C4 Bump vs. C2 Bump



C4 Bumps



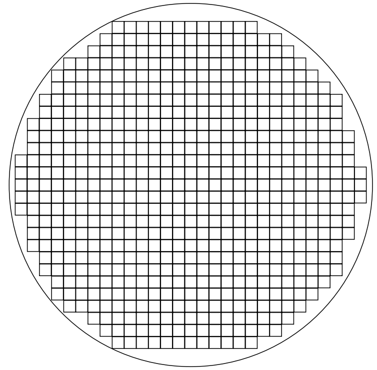
C2 Bumps (Cu Pillar with Solder Cap)
Also, called microbump (μbump)

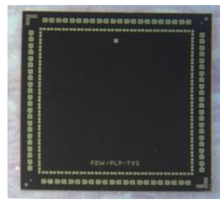
Structure	Thermal conductivity (W/m·K)	Electrical resistivity (μΩ·m)	Bump pitch	Self-alignment
Cu	400	0.0172	-	-
C4 Bump (Solder)	55 - 60	0.12 – 0.14	≥ 50μm	Very good
C2 Bump (Cu Pillar + Solder Cap)	300 (Effective)	0.025 (Effective)	< 50μm	Veery poor

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

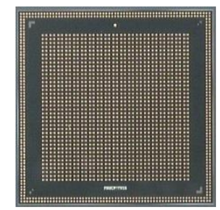
Flip Chip Technology

Wafer with Chips



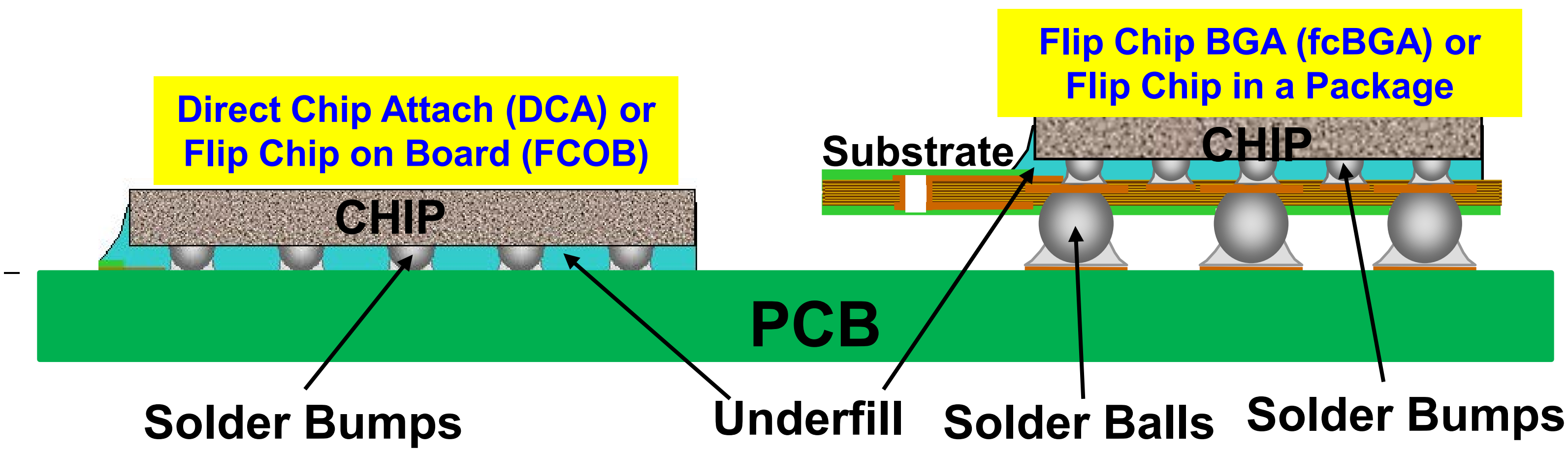


Chip with peripheral pads



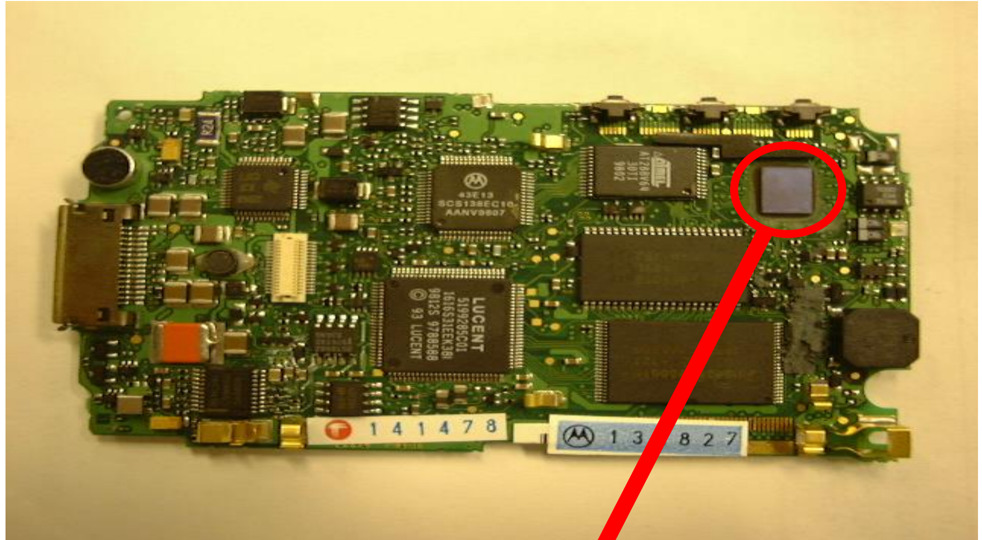
Chip with area-array pads

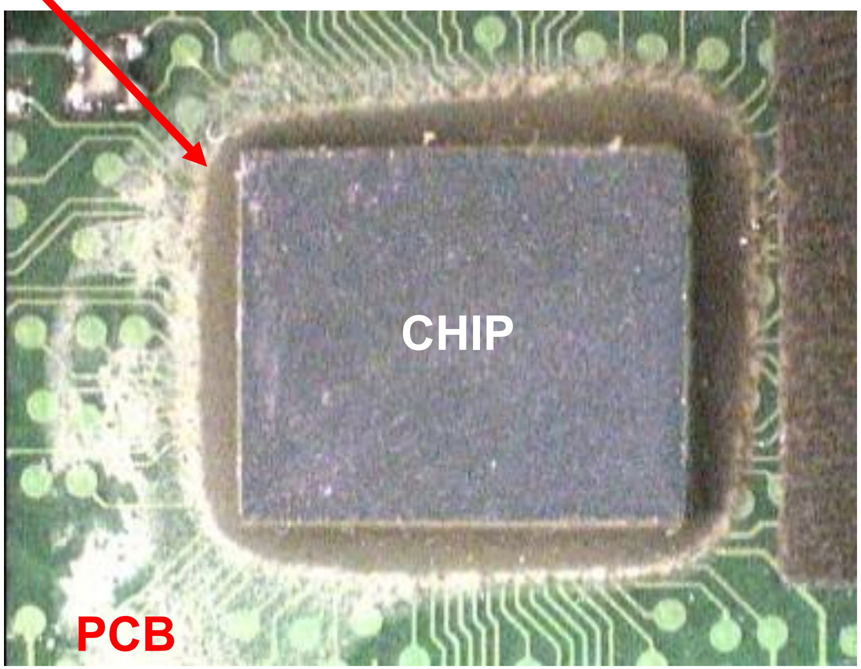
After Wafer Bumping and Dicing, then Flip Chip Assembly

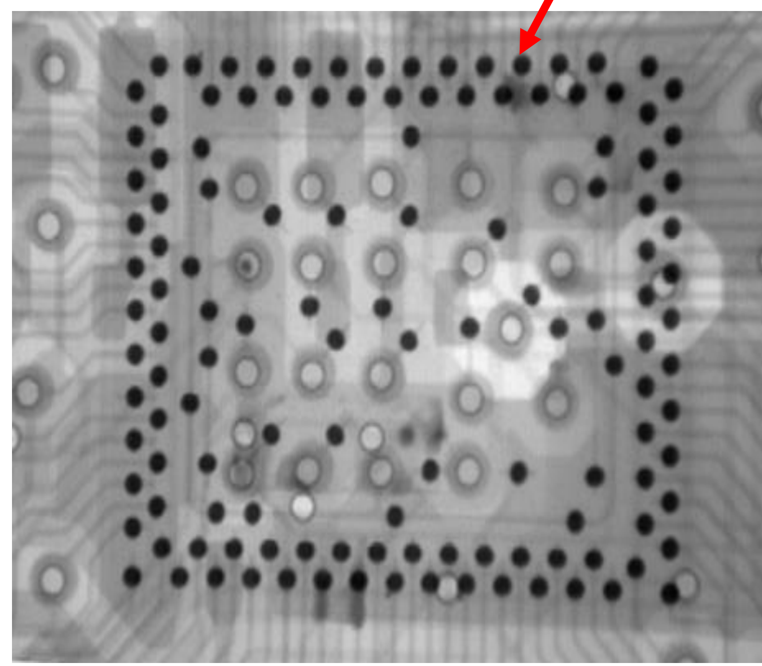


Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Direct Chip Attach (DCA)



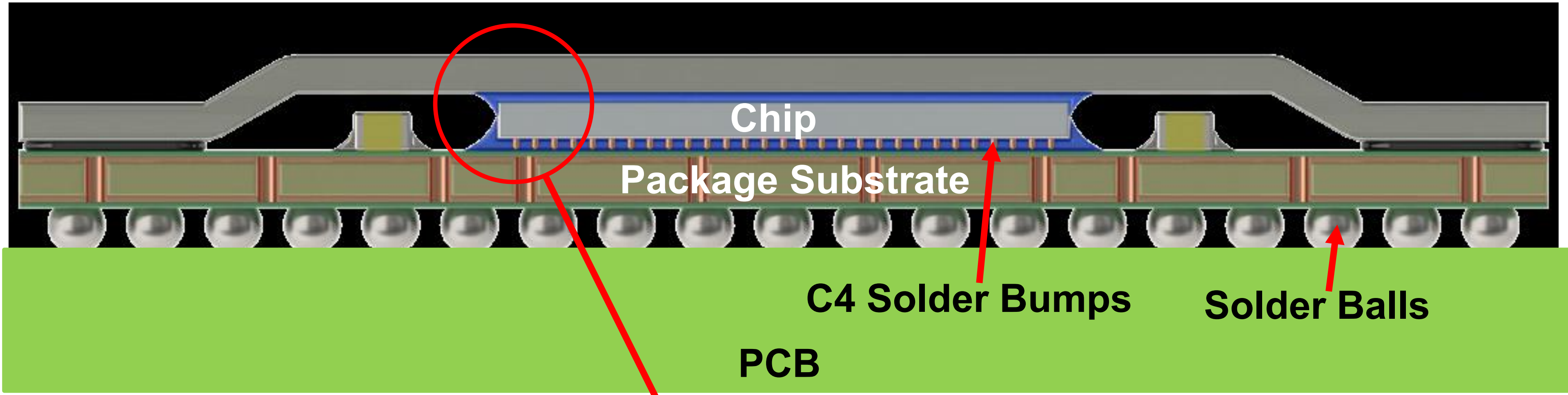


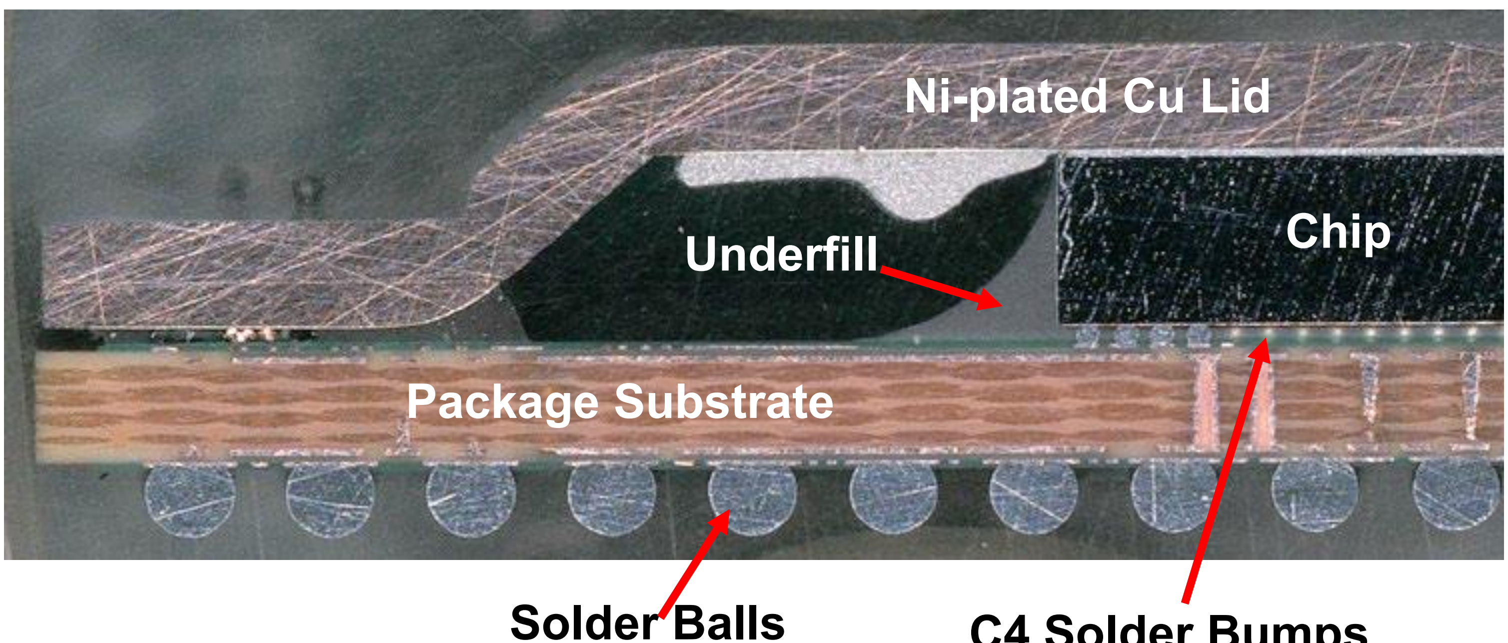


X-ray showing solder joints

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

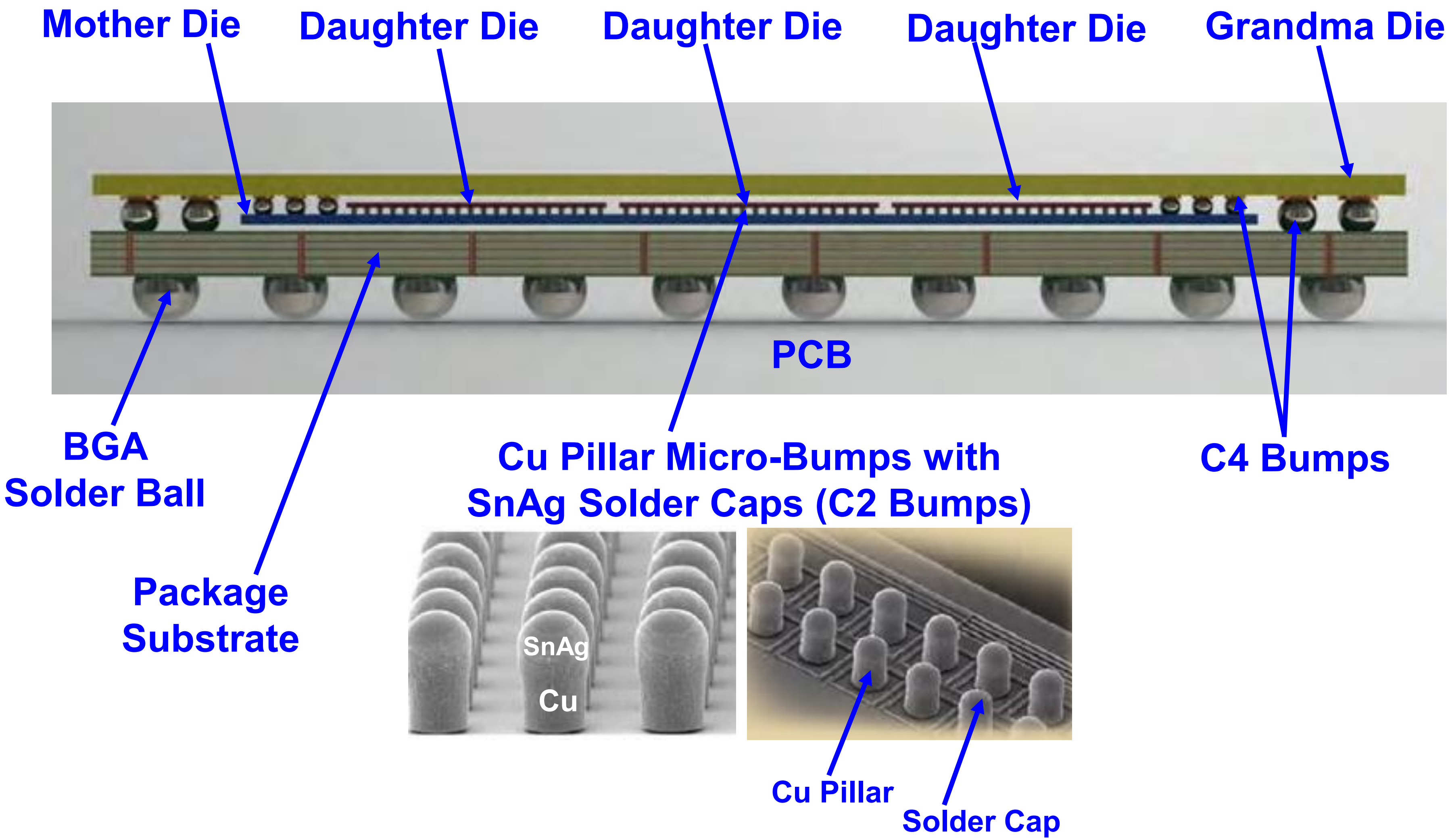
Flip Chip Ball Grid Array (fcBGA)





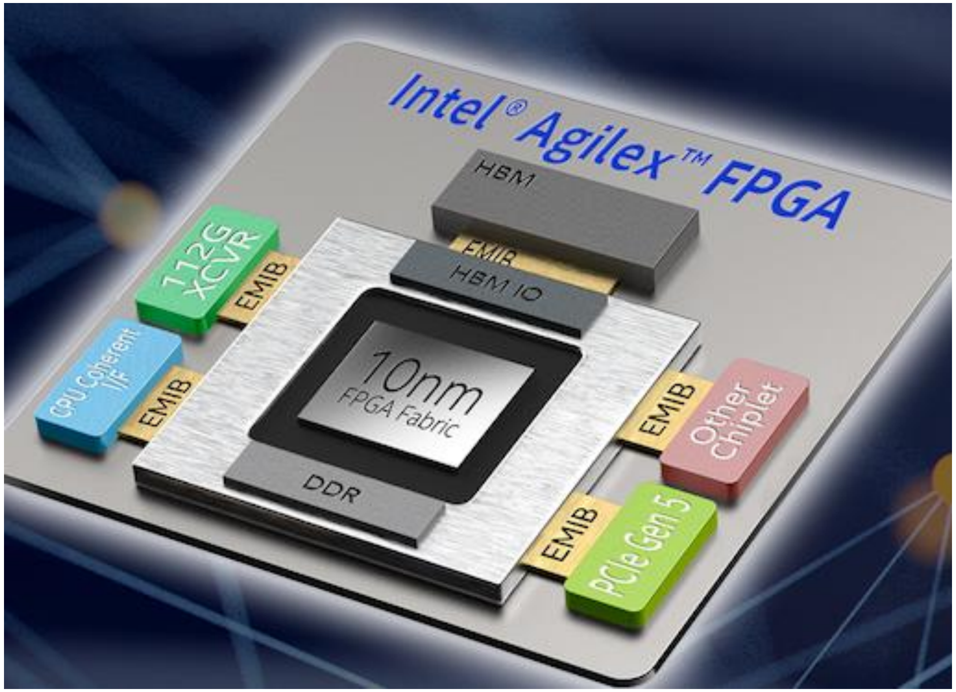
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

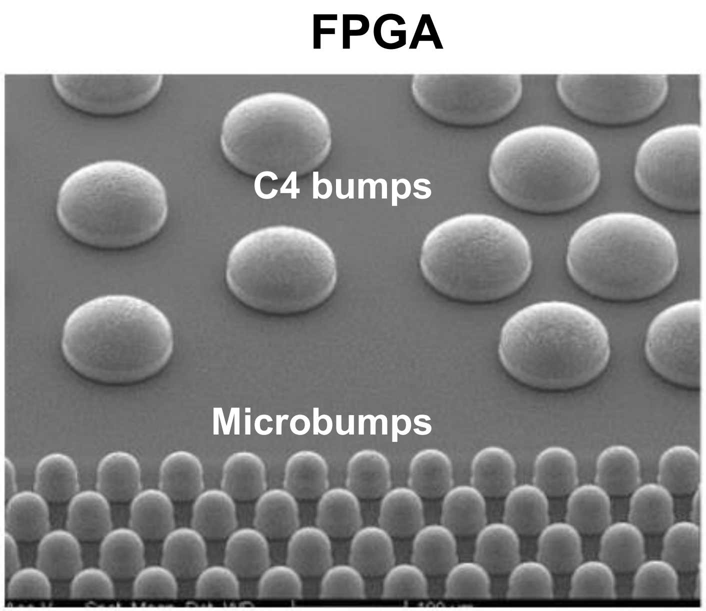
Amkor's Multiple Chip-to-Chip Interconnects (Double-POSSUM^{TM})

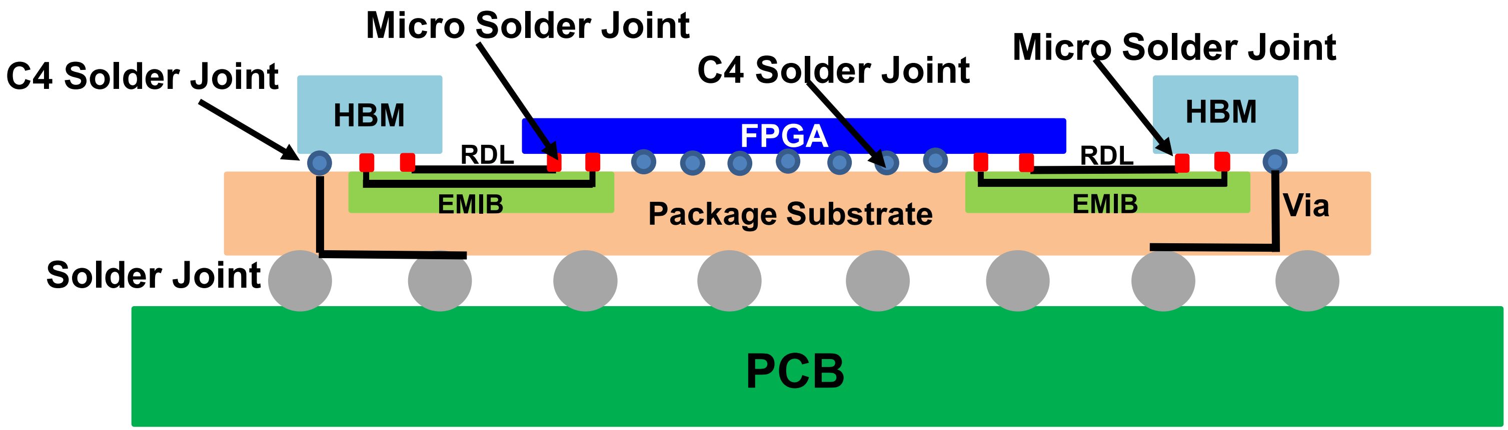


Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Intel's Agilex FPGA with EMIB





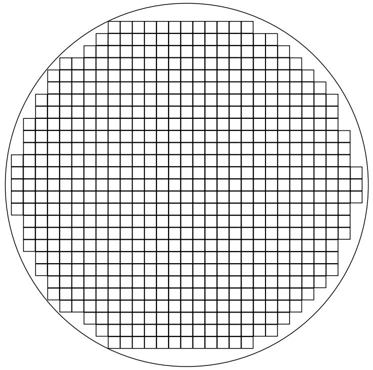


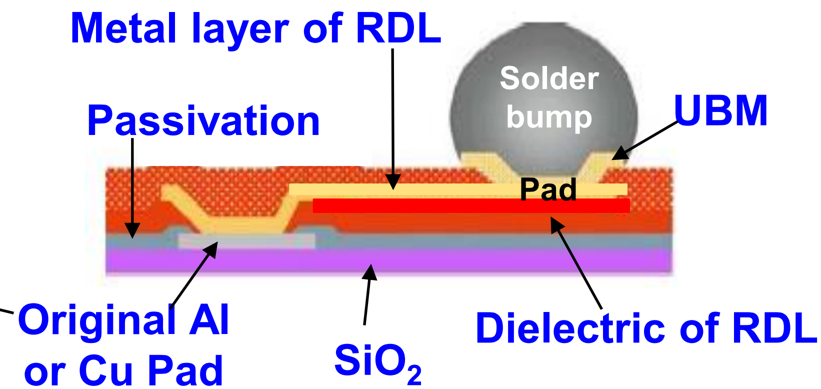
Shipped August 30, 2019

Wafer-Level Chip Scale Package (WLCSP)

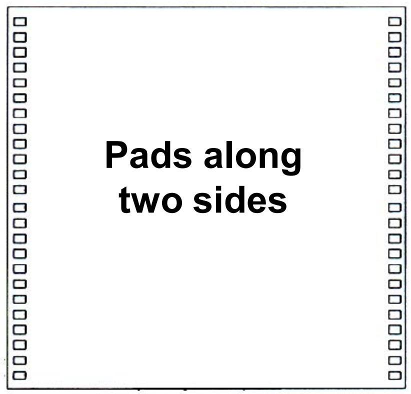
or Fan-In Wafer-Level Packaging

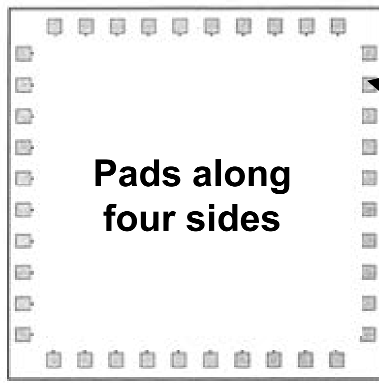
Wafer with Chips

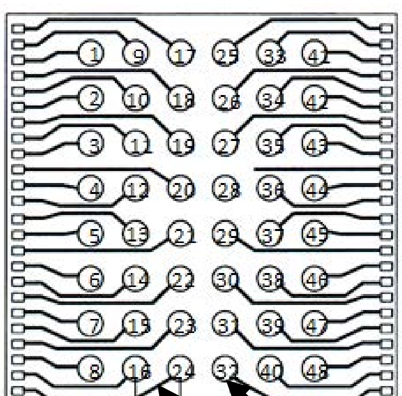


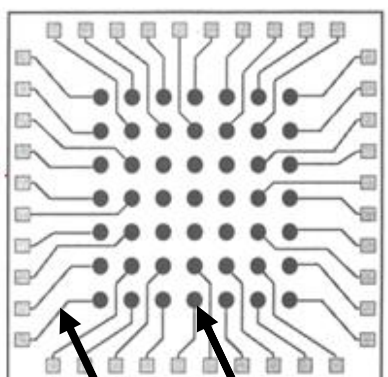


Chips with peripheral pads

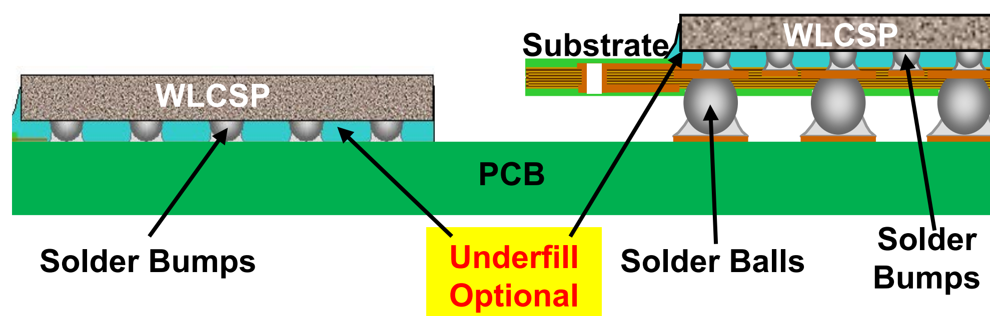






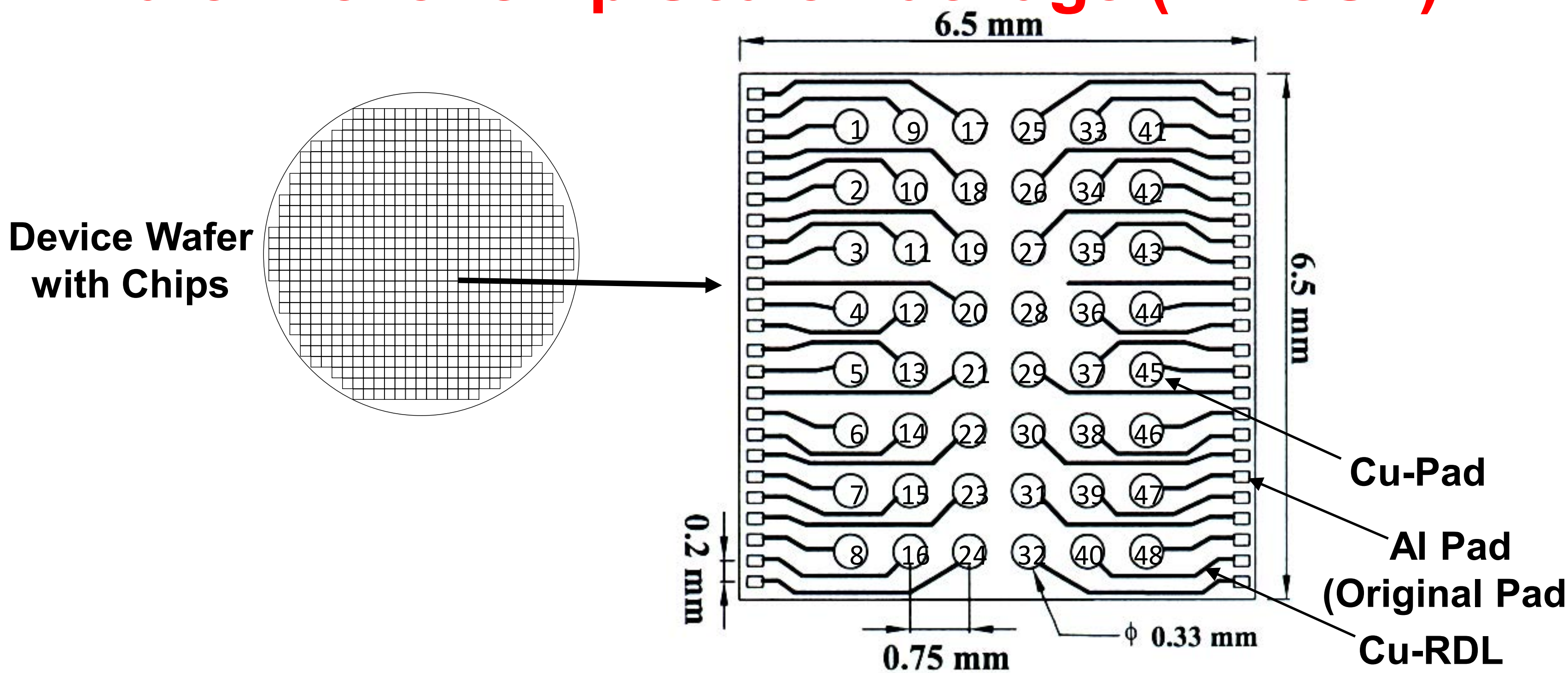


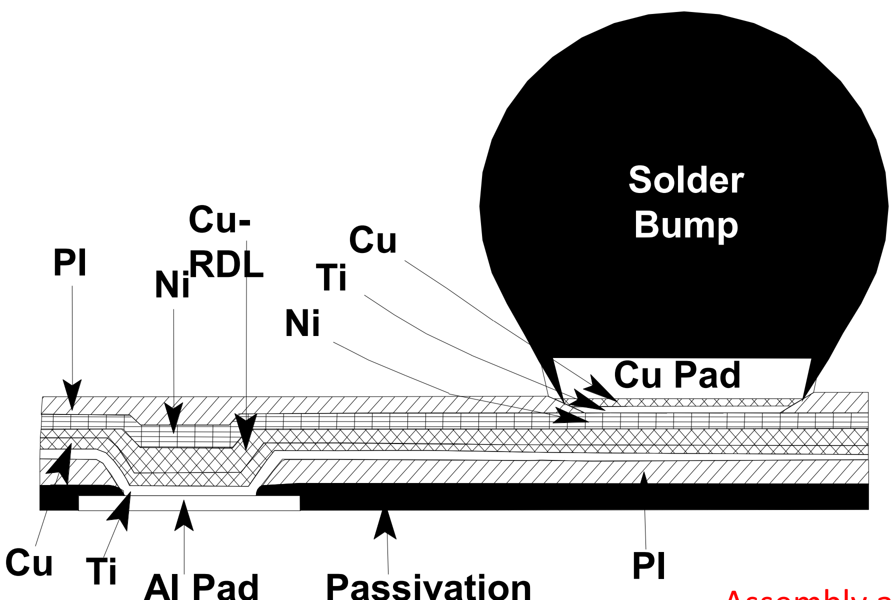
After Wafer Bumping, dicing, then WLCSP Assembly

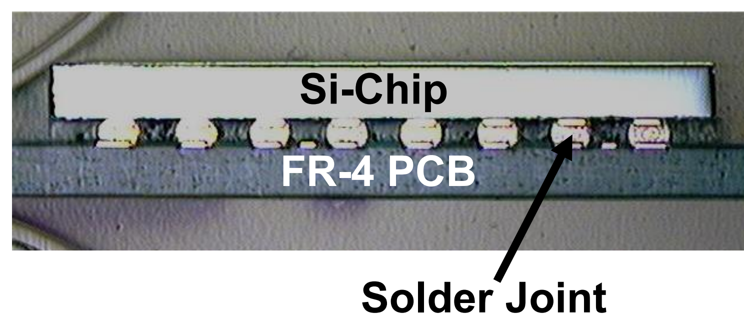


RDL = redistribution layer

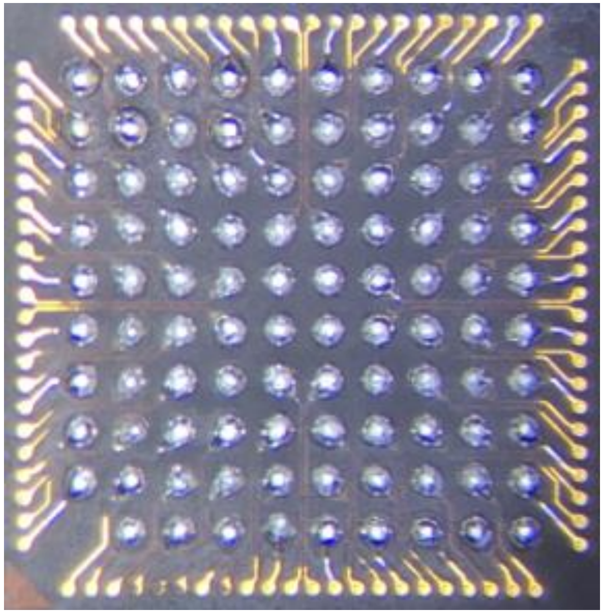
Wafer-Level Chip Scale Package (WLCSP)

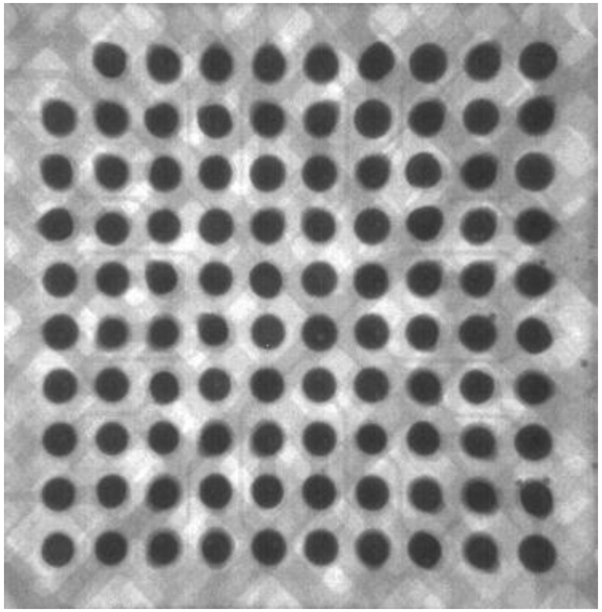


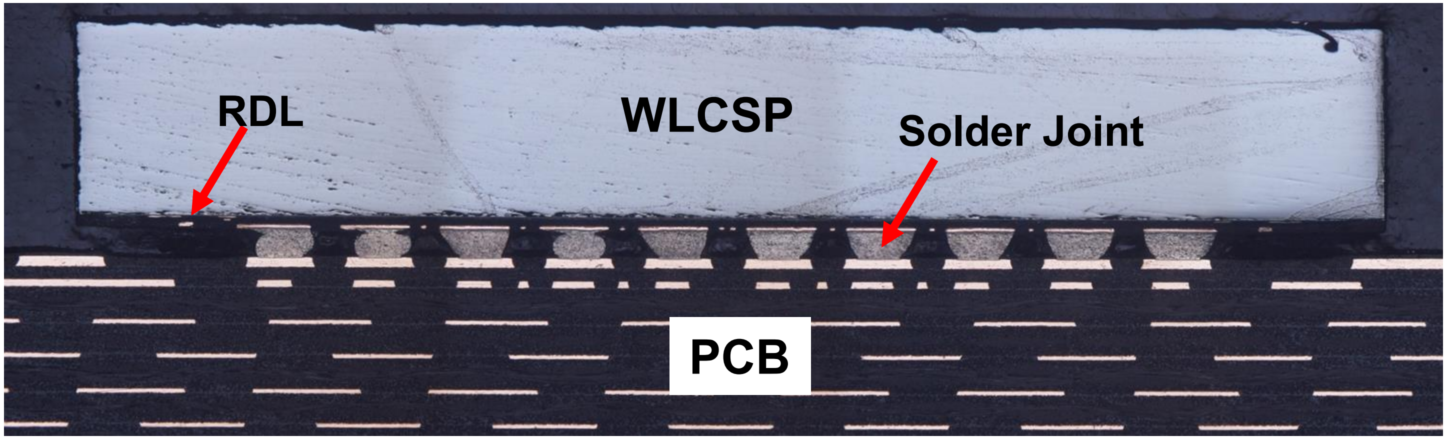




Wafer-Level Chip Scale Package (WLCSP)

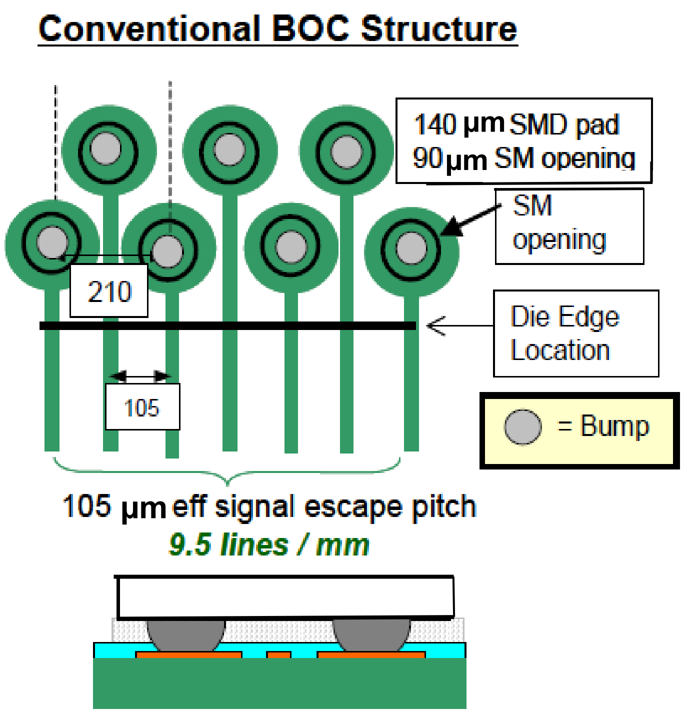


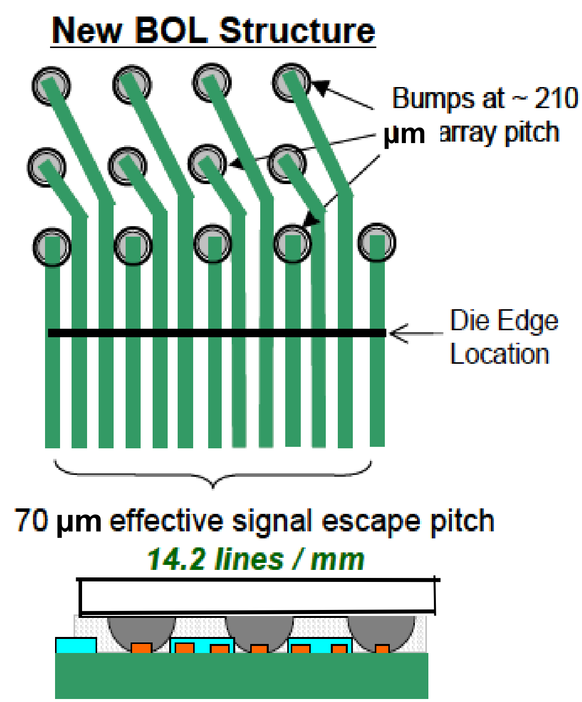


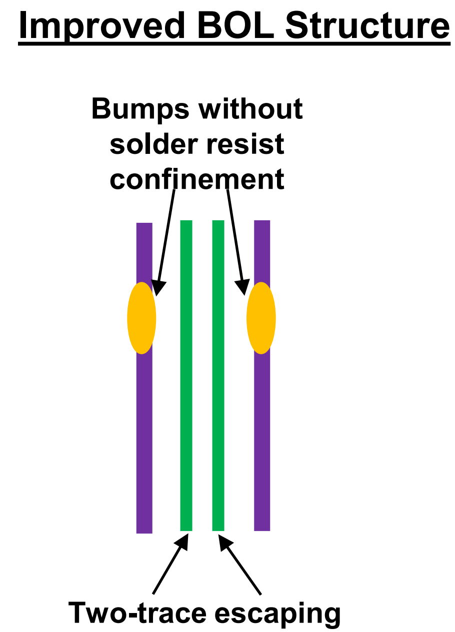


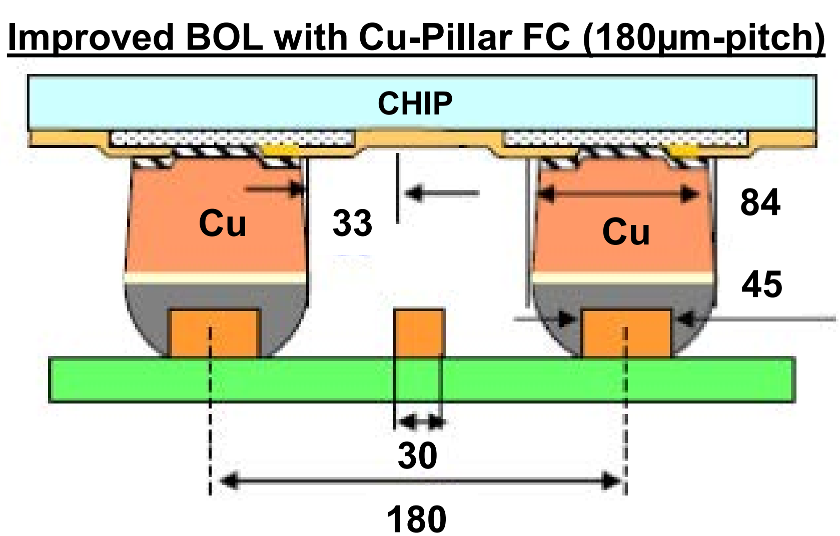
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

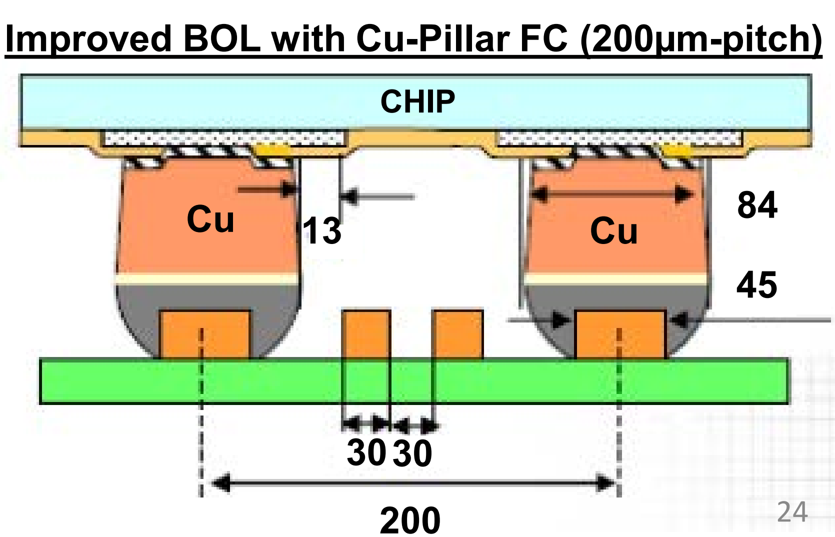
Bump on Lead (BOL)





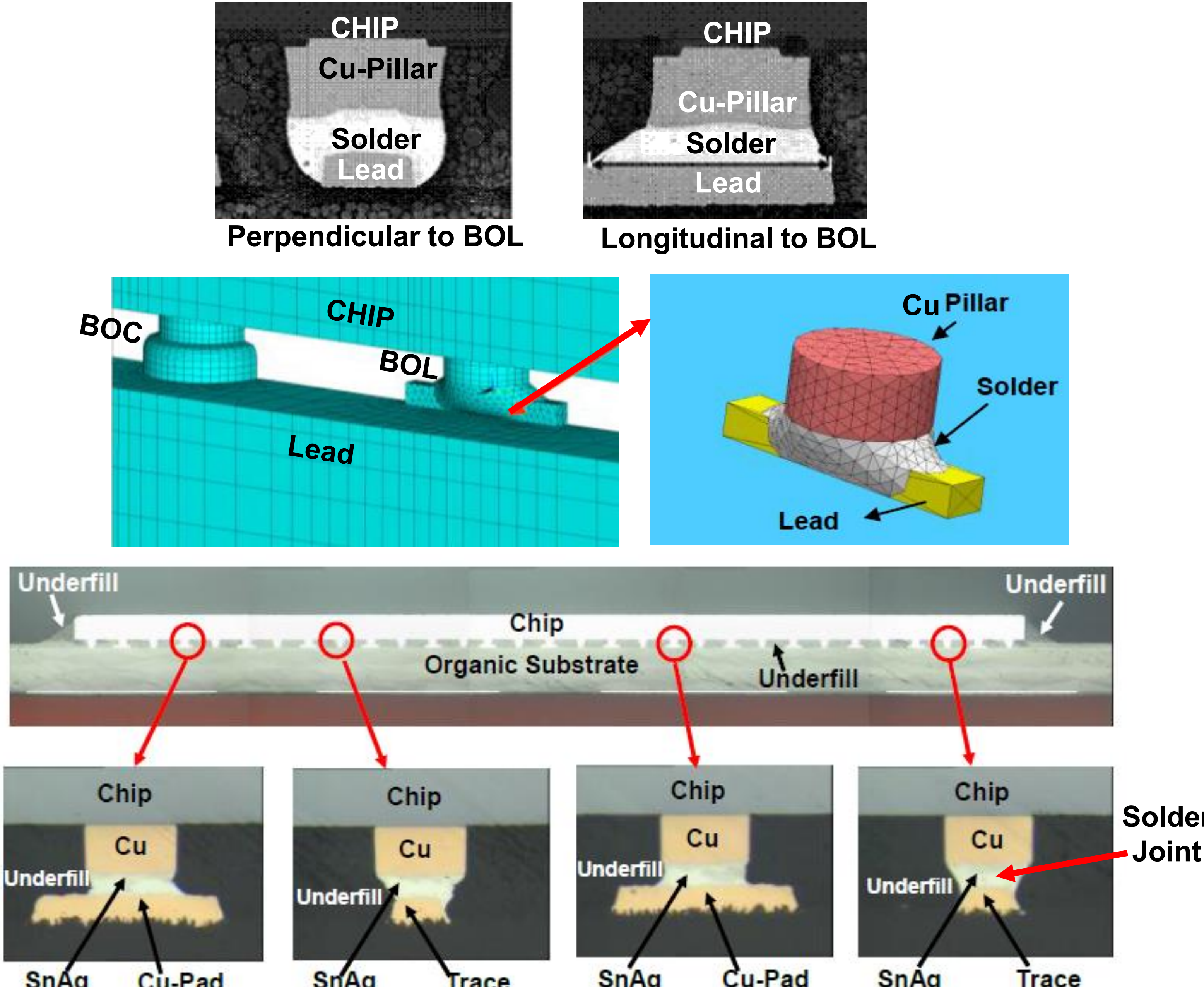






Fan-Out Wafer-Level Packaging, Springer, 2018

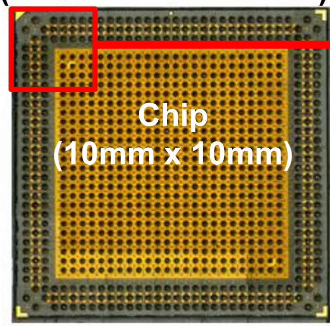
Bump on Lead (BOL)



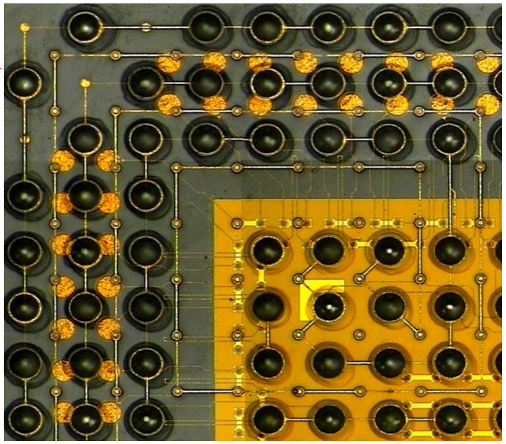
Lau, J. H., et al., "Stencil Printing of Underfill for Flip Chips on Organic-Panel and Si-Wafer Substrates", *IEEE Transactions on CPMT*, Vol. 5, No. 7, July 2015, pp. 1027-1035.

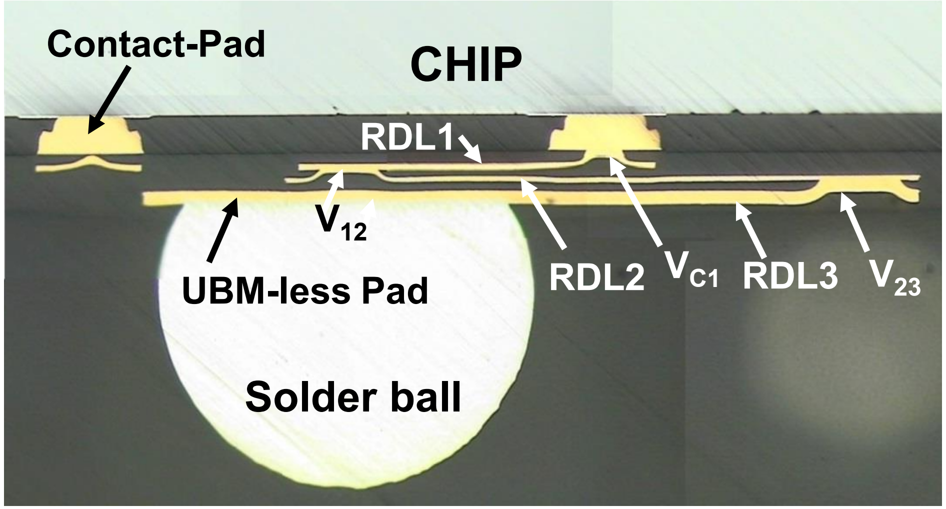
Fan-Out: Chip First (Die Face-Up)

(13.42mm x 13.42mm)



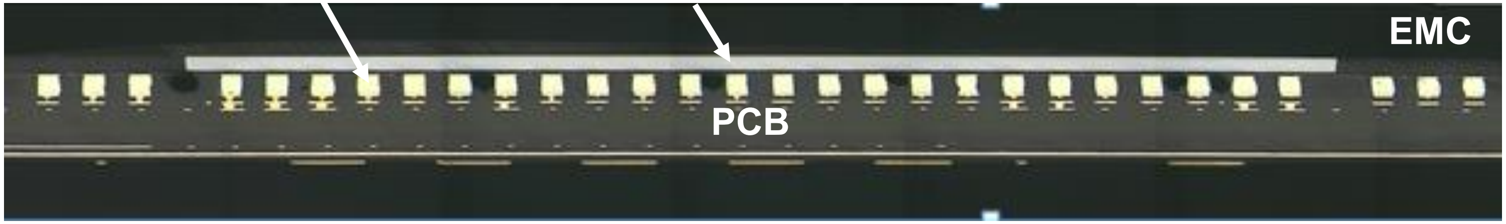
Package





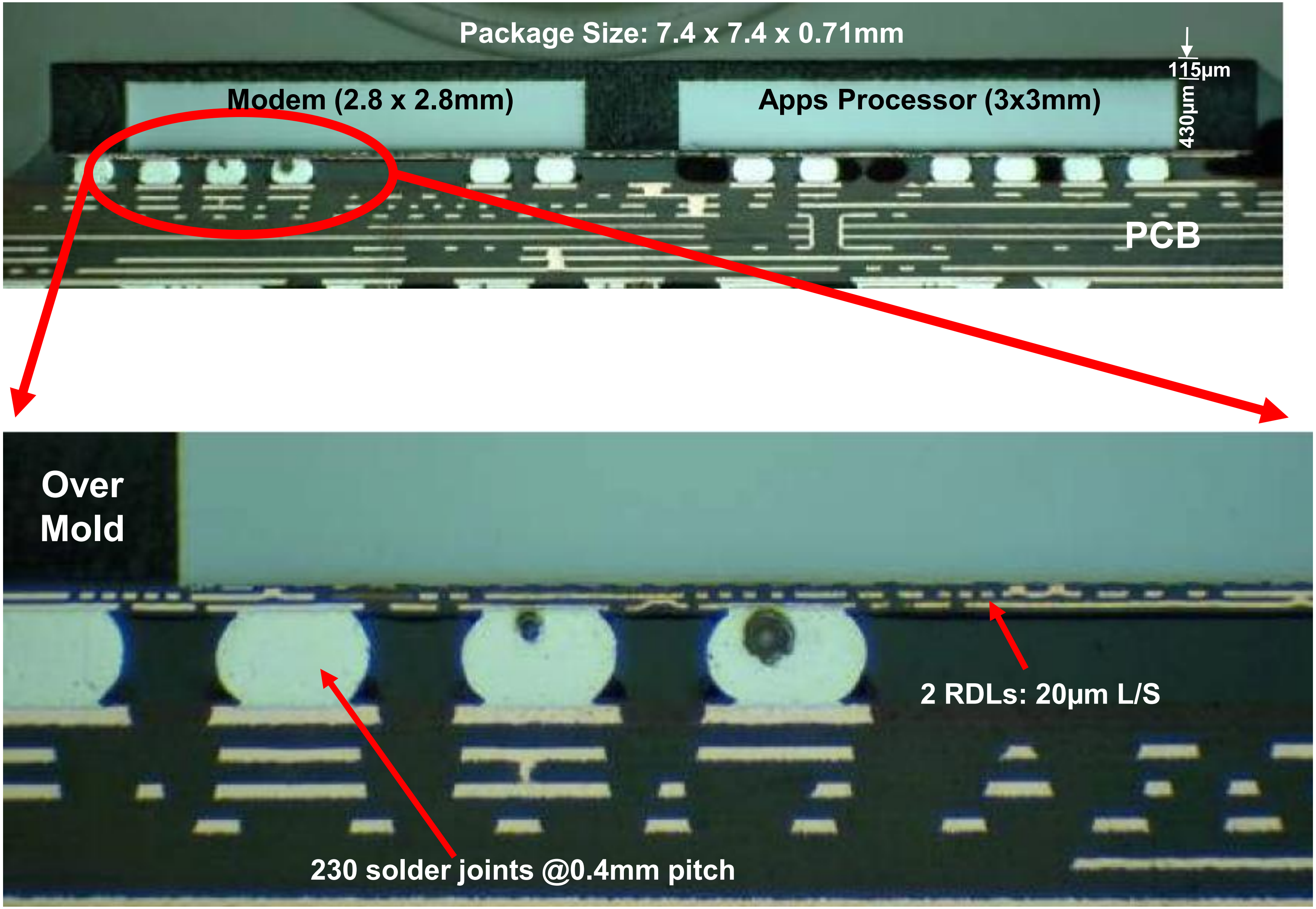
RDL1 = 5μm
RDL2 = 10μm
RDL3 = 15μm

Solder Joint   Chip (10mmx10mm)



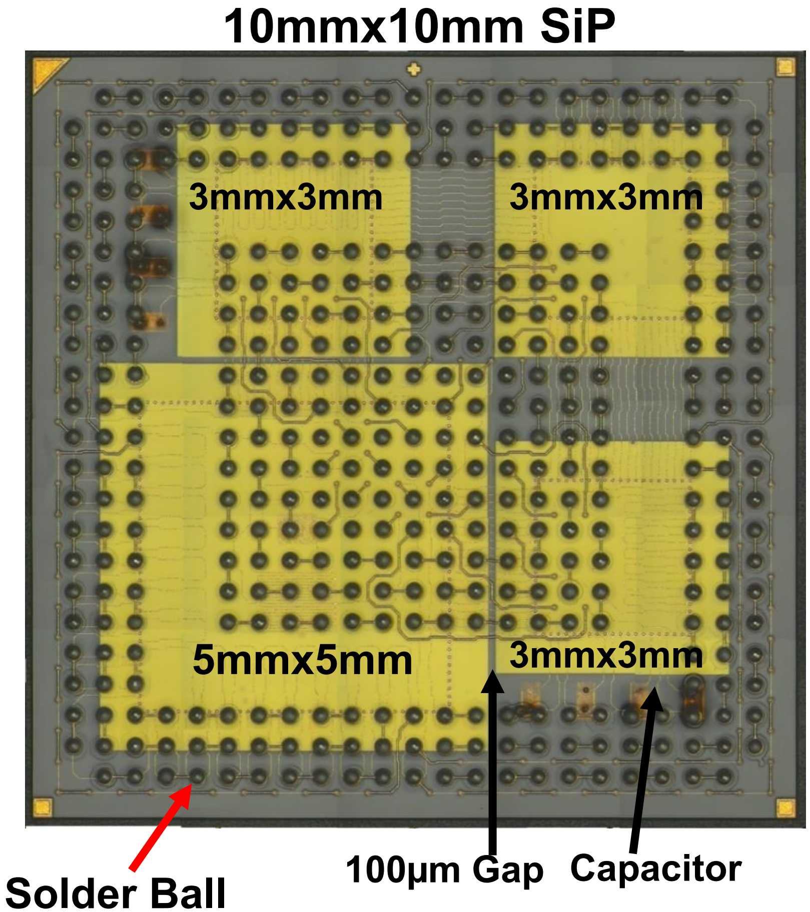
IEEE Trans., CPMT, JUN 2018

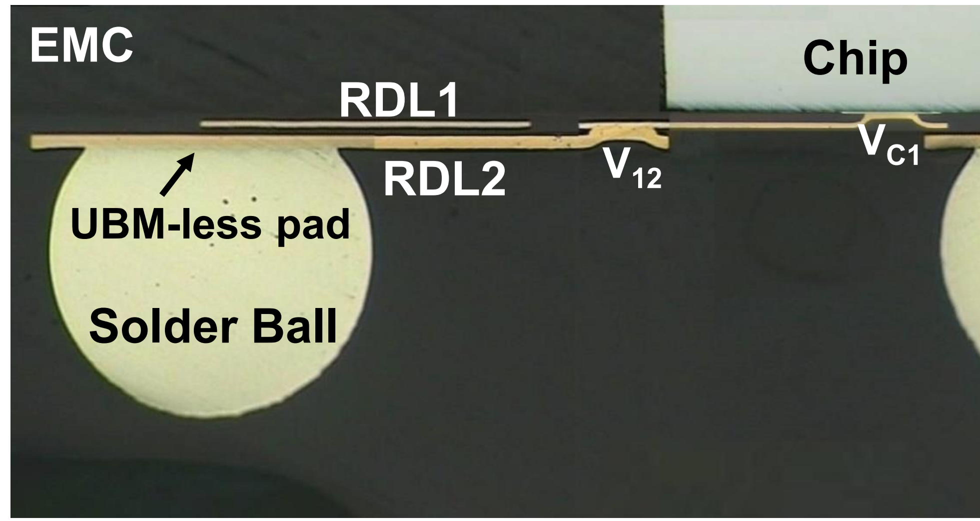
2D Fan-Out: Chip-First (Die Face-Down)



Fan-Out Wafer-Level Packaging, Springer, 2018

2D Fan-Out: Chip-First (Die Face-Down)

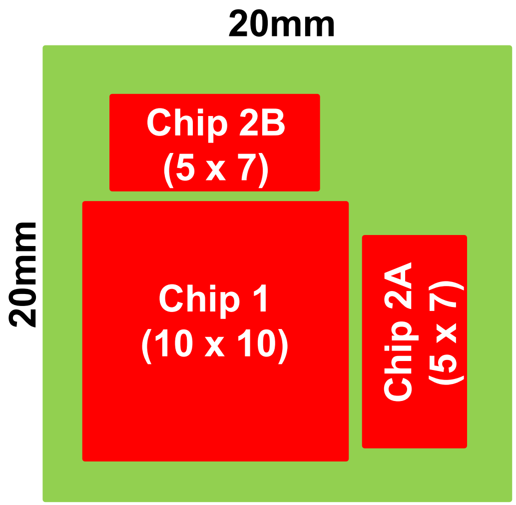


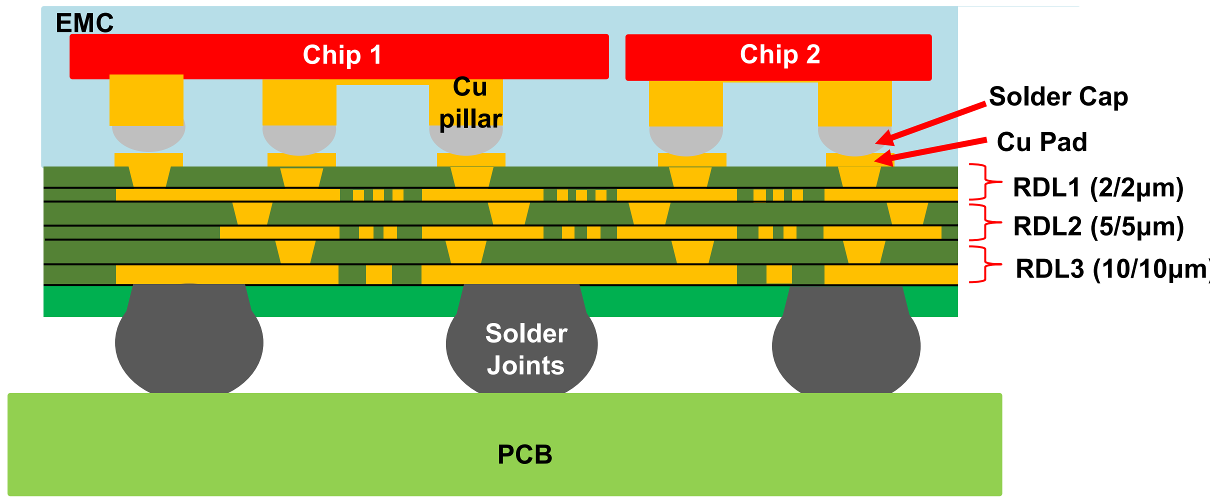


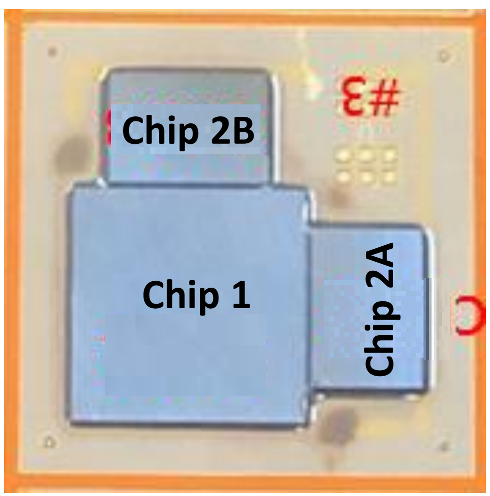
There is no solder bump and substrate which are replaced by RDLs (redistributed-Layers)

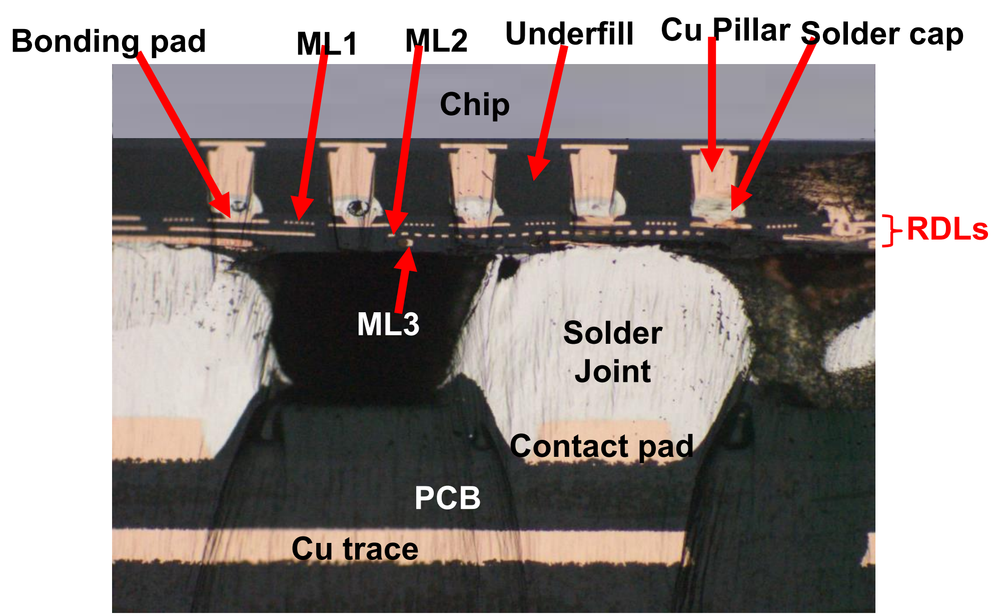
Heterogeneous Integration, Springer, 2019

2D Fan-Out: Chip-Last (RDL-First) Panel-Level Packaging



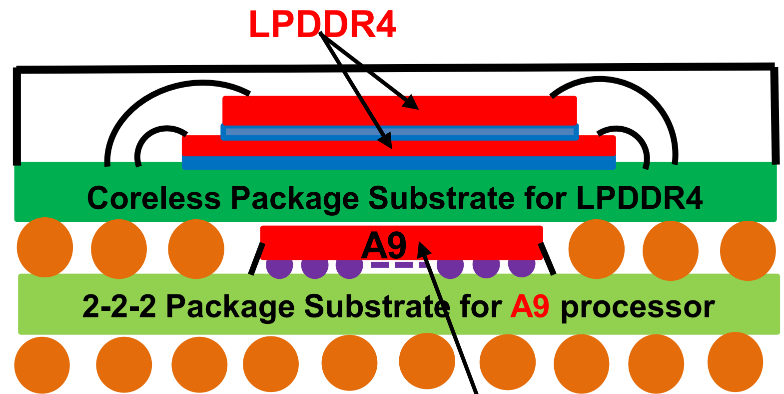




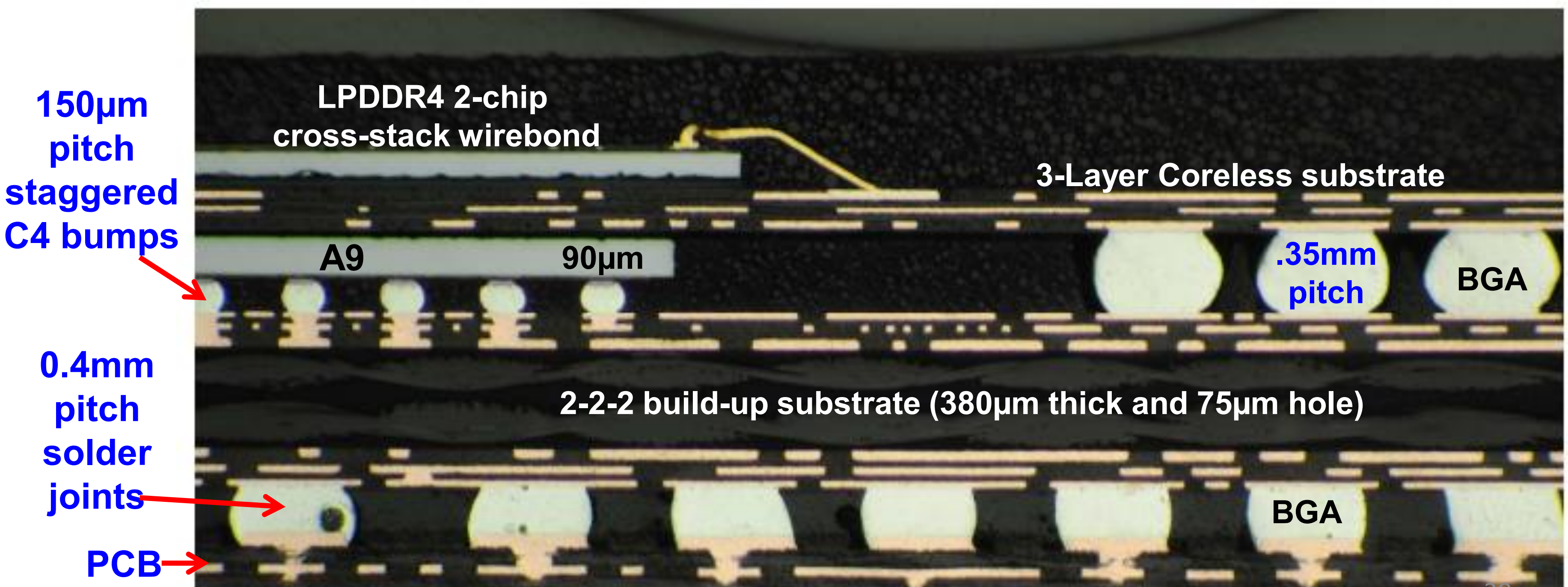


IEEE Trans. on CPMT, JUL 2020

PoP (Package-on-Package) with Flip Chip



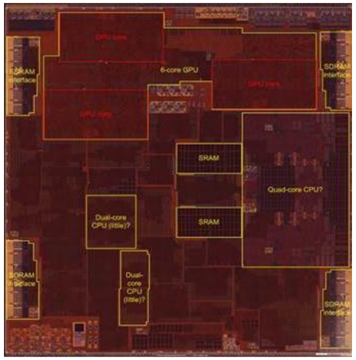
A9 application processor
fabricated by 14/16nm Fin-FET process technology



Fan-Out Wafer-Level Packaging, Springer, 2018

PoP with Fan-Out: Chip First (Die Face-Up)
Apple/TSMC InFO (Integrated fan-Out)

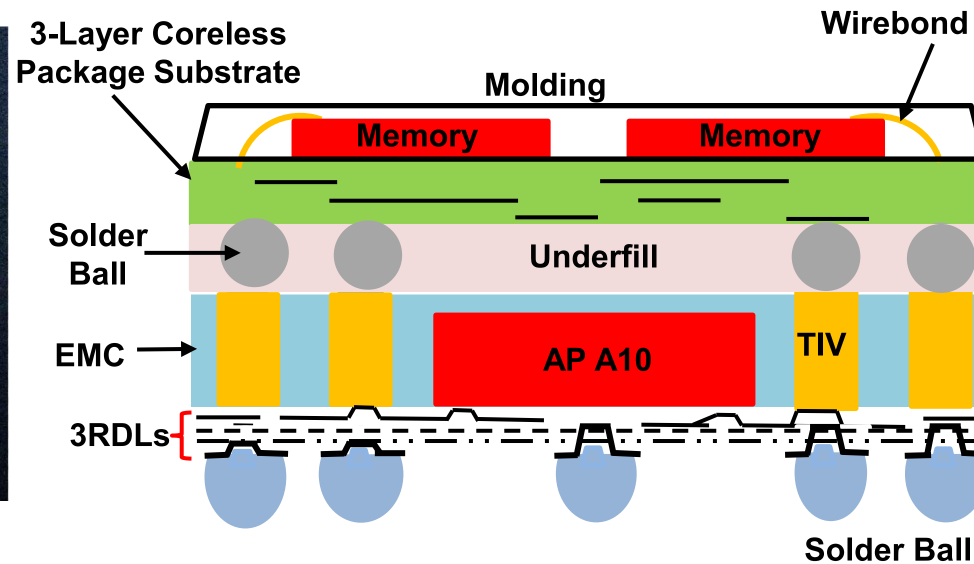
SoC

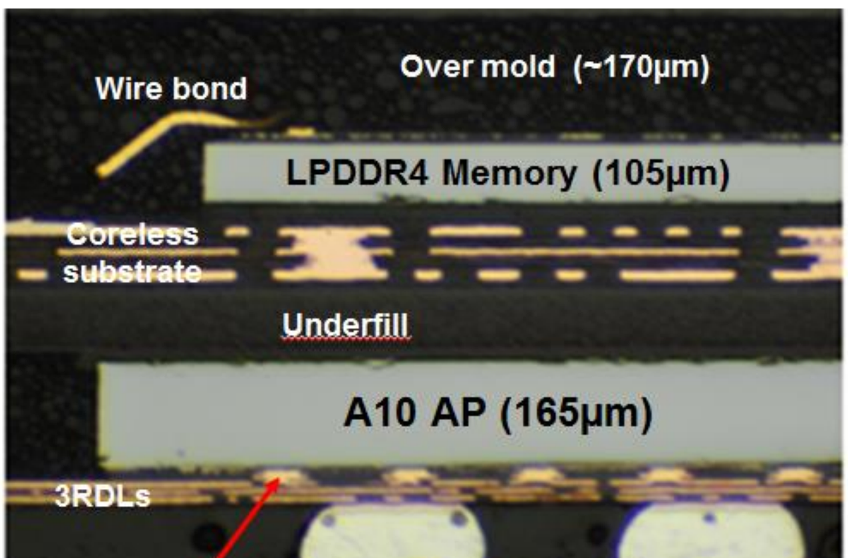


11.6mm x 10.8mm x 165µm

PoP

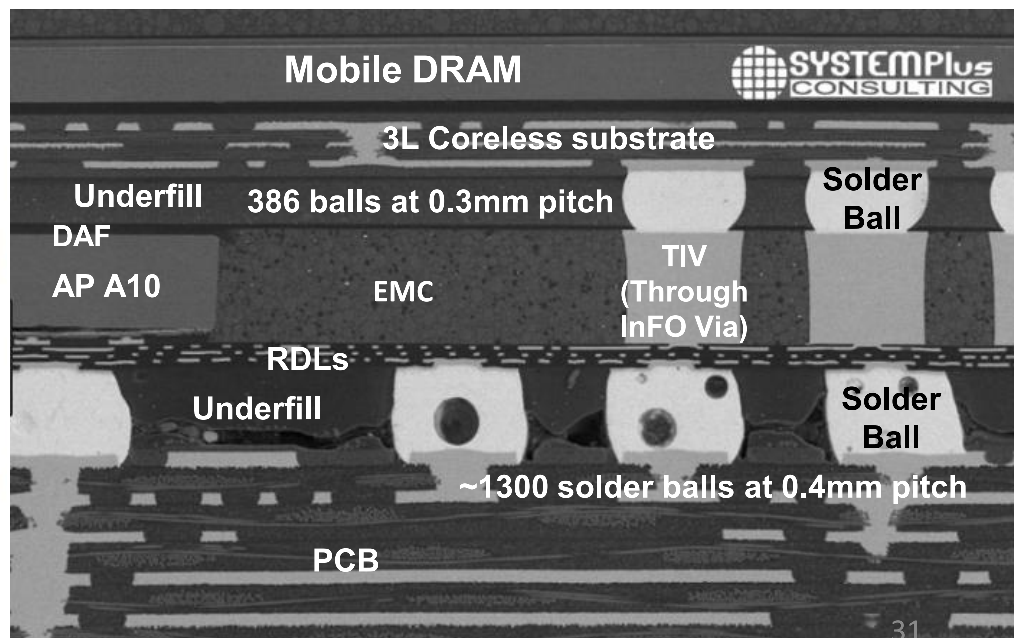
15.5mm x 14.4mm x 825µm





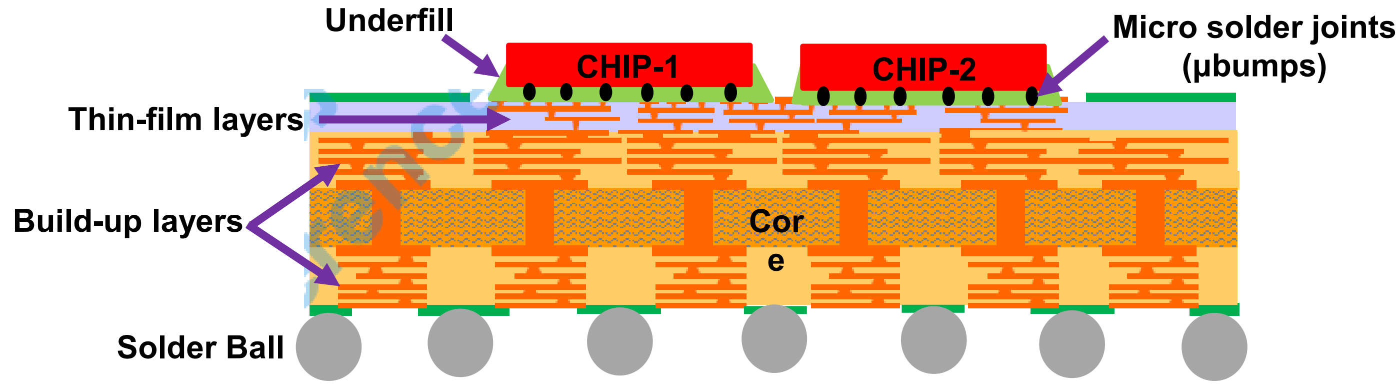
Contact Pad ~1300 solder balls at 0.4mm pitch

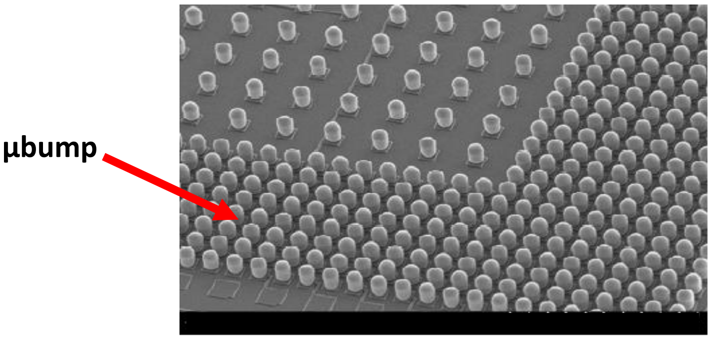
Shipped in 2016



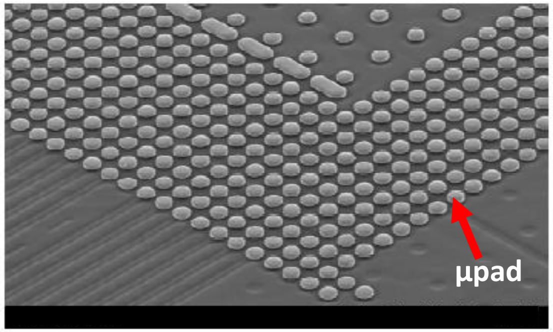
Fan-Out Wafer-Level Packaging, Springer, 2018

2.1D IC Integration with Thin-Film Layers Built Directly on Build-up Package Substrate (Shinko)

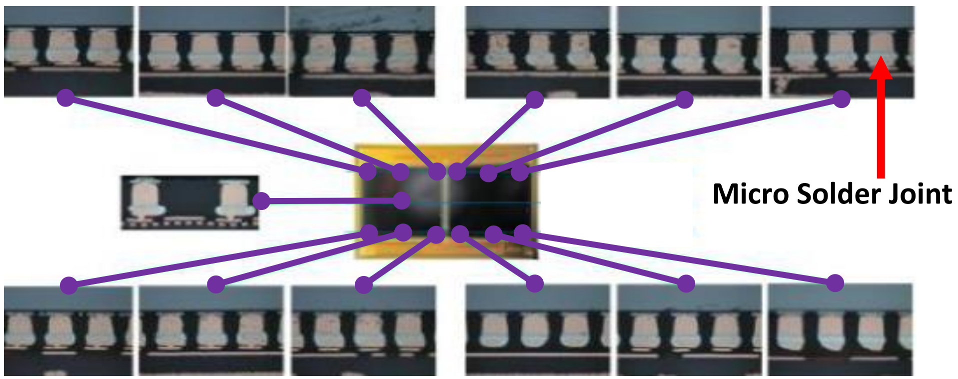




SEM image of test chip with µbumps



40µm pitch flip chip bonding pads

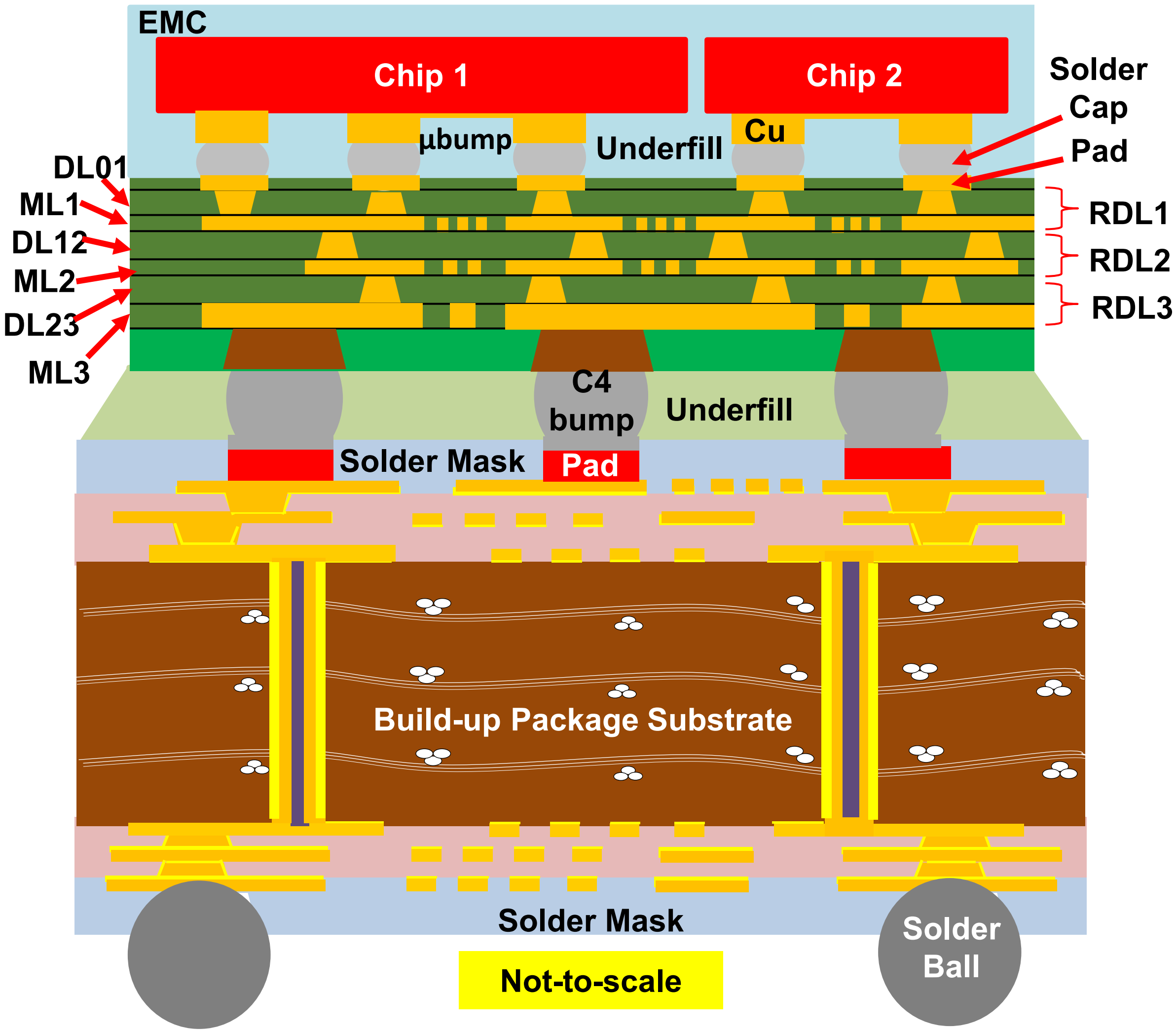


IMAPS 2013, ECTC2014

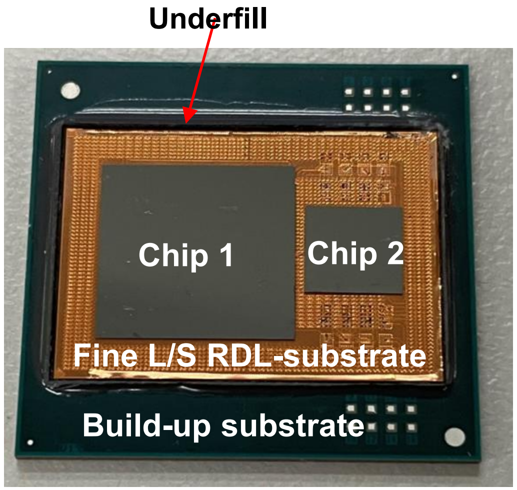
2.3D IC Integration: Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration

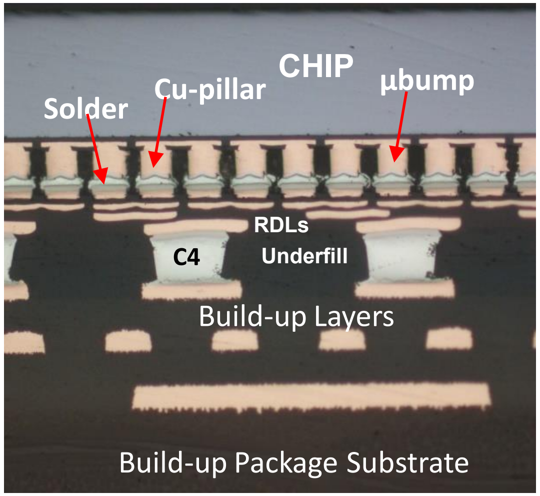
John H Lau, Gary Chang-Fu Chen, Jones Yu-Cheng Huang, Ricky Tsun-Sheng Chou, Channing Cheng-Lin Yang, Hsing-Ning Liu, and Tzvy-Jang Tseng
Unimicron Technology Corporation,
Taoyuan City, Taiwan
John_Lau@unimicron.com

Chip-Last



Not-to-scale



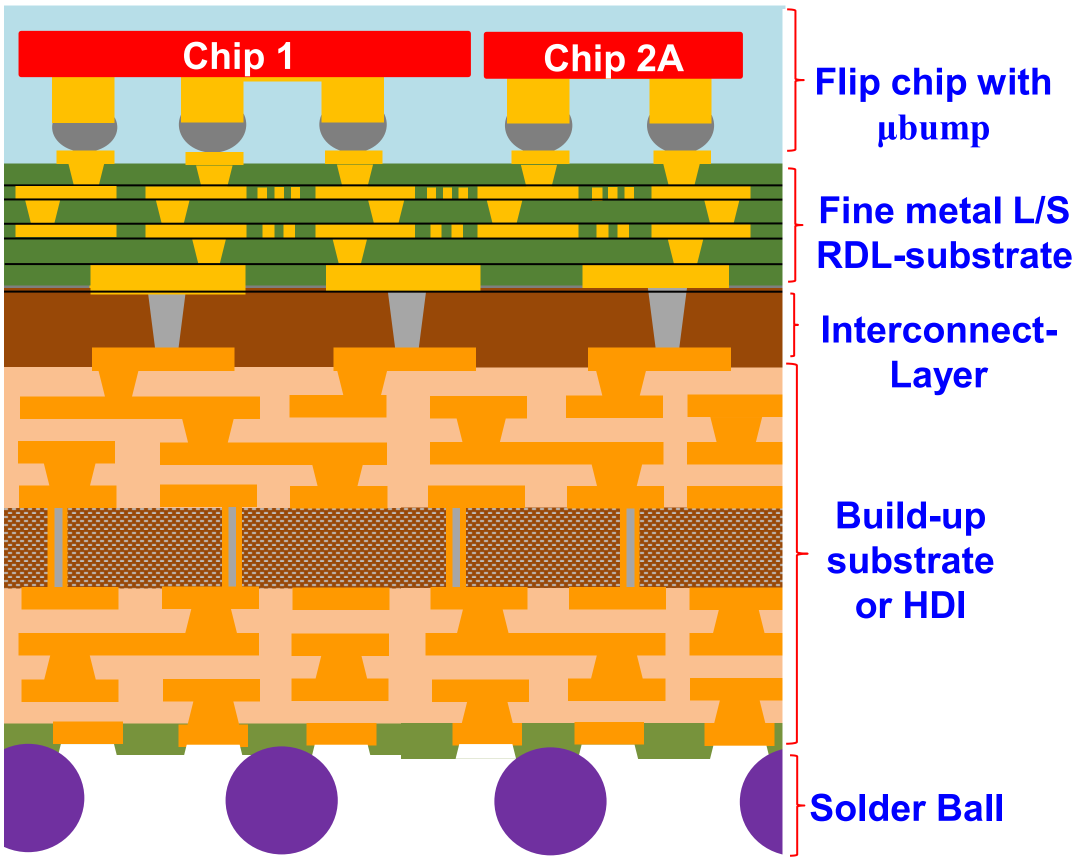


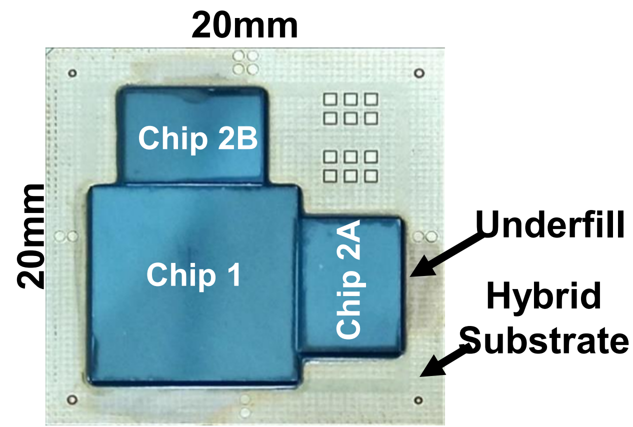
IEEE Trans. on CPMT, 2021

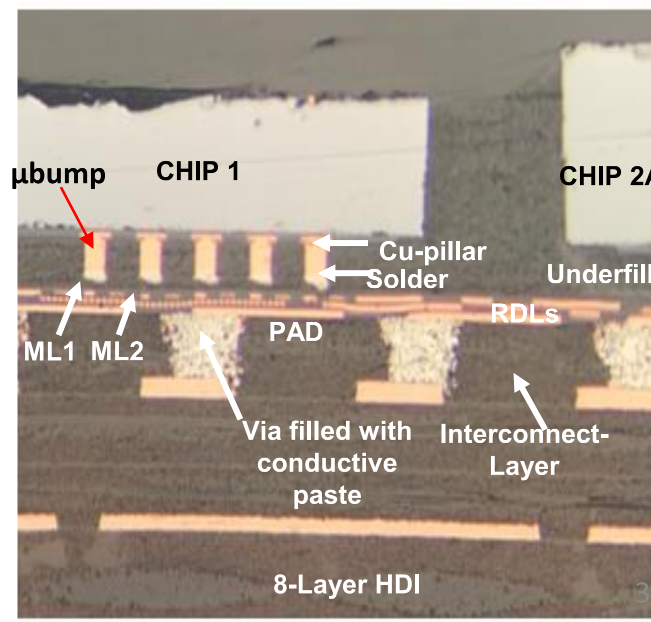
2.3D IC Integration: High-Density Hybrid Substrate for Heterogeneous Integration

Chia-Yu Peng , John H. Lau , Life Fellow, IEEE, Cheng-Ta Ko, Paul Lee, Eagle Lin, Kai-Ming Yang, Puru Bruce Lin, Tim Xia, Leo Chang, Ning Liu, Curry Lin, Tzu Nien Lee, Jason Wong, Mike Ma, Tzyy-Jang Tseng
Unimicron

Chip-Last

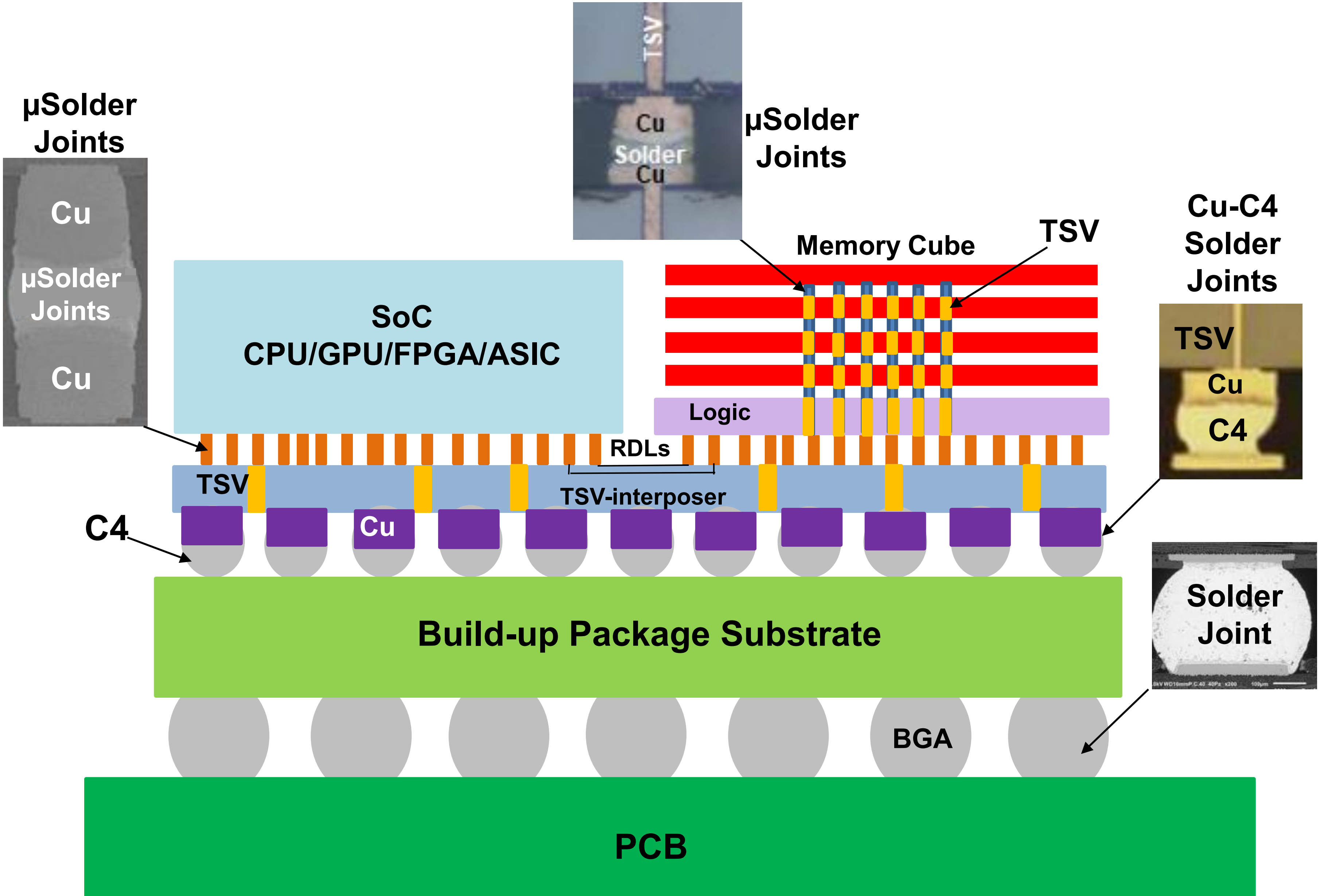






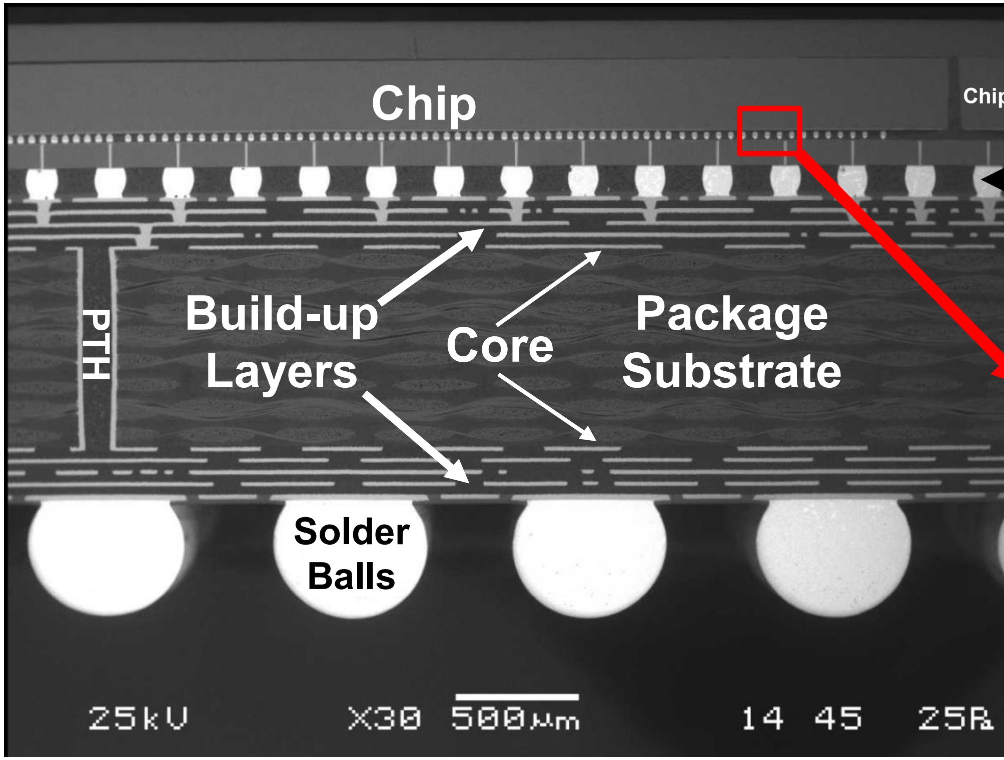
IEEE Transactions on CPMT, March 2022

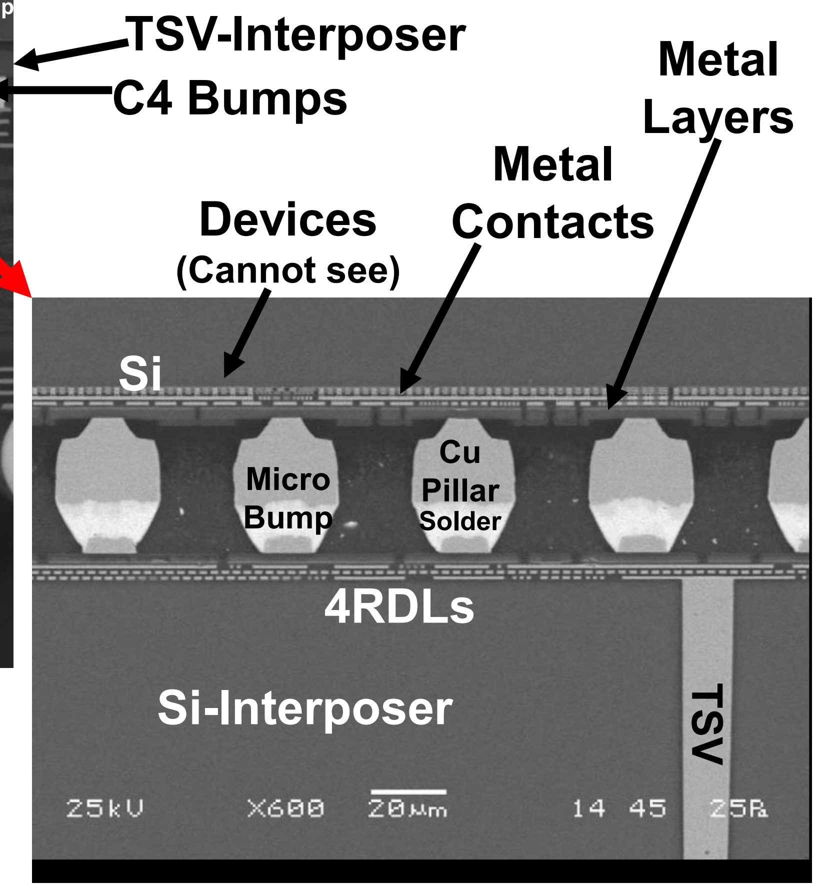
2.5D IC Integration



 Semiconductors for HPC applications driven by AI and 5G

Xilinx's 2.5D IC Integration with FPGA





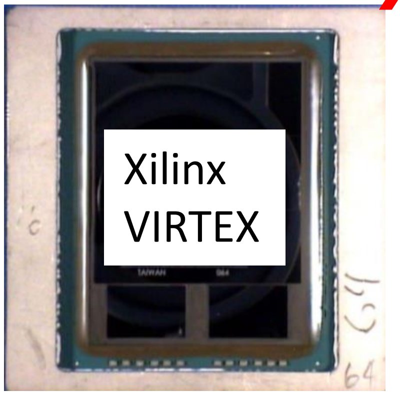
CoWoS
(chip on wafer on substrate)

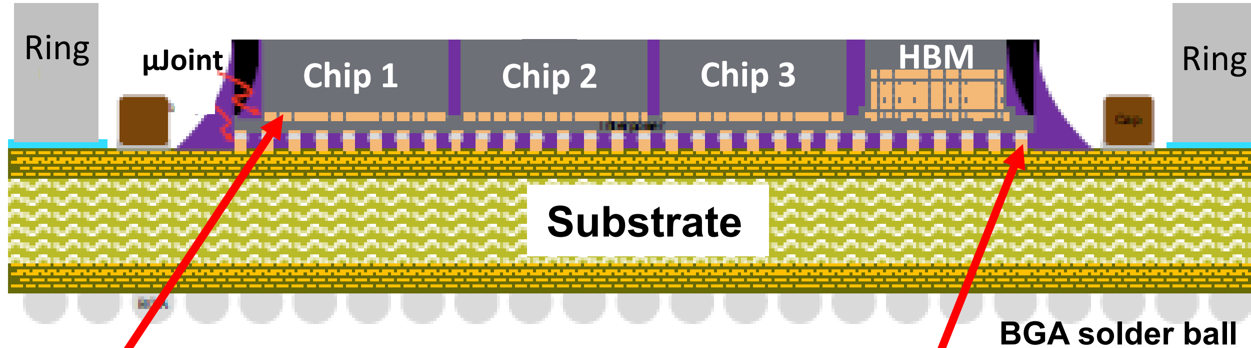
Homogeneous Integration on Si-substrate

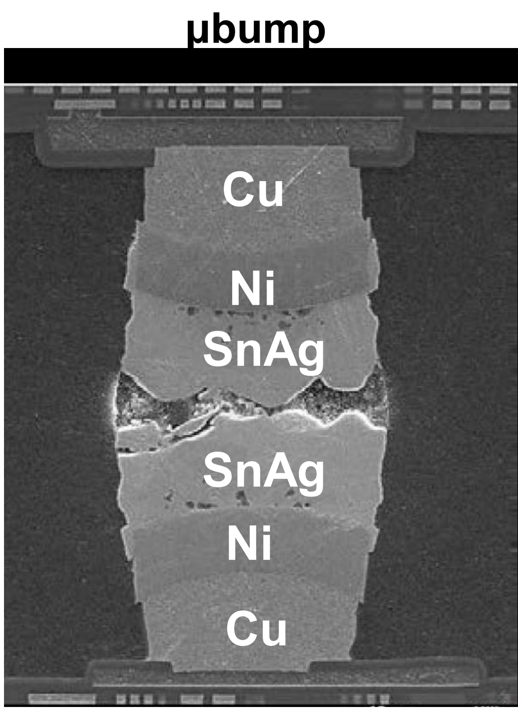
- RDLs: 0.4µm-pitch line width and spacing
- Each FPGA has >50,000 µbumps on 45µm pitch
- Interposer is supporting >200,000 µbumps

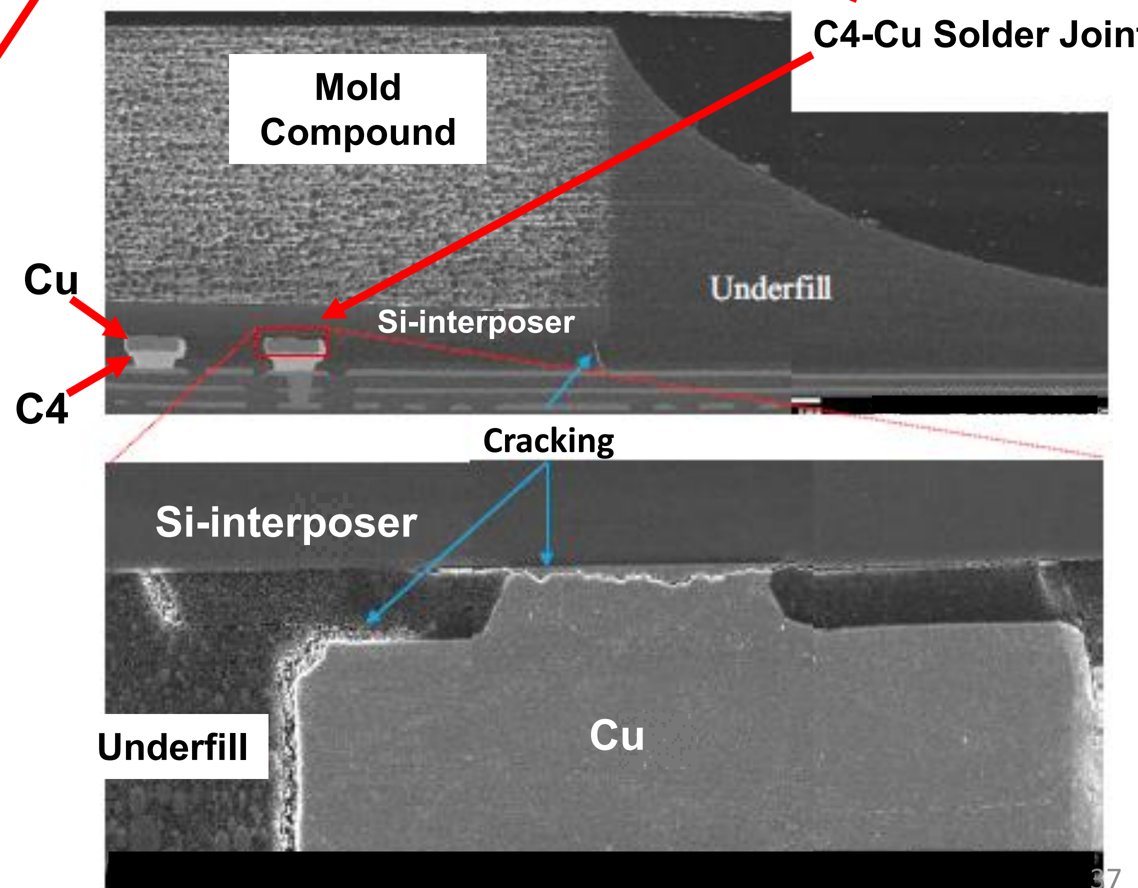
IEEE/ECTC2013

Xilinx's 2.5D IC Integration



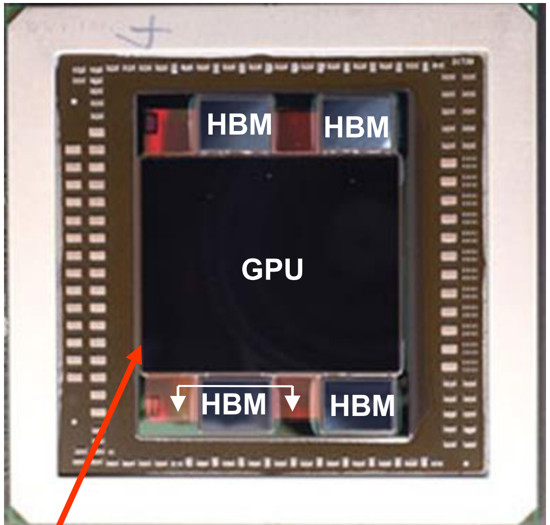


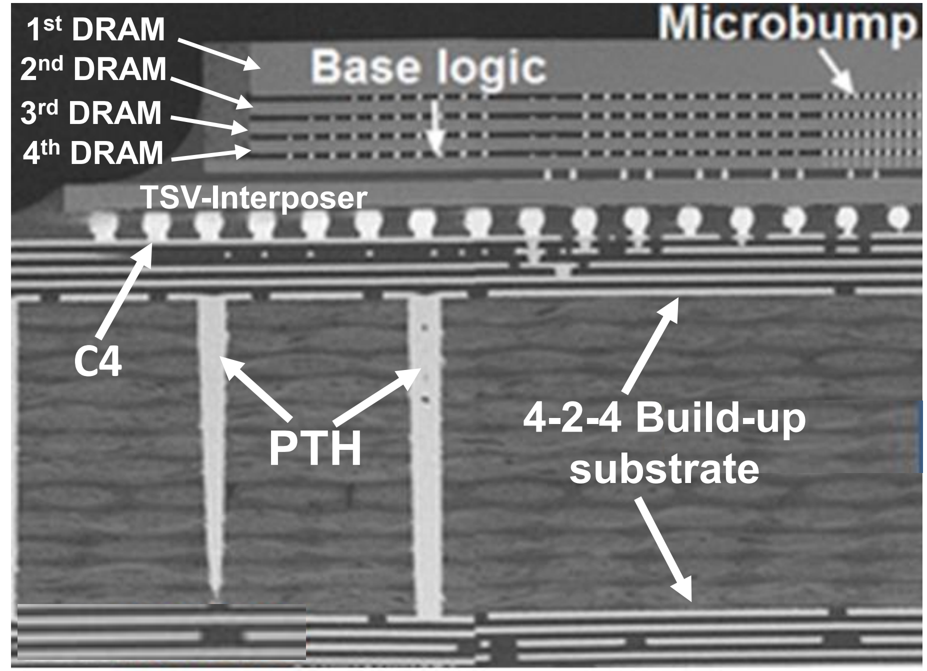




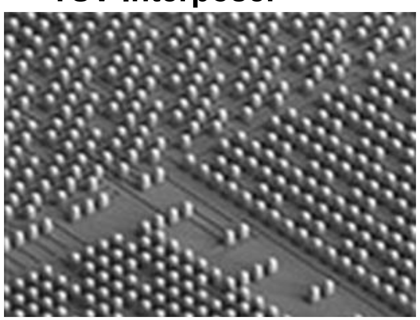
Shipped in 2013, 2019

AMD's 2.5D IC Integration

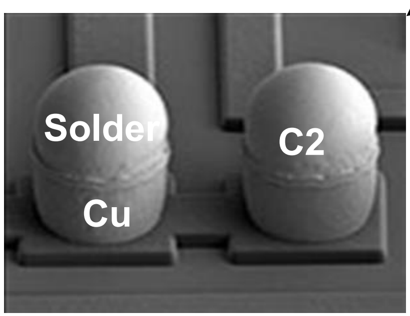


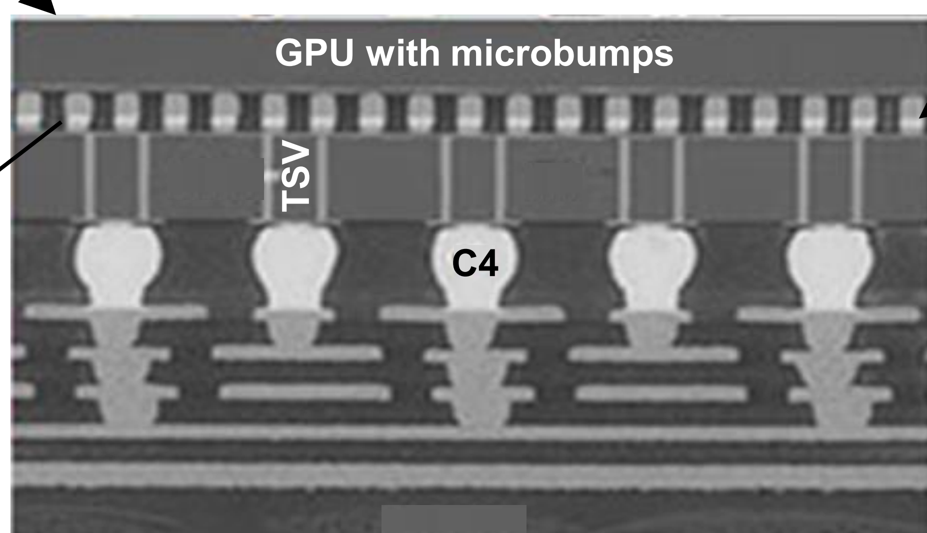


TSV-Interposer



Cu-Pillar with solder Cap





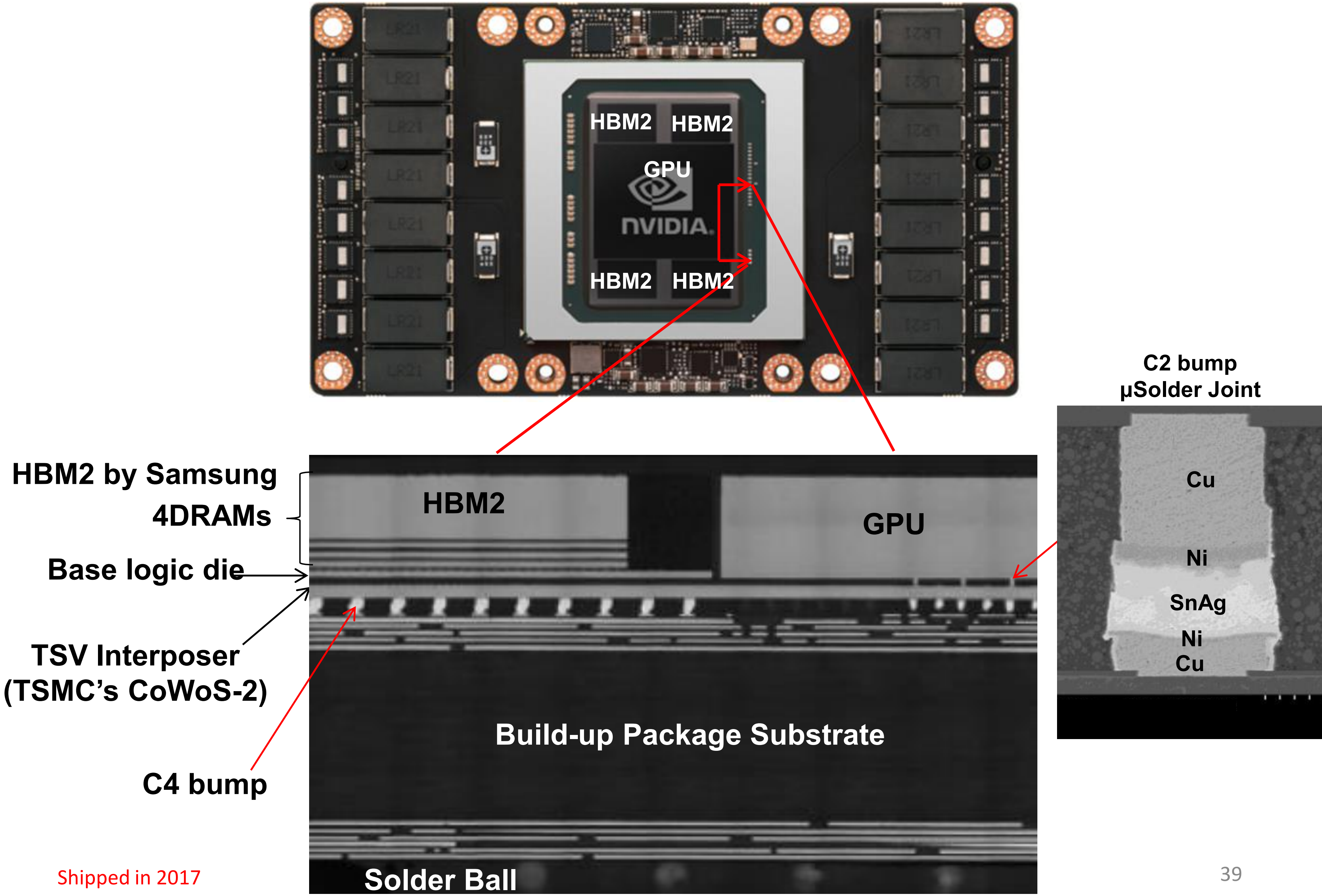
C2

TSV-Interposer

Build-up organic substrate

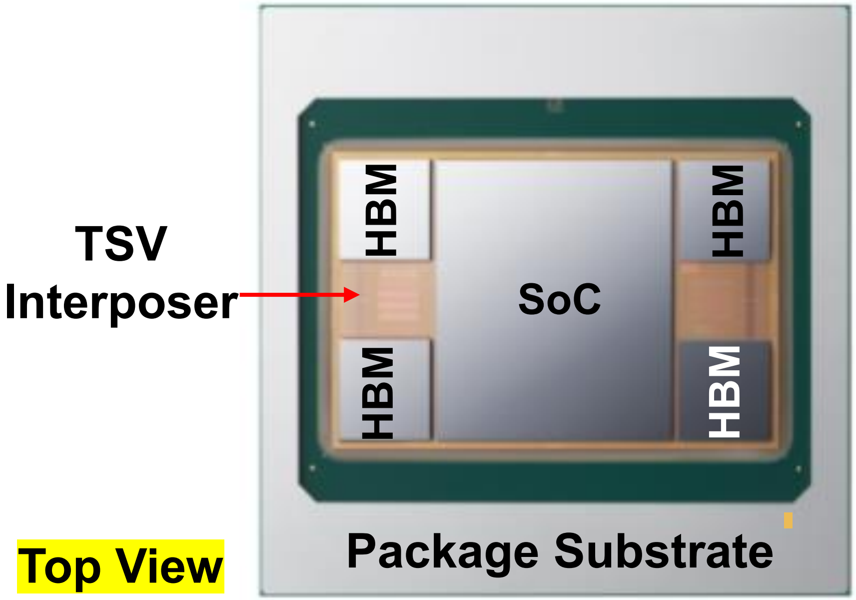
Shipped in 2016

NVidia's 2.5D IC Integration

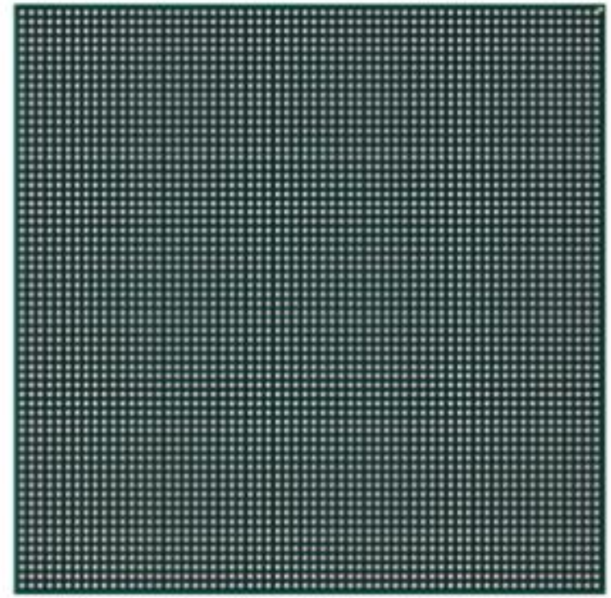


Shipped in 2017

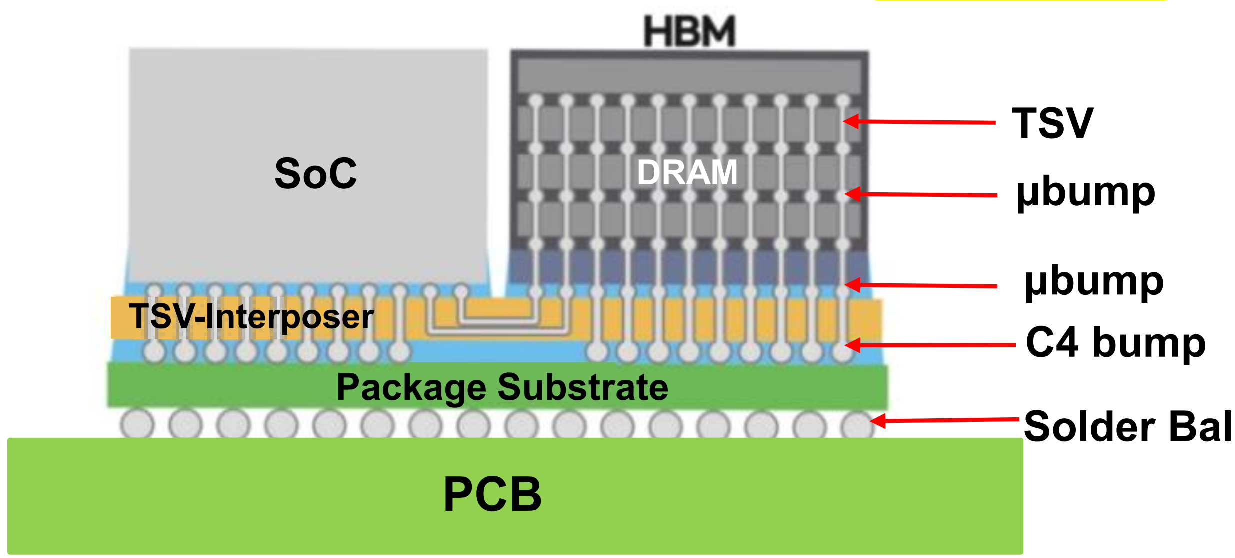
Samsung's Interposer-Cube4 (I-Cube4)
(2.5D IC Integration)



Top View



Bottom View



Cross-section
View

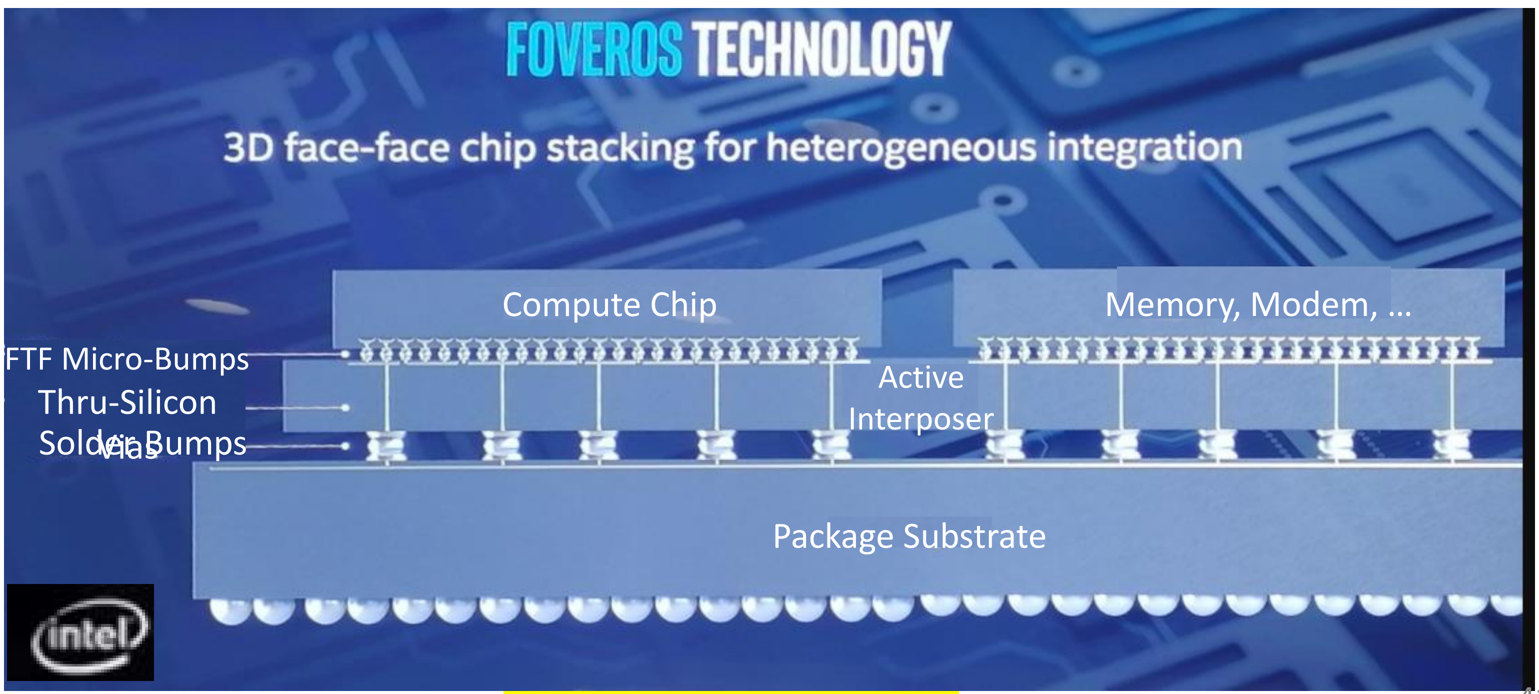
May 21,2021

Intel 3D IC Integration – FOVEROS Technology

Lakefield

10mm

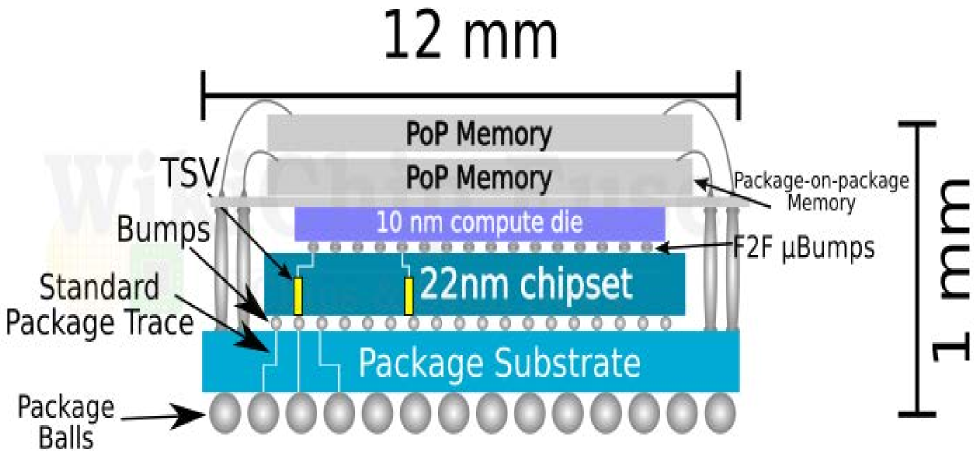
10mm



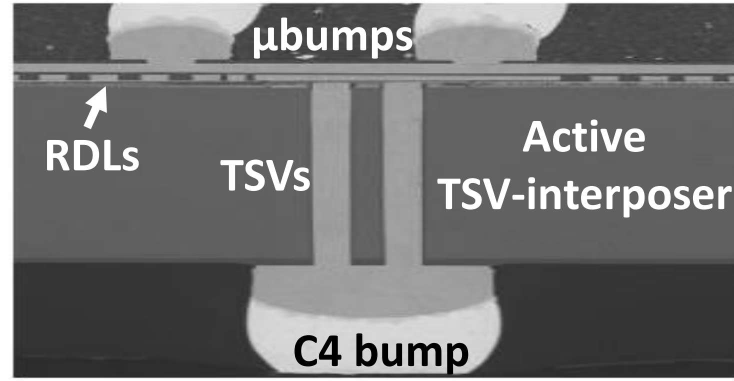
Shipped in 2020

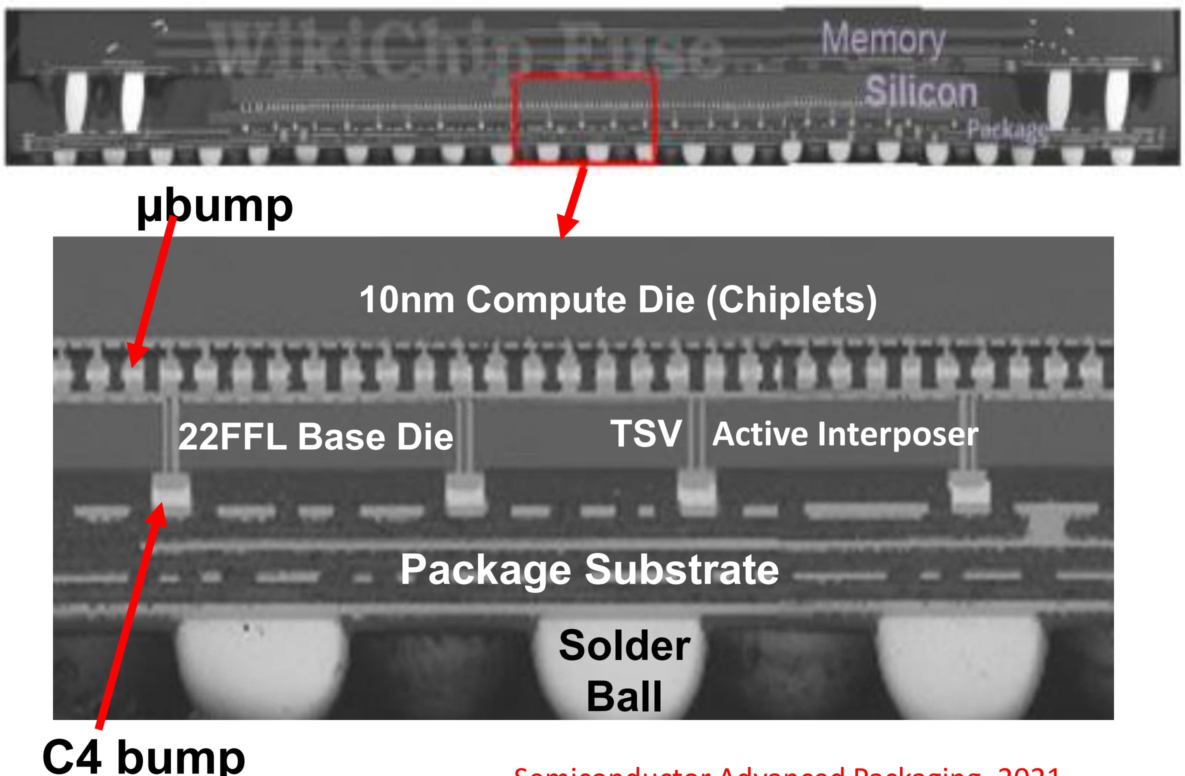
3D IC Integration

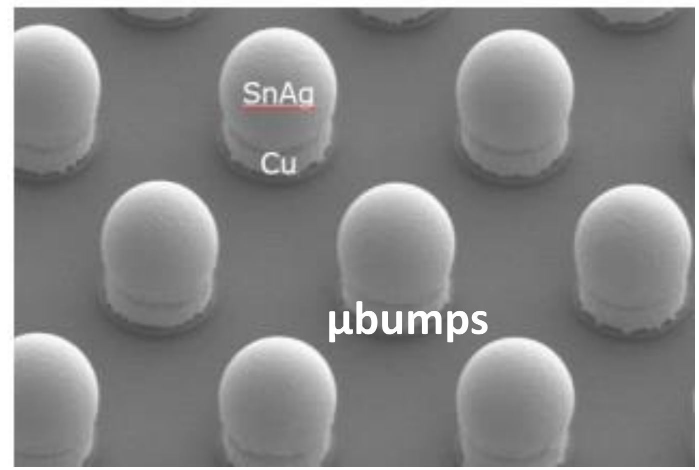
Intel 3D IC Integration – FOVEROS Technology

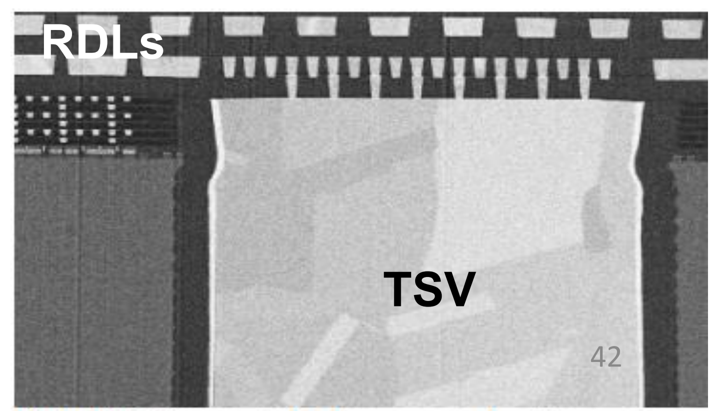


Lakefield









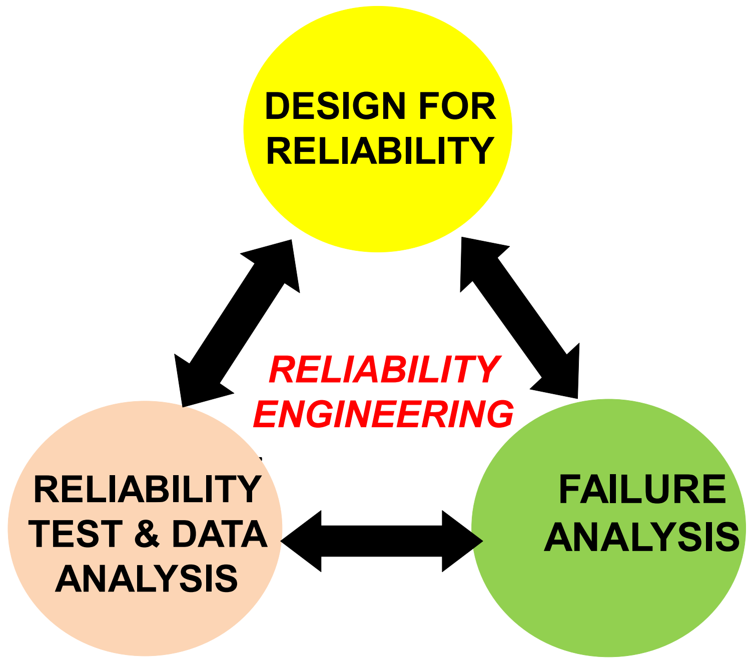
Reliability Testing and Data Analysis of Lead-Free Solder Joints

CONTENTS

Reliability Engineering

- Eliminate trial-and-error of reliability tests
- Reduce design/test/failure analysis cycles
- Comparison between material/geometry of structure
- Provide insight into the physical, chemical, electrical, mechanical, and thermal behaviors of the structure, e.g., failure location and failure mode

- Sample Size
- Test Condition
- Test Period
- Obtain Failures
- Life Distribution
- Reliability
- Failure Rate
- Mean-Time-to-Failure



- Provide Failure Locations, Failure Modes, and Failure Mechanisms
- Verify the reliability test data
- Verify the DFR analysis results
- Understanding why it failed and how to fix it or do better for the next round of DRF and Reliability test
- Help to chose acceleration models to determine the acceleration factors

Design for Reliability, Reliability Testing and Data Analysis, and Failure Analysis of Solder Joints, NEPCON West Workshops, Anaheim, CA, February 1990.

Definition of Reliability

- In this lecture, reliability of an interconnect (e.g., solder bump, solder joint, or microbump) of a particular package in an electronic product is defined as;
  - the probability that the interconnect will perform its intended function for a specified period under a given operating condition without failure.
- Numerically speaking, reliability is the percent of survivors; that is,
  - $R(x) = 1 – F(x)$,
    where $R(x)$ is the reliability (survival) function and $F(x)$ is the cumulative distribution function (CDF).
  - Life distribution is a theoretical population model used to describe the lifetime of an interconnect and is defined as the CDF, that is, $F(x)$ for the interconnect population.
- Thus, the one and only way to determine the interconnect reliability is by reliability testing to determine the $F(x)$

Design for Reliability, Reliability Testing and Data Analysis, and Failure Analysis of Solder Joints, NEPCON West Workshops, Anaheim, CA, February 1990.

Objective of Reliability Test

- **The objective of reliability tests is to obtain failures (the more, the better) and to best fit the failure data to determine the parameters of the CDF, F(x), of a chosen probability distribution (e.g., Weibull and lognormal).**

- **The number of items (i.e., sample size) to be tested should be such that the final data are statistically significant.**

- **The reliability test time is unknown, but usually takes a while (e.g., a few months for thermal cycling tests).**

- **It should be noted and emphasized that as soon as the life distribution F(x) of the interconnects is estimated by reliability testing, the reliability R(x), failure rate, cumulative failure rate, average failure rate, mean-time-to-failure, etc. of the interconnects are readily determined.**

- **Most reliability tests are accelerated tests, with increased intensity of exposure to aggressive environmental conditions and realistic sample sizes and test times. Thus, acceleration models are needed to map (transfer) the failure probability, reliability function, failure rate, and mean-time-to-failure from a test condition to an operating condition.**

Design for Reliability, Reliability Testing and Data Analysis, and Failure Analysis of Solder Joints, NEPCON West Workshops, Anaheim, CA, February 1990.

Objective of Qualification Test

- **Unlike reliability tests, the objective of qualification tests is "PASS" or "NOT PASS" and the test time is well defined ahead of time.**

- **As soon as there is a failure before the agreed test time, the test will usually stop and failure analysis is performed to find out why it fails.**

- **After all the changes, e.g., redesign, a new qualification test will start again.**

- **The sample size of qualification tests is usually less than that of reliability tests.**

- **In short, the objective of qualification tests is not intended to obtain failures nor life distribution (or reliability).**

Design for Reliability, Reliability Testing and Data Analysis, and Failure Analysis of Solder Joints, NEPCON West Workshops, Anaheim, CA, February 1990.

Test Methods

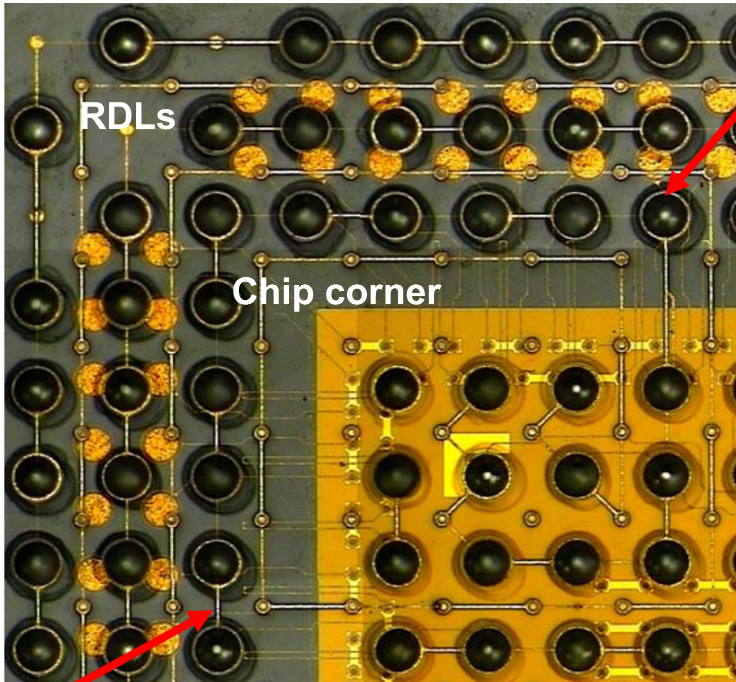
Some common tests for semiconductor packaging and interconnection are:

- temperature cycling tests (e.g., 25 ⇆ 125 C),
- power cycling tests (depend on devices),
- functional cycling tests (depend on devices),
- high-/low-temperature storage tests (120^{o}C/20^{o}C),
- biased 85/85 tests (85 C/85% relative humidity, 1.8 V),
- high-voltage extended life tests (100^{o}C, 1.8 V),
- pressure cook tests (autoclave tests) (121^{o}C, 2 atm),
- salt atmosphere test (MIL-STD-883D),
- moisture sensitivity tests (e.g., IPC/JEDEC-020C),
- shock (drop) tests (e.g., JESD 22-B111),
- vibration tests (e.g., JESD 22-B103),
- mechanical bending and shearing tests (e.g., IPC/ JEDEC-9702),
- electromigration test (e.g., JEP154),
- others

Thermal Cycling Test

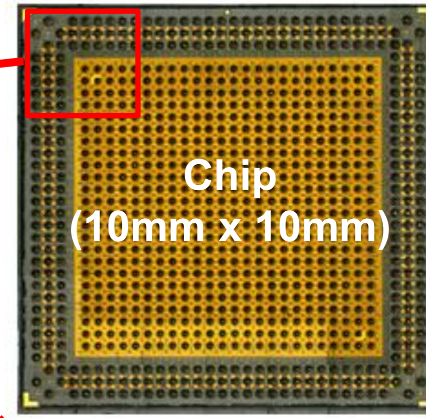
Drop (Shock) Test

FOWLP and the Reliability test PCB

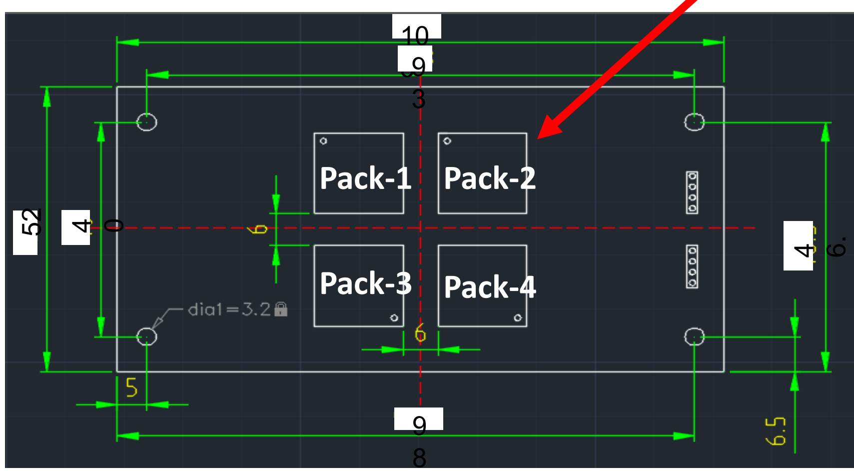


Solder balls

Package
(13.42mm x 13.42mm)



Daisy-chain on package solder balls (pads)



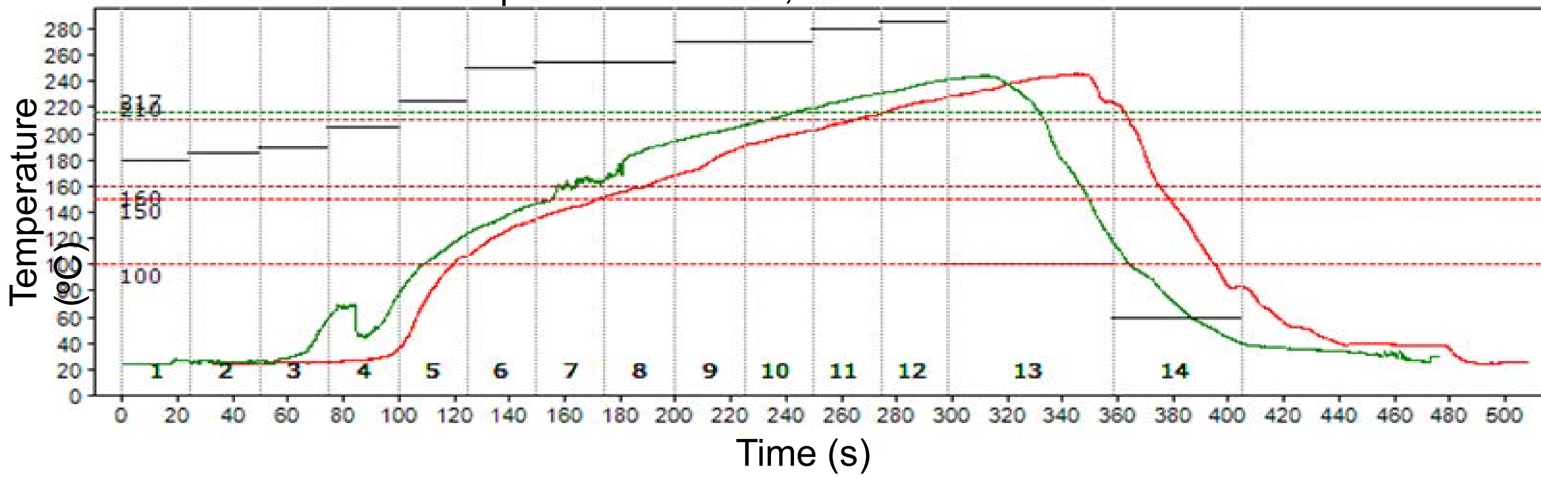
Thickness: 0.65mm
Material: FR-4
Size: 103mm x 52mm
Layer: 6
Pad finish: OSP

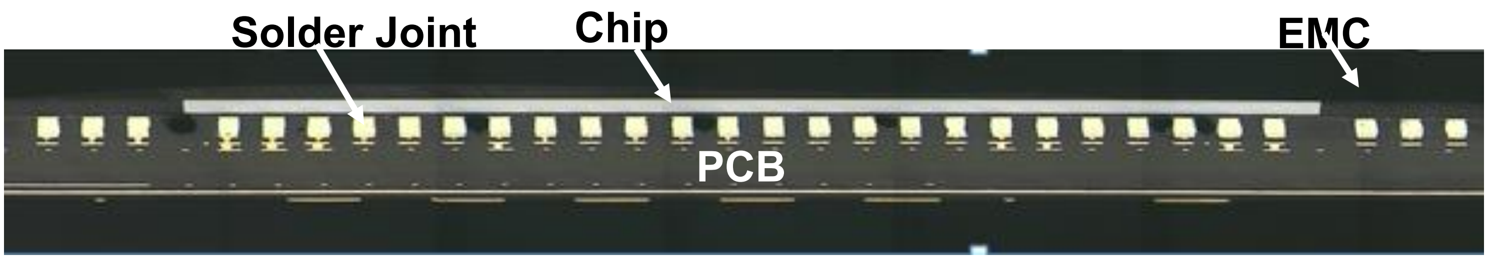
Units: mm

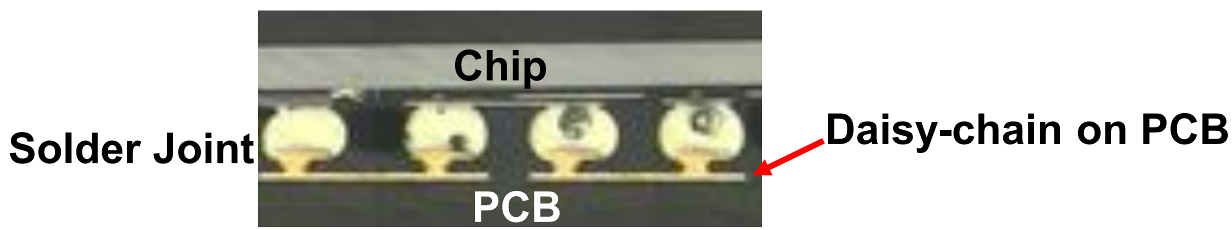
"Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

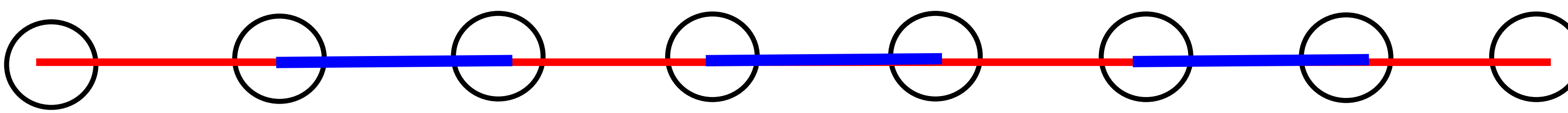
Reflow of the FOWLP on PCB with Daisy-Chains

Maximum temperature = 245°C; Time above 217°C = 85s







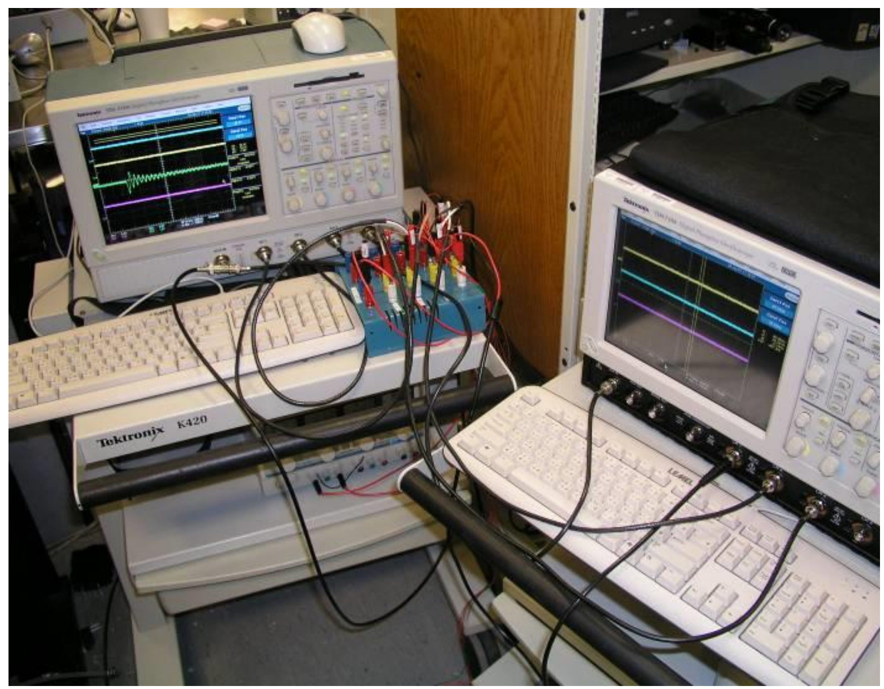


Daisy-chain on PCB pads **Daisy-chain on package pads**

"Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

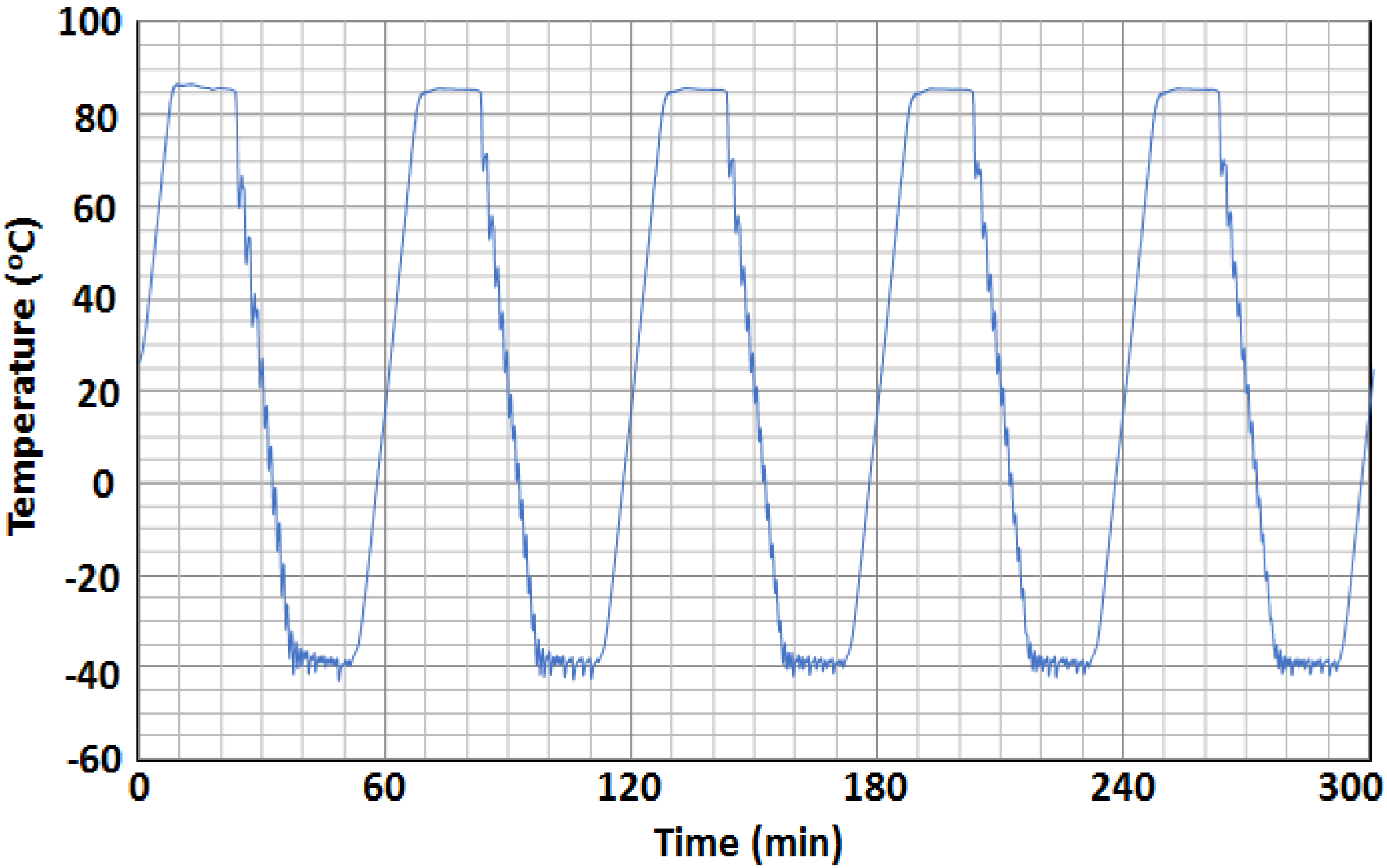
Thermal Cycling Chamber

Data Acquisition System



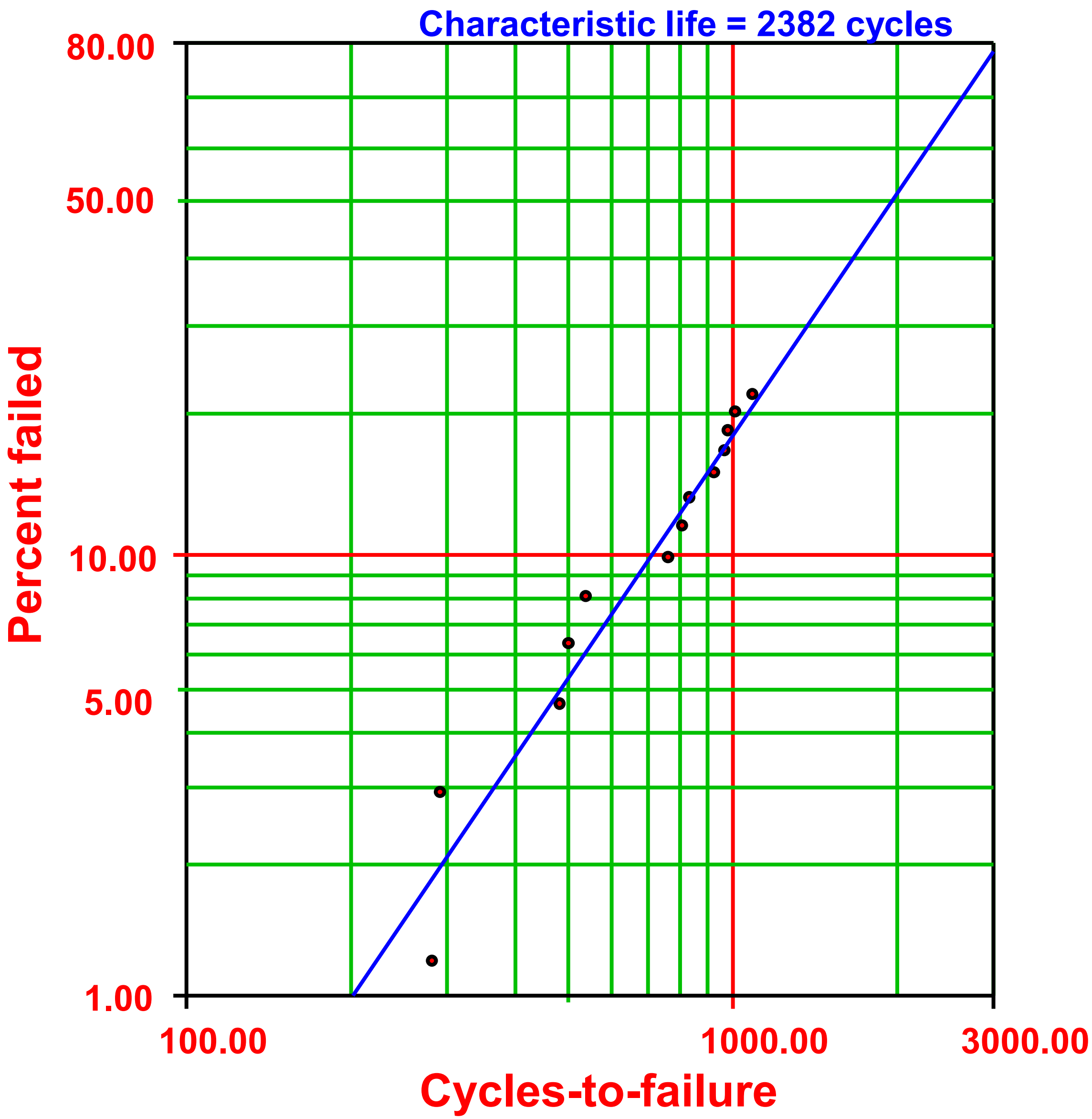
“Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging”, *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

Thermal Cycling Temperature Profile



“Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging”, *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

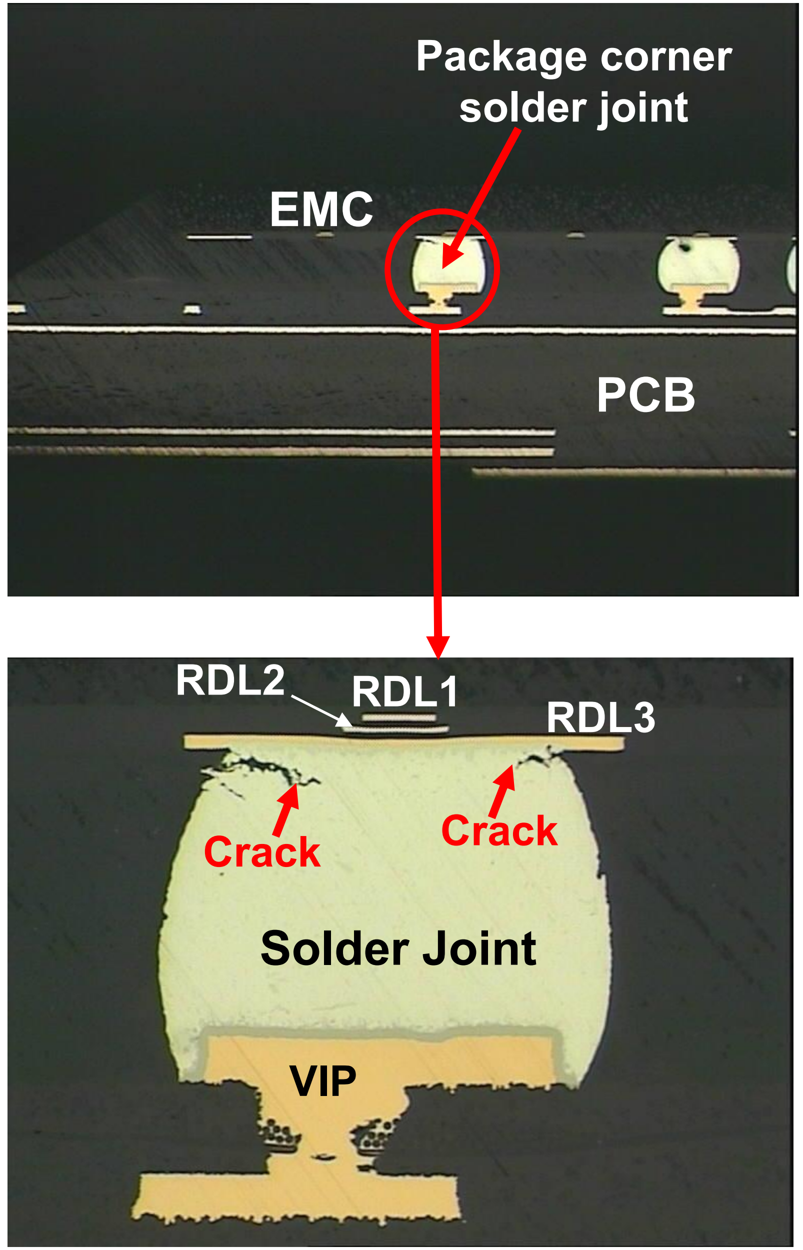
Weibull Plot of the FOWLP Lead-Free Solder Joints



“Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging”, *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

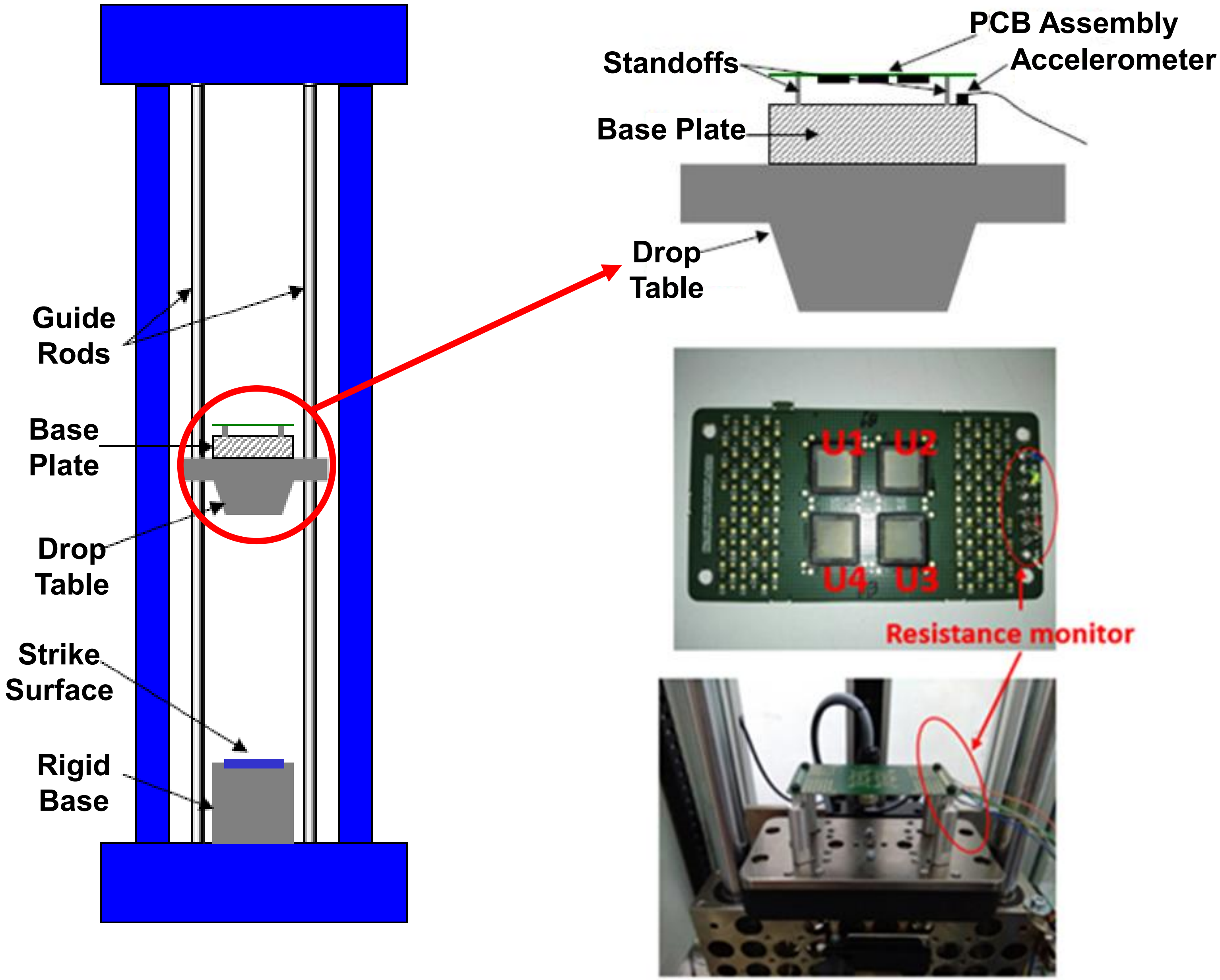
Failure Location

Failure Mode



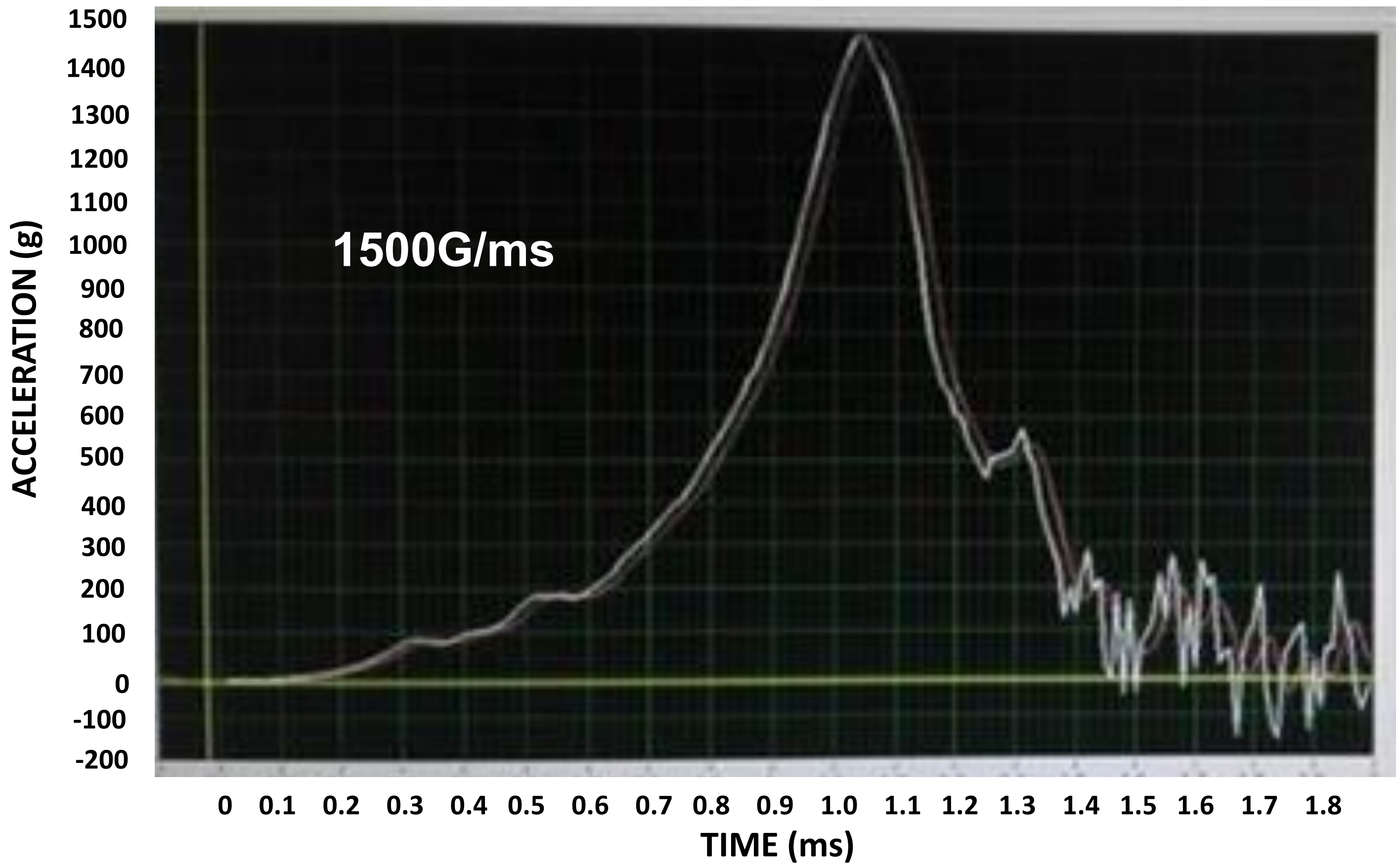
"Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

Drop Test Setup



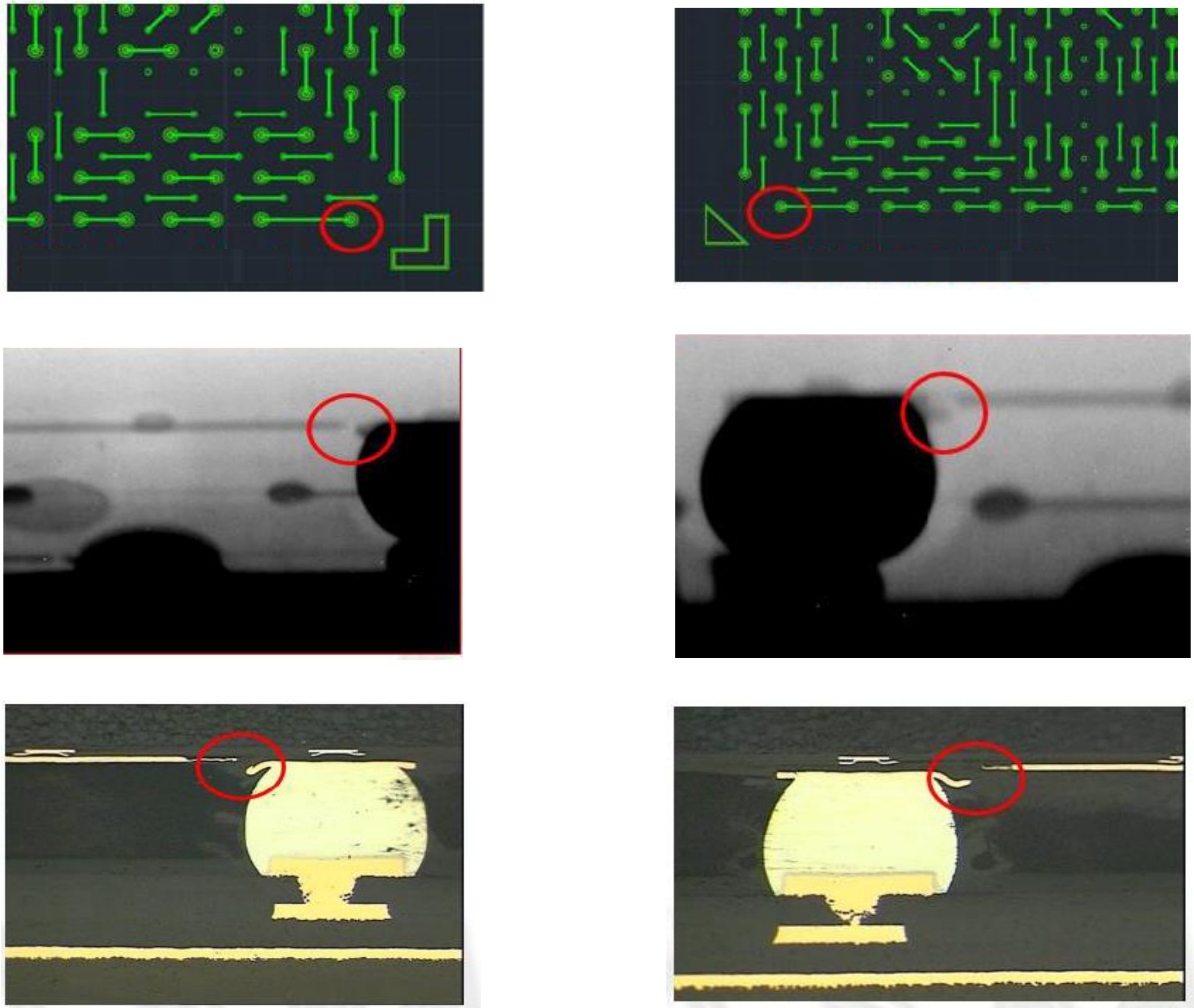
"Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

Drop Test Spectrum



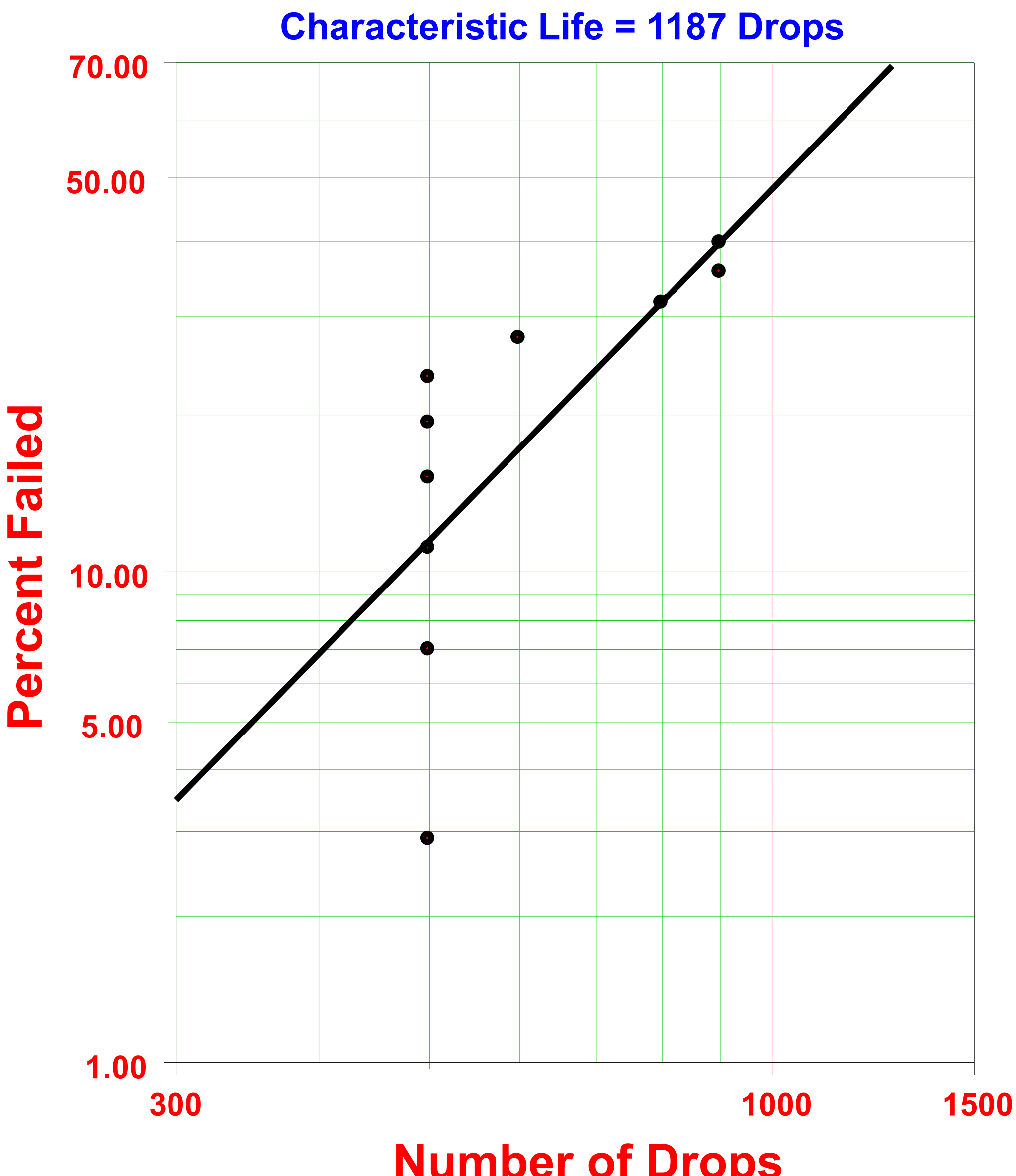
"Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

Drop Test Failure Locations of the FOWLP PCB Assembly without Underfill



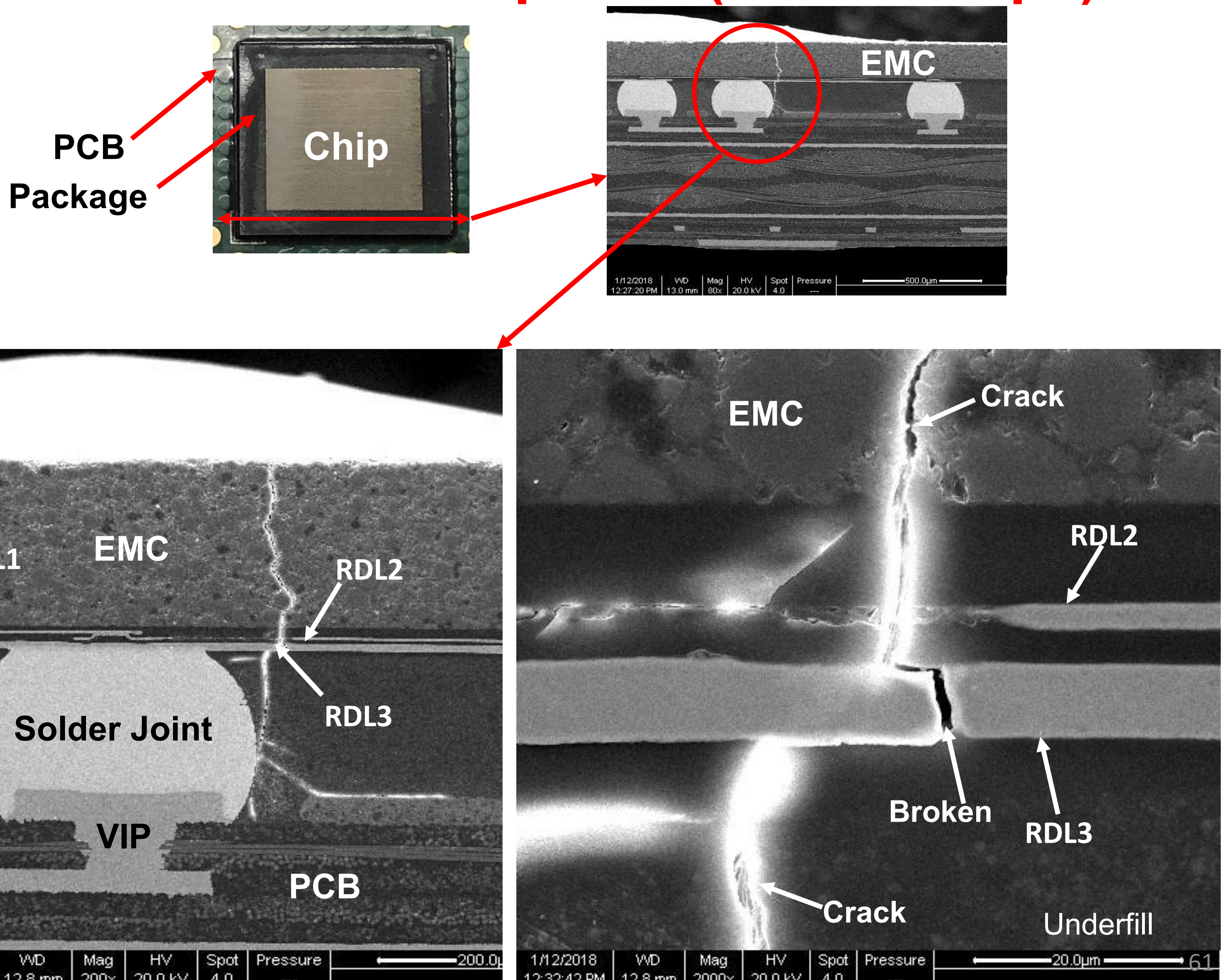
“Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging”, *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

Drop Test Weibull Plot of the FOWLP PCB Assembly with Underfill



"Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

Failure Mode of the FOWLP PCB Assembly with Underfill under Drop Test (at 550 drops)

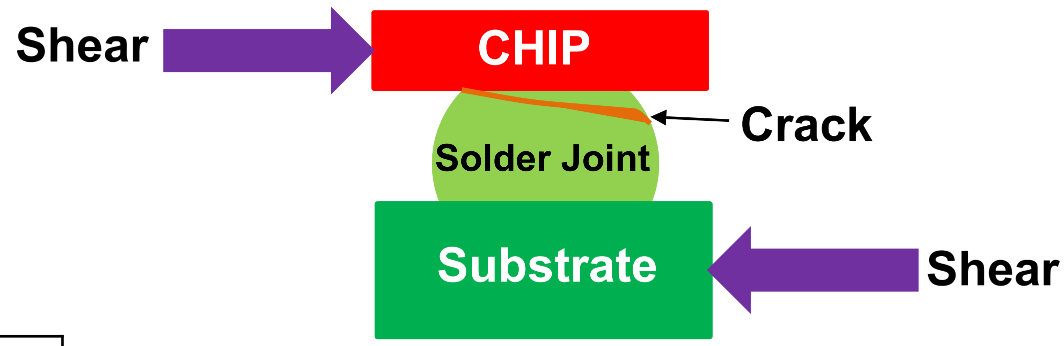


"Design, Materials, Process, and Fabrication of Fan-Out Wafer-Level Packaging", *IEEE Transactions on CPMT.* 2018, pp. 991-1002.

Reliability Data

Sample Mean and Sample Median

Shearing Test of Solder Joint



Sample number	Shearing Force (g) to Failure
1	9
2	8
3	7
4	9
5	6
6	8
7	8
8	5
9	6
10	7

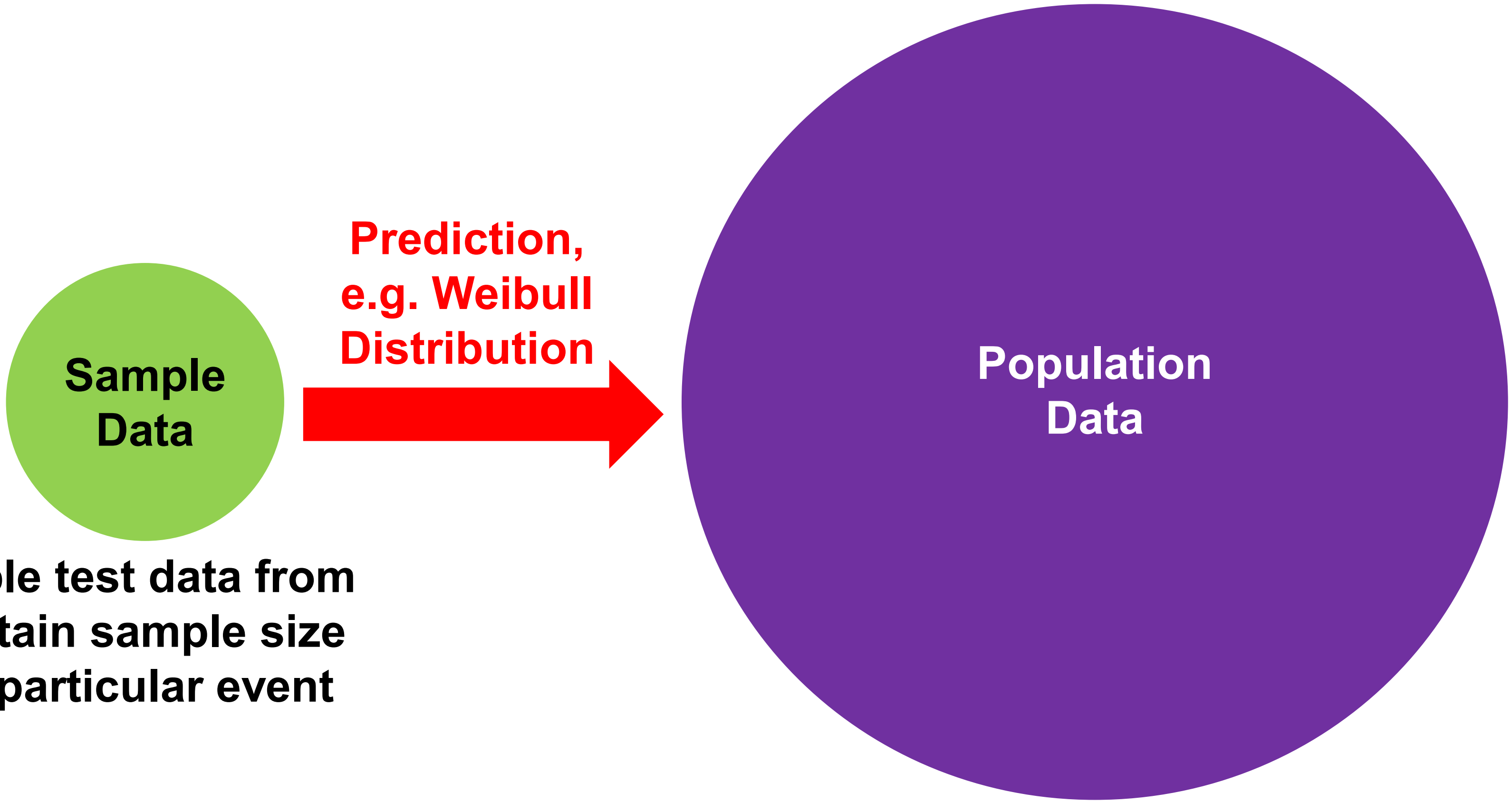
Sample Mean (arithmetic average) = $\frac{\sum_{i=1}^{n} x_i}{n}$

= (9 + 8 + 7 + 9 + 6 + 8 + 8 + 5 + 6 + 7)/10 = 7.3g

Sample Median is the number in the middle when all the observations are ranked in their order of magnitude. For example the median of 2, 7, 11, 15, 18, 20, 21, is 15.

In our case, we first rearrange the observations in their order of magnitude, i.e., 5, 6, 6, 7, 7, 8, 8, 8, 9, 9
Then, the sample median is (7 + 8)/2 = 7.5g

Sample Data vs. Population Data

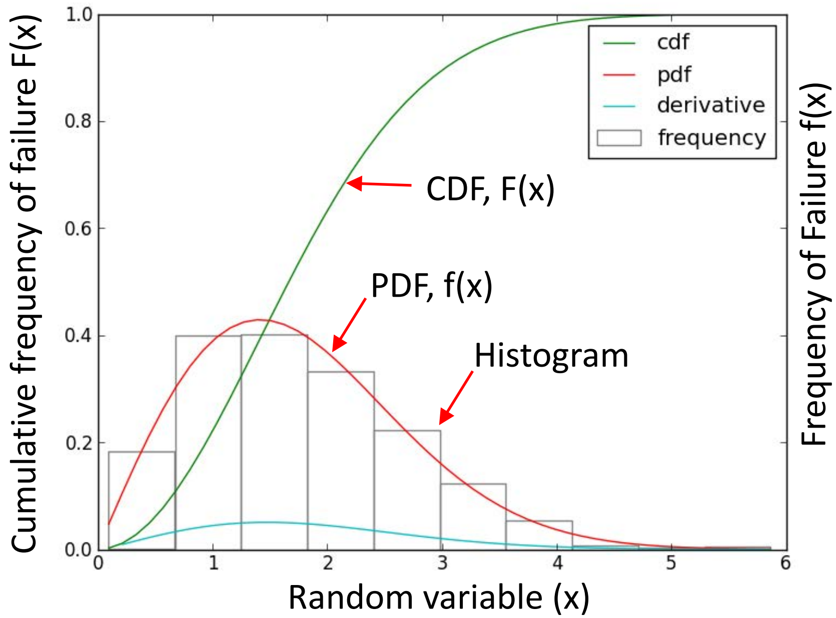


Sample test data from a certain sample size of a particular event

The whole population data of the particular event

Design for Reliability, Reliability Testing and Data Analysis, and Failure Analysis of Solder Joints, NEPCON West Workshops, Anaheim, CA, February 1990.

Reliability Data



PDF (probability density function), *f(x)*
When a large sample is available, the usual method of estimating population from the ample is to reduce the data into a frequency-histogram form.

CDF (cumulative distribution function), *F(x)*
However, in most engineering situations only a small sample is available. Therefore, the shape of the histogram varies considerably with change in class interval. Hence, for these situation a cumulative distribution plot is preferred. This involves plotting the observations on the abscissa against the rankings of these observations on the ordinate.

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Ranking

For any required ranking (*G*), the percent rank (*z*) can be determined by (*z* is the percent rank of the *j*th value in *n* samples):

$$1-(1-z)^n - nz(1-z)^{n-1} - \frac{n(n-1)}{2!}z^2(1-z)^{n-2} - \cdots$$
$$-\frac{n(n-1)\cdots(n-j+1)}{(j-1)!}z^{j-1}(1-z)^{n-j+1} = G$$

For example, given the sample size n = 10 and the required ranking G = 95%. The percent failure rank (z) is 25.89% for j = 1; 39.42% for j = 2; 50.69% for j = 3; 60.76% for j = 4; 69.65% for j = 5; 77.76% for j = 6; 85% for j = 7; 91.27% for j = 8; 96.32% for j = 9; and 99.49% for j = 10. The 95% failure rank of the lowest of ten measurements is 25.89%. This means that in 95% of the cases the lowest of ten would represent as much as 25.89% of the population. Only in 5% of cases would the lowest of ten represent even more than 25.89% of the population.

For median (or 50%) rank, G = 50%, then z can be approximated as

$$z = F(x) = (j - 0.3)/(n + 0.4)$$

where *j* = failure order number and *n* = sample size.

n = 5

Sample order (*j*)	Sample % Failures	Media Rank %
1	20	12.94
2	40	31.47
3	60	50.00
4	80	68.53
5	100	87.06

n = 10

Sample order (*j*)	Sample % Failures	Media Rank %
1	10	6.70
2	20	16.32
3	30	25.94
4	40	35.57
5	50	45.19
6	60	54.81
7	70	64.43
8	80	74.06
9	90	83.68
10	100	93.30

n = 50

Sample order (*j*)	Sample % Failures	Media Rank %
1	2.00	1.38
2	4.00	3.37
3	6.00	5.35
4	8.00	7.33
5	10.00	9.32
46	92.00	90.67
47	94.00	92.66
48	96.00	94.64
49	98.00	96.62
50	100.00	98.61

Median Rank = F(x) = (*j* - 0.3)/(*n* + 0.4)

n = Sample Size

j = Sample Order

STATISTICAL ANALYSIS OF RELIABILITY DATA – WEIBULL

Weibull PDF, CDF, Reliability, Failure Rate, and MTTF

- The three-parameter (γ, θ, β) Weibull probability density function (PDF) is:

$$f(x) = \frac{\beta}{\theta}\left(\frac{x-\gamma}{\theta}\right)^{\beta-1} \exp\left[-\left(\frac{x-\gamma}{\theta}\right)^{\beta}\right] \geq 0,\ x \geq \gamma,\ -\infty < \gamma > +\infty,\ \theta > 0,\ \beta > 0$$

where *x* is the random variable (e.g., life or cycles), γ is the expected minimum value of *x*, θ is the characteristic value, which could be used to represent the quality of a product, and β is the Weibull slope, which is a measure of the uniformity of a product.

- The Weibull cumulative distribution function (CDF) is:

$$F(x) = \int_{-\infty}^{x} f(t)dt = 1 - \exp\left[-\left(\frac{x-\gamma}{\theta}\right)^{\beta}\right]$$

- The Reliability function, *R(x)* is:

$$R(x) = 1 - F(x) = \exp\left[-\left(\frac{x-\gamma}{\theta}\right)^{\beta}\right]$$

- The failure rate, *h(x)* is:

$$h(x) = \frac{f(x)}{R(x)} = \frac{\beta}{\theta}\left(\frac{x-\gamma}{\theta}\right)^{\beta-1}$$

- The expected value, *E(x)*, or mean-time-to-failure, *MTTF* (or mean life) is:

$$E(x) = MTTF = \int_{0}^{\infty} x f(x)dx = \gamma + \theta\Gamma\left(1 + \frac{1}{\beta}\right)$$

Weibull Parameters Estimation

The CDF can be rewritten as follow

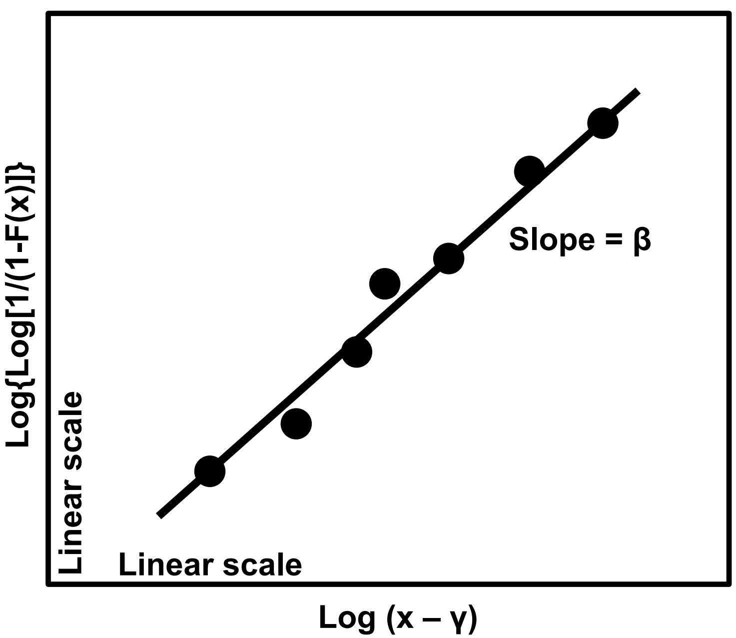
$$\ln\left\{\ln\left[\frac{1}{1-F(x)}\right]\right\} = \beta\ln(x-\gamma) - \beta ln\theta$$

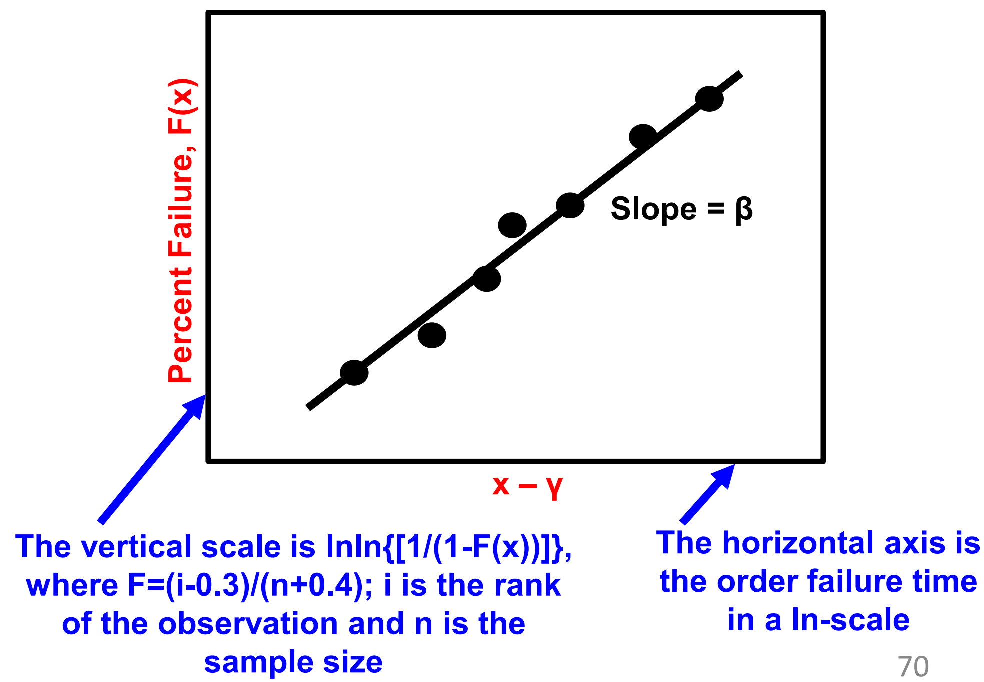
or

$$Y = aX + b \qquad \textbf{(\#)}$$

where $Y = \ln\left\{\ln\left[\frac{1}{1-F(x)}\right]\right\},\ X = \ln(x-\gamma),\quad a = \beta,\quad b = -\beta ln\theta = C$

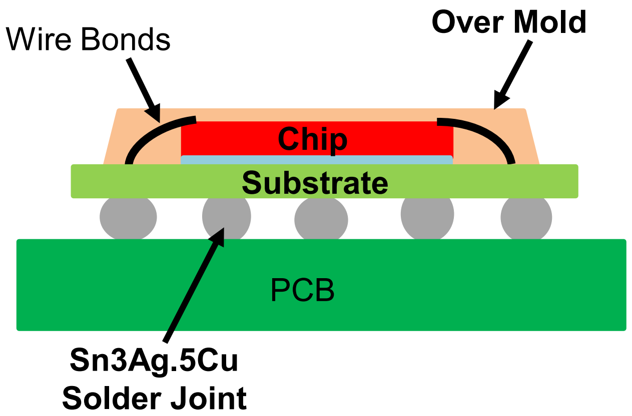
Equation (#) represents a straight line with a slope, *a* (or *β*), and intercept (*b or C*) on the Cartesian X-Y coordinates. Hence, a plot of lnln{[1/(1 - *F(x)*)]} against ln*(x-γ)* will also be a straight line with a slope, *a* (or *β*). A Weibull probability paper with the vertical scale as lnln{[1/(1 - *F(x)*)]} and the horizontal axis as ln-scale, can expedite the conversion.

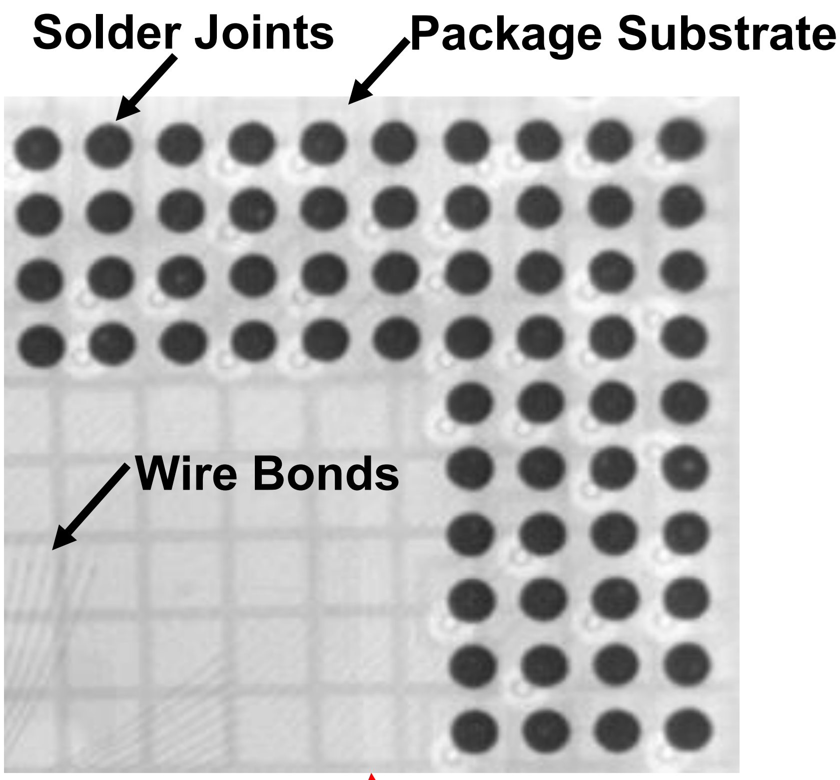




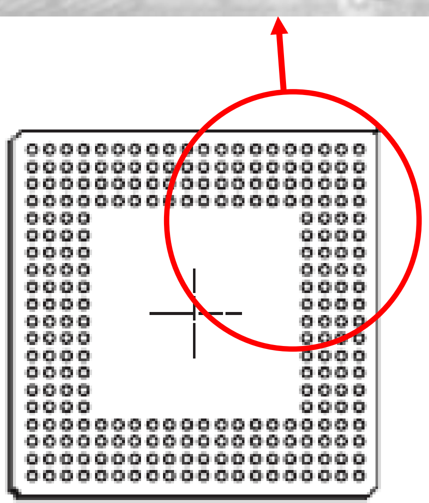
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

256-Pin Plastic Ball Grid Array (PBGA) PCB Assembly





- The sample size is 20.
- The test condition is:
  -25 ⇆ 125^{o}C, one cycle per hour, 15 minutes ramp time and 15 minutes dwell time.
- The failure criterion is a 50% increase in resistance.



Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

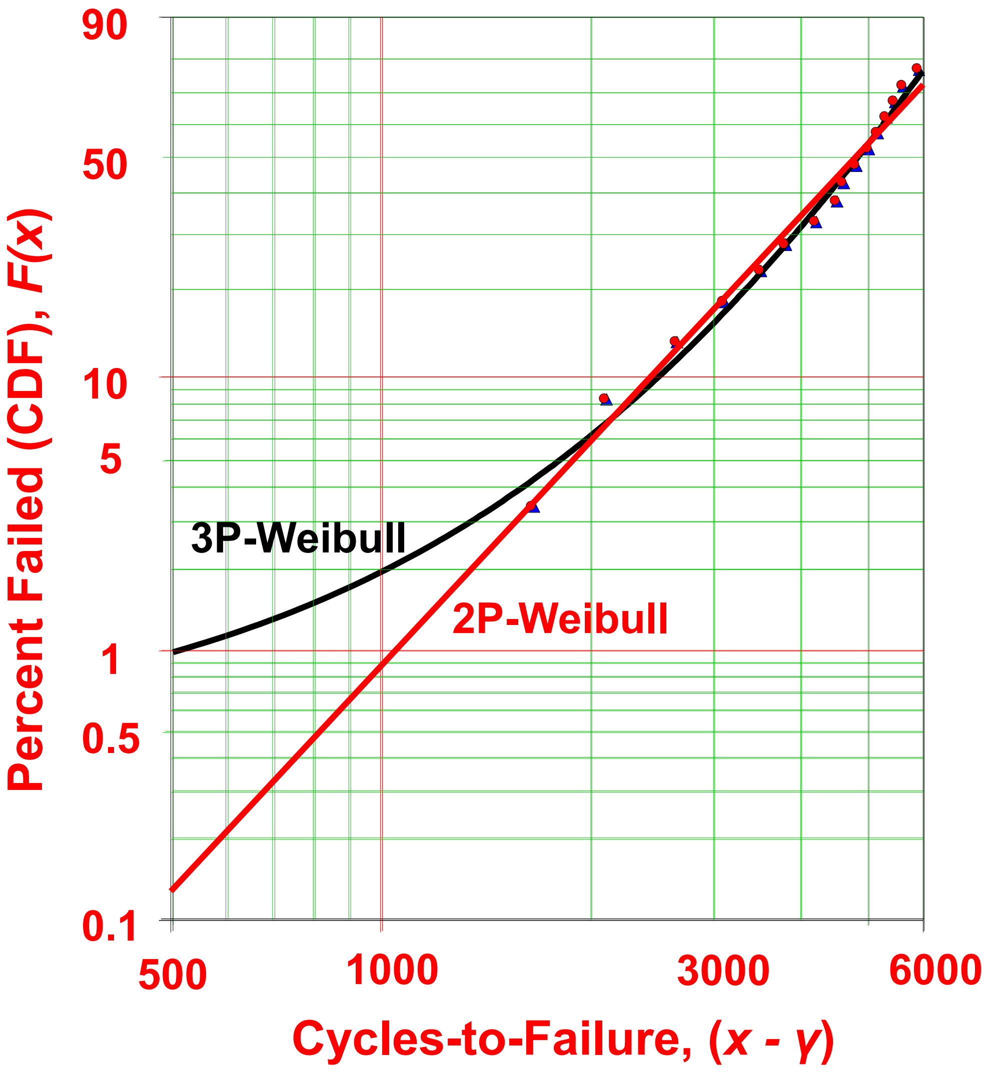
Test Data (Sample Size = 20)

Failure Order (*j*)	Cycles-to-Failure (*x*)	*F*(*x*) Median Rank	*F*(*x*) 5% Rank	*F*(*x*) 95% Rank
1	1650	3.4	0.3	13.9
2	2100	8.3	1.8	21.8
3	2650	13.2	4.3	28.6
4	3100	18.1	7.3	34.8
5	3500	23.0	10.5	40.4
6	3800	27.9	14.0	45.6
7	4200	32.8	17.9	50.7
8	4500	37.7	21.8	56.7
9	4600	42.6	25.9	60.4
10	4800	47.5	30.3	65.3
11	5000	52.5	34.7	69.7
12	5150	57.4	39.6	74.1
13	5300	62.3	44.3	78.1
14	5450	67.2	49.3	82.2
15	5600	72.1	54.4	86.0
16	5900	77.0	59.6	89.5

Median Rank = $(j - 0.3)/(n + 0.4)$; $n = 20$

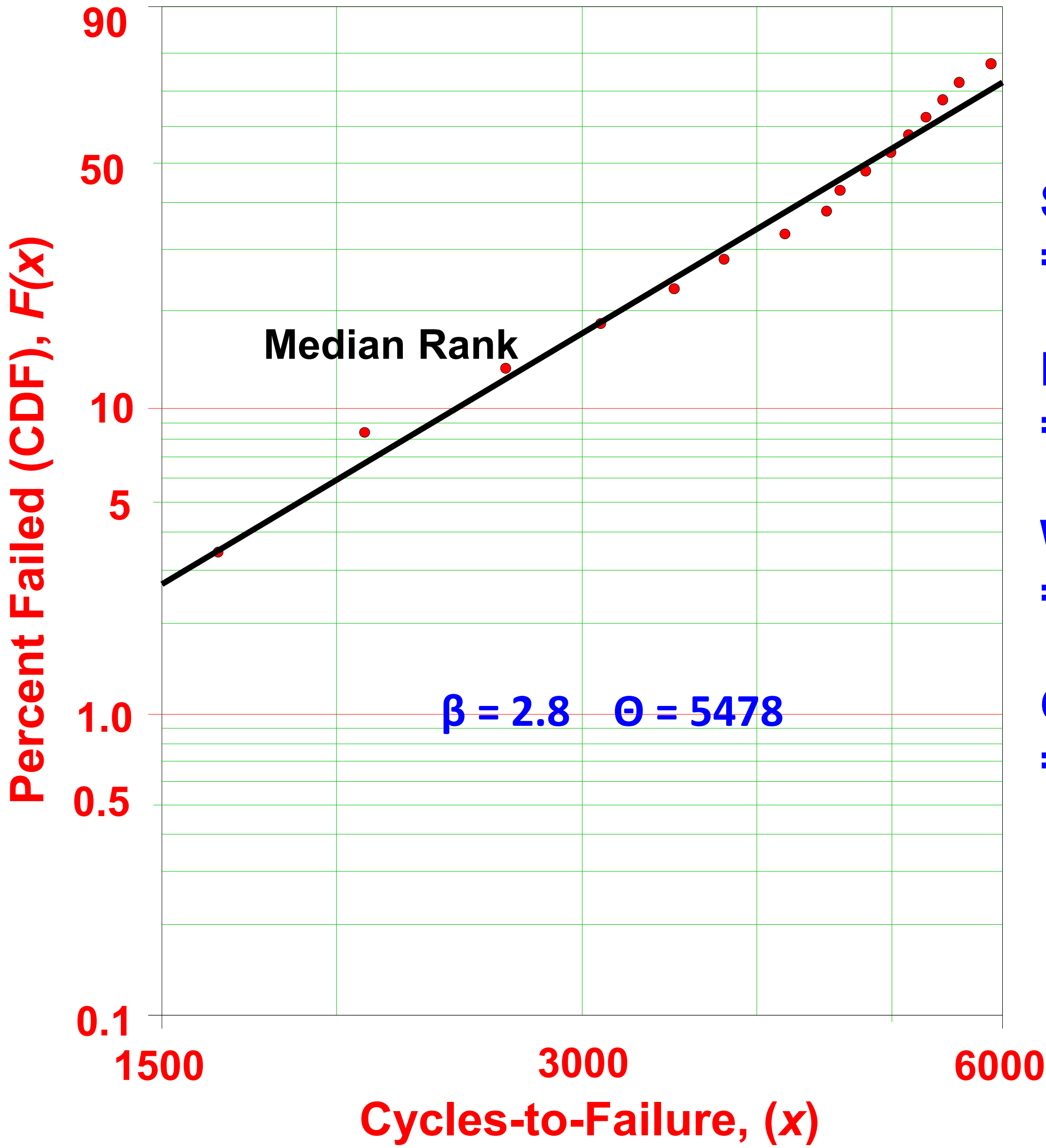
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

2-Parameter and 3-Parameter Weibull Plots



Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Weibull Plot of the 256-Pin Plastic Ball Grid Array (PBGA) PCB Assembly



Sample Size = 20

Number of Failures = 16

Weibull Slope = 2.8

Characteristic Life = 5478 cycles

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

As soon as we'd run the Reliability test, we can answer the following questions

- **What is the probability that the 256-pin lead-free PBGA will fail by 1500 cycles?**

$F(1500) = 1 - \exp[-(1500/5478)^{2.8}] = 0.026$, i.e., 2.6% of the lead-free PBGA will fail at 1500 cycles.

- **If we use 1000 units of them, how many do we expect to fail in the first 1500 cycles?**

We will expect $1000 \times 0.026 = 26$ lead-free PBGAs will fail in the first 1500 cycles.

- **What is the probability that the 256-pin PBGA lead-free solder joints will survive 1200 cycles?**

$R(1200) = \exp[-(1200/5478)^{2.8}] = 0.9859$, i.e., 98.59% of the lead-free PBGA will survive at 1200 cycles.

- **What is the failure rate of the 256-pin lead-free PBGA at 1500 cycles?**

$h(1500) = (2.8/5478)(1500/5478)^{1.8} = 49{,}657 \times 10^{-9}$ per cycle = 49,657 FITs (ppm/k)

- **What is the MTTF of the 256-pin lead-free PBGA?**

$MTTF = 5478 \times \Gamma(1 + 1/2.8) = 5478 \times \Gamma(1.357) = 5478 \times 0.89 = 4875$ cycles.

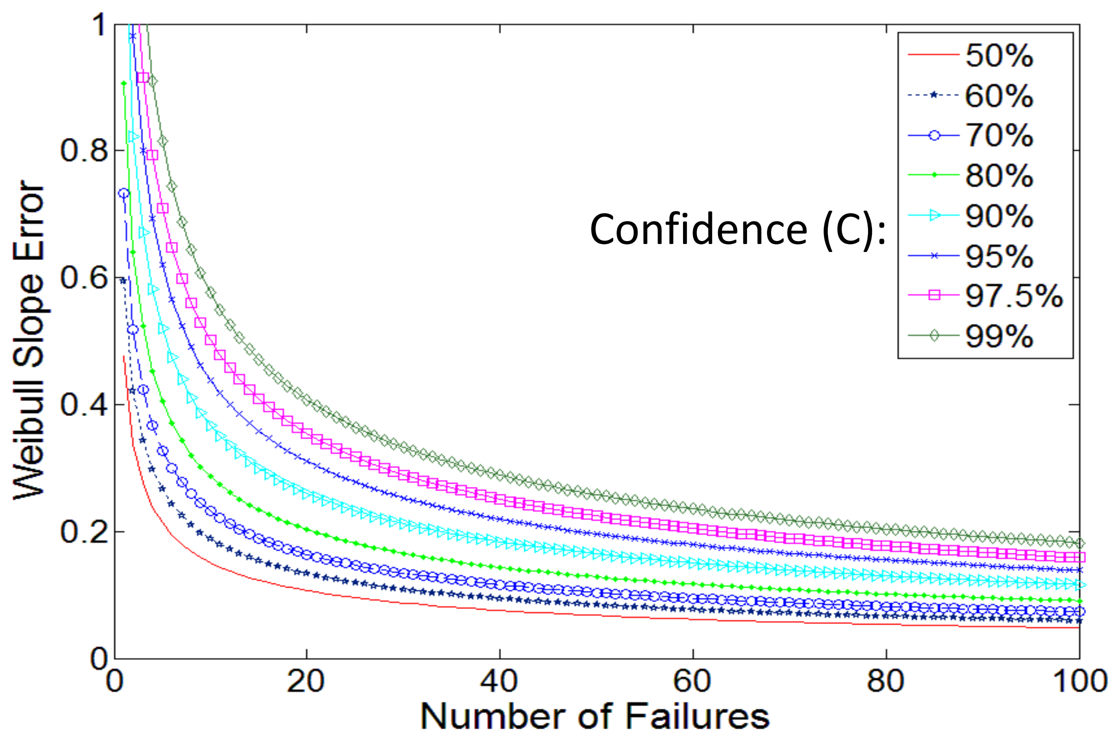
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

- **Reliability applies to the product!**
- **Confidence applies to the test itself!**
- **Confidence is defined as the probability that a given interval determined from the test data will contain the population parameters, such as (using Weibull as an example) the mean/characteristic life and Weibull slope.**

Weibull Slope Error (True Weibull Slope)

To predict the true Weibull slope (β_t) of the population, it is necessary to estimate the Weibull slope error in relation to the sample size (n) and the required confidence level (C). The error (*E*) in the Weibull slope depends on the number of failures (*N*) and *C*, which can be searched from the following equation:

$$\frac{1}{\sqrt{\pi}}\int_{-\infty}^{E\sqrt{2N}} e^{-\frac{t^2}{2}}\,dt = \frac{1+C}{2} \qquad (10)$$



Thus, for a given *C* (the confidence level) and *N* (the number of failures), the *E* (error) can be searched from the above equation or chart.

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Weibull Slope Error (True Weibull Slope)

For example, for a given confidence *C* = 0.9 (that means in 90 out of 100 cases) the Weibull slop error of the example (256-PBGA SnAgCu solder joints) (with *N* = 16 failures) is (by the chart) $\varepsilon = 0.3$.

Thus, the true Weibull slope β_t of the 256-PBGA SnAgCu solder joints will be happened in the intervals of

$$(2.8 - 0.3 \times 2.8) \leq \beta_t \leq (2.8 + 0.3 \times 2.8) \text{ or } 1.96 \leq \beta_t \leq 3.64$$

True Characteristic Life

For a given *C* (the confidence level), in order to predict the population (true) mean (μ) or population (true) characteristic value (θ_t) from the sample test data, it is necessary to determine the CDFs (life distributions) with certain percent ranks for the required confidence interval.

The lower percent ranks and upper percent ranks for *C* = 95% are respectively 2.5% and 97.5%; for *C* = 90% are 5% and 95%; for *C* = 80% are 10% and 90%; for *C* = 70% are 15% and 85%; and for *C* = 60% are 20% and 80%.

Required Confidence Level (%)	Lower percent rank	Upper percent rank
95	2.5	97.5
90	5	95
80	10	90
70	15	85
60	20	80

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Test Data (Sample Size = 20)

Failure Order (*j*)	Cycles-to-Failure (*x*)	*F*(*x*) Median Rank	*F*(*x*) 5% Rank	*F*(*x*) 95% Rank
1	1650	3.4	0.3	13.9
2	2100	8.3	1.8	21.8
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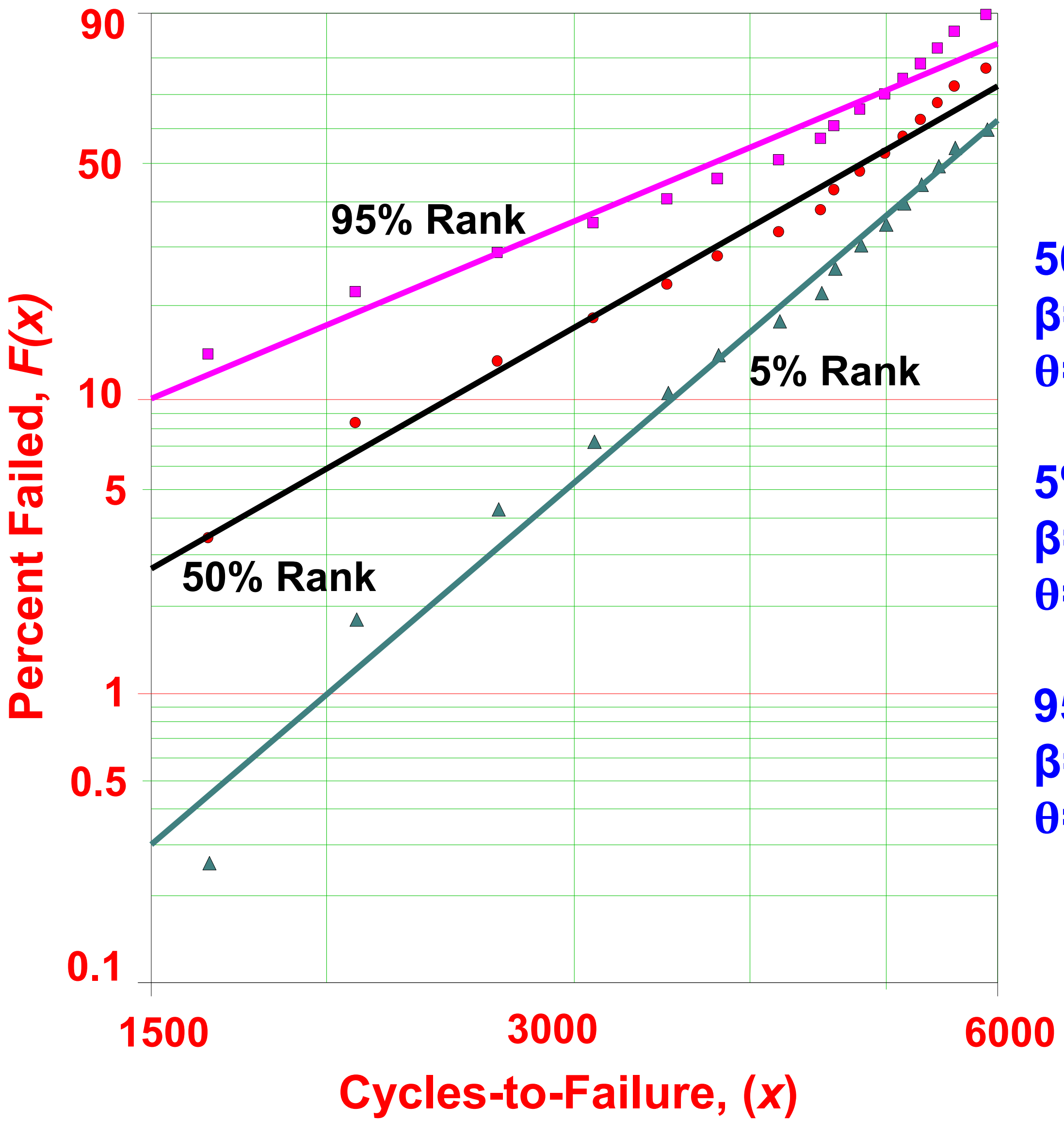
4	3100	18.1	7.3	34.8
5	3500	23.0	10.5	40.4
6	3800	27.9	14.0	45.6
7	4200	32.8	17.9	50.7
8	4500	37.7	21.8	56.7
9	4600	42.6	25.9	60.4
10	4800	47.5	30.3	65.3
11	5000	52.5	34.7	69.7
12	5150	57.4	39.6	74.1
13	5300	62.3	44.3	78.1
14	5450	67.2	49.3	82.2
15	5600	72.1	54.4	86.0
16	5900	77.0	59.6	89.5

Median Rank = $(j - 0.3)/(n + 0.4)$; $n = 20$

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Weibull Plot of the 256-Pin Plastic Ball Grid Array (PBGA) PCB Assembly at 90% Confidence



50% Rank
β= 2.8
θ= 5478 cycles

5% Rank
β= 4.2
θ= 6029 cycles

95% Rank
β= 2.1
θ= 4493 cycles

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Weibull PDF, CDF, Reliability, Failure Rate, and MTTF

- The three-parameter (γ, θ, β) Weibull probability density function (PDF) is:

$$f(x) = \frac{\beta}{\theta}\left(\frac{x-\gamma}{\theta}\right)^{\beta-1} \exp\left[-\left(\frac{x-\gamma}{\theta}\right)^{\beta}\right] \geq 0,\ x \geq \gamma,\ -\infty < \gamma > +\infty,\ \theta > 0,\ \beta > 0$$

where *x* is the random variable (e.g., life or cycles), γ is the expected minimum value of *x*, θ is the characteristic value, which could be used to represent the quality of a product, and β is the Weibull slope, which is a measure of the uniformity of a product.

- The Weibull cumulative distribution function (CDF) is:

$$F(x) = \int_{-\infty}^{x} f(t)dt = 1 - \exp\left[-\left(\frac{x-\gamma}{\theta}\right)^{\beta}\right] \quad (*)$$

- The Reliability function, *R(x)* is:

$$R(x) = 1 - F(x) = \exp\left[-\left(\frac{x-\gamma}{\theta}\right)^{\beta}\right]$$

- The failure rate, *h(x)* is:

$$h(x) = \frac{f(x)}{R(x)} = \frac{\beta}{\theta}\left(\frac{x-\gamma}{\theta}\right)^{\beta-1}$$

- The expected value, *E(x)*, or mean-time-to-failure, *MTTF* (or mean life) is:

$$E(x) = MTTF = \int_{0}^{\infty} x f(x)dx = \gamma + \theta\Gamma\left(1 + \frac{1}{\beta}\right) \quad (\$)$$

True Mean Life

The mean life i.e., *MTTF* from test samples can be determine by Equation ($) with θ = 5478 and β = 2.8, and is equal to [*MTTF* = 5478Γ(1+1/2.8) = 5478Γ(1.357) = 5478 x 0.89 = 4875 cycles], which occurs at 51.4% failed [by Equation (*) with x = 4875, θ = 5478 and β = 2.8]. The true mean life, μ, of the 265-pin PBGA SnAgCu solder joints will happen within the intervals 3846 ≤ μ ≤ 5578 cycles. The values of the intervals have been determined by rewriting Equation (*) and with the following forms

$$x = \theta[-\ln(1 - F(x))]^{\frac{1}{\beta}}$$

$$\mu_{lower} = \theta_{95\%\ Rank}[-\ln(1 - 0.514)]^{1/\beta_{95\%\ Rank}} = 4493[0.72]^{1/2.1} = 3846 \text{ cycles}$$

$$\mu_{upper} = \theta_{5\%\ Rank}[-\ln(1 - 0.514)]^{1/\beta_{5\%\ Rank}} = 6029[0.72]^{1/4.2} = 5578 \text{ cycles}$$

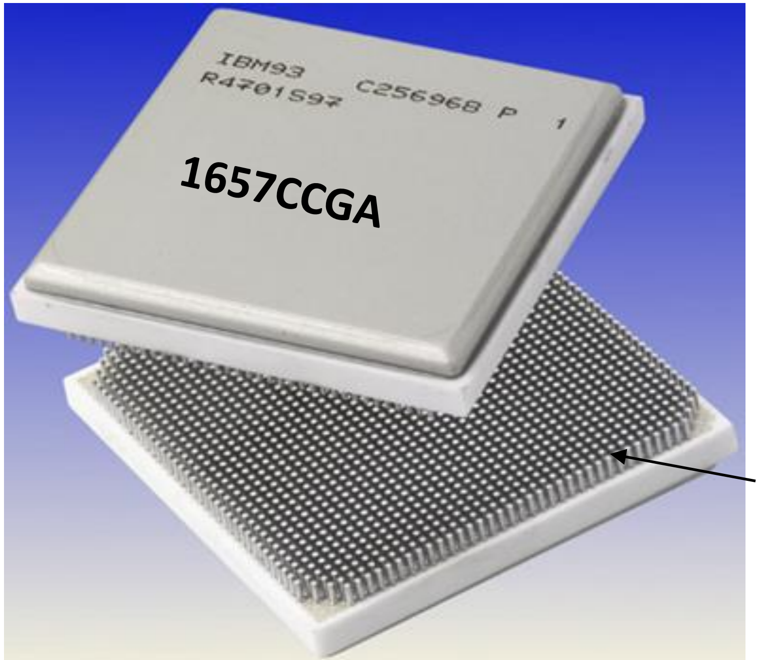
where $\theta_{5\%\ rank}$ = 6029, $\beta_{5\%\ rank}$ = 4.2 and $\theta_{95\%\ rank}$ = 4493, $\beta_{95\%\ rank}$ = 2.1 have been substituted.

Reliability of 256-Pin Plastic Ball Grid Array (PBGA) PCB Assembly

Characteristic Life (θ), cycle	Median rank	5478
	True θ at 90% confidence	4493 ≤ θ ≤ 6029
Weibull Slope (β)	Median rank	2.8
	β error (%) at 90% confidence	37
	True β at 90% confidence	1.96 ≤ β ≤ 3.64
Mean Life (μ), cycle	Median rank	4875
	Percent failed at mean	51.4
	True μ at 90% confidence	3846 ≤ μ ≤ 5578

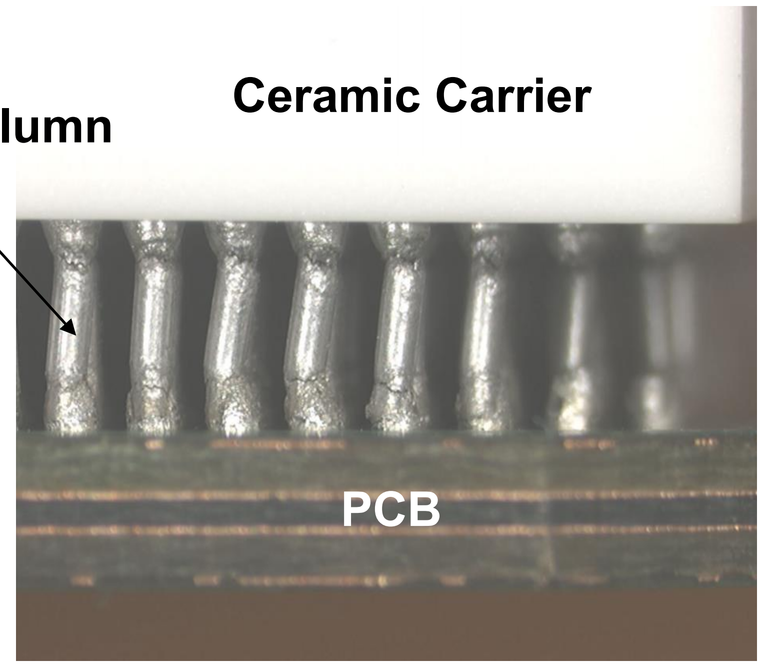
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

PCBs with HASL CuSn, ENIG NiAu, and Entek OSP (1657CCGA)



CCGA (Ceramic column grid array)

Solder Column

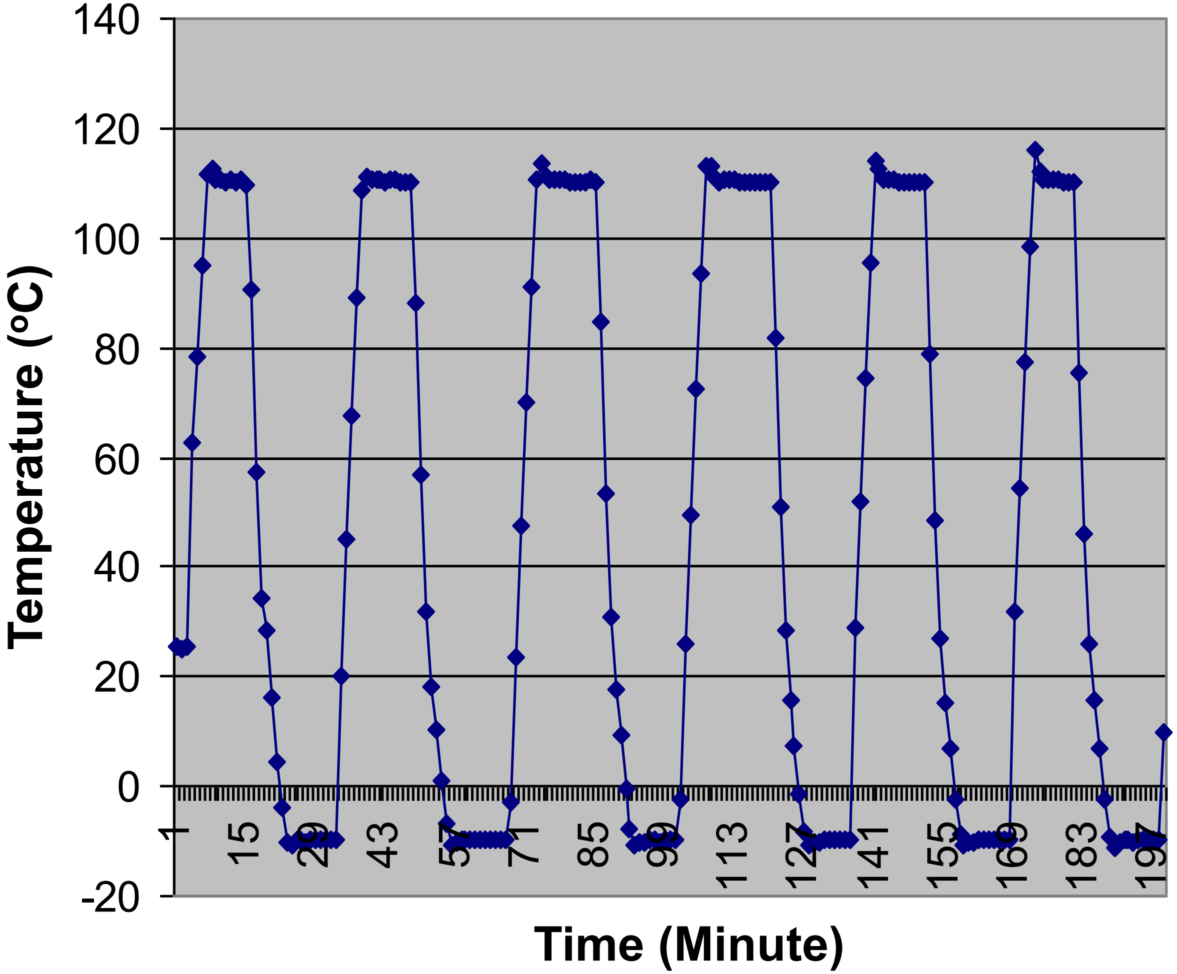


PCB with 3 different surface conditions:

- HASL (hot-air solder leveling)
- ENIG (electroless Ni and immersion)
- OSP (organic solderability preservative)

Lau, J. H., and W. Dauksher, "Reliability of an 1657CCGA (Ceramic Column Grid Array) Package with 96.5Sn3.9Ag0.6Cu Lead-Free Solder Paste on PCBs (Printed Circuit Boards), *ASME Transactions, Journal of Electronic Packaging*, Vol. 127, June 2005, pp. 96-105.

Thermal Cycling Condition: -10 ⇆ 110°C and 40-minute Cycle



Lau, J. H., N. Hoo, R. Horsley, J. Smetana, D. Shangguan, W. Dauksher, D. Love, I. Menis, and B. Sullivan, "Reliability Testing and Data Analysis of Lead-Free Solder Joints for High-Density Packages'", *Journal of Soldering & Surface Mount Technology*, Vol. 16, No. 2, 2004, pp. 46-68.

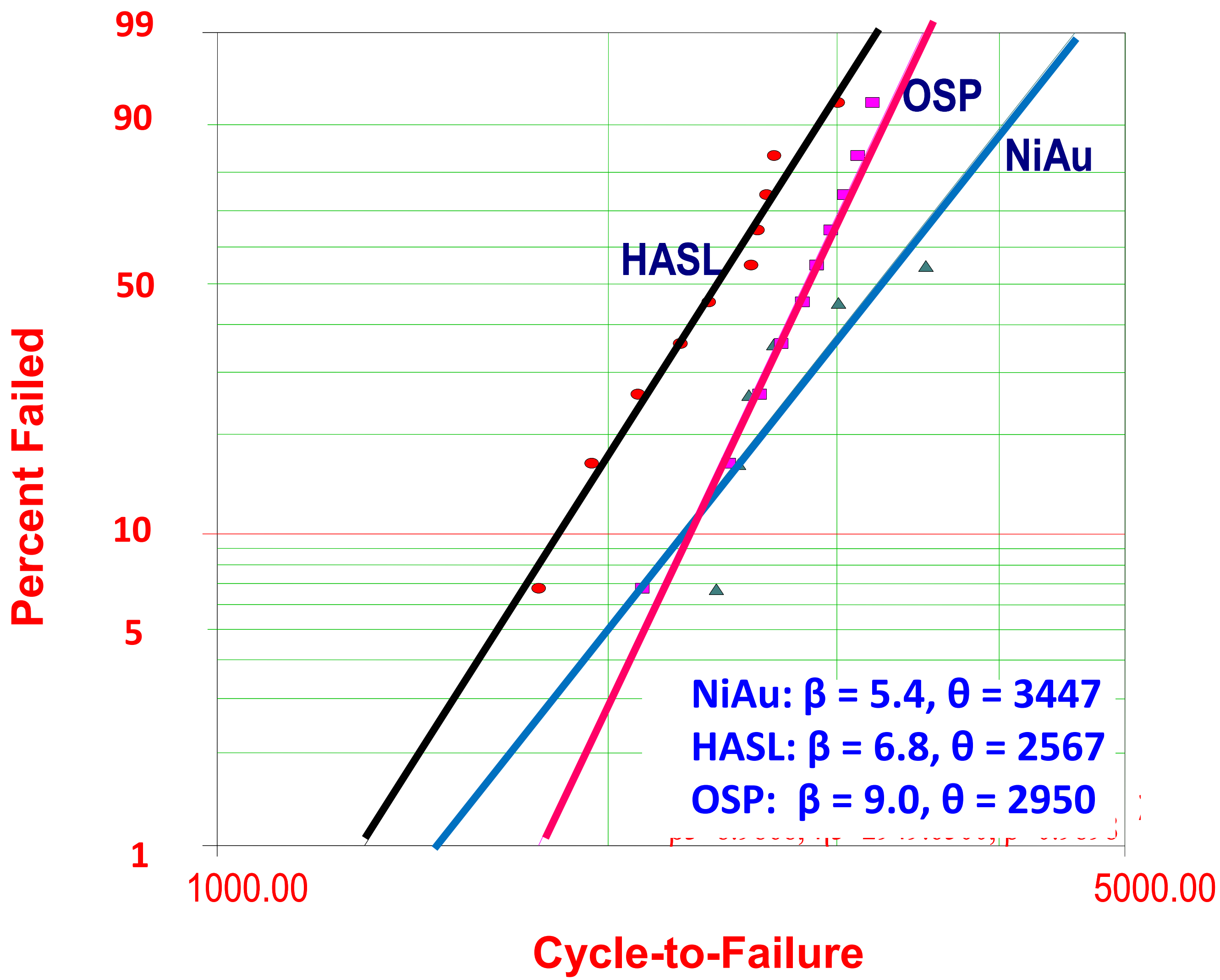
Test Data of PCBs with HASL CuSn, ENIG NiAu, and Entek OSP (1657CCGA)

Failure Order (*j*)	SnCu HASL PCB	ENIG (NiAu) PCB	OSP (Entek) PCB	Median (50%) Rank	5% Rank	95% Rank
1	1771	2423	2128	6.7	0.5	25.9
2	1945	2521	2480	16.3	3.7	39.4
3	2111	2568	2620	25.9	8.7	50.7
4	2276	2682	2722	35.6	15.0	60.8
5	2394	3009	2826	45.1	22.2	69.7
6	2581	3513	2899	54.8	30.4	77.8
7	2611		2972	64.4	39.3	85.0
8	2652		3045	74.0	49.3	91.3
9	2688		3118	83.7	60.6	96.3
10	3009		3200	93.3	74.1	99.5

Median Rank = $(j - 0.3)/(n + 0.4)$; $n = 10$

Lau, J. H., N. Hoo, R. Horsley, J. Smetana, D. Shangguan, W. Dauksher, D. Love, I. Menis, and B. Sullivan, "Reliability Testing and Data Analysis of Lead-Free Solder Joints for High-Density Packages'", *Journal of Soldering & Surface Mount Technology*, Vol. 16, No. 2, 2004, pp. 46-68.

Weibull Plots of 1567 CCGA PCB Assemblies with various Surface Finishing



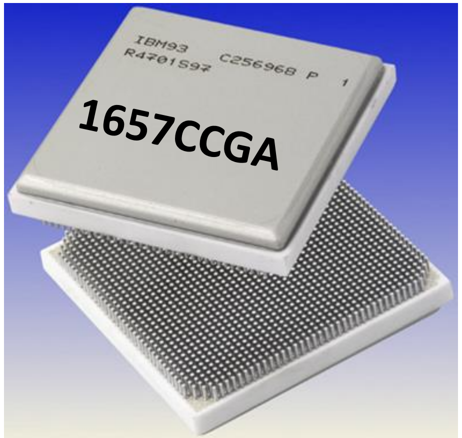
Lau, J. H., N. Hoo, R. Horsley, J. Smetana, D. Shangguan, W. Dauksher, D. Love, I. Menis, and B. Sullivan, "Reliability Testing and Data Analysis of Lead-Free Solder Joints for High-Density Packages'", *Journal of Soldering & Surface Mount Technology*, Vol. 16, No. 2, 2004, pp. 46-68.

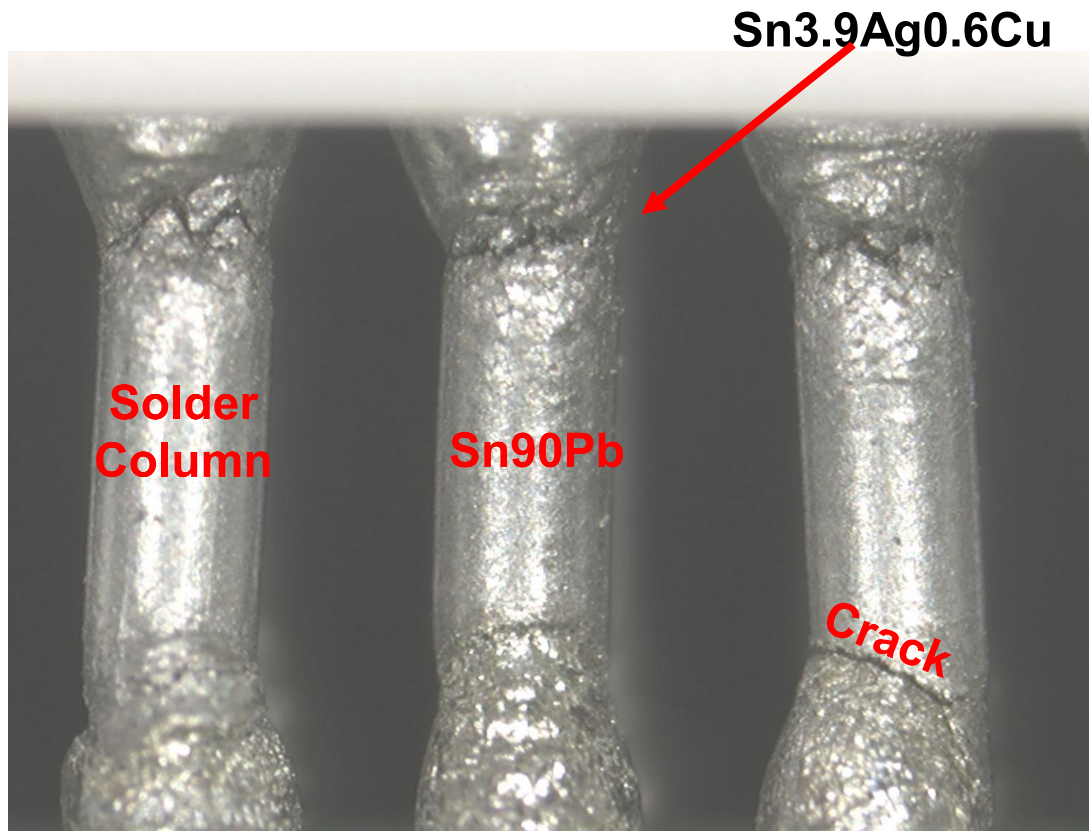
Reliability of PCBs with HASL CuSn, ENIG NiAu, and Entek OSP (1657CCGA) at 90% Confidence

		SnAgCu paste on SnCu PCB	SnAgCu paste on NiAu PCB	SnAgCu paste on OSP PCB
Characteristic Life (θ), cycle	Sample	2567	3447	2950
	True θ at 90% confidence	2259 ≤ θ ≤ 2786	2984 ≤ θ ≤ 3673	2677 ≤ θ ≤ 3127
Weibull Slope (β)	Sample	6.8	5.4	9.0
	β error (%) at 90% confidence	37	47	37
	True β at 90% confidence	4.25 ≤ β ≤ 9.25	2.86 ≤ β ≤ 7.92	5.66 ≤ β ≤ 12.32
Mean Life (μ), cycle	sample	2397	3197	2793
	Percent failed at mean	46.72	47.61	45.75
	Population μ at 90% confidence	2069 ≤ μ ≤ 2552	2655 ≤ μ ≤ 3497	2492 ≤ μ ≤ 3017

Lau, J. H., N. Hoo, R. Horsley, J. Smetana, D. Shangguan, W. Dauksher, D. Love, I. Menis, and B. Sullivan, "Reliability Testing and Data Analysis of Lead-Free Solder Joints for High-Density Packages'", *Journal of Soldering & Surface Mount Technology*, Vol. 16, No. 2, 2004, pp. 46-68.

PCBs with HASL CuSn, ENIG NiAu, and Entek OSP (1657CCGA)





- The failure locations are the solder joints near the perimeter-row (outer-row) columns of the 1657CCGA package.
- The failure mode of solder joints for all the PCB surface finishings is the fracture near the interface between the solder columns and the solder fillets on the package side and interface between the solder column and the solder fillets on the PCB side.

Lau, J. H., D. Shangguan, T. Castello, R. Horsley, J. Smetana, W. Dauksher, D. Love, I. Menis, and B. Sullivan, "Failure Analysis of Lead-Free Solder Joints for High-Density Packages'", *Journal of Soldering & Surface Mount Technology*, Vol. 16, No. 2, 2004, pp. 69-76.

STATISTICAL ANALYSIS OF RELIABILITY DATA – LOGNORMAL

STATISTICAL ANALYSIS OF RELIABILITY DATA – LOGNORMAL

The PDF of the standard 2-parameter lognormal distribution is given as

$$f(x) = \frac{1}{x\sigma\sqrt{2\pi}} \exp\left[-\frac{(lnx-\mu)^2}{2\sigma^2}\right]$$

where x is the random variable of the lognormal distribution, σ is the shape parameter (of the standard deviation of the normal distribution) and μ is the location parameter (of the mean of the normal distribution).

The CDF of the standard 2-parameter lognormal distribution is given as

$$F(x) = \int_x^\infty f(t)dt = \frac{1}{\sigma\sqrt{2\pi}} \int_{\ln(x)}^\infty \exp\left[-\frac{(t-\mu)^2}{2\sigma^2}\right] \mathrm{dt} = \Phi\left(\frac{\ln x-\mu}{\sigma}\right)$$

where Φ(z) denotes the CDF of the standard normal distribution.

The reliability of the lognormal distribution is given as $R(x) = 1 - F(x) = 1 - \frac{1}{\sigma\sqrt{2\pi}} \int_{\ln(x)}^\infty \exp\left[-\frac{(t-\mu)^2}{2\sigma^2}\right] \mathrm{dt}$

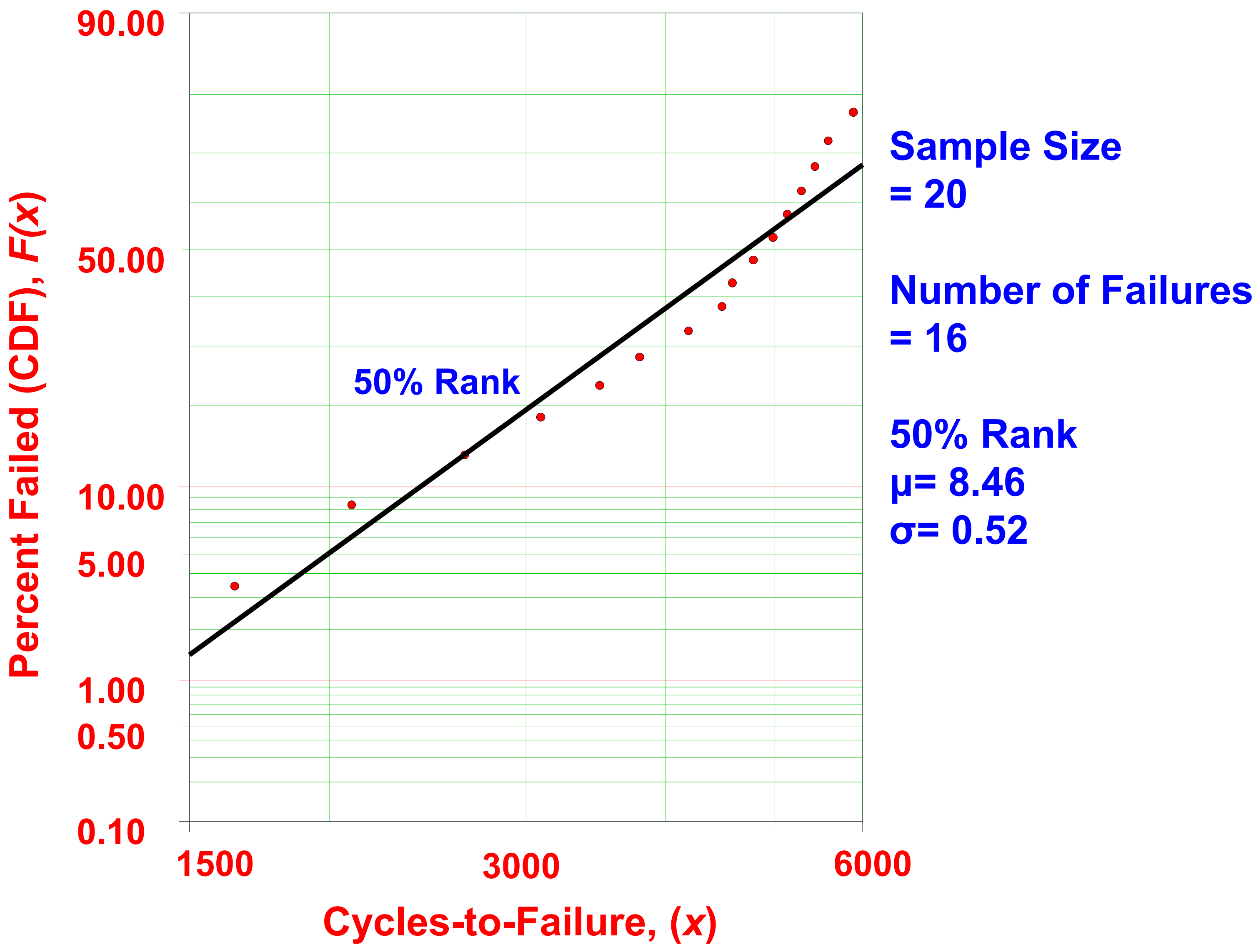
The failure rate of the lognormal distribution is given by: $h(x) = \frac{\frac{1}{x\sigma\sqrt{2\pi}}\exp\left[-\frac{(\ln x-\mu)^2}{2\sigma^2}\right]}{1-\int_{\ln(x)}^\infty \frac{1}{\sigma\sqrt{2\pi}}\exp^{-\frac{1}{2}\left(\frac{t-\mu}{\sigma}\right)^2} dt}$

The *MTTF* of the lognormal distribution is given by: $MTTF = \exp\left(\mu + \frac{\sigma^2}{2}\right)$

The median of the lognormal distribution (T_{50}) is given by: $T_{50} = \exp(\mu)$ or $\mu = \ln T_{50}$

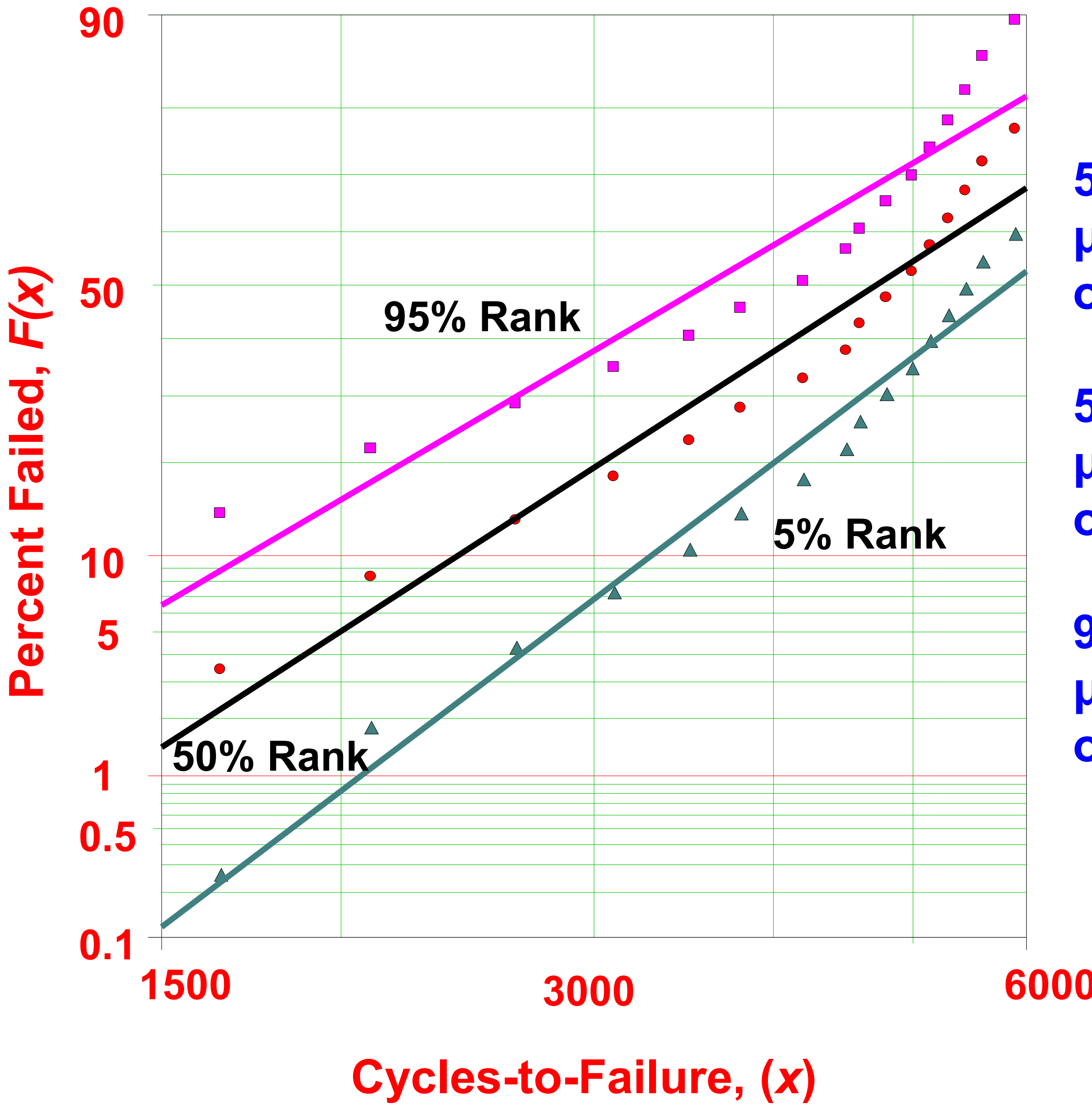
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Lognormal Plot of the 256-Pin Plastic Ball Grid Array (PBGA) PCB Assembly



Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Lognormal Plot of the 256-Pin Plastic Ball Grid Array (PBGA) PCB Assembly at 90% Confidence



50% Rank
μ= 8.46
σ= 0.52

5% Rank
μ= 8.67
σ= 0.44

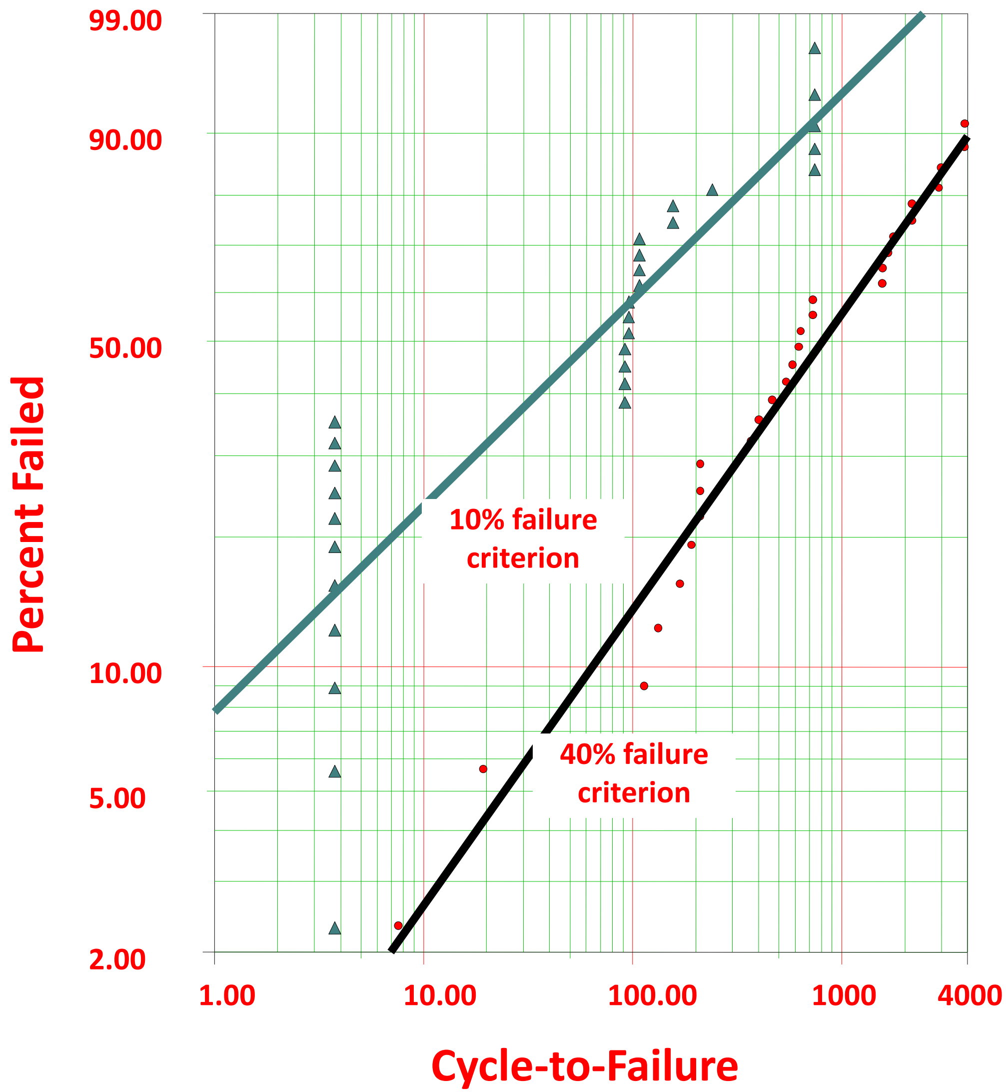
95% Rank
μ= 8.18
σ= 0.57

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

A NOTE ON FAILURE CRITERIA

- **The most important factor in reliability tests is the failure criteria.**
-
- **During reliability tests, we continuously perform the resistance measurements.**
- **The failure criterion is defined as the resistance increases to certain (e.g., 1 to ∞) percentages of the original resistance.**
- **Usually daisy chains, which connect the solder interconnects of the chip/package and substrate/PCB, allow the measurements.**
- **Since most solder joints under fatigue loadings will go through crack initiation, crack propagation, and crack rupture sooner or later, the daisy chains' resistance will increase accordingly, that is, from small to large, and become ∞ when the solder joint is totally cracked (opened). (Most people unintentionally pick the last one.)**
- **Since the exact "resistance vs. crack length" relations of various lead-free solder joints don't exist today, people just randomly pick a number, which is from 1 to ∞ percent of the initial resistance. That's one of the reasons why there are so many different Weibull/lognormal plots in the lectures, even with the same package, PCB, solder paste, sample size, test condition, and test period.**

Effect of Failure Criterion on Reliability Testing



(1) The life distribution is many times different from the failure criterion based on the 10% resistance increase and the 40% resistance increase,
(2) for the same percent failures, the life taken from the failure criterion based on higher resistance increases is longer, and
(3) as expected, there are more failures with the failure criterion based on lower resistance increases.

208-pin PQFP (plastic quad flat pack) with a lead-free solder joint subject to -40 ⇆ 125°C thermal cycling.

Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Why Acceleration Models?

- **In reliability tests, the most idea situation is to have the test conditions very close to the use (operating) conditions.**

- **However because of time-to-market and costs saving, this is almost impossible.**

- **The practical way is to run accelerated tests with increased intensity, and realistic sample sizes and test times.**

- **Thus, most reliability tests are accelerated tests.**

- **In this case, the price to pay is to construct the acceleration factors to map (transfer) the failure probability, reliability function, mean life, and failure rate from a test condition to the service operating (use) condition.**

- **Acceleration Models are needed for determining the acceleration factors.**

$$x_o = \alpha x_T^{\eta}$$

where x_o is the time-to-failure at operating condition, α is the acceleration factor, η is a larger than zero real number, and x_T is the time-to-failure at test condition. When $\eta = 1$, then we have liner acceleration

$$x_o = \alpha x_T$$

"Acceleration Models, Constitutive Equations and Reliability of Lead-Free Solders and Joints," *IEEE/ECTC Proceedings*, May 2003, pp. 229-236.

Well-Known Linear Acceleration Factors

- **How to determine α (the acceleration factor)?**
  The answer is that you need an acceleration model.

- **How do you choose an acceleration model?**
  The answer is tests and failure mechanisms!

- **Some Well-Known Linear Acceleration Factors**
  Norris-Landzberg (in terms of maximum temperature and frequency):

$$\alpha = \left(\frac{f_o}{f_T}\right)^q \left(\frac{\Delta T_T}{\Delta T_o}\right)^c \exp\left[1414(1/T_o - 1/T_T)\right]$$

T_T = maximum temperature during cycling (in degrees Kelvins) at testing condition
f_T = temperature cycling frequency at testing condition
ΔT_T = temperature range (in degree Celsius) at testing condition
T_o = maximum temperature during cycling (in degrees Kelvins) at operating condition
f_o = temperature cycling frequency at operating condition
ΔT_o= temperature range (in degree Celsius) at operating condition
For SnPb solders, q = 1/3 and c = 1.9 ~ 2.0 have been used.

Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies, McGraw-Hill, New York, 1997.

Linear Acceleration Factor for Sn3Ag0.5Cu in Terms of Dwell-Time and Maximum Temperature

For Sn3Ag0.5Cu, **Pan et al**. proposed a modification of **Norris-Landzberg** equation by replacing the cyclic frequency (*f*) with dwell time at high temperature (*t*):

$$\alpha = \left(\frac{\Delta T_t}{\Delta T_o}\right)^a \left(\frac{t_t}{t_o}\right)^b \exp\left[c\left(\frac{1}{T_{max,o}} - \frac{1}{T_{max,t}}\right)\right]$$

where *a*, *b*, and *c* are the coefficients for the temperature range (ΔT), dwell time (*t*), and maximum temperature during cycling (T_{max}), respectively. A nonlinear curve fit of the temperature cycling data of the CBGA (ceramic ball grid array), CSP (chip scale package), and TSOP (thin small outline package) on PCB at various temperature ranges such as 0 ⇆ 60°C, 0 ⇆ 100°C, and -25 ⇆ 125°C, Pan et al. obtained the following acceleration factor:

$$\alpha = \left(\frac{\Delta T_t}{\Delta T_o}\right)^{2.65} \left(\frac{t_t}{t_o}\right)^{0.136} \exp\left[2185\left(\frac{1}{T_{max,o}} - \frac{1}{T_{max,t}}\right)\right]$$

where t_t and t_o are the dwell time at high temperature, ΔT_t and ΔT_o are the temperature range (in degree Celsius) during thermal cycling, and $T_{max,t}$ and $T_{max,o}$ are the maximum (peak) temperature (in degrees Kelvins) attained during thermal cycling, respectively at testing condition and at operating condition.

Pan, et al., "An Acceleration Model for Sn-Ag-Cu Solder Joint Reliability under Various Thermal Cycle Conditions", *SMTA,* September 2005, pp. 876-883.

Linear Acceleration Factor for Sn3Ag0.5Cu in Terms of Dwell-Time and Maximum Temperature

For example, the test conditions are: 0 ⇆ 100°C with the dwell time at high temperature = 15 minutes; and the operating conditions are: 20 ⇆ 70°C with the dwell time at high temperature = 720 minutes.

$$\alpha = \left(\frac{\Delta T_t}{\Delta T_o}\right)^{2.65} \left(\frac{t_t}{t_o}\right)^{0.136} \exp\left[2185\left(\frac{1}{T_{max,o}} - \frac{1}{T_{max,t}}\right)\right]$$

Then the acceleration factor is:

$$\alpha = \left(\frac{100}{50}\right)^{2.65} \left(\frac{15}{720}\right)^{0.136} \exp\left[2185\left(\frac{1}{273+70} - \frac{1}{273+100}\right)\right]$$

$$\alpha = 6.18$$

Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", *ASME Transactions, Journal of Electronic Packaging*, June 2021, pp. 1-36.

Linear Acceleration Factor for Sn3Ag0.5Cu in Terms of Frequency and Maximum Temperature

For Sn3Ag0.5Cu, some of the researchers still use the classical Norris-Lanzberg acceleration model, i.e., in terms of the cyclic frequency and maximum temperature during thermal cycling:

$$\alpha = \left(\frac{\Delta T_t}{\Delta T_o}\right)^a \left(\frac{f_o}{f_t}\right)^b \exp\left[c\left(\frac{1}{T_{max,o}} - \frac{1}{T_{max,t}}\right)\right]$$

For PBGA, fc-PBGA, CBGA (ceramic ball grid array), CSP, QFP (quad flat pack), flip chip, etc. with test conditions such as ΔT = 135°C and ΔT = 180°C, Lall et al. obtained the following acceleration factor for Sn3Ag0.5Cu

$$\alpha = \left(\frac{\Delta T_t}{\Delta T_o}\right)^{2.3} \left(\frac{f_o}{f_t}\right)^{0.3} \exp\left[4562\left(\frac{1}{T_{max,o}} - \frac{1}{T_{max,t}}\right)\right]$$

For example, the test conditions are: 0 ⇆ 100°C with one cycle per hour and the operating conditions are: 20 ⇆ 70°C with one cycle per day. Then the acceleration factor is, for example from Equation (6.63):

$$\alpha = \left(\frac{100}{50}\right)^{2.3} \left(\frac{1}{24}\right)^{0.3} \exp\left[4562\left(\frac{1}{273+70} - \frac{1}{273+100}\right)\right] = 5.52$$

Lall, P., A. Shirgaokar, and D. Arunachalam, “Norris-Landzberg Acceleration Factor and Goldmann Constants for SAC305 Lead-Free Electronics”, *ASME Transactions, Journal of Electronic Packaging*, Vol. 134, September 2012, pp. 1-8.

Linear Acceleration Factor for Sn3Ag0.5Cu in Terms of Frequency and Mean Temperature

Osterman, et al. proposed another modification of the Norris-Landzberg Equation by replacing the maximum temperature during thermal cycling with mean temperature during thermal cycling. The revised equation takes the following form:

$$\alpha = \left(\frac{\Delta T_t}{\Delta T_o}\right)^a \left(\frac{f_o}{f_t}\right)^b exp\left[c\left(\frac{1}{T_{mean,o}} - \frac{1}{T_{mean,t}}\right)\right]$$

where *a*, *b*, and *c* are the coefficients for the temperature range (ΔT), frequency (*f*), and mean temperature during cycling (T_{mean}), respectively. A nonlinear curve fit of the temperature cycling data of the CABGA (ChipArray BGA) and CTBGA (Thin ChipArray BGA) on PCB at various temperature ranges such as 0 ⇆ 100°C, -40 ⇆ 100°C, -40 ⇆ 125°C, 25 ⇆ 125°C, and -15 ⇆ 125°C, Osterman, et al. obtained the following acceleration factor for Sn3Ag0.5Cu:

$$\alpha = \left(\frac{\Delta T_t}{\Delta T_o}\right)^{2.728} \left(\frac{f_o}{f_t}\right)^{0.345} exp\left[1602\left(\frac{1}{T_{mean,o}} - \frac{1}{T_{mean,t}}\right)\right]$$

For example, the test conditions are: 0 ⇆ 100°C with 24 cycles per day and find the product survives 900 cycles. Is it sufficient for a 10-year operating conditions of 20 ⇆ 60°C with 1 cycle per day?

$$\alpha = \left(\frac{100}{40}\right)^{2.728} \left(\frac{1}{24}\right)^{0.345} exp\left[1602\left(\frac{1}{273+40} - \frac{1}{273+50}\right)\right] = 4.73$$

Osterman, M., "Modeling Temperature Cycle Fatigue Life of Select SAC Solders", *SMTA International Conference,* September 2018.

Comparison of the Mean-Life of Two Sets of Samples

- **In many situations, the qualities and uniformities of two products are to be compared from the knowledge of the limited test data.**

- **One of the difficult tasks in life testing is to draw conclusions about a population from a small sample size.**

- **It is even more difficult to compare the populations of two products from the knowledge of their limited test data.**

- **If one product is found to be superior to another, how CONFIDENT, *P* (this is different from the confidence (*C*) discussed earlier) can it be that the same is true of their populations?**

- **Herein, a simple approach is used to determine whether one product is better than the other, without inquiring what the actual differences.**

"Reliability Testing and Data Analysis of Lead-Free Solder Joints for High-Density Packages'", *Journal of Soldering & Surface Mount Technology*, Vol. 16, No. 2, 2004, pp. 46-68.

Determined Confidence (*P*)

$$P = \frac{1}{1 + \frac{\log 1/q}{\log 1/(1-q)}}$$

where

$$q = 1 - \frac{1}{\left[1 + \left(\frac{t + 4.05}{6.12}\right)^5\right]^{40/7}}$$

$$t = \frac{\sqrt{1 + \sqrt{T}}\,(\rho - 1)}{\rho\Omega_2 + \Omega_1}$$

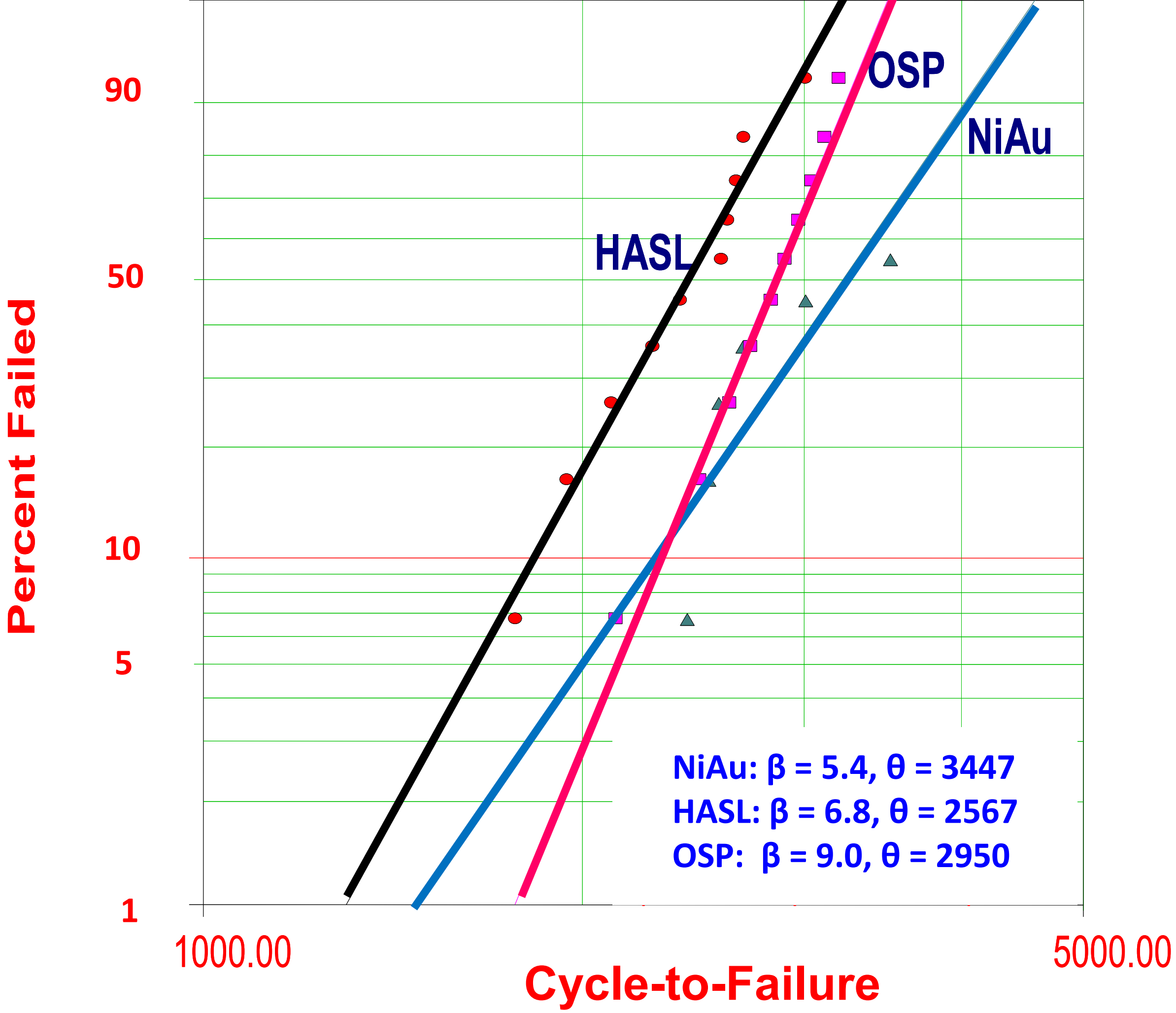
$$\rho = \frac{M_2}{M_1} \qquad T = (r_1 - 1)(r_2 - 1)$$

$$\Omega_1 = \sqrt{\frac{\Gamma(1 + 2/\beta_1)}{\Gamma^2(1 + 1/\beta_1)} - 1} \qquad \Omega_2 = \sqrt{\frac{\Gamma(1 + 2/\beta_2)}{\Gamma^2(1 + 1/\beta_2)} - 1}$$

and M_1 is the mean life of Simple 1 (S1), M_2 is the mean life of Simple 2 (S2), r_1 is the number of failures in S1, r_2 is the number of failures in S2, β_1 is the Weibull slope of S1, and β_2 is the Weibull slope of S2. It can be seen that this confidence *P* (is to be determined) which is different from the confidence *C* (a given value).

“Reliability Testing and Data Analysis of Lead-Free Solder Joints for High-Density Packages’”, *Journal of Soldering & Surface Mount Technology*, Vol. 16, No. 2, 2004, pp. 46-68.

Weibull Plots of 1567 CCGA PCB Assemblies with various Surface Finishing



Different Assembly	Assigned Symbol	Mean Life, cycles	Mean Life Ratio (Comparison)	Determined Confidence
SnAgCu paste on HASL PCB	A	2397	B/A = 1.33	99%
SnAgCu paste on NiAu PCB	B	3179	B/C = 1.14	89%
SnAgCu paste on OSP PCB	C	2793	C/A = 1.17	94%

Design for Reliability

CONTENTS

DESIGN FOR RELAIBILITY

In the past three decades, DFR of solder joints is becoming very important. DFR is usually performed by a mathematical modeling based on the material properties and geometries of the structure, and laws of engineering and physics in order to:

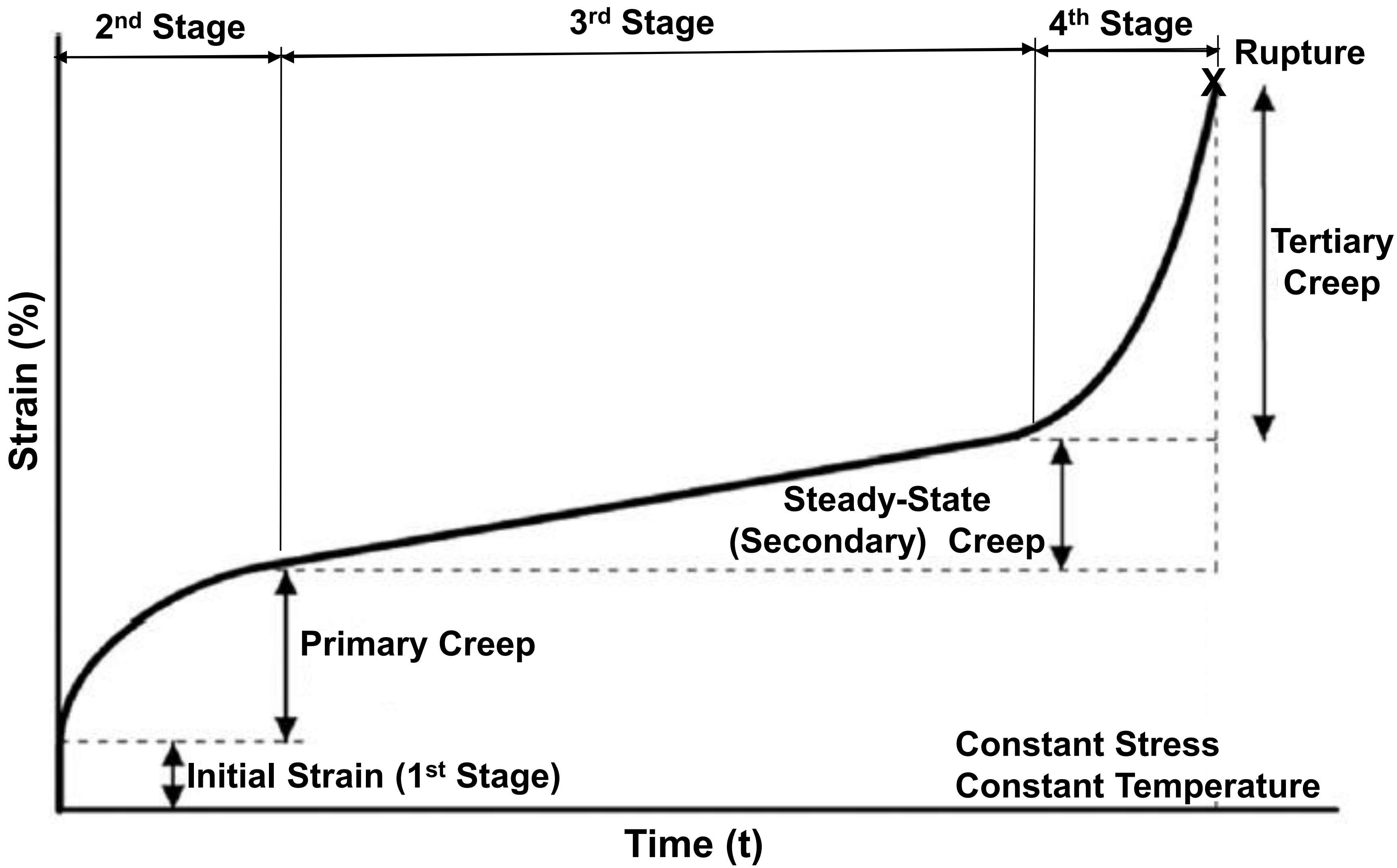
- **eliminate trial-and-error of reliability tests,**
- **reduce cost,**
- **reduce test and failure analysis cycles,**
- **reduce time-to-market,**
- **provide insight into the physical, electrical, mechanical, and thermal behaviors of the solder joints, e.g., (a) the maximum stress/strain locations - to help test-board designs to capture the most likely (solder joint) failure locations and to help failure analysis to find these failures sites, and (b) the failure mode - to help failure analysis to look for crack and delamination,**
- **provide comparison between material properties, and**
- **provide comparison between structural geometries.**

Key Steps in Design for Reliability of Solder Joints

Structure Geometry	Geometry and Materials
Boundary Conditions	Kinetic and Kinematics
Problem Definition	Overload or Fatigue or Both
Material Properties	Constitutive Equation, Young's Modulus, CTE, etc.
Structural Analysis	Finite Element Method
Determine the Strain or Inelastic Energy Density per Cycle (ΔW_i) in Solder Joints	Post Processing
Life Prediction	$N_f = \sum_j \alpha_j \left[\frac{\sum_i \Delta W_i \, x \, V_i}{\sum_i V_i}\right]^{\beta_j}$

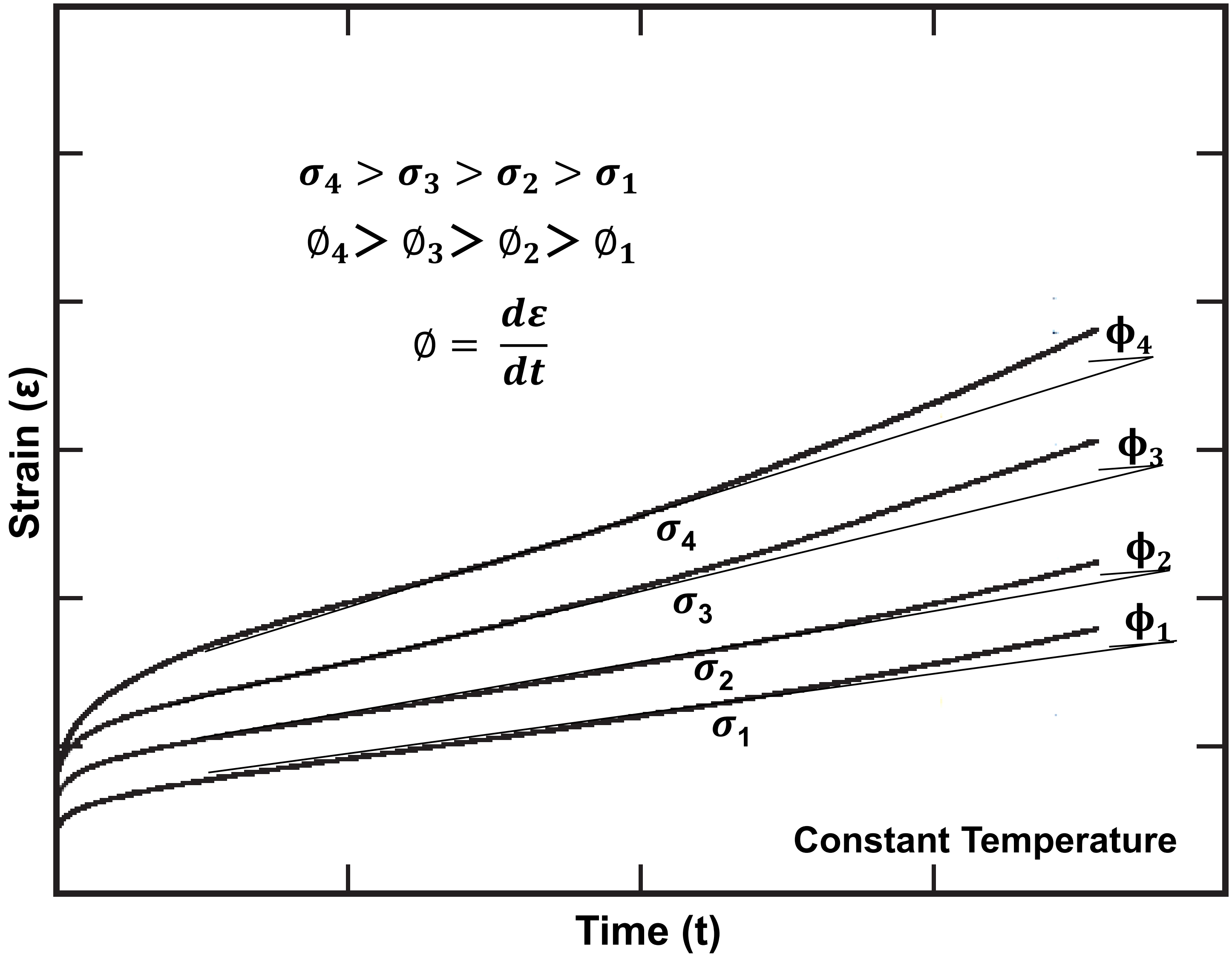
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Creep Curve



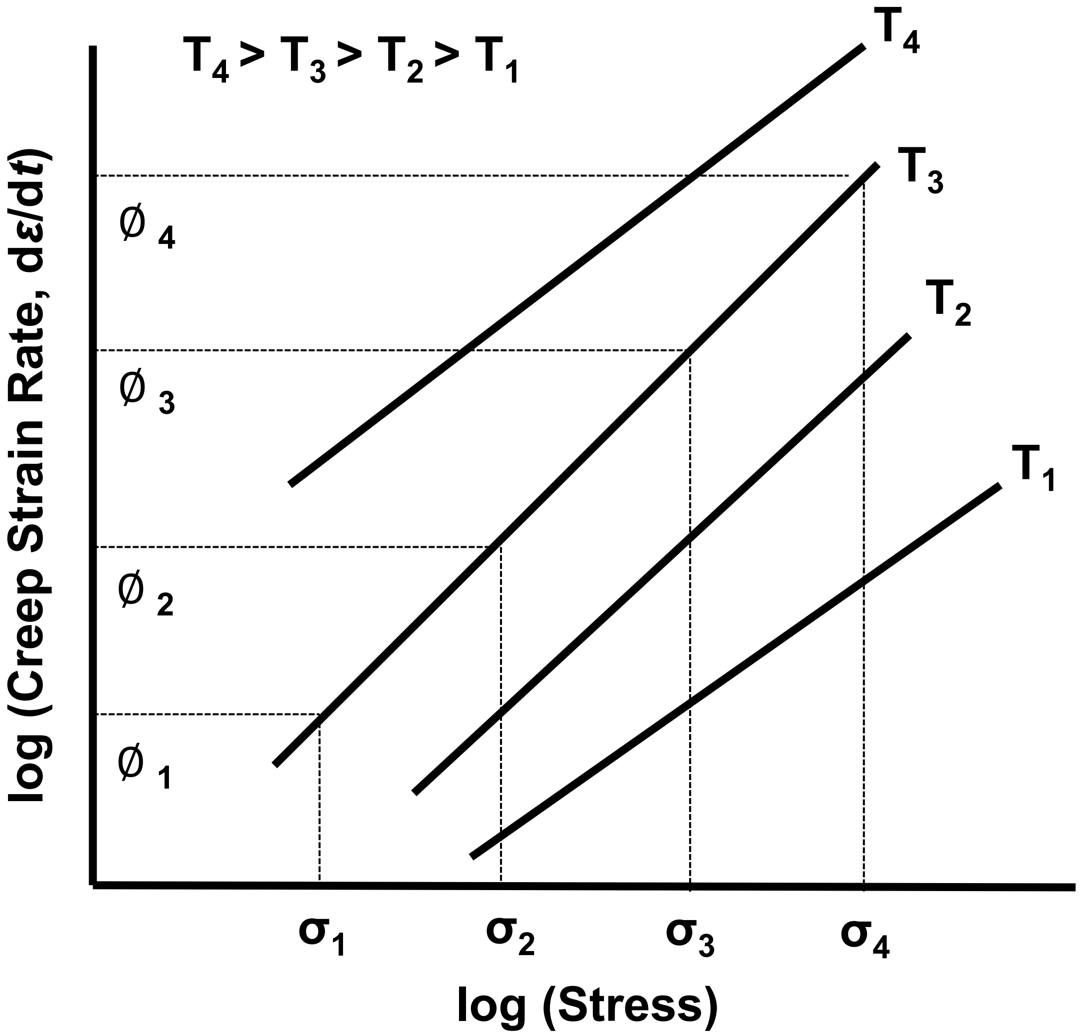
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Creep Curves with Various Stresses at a Constant Temperature



Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Log-log Plots of Stress vs. Creep Strain Rate for Constant Temperatures



Norton Power Creep Law

$$\dot{\varepsilon} = A\sigma^{n}\left(\frac{-Q}{RT}\right)$$

$\dot{\varepsilon}$ **is the steady-state creep stain rate (1/s),**
σ **is the applied stress (MPa),**
R **is the Boltzmann's constant (7.617x10^{-5} eV/K),**
and *T* is the absolute temperature (Kelvin).

The constants *A*, *n*, and *Q* for a particular lead-free solder can be determined from the creep curve of that solder.

Norton, F. H., *The Creep of Steel at High Temperatures*, McGraw-Hill, New York, 1929.

Norton Power Creep Law for Various Solders

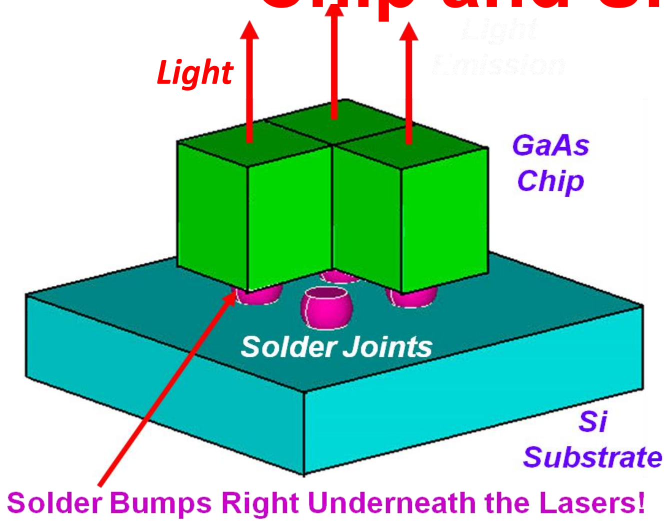
$$\dot{\varepsilon} = A\sigma^n\left(\frac{-Q}{RT}\right)$$

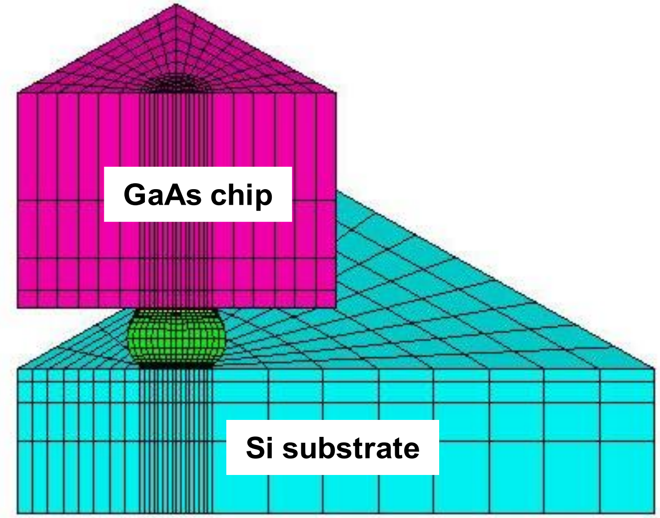
	A	*n*	*Q*
Au20Sn [6, 107, 108]	$1.3977\text{x}10^{-21}$	2.55	9516
Sn58Bi [6, 107, 108]	$9.82\text{x}10^{-24}$	4.05	8483
Sn3.8Ag0.7Cu [61]	$1.5\text{x}10^{-9}$	8.2	8540
Sn3.8Ag0.7Cu0.03Ce [61]	$6.2\text{x}10^{-11}$	8	9622

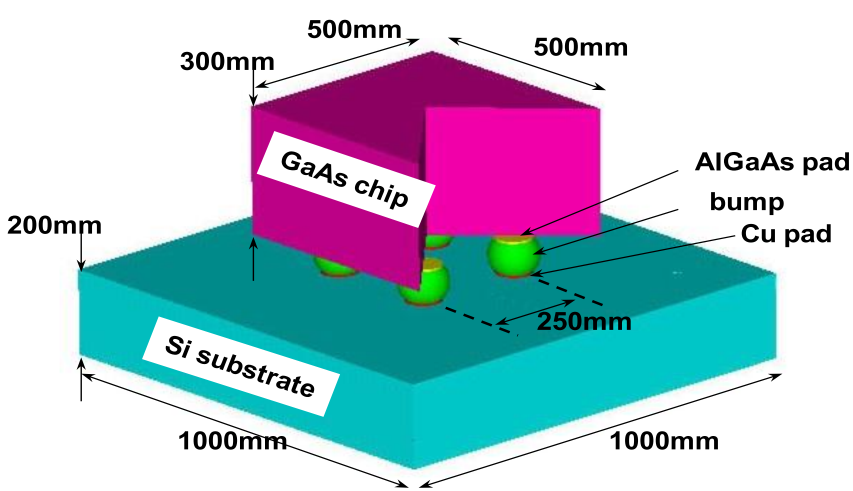
R **is the Boltzmann's constant = 7.617x10^{-5} eV/K.**
T (Kelvin), $\dot{\varepsilon}$ (1/s).
For Au20Sn and Sn58Bi, σ is in Pa.
For Sn3.8Ag0.7Cu and Sn3.8Ag0.7Cu0.03Ce, σ is in MPa.

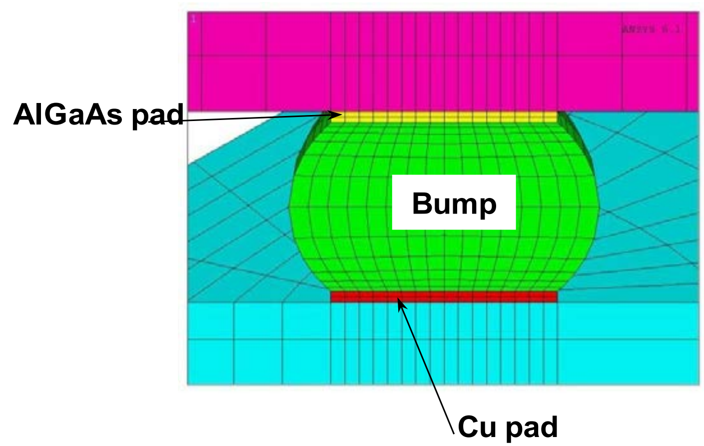
[6] Lau, J. H., and Pao, Y., 1997, Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies, McGraw-Hill, New York.
[61] Zhang, L., Xue, S., Gao, L., Zeng, G., Chen, Y., Yu, S., and Sheng, Z., 2010, "Creep Behavior of SnAgCu Solders With Rare Earth Ce Doping," Trans. Nonferrous Met. Soc, 20(3), pp. 412–417.
[107] Lau, J. H., and Dauksher, W., 2005, "Thermal-Mechanical Analysis of a Flip Chip VCSEL (Vertical-Cavity Surface-Emitting Laser) Package With Low Temperature Lead-Free (Sn-Bi) Solder Joints," ASME Paper No. IMECE2005-79981.
[108] Lau, J. H., and Dauksher, W., 2006, "Thermal Stress Analysis of a Flip-Chip Parallel VCSEL (Vertical-Cavity Surface-Emitting Laser) Package With Low Temperature Lead-Free (48Sn-52In) Solder Joints," IEEE/ECTC Proceedings, San Diego, CA, May 30–June 2, pp. 1009–1017.

VCSEL Assembly with Lead-free Solder Joints, GaAs Chip and Silicon Substrate





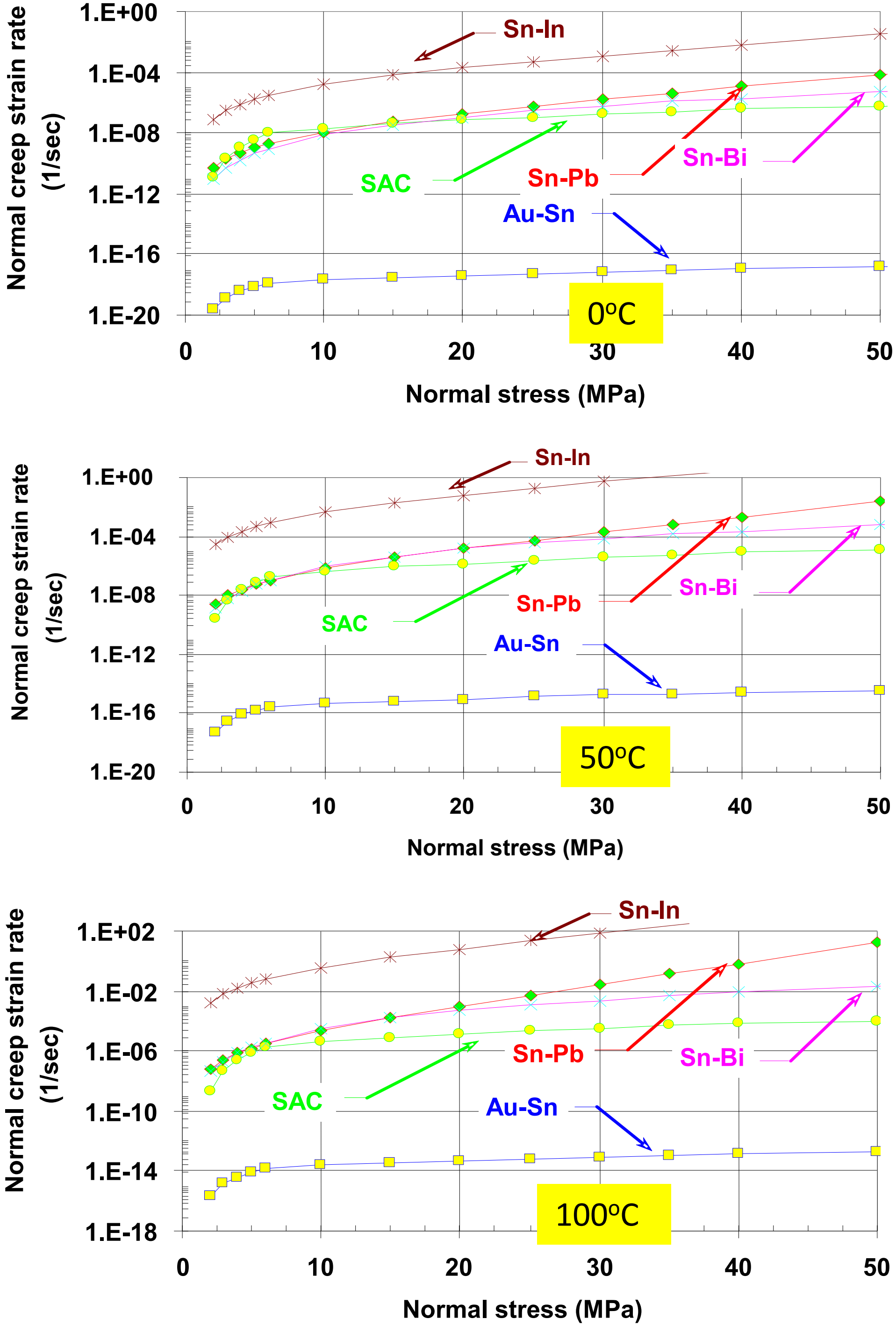




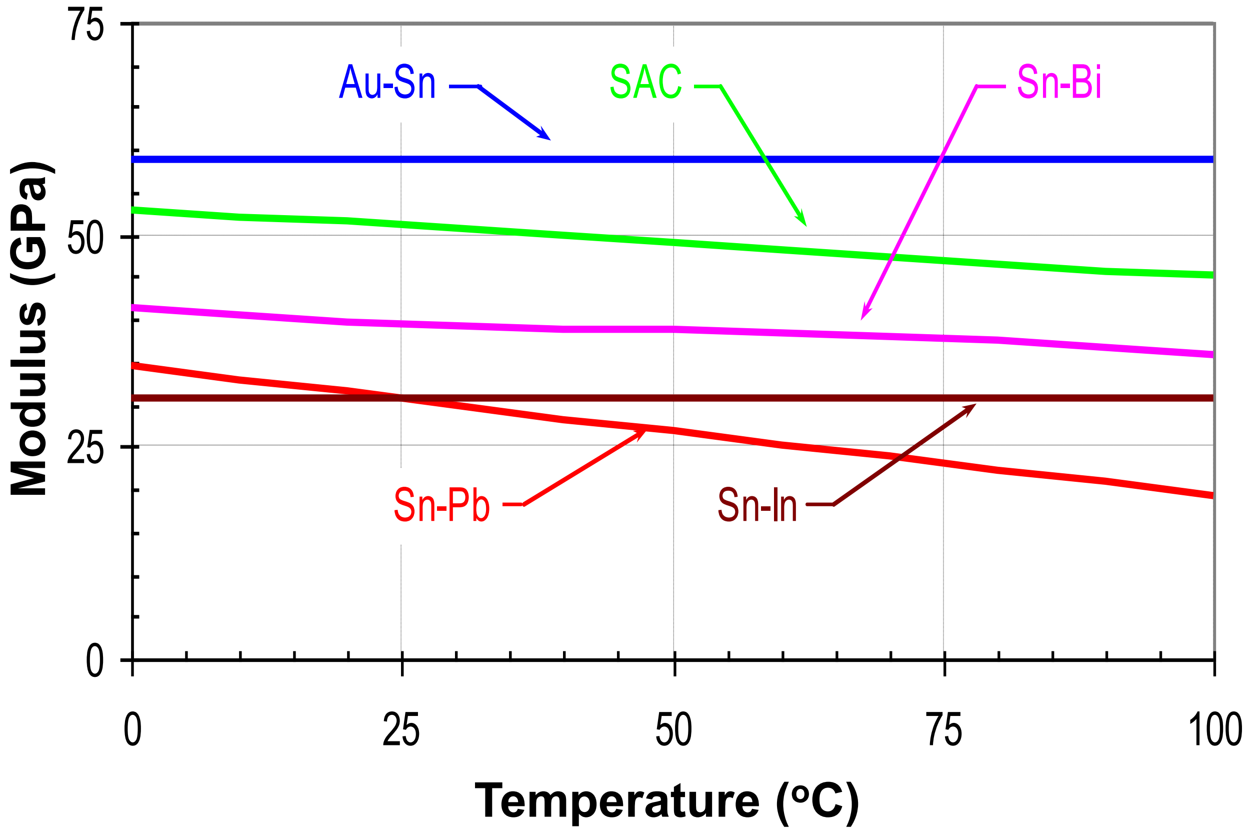
Lau, J. H., and W. Dauksher, "Thermal-Mechanical Analysis of a Flip-Chip VCSEL (Vertical-Cavity Surface-Emitting Laser) Package with Low-Temperature Lead-Free (Sn-Bi) Solder Joints", *ASME Paper No. IMECE2005-79981*, November 2005.

Lau, J. H., and Walter Dauksher, "Thermal Stress Analysis Of A Flip-Chip Parallel VCSEL (Vertical-Cavity Surface-Emitting Laser) Package With Low-Temperature Lead-Free (48Sn-52In) Solder Joints", *IEEE/ECTC Proceedings*, May 2006, pp. 1009-1017.

Creep Strain rate vs. Stress Curves (at 0°C, 50°C, and 100°C) for Various Lead-Free Solders



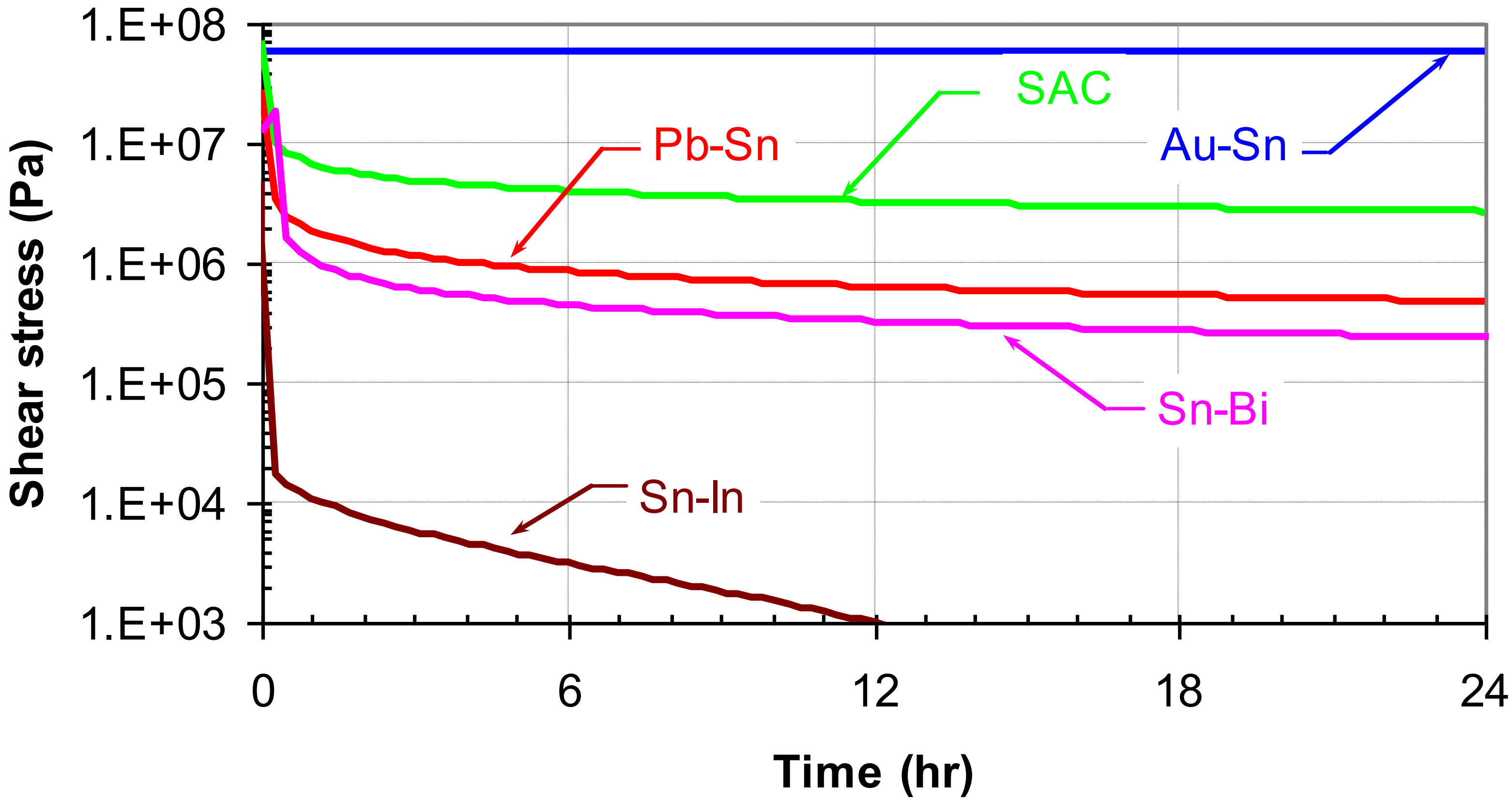
Yong's Modulus vs. Temperatures for Various Lead-Free Solders



Lau, J. H., and W. Dauksher, "Thermal-Mechanical Analysis of a Flip-Chip VCSEL (Vertical-Cavity Surface-Emitting Laser) Package with Low-Temperature Lead-Free (Sn-Bi) Solder Joints", *ASME Paper No. IMECE2005-79981*, November 2005.

Lau, J. H., and Walter Dauksher, "Thermal Stress Analysis Of A Flip-Chip Parallel VCSEL (Vertical-Cavity Surface-Emitting Laser) Package With Low-Temperature Lead-Free (48Sn-52In) Solder Joints", *IEEE/ECTC Proceedings*, May 2006, pp. 1009-1017.

Shear Stress Time-history of the AuSn and SnBi Solder Joints



Lau, J. H., and W. Dauksher, "Thermal-Mechanical Analysis of a Flip-Chip VCSEL (Vertical-Cavity Surface-Emitting Laser) Package with Low-Temperature Lead-Free (Sn-Bi) Solder Joints", *ASME Paper No. IMECE2005-79981*, November 2005.

Lau, J. H., and Walter Dauksher, "Thermal Stress Analysis Of A Flip-Chip Parallel VCSEL (Vertical-Cavity Surface-Emitting Laser) Package With Low-Temperature Lead-Free (48Sn-52In) Solder Joints", *IEEE/ECTC Proceedings*, May 2006, pp. 1009-1017.

Material Properties of the VCSEL Assembly

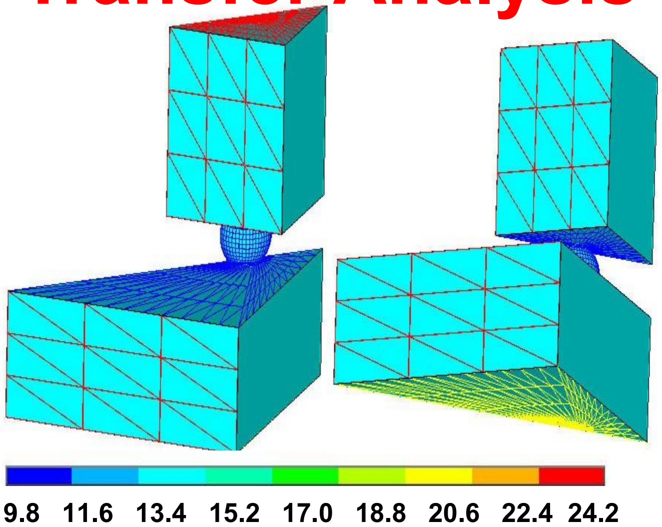
Material	E (GPa)	α (ppm/°K)	v	k (W/m°K)
Si	167	2.54	0.28	154
Cu	76	17	0.35	398
Au20Sn	59	16	0.3	251
Sn58Bi	$381.5-3.13T+0.009T^2$	14	0.35	18.3
AlGaAs	86	5.8	0.31	33.67
GaAs	86	5.8	0.31	33.7

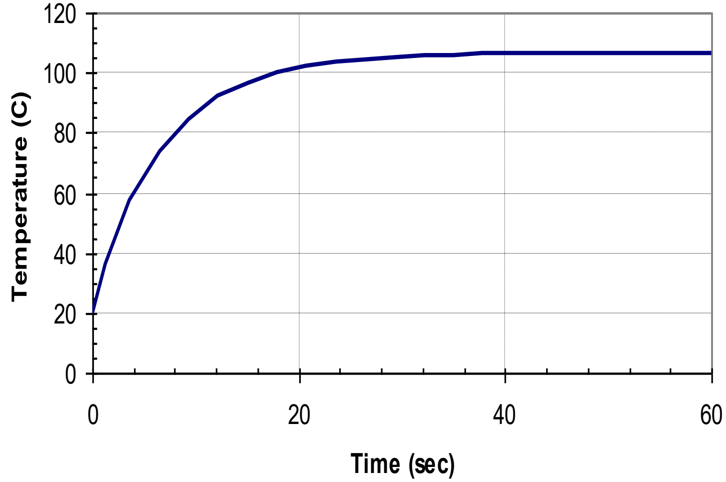
Note: T in degrees Kelvin

Lau, J. H., and W. Dauksher, "Thermal-Mechanical Analysis of a Flip-Chip VCSEL (Vertical-Cavity Surface-Emitting Laser) Package with Low-Temperature Lead-Free (Sn-Bi) Solder Joints", *ASME Paper No. IMECE2005-79981*, November 2005.

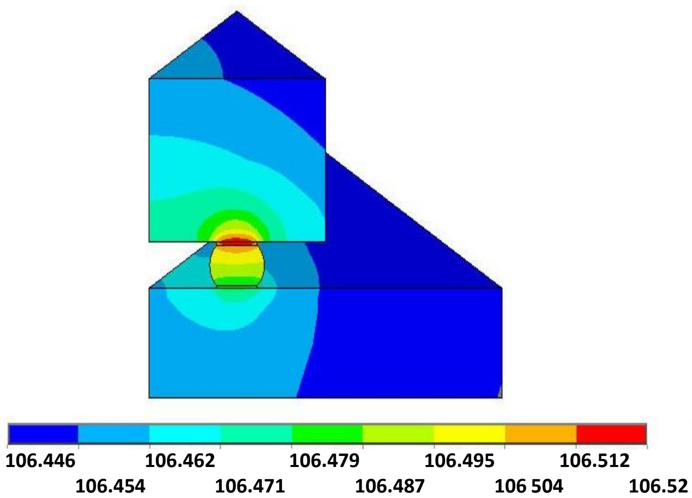
Lau, J. H., and Walter Dauksher, "Thermal Stress Analysis Of A Flip-Chip Parallel VCSEL (Vertical-Cavity Surface-Emitting Laser) Package With Low-Temperature Lead-Free (48Sn-52In) Solder Joints", *IEEE/ECTC Proceedings*, May 2006, pp. 1009-1017.

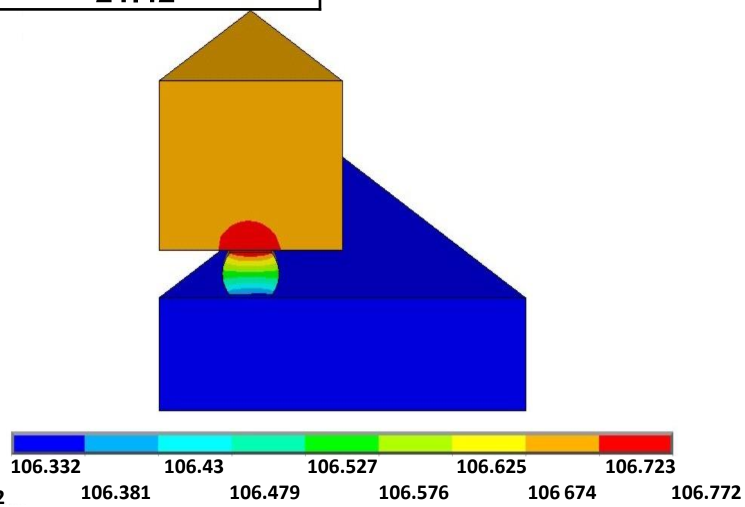
Heat Transfer Analysis of the VCSEL Assembly



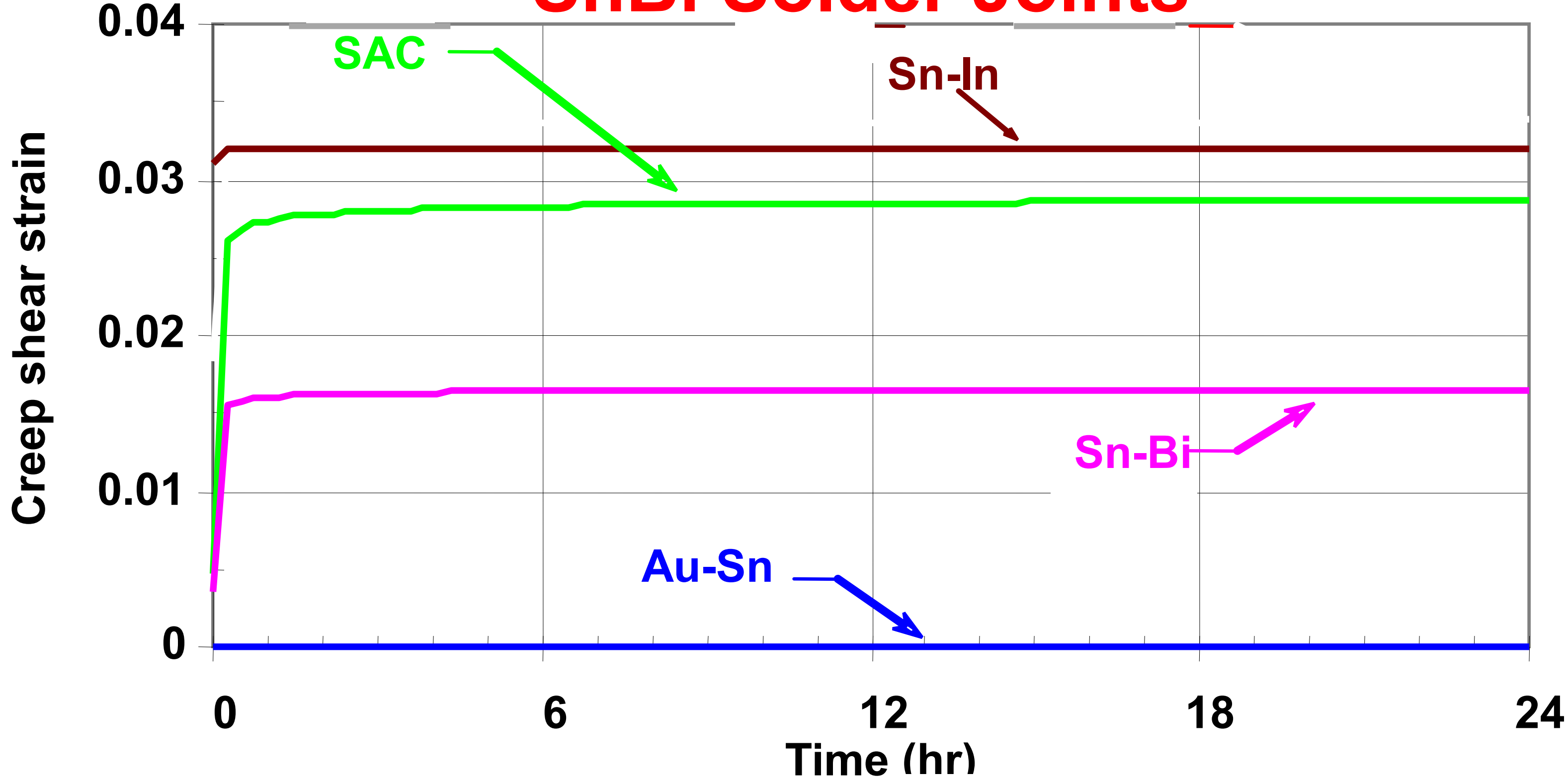


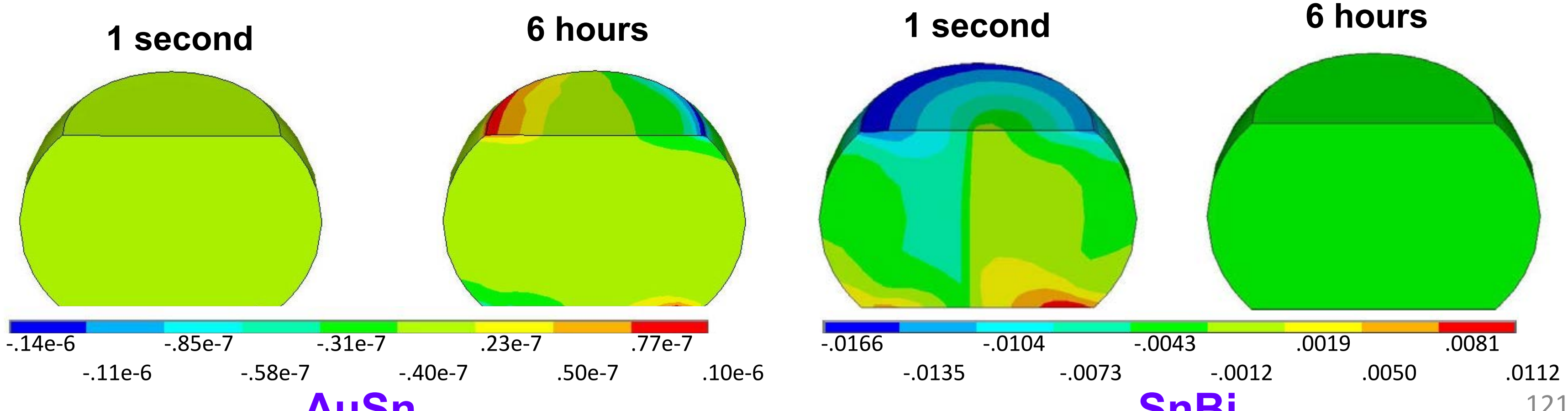
Location	Convection coefficient (W/m²°C)
GaAs chip, inner surface	9.82
GaAs chip, edge	25.96
GaAs chip, outer surface	25.96
Si substrate, inner surface	9.82
Si substrate, edge	25.96
Si substrate, outer surface	21.42





Creep Shear Strain Time-history of the AuSn and SnBi Solder Joints





WISES TWO-POWER CREEP

Wises, et al. proposed to modify Norton power creep equation into the sum of two power law terms:

$$\dot{\varepsilon} = \frac{\sigma}{E} + A_1 \left(\frac{\sigma}{\sigma_n}\right)^{n_1} \exp\left(-\frac{Q_1}{RT}\right) + A_2 \left(\frac{\sigma}{\sigma_n}\right)^{n_2} \exp\left(-\frac{Q_2}{RT}\right)$$

The first term is for the initial stress (elastic)

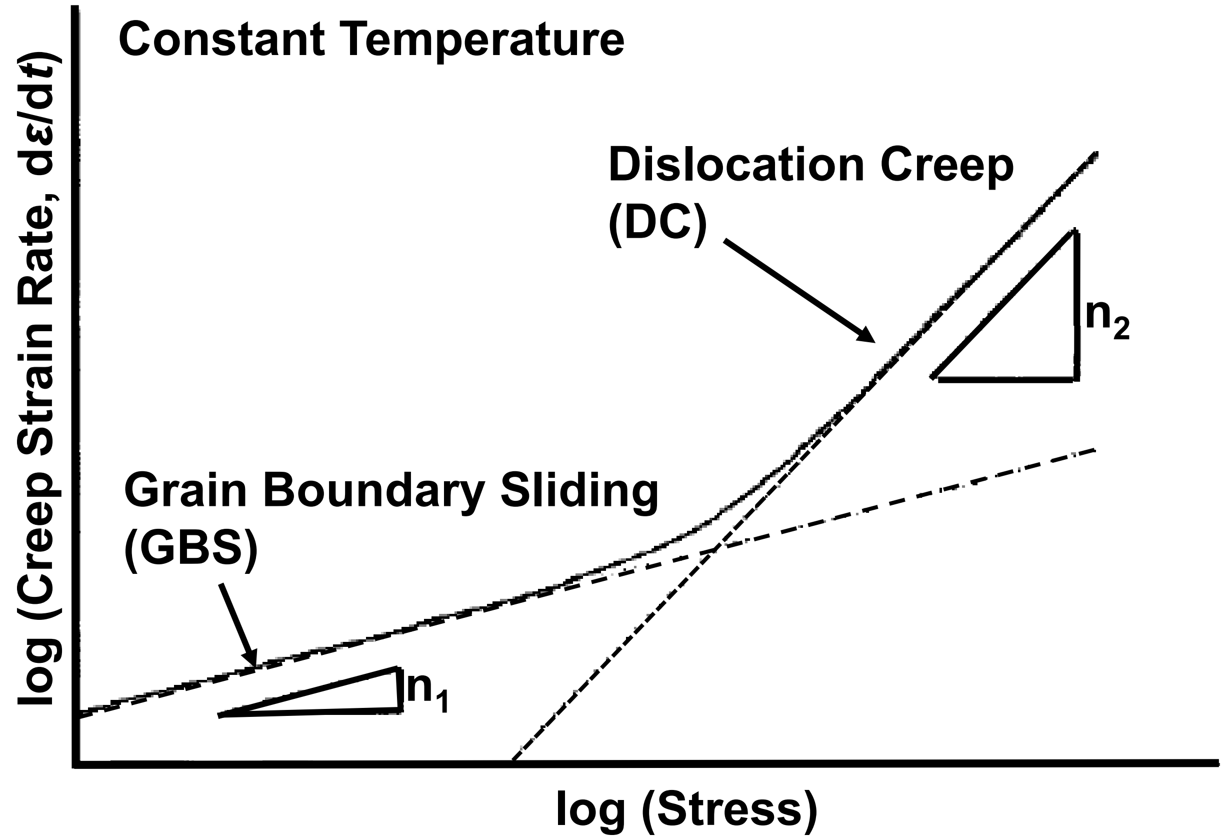
The second term corresponds to the creep behavior at low stresses, where co-operative climb processes are dominant

The third term corresponds to the creep behavior at high stresses, where combined glide/climb processes dominate.

The commercial finite element codes such as ABAQUS and ANSYS can take this form of constitutive equation

- Wiese, S., Schubert, A., Walter, H., Dudek, R., Feustel, F., Meusel, E., and Michel, B., 2001, "Constitutive Behaviour of Lead-Free Solders Vs. LeadContaining Solders - Experiments on Bulk Specimens and Flip-Chip Joints," IEEE/ECTC Proceedings, Orlando, FL, May 29–June 1, pp. 1–13.
- Wiese, S., Meusel, E., and Wolter, K., 2003, "Microstructural Dependence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders," IEEE/ECTC Proceedings, New Orleans, LA, May 27–30, pp. 197–206.
- Wiese, S., Roellig, M., and Wolter, K.-J., 2005, "Creep of Eutectic SnAgCu in Thermally Treated Solder Joints," IEEE/ECTC Proceedings, Lake Buena Vista, FL, May 31–June 3, pp. 1272–1281.
- Wiese, S., Roellig, M., Mueller, M., Bennemann, S., Petzold, M., and Wolter, K.-J., 2007, "The Size Effect on the Creep Properties of SnAgCu Solder Alloys," IEEE/ECTC Proceedings, Reno, NV, May 29–June 1, pp. 548–557.

Wises' Two-power Creep



- Wiese, S., Schubert, A., Walter, H., Dudek, R., Feustel, F., Meusel, E., and Michel, B., 2001, "Constitutive Behaviour of Lead-Free Solders Vs. LeadContaining Solders - Experiments on Bulk Specimens and Flip-Chip Joints," IEEE/ECTC Proceedings, Orlando, FL, May 29–June 1, pp. 1–13.
- Wiese, S., Meusel, E., and Wolter, K., 2003, "Microstructural Dependence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders," IEEE/ECTC Proceedings, New Orleans, LA, May 27–30, pp. 197–206.
- Wiese, S., Roellig, M., and Wolter, K.-J., 2005, "Creep of Eutectic SnAgCu in Thermally Treated Solder Joints," IEEE/ECTC Proceedings, Lake Buena Vista, FL, May 31–June 3, pp. 1272–1281.
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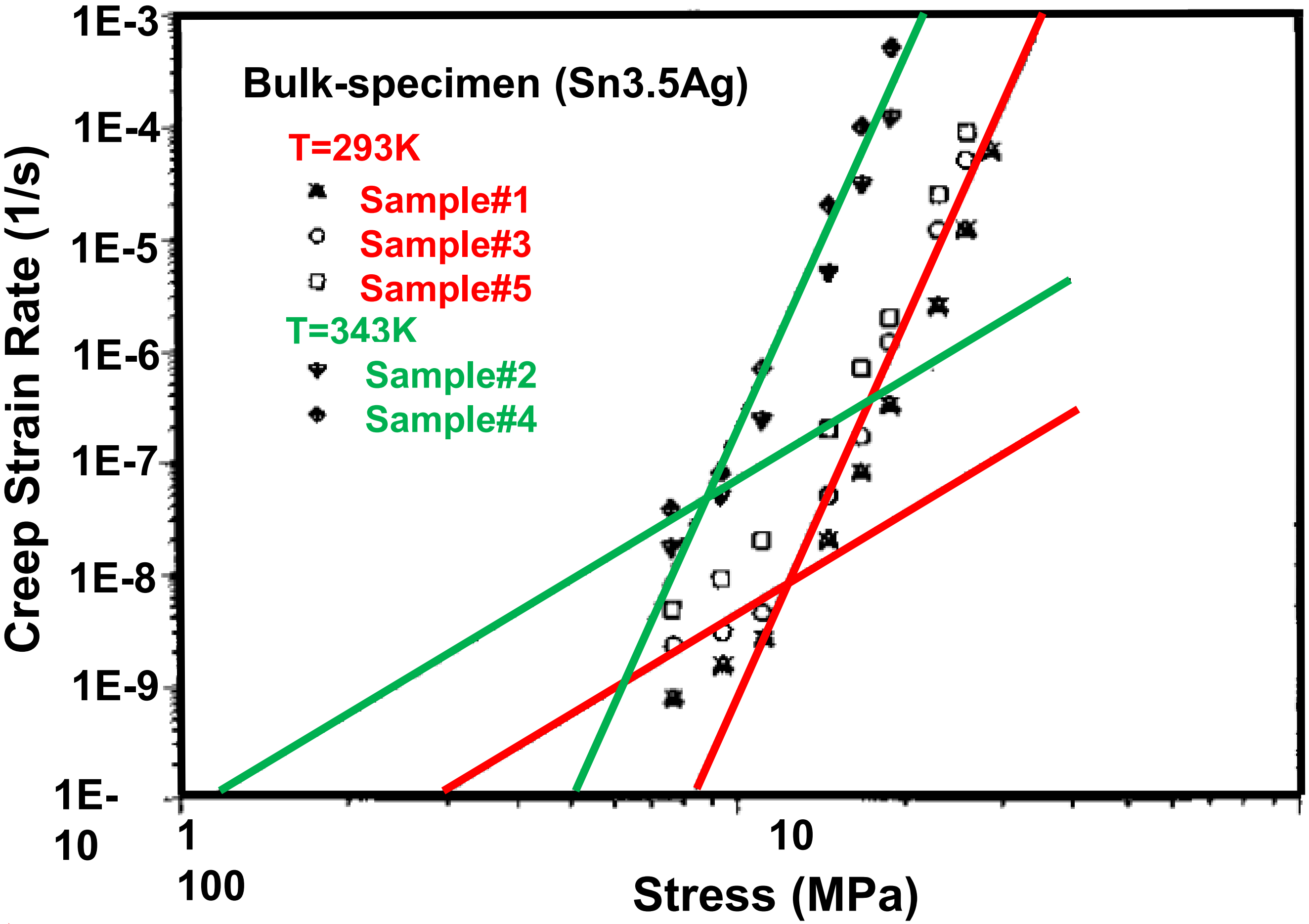
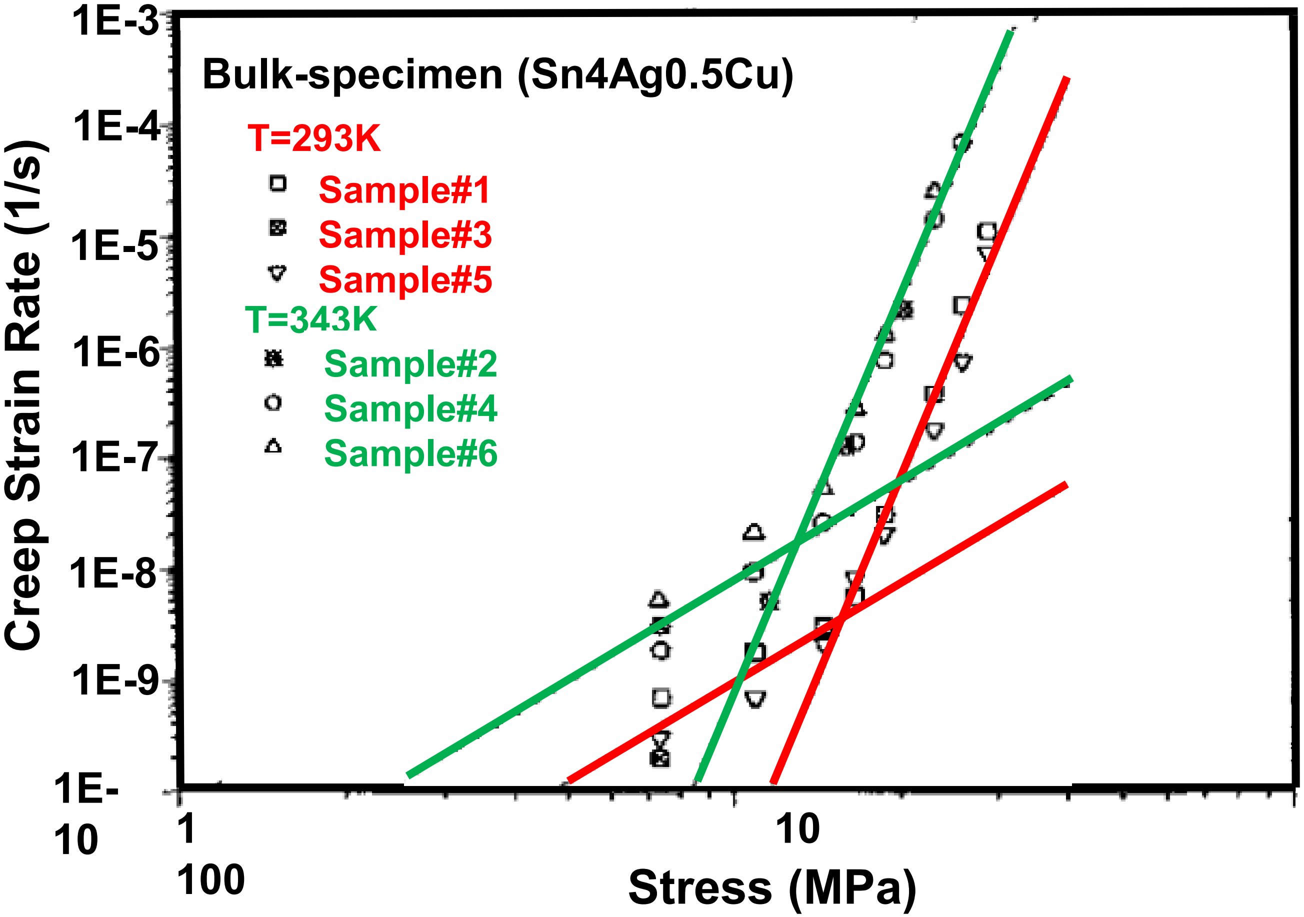
Wises' Two-Power Creep Data for Sn3.5Ag Bulk-Specimen



$A_1 = 7\text{x}10^{-4}$;
$n_1 = 3$;
$Q_1 = 46.8$ kJ/mol;
$A_2 = 2\text{x}10^{-4}$;
$n_2 = 11$;
$Q_2 = 93.1$ kJ/mol;
$\sigma_n = 1$MPa;
$R = 8.314462$ J/mol•K
T = temperature (K)
$E = 52.71 - 0.067$T(K) (GPa)
σ = Stress (MPa)

- Wiese, S., Schubert, A., Walter, H., Dudek, R., Feustel, F., Meusel, E., and Michel, B., 2001, "Constitutive Behaviour of Lead-Free Solders Vs. LeadContaining Solders - Experiments on Bulk Specimens and Flip-Chip Joints," IEEE/ECTC Proceedings, Orlando, FL, May 29–June 1, pp. 1–13.
- Wiese, S., Meusel, E., and Wolter, K., 2003, "Microstructural Dependence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders," IEEE/ECTC Proceedings, New Orleans, LA, May 27–30, pp. 197–206.
- Wiese, S., Roellig, M., and Wolter, K.-J., 2005, "Creep of Eutectic SnAgCu in Thermally Treated Solder Joints," IEEE/ECTC Proceedings, Lake Buena Vista, FL, May 31–June 3, pp. 1272–1281.
- Wiese, S., Roellig, M., Mueller, M., Bennemann, S., Petzold, M., and Wolter, K.-J., 2007, "The Size Effect on the Creep Properties of SnAgCu Solder Alloys," IEEE/ECTC Proceedings, Reno, NV, May 29–June 1, pp. 548–557.

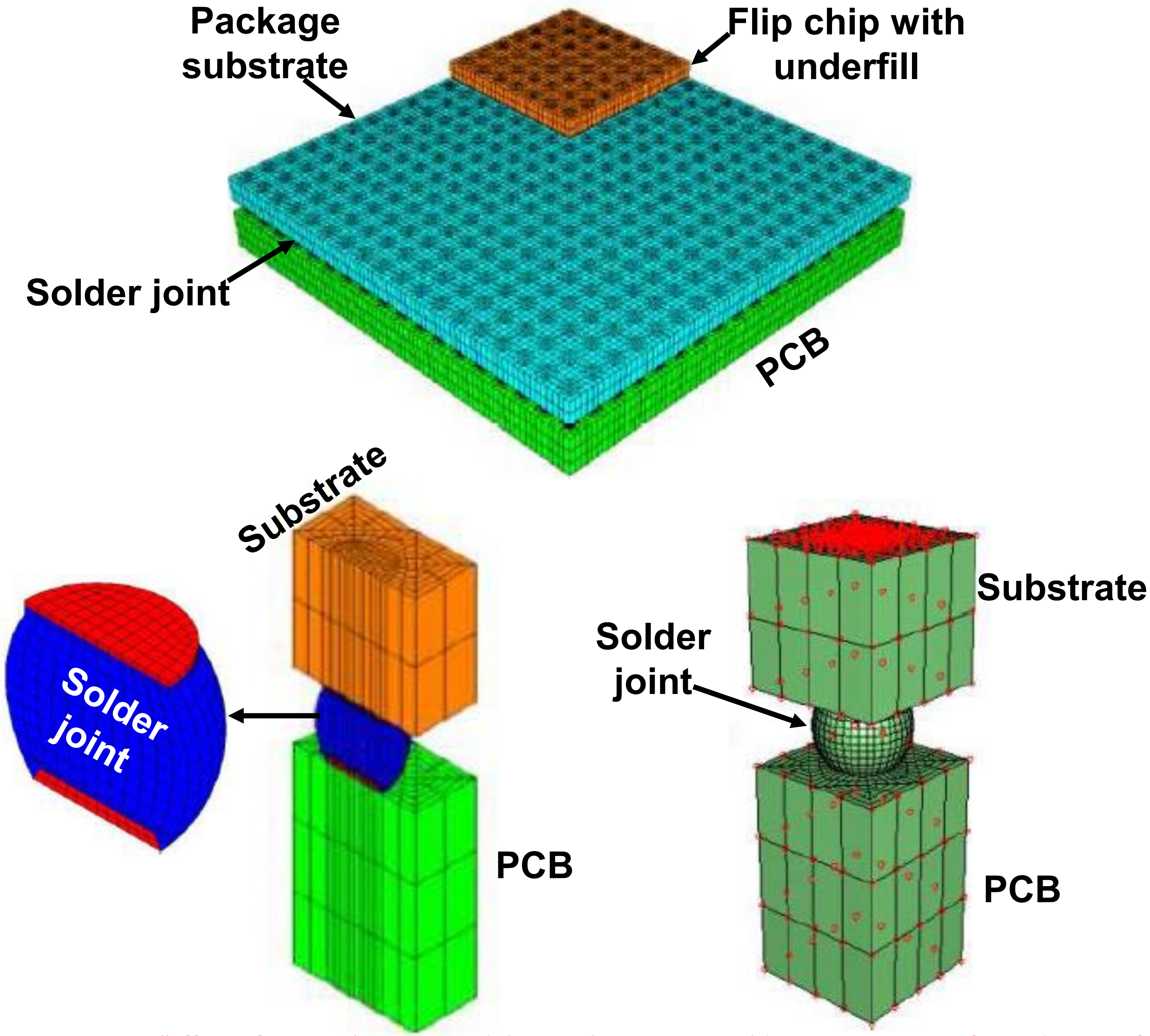
Wises' Two-Power Creep Data for Sn4Ag0.5Cu Bulk-Specimen



$A_1 = 1\text{x}10^{-6}$;
$n_1 = 3$;
$Q_1 = 34.6$ kJ/mol;
$A_2 = 1\text{x}10^{-12}$
$n_2 = 12$;
$Q_2 = 61.1$ kJ/mol;
$\sigma_n = 1$MPa;
$R = 8.314462$ J/mol•K
T = temperature (K)
$E = 62.24 - 0.075$T(K) (GPa)
σ = Stress (MPa)

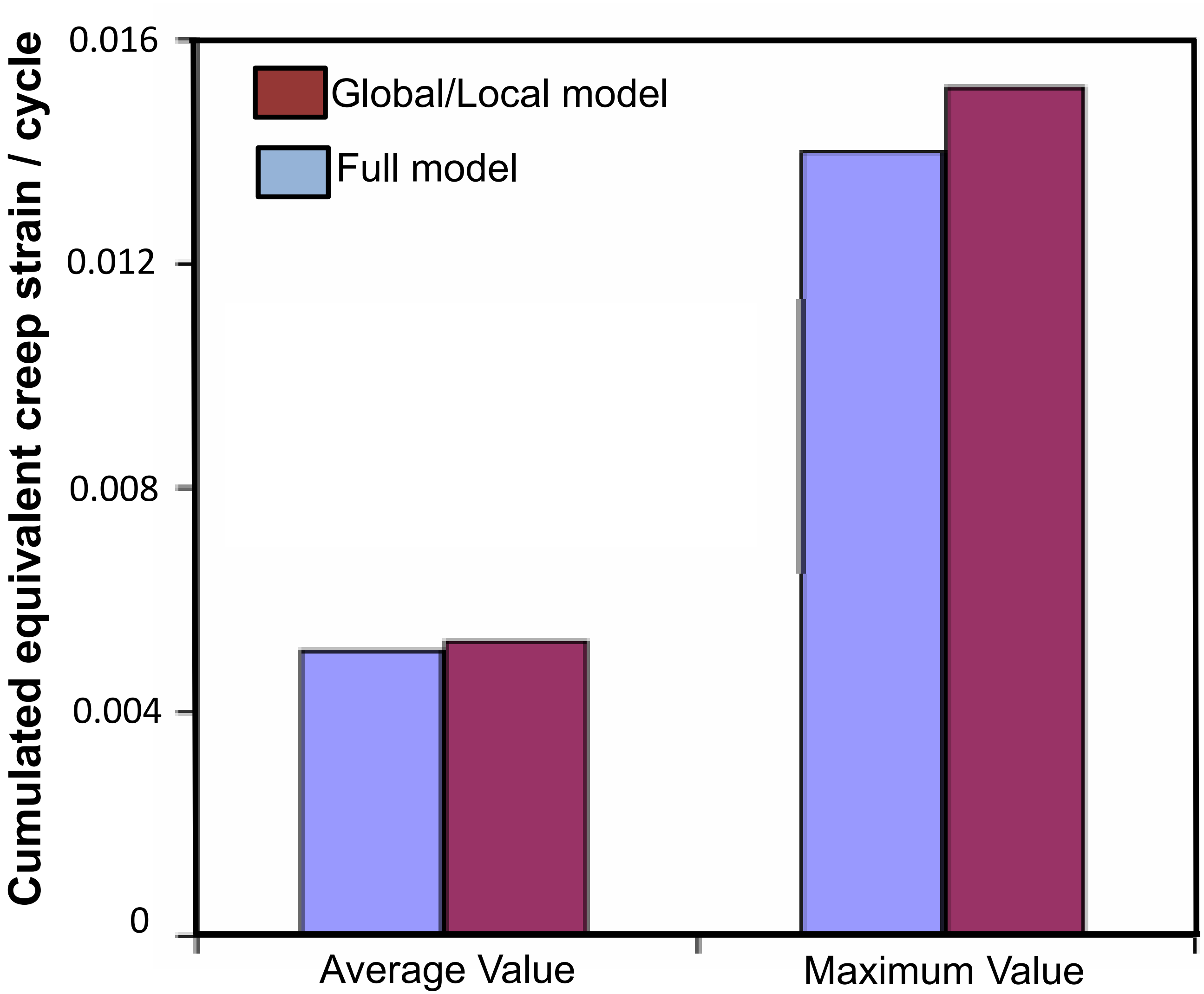
- Wiese, S., Schubert, A., Walter, H., Dudek, R., Feustel, F., Meusel, E., and Michel, B., 2001, "Constitutive Behaviour of Lead-Free Solders Vs. LeadContaining Solders - Experiments on Bulk Specimens and Flip-Chip Joints," IEEE/ECTC Proceedings, Orlando, FL, May 29–June 1, pp. 1–13.
- Wiese, S., Meusel, E., and Wolter, K., 2003, "Microstructural Dependence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders," IEEE/ECTC Proceedings, New Orleans, LA, May 27–30, pp. 197–206.
- Wiese, S., Roellig, M., and Wolter, K.-J., 2005, "Creep of Eutectic SnAgCu in Thermally Treated Solder Joints," IEEE/ECTC Proceedings, Lake Buena Vista, FL, May 31–June 3, pp. 1272–1281.
- Wiese, S., Roellig, M., Mueller, M., Bennemann, S., Petzold, M., and Wolter, K.-J., 2007, "The Size Effect on the Creep Properties of SnAgCu Solder Alloys," IEEE/ECTC Proceedings, Reno, NV, May 29–June 1, pp. 548–557.

Global/local and full models for flip chip with underfill on package substrate and then lead-free solder joints on PCB



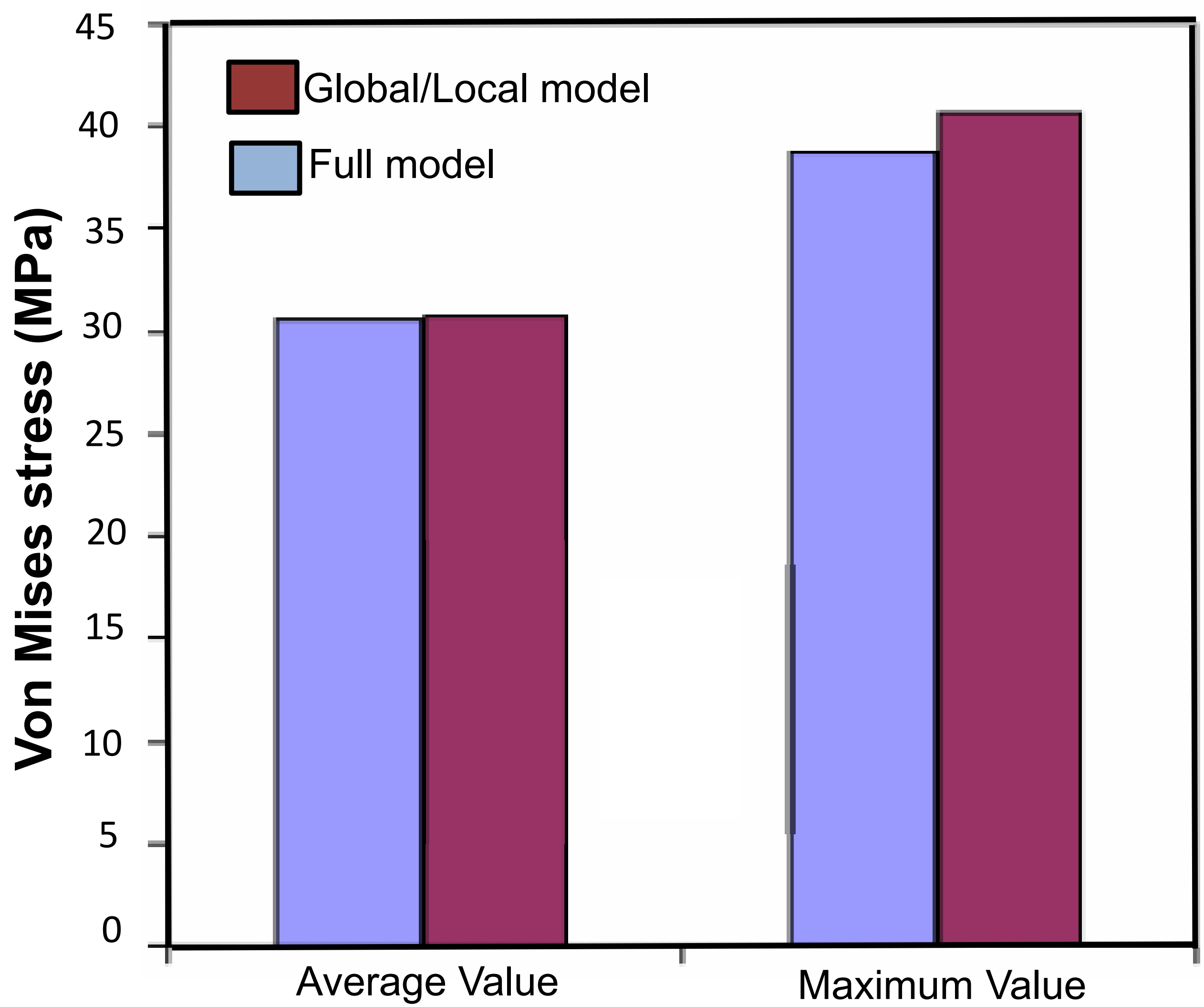
Fan, X., Pei, M., and Bhatti, P. K., 2006, "Effect of Finite Element Modeling Techniques on Solder Joint Fatigue Life Prediction of Flip-Chip BGA Packages," IEEE/ECTC Proceedings, San Diego, CA, May 30–June 2, pp. 972–980.

CEEQ per Cycle from Global/Local and Full Models



Fan, X., Pei, M., and Bhatti, P. K., 2006, "Effect of Finite Element Modeling Techniques on Solder Joint Fatigue Life Prediction of Flip-Chip BGA Packages," IEEE/ECTC Proceedings, San Diego, CA, May 30–June 2, pp. 972–980.

Mises Stress from Global/Local and Full Models



Fan, X., Pei, M., and Bhatti, P. K., 2006, "Effect of Finite Element Modeling Techniques on Solder Joint Fatigue Life Prediction of Flip-Chip BGA Packages," IEEE/ECTC Proceedings, San Diego, CA, May 30–June 2, pp. 972–980.

Garofalo Hyperbolic Sine Creep

Garofalo-Arrhenius creep constitutive equation is expressed by:

$$\frac{d\gamma}{dt} = C\left(\frac{G}{\Theta}\right)\left[\sinh\left(\omega\frac{\tau}{G}\right)\right]^{n}\exp\left(-\frac{Q}{k\Theta}\right)$$

where γ is the creep shear strain, $d\gamma/dt$ is the creep shear strain rate, t is the time, C is a material constant, G is the modulus, Θ is the absolute temperature (Kevin), ω defines the stress level at which the power law stress dependence breaks down, τ is the shear stress, n is the stress exponent, Q is the activation energy for a specific diffusion mechanism (for example, dislocation diffusion, solute diffusion, lattice self-diffusion, and grain boundary diffusion), and k is the Boltzmann's constant ($7.617\text{x}10^{-5}$eV/^{o}K). It can be rearranged by lumping certain coefficients and expressed as:

$$\frac{d\gamma}{dt} = A\left[\sinh\left(\frac{\tau}{B}\right)\right]^{n}\exp\left(-\frac{Q}{kT}\right)$$

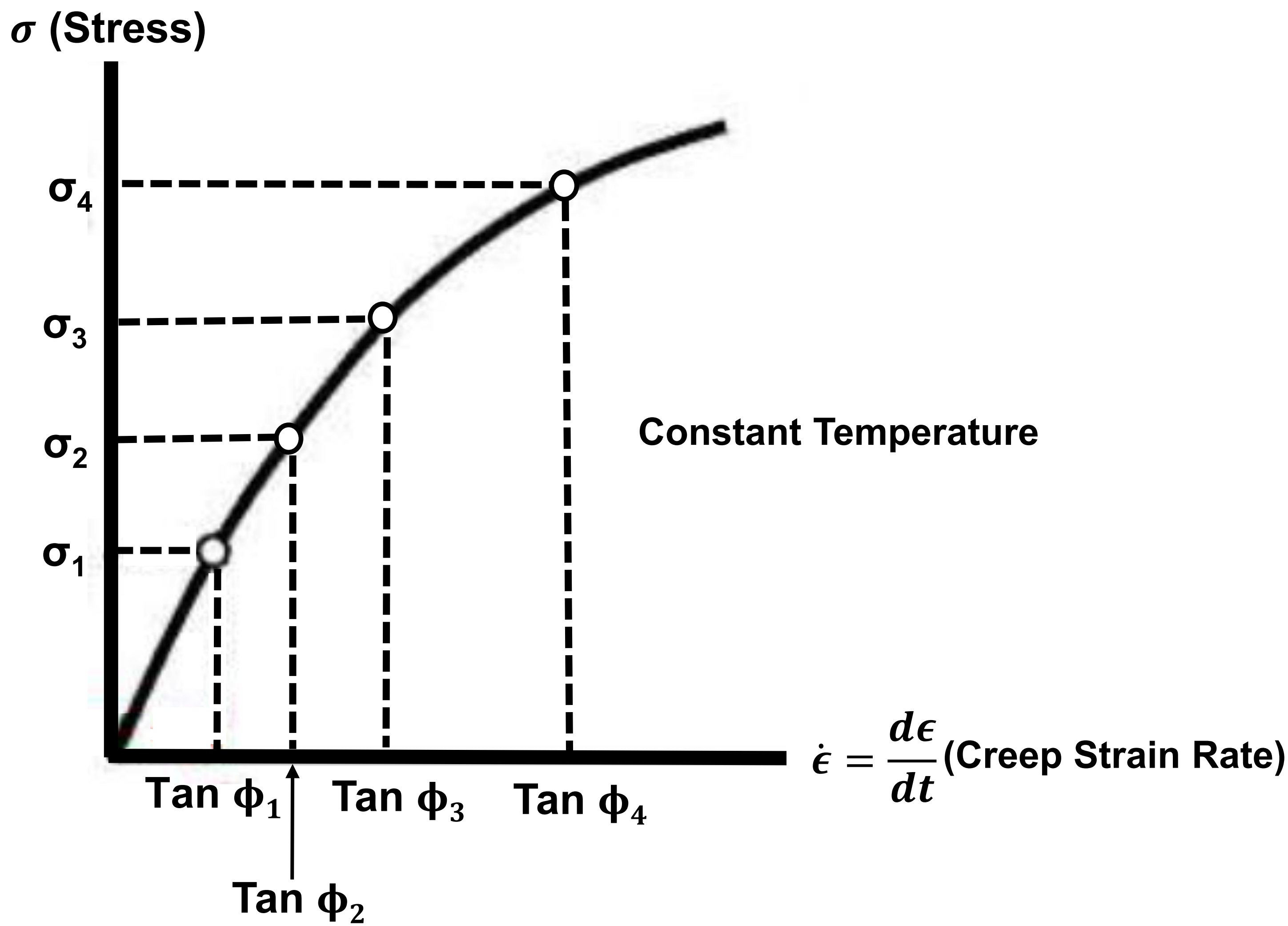
If the solder obeys the von Mises criterion, then it can can be re-written as:

$$\frac{d\varepsilon}{dt} = C_1[\sinh(C_2\sigma)]^{C_3}\exp\left(-\frac{C_4}{T}\right)$$

where the constants, A, B, n, and Q or C_1, C_2, C_3, and C_4 are determined by creep tests (curves) at various sets of constant stress and temperature. It should be noted that this form is exactly the same as the input form of the implicit creep model in ANSYS and ABAQUS. σ is the effective normal stress; τ is the shear stress; and $d\varepsilon/dt$ is the effective normal creep strain rate.

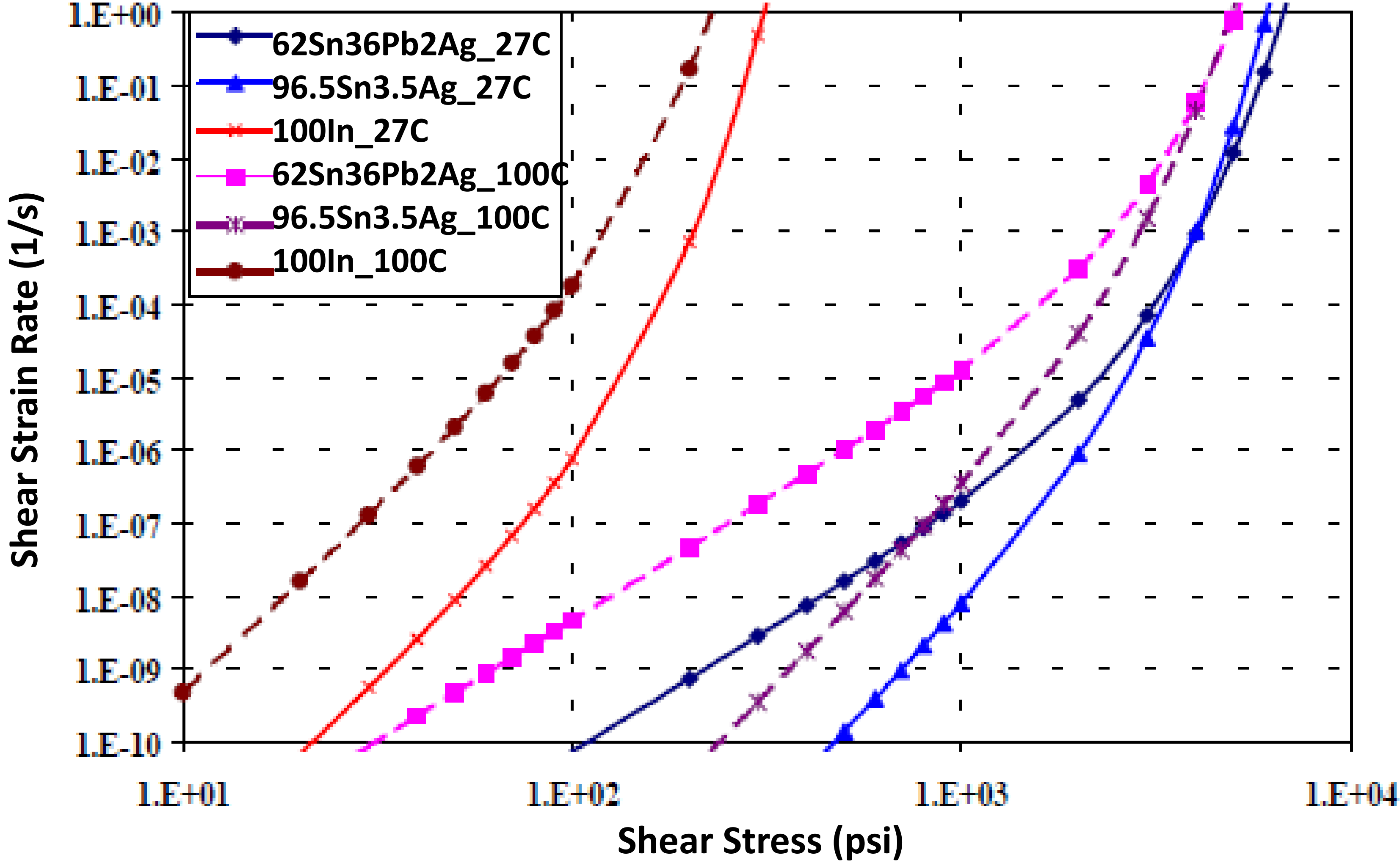
Garofalo, F., 1965, Fundamentals of Creep and Creep-Rupture in Metals, Macmillan Publishing, New York.

Stress vs. Creep Strain Rate Curve with Various Stresses at a Constant Temperature



Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

Shear Stress vs. Shear Creep Strain Rate Curves for Various Solders



Darveaux, R., and K. Banerji, "Constitutive Relations for Tin-Based-Solder Joints", *IEEE/ECTC Proceedings*, May 1992, pp. 538-551.

Parameters in the Garofalo hyperbolic sine creep constitutive equation

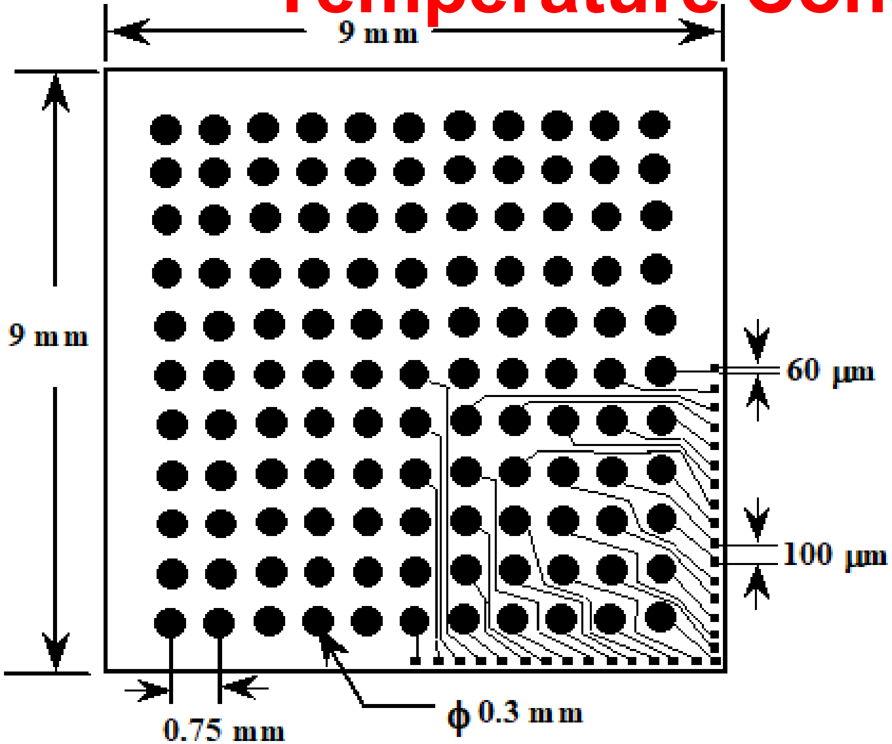
$$\frac{d\varepsilon}{dt} = C_1[\sinh(C_2\sigma)]^{C_3}\exp\left(-\frac{C_4}{T}\right)$$

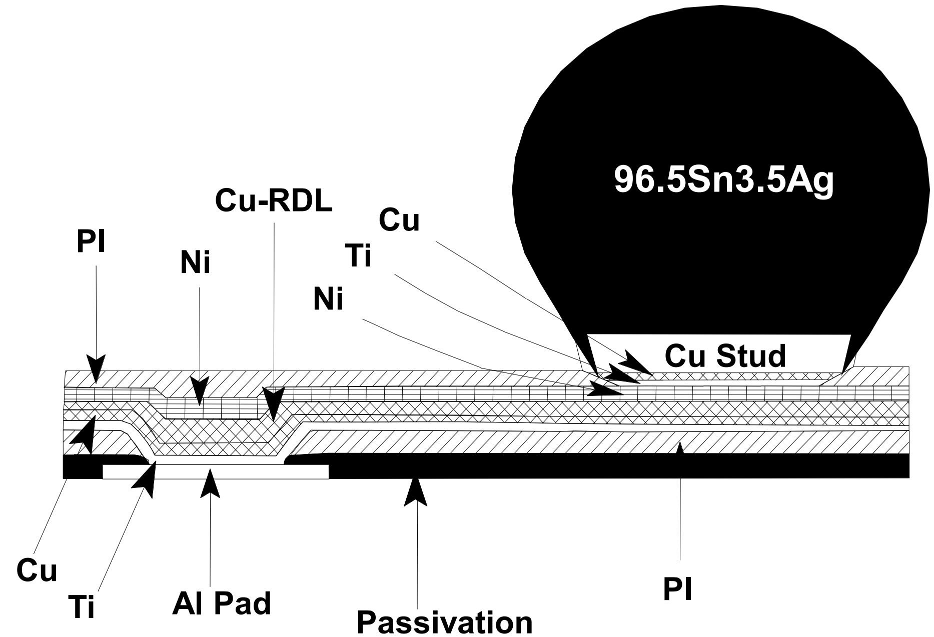
	C_1	C_2	C_3	C_4
Sn3.5Ag [66,67]	18(553-T)/T	1/(6386–11.55T)	5.5	5802
Sn3.9Ag0.6Cu [36]	441000	0.005	4.2	5412
Sn3.8Ag0.7Cu, Sn3.5Ag0.5Cu, Sn3.5Ag0.75Cu [72]	277,984	0.02447	6.41	6500
Sn4Ag0.5Cu [71]	0.17	0.14	4.2	6875
Sn3Ag0.5Cu [74]	2631	0.0453	5	7096
Sn(3.5–3.9)Ag(0.5–0.8)Cu [89]	500,000	0.01	5	5800
100In [66,67]	40647(593-T)/T	1/(274–0.47T)	5	8356
Sn52In [83,112]	2.54×10^{11}(593–T)/T	1/(5235–8.65T)	3.11	9705
Au20Sn [70]	4.62×10^{15}	2×10^{-5}	2.07	12268
Sn3.8Ag0.7Cu0.03Ce [103]	284,000	0.024	6.1	6400

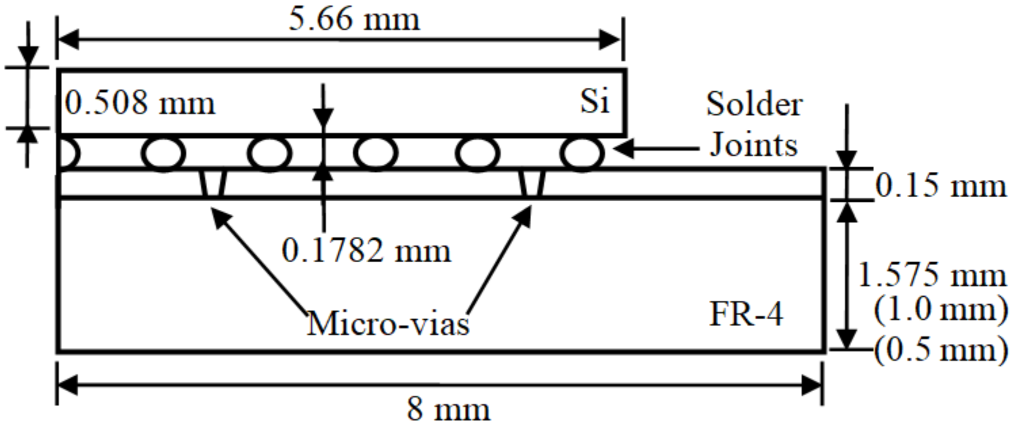
For Sn3.5Ag, 100In, and Sn52In, σ is in psi. For all other solder alloys, σ is in MPa. For all solder alloys, $d\varepsilon/dt$ is in 1/s, and T is in Kelvin.

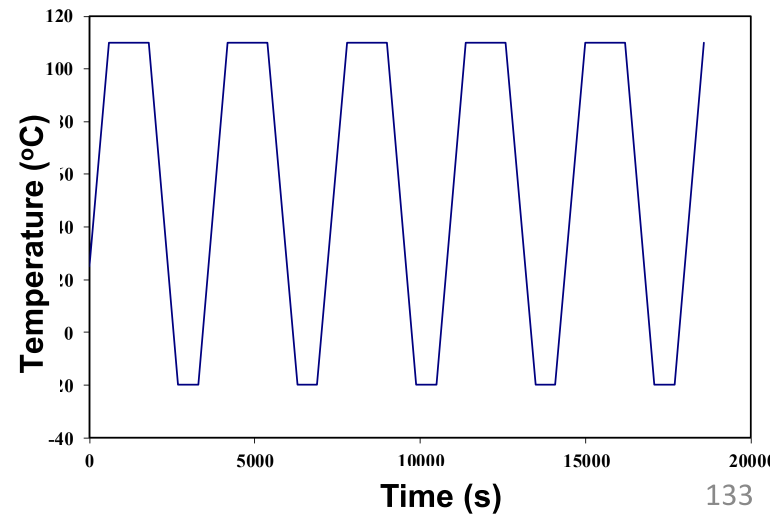
[66] Darveaux, R., and Banerji, K., 1992, "Constitutive Relations for Tin-Based Solder Joints," IEEE/ECTC Proceedings, San Diego, CA, May 18–20, pp. 538–551.
[36] Lau, J., Dauksher, W., and Vianco, P., 2003, "Acceleration Models, Constitutive Equations and Reliability of Lead-Free Solders and Joints," IEEE/ECTC Proceedings, New Orleans, LA, May 27–30, pp. 229–236.
[72] Schubertt, A., Dudek, R., Auerswald, E., Gollhardt, A., Michel, B., and Reicbl, H., 2003, "Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation," IEEE/ECTC Proceedings, New Orleans, LA, May 27–30, pp. 603–610.
[71] Wang, Q., Johnson, W., Ma, H., Gale, W., and Lindahl, D., 2005, "Properties of Lead Free Solder Alloys as a Function of Composition Variation," 10th Electronic Circuit World Conversion Conference, Anaheim, CA, Mar. 12–15, pp. 1–18.
[74] Vianco, P., 2005, "Fatigue and Creep of Pb-Free Solder Alloys: Fundamental Properties," Lead-Free Soldering, D. Shangguan, ed., ASM International, Cleveland, OH, pp. 67–106.
[89] Lau, J. H., and Dauksher, W., 2004, "Creep Constitutive Equations of Sn(3.5- 3.9)wt%Ag(0.5-0.8)wt%Cu Lead-Free Solder Joints," MicroMaterails and Nanomaterials, B. Michel, ed., pp. 54–62.
[83] Lau, J. H., Mei, Z., Pang, S., Amsden, C., Rayner, J., and Pan, S., 2002, "Creep Analysis and Thermal-Fatigue Life Prediction of the Lead-Free Solder Sealing Ring of a Photonic Switch," ASME J. Electron. Packag., 124(4), pp. 403–410.
[112] i, Z., and Morris, J., 1992, "Superplastic Creep of Low Melting Point Solder Joints," J. Electron. Mater., 21(4), pp. 401–407.
[70] Zhang, G., Jing, H., Xu, L., Wei, J., and Han, Y., 2009, "Creep Behavior of Eutectic 80Au/20Sn Solder Alloy," J. Alloys Compd., 476(1–2), pp. 138–141.
[103] Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.

WLCSP on PCB with Microvias. Temperature Condition for Simulation.



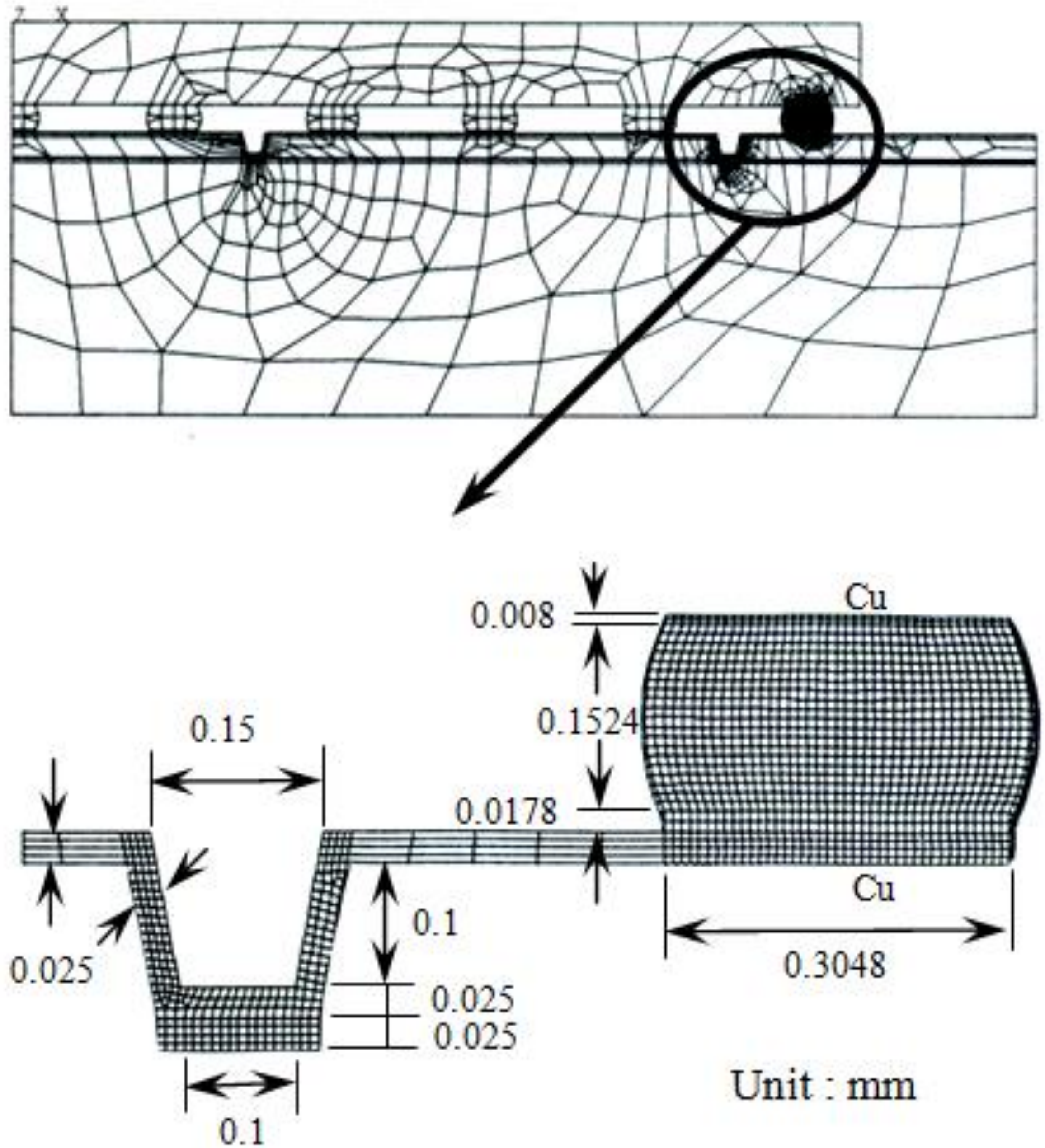






Lau, J. H., and Lee, R., 2002, "Modeling and Analysis of 96.5Sn-3.5Ag LeadFree Solder Joints of Wafer Level Chip Scale Package (WLCSP) on Build-Up Microvia Printed Circuit Board," IEEE Trans. Electron. Packag. Manuf., 25(1), pp. 51–58

Dimensions of the Microvia and Sn3.5Ag Solder Joint



Lau, J. H., and Lee, R., 2002, "Modeling and Analysis of 96.5Sn-3.5Ag LeadFree Solder Joints of Wafer Level Chip Scale Package (WLCSP) on Build-Up Microvia Printed Circuit Board," IEEE Trans. Electron. Packag. Manuf., 25(1), pp. 51–58

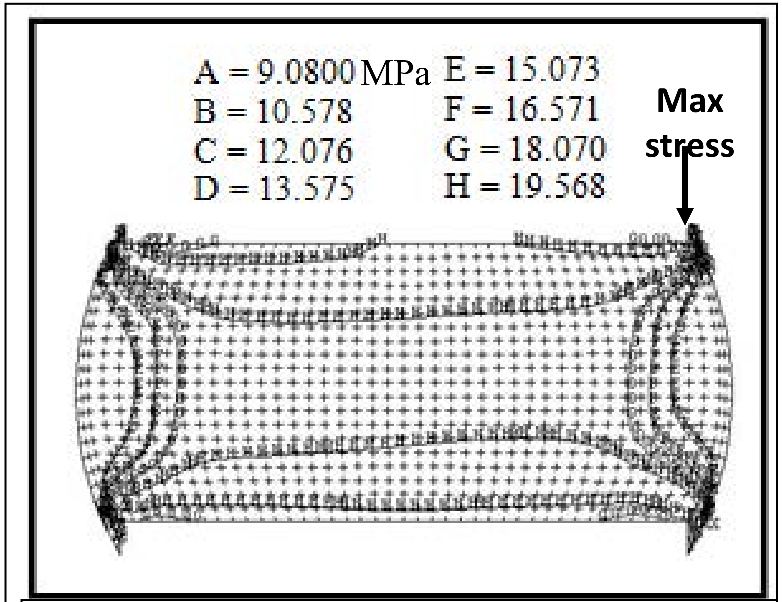
Material Properties of the WLCSP on PCB with Microvias Assembly

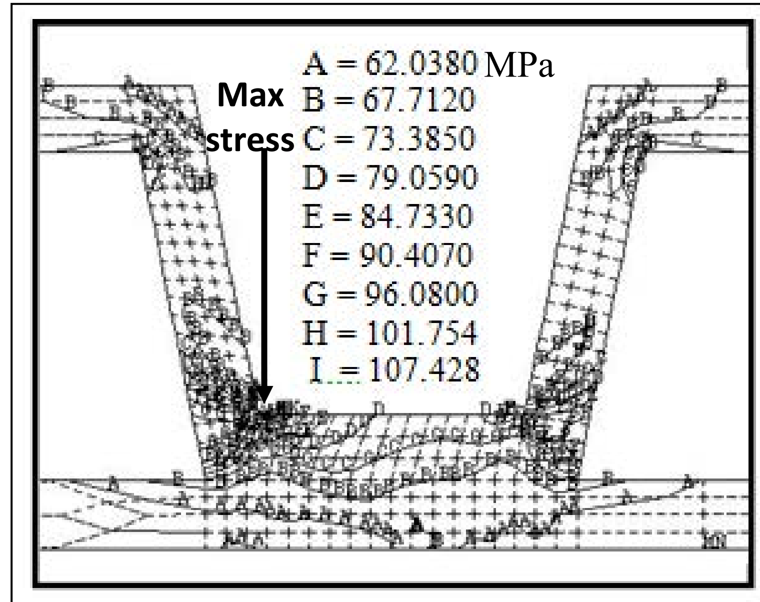
Material	Young's Modulus (MPa)	Poisson's Ratio	CTE (ppm/^oC)
Sn3.5Ag	$52708 - 67.14T - 0.06T^2$	0.4	$21.85 + 0.02T$
Underfill	$9292 - 35.4T$	0.35	$31.04 + 0.09T$
Si	131000	0.3	2.8
FR-4	22000	0.28	18
Copper	76000	0.35	17
Build-up resin	20000	0.3	50

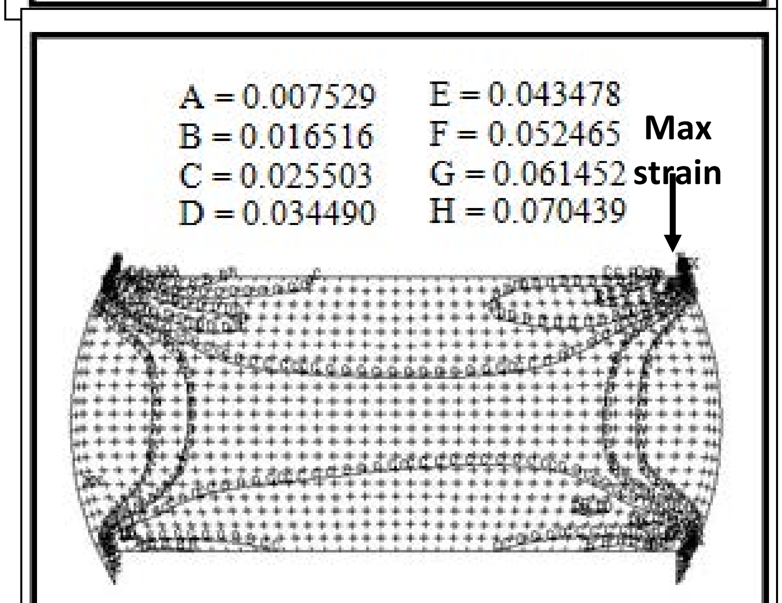
T is temperature (^oC)

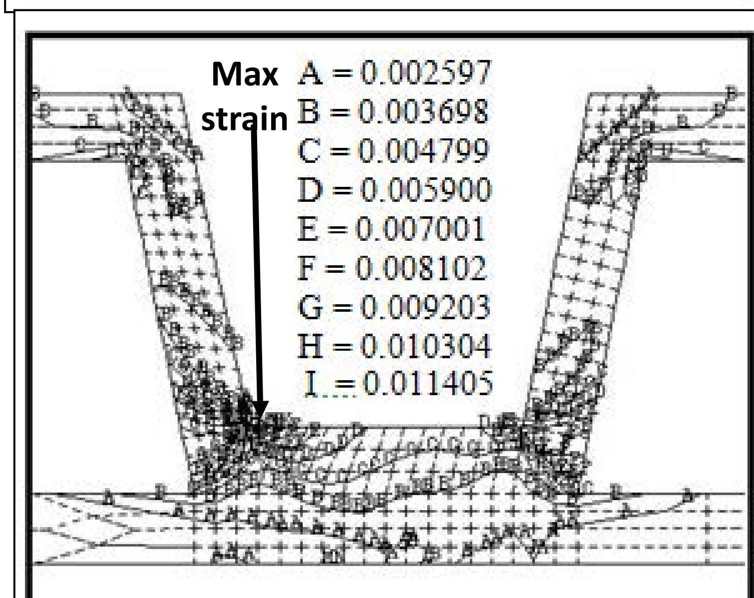
Lau, J. H., and Lee, R., 2002, "Modeling and Analysis of 96.5Sn-3.5Ag LeadFree Solder Joints of Wafer Level Chip Scale Package (WLCSP) on Build-Up Microvia Printed Circuit Board," IEEE Trans. Electron. Packag. Manuf., 25(1), pp. 51–58

Stress and Strain Contours at the Corner Solder Joint and Microvia



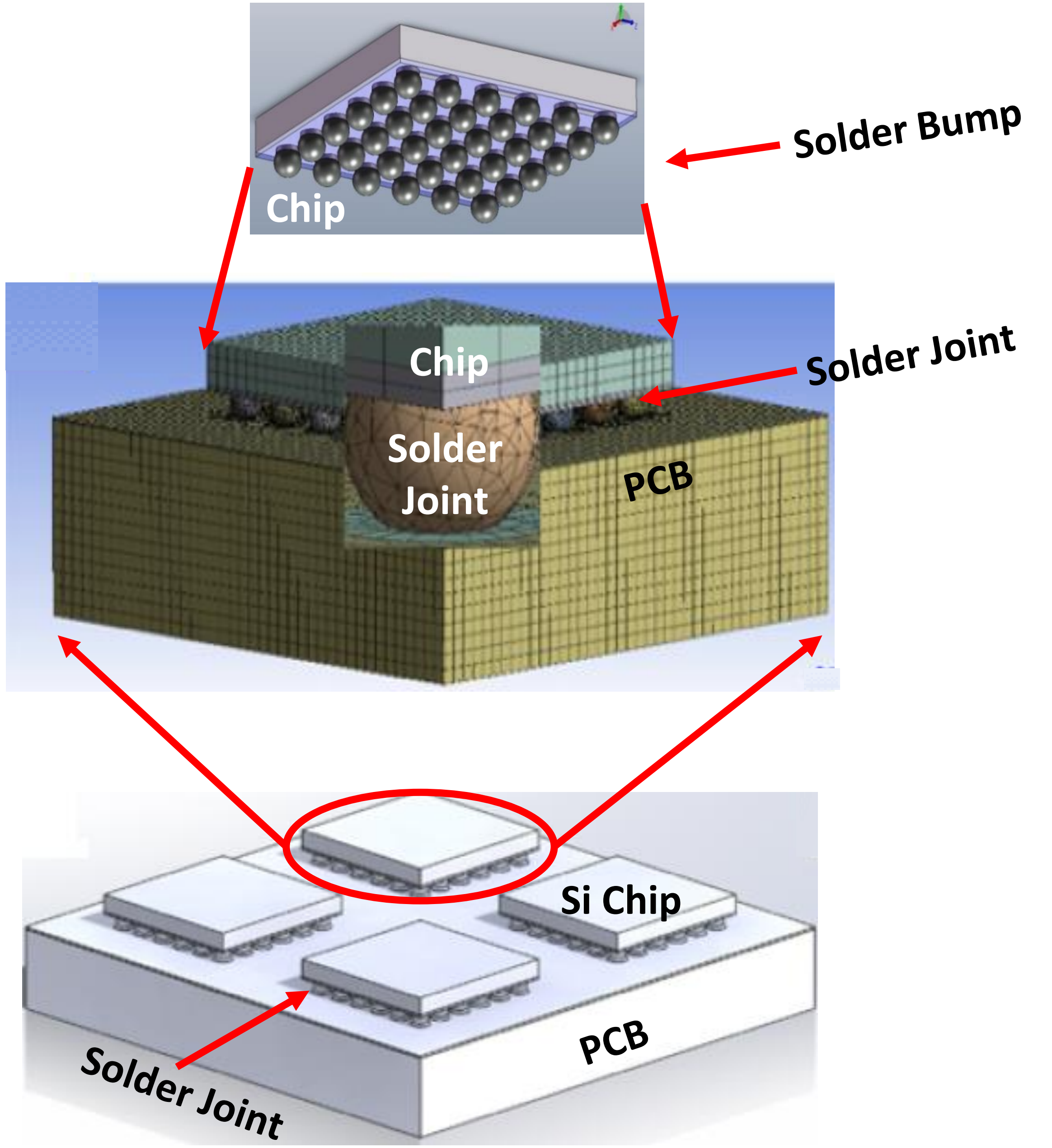






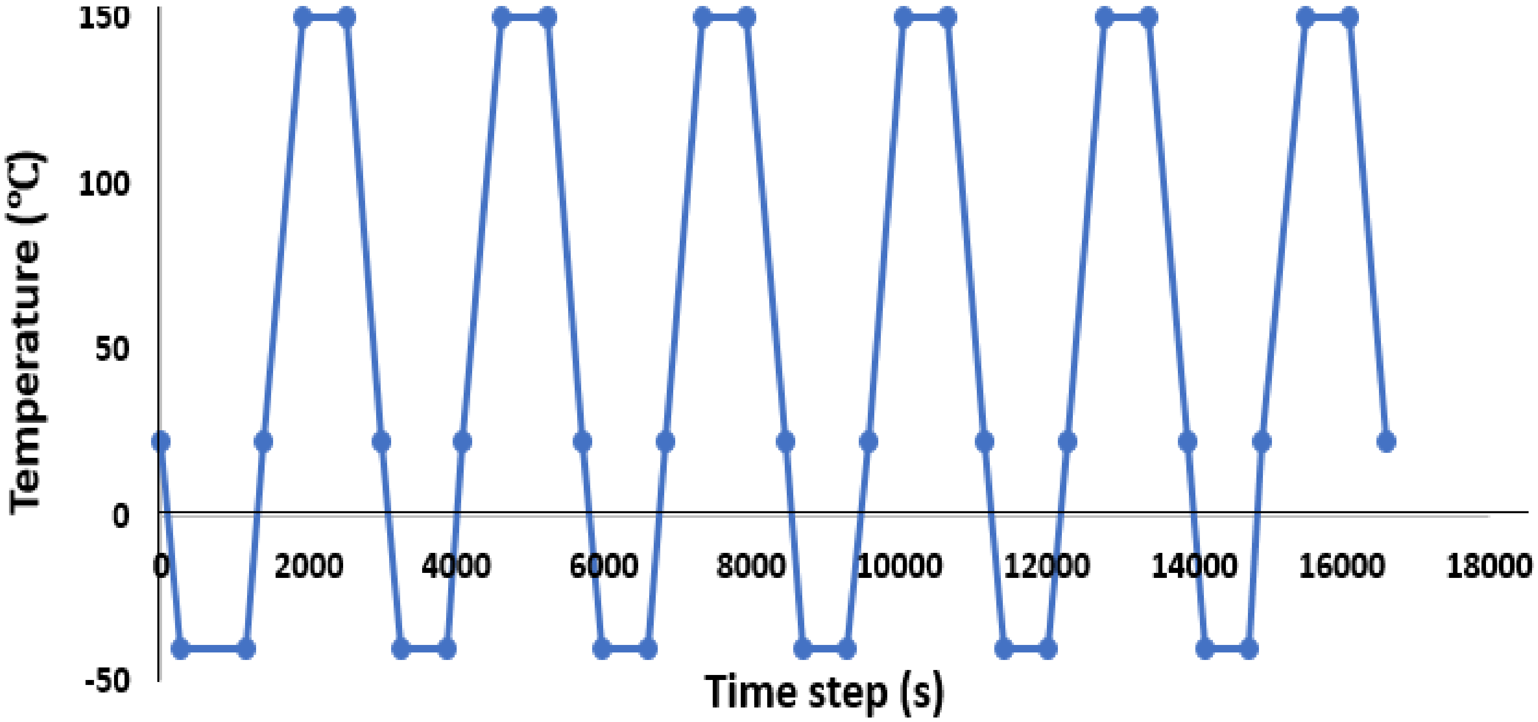
Lau, J. H., and Lee, R., 2002, "Modeling and Analysis of 96.5Sn-3.5Ag LeadFree Solder Joints of Wafer Level Chip Scale Package (WLCSP) on Build-Up Microvia Printed Circuit Board," IEEE Trans. Electron. Packag. Manuf., 25(1), pp. 51–58

Heterogeneous Integration of Four Chips on a PCB



Depiver, J., Mallik, S., and Amalu, E., 2019, "Creep Response of Various Solders Used in Soldering Ball Grid Array (BGA) on Printed Circuit Board (PCB)," Proceedings of the World Congress on Engineering and Computer Science (WCECS), San Francisco, CA, Oct. 22–24, pp. 1–10

Temperature Profile for Finite Element Simulation



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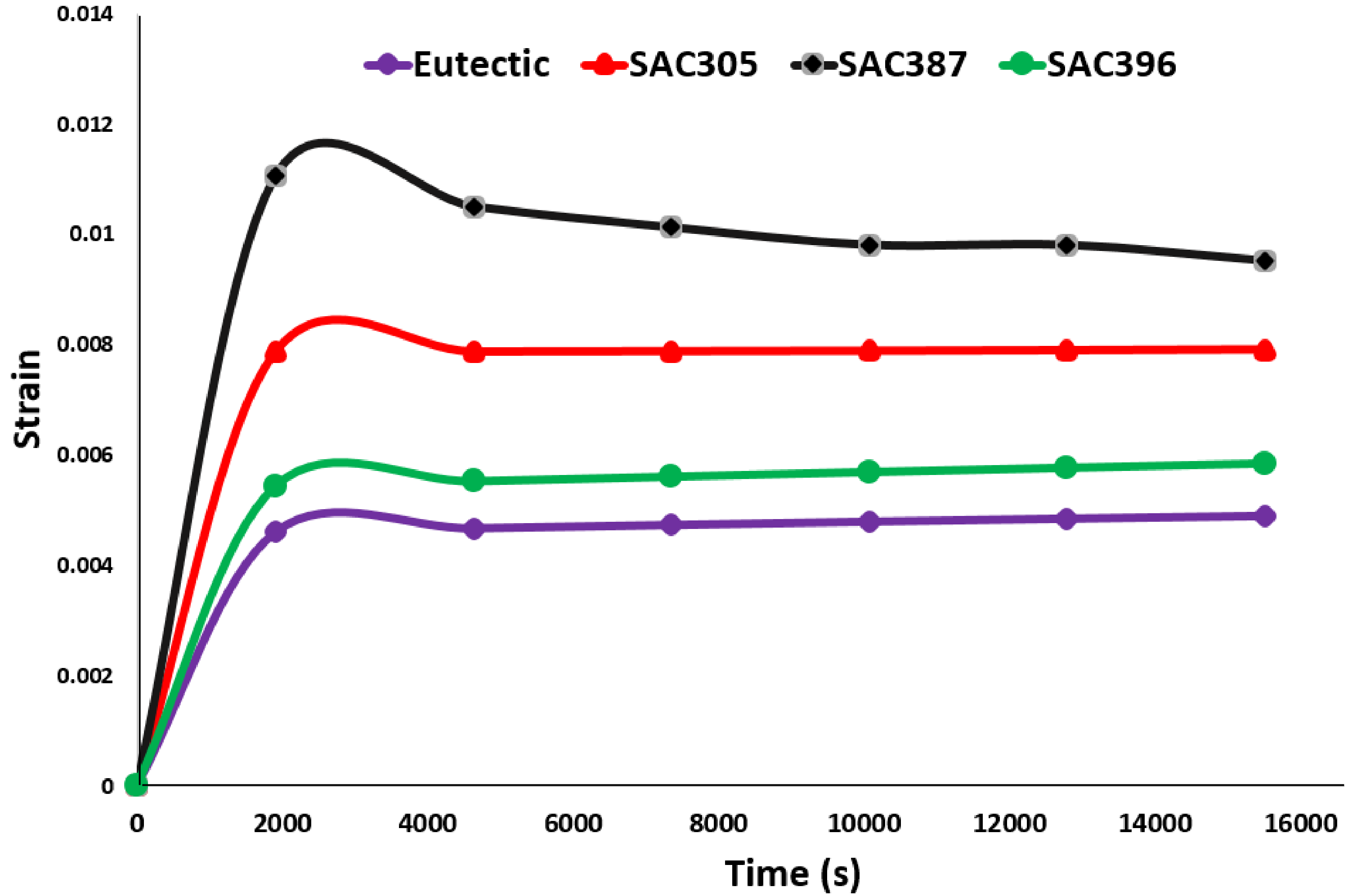
Strain Time-History for SAC305, SAC387, and SAC396 Solder Joints



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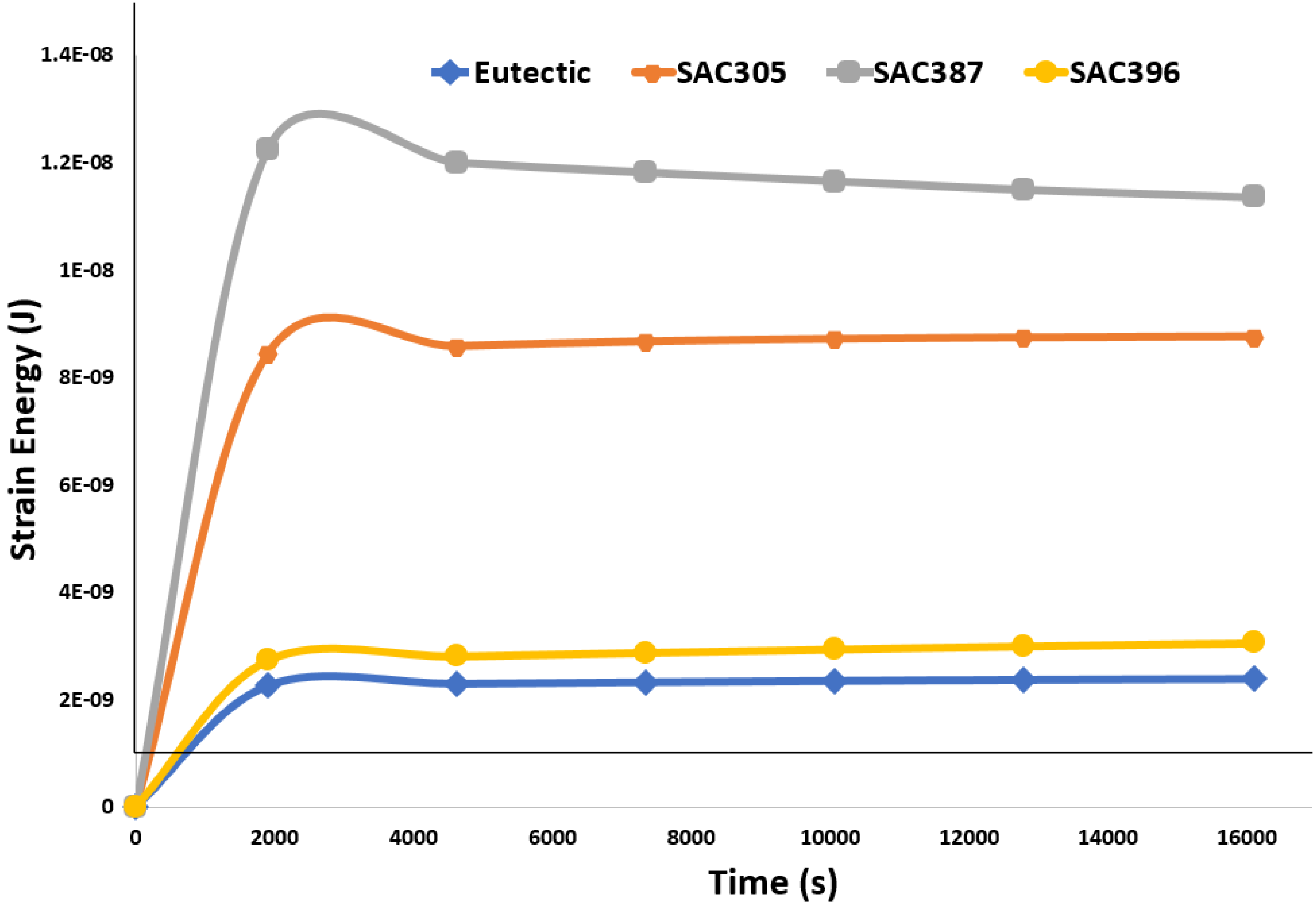
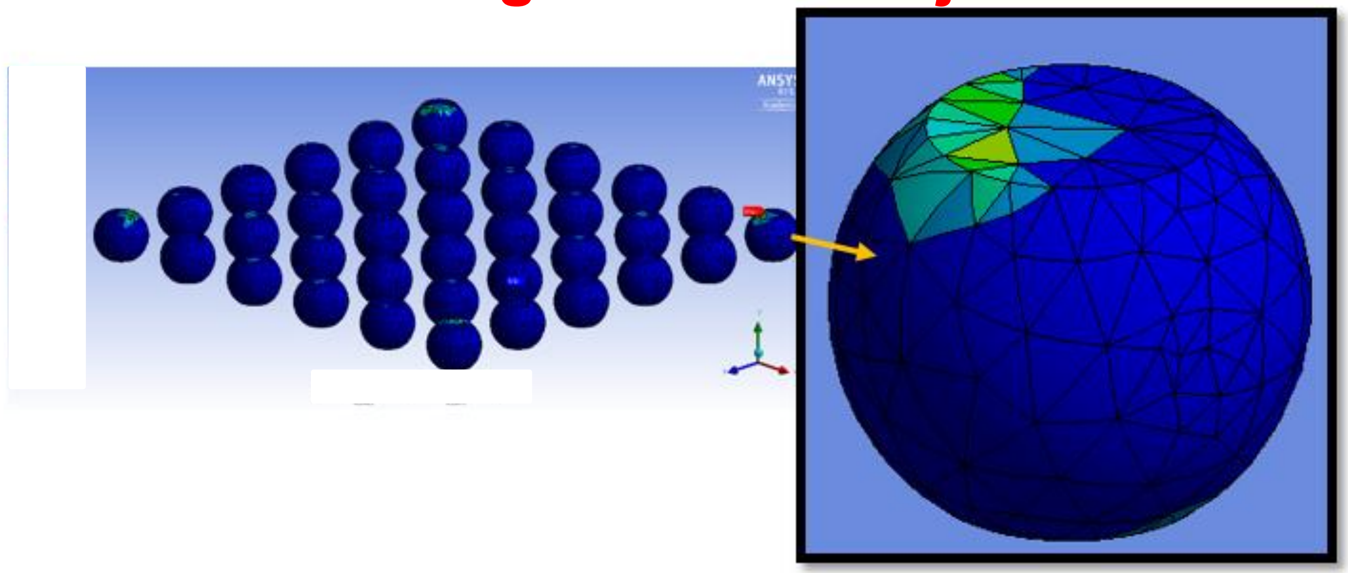
Strain Energy Time-History for SAC305, SAC387, and SAC396 Solder Joints



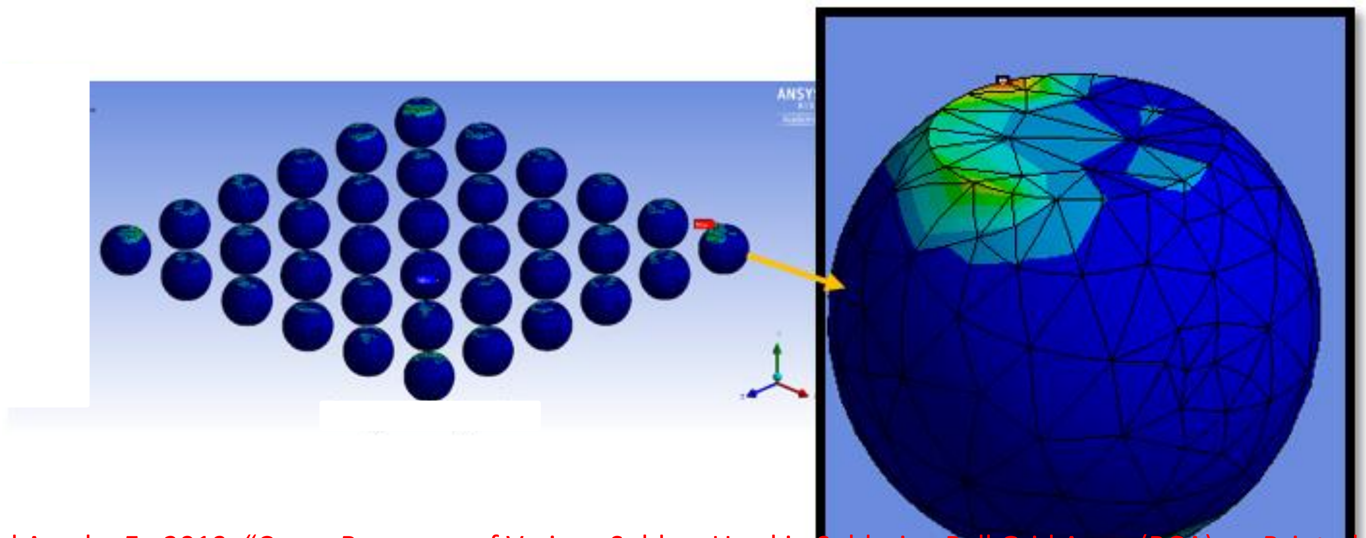
Depiver, J., Mallik, S., and Amalu, E., 2019, "Creep Response of Various Solders Used in Soldering Ball Grid Array (BGA) on Printed Circuit Board (PCB)," Proceedings of the World Congress on Engineering and Computer Science (WCECS), San Francisco, CA, Oct. 22–24, pp. 1–10

(a) Maximum strain energy contours of the Sn3.9Ag0.5Cu solder joint. (b) Maximum equivalent total strain contours of the Sn3.9Ag0.5Cu solder joint.

(a)

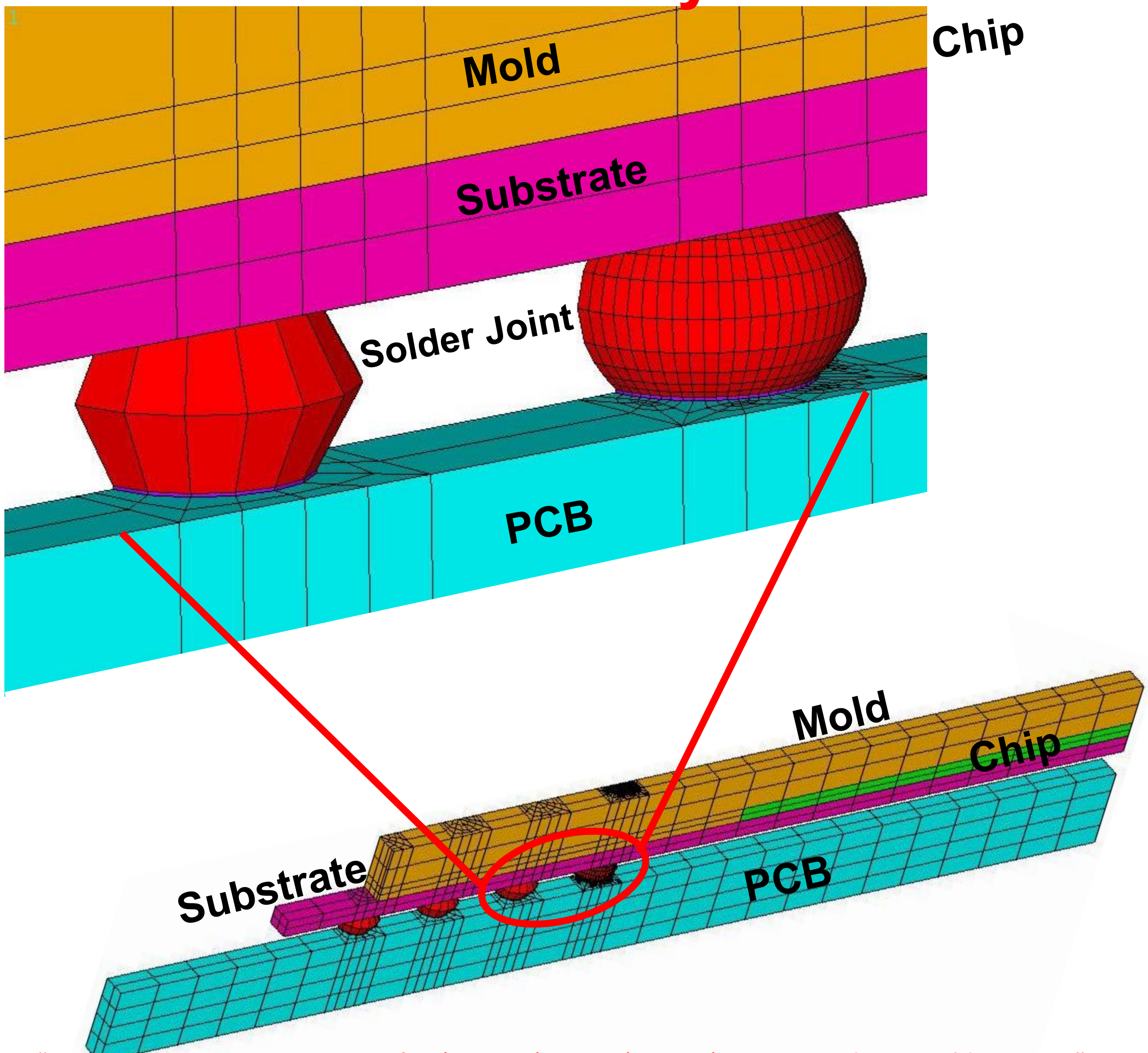


(b)



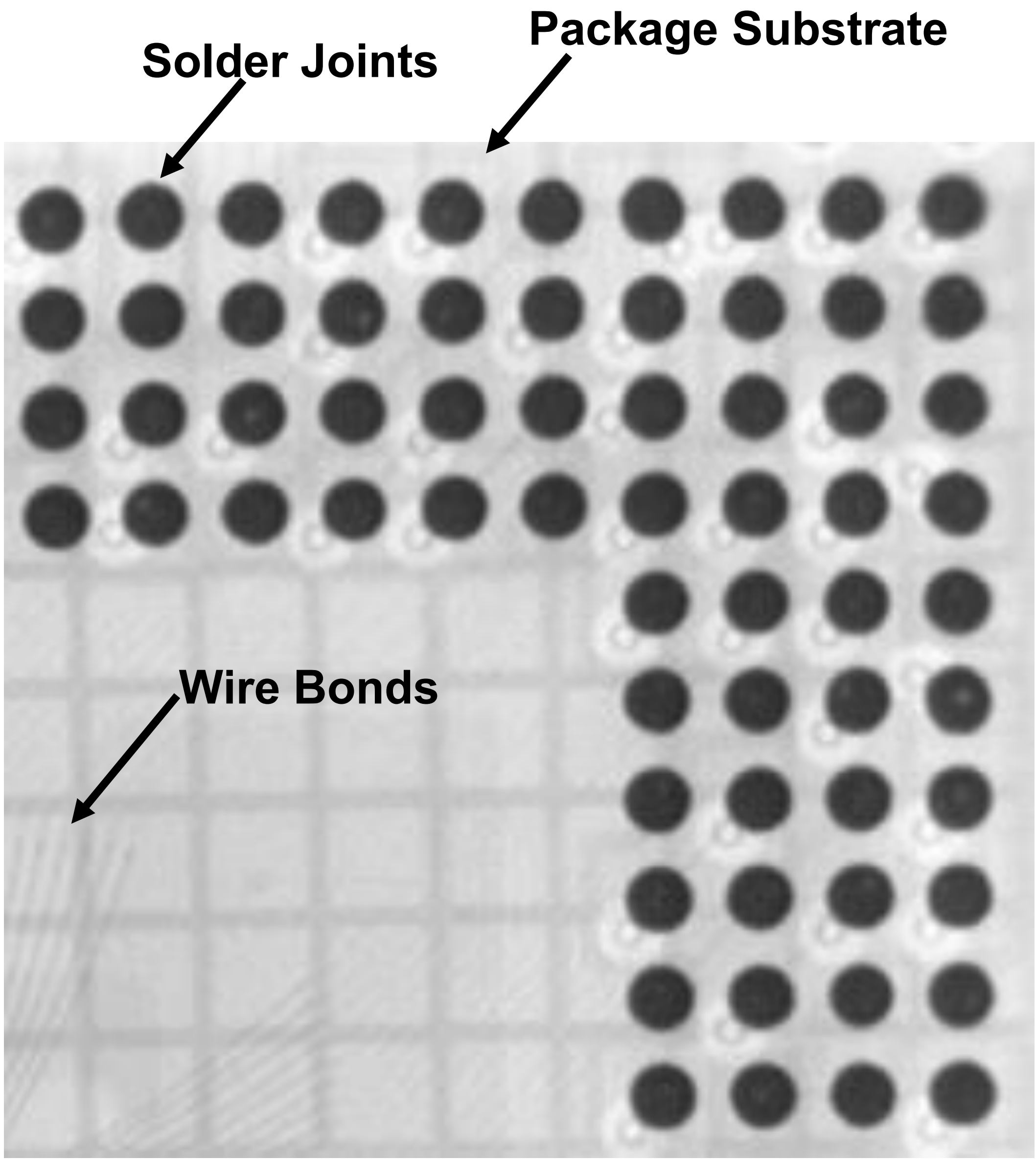
Depiver, J., Mallik, S., and Amalu, E., 2019, “Creep Response of Various Solders Used in Soldering Ball Grid Array (BGA) on Printed Circuit Board (PCB),” Proceedings of the World Congress on Engineering and Computer Science (WCECS), San Francisco, CA, Oct. 22–24, pp. 1–10

3D Finite Element Modeling of the 256-pin PBGA PCB Assembly

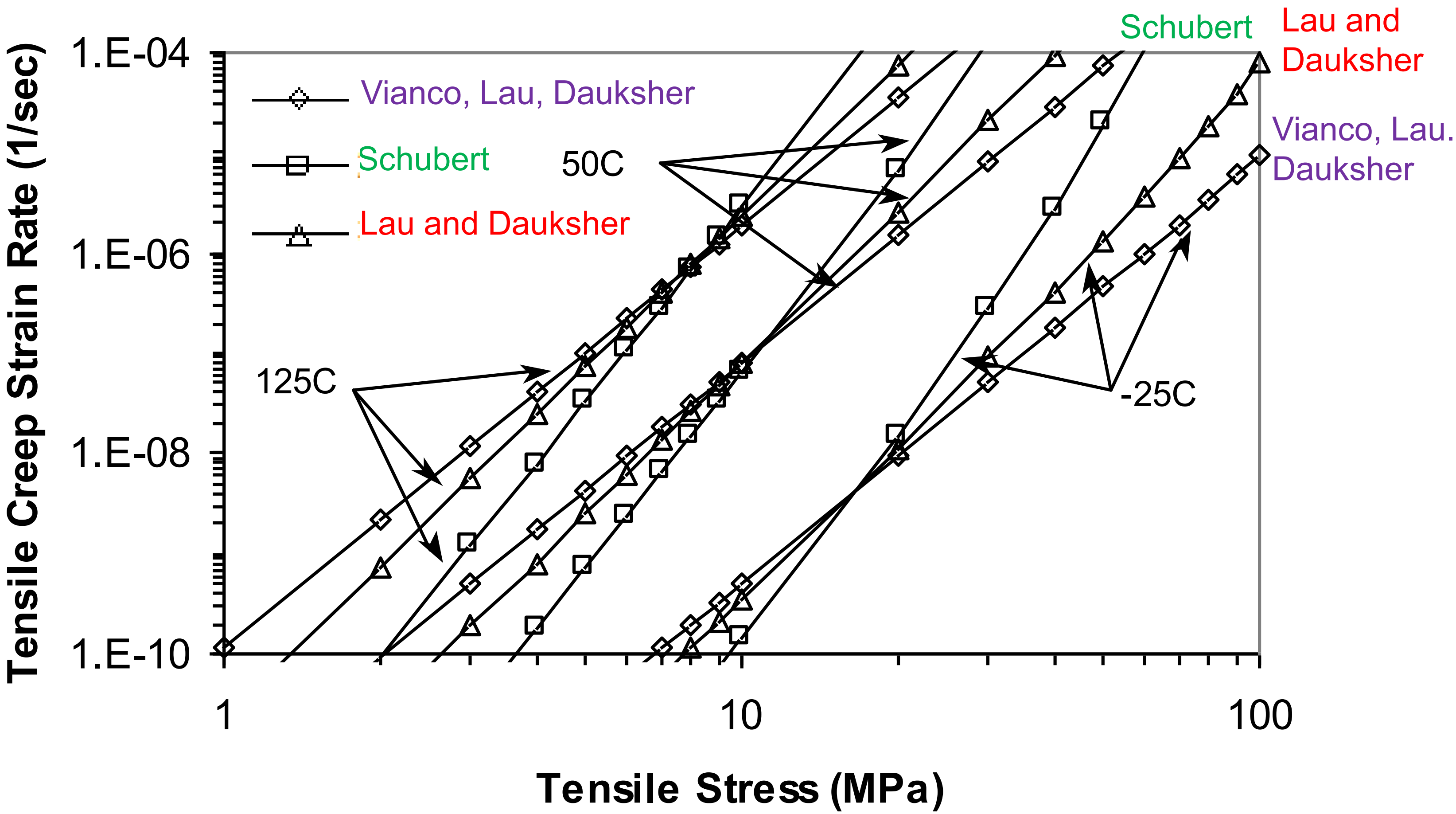


Lau, J. H., and Dauksher, W., 2004, "Creep Constitutive Equations of Sn(3.5- 3.9)wt%Ag(0.5-0.8)wt%Cu Lead-Free Solder Joints," MicroMaterails and Nanomaterials, B. Michel, ed., pp. 54–62.

X-ray of one Quarter of a 256-pin PBGA PCB Assembly

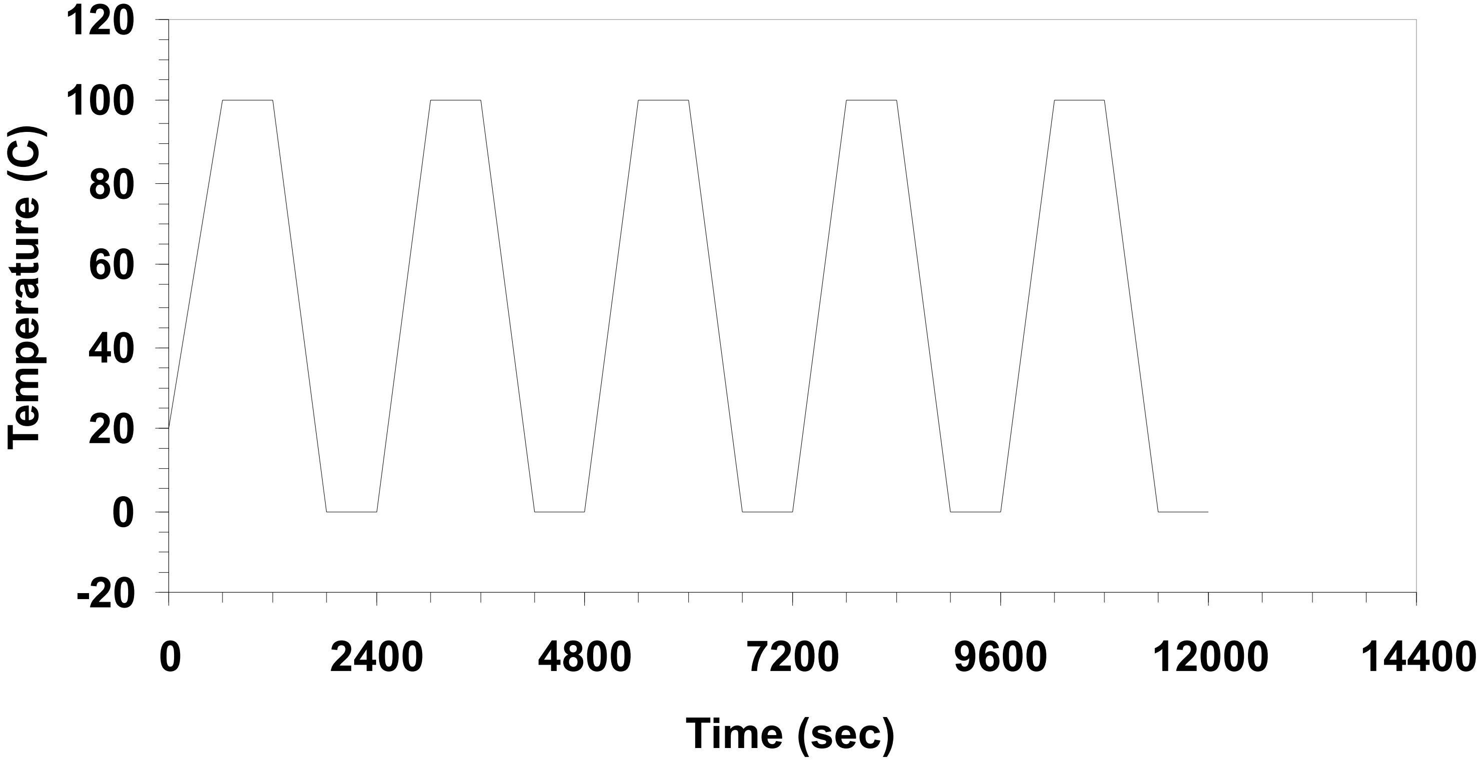


Stress vs. Creep Strain Rate Curves (at -25°C, 50°C, and 125°C)



Lau, J. H., and Dauksher, W., 2004, "Creep Constitutive Equations of Sn(3.5- 3.9)wt%Ag(0.5-0.8)wt%Cu Lead-Free Solder Joints," MicroMaterails and Nanomaterials, B. Michel, ed., pp. 54–62.

Temperature Condition for Finite Element Simulation



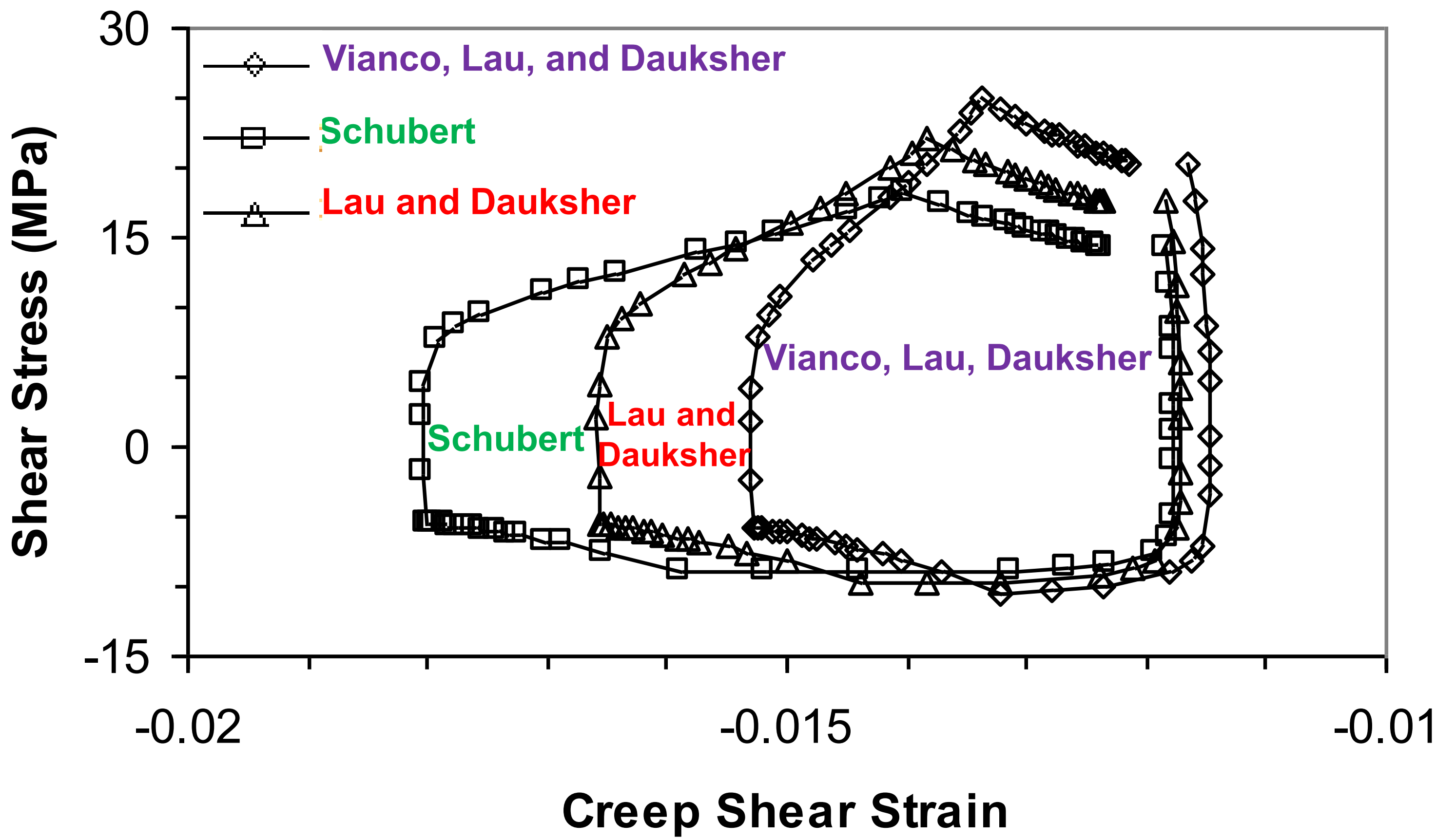
Lau, J. H., and Dauksher, W., 2004, "Creep Constitutive Equations of Sn(3.5- 3.9)wt%Ag(0.5-0.8)wt%Cu Lead-Free Solder Joints," MicroMaterails and Nanomaterials, B. Michel, ed., pp. 54–62.

Material Properties of the 256-pin PBGA PCB Assembly

Materials	E (GPa)	α (ppm/ºC)	v	C_1	C_2	C_3	C_4
PC board	27	18	0.39	-	-	-	-
Copper pads	76	17	0.35	-	-	-	-
Laminate substrate	27	18	0.39	-	-	-	-
Die	167	2.54	0.28	-	-	-	-
Overmold	13	15	0.30	-	-	-	-
[36]	49 - 0.07T	21.301 + 0.017T	0.35	441000	.005	4.2	5412
[72]	49 - 0.07T	21.301 + 0.017T	0.35	277984	.025	6.41	6500
[89]	49 - 0.07T	21.301 + 0.017T	0.35	500000	.01	5	5800

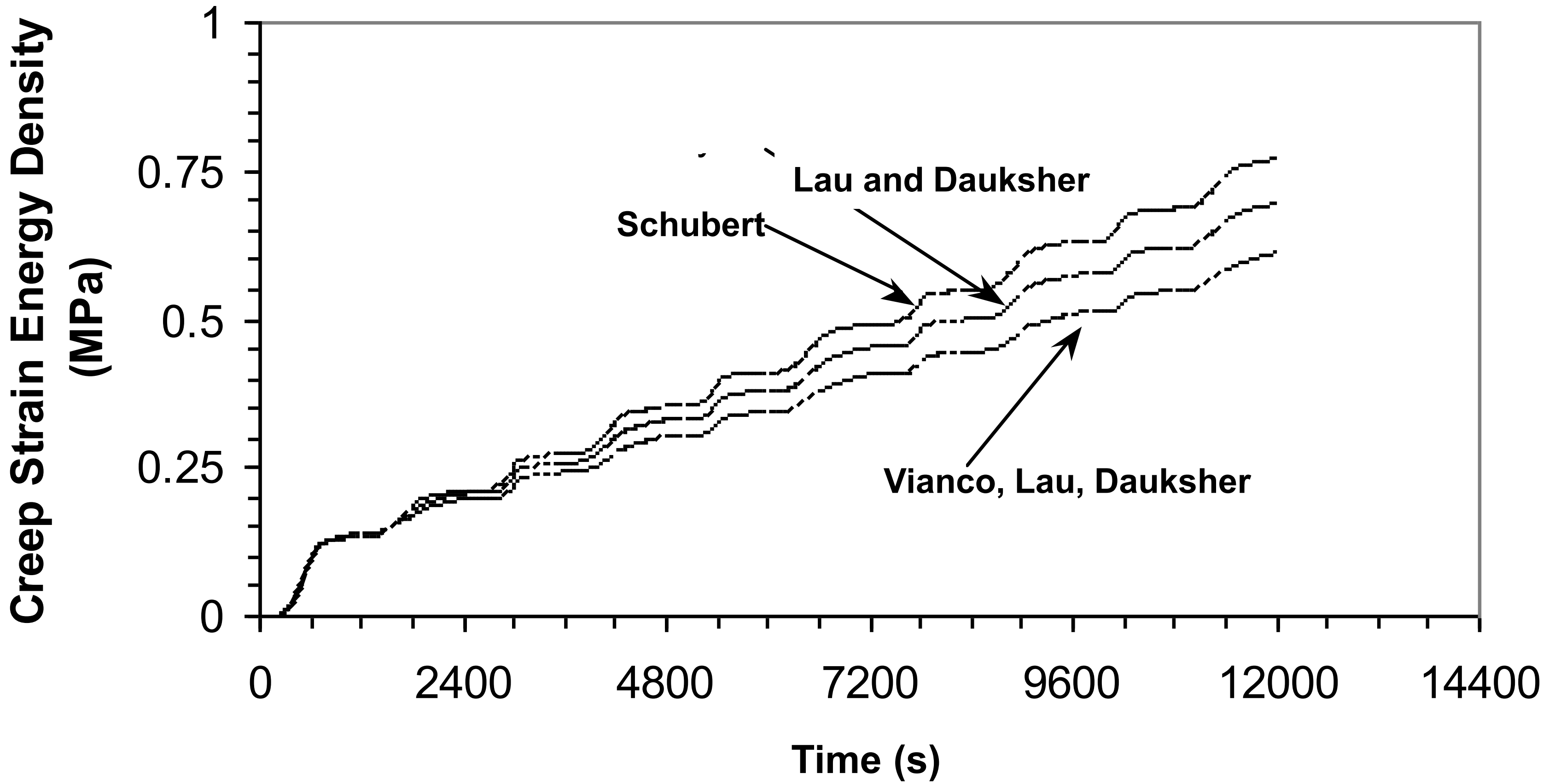
[36] Lau, J., Dauksher, W., and Vianco, P., 2003, "Acceleration Models, Constitutive Equations and Reliability of Lead-Free Solders and Joints," IEEE/ECTC Proceedings, New Orleans, LA, May 27–30, pp. 229–236.
[72] Schubertt, A., Dudek, R., Auerswald, E., Gollhardt, A., Michel, B., and Reicbl, H., 2003, "Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation," IEEE/ECTC Proceedings, New Orleans, LA, May 27–30, pp. 603–610.
[89] Lau, J. H., and Dauksher, W., 2004, "Creep Constitutive Equations of Sn(3.5- 3.9)wt%Ag(0.5-0.8)wt%Cu Lead-Free Solder Joints," MicroMaterails and Nanomaterials, B. Michel, ed., pp. 54–62.

The Fifth Shear Stress – Creep Shear Strain Hysteresis Loop of the Critical Solder Joint



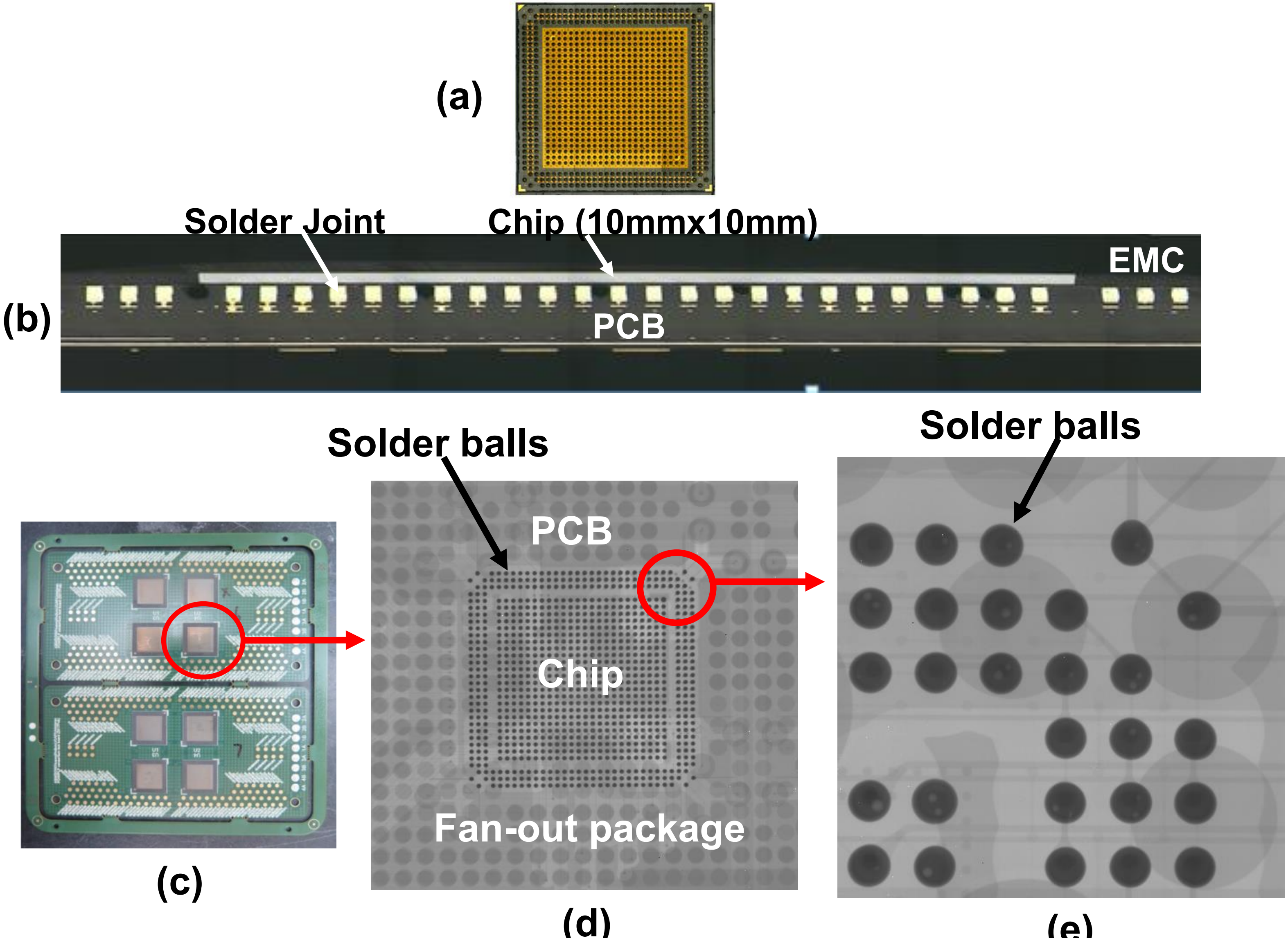
Depiver, J., Mallik, S., and Amalu, E., 2019, "Creep Response of Various Solders Used in Soldering Ball Grid Array (BGA) on Printed Circuit Board (PCB)," Proceedings of the World Congress on Engineering and Computer Science (WCECS), San Francisco, CA, Oct. 22–24, pp. 1–10

Creep Strain Energy Density Time-History of the Critical Solder Joint



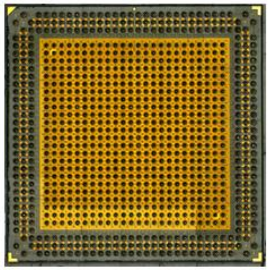
Depiver, J., Mallik, S., and Amalu, E., 2019, “Creep Response of Various Solders Used in Soldering Ball Grid Array (BGA) on Printed Circuit Board (PCB),” Proceedings of the World Congress on Engineering and Computer Science (WCECS), San Francisco, CA, Oct. 22–24, pp. 1–10

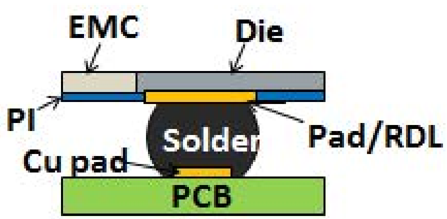
(a) Fan-out package with a 10mm x 100mm chip. (b) PCB assembly of the fan-out package. (c) Fan-out packages on a test board. (d) X-ray image of the PCB assembly. (e) Close-up of the assembly.



Lau, J. H., et al., 2018, "Design, Materials, Process, and Fabrication of Fan-Out Wafer Level Packaging," IEEE Trans. CPMT, 8(6), pp. 991–1002.

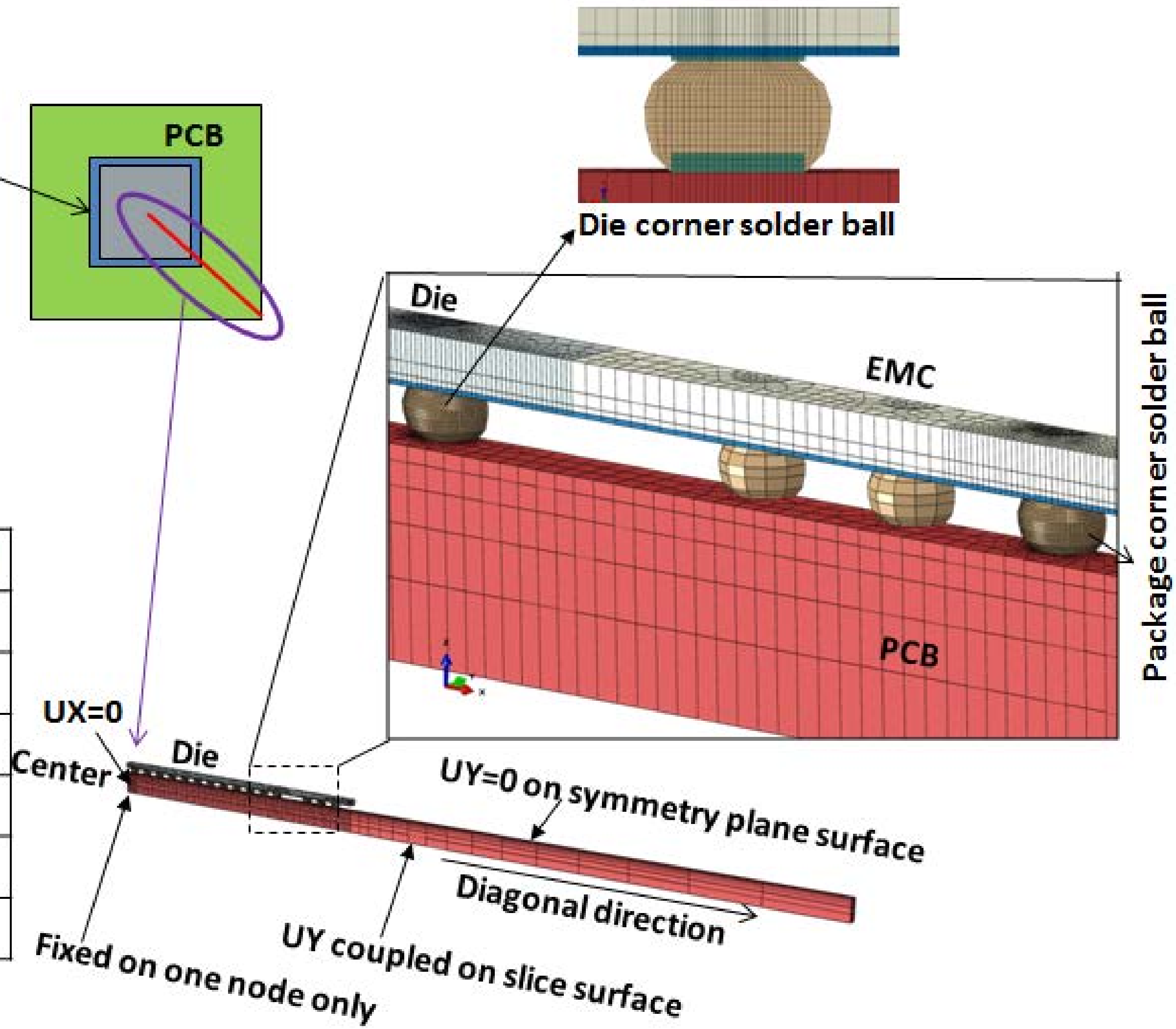
Finite Element Model of the Fan-Out Package PCB Assembly





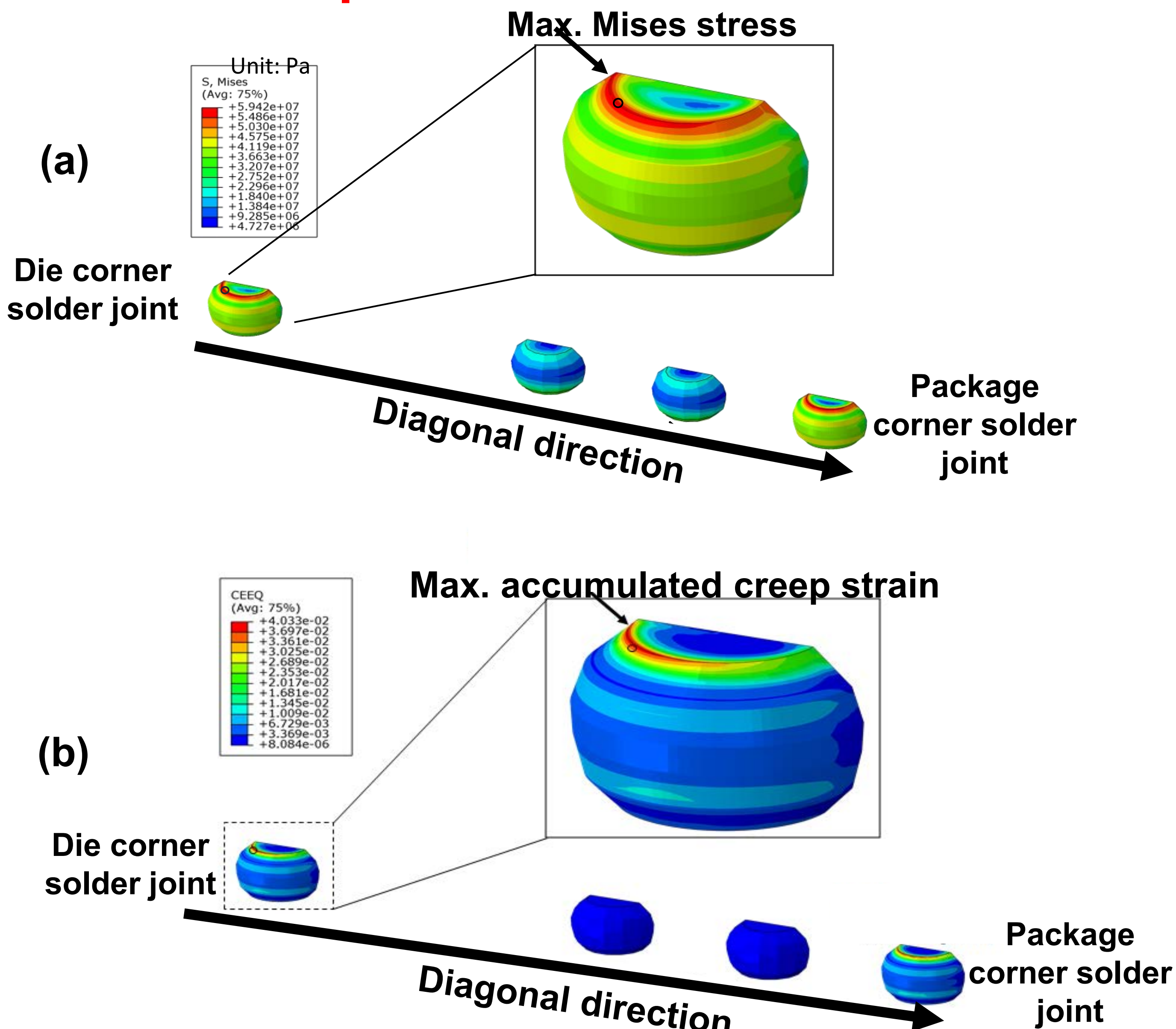
Schematic for model

Material	Thickness (μm)
Die	150
PI	15
RDL	7.5
Solder	140
Cu trace on sub.	30
PCB	650



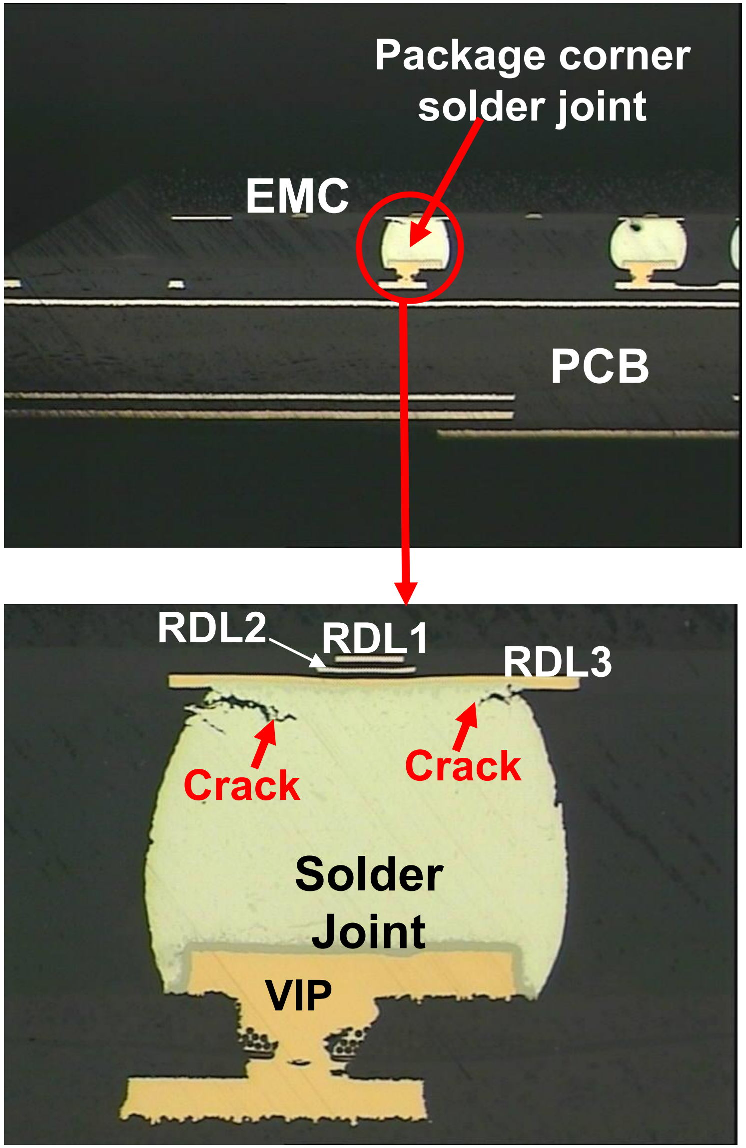
Lau, J. H., et al., 2018, "Design, Materials, Process, and Fabrication of Fan-Out Wafer Level Packaging," IEEE Trans. CPMT, 8(6), pp. 991–1002.

(a) Maximum Mises Stress in the Solder Joints. (b) Maximum Accumulated Creep Strain in the Solder Joints.



Lau, J. H., et al., 2018, “Design, Materials, Process, and Fabrication of Fan-Out Wafer Level Packaging,” IEEE Trans. CPMT, 8(6), pp. 991–1002.

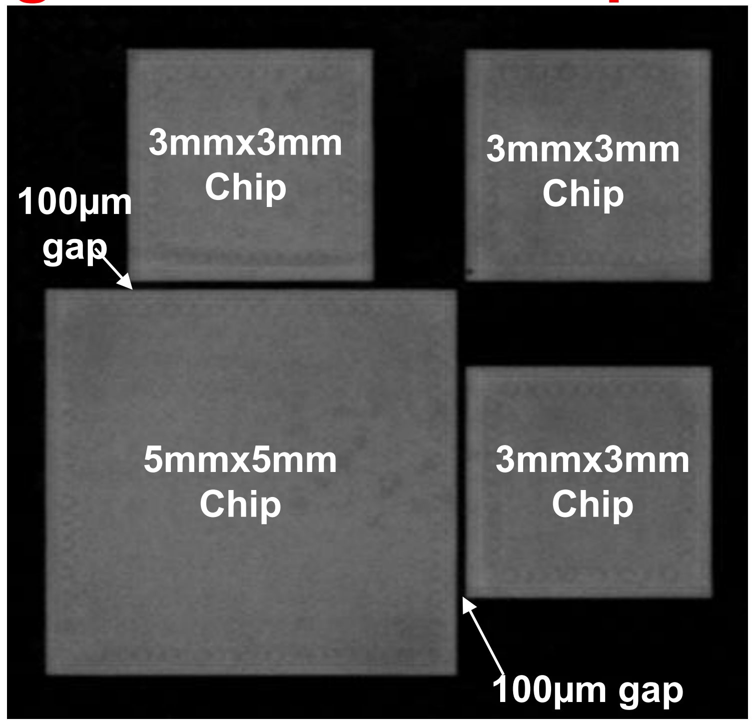
Failure Location and Mode of the Fan-Out Package Solder Joint

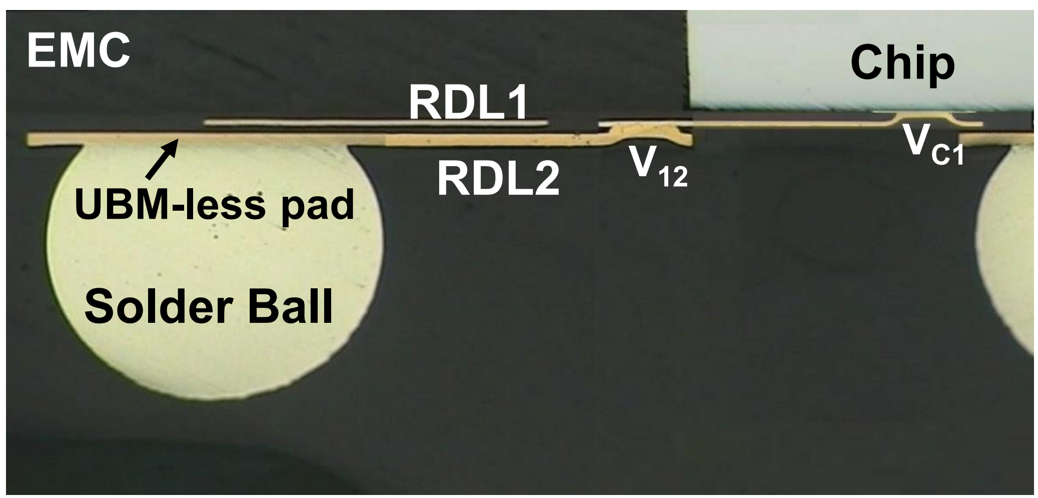


Lau, J. H., et al., 2018, "Design, Materials, Process, and Fabrication of Fan-Out Wafer Level Packaging," IEEE Trans. CPMT, 8(6), pp. 991–1002.

Heterogeneous integration of four chips fan-out package

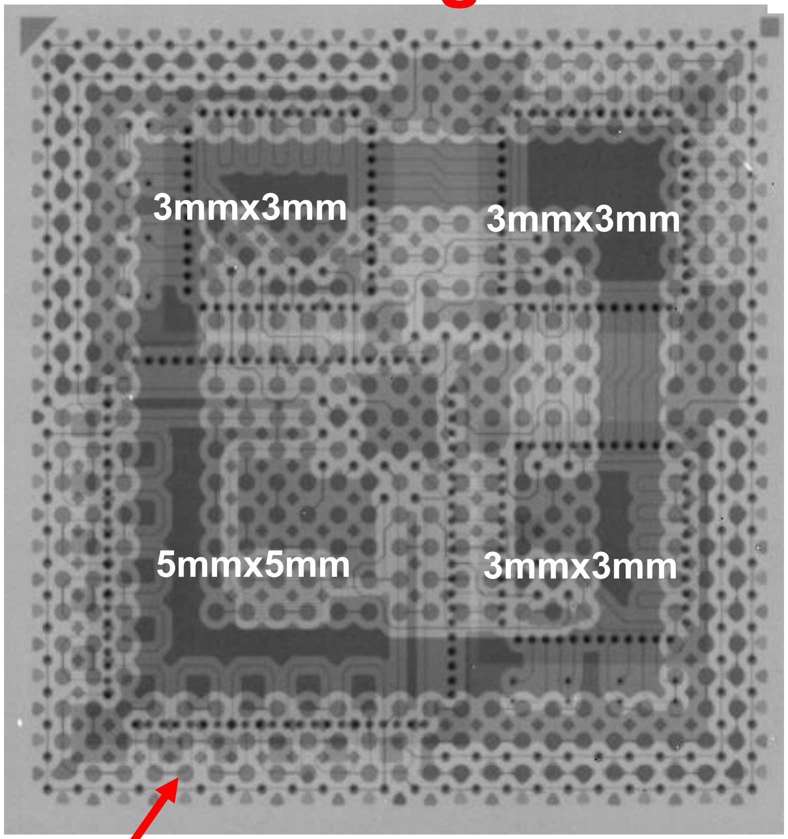
SiP: 10mmx10mm

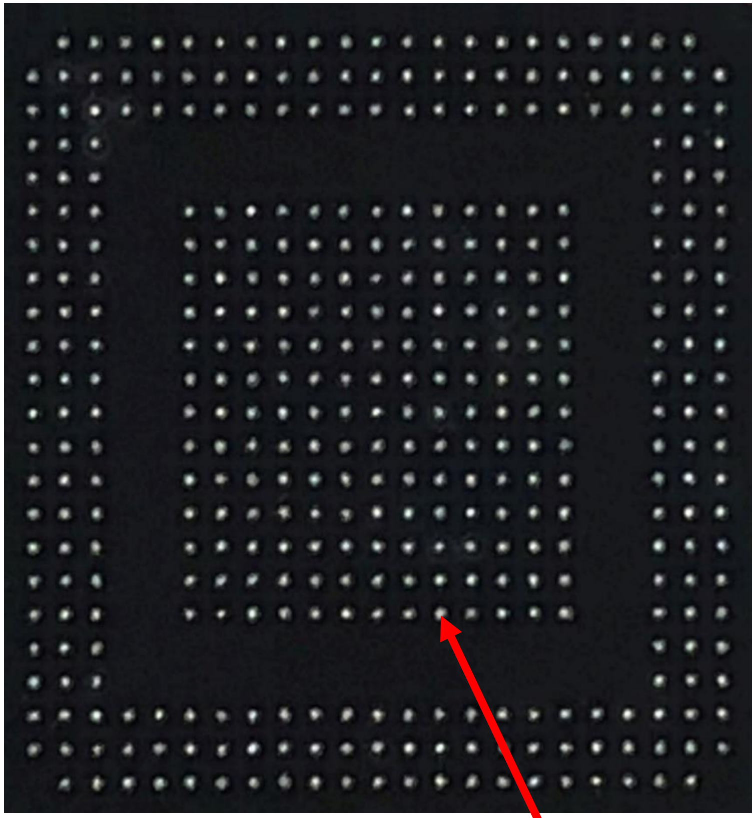




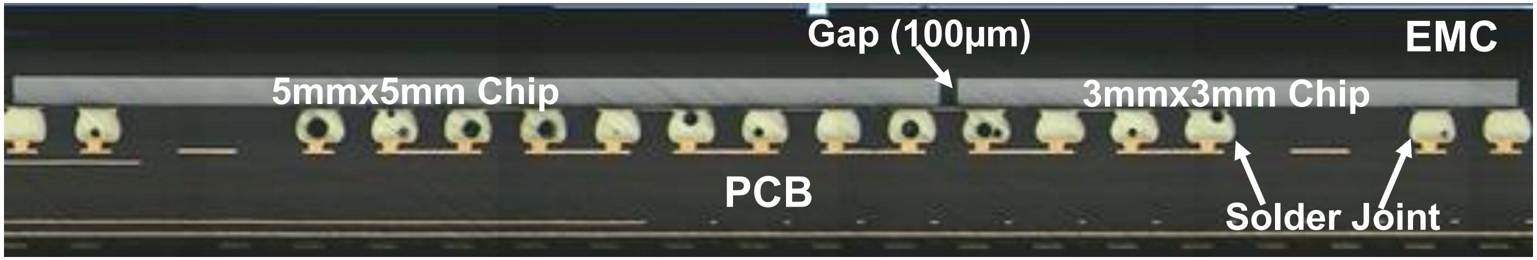
Lau, J. H.,, et al., "Fan-out wafer-level packaging for heterogeneous integration," *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.

PCB Assembly of the Heterogeneous Integration Fan-out Package with Sn3Ag0.5Cu Solder Joints



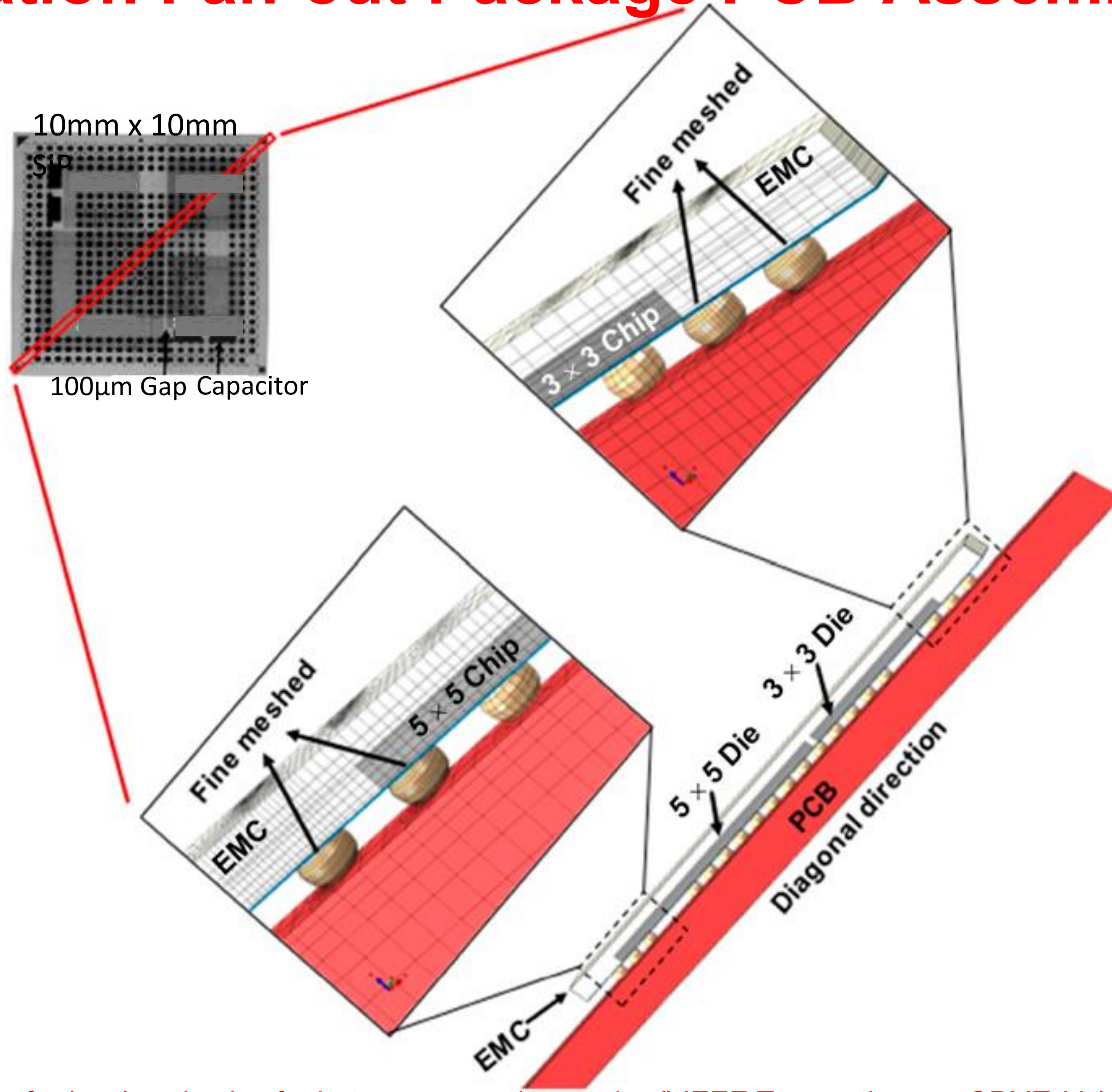


SiP: 10mmx10mm



Lau, J. H.,, et al., “Fan-out wafer-level packaging for heterogeneous integration,” *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.

Finite Element Model of the Heterogeneous Integration Fan-out Package PCB Assembly



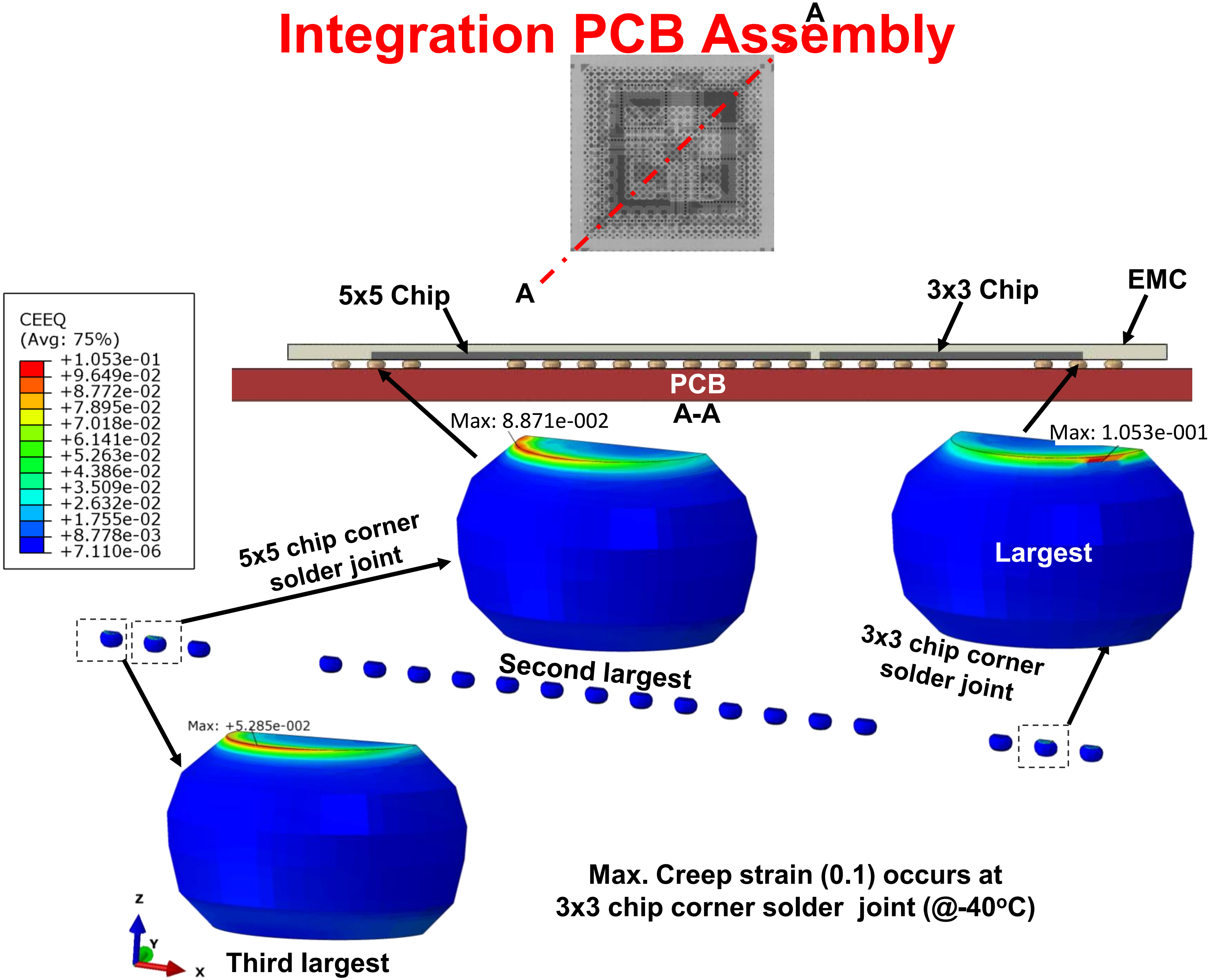
Lau, J. H.,, et al., "Fan-out wafer-level packaging for heterogeneous integration," *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.

Material Properties of the Heterogeneous Integration of Four Chips PCB Assembly

Materials	CTE (ppm/°C)	Young's Modulus (GPa)	Poison's Ratio
Copper	16.3	121	0.34
PCB	$\alpha_x = \alpha_y = 18$ $\alpha_z = 70$	$E_x = E_y = 22$ $E_z = 10$	0.28
Silicon	2.8	131	0.278
Solder	21 + 0.017T	49 – 0.07T	0.3
Polyimide	35	3.3	0.3
EMC	10 (< 150°C)	19	0.25

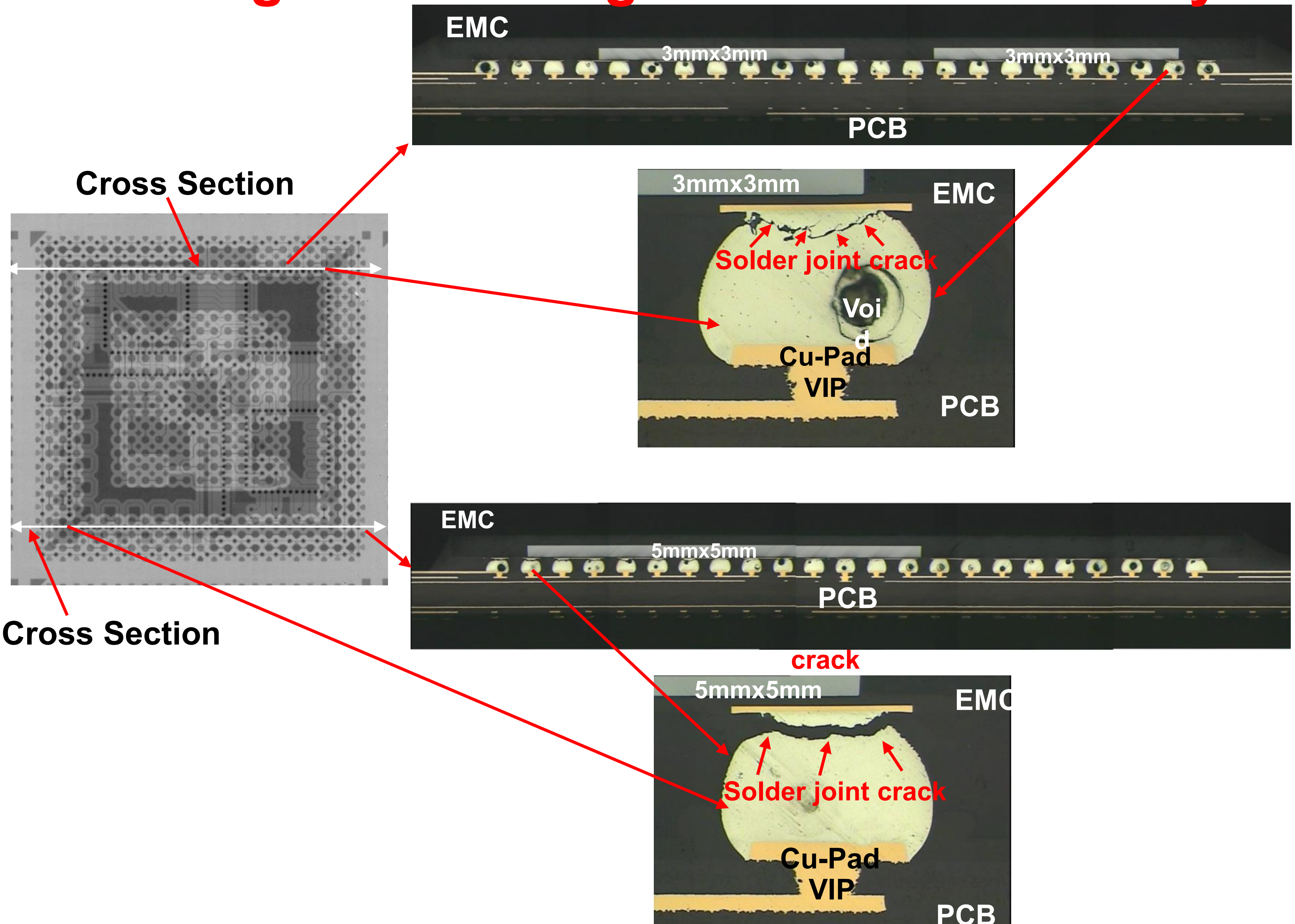
Lau, J. H.,, et al., "Fan-out wafer-level packaging for heterogeneous integration," *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.

Maximum Creep Strain in the Heterogeneous Integration PCB Assembly



Max. Creep strain (0.1) occurs at 3x3 chip corner solder joint (@-40°C)

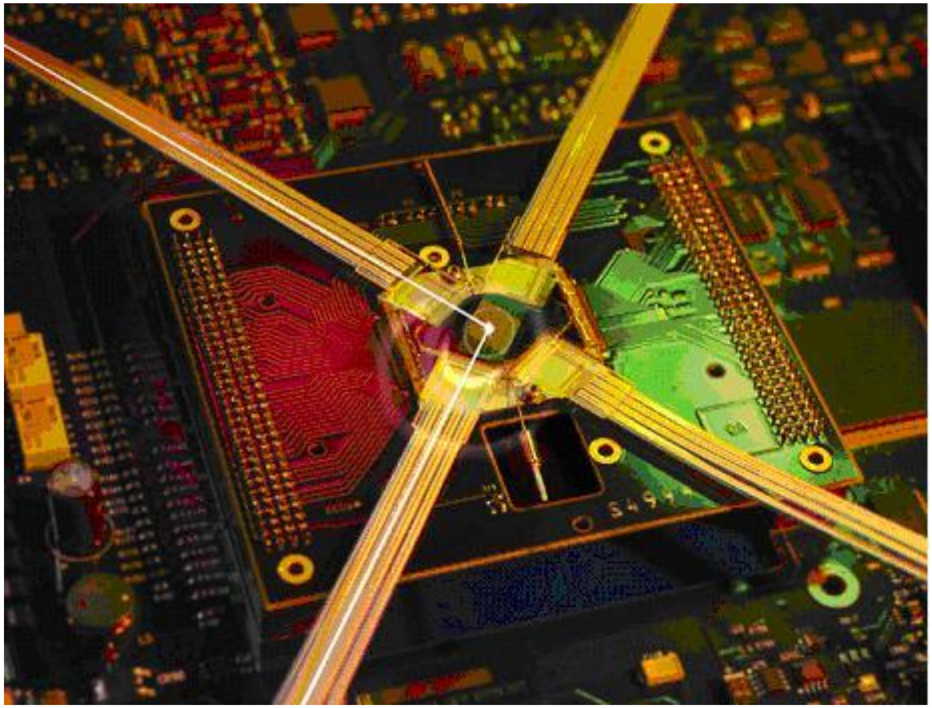
Failure Locations and Failure Modes in the Heterogeneous Integration PCB Assembly



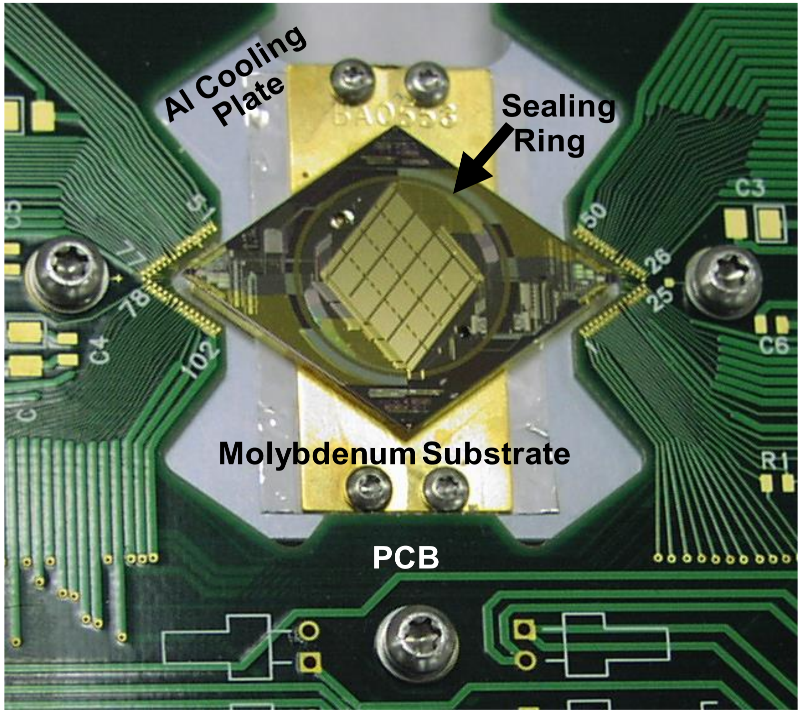
Lau, J. H.,, et al., “Fan-out wafer-level packaging for heterogeneous integration,” *IEEE Transactions on CPMT*, Vol. 8, Issue 9, September 2018, pp. 1544-1560.

(a) Full Assembled (Fiber-Attached) 32x32 All-Optical Device Developed by Agilent. (b) Close-up.

(a)

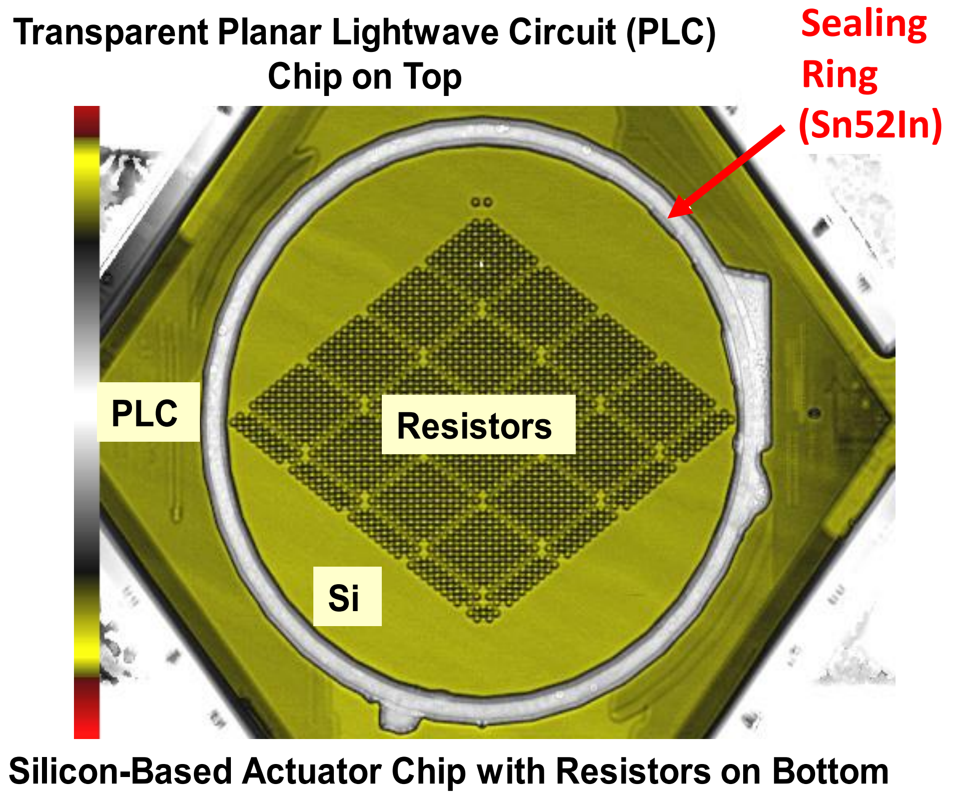


(b)

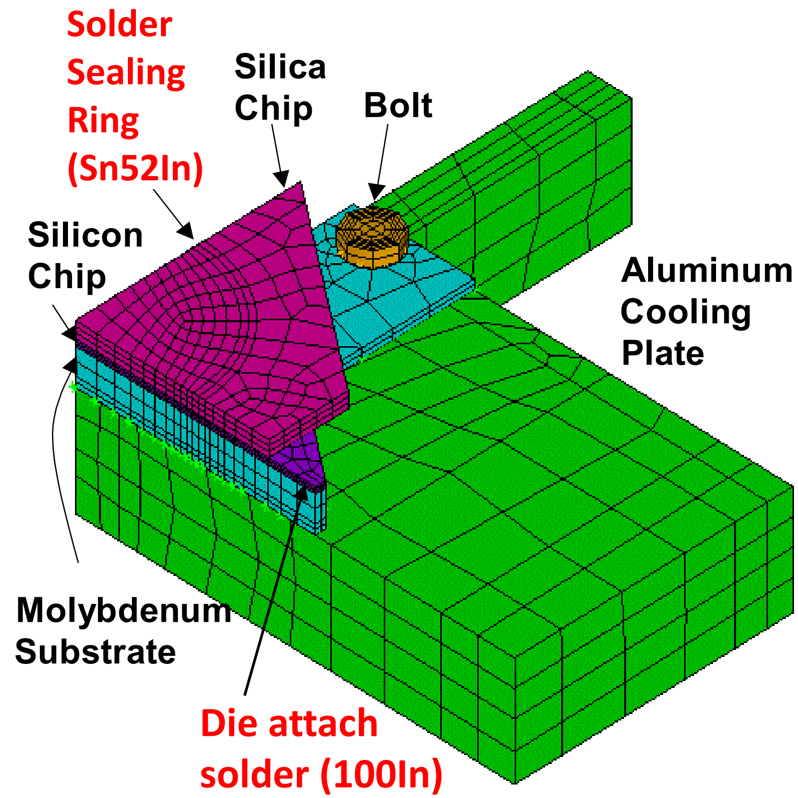


Lau, J. H., Mei, Z., Pang, S., Amsden, C., Rayner, J., and Pan, S., 2002, “Creep Analysis and Thermal-Fatigue Life Prediction of the Lead-Free Solder Sealing Ring of a Photonic Switch,” ASME J. Electron. Packag., 124(4), pp. 403–410.

(a) The silica-based planar light wave circuit chip and the silicon-based actuator chip are connected with a Sn52In sealing ring. (b) Finite element model.



(a)



(b)

Lau, J. H., Mei, Z., Pang, S., Amsden, C., Rayner, J., and Pan, S., 2002, "Creep Analysis and Thermal-Fatigue Life Prediction of the Lead-Free Solder Sealing Ring of a Photonic Switch," ASME J. Electron. Packag., 124(4), pp. 403–410.

Material Properties of the Photonic Switch

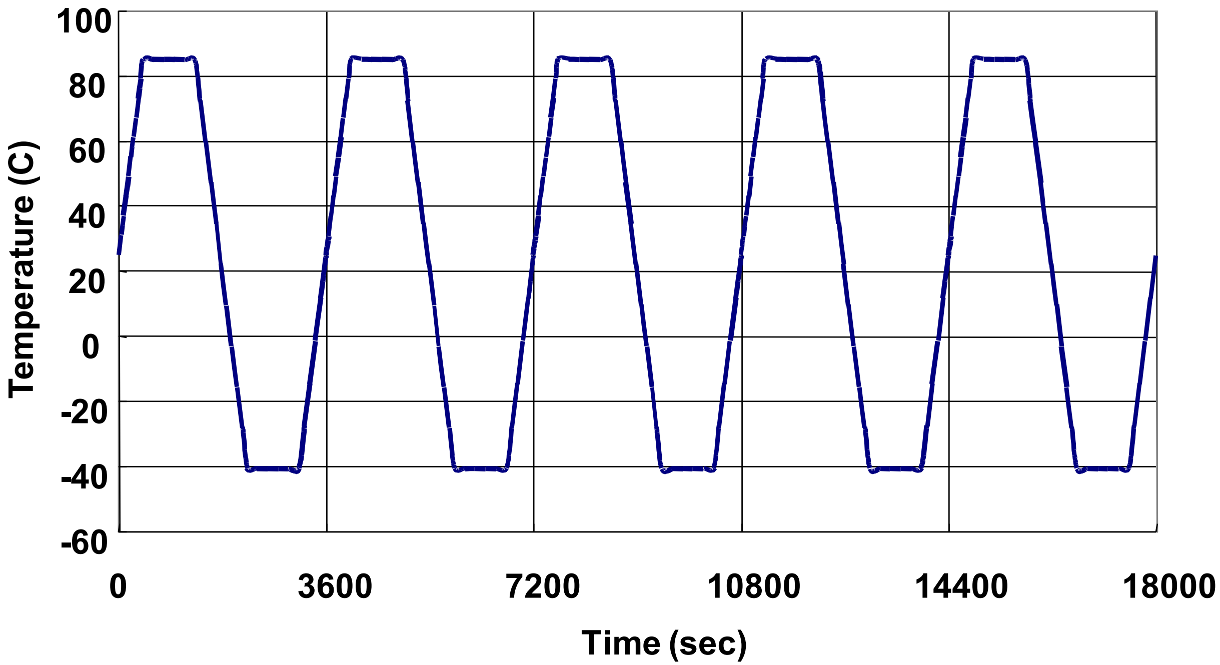
Material	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/°C)	Yield Strength (MPa)	Tensile Strength (MPa)	Elongation (%)	Thermal Conductivity (W/m-°K)	Density (g/cm³)	Specific Heat (cal/g-°K)	Creep
Molybdenum (Mo)	355 (1)	0.3 (7)	4.8 (1)	552 (1)	655 (1)	2.5 (3)	139 (1)	10.24 (7)	0.06 (7)	No
Silicon (Si)	163.3 (1)	0.28 (1)	2.5 (1)	34.5 (1)	185 (1)		165.43 (1)	2.4 (2)	0.169	No
48Sn-52In	30.5 (8)	0.36 (8)	28 (1)					7.3 (11)		Yes
100 In	11 (9)	0.45 (9)	32.1 (6)				82 (4)	7.3 (4)		Yes
Silica Fused Quartz (SiO_2)	72.4 (3)	0.14 (3)	0.5 (3)	66.9 (3)	75.9 (3)		0.33 (3)	2.2 (3)		No
Aluminum 6061-T6	70.3 (3)	0.35 (7)	23.2 (3)	10.3 (7)	45 (7)	12 (7)	237 (3)	2.7 (7)	0.211 (7)	No

Notes:

1. *Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies,* Lau and Pao, McGraw-Hill, 1997.
2. *Electronic Packaging and Interconnection Handbook,* Charles Harper, McGraw-Hill, 2000.
3. *Materials Handbook for Hybrid Microelectronics,* J. A. King, Teledyne Microelectronics, 1988.
4. www.webelements.com, 2001.
5. *Ball Grid Array Technology,* John Lau,
6. *Microvias for Low Cost and High Density Interconnects,* John Lau and Ricky Lee, McGraw-Hill, 2001.
7. *Mark's Standard Handbook for Mechanical Engineers,* Eighth Edition, McGraw-Hill, 1978.
8. Average of Sn and In from Note 4.
9. *Technical Bulletin of Pure Indium,* Indium Corporation of America, 2001.
10. *Superplastic Creep of Low Melting Point Solder Joints,* Mei and Morris, J. of Electronic Materials, 401-407, 1992.
11. *Solder Paste in Electronics Packaging,* J. Hwang, Van Nostrand Reinhold, 1989.

Lau, J. H., Mei, Z., Pang, S., Amsden, C., Rayner, J., and Pan, S., 2002, "Creep Analysis and Thermal-Fatigue Life Prediction of the Lead-Free Solder Sealing Ring of a Photonic Switch," ASME J. Electron. Packag., 124(4), pp. 403–410.

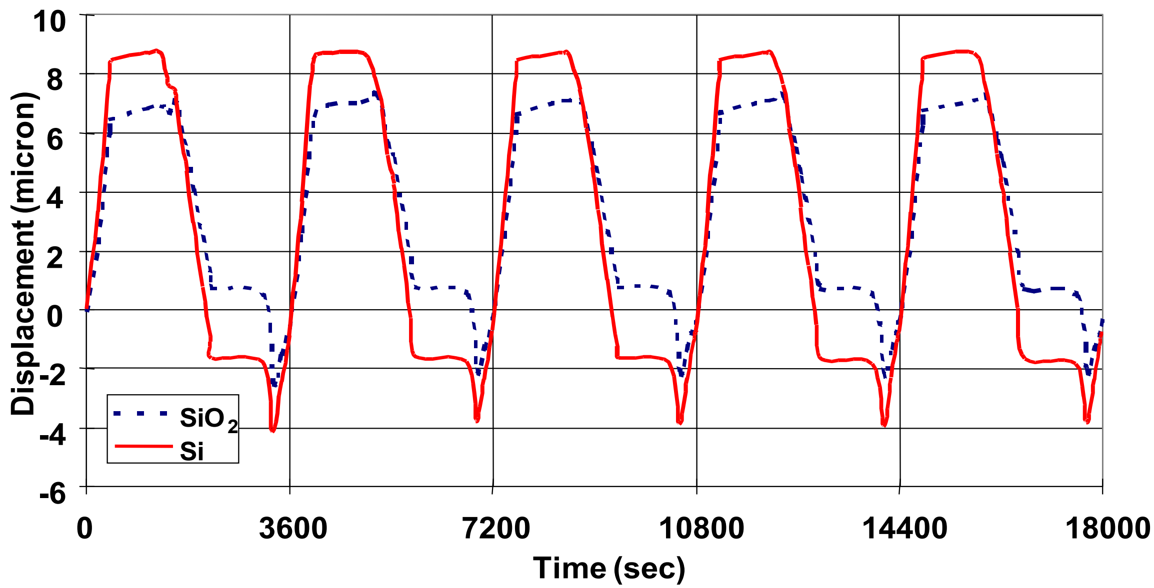
Temperature Condition for Finite Element Simulation



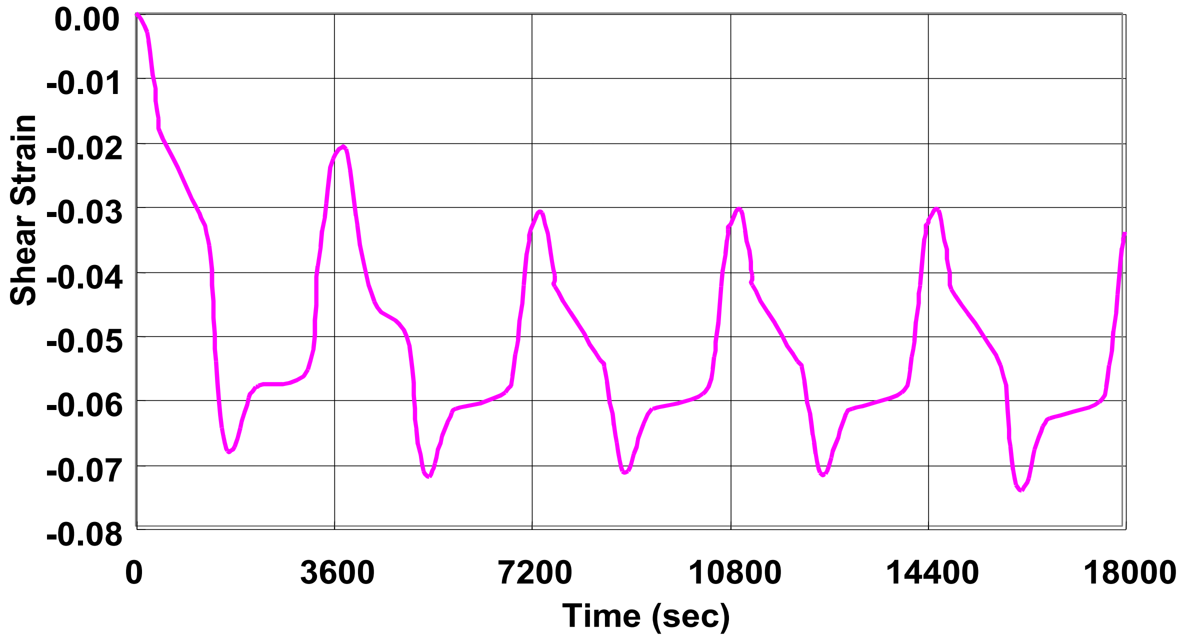
Lau, J. H., Mei, Z., Pang, S., Amsden, C., Rayner, J., and Pan, S., 2002, "Creep Analysis and Thermal-Fatigue Life Prediction of the Lead-Free Solder Sealing Ring of a Photonic Switch," ASME J. Electron. Packag., 124(4), pp. 403–410.

(a) Displacement of the SiO_2 and Si chips vs. time. (b) Shear strain time-history at the Sn52In sealing ring.

(a)

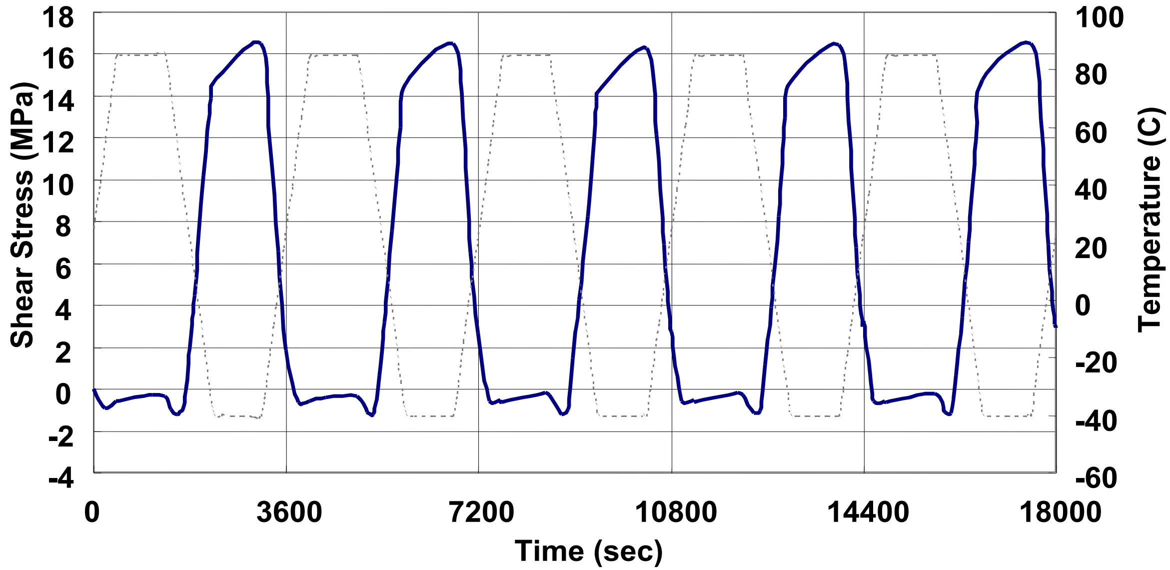


(b)

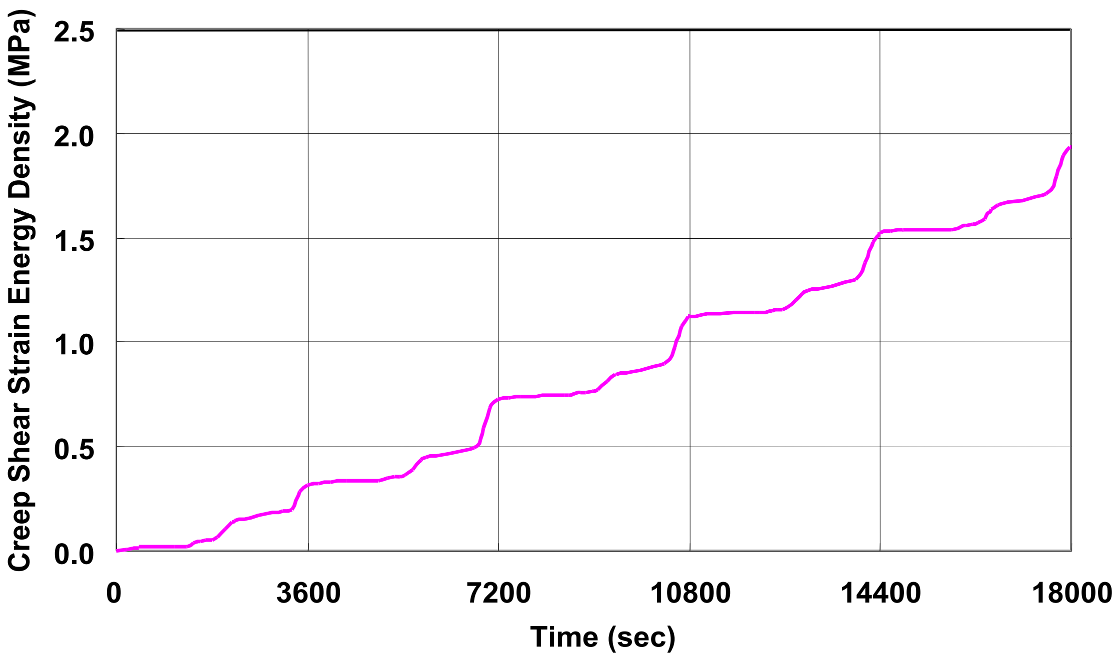


(a) Displacement of the SiO_2 and Si chips vs. time. (b) Shear strain time-history at the Sn52In sealing ring.

(a)



(b)



Anand Viscoplasticity

The Anand viscoplastic model is an internal variable based model in which the inelastic behavior including temperature- and rate-dependent, and rate-independent plasticity effects are unified. The Anand flow equation which governs the inelastic strain *ε* has the following form:

$$\frac{d\varepsilon}{dt} = A\left[\sinh\left(\frac{\xi\sigma}{s}\right)\right]^{1/m} \exp\left(-\frac{Q}{RT}\right)$$

where *dε/dt* is the inelastic strain rate, A is the pre-exponential factor, Q is the activation energy, R is the universal gas constant (8.314 J·K^{-1}·mol^{-1}), T is the absolute temperature (Kevin), ξ is the multiplier of stress, σ is the equivalent stress, *m* is strain rate sensitivity. The evolution equation which defines an internal variable *s* of the model and its saturation value is:

$$\frac{ds}{dt} = \left\{h_0(|B|)^{\alpha}\frac{B}{|B|}\right\}\frac{d\varepsilon}{dt}$$

where

$$B = 1 - \frac{s}{s^*}$$

and

$$s^* = \hat{s}\left[\frac{d\varepsilon_p/dt}{A}\exp\left(\frac{Q}{RT}\right)\right]^n$$

Anand, L., 1982, "Constitutive Equations for the Rate-Dependent Deformation of Metals at Elevated Temperatures," ASME, J. Eng. Mater. Technol., 104(1), pp. 12–17.

Anand Viscoplasticity

where h_0 is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening. The quantity s^* represents a saturation value of deformation resistances. $\hat{s}$ is a coefficient, and *n* is the strain rate sensitivity for the saturation value of deformation resistance, respectively. The evolution equation has an extra initial condition of $s(0) = s_0$, where s_0 is the initial value of *s* at initial time $t = 0$. The Anand model does not have an explicit yield criterion or a loading-unloading criterion and viscoplastic flow occurs for any non-zero stress.

There are a total of nine (9) constants (parameters) of the Anand equation (model), namely *A*, *Q*, ξ, *m*, s, *n*, $h_{0,}$ α, and $s_{0,}$ and their definition are tabulated for easy reference. These parameters can be determined through fitting to the experimental data of solders. These parameters can be taken as input in ANSYS and ABAQUS. These parameters can be taken as input in ANSYS and ABAQUS and determined through fitting to the experimental data of solders. Most researchers use the stress-strain curves (data) with various strain rates and temperatures of solders. However, some use the creep curves (data) with various stresses and temperatures of solders.

Definition of the Parameters in Anand's Model

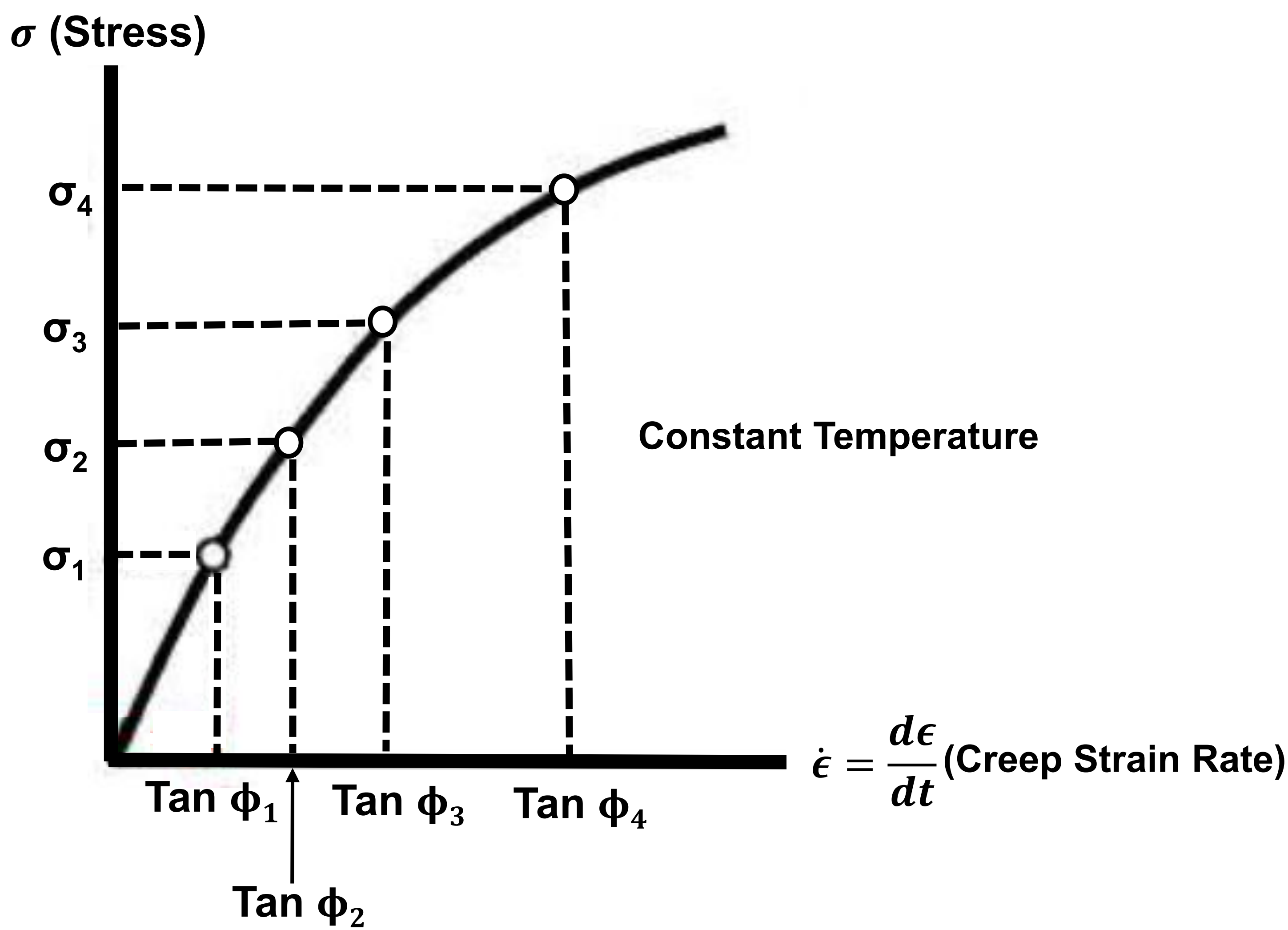
Parameters	Definition in Anand's Model
A(1/s)	Pre-exponential factor
Q/R (°K)	Activation energy/Universal gas constant
ξ	Stress multiplier
m	Strain rate sensitivity of stress
$\hat{s}$ (MPa)	Coefficient for deformation resistance saturation value
n	Strain rate sensitivity of saturation value
h_o (MPa)	Hardening constant
a	Strain rate sensitivity of hardening/softening
s_o (MPa)	Initial value of deformation resistance

Anand Parameters of Solders Based on Creep Curves

Parameters	Sn 3Ag [102]	Sn 3Ag 0.5 Cu [97]	Au20Sn [100]
A (1/s)	2.23×10^4	3484	69.53
Q/R (°K)	8900	9096	5240
ξ	6	4	0.4
m	0.181	0.2	0.2598
$\hat{s}$ (MPa)	73.81	26.4	27.11
n	0.018	0.01	0.0917
h_o (MPa)	3321.15	144,000	27,595
a	1.82	1.9	1.017
s_0 (MPa)	39.09	18.07	14.75

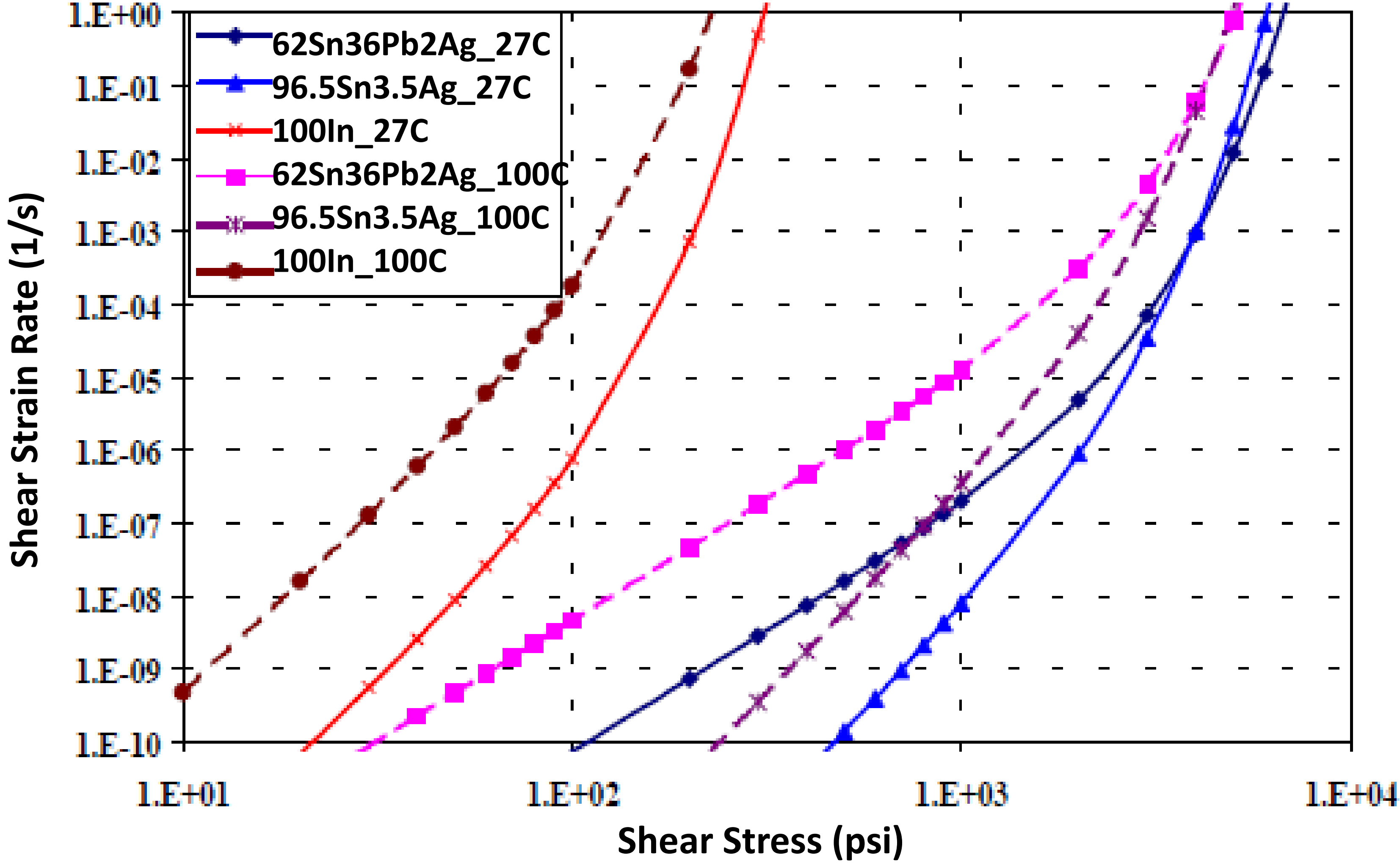
[97] Motalab, M., Cai, Z., Suhling, J. C., and Lall, P., 2012, "Determination of Anand Constants for SAC Solders Using Stress-Strain or Creep Data," IEEE/ITHERM Proceedings, San Diego, CA, May 30–June 1, pp. 910–923.
[100] Jin, T., 2017, "Investigation on Viscoplastic Properties of Au-Sn Die-Attach Solder," Master thesis, Delft University of Technology, Delft, The Netherlands.
[102] Wang, G., Cheng, Z., Becker, K., and Wilde, J., 2001, "Applying Anand Model to Represent the Viscoplastic Deformation Behavior of Solder Alloys," ASME J. Electron. Packag., 123(3), pp. 247–253.

Stress vs. Creep Strain Rate Curve with Various Stresses at a Constant Temperature



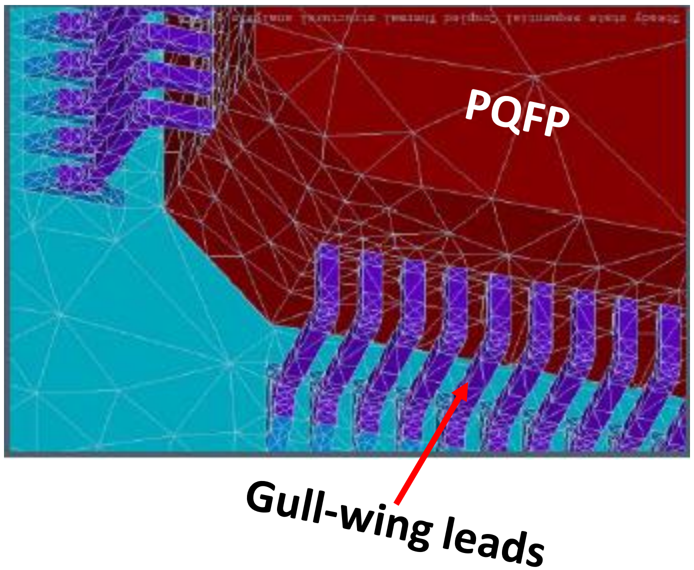
Assembly and Reliability of Lead-Free Solder Joints, Springer, 2020

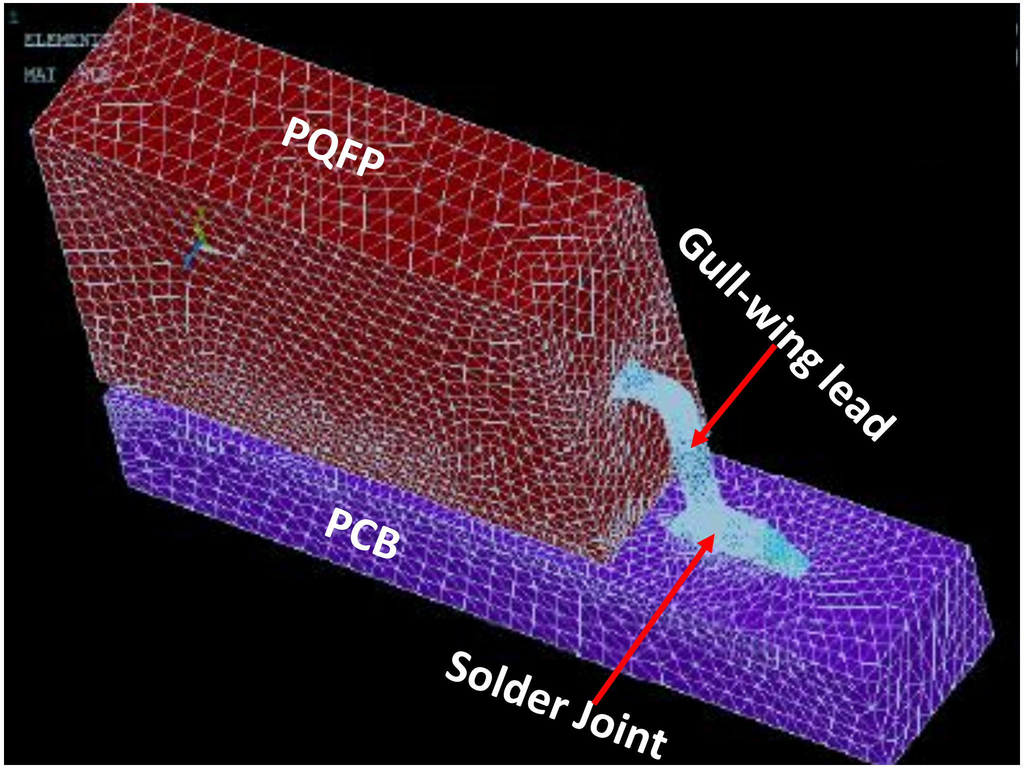
Shear Stress vs. Shear Creep Strain Rate Curves for Various Solders



Darveaux, R., and K. Banerji, “Constitutive Relations for Tin-Based-Solder Joints”, *IEEE/ECTC Proceedings*, May 1992, pp. 538-551.

Goble and local finite element models of a 256-pin PQFP with Sn3.5Ag solder joints





Hamdani, H., Radi, B., and Elhami, A., 2017, "Submodeling Technique for Assessment and Numerical Prediction of Solder Joints Failures in Mechatronic Devices," 13th Mechanical Congress, Meknes, Morocco, Apr. 11–14, pp. 1–3

Parameters in Anand's Model for Sn3.5Ag

Material Constants	96.5Sn3.5Ag [Wang, et al.]
A(1/s)	2.23x10^4
Q/R (°K)	8900
ξ	6
m	0.181
$\hat{s}$ (MPa)	73.81
n	0.018
h_o (MPa)	3321.15
a	1.82
s_o (MPa)	39.09

Wang, G., Cheng, Z., Becker, K., and Wilde, J., 2001, "Applying Anand Model to Represent the Viscoplastic Deformation Behavior of Solder Alloys," ASME J. Electron. Packag., 123(3), pp. 247–253.

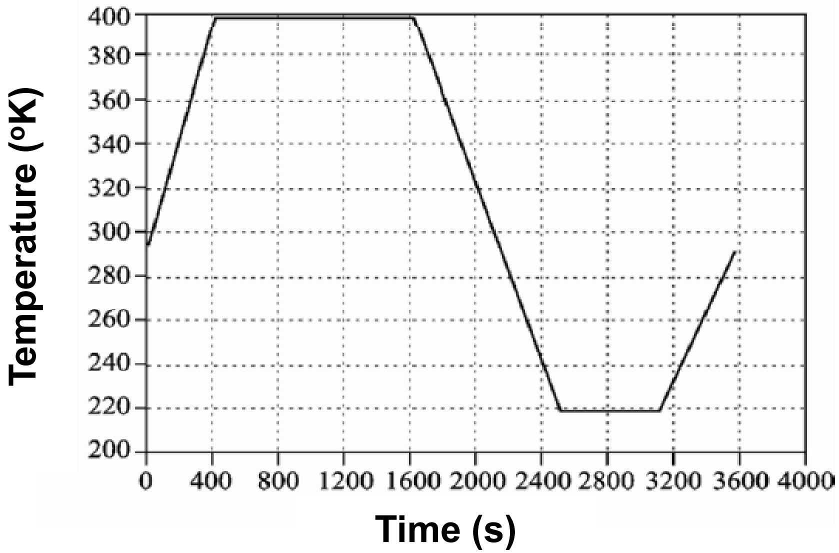
Material Properties of the 256-pin PQFP PCB Assembly

Materials	96.5Sn3.5Ag	FR4	Epoxy	Cu
Young's Module (GPa)	51.3	17	17	115
Poisson's Ratio	0.3	0.3	0.2	0.31
Density (Kg/m^3)	740	180	180	8890
CTE (µm/K)	20	18	22	17
Shear Module (GPa)	19	2.4	7.4	44

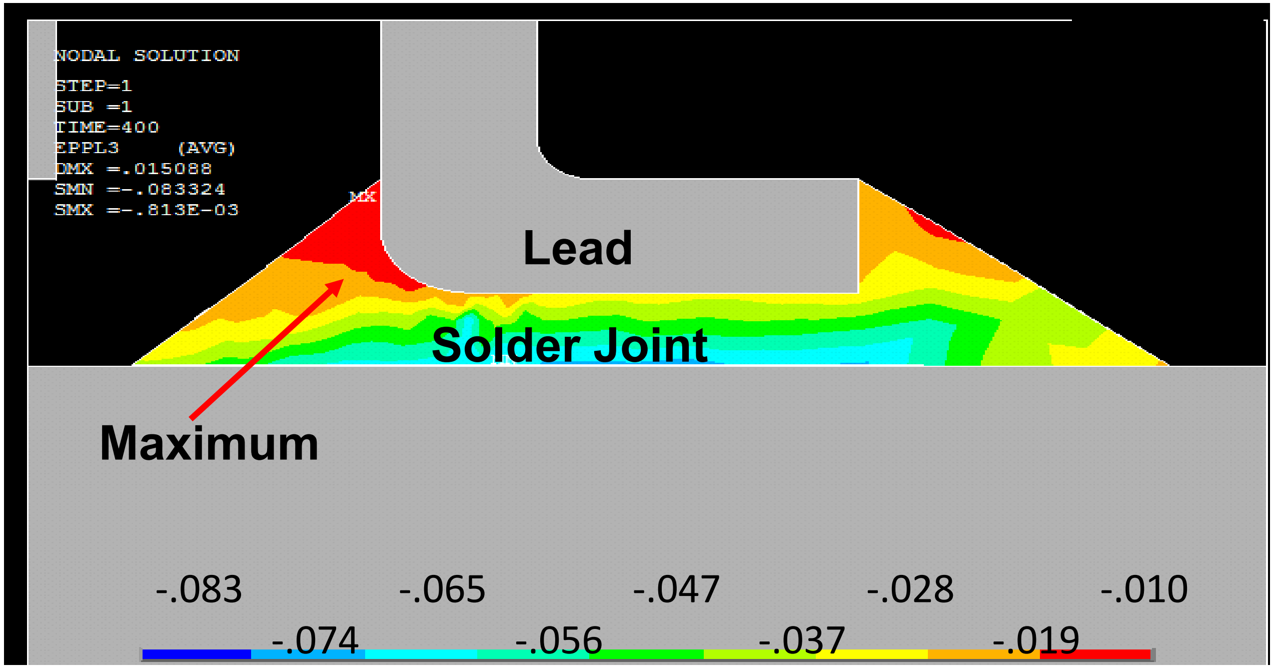
Hamdani, H., Radi, B., and Elhami, A., 2017, "Submodeling Technique for Assessment and Numerical Prediction of Solder Joints Failures in Mechatronic Devices," 13th Mechanical Congress, Meknes, Morocco, Apr. 11–14, pp. 1–3.

(a) Temperature condition for finite element simulation. (b) Strain contours at the lead-free solder joint.

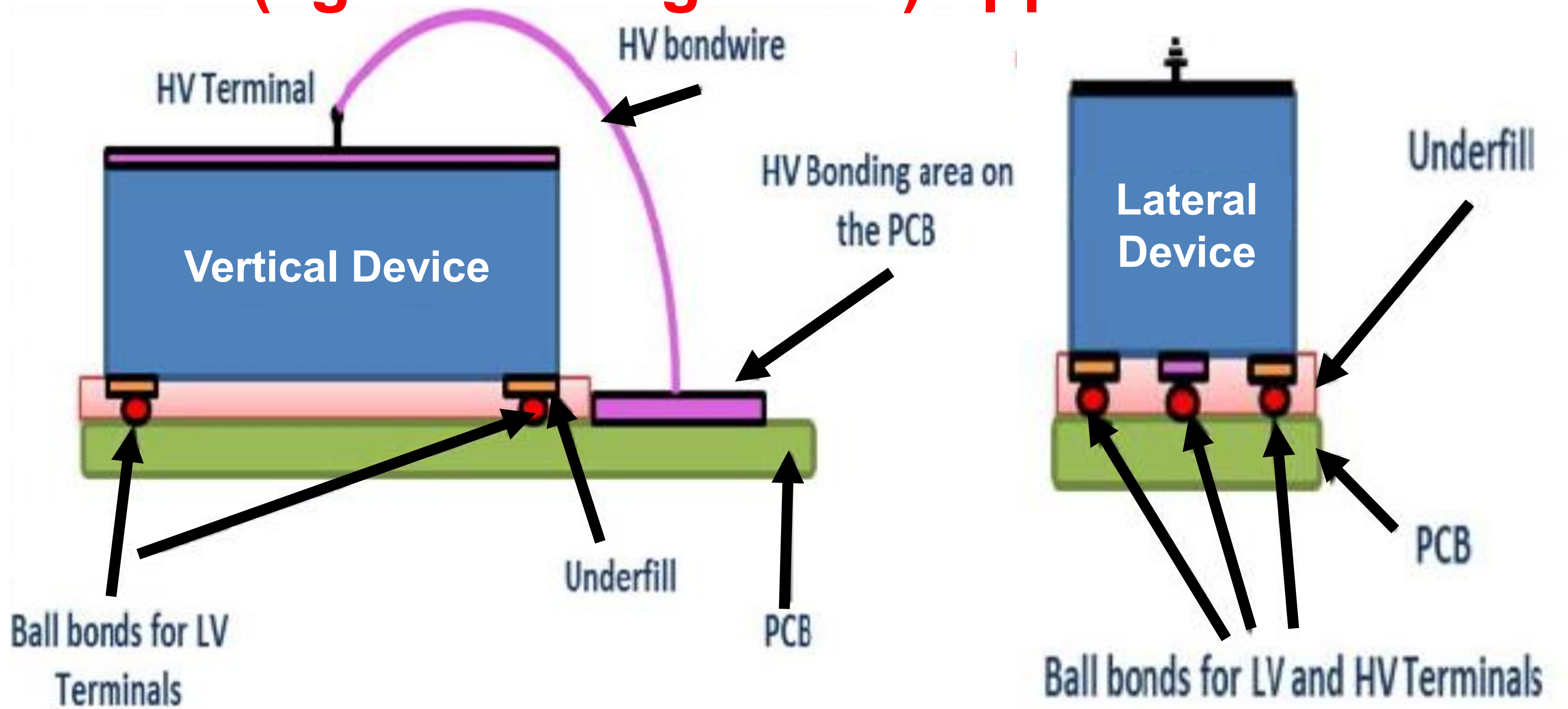
(a)



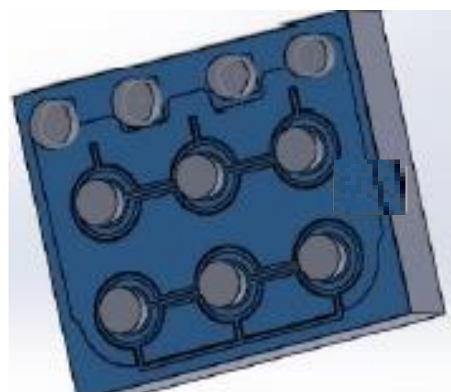
(b)



IGBT (insulated-gate bipolar transistor) for LED (light-emitting diode) applications

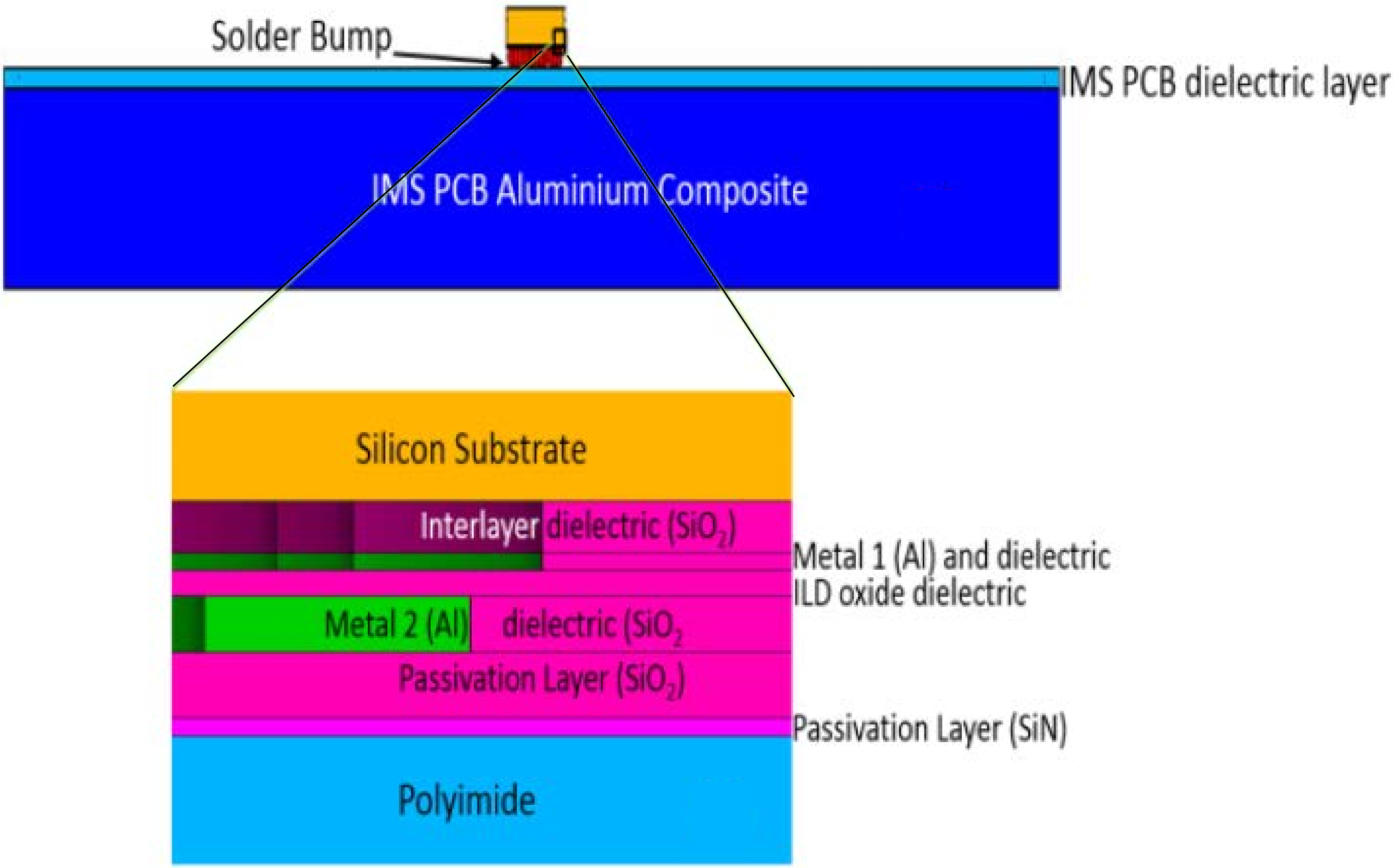


3D Device



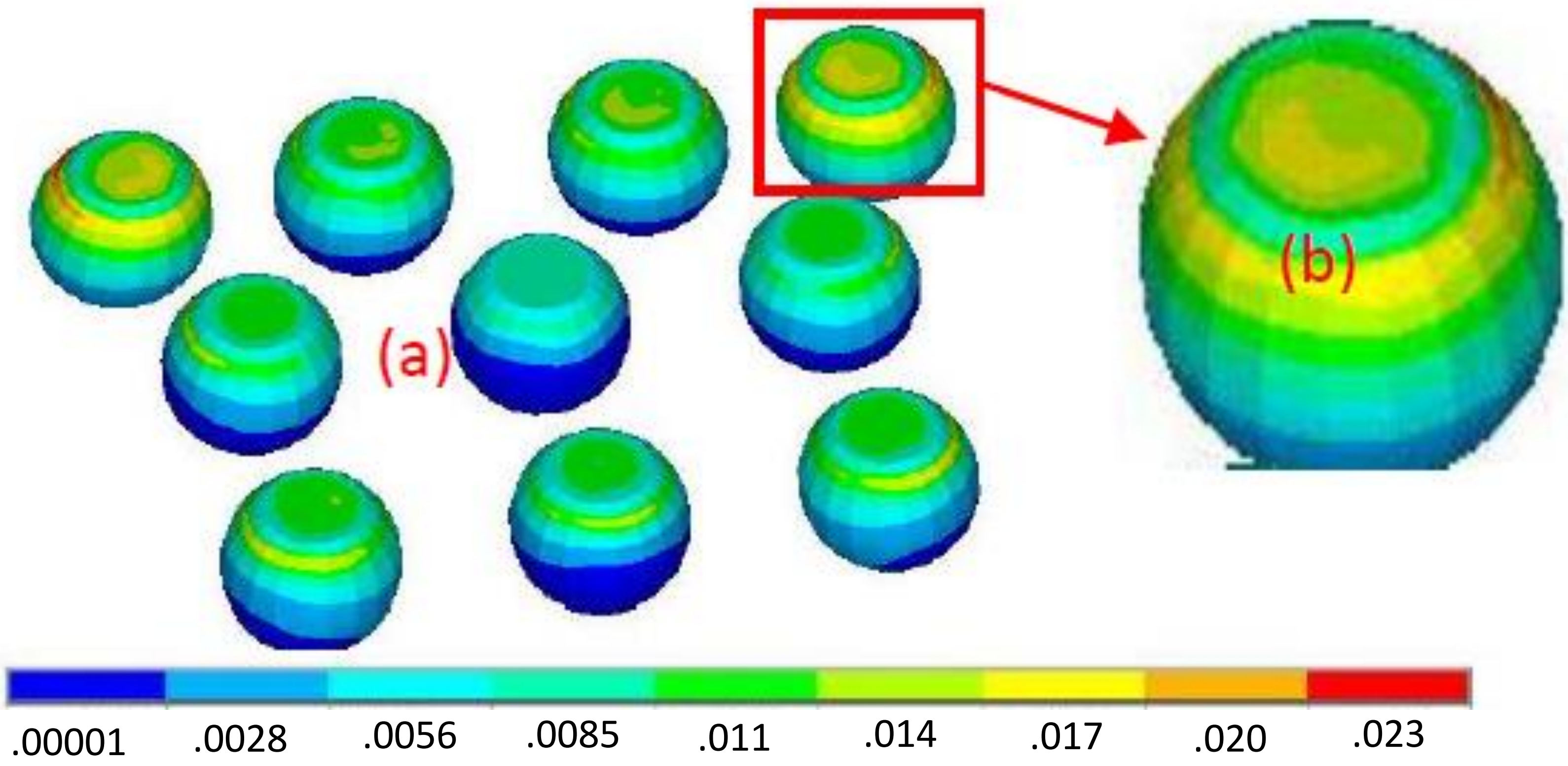
Bailey, C., Rajaguru, P., Lu, H., Castellazzi, A., Antonini, M., Pathirana, V., Udugampola, N., Udrea, F., Mitchelson, P., and Aldhaher, S., 2018, "Mechanical Modelling of High Power Lateral IGBT for LED Driver Applications," IEEE/ECTC Proceedings, San Diego, CA, May 29–June 1, pp. 1375–1381.

Side-view of IGBT and the Layers of the Device



Bailey, C., Rajaguru, P., Lu, H., Castellazzi, A., Antonini, M., Pathirana, V., Udugampola, N., Udrea, F., Mitchelson, P., and Aldhaher, S., 2018, "Mechanical Modelling of High Power Lateral IGBT for LED Driver Applications," IEEE/ECTC Proceedings, San Diego, CA, May 29–June 1, pp. 1375–1381.

Accumulated Inelastic Strain Contours in the Solder Joints



Bailey, C., Rajaguru, P., Lu, H., Castellazzi, A., Antonini, M., Pathirana, V., Udugampola, N., Udrea, F., Mitchelson, P., and Aldhaher, S., 2018, "Mechanical Modelling of High Power Lateral IGBT for LED Driver Applications," IEEE/ECTC Proceedings, San Diego, CA, May 29–June 1, pp. 1375–1381.

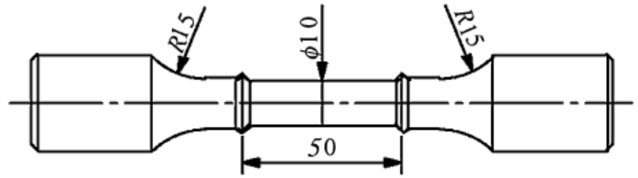
Anand Parameters of Solders Based on Stress-Strain Curves

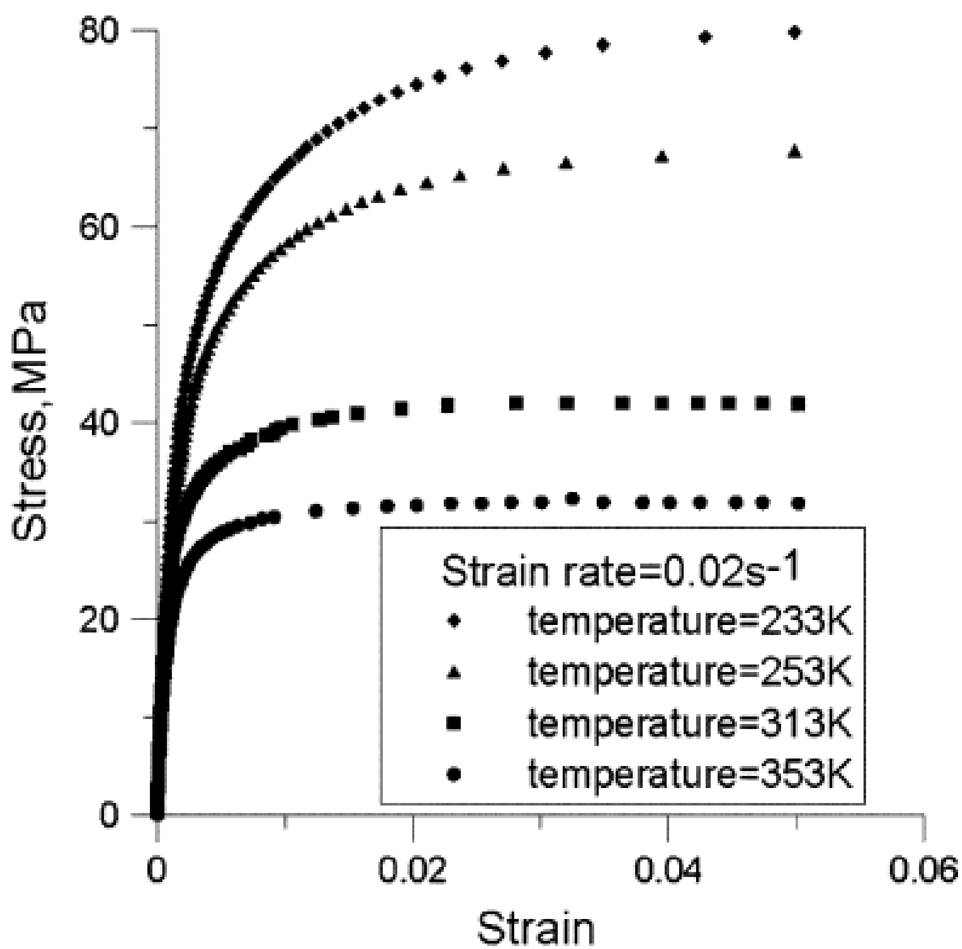
Material constant	Sn3.5 Ag [51]	Sn3.5Ag [94]	Sn3.5Ag [68]	Sn3.8Ag0.7Cu [103]	Sn3.8Ag0.7Cu0.03Ce [103]	Sn3.8Ag0.7Cu0.1Al [104]
A (1/s)	177,016	177,016	177,016	24,300	21,200	22,100
Q/R (°K)	10,279	10,279	10,279	8710	8026	8015
ξ	7	7	7	5.8	5	4.1
m	0.207	0.207	0.207	0.183	0.130	0.150
$\hat{s}$ (MPa)	52.4	52.4	52.4	65.3	57.6	59.0
n	0.0177	0.0177	0.0177	0.019	0.0175	0.0154
h_o (MPa)	β	27782	27782	3541.2	4352.6	4132
a	1.6	1.6	1.6	1.9	2.3	2.0
s_o (MPa)	Ω	9.53	φ	39.5	28.5	27.0

$\beta = -90940 + 961\,T - 0.956T^2 - 3260582\dot{\varepsilon} + 24976816(\dot{\varepsilon})^2$.
$\Omega = -0.0673\,T + 28.6$.
$\varphi = -0.0673\,T + 28.6$.
T is in Kelvin and $\dot{\varepsilon}$ is the strain rate (1/s).

[51] Chen, X., Chen, G., and Sakane, M., 2005, "Prediction of Stress-Strain Relationship With an Improved Anand Constitutive Model for Lead-Free Solder Sn-3.5Ag," IEEE Trans. CPMT, 28, pp. 111–116.
[94] Deshpande, A., Khan, H., Mirza, F., and Agonafer, D., 2014, "Global-Local Finite Element Optimization Study to Minimize BGA Damage Under Thermal Cycling," IEEE/ITHERM Proceedings, Orlando, FL, May 27–30, pp. 483–487.
[68] Ramachandran, V., Wu, K., and Chiang, K., 2018, "Overview Study of Solder Joint Reliability Due to Creep Deformation," J. Mech., 34(5), pp. 637–643.
[103] Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.
[104] Zhang, L., Liu, Z., and Ji, Y., 2016, "Anand Constitutive Model of Lead-Free Solder Joint in 3D IC Device," Journal of Physics: Fifth International Conference on Mathematical Modeling in Physical Science, Athens, Greece, May 23–26, pp. 1–8.

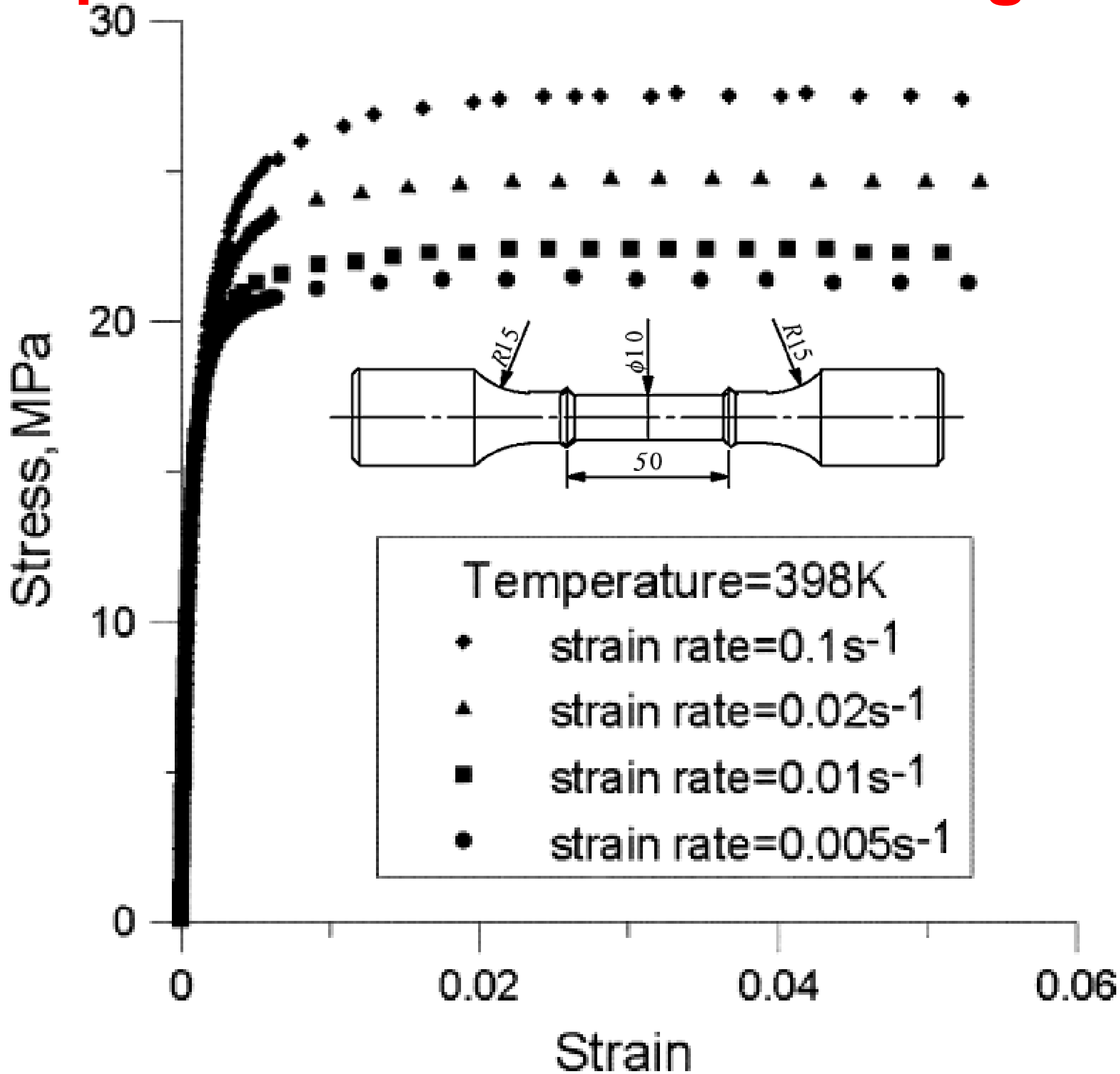
Stress-strain curves with various temperatures and strain rate = 0.02/s of Sn3.5Ag





Chen, X., Chen, G., and Sakane, M., 2005, "Prediction of Stress-Strain Relationship With an Improved Anand Constitutive Model for Lead-Free Solder Sn-3.5Ag," IEEE Trans. CPMT, 28, pp. 111–116

Stress-strain curves with various strain rates and temperature = 398°K of Sn3.5Ag



Chen, X., Chen, G., and Sakane, M., 2005, "Prediction of Stress-Strain Relationship With an Improved Anand Constitutive Model for Lead-Free Solder Sn-3.5Ag," IEEE Trans. CPMT, 28, pp. 111–116

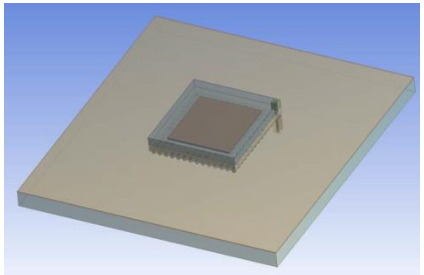
Parameters in Anand's Model with Temperature and Strain Rate Dependent for Sn3.5Ag

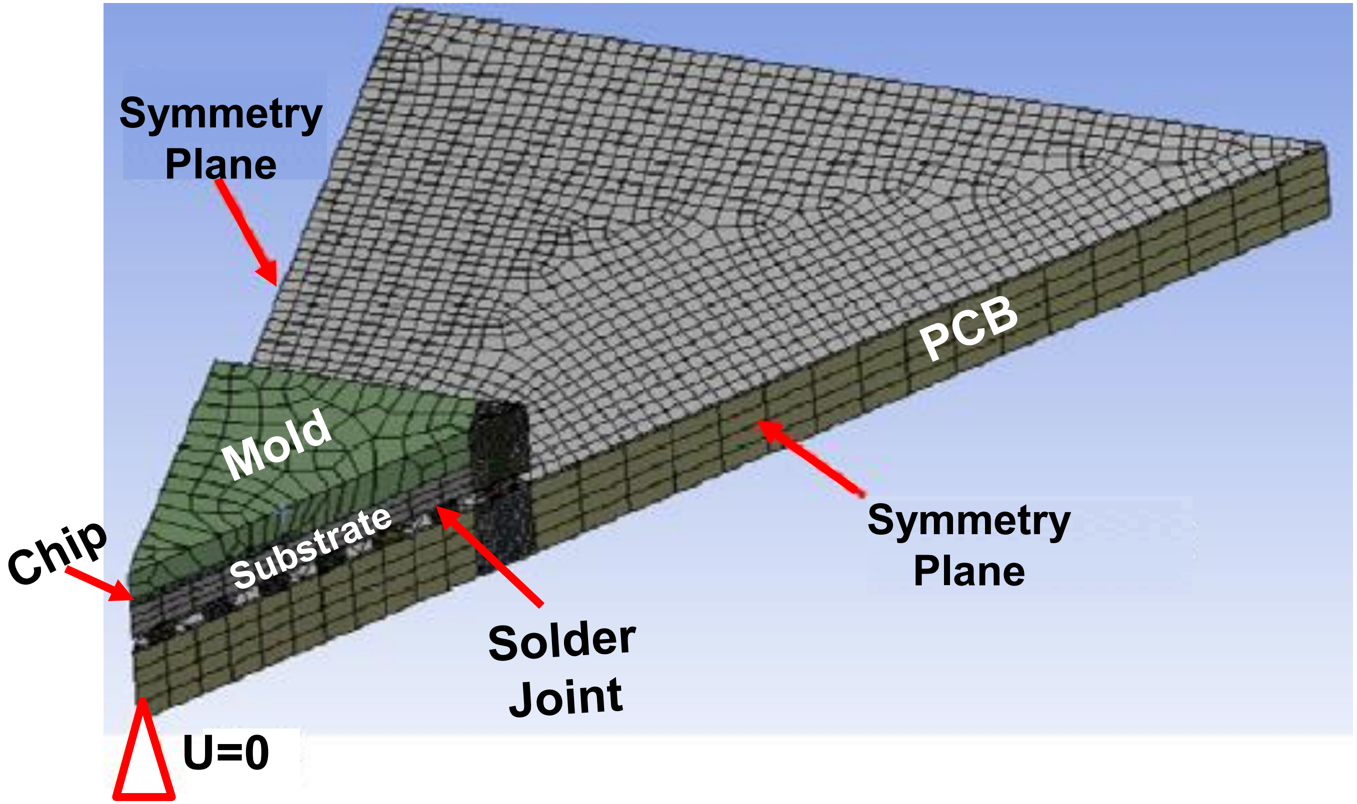
Material Constants	96.5Sn3.5Ag [Chen, et al.]
A(1/s)	177016
Q/R (°K)	10279
ξ	7
m	0.207
$\hat{s}$ (MPa)	52.4
n	0.0177
h_o (MPa)	$-90940 + 960T - 0.956T^2 - 3260582\dot{\varepsilon} + 24976816(\dot{\varepsilon})^2$
a	1.6
s_o (MPa)	$-0.0673T + 28.6$

T is in Kevin and $\dot{\varepsilon}$ is the strain rate (1/s)

Chen, X., Chen, G., and Sakane, M., 2005, "Prediction of Stress-Strain Relationship With an Improved Anand Constitutive Model for Lead-Free Solder Sn-3.5Ag," IEEE Trans. CPMT, 28, pp. 111–116

PBGA with Sn3.5Ag Solder Joints on PCB





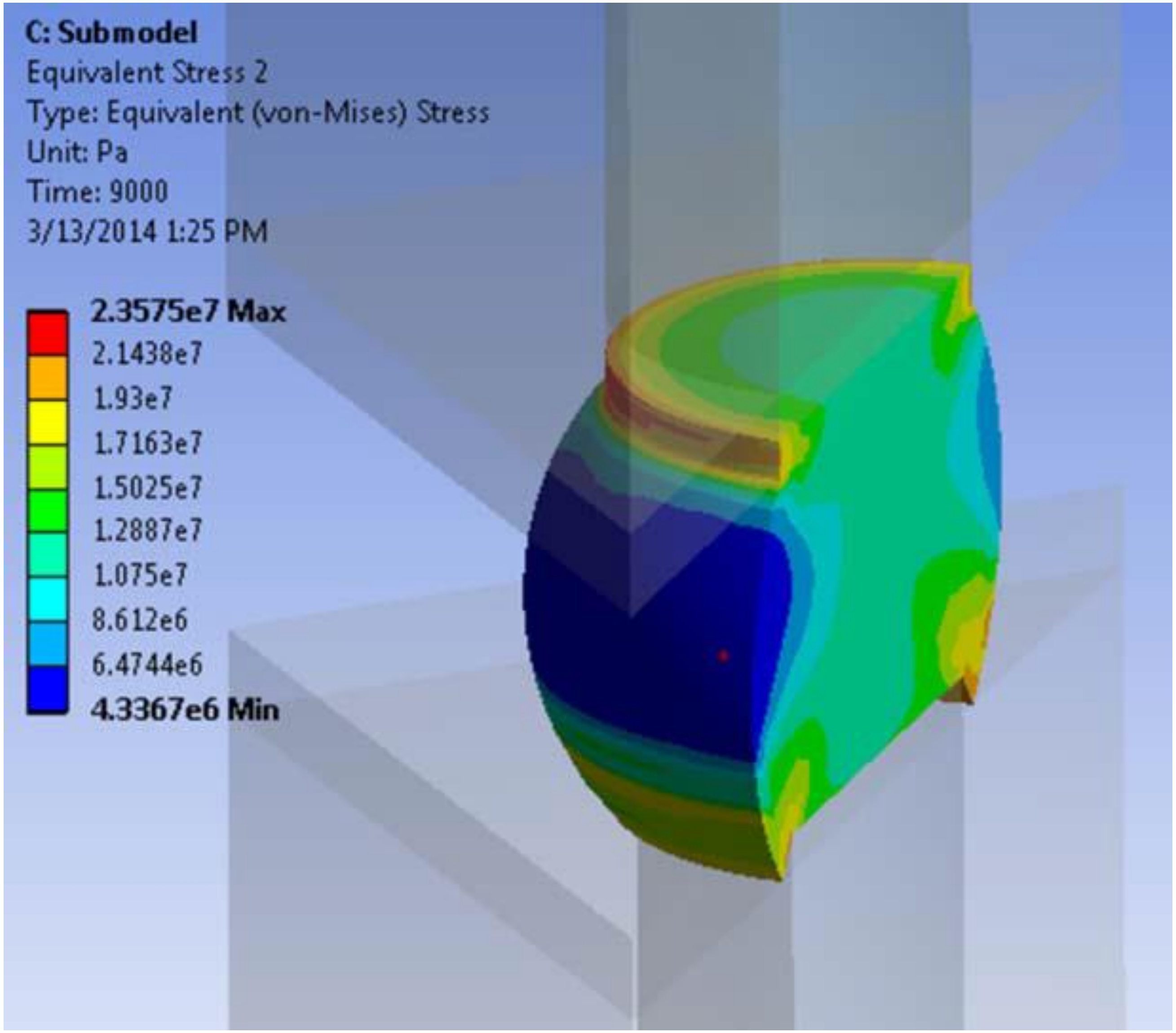
Deshpande, A., Khan, H., Mirza, F., and Agonafer, D., 2014, "Global-Local Finite Element Optimization Study to Minimize BGA Damage Under Thermal Cycling," IEEE/ITHERM Proceedings, Orlando, FL, May 27–30, pp. 483–487

Parameters in Anand's Model for Sn3.5Ag of a PBGA PCB Assembly

Material Constants	96.5Sn3.5Ag [Deshpande]
A(1/s)	177016
Q/R (°K)	10279
ξ	7
m	0.207
$\hat{s}$ (MPa)	52.4
n	0.0177
h_o (MPa)	27782
a	1.6
s_o (MPa)	9.53

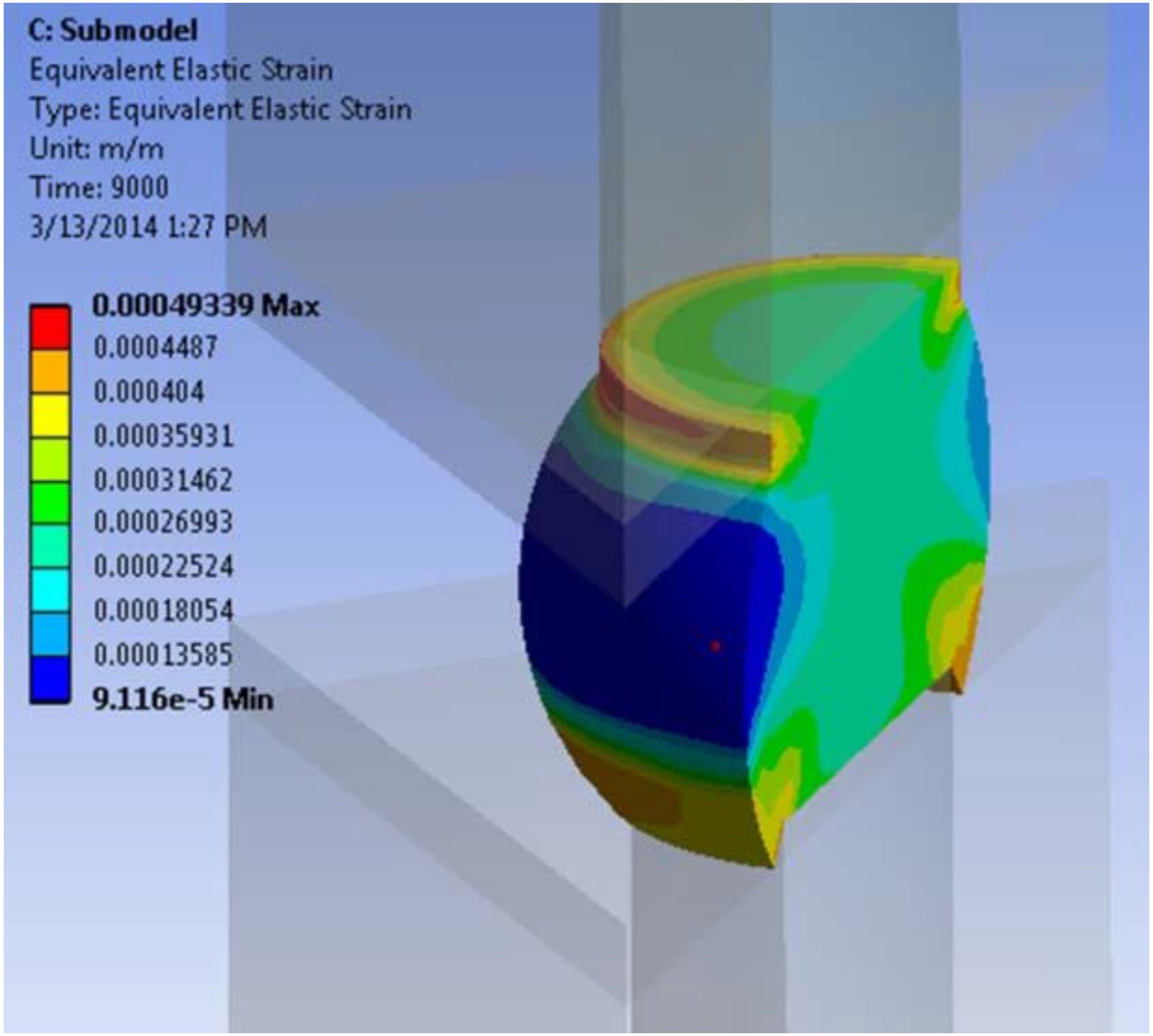
Deshpande, A., Khan, H., Mirza, F., and Agonafer, D., 2014, "Global-Local Finite Element Optimization Study to Minimize BGA Damage Under Thermal Cycling," IEEE/ITHERM Proceedings, Orlando, FL, May 27–30, pp. 483–487

Maximum Equivalent Stress Contours at Corner Solder Joint



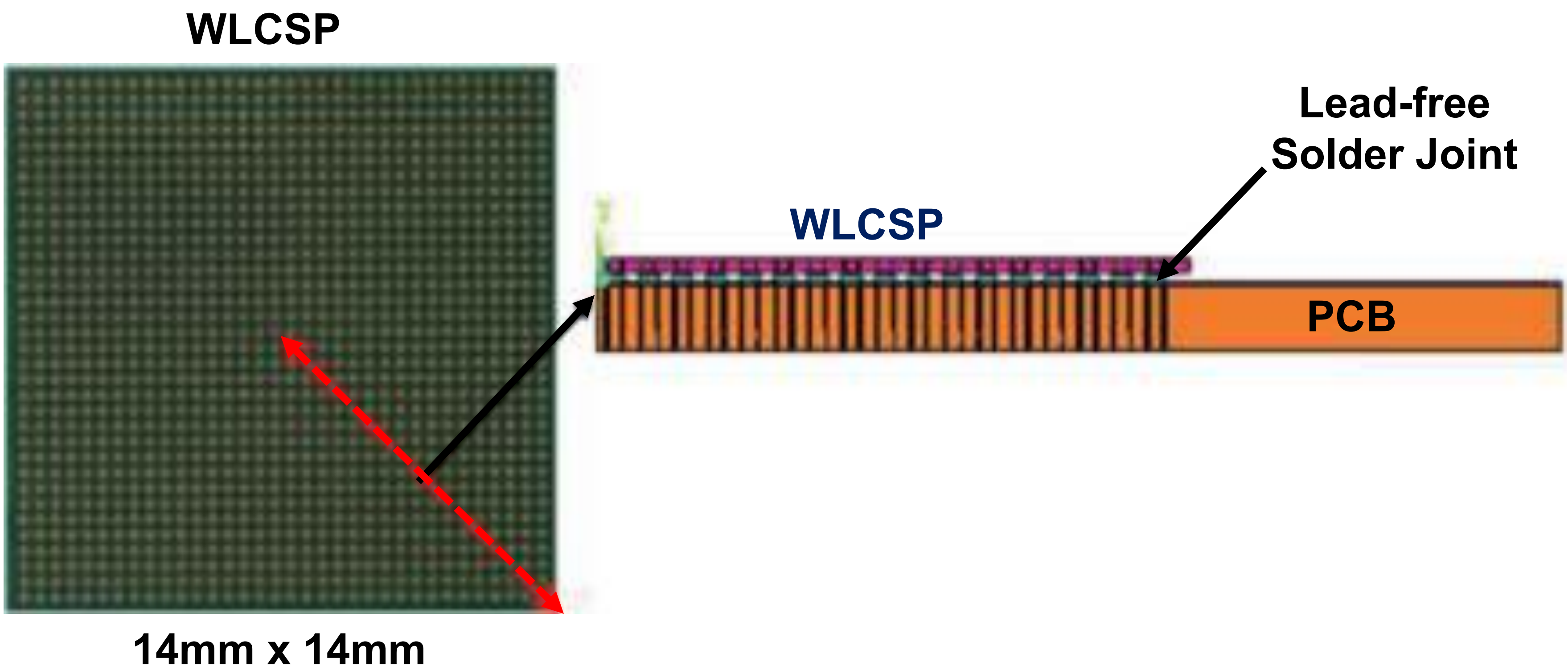
Deshpande, A., Khan, H., Mirza, F., and Agonafer, D., 2014, "Global-Local Finite Element Optimization Study to Minimize BGA Damage Under Thermal Cycling," IEEE/ITHERM Proceedings, Orlando, FL, May 27–30, pp. 483–487

Maximum Equivalent Inelastic Strain Contours at Corner Solder Joint



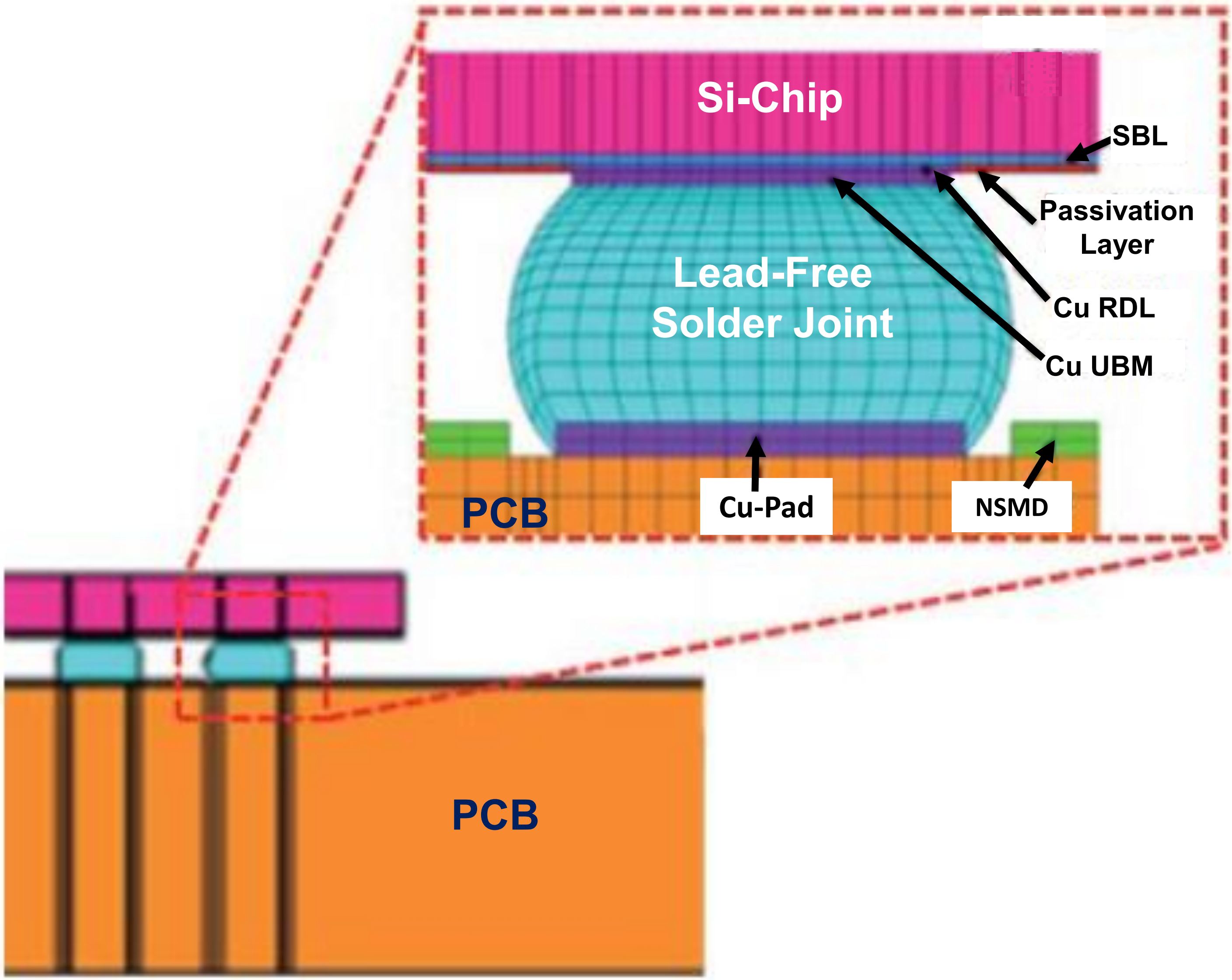
Deshpande, A., Khan, H., Mirza, F., and Agonafer, D., 2014, “Global-Local Finite Element Optimization Study to Minimize BGA Damage Under Thermal Cycling,” IEEE/ITHERM Proceedings, Orlando, FL, May 27–30, pp. 483–487

WLCSP on a PCB with Sn3.5Ag Solder Joints



Ramachandran, V., Wu, K., and Chiang, K., 2018, “Overview Study of Solder Joint Reliability Due to Creep Deformation,” J. Mech., 34(5), pp. 637–643.

2D Finite Element Model of the WLCSP PCB Assembly



Ramachandran, V., Wu, K., and Chiang, K., 2018, “Overview Study of Solder Joint Reliability Due to Creep Deformation,” J. Mech., 34(5), pp. 637–643.

Parameters in Anand's Model for Sn3.5Ag of a WLCSP PCB Assembly

Material Constants	96.5Sn3.5Ag [Ramchandran, et al.]
A(1/s)	177016
Q/R (°K)	10279
ξ	7
m	0.207
$\hat{s}$ (MPa)	52.4
n	0.0177
h_o (MPa)	27782
a	1.6
s_o (MPa)	-0.0673T + 28.6

Ramachandran, V., Wu, K., and Chiang, K., 2018, "Overview Study of Solder Joint Reliability Due to Creep Deformation," J. Mech., 34(5), pp. 637–643.

(a) Material properties of a WLCSP PCB assembly. (b) Temperature dependent Young's modulus and yield stress.

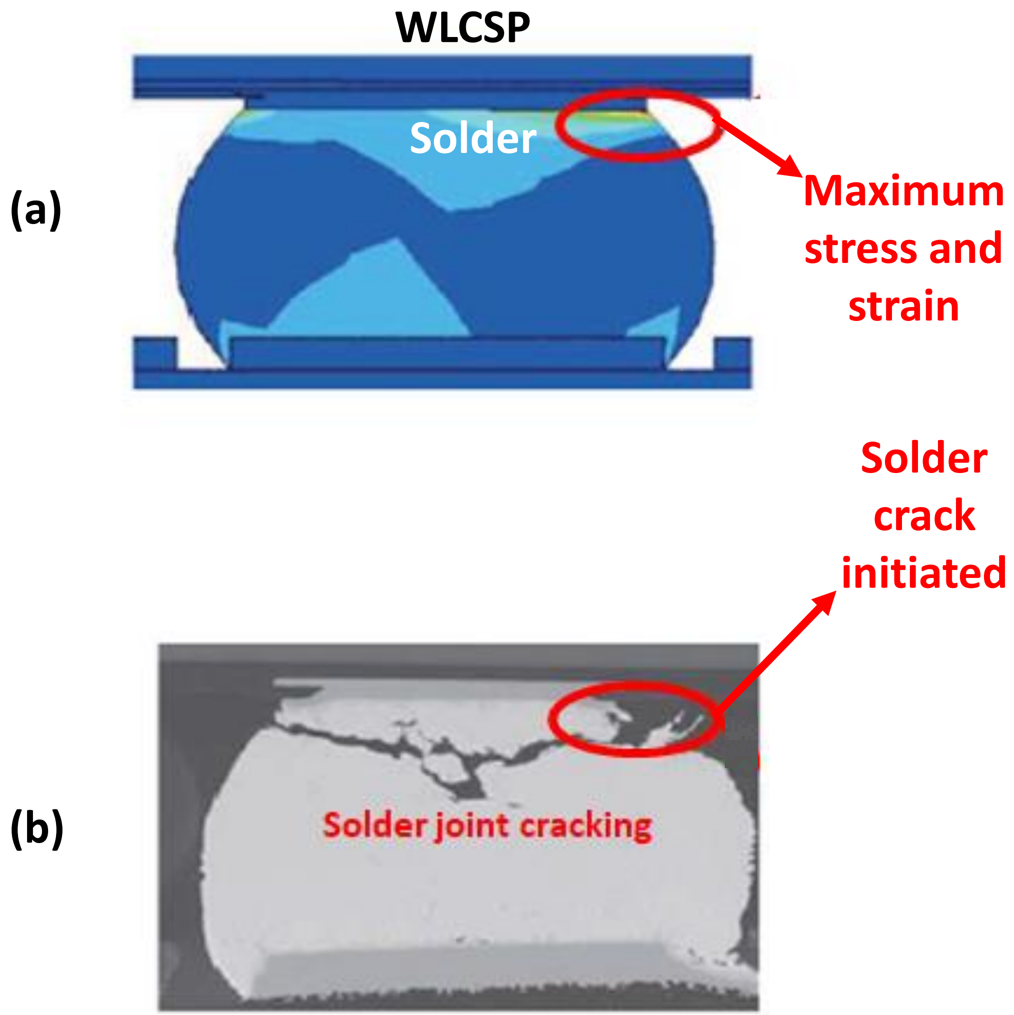
(a)

Materials	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/°C)
Silicon	150	0.28	2.62
SBL/PL	2	0.33	55
Cu	68.9	0.34	16.7
Sn3.5Ag	Non-linear	0.4	22.4
Solder Mask	6.87	0.35	19
PCB	18.3	0.19	16

(b)

96.5Sn3.5Ag Solder		
Temperature (°C)	Young's Modulus (GPa)	Yield Stress (MPa)
-40	55.3	42.2
-20	54.0	41.2
40	49.9	32.4
80	46.9	26.1
125	43.4	20.5

(a) Maximum stress/strain occur at the solder between the WLCSP and the bulk solder. (b) The failure mode from the thermal cycling test



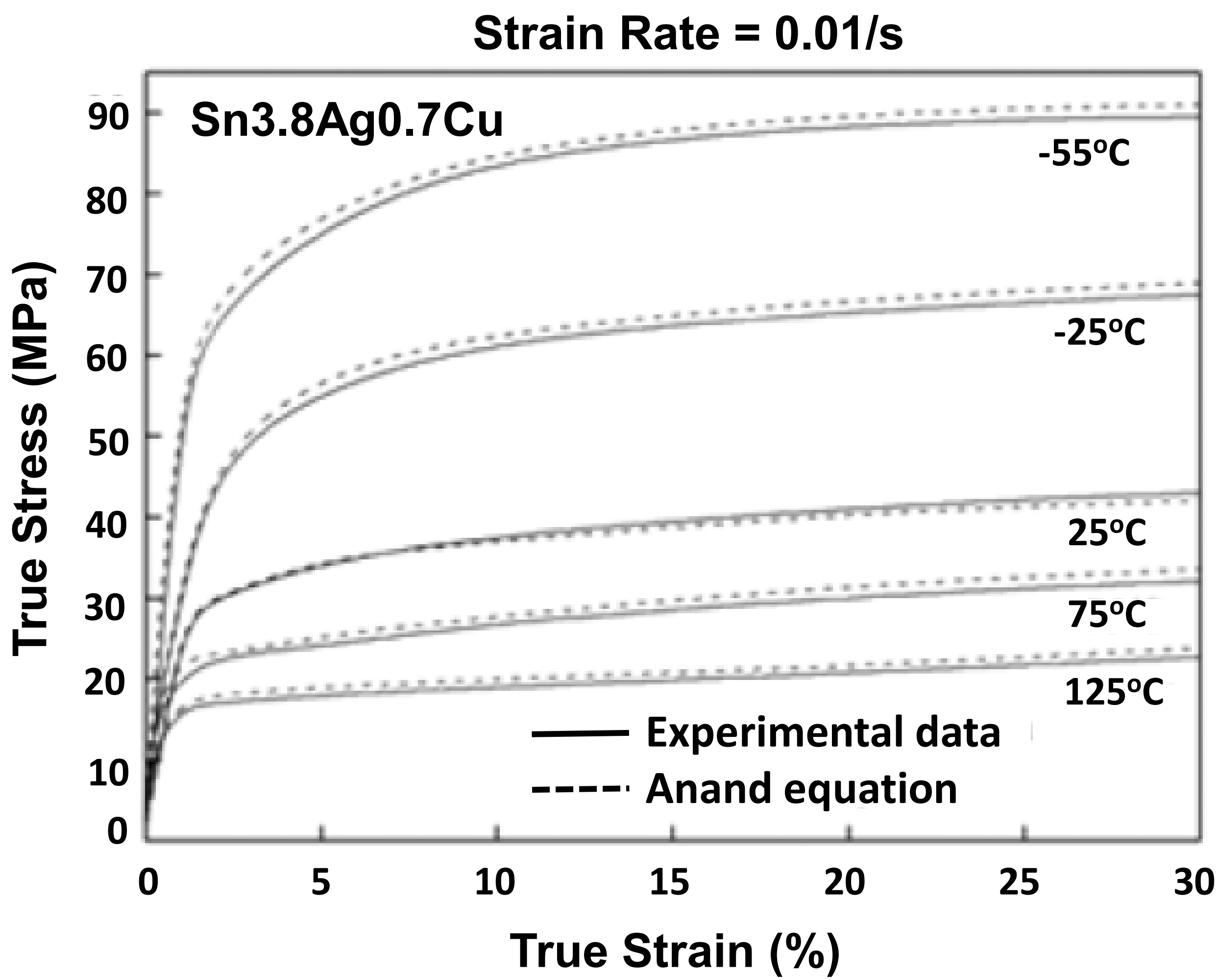
Ramachandran, V., Wu, K., and Chiang, K., 2018, "Overview Study of Solder Joint Reliability Due to Creep Deformation," J. Mech., 34(5), pp. 637–643.

Parameters in Anand's model for Sn3.8Ag0.7Cu, Sn3.8Ag0.7Cu0.03Ce, and Sn3.8Ag0.7Cu0.1Al

Material Constants	Sn3.8Ag0.7Cu [L. Zhang, 103]	Sn3.8Ag0.7Cu0.03Ce [L. Zhang, 103]	Sn3.8Ag0.7Cu0.1Al [L. Zhang, 104]
A(1/s)	24300	21200	22100
Q/R (°K)	8710	8026	8015
ξ	5.8	5	4.1
m	0.183	0.130	0.15
$\hat{s}$ (MPa)	65.3	57.6	59.0
n	0.019	0.0175	0.0154
h_o (MPa)	3541.2	4352.6	4132
a	1.9	2.3	2.0
s_o (MPa)	39.5	28.5	27.0

[103] Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.
[104] Zhang, L., Liu, Z., and Ji, Y., 2016, "Anand Constitutive Model of Lead-Free Solder Joint in 3D IC Device," Journal of Physics: Fifth International Conference on Mathematical Modeling in Physical Science, Athens, Greece, May 23–26, pp. 1–8.

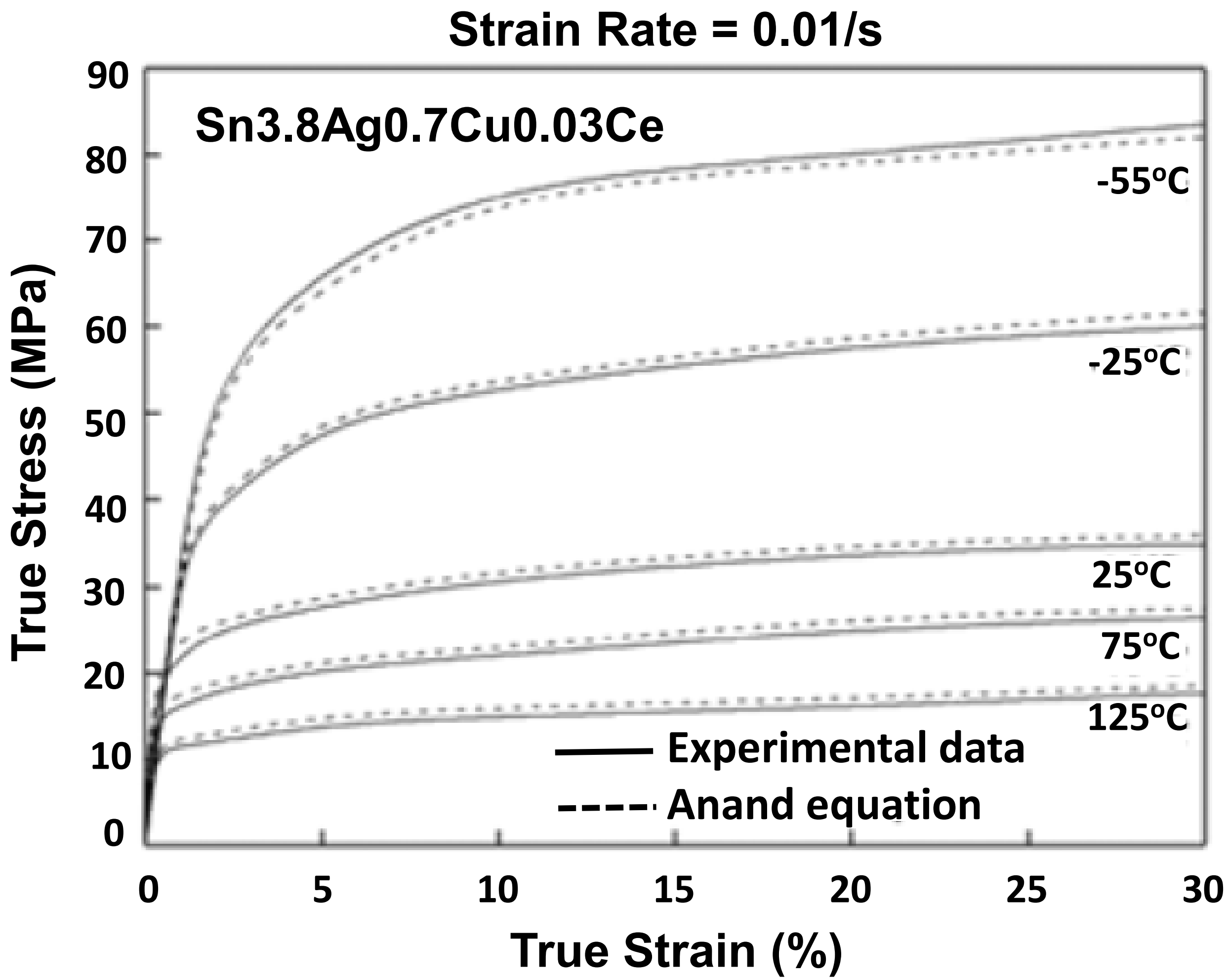
Stress-strain curves at various temperatures (strain rate = 0.01/s) for Sn3.8Ag0.7Cu solder



[103] Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.

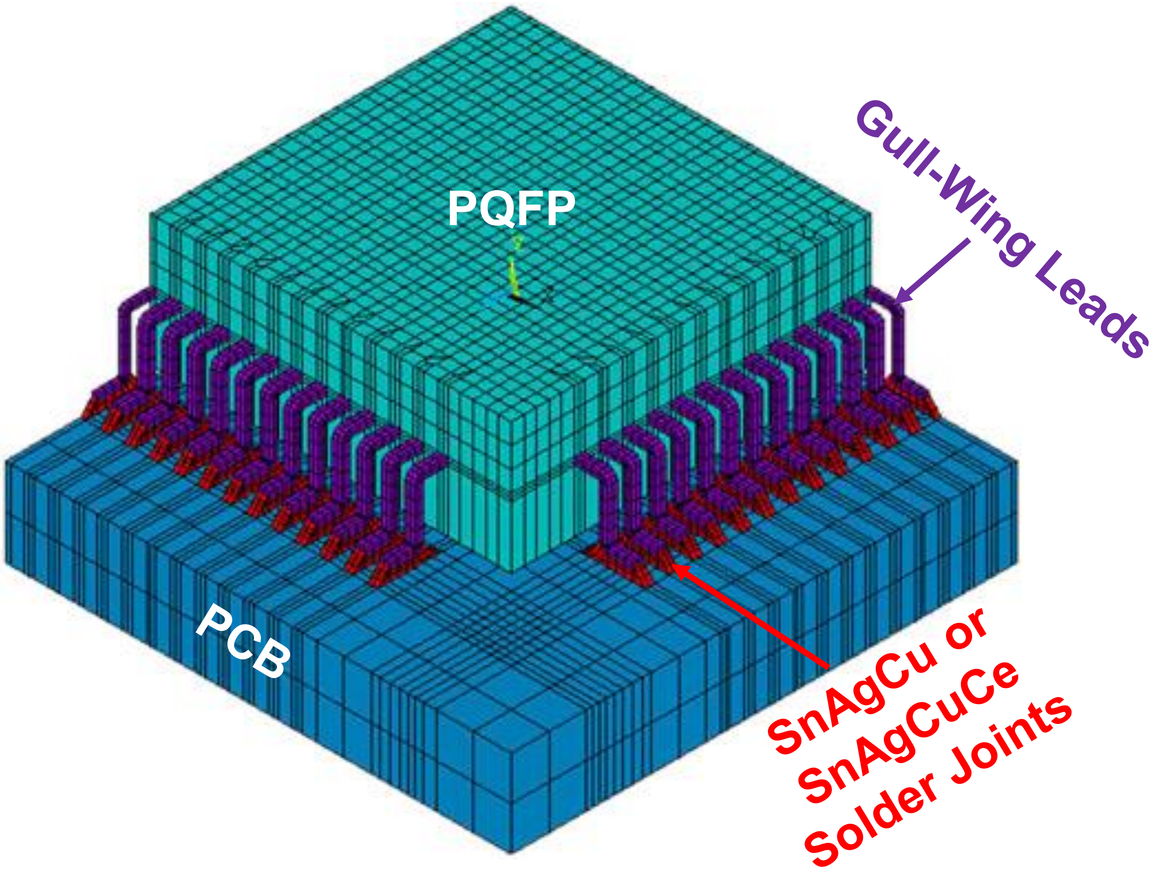
[104] Zhang, L., Liu, Z., and Ji, Y., 2016, "Anand Constitutive Model of Lead-Free Solder Joint in 3D IC Device," Journal of Physics: Fifth International Conference on Mathematical Modeling in Physical Science, Athens, Greece, May 23–26, pp. 1–8.

Stress-strain curves at various temperatures (strain rate = 0.01/s) for Sn3.8Ag0.7Cu0.03Ce solder



[103] Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.
[104] Zhang, L., Liu, Z., and Ji, Y., 2016, "Anand Constitutive Model of Lead-Free Solder Joint in 3D IC Device," Journal of Physics: Fifth International Conference on Mathematical Modeling in Physical Science, Athens, Greece, May 23–26, pp. 1–8.

Finite element model of a (quarter) PQFP package PCB assembly



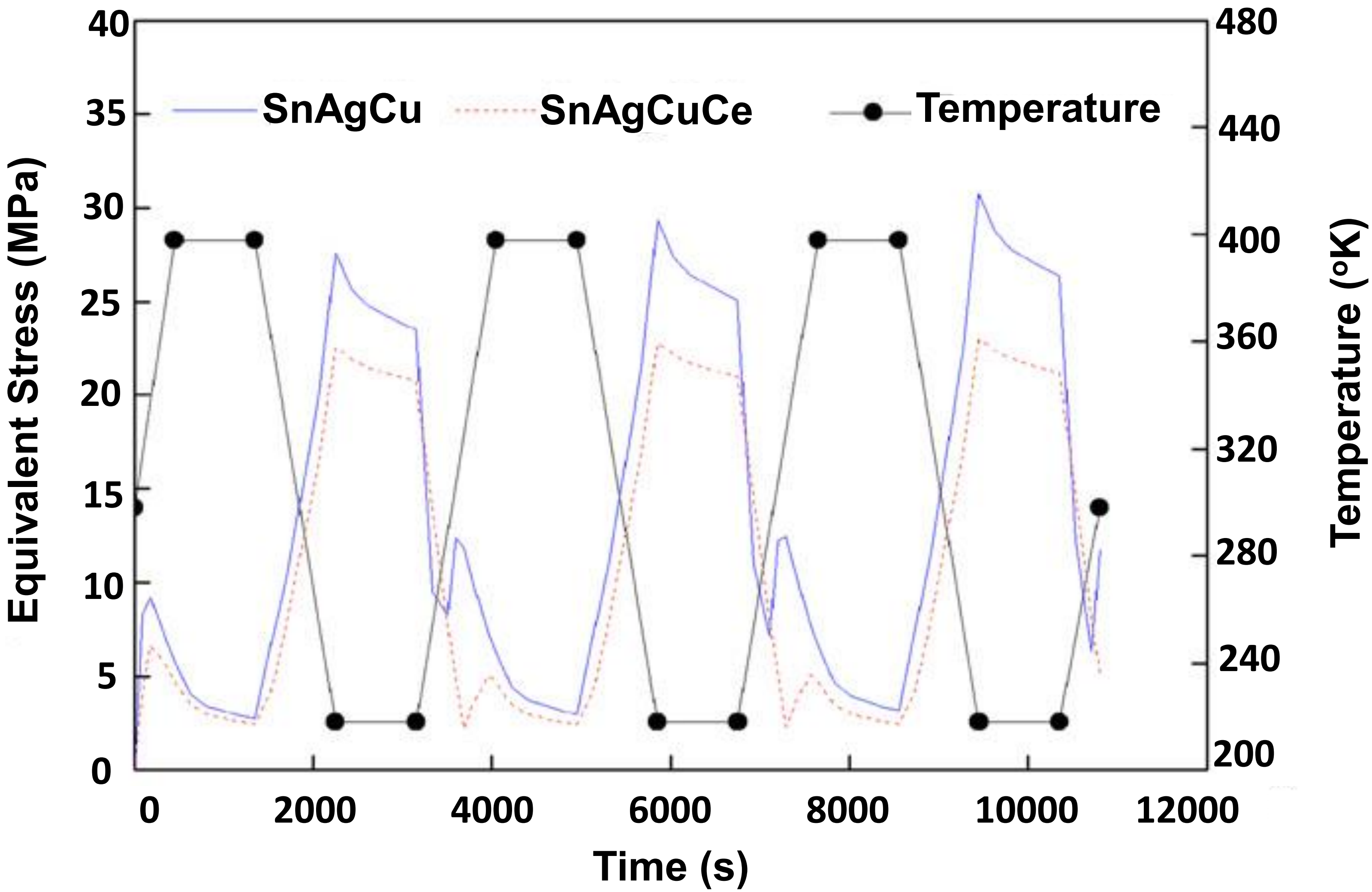
Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.

Material Properties of a PBGA PCB Assembly

Materials	E (GPa)	Poisson's Ratio	CTE (ppm/°C)
Substrate	24.5	0.22	17 (in-plane) 52 (out-of-plane)
Die	131	0.28	3
PCB	17.2	0.3	14.8
Mold	24	0.35	20
Cu Pad	110	0.34	17
Die Attach	10	0.3	33
IMC	143	0.3	18.2
Solder Mask	4	0.4	52

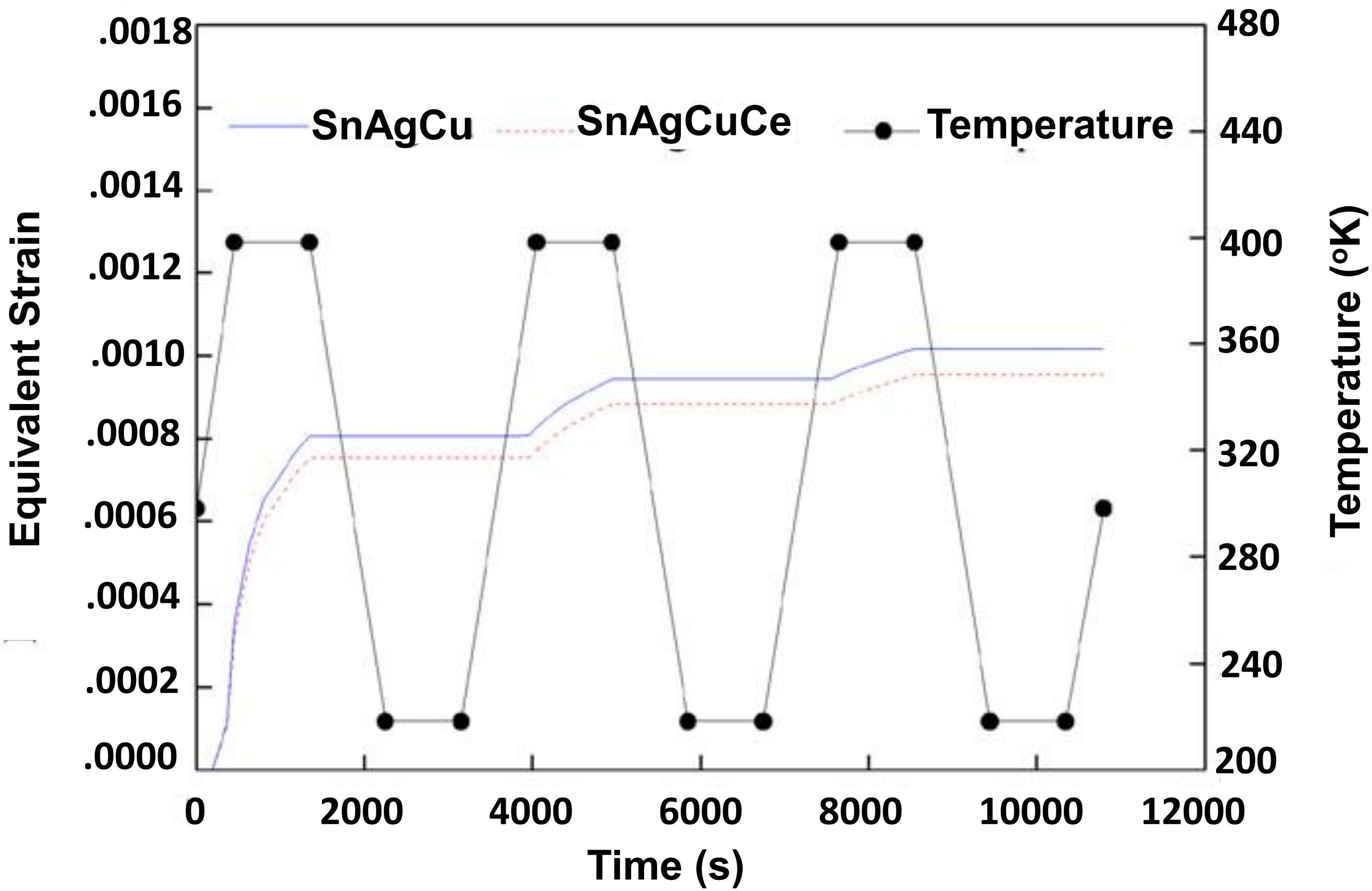
Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.

Maximum equivalent (Mises) stress (MPa) time-history at the corner solder joint



Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.

Maximum equivalent inelastic strain time-history at the corner solder joint



Zhang, L., Xue, S., Gao, L., Zeng, G., Sheng, Z., Chen, Y., and Yu, S., 2009, "Determination of Anand Parameters for SnAgCuCe Solder," Modell. Simul. Mater. Sci. Eng., 17(7), p. 075014.

Parameters in Anand's model for Sn1Ag0.5Cu after extreme aging

Anand Parameters	Sn1Ag0.5Cu (SAC105) [Basit, et al.]			
	No Aging		6 Months Aging	12 Months Aging
	WQ	RF	RF	EF
A (1/s)	5500	6900	8250	9000
Q/R (^{o}K)	8846	8850	8850	8850
ξ	4	4	4	4
m	0.25	0.215	0.16	0.16
$\hat{s}$ (MPa)	38.15	25.1	18.9	17.9
n	0.01	0.0062	0.00115	0.001
h_o (MPa)	142000	137500	60000	58750
a	1.85	1.96	2.21	2.22
s_o (MPa)	16.7	7.5	2.9	2.89

Basit, M., Ahmed, S., Motalab, M., Roberts, J. C., Suhling, J. C., and Lall, P., 2016, "The Anand Parameters for SAC Solders After Extreme Aging," IEEE/ ITHERM Proceedings, Las Vegas, NV, May 31–June 3, pp. 440–448.

Parameters in Anand's model for Sn2Ag0.5Cu after extreme aging

Anand Parameters	Sn2Ag0.5Cu (SAC205) [Basit, et al.]			
	No Aging		6 Months Aging	12 Months Aging
	WQ	RF	RF	EF
A (1/s)	3200	4300	4900	5200
Q/R (°K)	9080	9090	9090	9090
ξ	4	4	4	4
m	0.28	0.238	0.177	0.177
$\hat{s}$ (MPa)	43.0	29.0	21.6	19.94
n	0.0115	0.0087	0.00145	0.0013
h_o (MPa)	174000	169000	75000	73300
a	1.75	1.84	2.09	2.1
s_o (MPa)	27.9	16.5	5.2	5.0

Basit, M., Ahmed, S., Motalab, M., Roberts, J. C., Suhling, J. C., and Lall, P., 2016, "The Anand Parameters for SAC Solders After Extreme Aging," IEEE/ ITHERM Proceedings, Las Vegas, NV, May 31–June 3, pp. 440–448.

Parameters in Anand's model for Sn3Ag0.5Cu after extreme aging

Anand Parameters	Sn3Ag0.5Cu (SAC305) [Basit, et al.]			
	No Aging		6 Months Aging	12 Months Aging
	WQ	RF	RF	RF
A (1/s)	2800	3501	4110	4210
Q/R (°K)	9320	9320	9320	9320
ξ	4	4	4	4
m	0.29	0.25	0.18	0.18
$\hat{s}$ (MPa)	44.67	30.2	21.9	21.4
n	0.012	0.01	0.0016	0.001
h_o (MPa)	186000	180000	77540	73708
a	1.72	1.78	2.05	2.06
s_o (MPa)	32.2	21.0	5.8	5.4

Basit, M., Ahmed, S., Motalab, M., Roberts, J. C., Suhling, J. C., and Lall, P., 2016, "The Anand Parameters for SAC Solders After Extreme Aging," IEEE/ ITHERM Proceedings, Las Vegas, NV, May 31–June 3, pp. 440–448.

Parameters in Anand's model for Sn4Ag0.5Cu after extreme aging

Anand Parameters	Sn4Ag0.5Cu (SAC405) [Basit, et al.]			
	No Aging		6 Months Aging	12 Months Aging
	WQ	RF	RF	EF
A (1/s)	2650	3175	3725	3800
Q/R (°K)	9560	9580	9580	9580
ξ	4	4	4	4
m	0.3	0.263	0.184	0.184
$\hat{s}$ (MPa)	45.51	31.3	22.2	23
n	0.0123	0.011	0.0018	0.0014
h_o (MPa)	192000	183000	80000	79840
a	1.7	1.77	2.01	2.01
s_o (MPa)	34.35	23.65	6.2	6.14

Basit, M., Ahmed, S., Motalab, M., Roberts, J. C., Suhling, J. C., and Lall, P., 2016, "The Anand Parameters for SAC Solders After Extreme Aging," IEEE/ ITHERM Proceedings, Las Vegas, NV, May 31–June 3, pp. 440–448.

THERMAL-FATIGUE LIFE PREDICTION

There are many thermal-fatigue life prediction models of solder joints in the literature. A couple simple models are shown below.

$$N_f = \sum_j \alpha_j [\Delta W]^{\beta_j} \quad (1)$$

and

$$N_f = \sum_j \alpha_j \left[\frac{\sum_i \Delta W_i \text{ x } V_i}{\sum_i V_i}\right]^{\beta_j} \quad (2)$$

where N_f is the thermal fatigue life, and α_j and β_j are constants to be determined by experiments (usually isothermal fatigues) for a specific component/package and solder joint. ΔW_i is the creep (or inelastic) strain energy density (or accumulated equivalent creep strain) per cycle in the *i*th element determined from finite element simulations, and V_i is the volume of that *i*th element.

The value of ΔW_i depends on the accuracy of material properties of the structure. These include the solder joint, package, chip, PCB, and etc.

The value of ΔW_i also depends on the construction of the finite element model. This includes finer mesh to capture the stress/strain concentration areas.

Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", ASME Transactions, Journal of Electronic Packaging, June 2021, pp. 1-36.

Notes

In the literature, many authors called N_f the reliability (number of thermal cycle) of solder joint.

Actually, it should be emphasized that the reliability (N_f) obtained from DFR and thermal fatigue life prediction equation, is not the same as the reliability (probability) obtained from reliability tests.

For example, the life (number of cycles-to-failure) of the solder joints from reliability tests depends on the percent failed (or survived). Statistically, there are an infinite number of possible lives, e.g., the characteristic life is corresponding 63.2% failed (or 32.8% survived).

On the other hand, the best one can do from DFR is to predict a (one) life of the solder joint for a given material and geometry of the structure, and given boundary condition, and from a thermal-fatigue life prediction model.

Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", ASME Transactions, Journal of Electronic Packaging, June 2021, pp. 1-36.

Notes (Continue)

Many authors compare the reliability, N_f (number of thermal cycle) to the cycle-to-failure at 1% failure from the reliability test. If they find the value of N_f is too big, then they compare to the cycle-to-failure at 50% or 63.2% failures from the reliability test. Actually, N_f and the reliability from test are two different things and cannot be compared.

One more thing, many authors use finite element simulation to determine the maximum value of ΔW and then substitute into Equation (1) and calculate the N_f. It should be emphasized that the calculated maximum value is acting only at one point in an element (usually near the corner) of the solder joint. The way what they do is (unknowingly) presuming that ΔW is uniformly distributed through the whole volume of the solder joint. There is another thing, even some authors don't assume the uniformity of the ΔW, i.e., use Equation (2), they still have to assume a crack propagation path of the solder joint to calculate the N_f.

Finally, it should be pointed out that all the low-cycle thermal-fatigue life prediction models for lead-free solder joints in the literatures have not been experimentally (satisfactorily) verified. More works should be done in this area.

Lau, J. H., "State of the Art of Lead-Free Solder Joint Reliability", ASME Transactions, Journal of Electronic Packaging, June 2021, pp. 1-36.

SUMMARY AND RECOMMENDATIONS

- **Reliability engineering consists of three major tasks, namely, DFR (design for reliability), reliability testing and data analysis, and failure analysis.**
- **Reliability of an interconnect (e.g., solder joint) of a particular package in an electronic product is defined as the probability that the interconnect will perform its intended function for a specified period of time under a given operating condition without failure.**
- **Interconnect (e.g., solder joint) reliability should be determined by reliability tests. The objective of reliability tests is to obtain failures (the more, the better) and to best fit the failure data to estimate the parameters of a chosen probability distribution, *F(x)*. Once *F(x)* is estimated, the reliability, failure rate, cumulative failure rate, average failure rate, mean-time-to-failure, etc., of the interconnect are readily determined.**
- **The life distribution, *F(x)*, is package/component dependent. Actually, it is also affected by the chip size, solder alloy, type of pastes, PCB thickness, PCB material, number of copper layer in PCB, reflow condition, solder joint volume, voids in solder joint, test condition, continuity measurement, number of measurement during each cycle, data acquisition system, failure criterions, data analysis method, etc.**
- **Examples on using the Weibull and Lognormal life distributions for lead-free solder joints under thermal-cycling and drop tests have been provided.**
- **True Weibull slope, true characteristic life, and true mean life have been briefly mentioned.**

SUMMARY AND RECOMMENDATIONS

- **All the papers in the literature are dealing with liner acceleration, i.e., $x_o = \alpha x_T$, or $N_o = \alpha N_T$, where α is the linear acceleration factor. Other accelerations and factors have to be investigated.**
- **Linear acceleration factors for various lead-free solder alloys based on: (a) frequency and maximum temperature, (b) dwell time and maximum temperature, and (c) frequency and mean temperature have been presented.**
- **The advantages of DFR are to: (a) eliminate trial-and-error of reliability tests, (b) provide insight into the physical, chemical, electrical, mechanical, and thermal behaviors of the solder joints, e.g., failure location and failure mode, and (c) provide comparison between material properties and structural geometries of package, PCB, and solder joints.**
- **The most important property of DFR of solder joints is the constitutive equation of the solder alloy.**
- **Norton power creep constitutive equations and examples for Au20Sn, Sn58Bi, Sn3.8Ag0.7Cu, and Sn3.8Ag0.7Cu0.03Ce have been provided.**
- **Wises two power creep constitutive equations and examples for Sn3.5Ag and Sn4Ag0.5Cu have been provided.**
- **Garofalo hyperbolic sine creep constitutive equations and examples for Sn3.5Ag, Sn3Ag0.5Cu, Sn3.9Ag0.6Cu, Sn3.8Ag0.7Cu, Sn3.5Ag0.5Cu, and Sn3.5Ag0.75Cu, Sn4Ag0.5Cu, Sn(3.5-3.9)Ag(0.5-0.8)Cu, 100In, Sn52In, Sn3.8Ag0.7Cu0.03Ce, and Au20Sn have been provided.**

SUMMARY AND RECOMMENDATIONS

- Anand viscoplasticity constitutive equations and examples for Sn3.5Ag, Sn3Ag0.5Cu, Sn3.8Ag0.7Cu, Sn3.8Ag0.7CuCe, Sn3.8Ag0.7CuAl, Au20Sn, Sn3.5Ag with temperature and strain rate dependent parameters, and Sn1Ag0.5Cu, Sn2Ag0.5Cu, Sn3Ag0.5Cu, and Sn4Ag0.5Cu after extreme aging have been provided.
- The above four types of constitutive equations can be input into the commercial computer simulation codes such as ANSYS and ABAQUS.
- The constants α_i and β_i have to be determined (isothermal fatigue test) for a specific component/package and solder alloy. However, how to relate the isothermal fatigue to the low-cycle thermal fatigue is a key question need to be answered. More research works need to be done in this area.
- The calculated value of ΔW_i depends on the accuracy of material properties of the structures. These include the solder joint, package, PCB, etc.
- The accuracy of the calculated ΔW_i also depends on the construction of the finite element model. This includes the finer meshes for the stress/strain concentration areas of the solder joints.
- The reliability, N_f (number of thermal cycle) obtained from DFR, e.g., Equations (1) or (2), is not the same as the reliability (probability) obtained from reliability tests. They cannot be compared.
- In this lecture, there is not any intention to present/propose thermal-fatigue life prediction models for the determination of N_f (reliability) of lead-free solder joints through the DFR. More new models and experimental works should be done in this area.

Thank You Very Much for Your Attention!

☺

A. Reliability of 6-Side Molded Panel-Level Chip-Scale Packages (PLCSPs)

B. Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration

C. Development of High-Density Hybrid Substrate for Heterogeneous Integration

Reliability of 6-Side Molded Panel-Level Chip-Scale Packages (PLCSPs)

John H Lau, Cheng-Ta Ko, Chia-Yu Peng, Tzvy-Jang Tseng, Kai-Ming Yang, Tim Xia, Puru Bruce Lin, Eagle Lin, Leo Chang, Hsing Ning Liu, Curry Lin, Yan-Jun Fan, David Cheng, and Winnie Lu

Unimicron Technology Corporation

- Lau, J. H., C. Ko, T. Tseng, K. Yang, C. Peng, T. Xia, P. Lin, E. Lin, L. Chang, H. Liu, and D. Cheng, "Panel-Level Chip-Scale Package with Multiple Diced Wafers", *IEEE Transactions on CPMT*, Vol. 10, No. 7, July 2020, pp. 1110-1124.
- Lau, J. H., C. Ko, T. Tseng, T. Peng, K. Yang, T. Xia, P. Lin, E. Lin, L. Chang, N. Liu, C. Lin, D. Cheng, and W. Lu, "Six-Side Molded Panel-Level Chip-Scale Package with Multiple Diced Wafers", *IMAPS Transactions, Journal of Microelectronics and Electronic Packaging*, Vol. 17, No. 4, December 2020, pp. 111-120.

CONTENTS

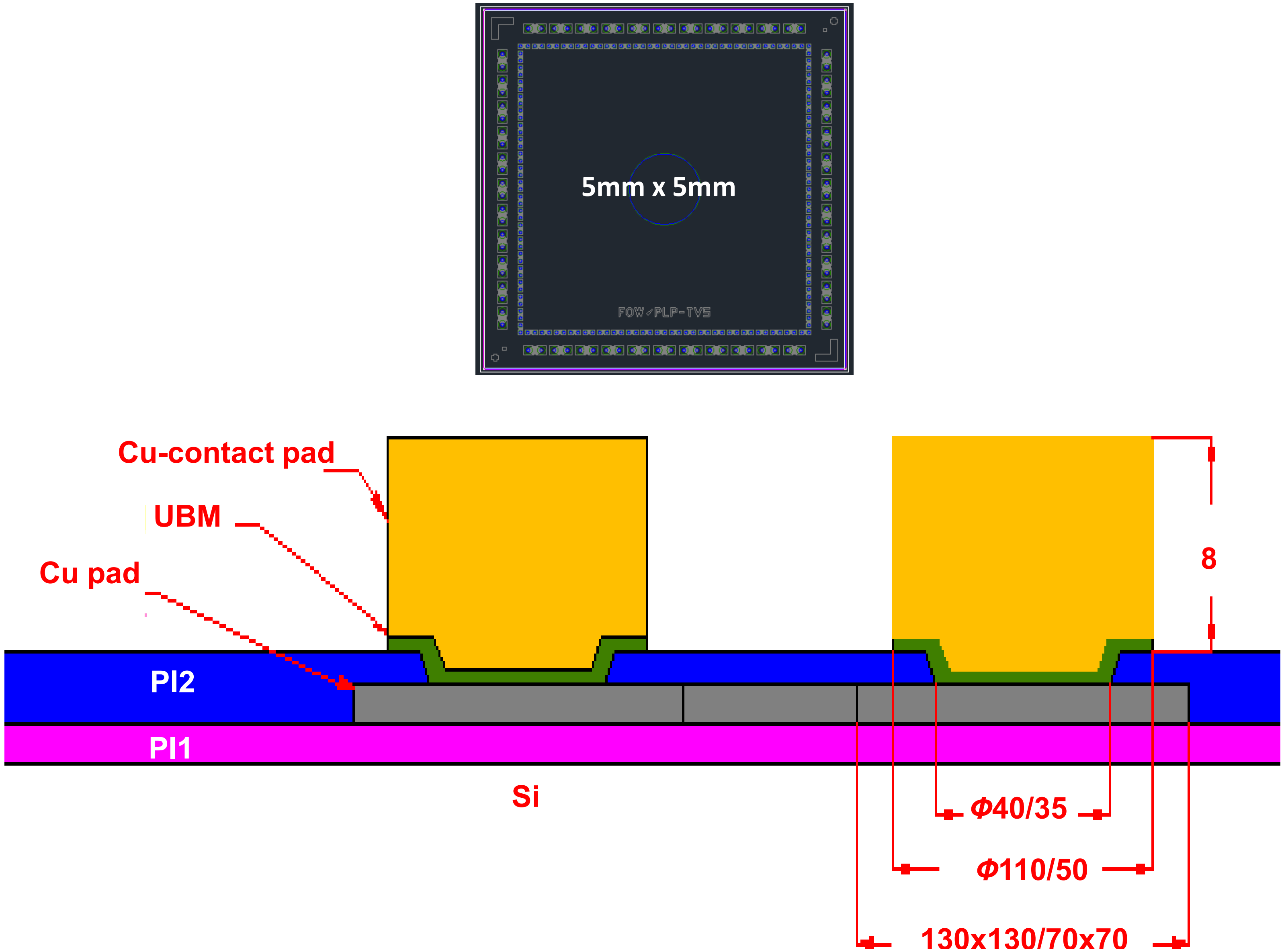
- **INTRODUCTION**
- **TEST CHIP AND TEST PACKAGE**
- **PROCESS FLOW IN FABRICATING THE 6-SIDE MOLDED PLCSP**
- **PCB ASSEMBLY OF THE PLCSPs**
- **THERMAL CYCLING TEST OF PLCSPs**
- **THERMAL CYCLING SIMULATION OF THE PLCSP PCB ASSEMBLIES**
- **SUMMARY**

Why use the Higher Cost 6-Side Molded PLCSP?

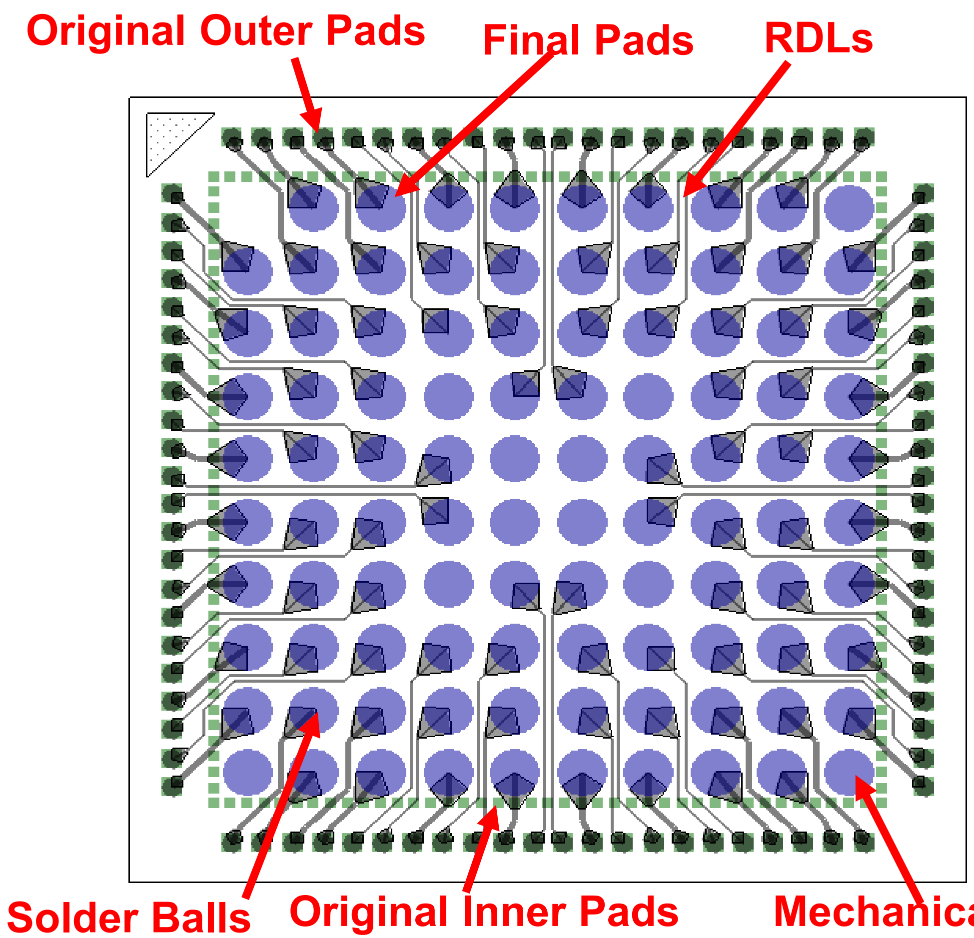
Because:

- of the delamination of the dielectric layer in the front-side of the WLCSP, which is particularly true for advanced nodes (< 14nm process technology) products with fragile polyimides,
- of the back-side chipping and sidewall cracking due to the mechanical blade dicing the wafer,
- of the concern of the handling and SMT (surface mount technology) pick and place to damage the chip, and
- in automotive electronics, the trends are driving lead-free solder joint reliability for new functions such as the advanced driver-assistance systems (ADAS), under-the-hood operations often require high sustained heating/cooling temperatures.

Test Chip


5mm x 5mm
FOW/PLP-TV5
Cu-contact pad
UBM
Cu pad
PI2
PI1
Si
8
Φ40/35
Φ110/50
130x130/70x70

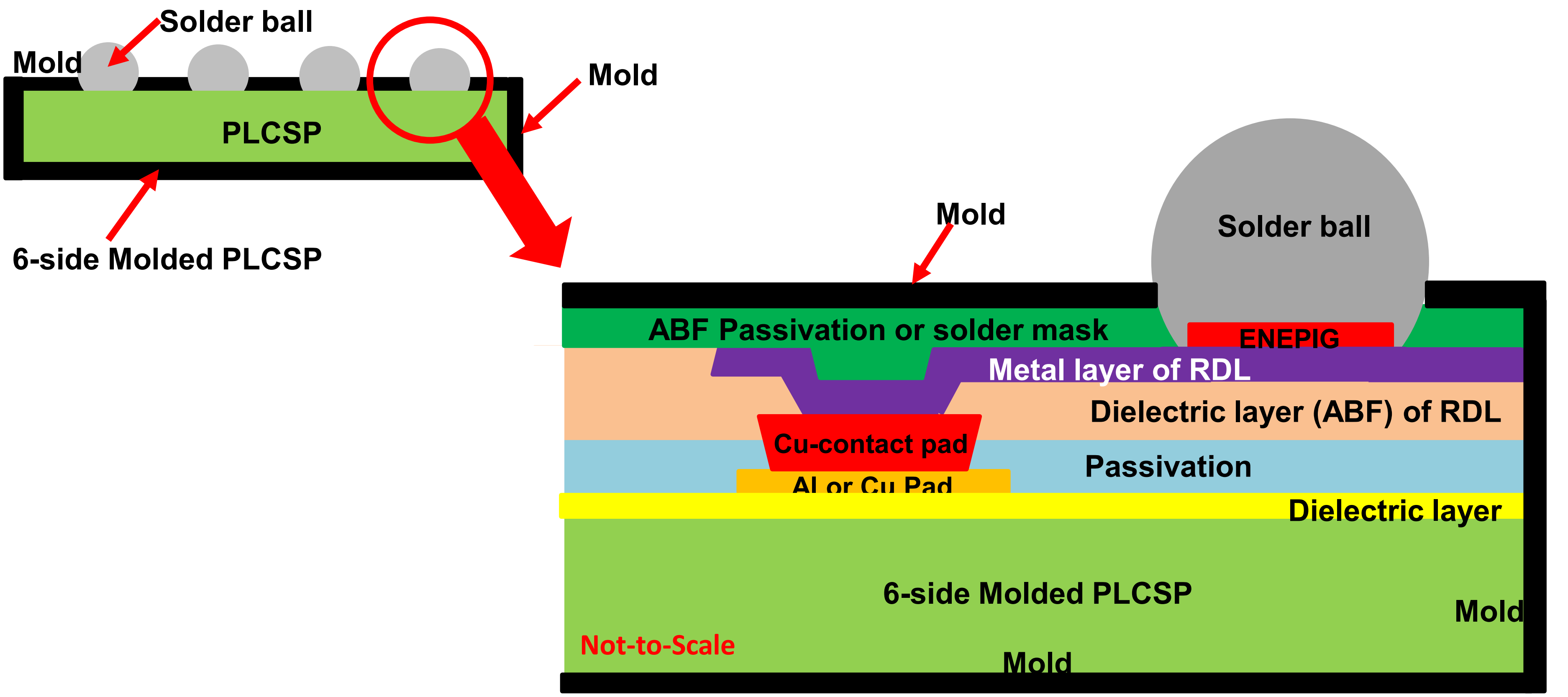
Top-View of the Test Package



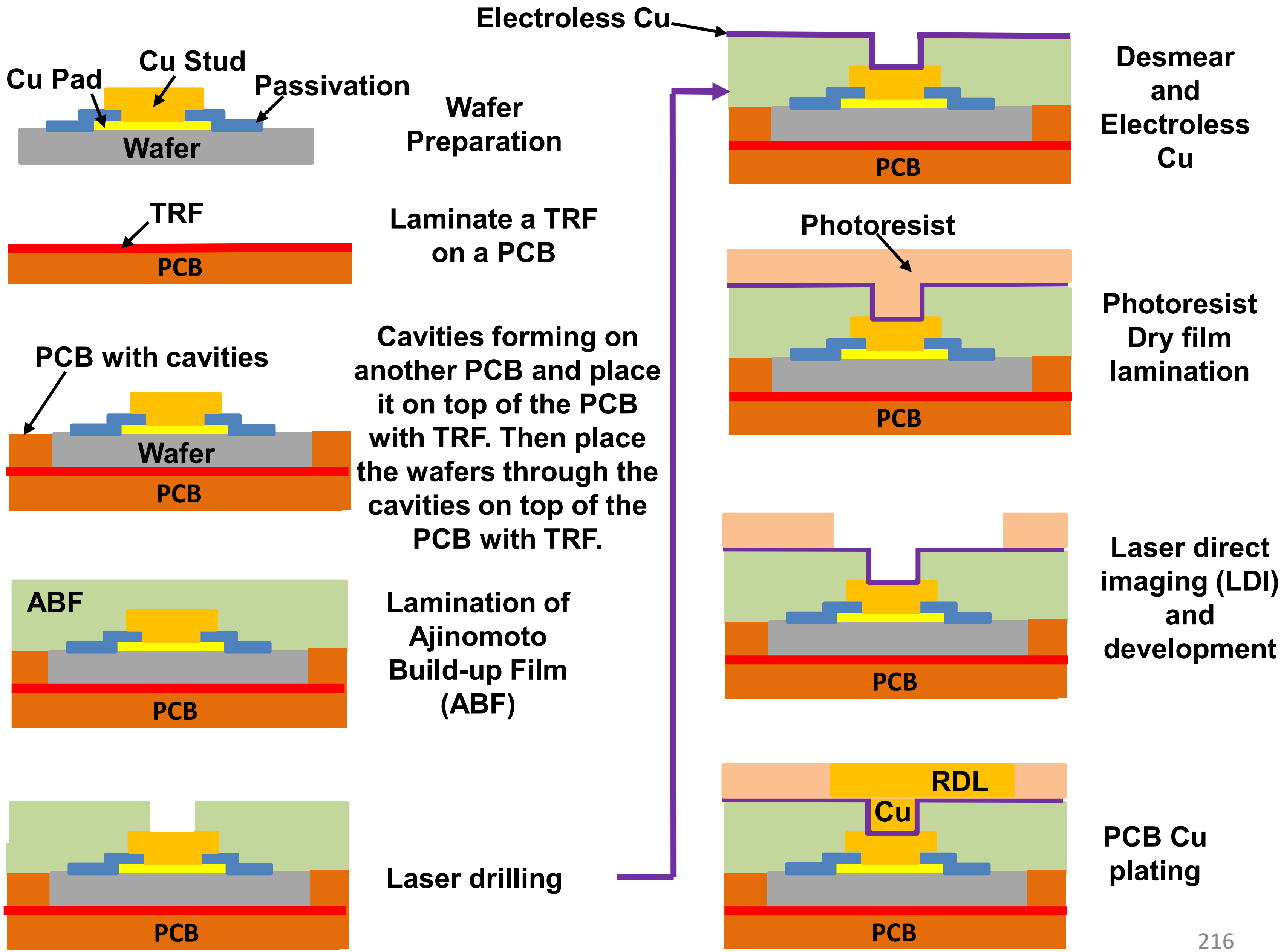
6-side Molded PLCSP

- Package Size: 5mm X 5mm
- RDL L/S : 20/20µm
- Via drill/Pad : 50/110µm
- Ball pitch: 0.4mm
- Ball Pad: 300µm
- Ball SRO: 220µm
- Ball Size: 200µm
- Ball Count: 99

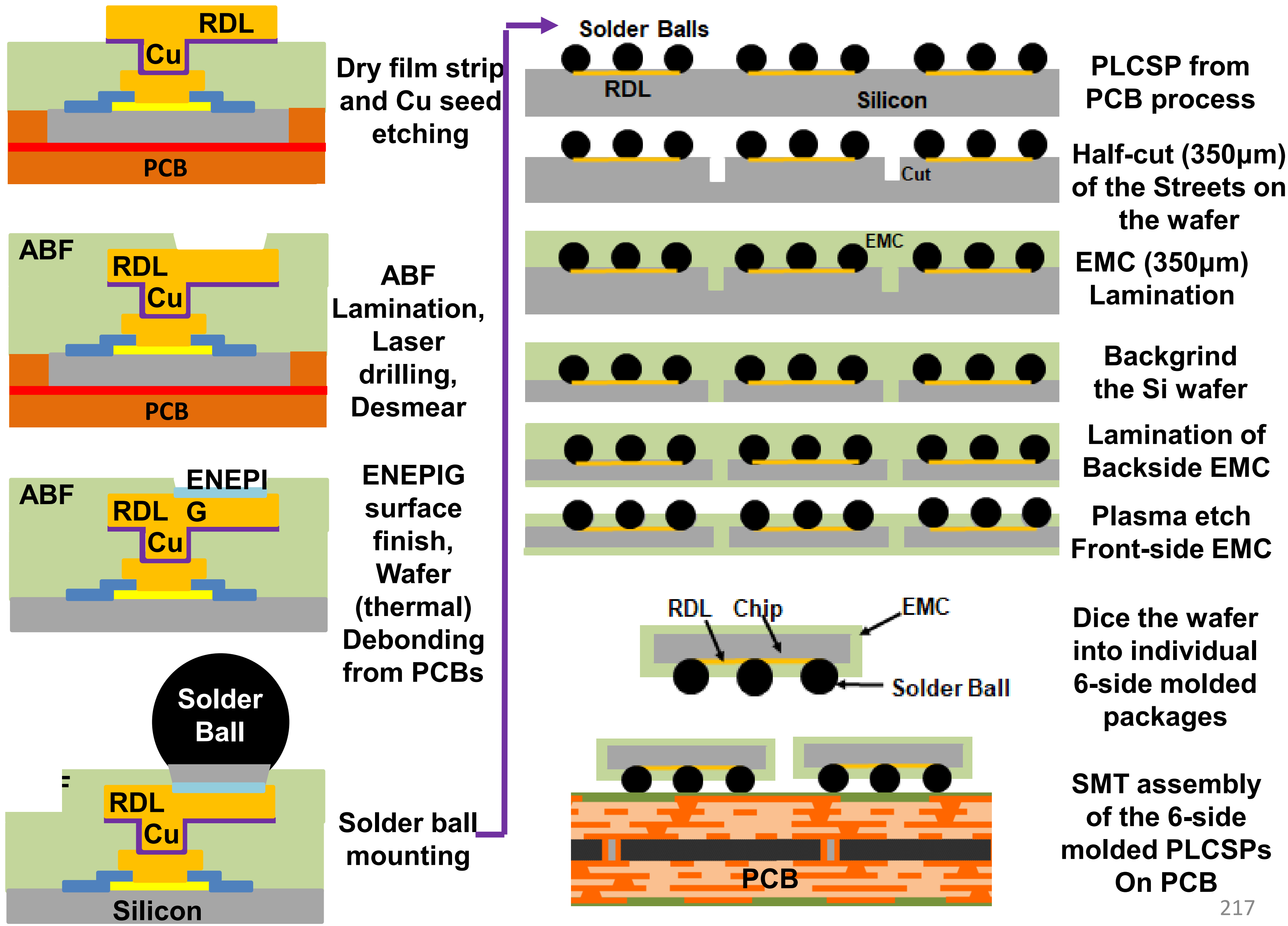
Cross Section of the 6-Side Molded PLCSP



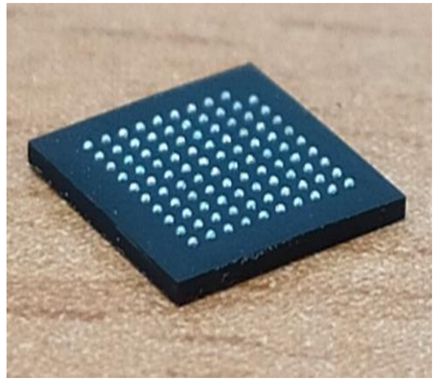
Key process steps in fabricating the PLCSP

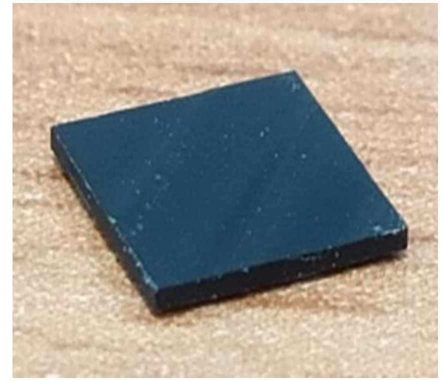


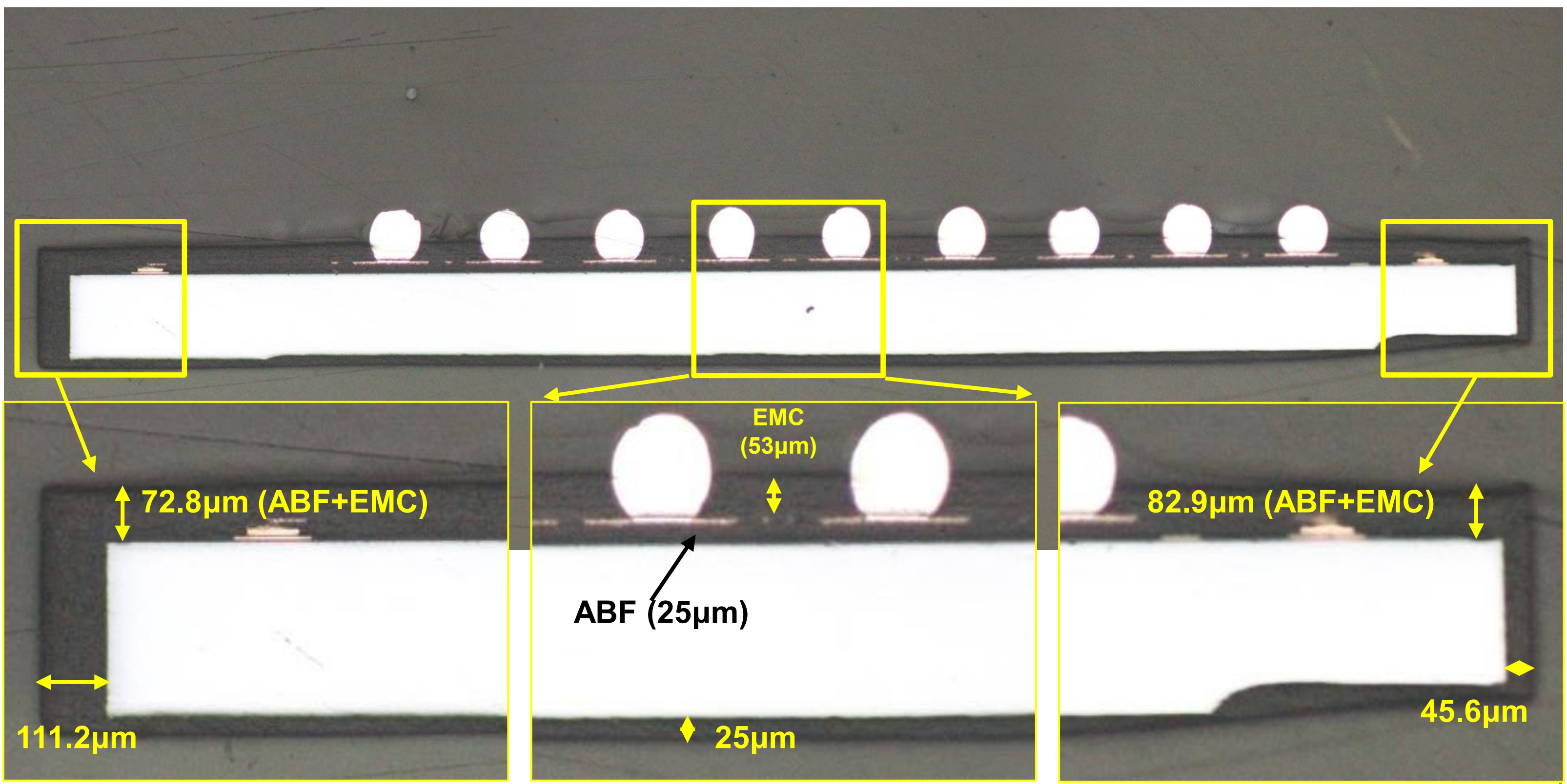
Continue to fabricate the 6-side molded PLCSP.



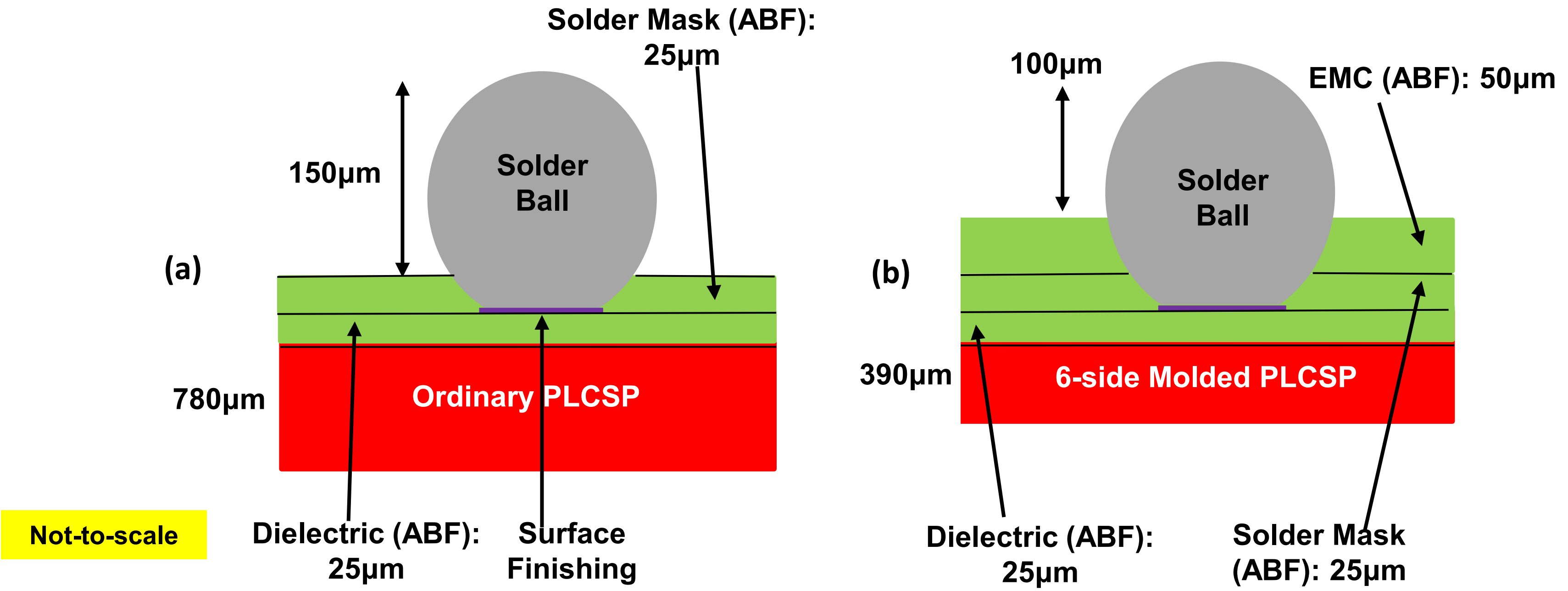
Various-View of the 6-side Molded PLCSP

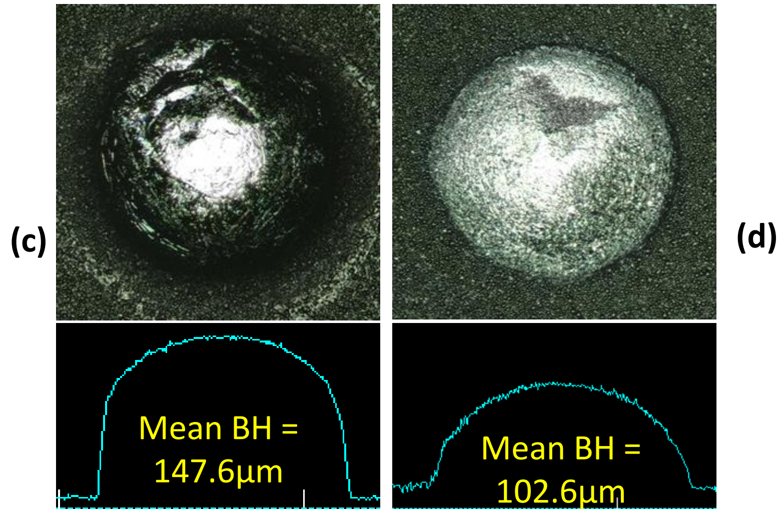






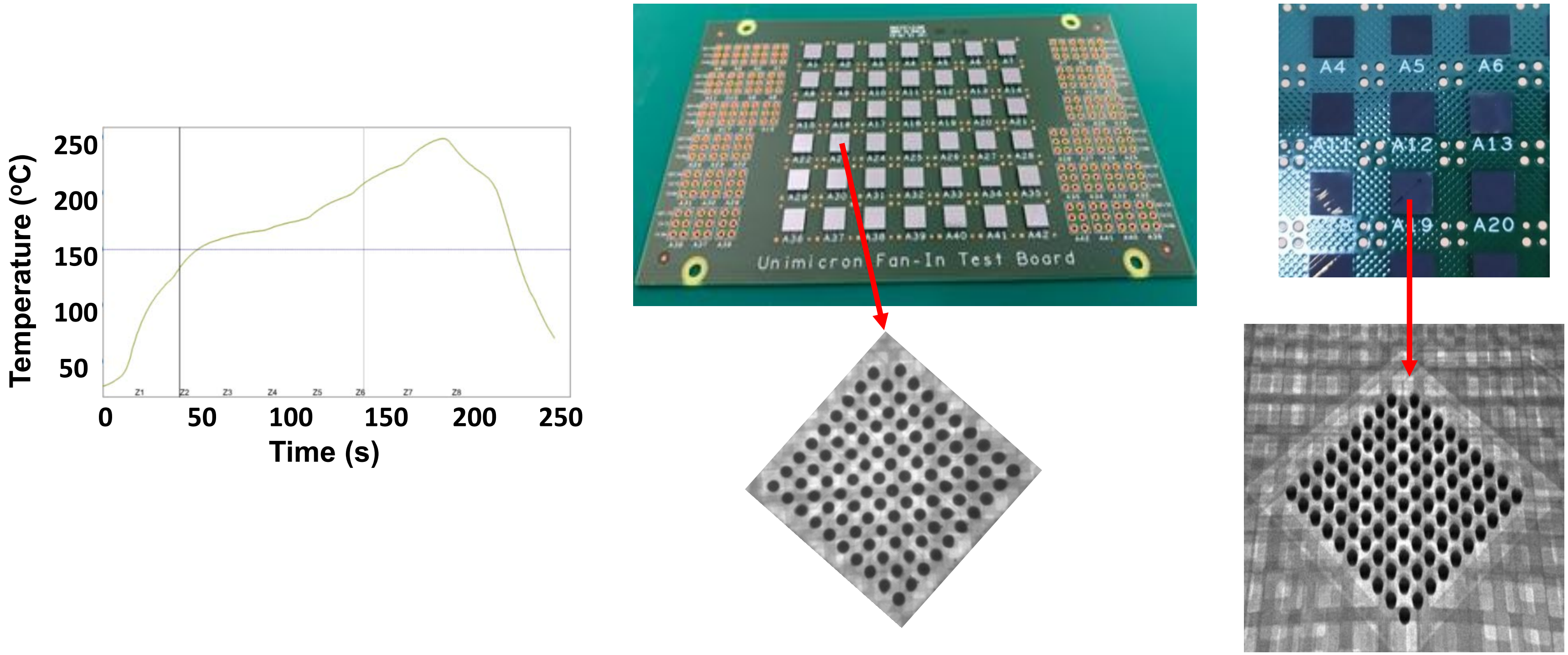
Solder ball height. (a) Ordinary PLCSP. (b) 6-side molded PLCSP. (c) Ordinary PLCSP solder ball image. (d) 6-side molded PLCSP solder ball image.





(a) Reflow profile. (b) Ordinary PLCSP. (c) 6-side molded PLCSP.

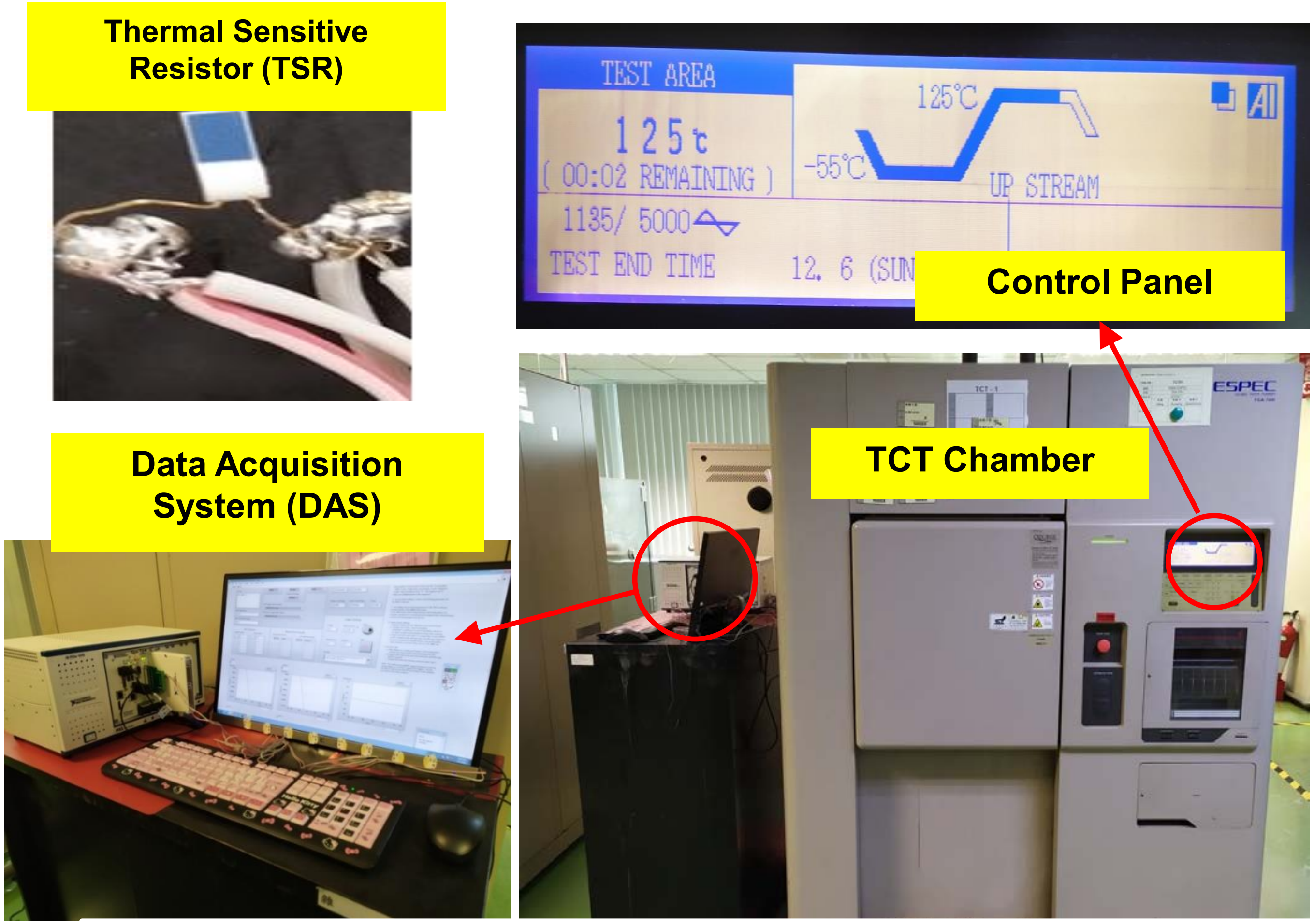
(a)



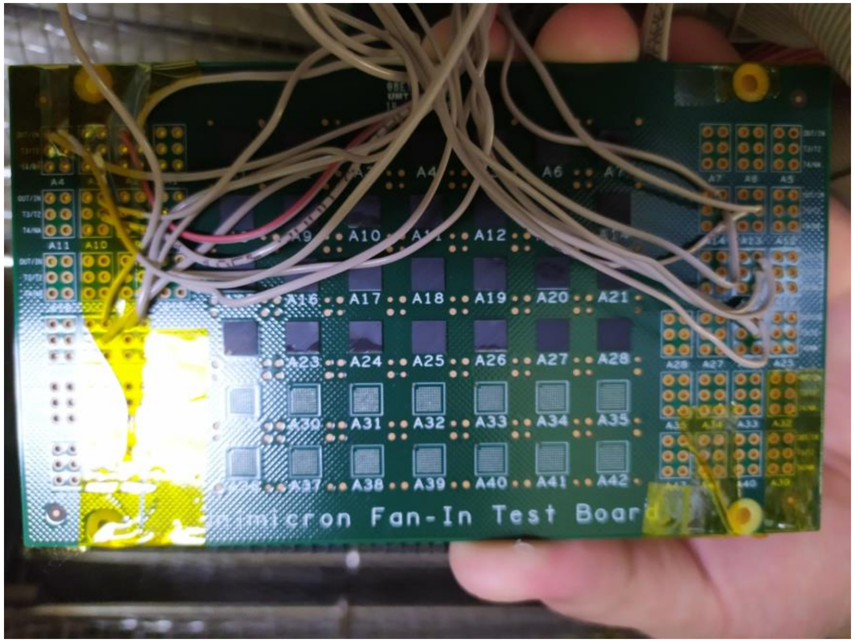
(b)

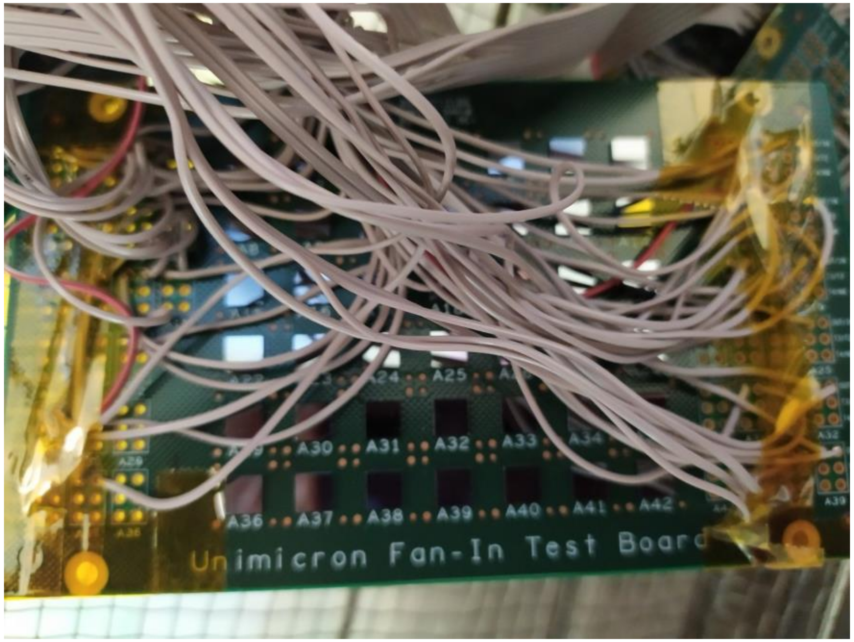
(c)

Thermal cycling chamber, thermal couple, and data acquisition system

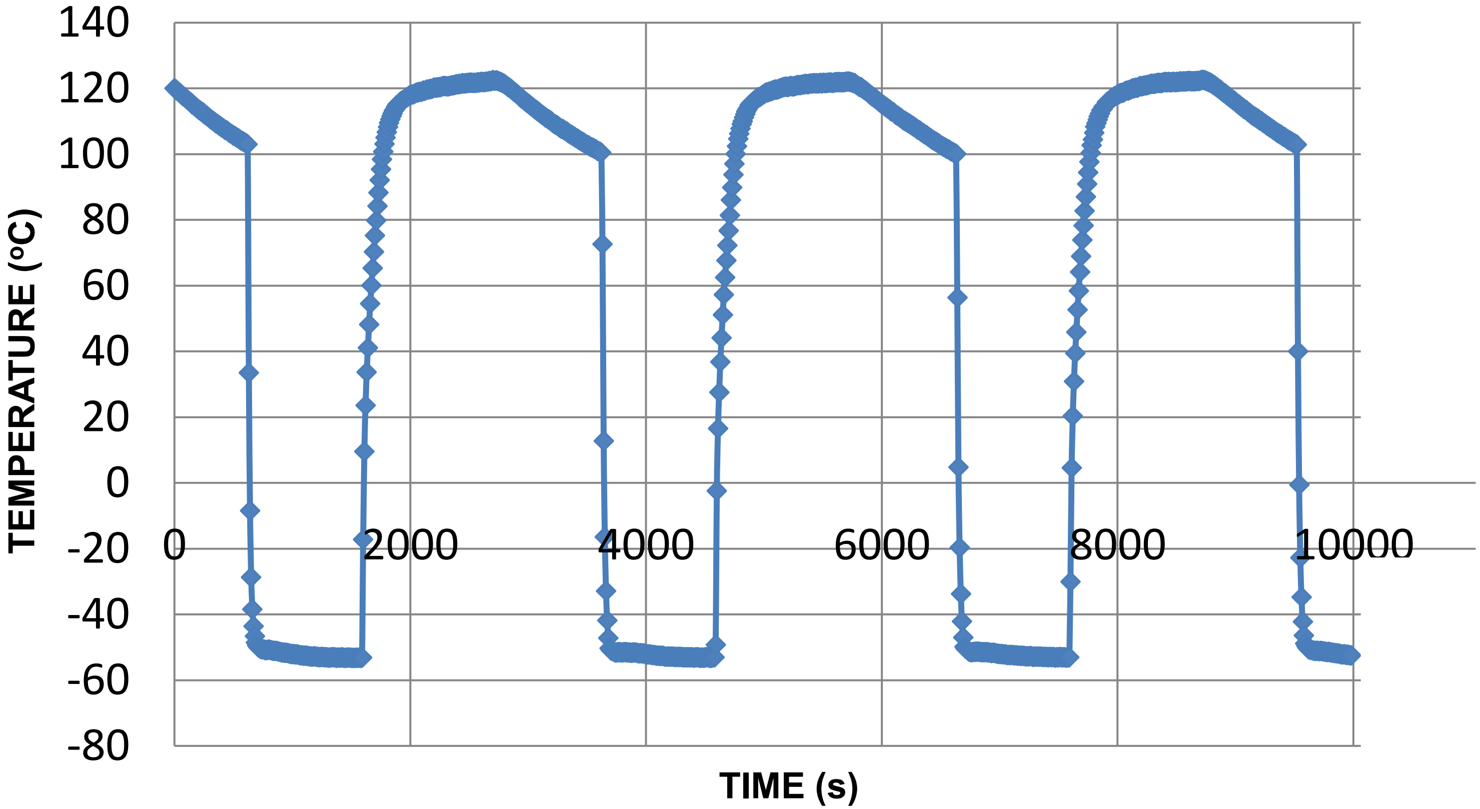


Test boards with 6-die molded PLCSPs and ordinary PLCSPs inside thermal cycling chamber





Thermal Cycling Temperature Profile

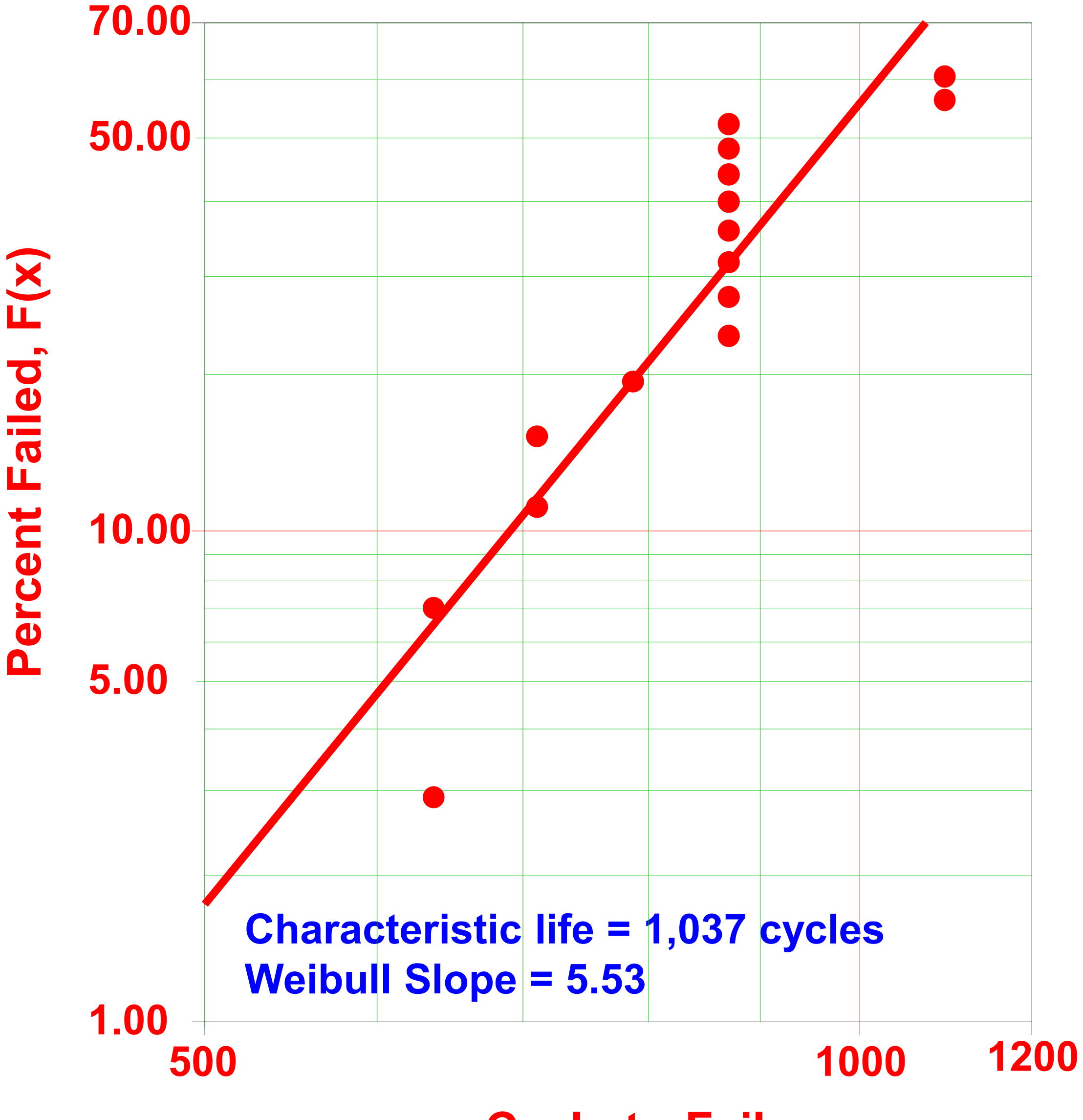


Test Results of the 6-Side Molded PLCSP at 50%, 5%, and 95% Ranks

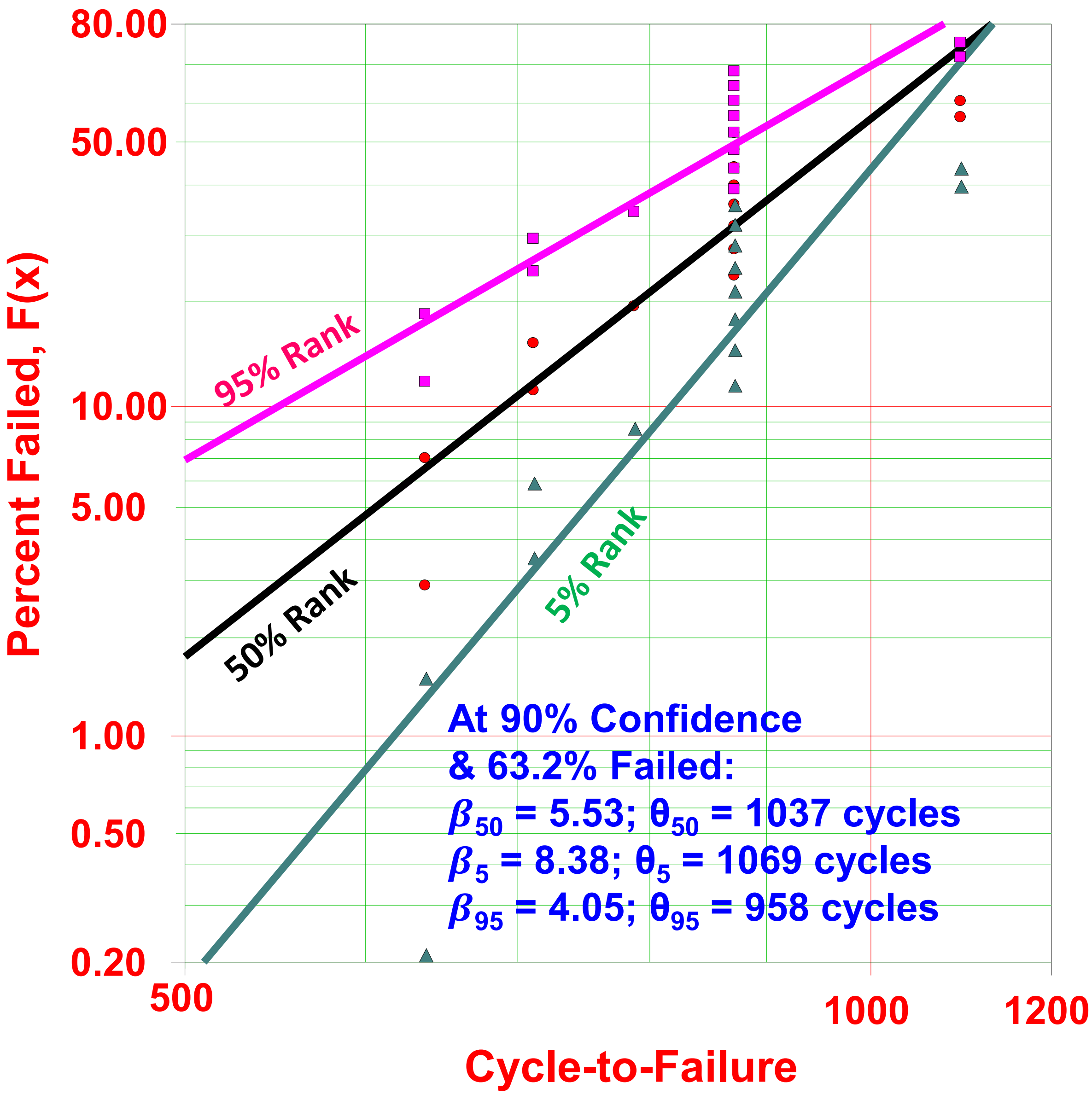
Failure Order	Cycles-to-Failure	*F(x)*		
		Median (50%) Rank	90% Confidence	
			5% Rank	95% Rank
1	638	2.88	0.21	11.73
2	638	6.98	1.50	18.29
3	712	11.08	3.50	23.98
4	712	15.17	5.90	29.23
5	788	19.27	8.59	34.18
6	872	23.37	11.49	38.91
7	872	27.46	14.57	43.47
8	872	31.56	17.80	47.87
9	872	35.66	21.26	52.14
10	872	39.75	24.64	56.29
11	872	43.85	28.24	60.32
12	872	47.95	31.94	64.24
13	872	52.04	35.76	68.06
14	1096	56.14	39.68	71.76
15	1096	60.24	43.71	75.36

Sample Size = 24 Failed = 15

Weibull plot of the 6-side molded PLCSP solder joint at median rank



Weibull plot of the 6-side molded PLCSP solder joint at 90% confidence



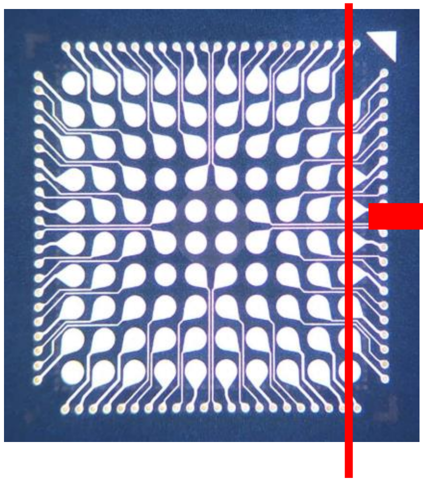
The true characteristic life (θ_t) at 90% confidence is:

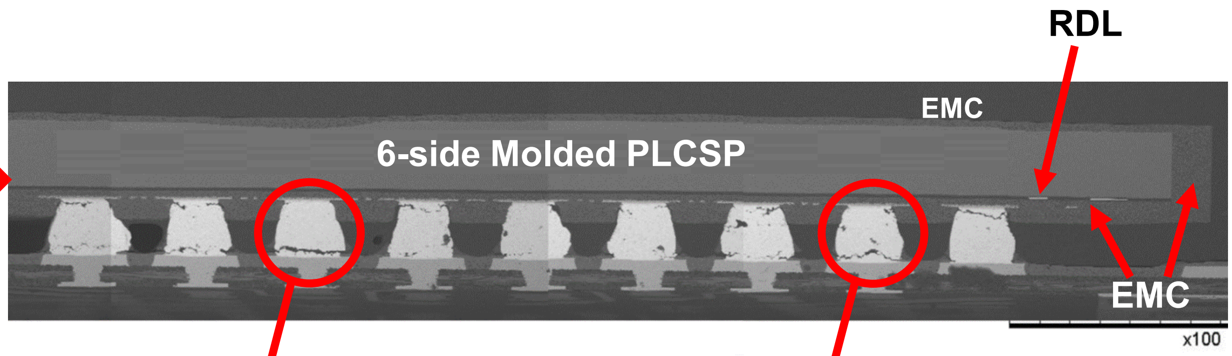
$958 \leqq \theta_t \leqq 1{,}069$ cycles.

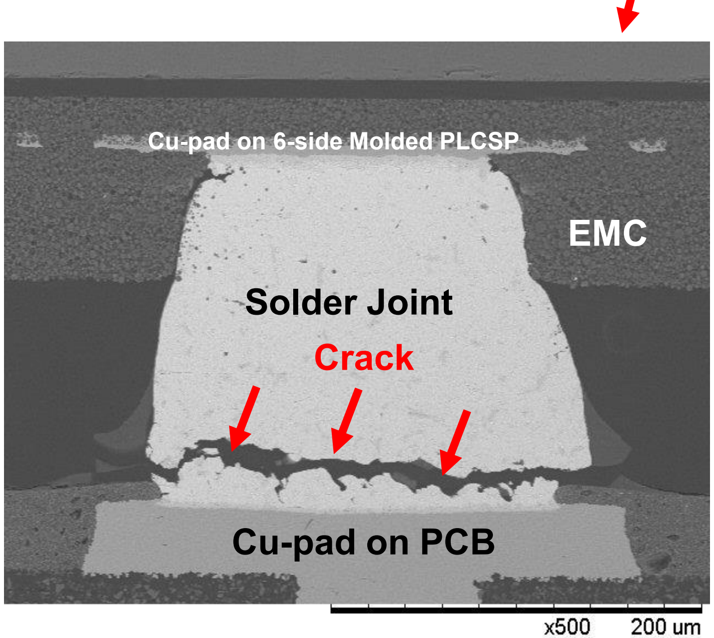
The true Weibull slope (β_t) at 90% confidence is:

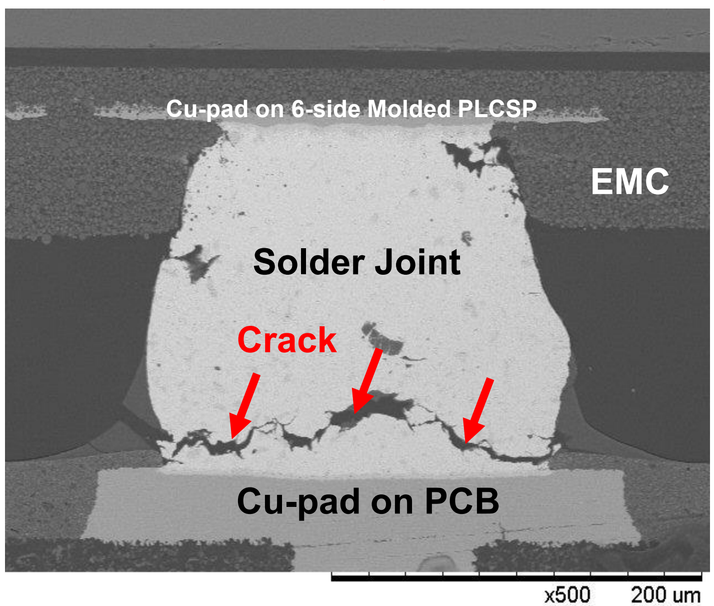
$3.93 \leqq \beta_t \leqq 7.13$.

Failure location and failure mode of the 6-side molded PLCSP solder joints







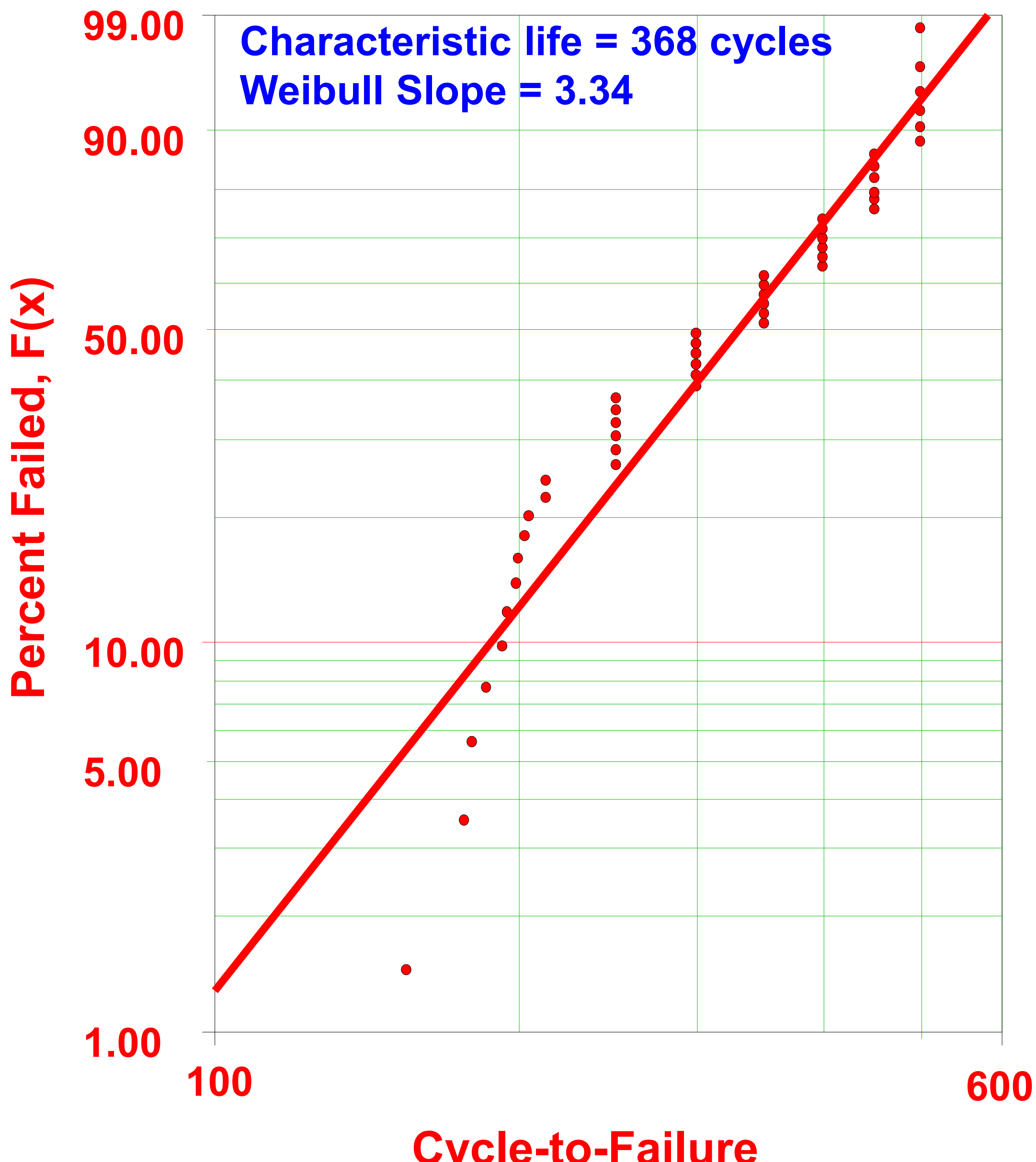


Test Results of the Ordinary PLCSP at 50%, 5%, and 95% Ranks

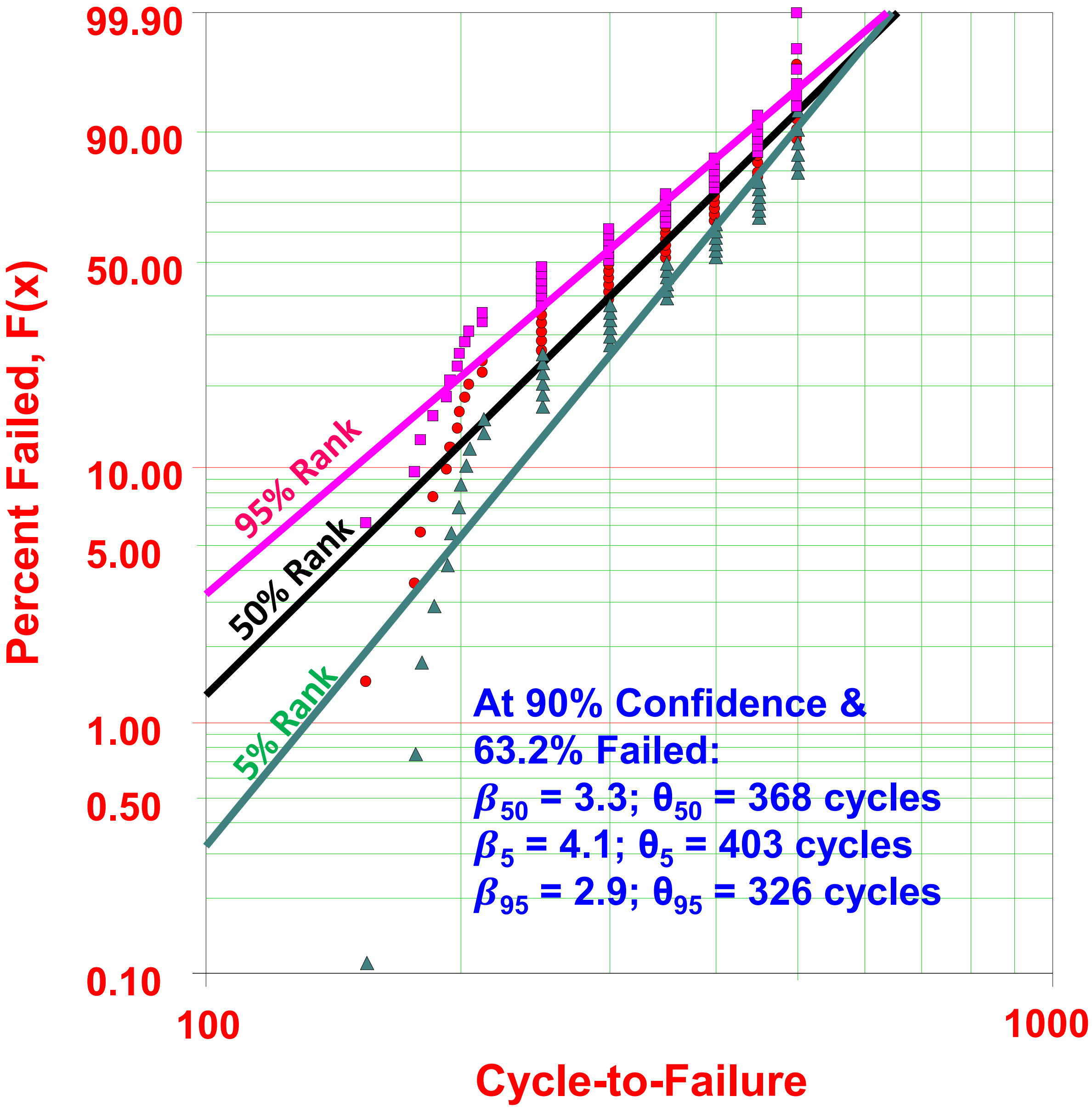
Failure Order	Cycles-to-Failure	F(x)		
		Median (50%) Rank	90% Confidence	
			5% Rank	95% Rank
1	155	1.44	0.11	6.05
2	177	3.51	0.75	9.51
3	180	5.57	1.73	12.54
4	186	7.64	2.90	15.37
5	193	9.70	4.20	18.06
6	195	11.77	5.59	20.66
7	199	13.84	7.05	23.19
8	200	15.90	8.57	25.65
9	203	17.97	10.15	28.07
10	205	20.04	11.76	30.44
11	213	22.10	13.42	32.77
12	213	24.17	15.10	35.07
13	250	26.23	16.83	37.34
14	250	28.30	18.57	39.57
15	250	30.37	20.35	41.78
16	250	32.43	22.15	43.97
17	250	34.50	23.98	46.13
18	250	36.56	25.83	48.27
19	300	38.63	27.70	50.38
20	300	40.70	29.59	52.48
21	300	42.76	31.50	54.55
22	300	44.83	33.43	56.60
23	300	46.90	35.39	58.63
24	300	48.96	37.36	60.65
25	350	51.03	39.35	62.64
26	350	53.09	41.37	64.61
27	350	55.16	43.40	66.57
28	350	57.23	45.45	68.50
29	350	59.29	47.52	70.41
30	350	61.36	49.62	72.30
31	400	63.43	51.73	74.17
32	400	65.49	53.87	76.02
33	400	67.56	56.03	77.85
34	400	69.62	58.22	79.65
35	400	71.69	60.43	81.43
36	400	73.76	62.66	83.17
37	450	75.82	64.93	84.90
38	450	77.89	67.23	86.58
39	450	79.16	69.56	88.24
40	450	82.02	71.93	89.85
41	450	84.09	74.35	91.43
42	450	86.15	76.81	92.95
43	500	88.22	79.4	94.41
44	500	90.29	81.94	95.80
45	500	92.35	84.63	97.10
46	500	94.42	87.46	98.27
47	500	96.48	90.49	99.25
48	500	98.55	93.95	99.89

Sample Size = 48 Failed = 48

Weibull plot of the ordinary PLCSP solder joint at median rank



Weibull plot of the ordinary PLCSP solder joint at 90% confidence



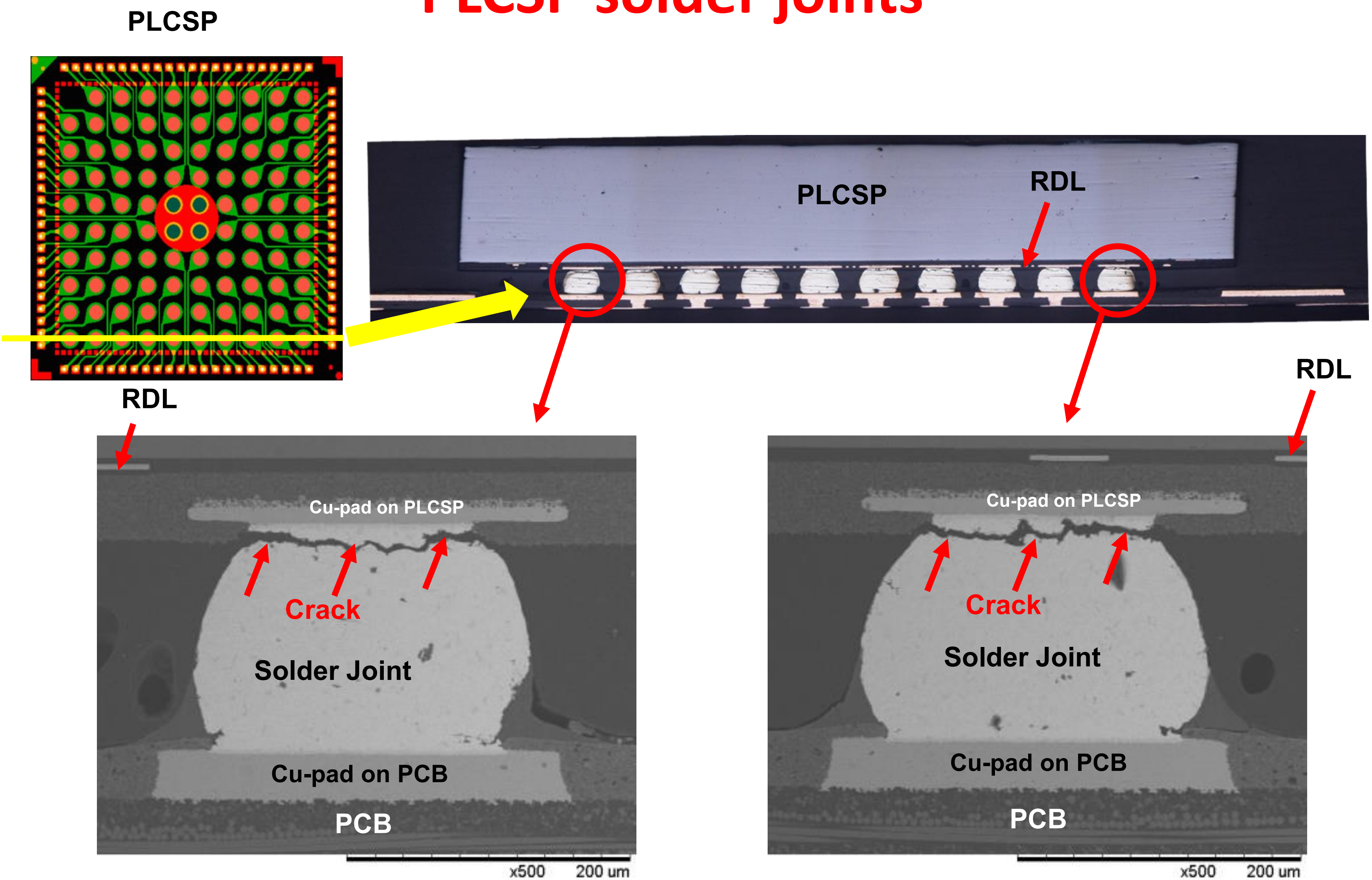
The true characteristic life (θ_t) at 90% confidence is:

$326 \leqq \theta_t \leqq 403$ cycles.

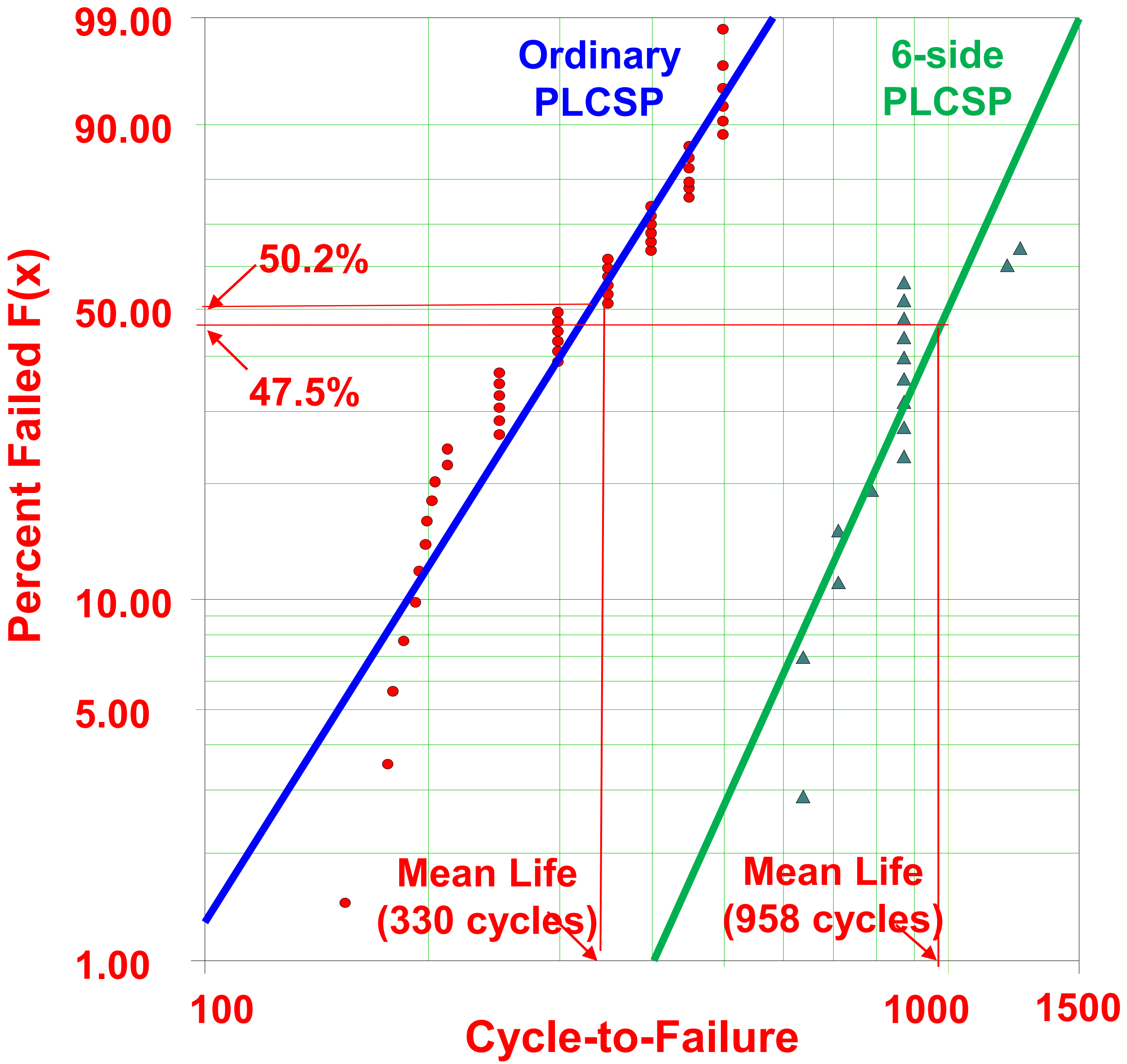
The true Weibull slope (β_t) at 90% confidence is:

$2.6 \leqq \beta_t \leqq 4.1$.

Failure location and failure mode of the ordinary PLCSP solder joints

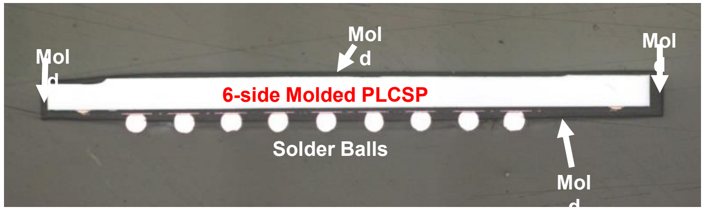


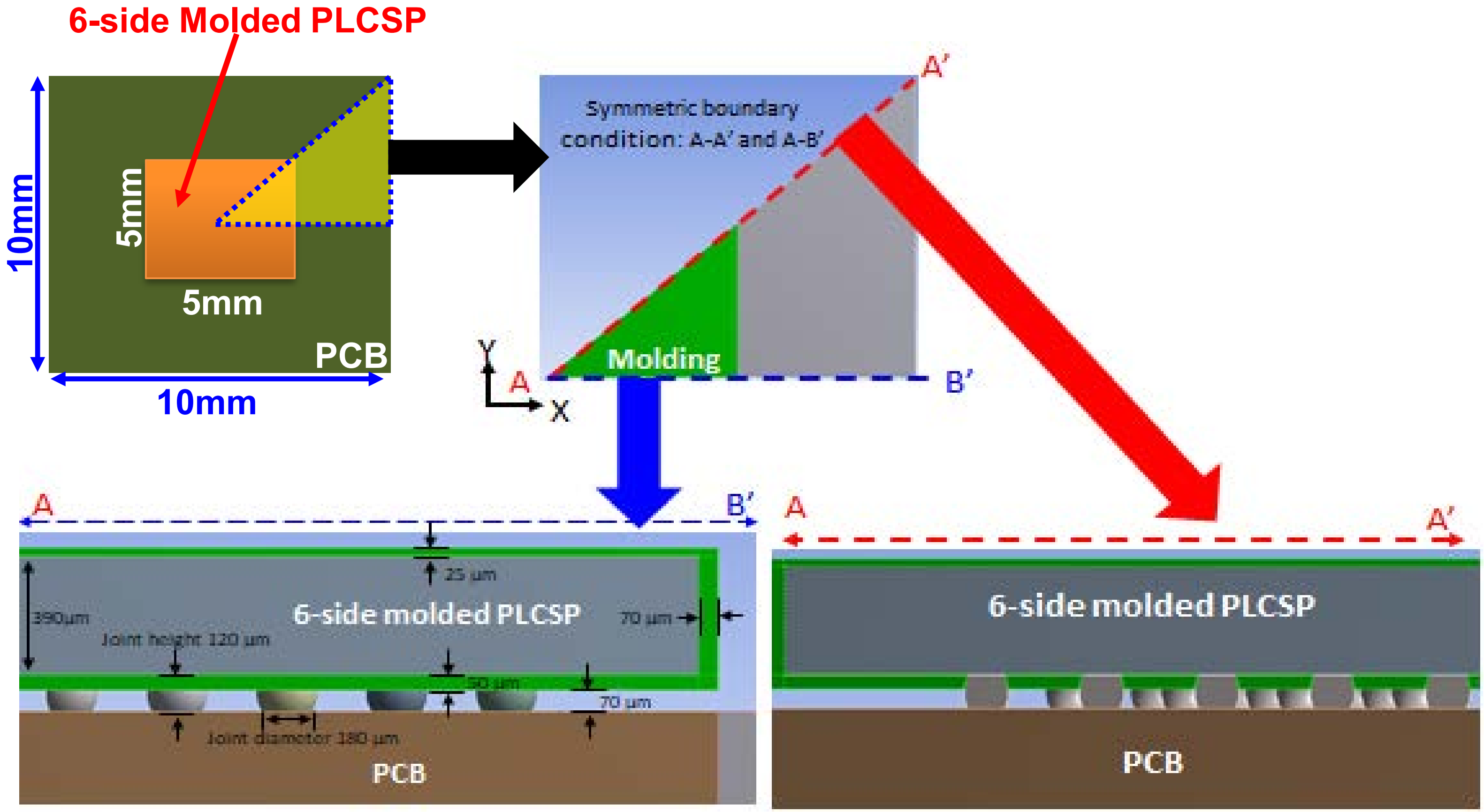
Comparison between the 6-side Molded PLCSP and the Ordinary PLCSP solder joints



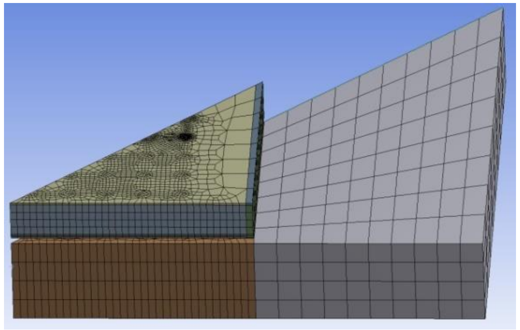
In 999 out of one thousand cases the mean life of the 6-side molded PLCSP solder joint is superior (by 2.9 times) to the ordinary PLCSP.

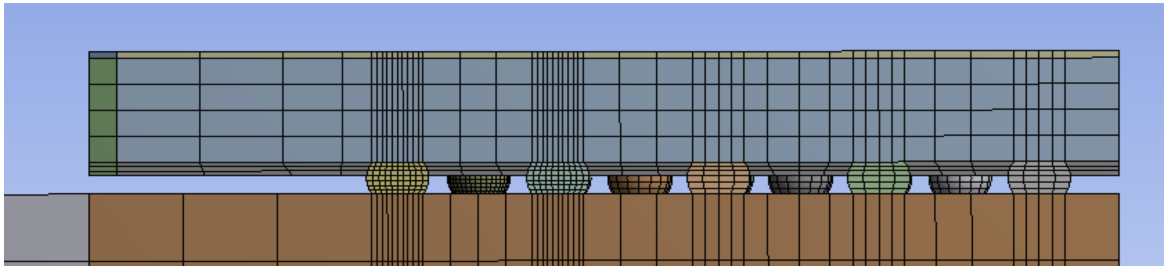
Geometry and Boundary-Value Problem

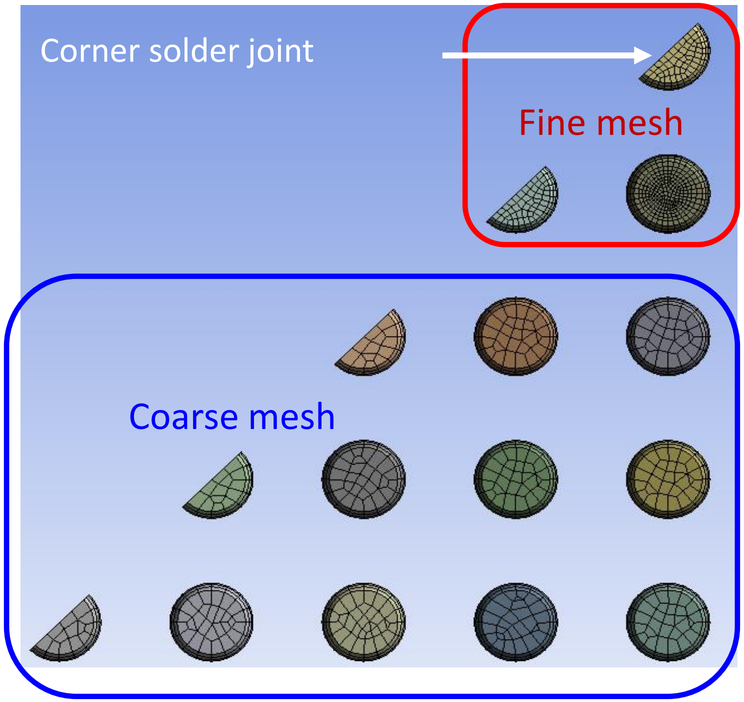


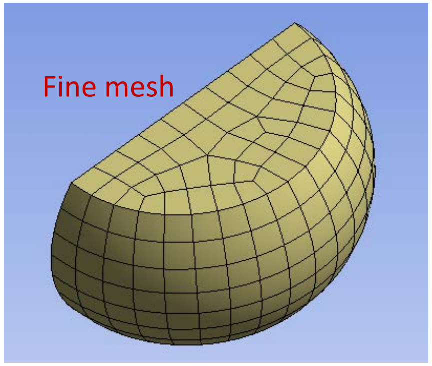


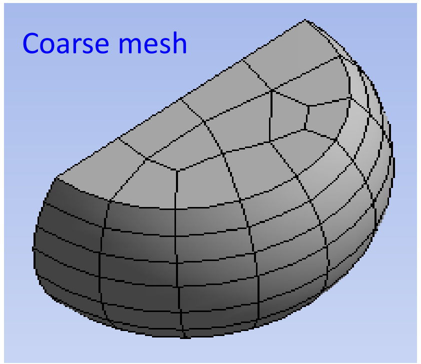
Finite Element Model for Simulations

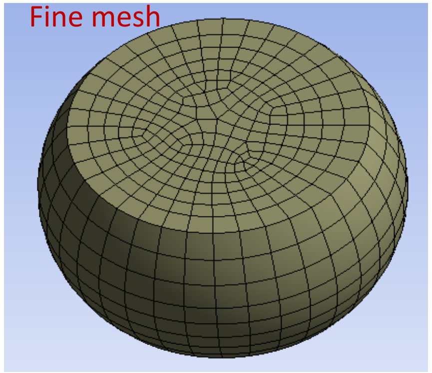


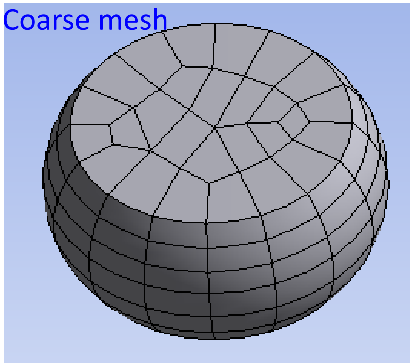










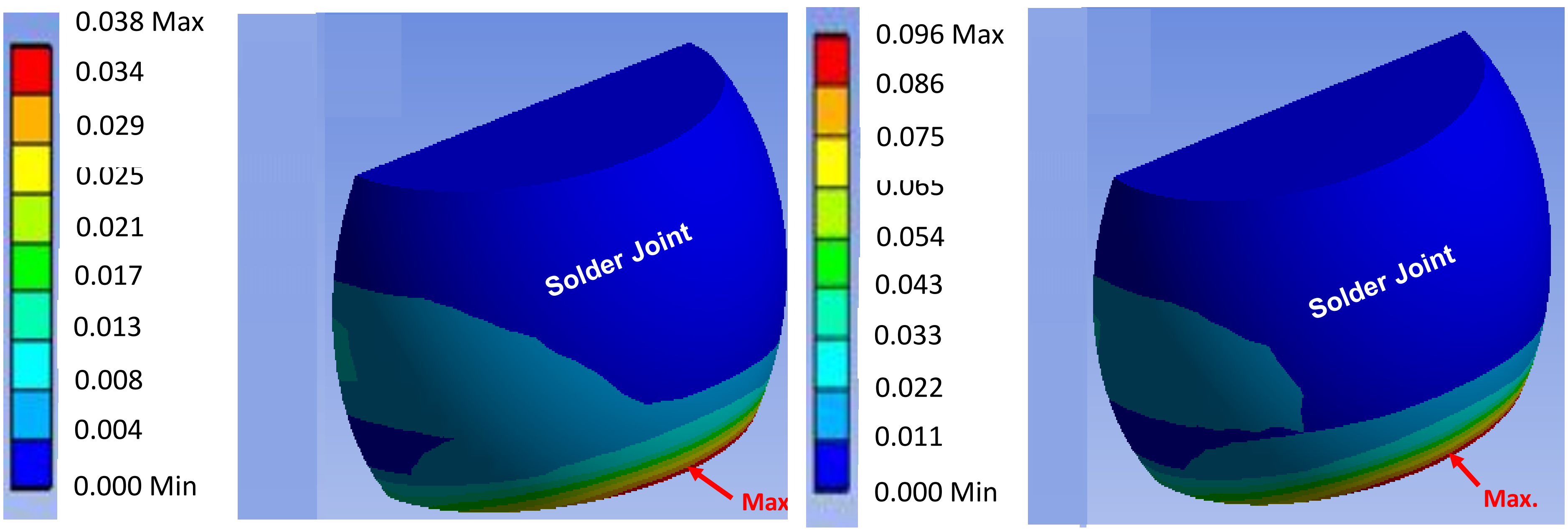


Materials Property

Materials	CTE ($10^{-6}/^{o}C$)	Young's Modulus (GPa)	Poisson's Ratio
Copper	16.3	121	0.34
PCB	$\alpha_x = \alpha_y = 18$ $\alpha_z = 70$	$E_x = E_y = 22$ $E_z = 10$	0.28
Silicon	2.8	131	0.278
Solder	21 + 0.017T	49 - 0.07T	0.3
ABF	7.0	7.0	0.3

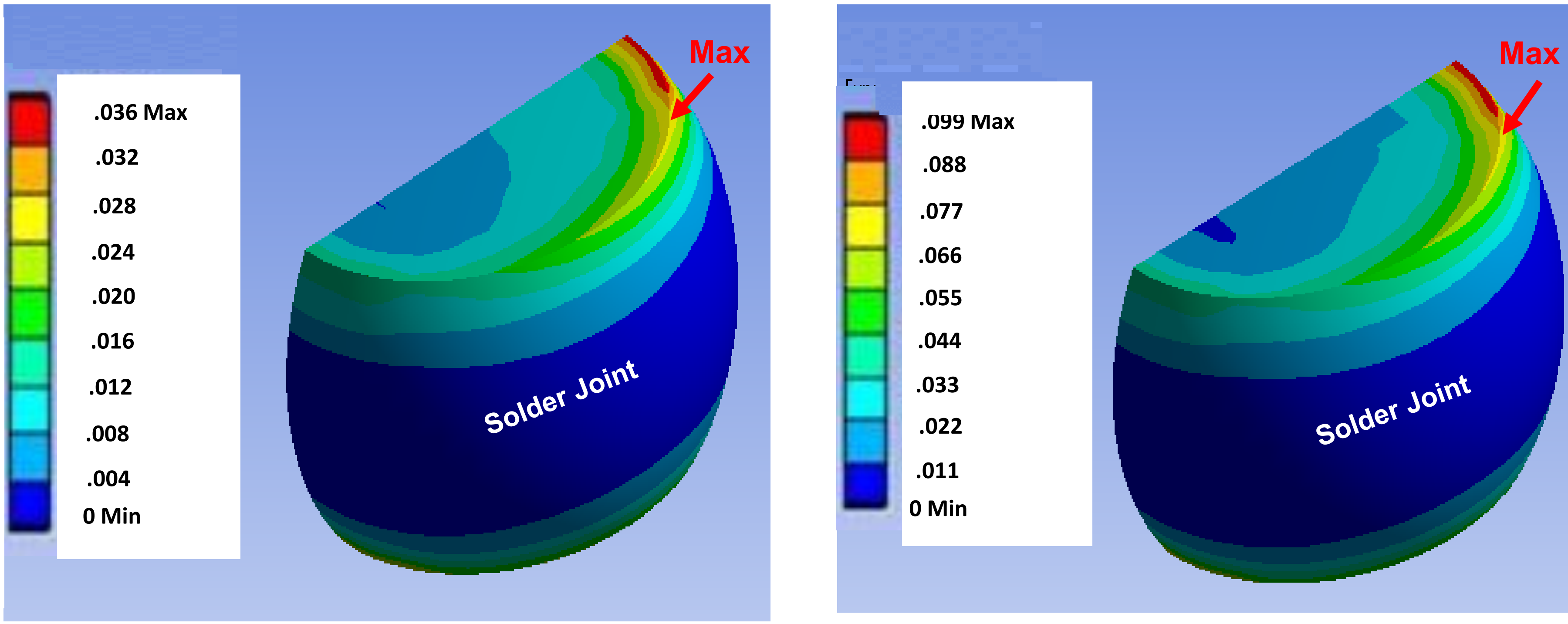
T is in Celsius

Accumulated creep strain at the corner solder joint of the 6-side molded PLCSP PCB assembly. (a) At 85°C (450s). (b) At -40°C (2,250s).



(a) (b)

Accumulated creep strain at the corner solder joint of the ordinary PLCSP. PCB assembly. (a) At 85°C (450s). (b) At -40°C (2,250s).



(a) (b)

SUMMARY

- PCB assemblies of the 6-side molded PLCSP and the ordinary PLCSP have been subjected to thermal cycling test (-55°C ⇆ 125°C, 50-minute cycle). The sample size of the 6-side molded PLCSP is 24 and that of ordinary PLCSP is 48. The test stopped at 1,300 cycles. There were 15 failures of the 6-side molded PLCSP samples and 48 failures of the ordinary PLCSP samples.
- The failure criterion is when the resistance of the daisy chain of the PLCSP PCB assembly increases by 50%.
- For median rank, the Weibull slope and the characteristic life of the 6-side molded PLCSP solder joints are, respectively 5.53 and 1,037 cycles. For 90% confidence, the true Weibull slope is $3.93 \leqq \beta_t \leqq 7.13$ and the true characteristic life is $958 \leqq \theta_t \leqq 1{,}069$ cycles.
- The failure location of the 6-side molded PLCSP is along the outer row (near the corner) of solder joints. The failure mode is the cracking of solder near the interface between the PCB and the bulk solders.
- For median rank, the Weibull slope and the characteristic life of the ordinary PLCSP solder joints are, respectively 3.34 and 368 cycles. For 90% confidence, the true Weibull slope is $2.6 \leqq \beta_t \leqq 4.1$ and the true characteristic life is $326 \leqq \theta_t \leqq 403$ cycles.
- The failure location of the ordinary PLCSP is along the outer row (near the corner) of solder joints. The failure mode is the cracking of solder near the interface between the chip and the bulk solders.

SUMMARY

- **By comparing the mean life between the 6-side molded PLCSP solder joint (958 cycles) with the ordinary PLCSP solder joints (330), it has been determined that in 999 out of one thousand cases, the mean life of the 6-side molded PLCSP is 2.9 times of the ordinary PLCSP.**
- **A non-linear time and temperature dependent 3D finite element simulation of the 6-side molded PLCSP PCB assembly showed that the maximum accumulated creep strain occurs near the interface between the PCB and the bulk solders. Thus, any failure should occur (initially) at this location. This confirms with the failure mode from the thermal cycling test results.**
- **The simulation of the ordinary PLCSP PCB assembly showed that the maximum accumulated creep strain occurs near the interface between the chip and the bulk solders. Thus, any failure should occur (initially) at this location. This confirms with the failure mode from the thermal cycling test results.**
- **The reason for the switch of the failure mode from the interface between the PCB and the bulk solders (for the 6-side molded PLCSP) to the interface between the chip and the bulk solders (ordinary) is because there is protection of the upper solder joint from the EMC molding.**
- **The maximum values of the accumulated creep strain in the corner solder joint for the 6-side molded PLCSP and the ordinary PLCSP are about the same. However, this maximum values only occurred at a very small volume of the 6-side molded PLCSP solder joint. The accumulated creep strain in most of the volumes of the 6-side molded solder joint is smaller than those in the ordinary PLCSP solder joins. Thus, the thermal-fatigue life of the 6-side molded PLCSP should be longer than that of the ordinary PLCSP.**

Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration

John H Lau, Gary Chang-Fu Chen, Jones Yu-Cheng Huang, Ricky Tsun-Sheng Chou, Channing Cheng-Lin Yang, Hsing-Ning Liu, and Tzvy-Jang Tseng

Unimicron Technology Corporation

Lau, J. H., G. Chen, J. Huang, R. Chou, C. Yang, N. Liu, and T. Tseng, "Hybrid Substrate by Fan-Out RDL-First Panel-Level Packaging, *IEEE Transactions on CPMT*, Vol. 11, No. 8, August 2021, pp. 1301-1309.

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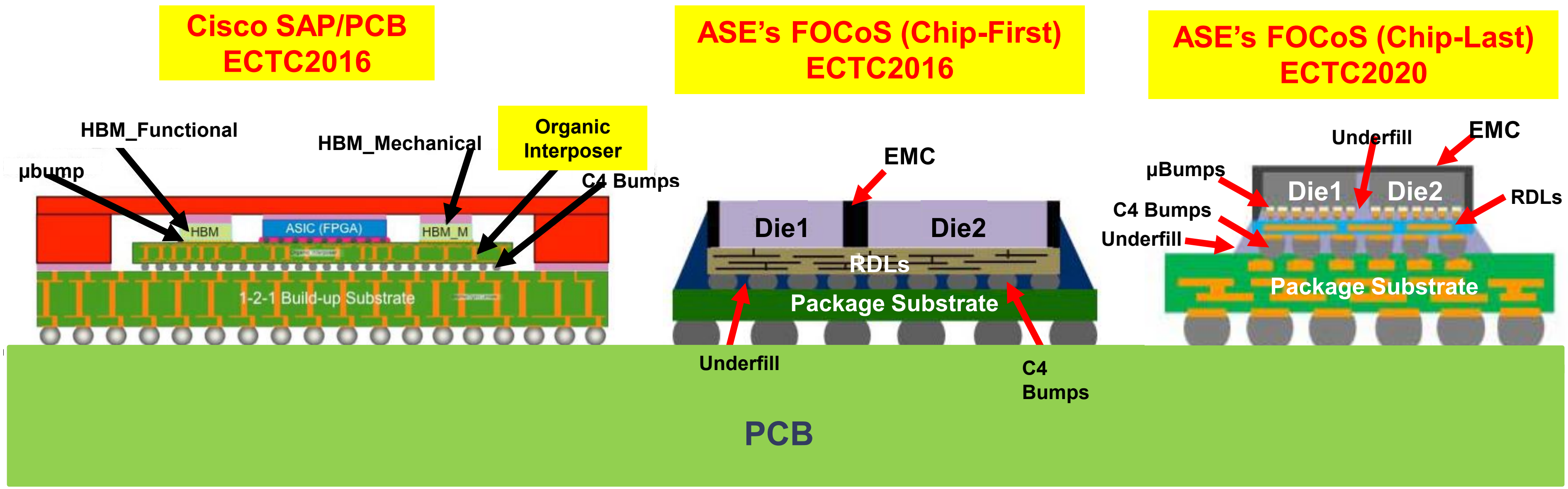
- INTRODUCTION
- TEST CHIPS
- HETEROGENEOUS INTEGRATION TEST PACKAGE
- HYBRID SUBSTRATE FABRICATION
- FINAL PACKAGE ASSEMBLY
- THERMAL CYCLING SIMULATION
- SUMMARY

INTRODUCTION

The 2.3D IC integration is defined as fabricating a coreless organic interposer (substrate) on top of a build-up package substrate.

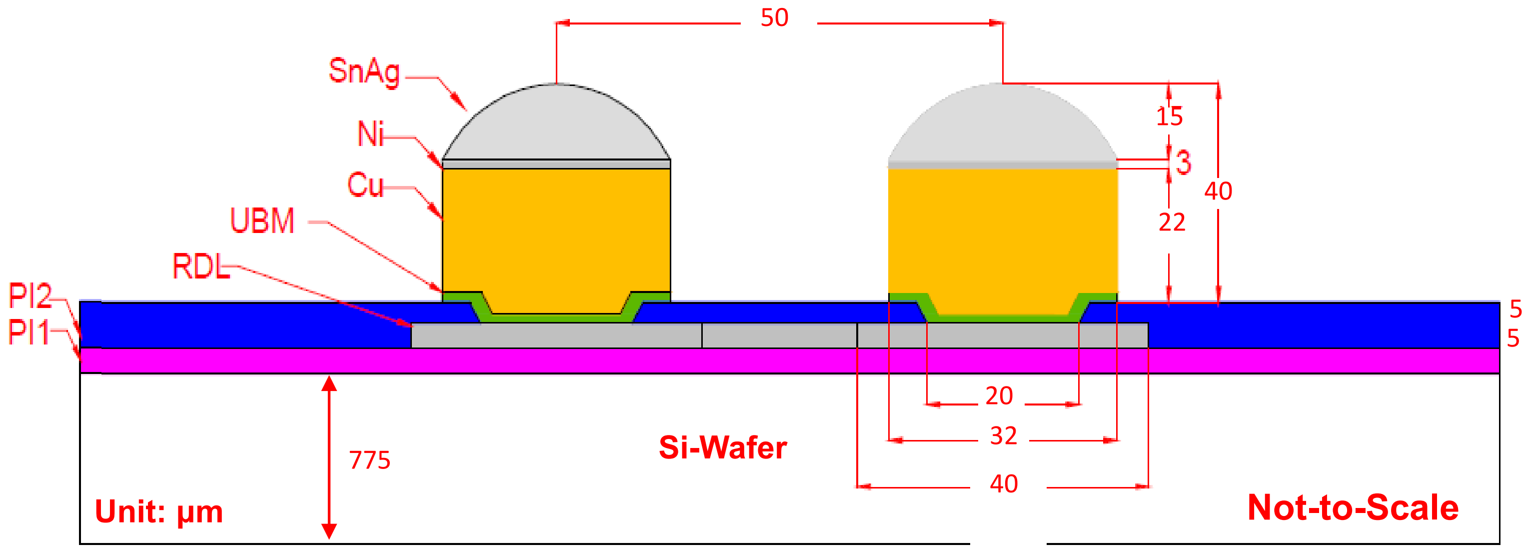


INTRODUCTION

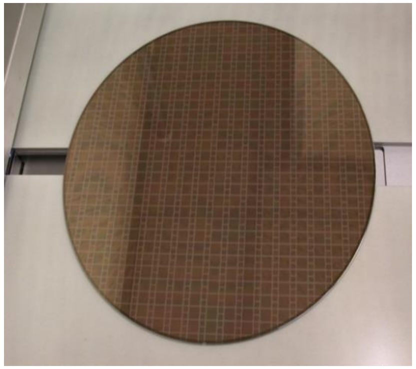
	Chip-First (Face-Down), e.g., eWLB	Chip-First (Face-Up), e.g., In_FO	Chip-Last (RDL-First), e.g., SiWLP
Chip Size	≦ 5 x 5mm[1]	≦ 12 x 12mm[1]	≦ 20 x 20mm
Package Size	≦ 10 x 10mm[2]	≦ 25 x 25mm[2]	≦ 40 x 40mm
RDL (Metal L/S)	≦ 10µm	≦ 5µm	≧ 2µm or < 1µm[3]
RDL (Layers)	≦ 3	≦ 4	≦ 6
Wafer bumping	No	No	Yes
Chip-to-substrate bonding	No	No	Yes
Underfill or MUF	No	No	Yes
Process steps	Simple	Slightly more	More
Cost	Low	Middle	High
Performance	Low	Middle	High
Applications	Baseband, MCU, RF/analog, PMIC, etc.	Apple's Application processors	High-performance and high-density (Not in HVM)

[1]Limited by die shift; [2]Limited by warpage; [3]With PECVD, Cu damascene + CMP

Test chips: 10mm x 10mm and 5mm x 5mm with 50µm-pitch.

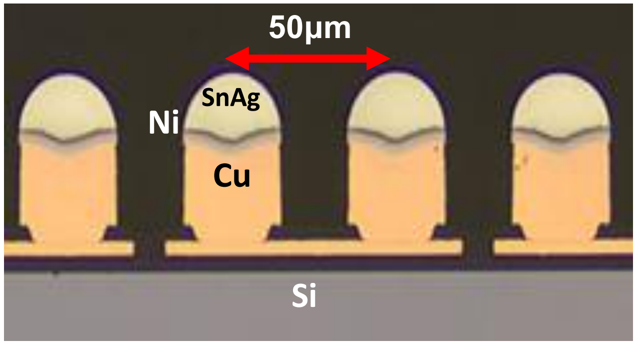


300mm wafer

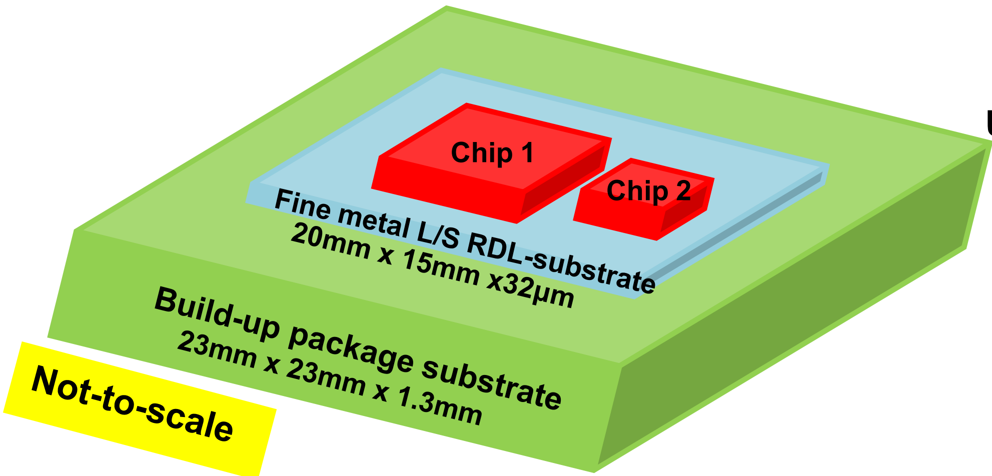


400 @ 10mm x 10mm chips
804 @ 5mm x 5mm chips

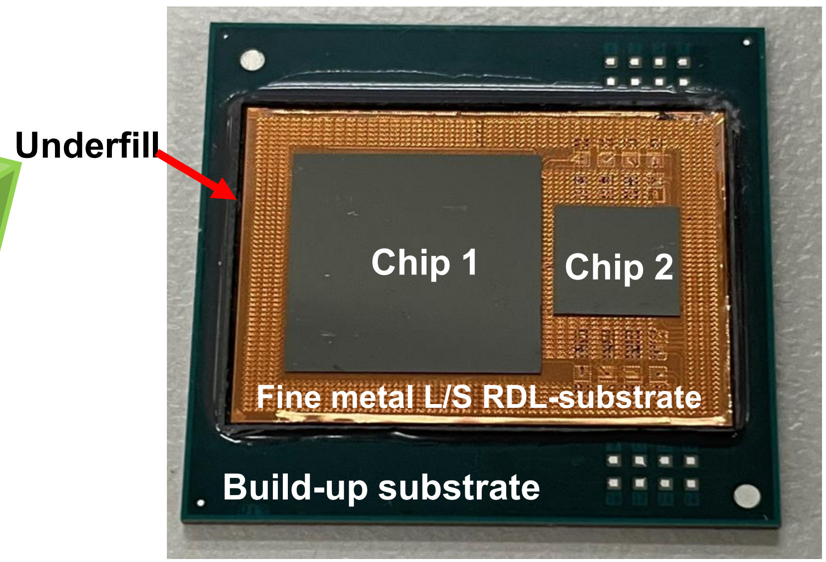
10mm x 10mm chip



(a) Schematic of the test package. (b) Assembled test package. Chips are bonded on the hybrid substrate which consists of the (20mm x 15mm) fine metal L/S RDL- substrate and (23mm x 23mm) build-up substrate.

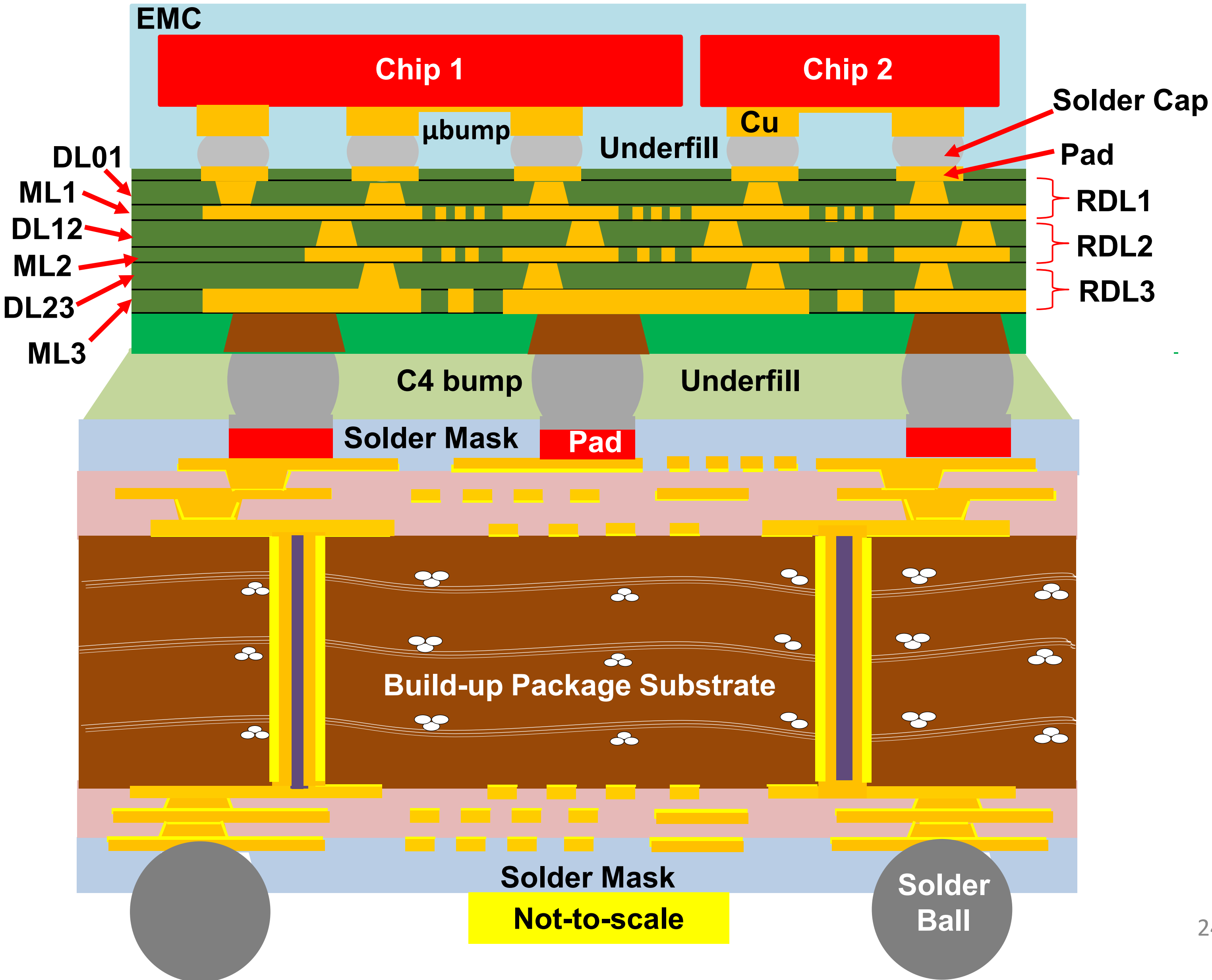


(a)

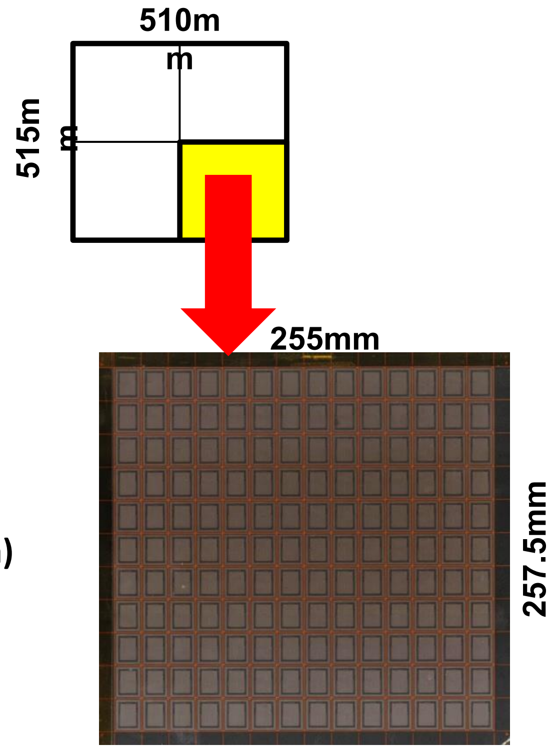


(b)

Schematic of the cross section of the heterogeneous integration test package

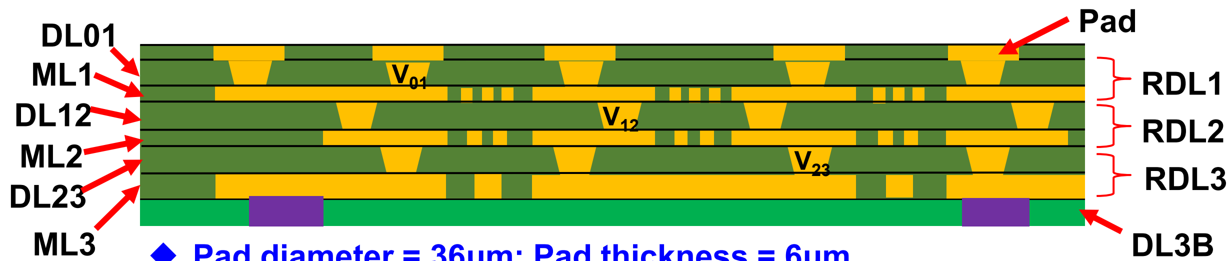


(a) Panel for fabricating the RDL-substrate and the assembled one. (b) Fine metal L/S RDL-substrate.



(a)

154 @ 20mm x 15mm RDL-substrates

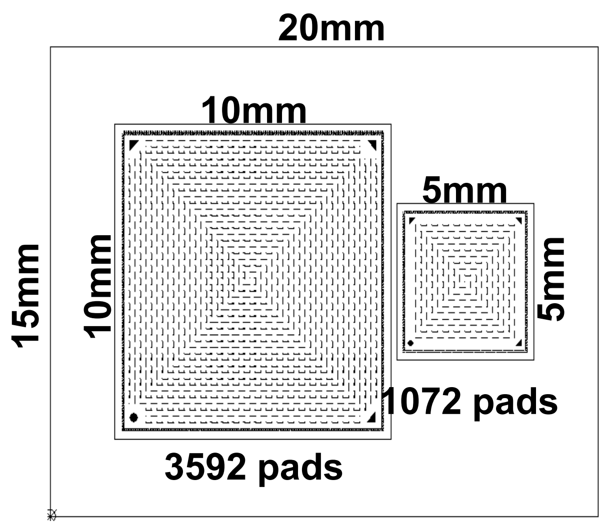


- Pad diameter = 36µm; Pad thickness = 6µm
- Via opening: V_{01} = 10µm; V_{12} = 20µm; V_{23} = 18µm
- Dielectric thickness: DL01 = 3µm; DL12 = 6µm; DL23 = 4µm
- Metal thickness: ML1 = 3µm; ML2 = 5µm; ML3 = 5µm
- L/S: ML1 = 2/2µm; ML2 = 5/5µm; ML3 = 10/10µm and ball pad = 105µm
- Solder Mask opening = 80µm; Thickness (DL3B) = 2µm

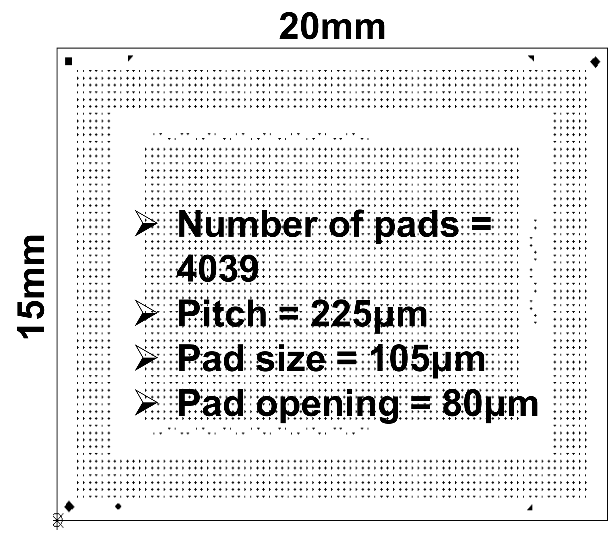
(b)

(a) Schematic of the top-view of RDL-substrate. (b) Top-view of the fabricated RDL-substrate. (c) Schematic of the bottom-view of RDL-substrate. (d) Bottom-view of the fabricated RDL-substrate.

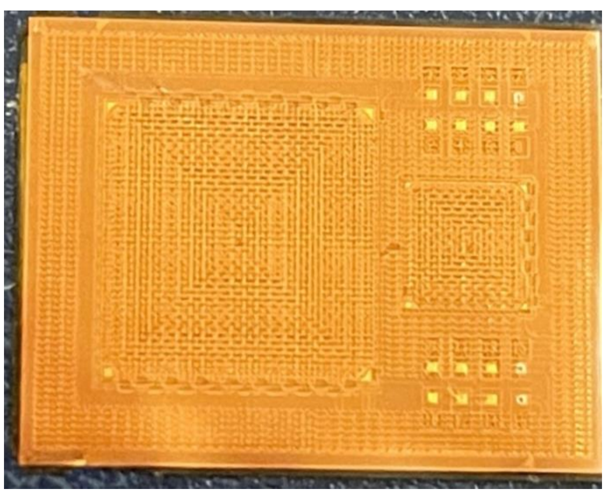
(a)



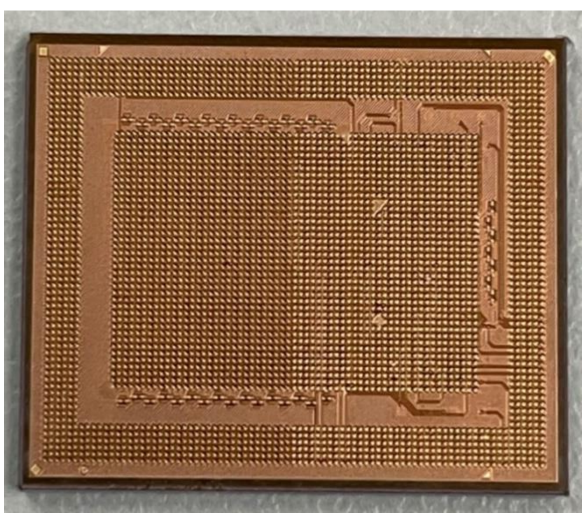
(c)



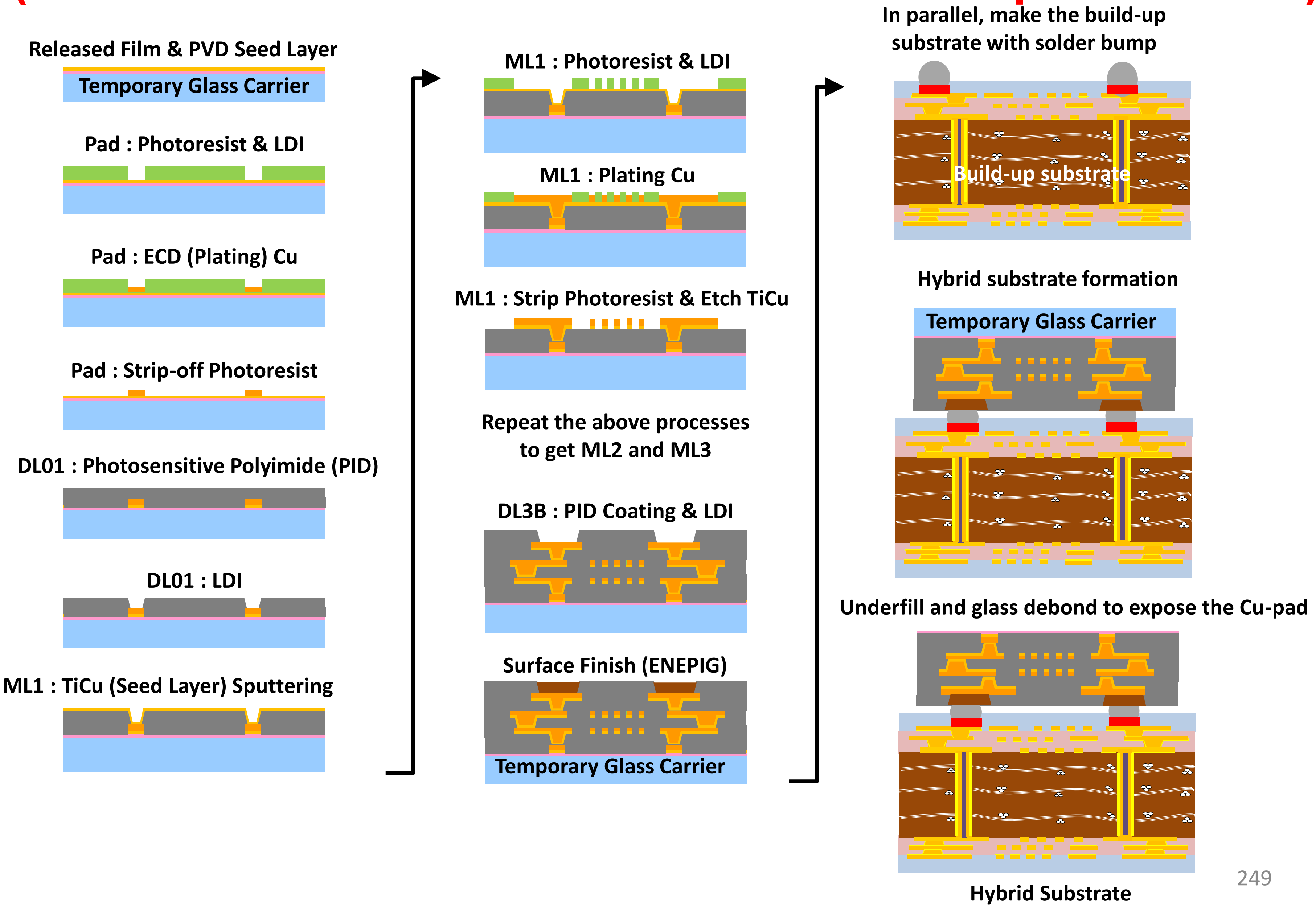
(b)



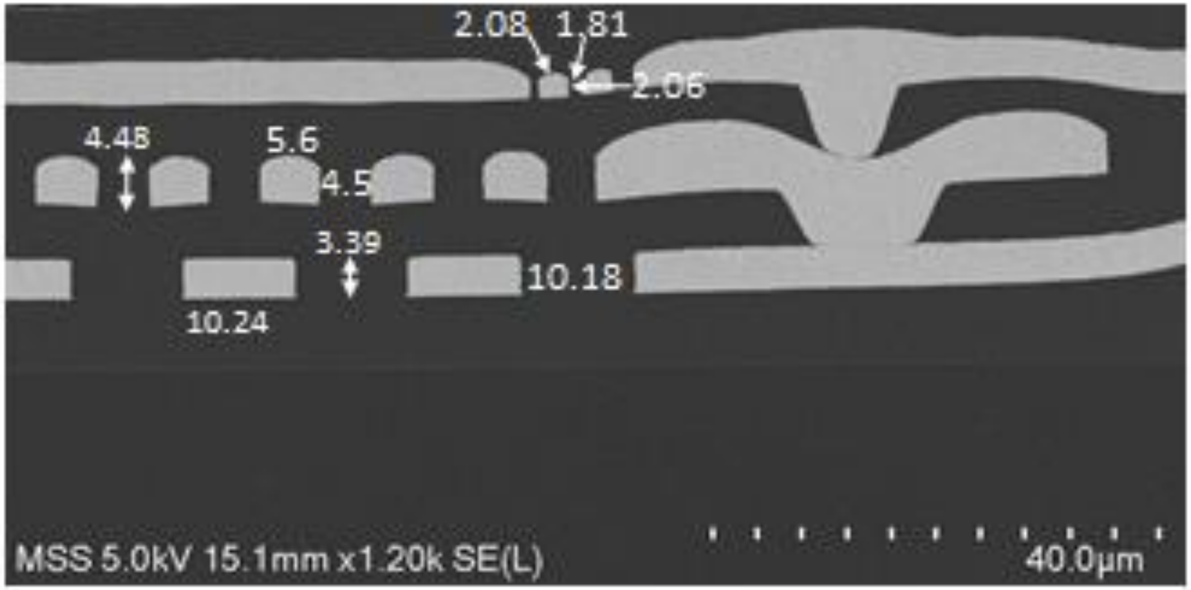
(d)

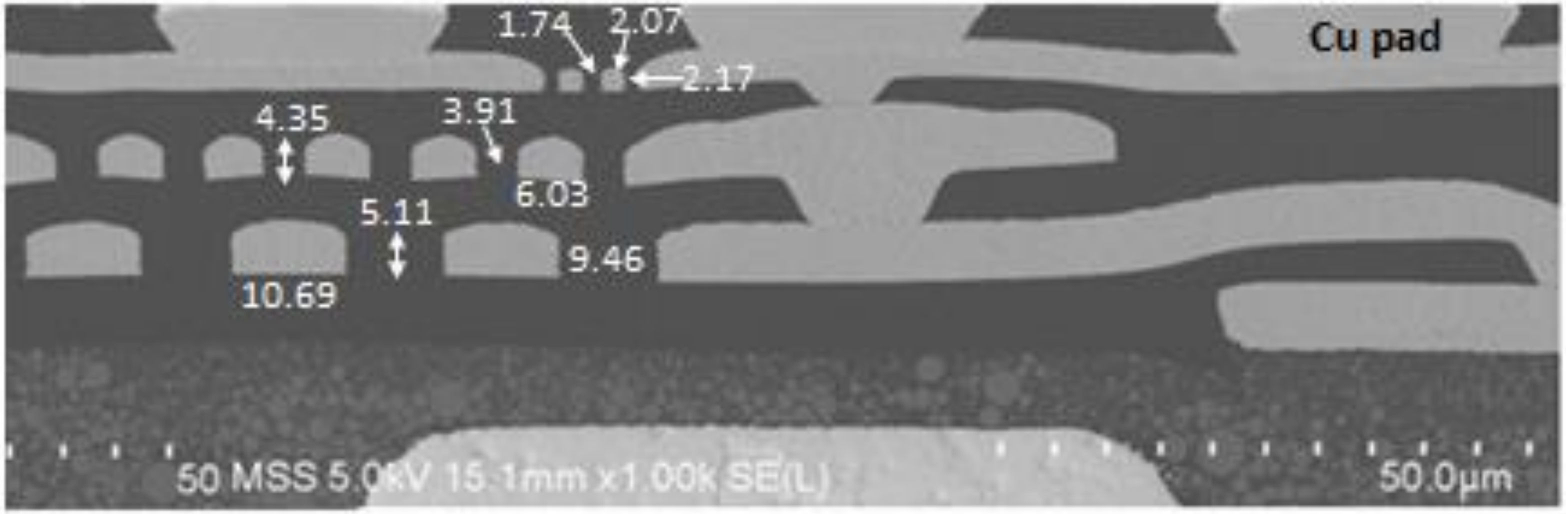


Key process steps to fabricate the hybrid substrate (fine metal L/S RDL-substrate + build-up substrate)

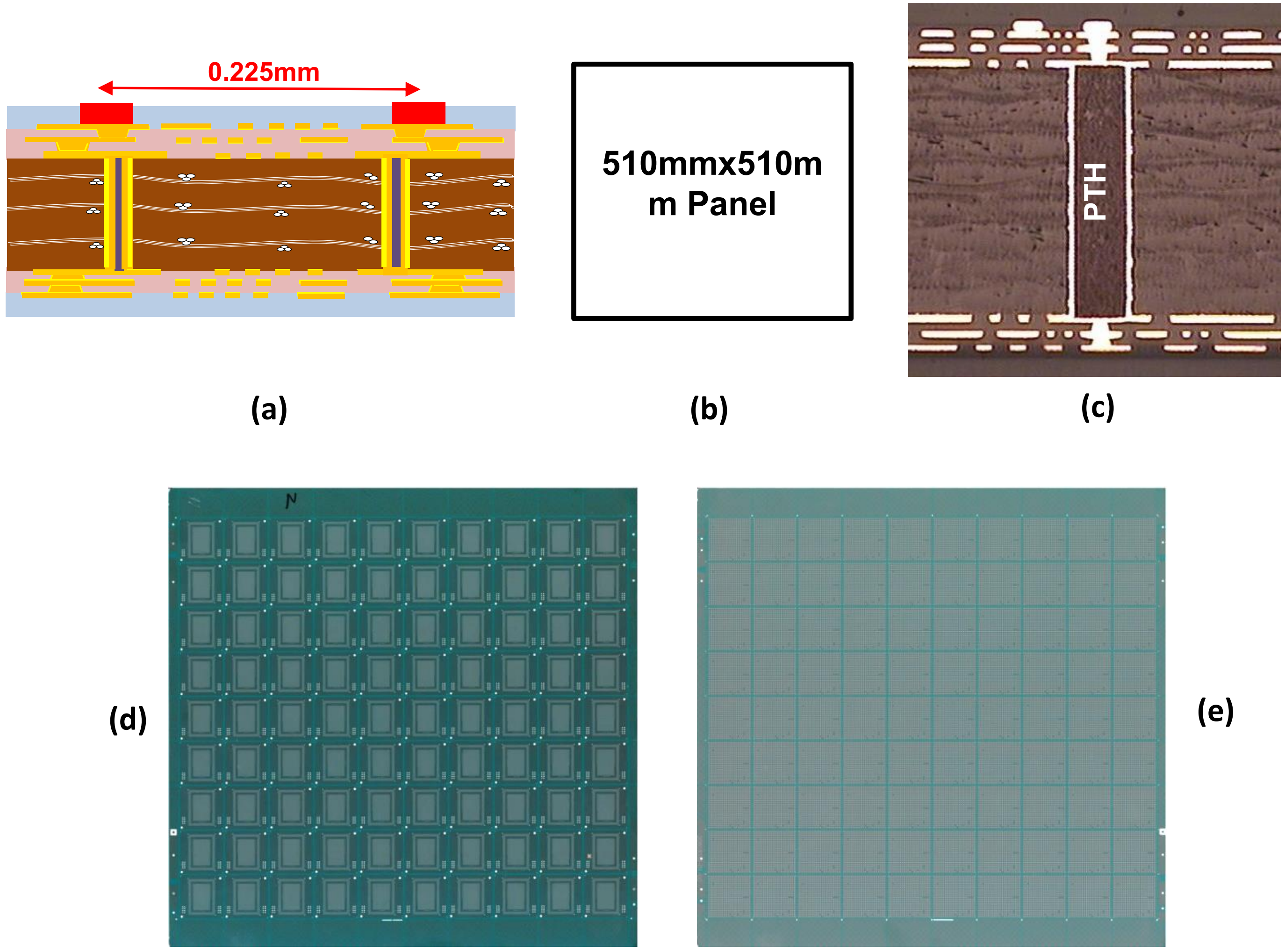


Cross sections of SEM image of RDL-substrate.

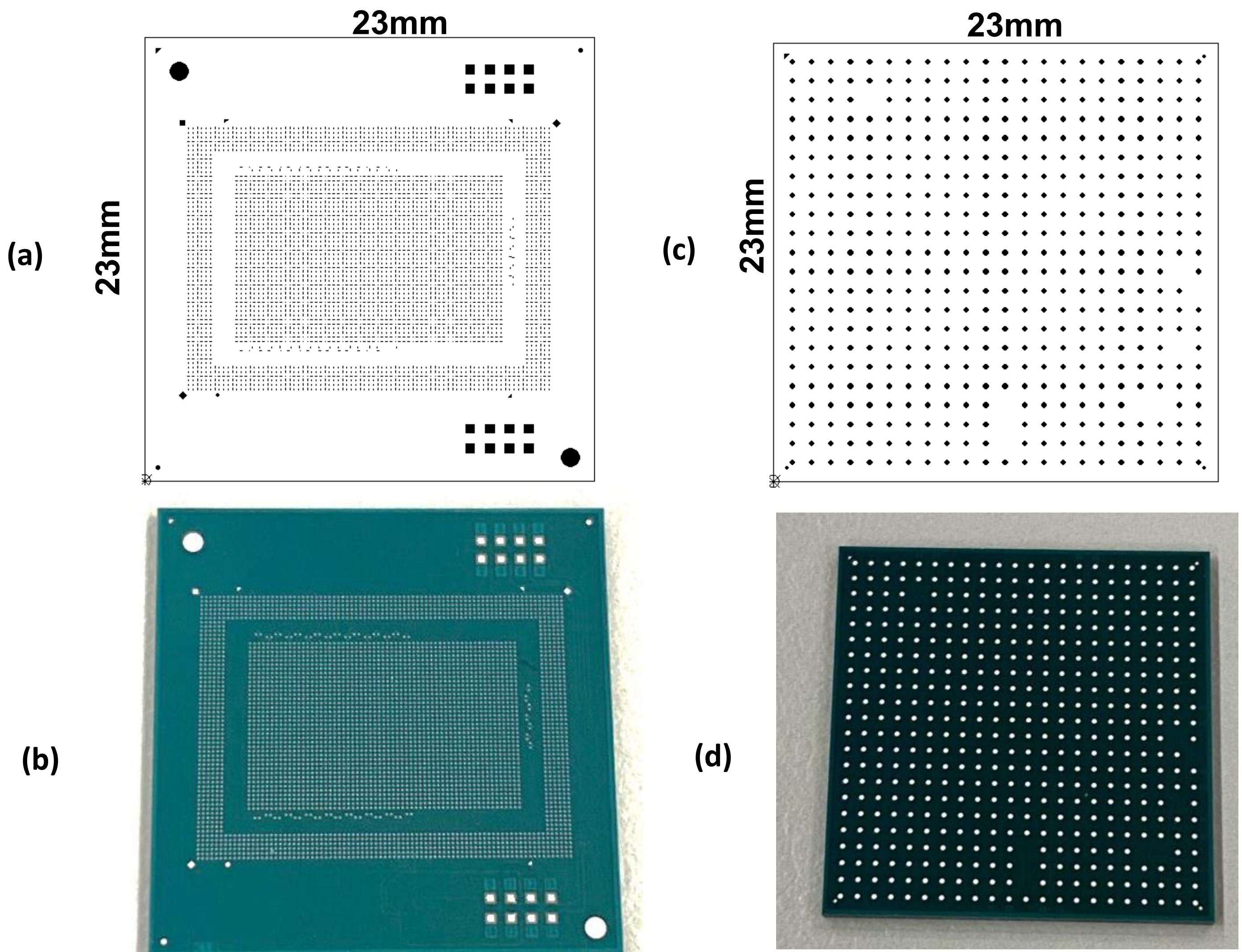




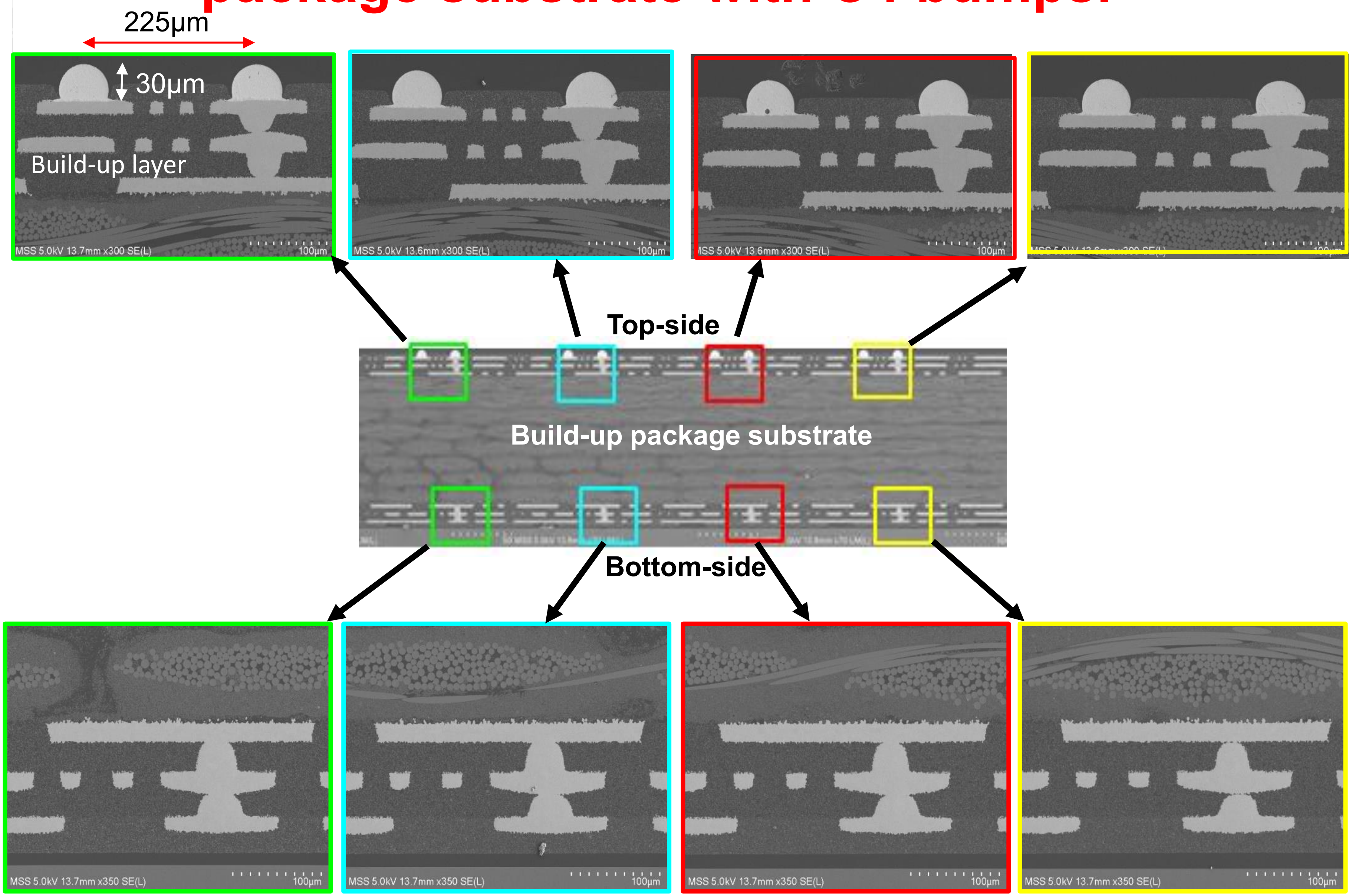
2-2-2 build-up package substrate panel. (a) Schematic. (b) Panel size. (c) Cross section image. (d) Tow- view of the fabricated build-up substrate. (e) Bottom-view of the fabricated build-up substrate.



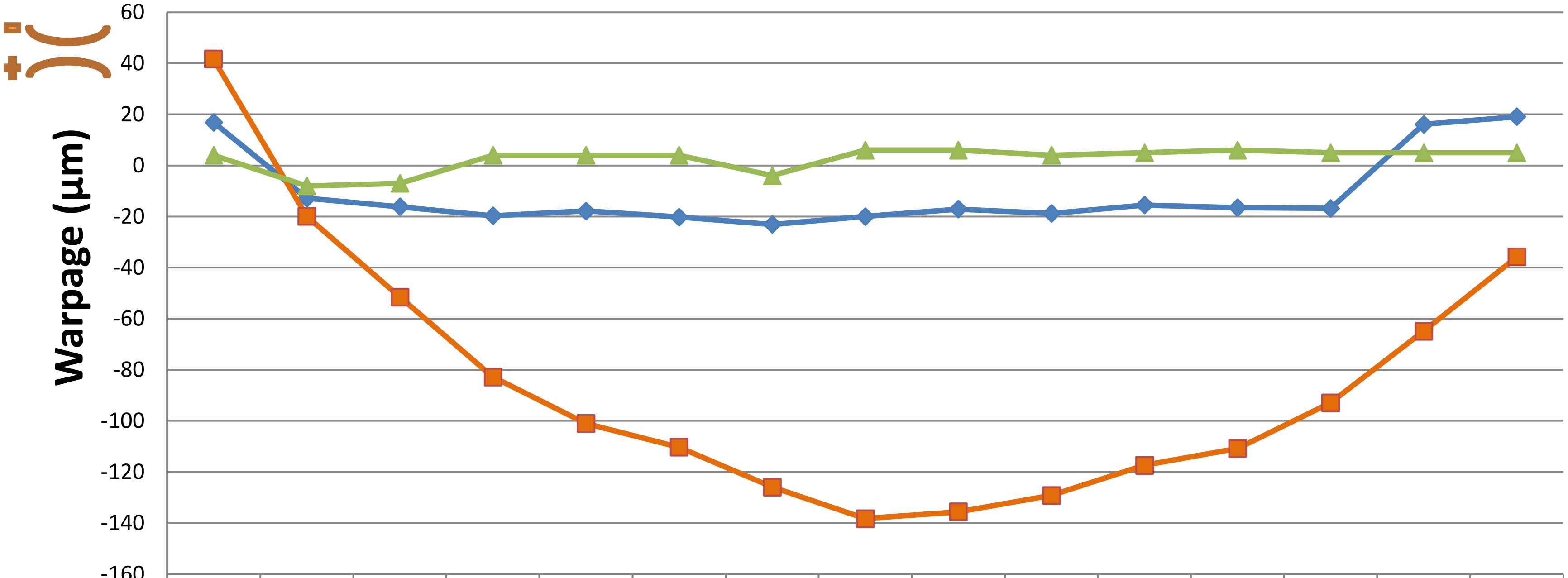
Individual build-up package substrate. (a) Schematic of the top-view of the build-up substrate. (b) Top-view of the fabricated build-up substrate. (c) Schematic of the bottom-view of the build-up substrate. (d) Bottom-view of the fabricated build-up substrate.



SEM images of the fabricated 2-2-2 build-up package substrate with C4 bumps.

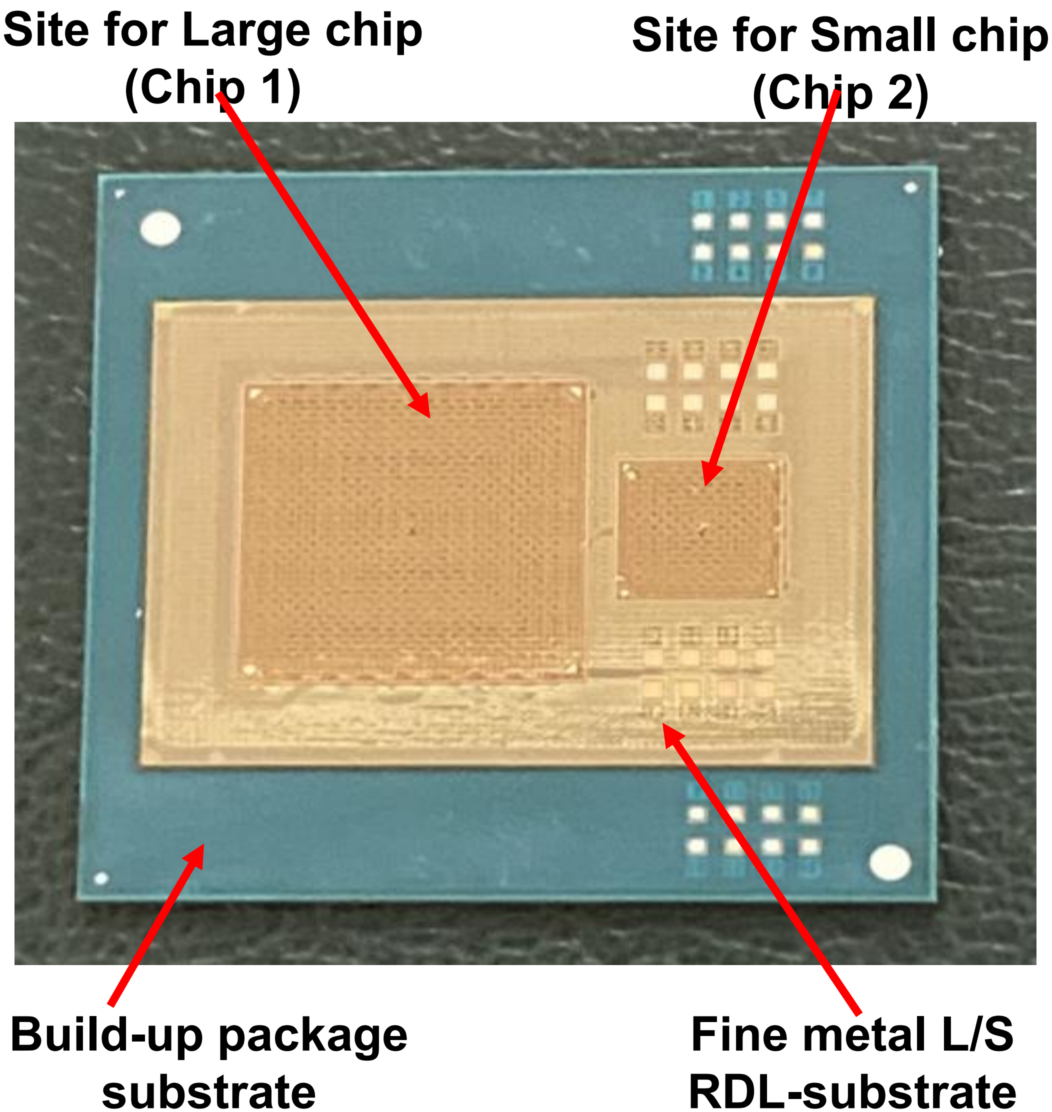


Shadow Moire warpage measurement of build-up substrate (BU), fine metal L/S RDL-substrate on glass carrier RDL(G), and fine metal L/S RDL-substrate on organic carrier RDL(O).

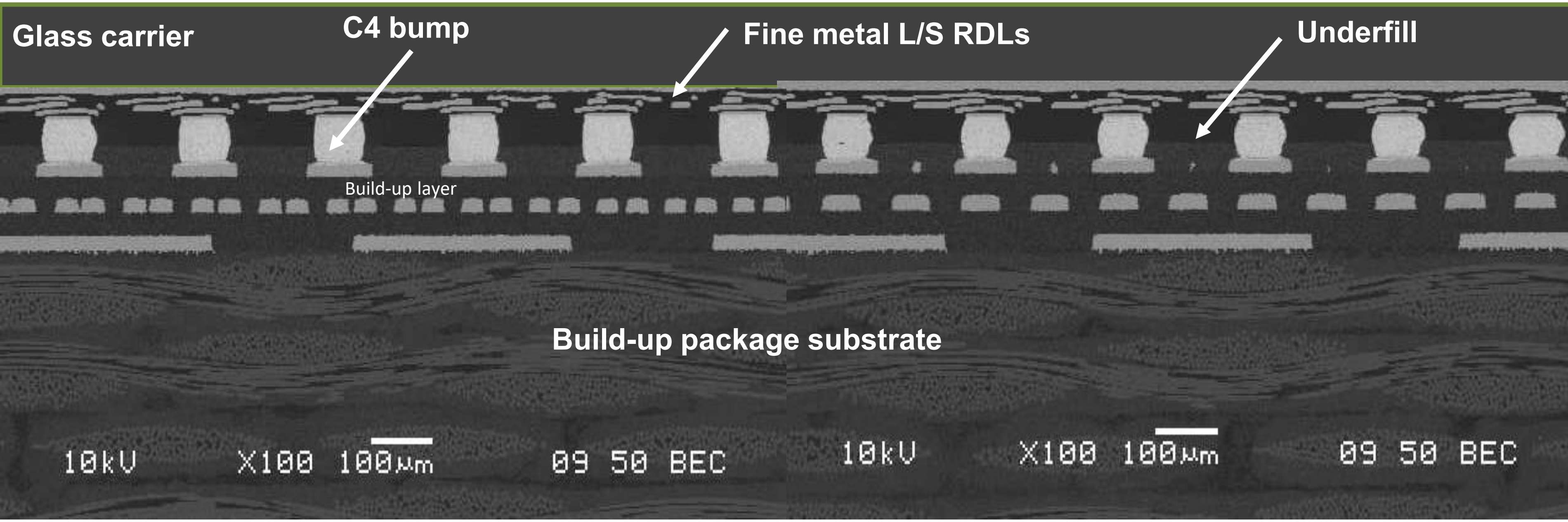


	30oC	100oC	150oC	180oC	200oC	220oC	240oC	260oC	240oC	220oC	200oC	180oC	150oC	100oC	30oC
BU	16.9	-12.8	-16.2	-19.7	-17.8	-20.2	-23.1	-20	-17.1	-18.8	-15.5	-16.5	-16.8	16.1	19.1
RDL(O)	41.7	-19.9	-51.5	-82.8	-101	-110.3	-125.9	-138.3	-135.6	-129.2	-117.4	-110.8	-92.9	-64.9	-35.8
RDL(G)	4	-8	-7	4	4	4	-4	6	6	4	5	6	5	5	5

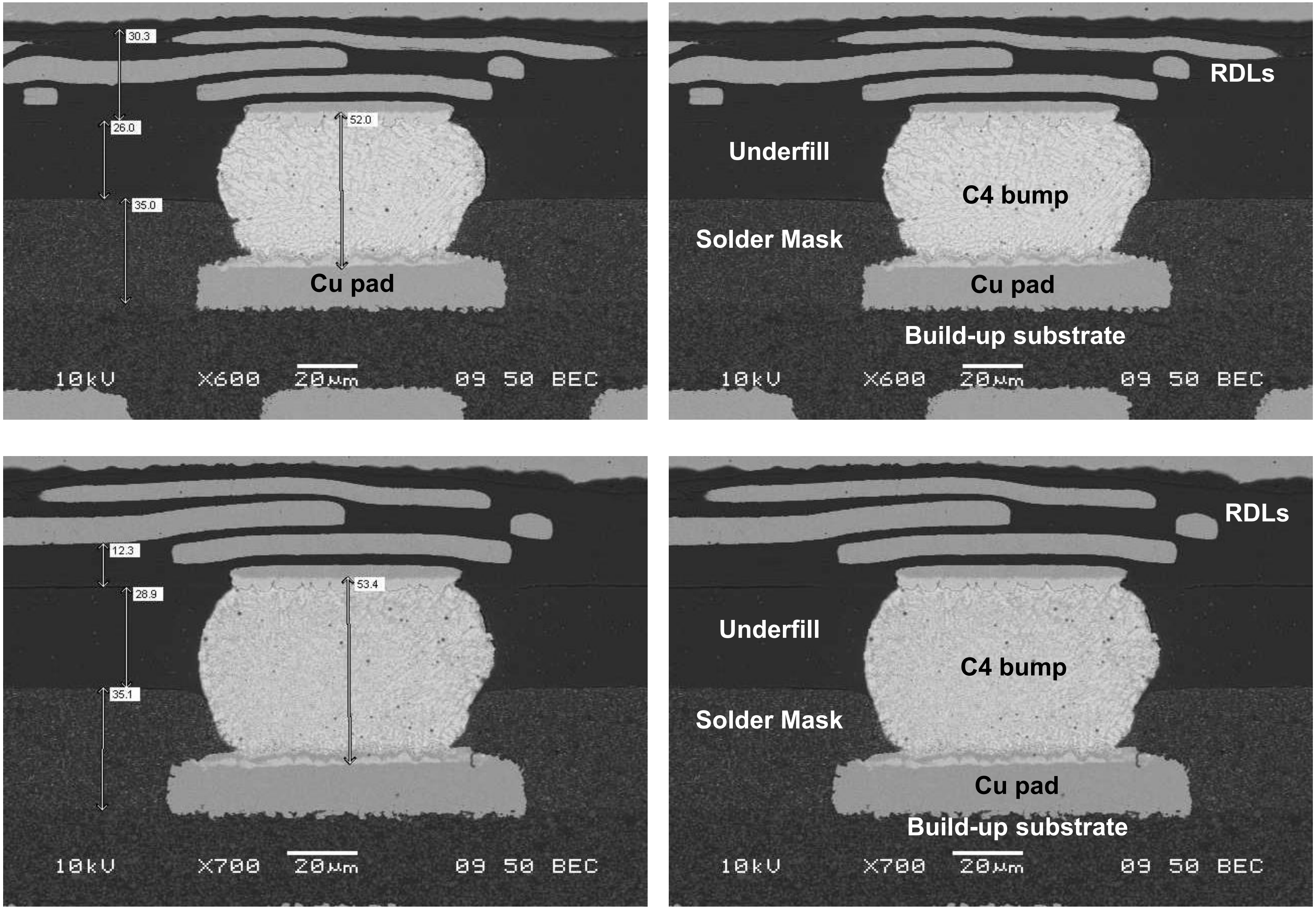
Hybrid substrate = fine metal L/S RDL-substrate soldered on top of the build-up package substrate.



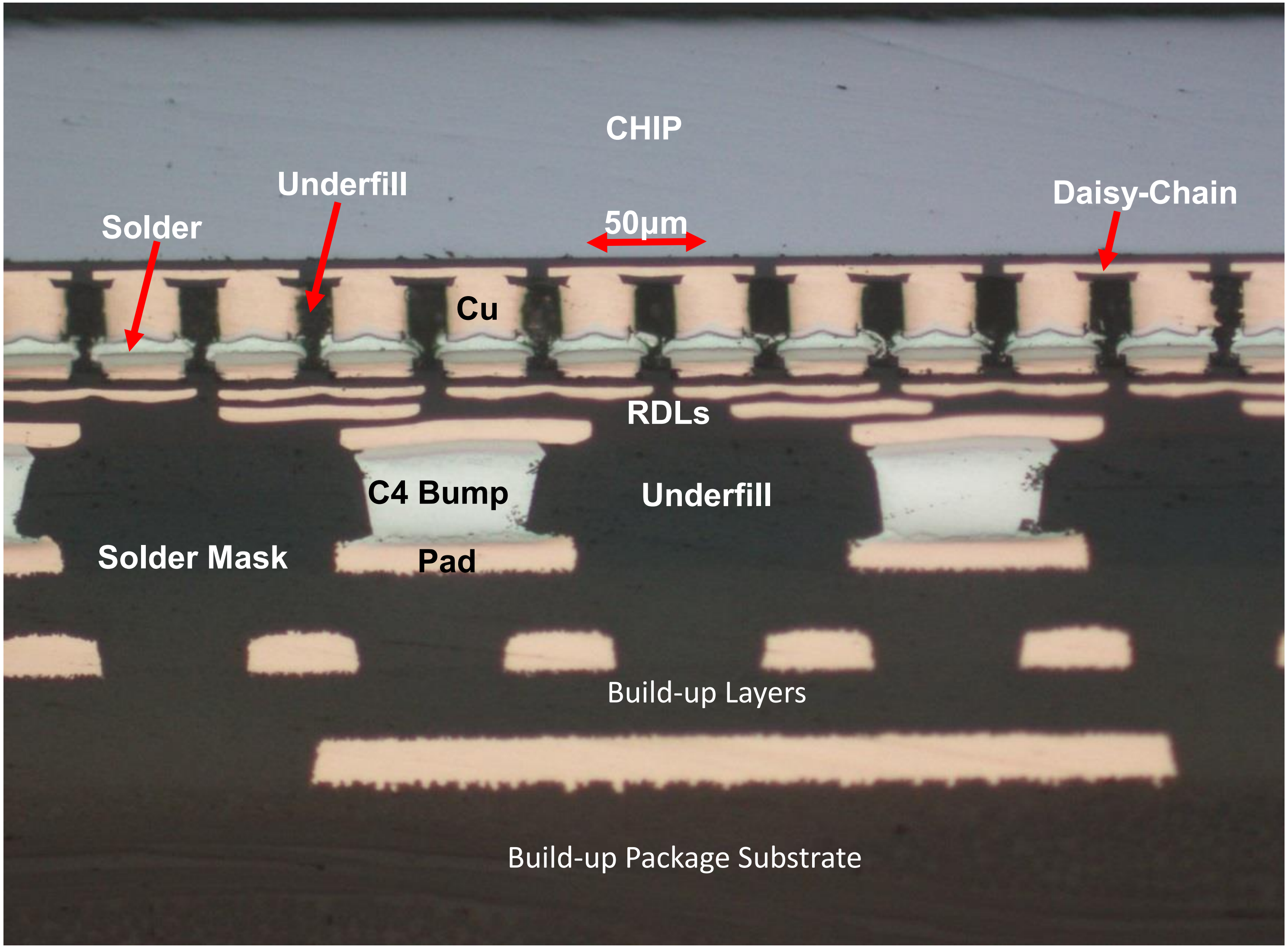
Cross section image of the hybrid substrate



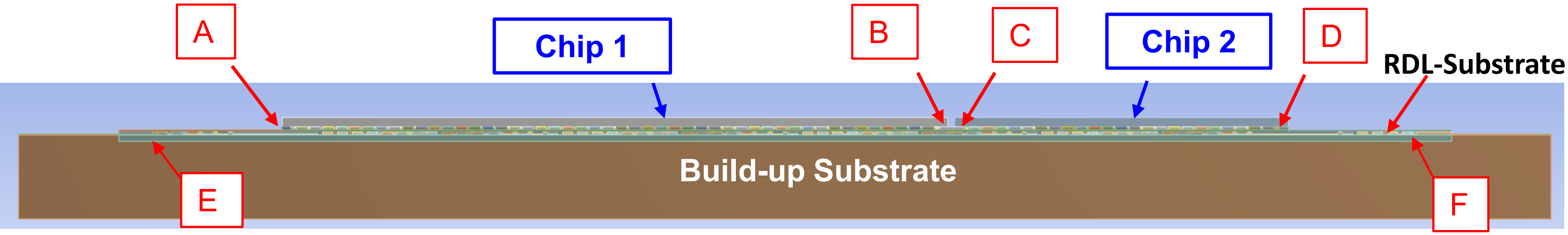
Close-up look at the cross section SEM images of the hybrid substrate



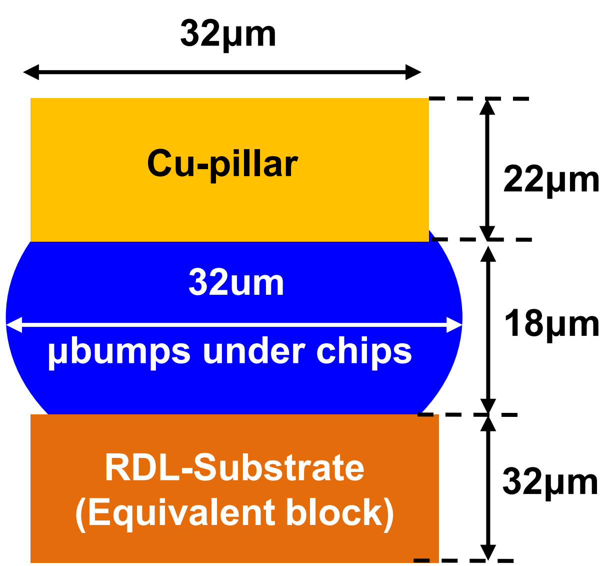
Heterogeneous integration of 2-chip package on the hybrid substrate = fine metal L/S RDL-substrate + build-up substrate.

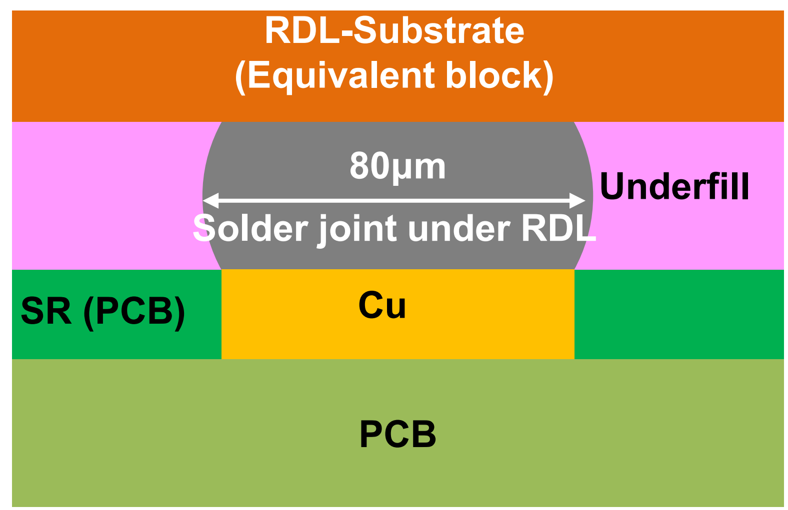


The structure and µbump joints and solder joints



A and B are the µbumps under Chip 1. C and D are the µbumps under Chip 2.
E and F are the solder joints under the RDL-substrate.

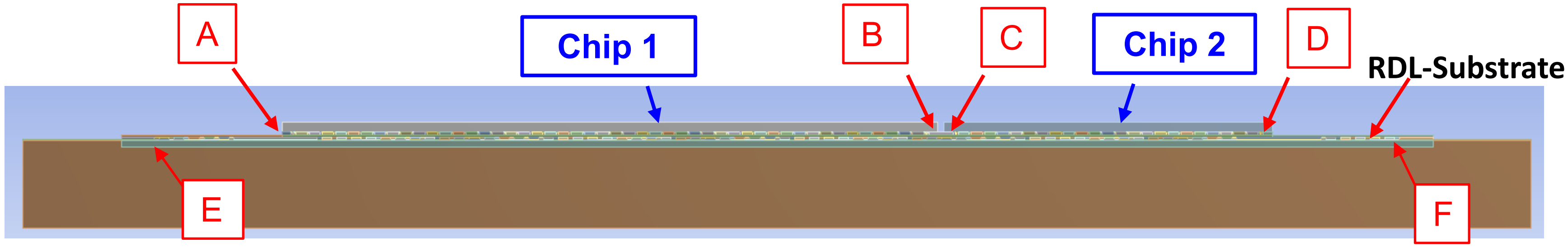




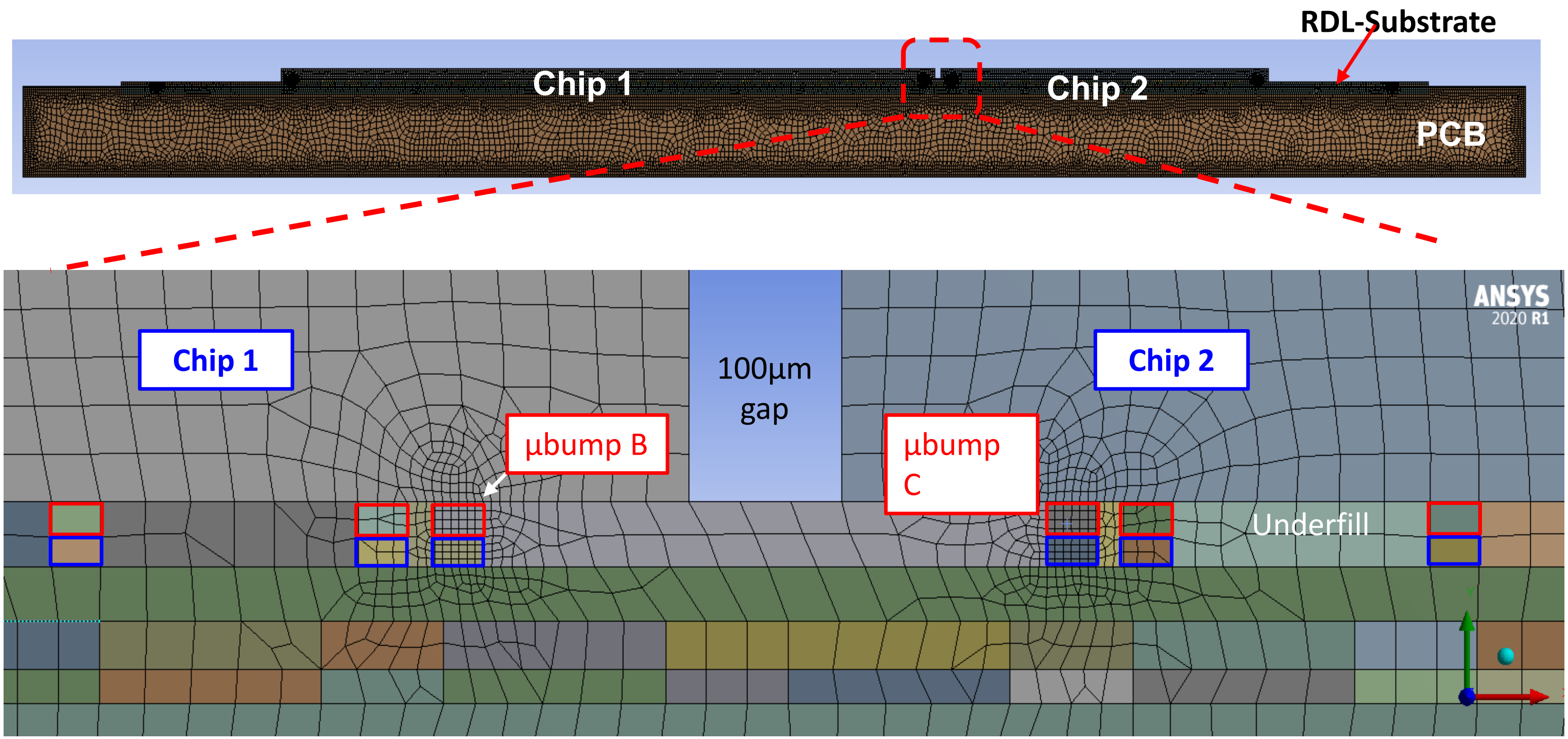
µbumps: A B C D

Solder joints: E F

Finite element modeling of the PCB assembly of heterogeneous integration of 2 chips on hybrid substrate



A and B are the µbumps under Chip 1. C and D are the µbumps under Chip 2.
E and F are the solder joints under the RDL-substrate.

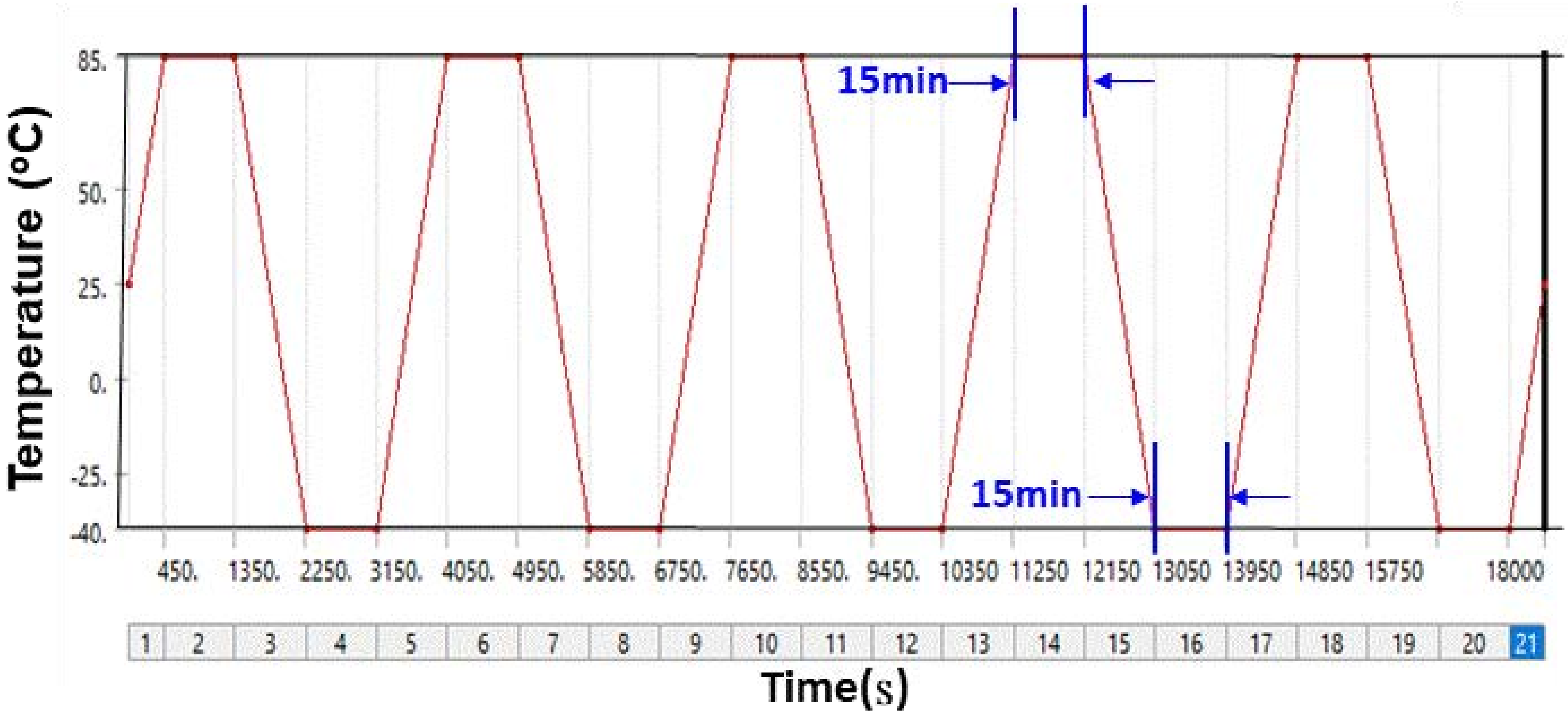


Material Properties for simulation

Materials	CTE ($10^{-6}/^oC$)	Young's Modulus (GPa)	Poisson's Ratio
Copper	16.3	121	0.34
PCB	$\alpha_x = \alpha_y = 18$ $\alpha_z = 70$	$E_x = E_y = 22$ $E_z = 10$	0.28
Solder Mask (RDL)	60	2.1	0.3
Solder	21 + 0.017T(°C)	49 - 0.07T(°C)	0.3
EMC(PID)	60	2.1	0.3
Silicon	2.8	131	0.278
Solder Mask (PCB)	39	4.1	0.3
RDL Equiv. block	35.58	68.54	0.32
Underfill	50	4.5	0.35

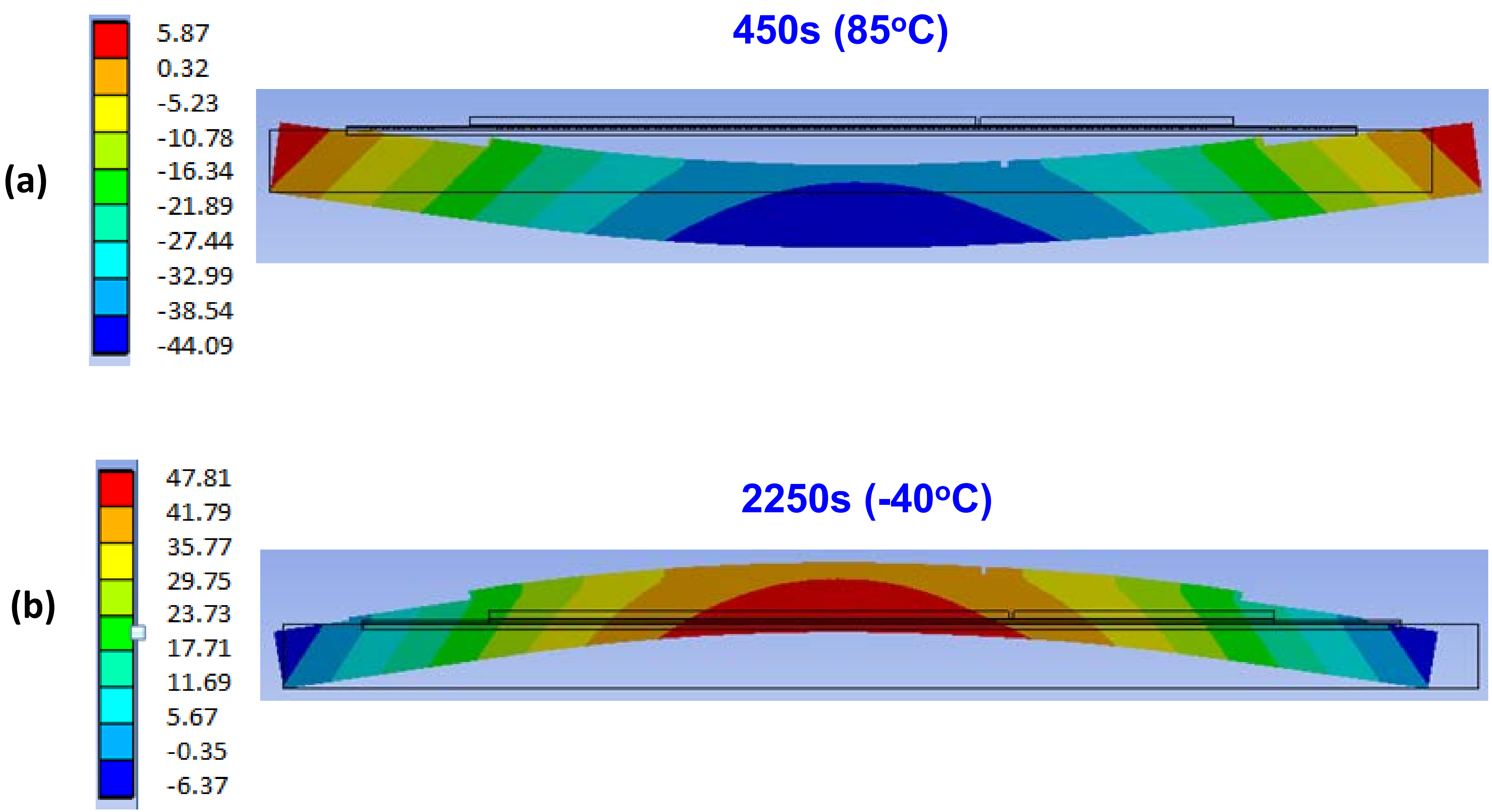
The constitutive equation of solder: $\frac{d\varepsilon}{dt} = 500000[sinh(0.01\sigma)]^5 exp\left(-\frac{5800}{T}\right)$
where T is in Kelvin and σ is in MPa.

Temperate boundary condition

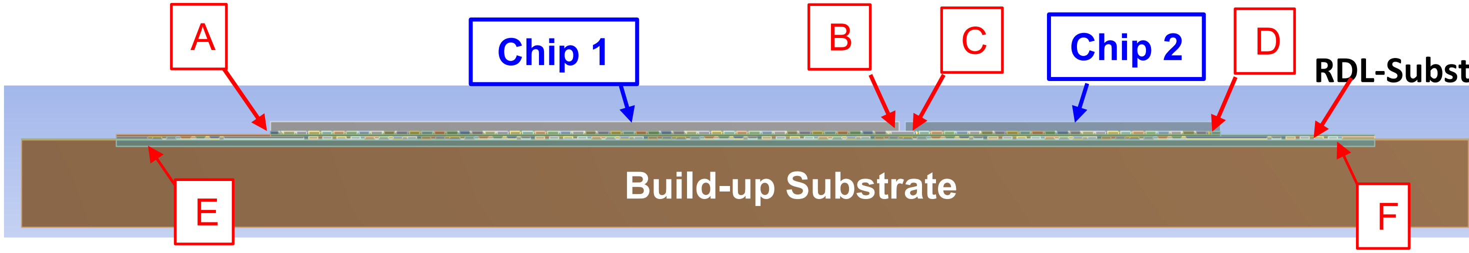


- ➢ **The temperature is −40 ⇆ 85°C.**
- ➢ **The cycle time is 60 min.**
- ➢ **The ramp-up, ramp-down, dwell-at-hot, and dwell-at-cold are each 15 min.**

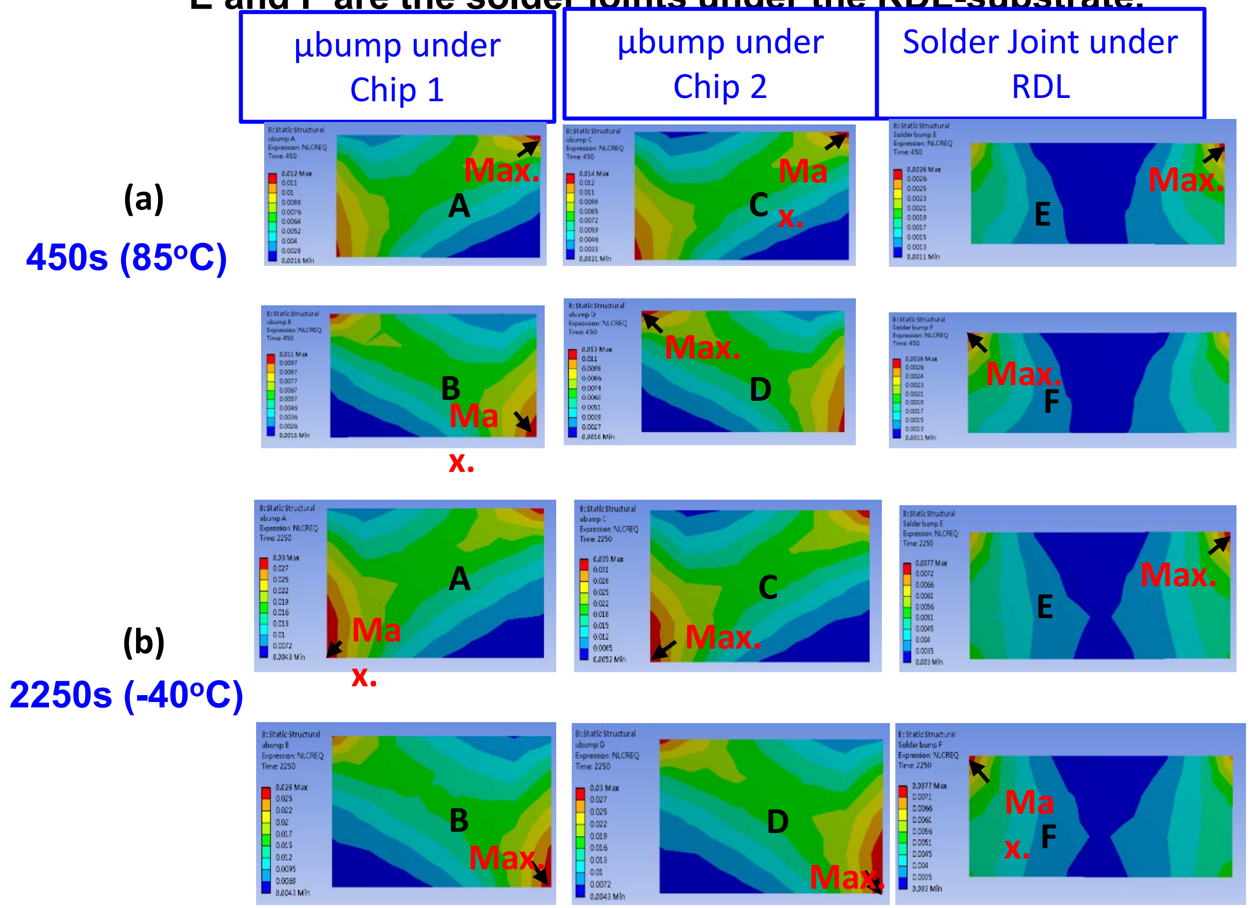
Deformed shape (color contours) and un-deformed shape (dark lines).
(a) At 450s (85°C). (b) At 2250s (-40°C).



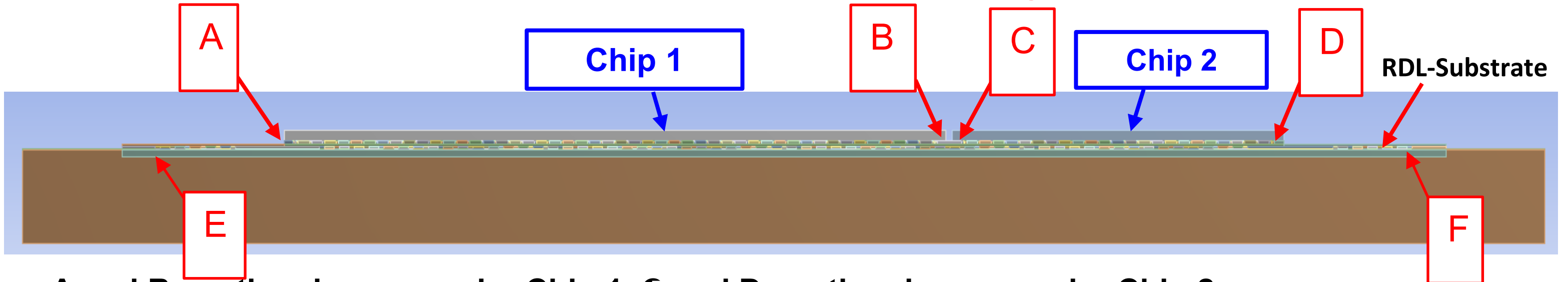
Accumulated creep strain contour distributions in µbump joints A, B, C, and D, and solder joints E and F.



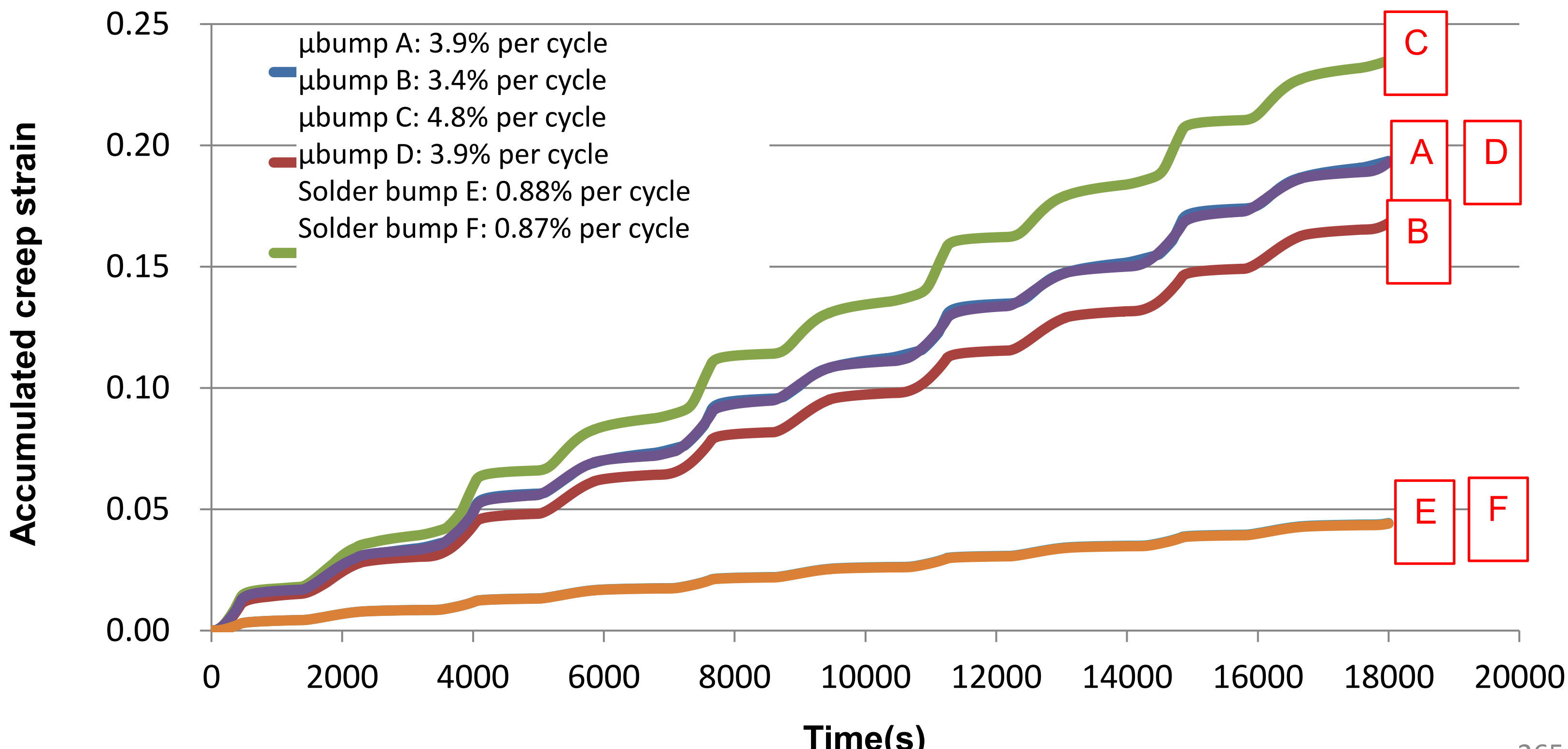
A and B are the µbumps under Chip 1. C and D are the µbumps under Chip 2.
E and F are the solder joints under the RDL-substrate.



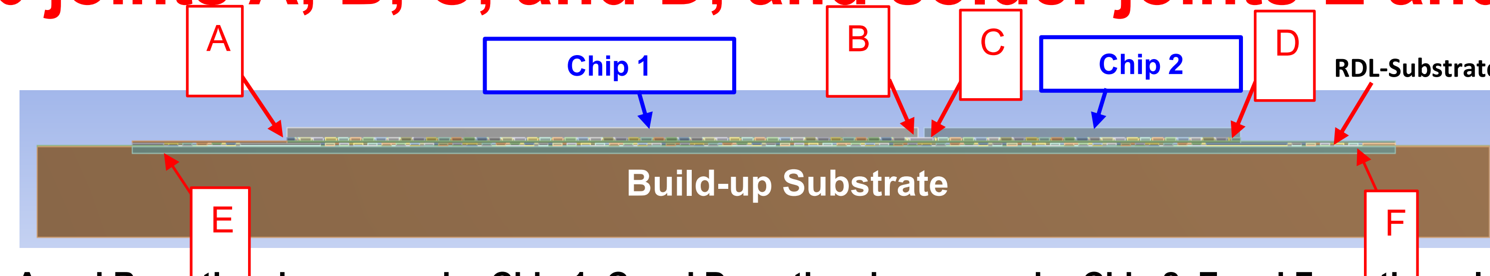
Accumulated creep strain time-history in µbump joints A, B, C, and D, and solder joints E and F.



A and B are the µbumps under Chip 1. C and D are the µbumps under Chip 2.
E and F are the solder joints under the RDL-substrate.



Creep strain energy density contour distributions in µbump joints A, B, C, and D, and solder joints E and F



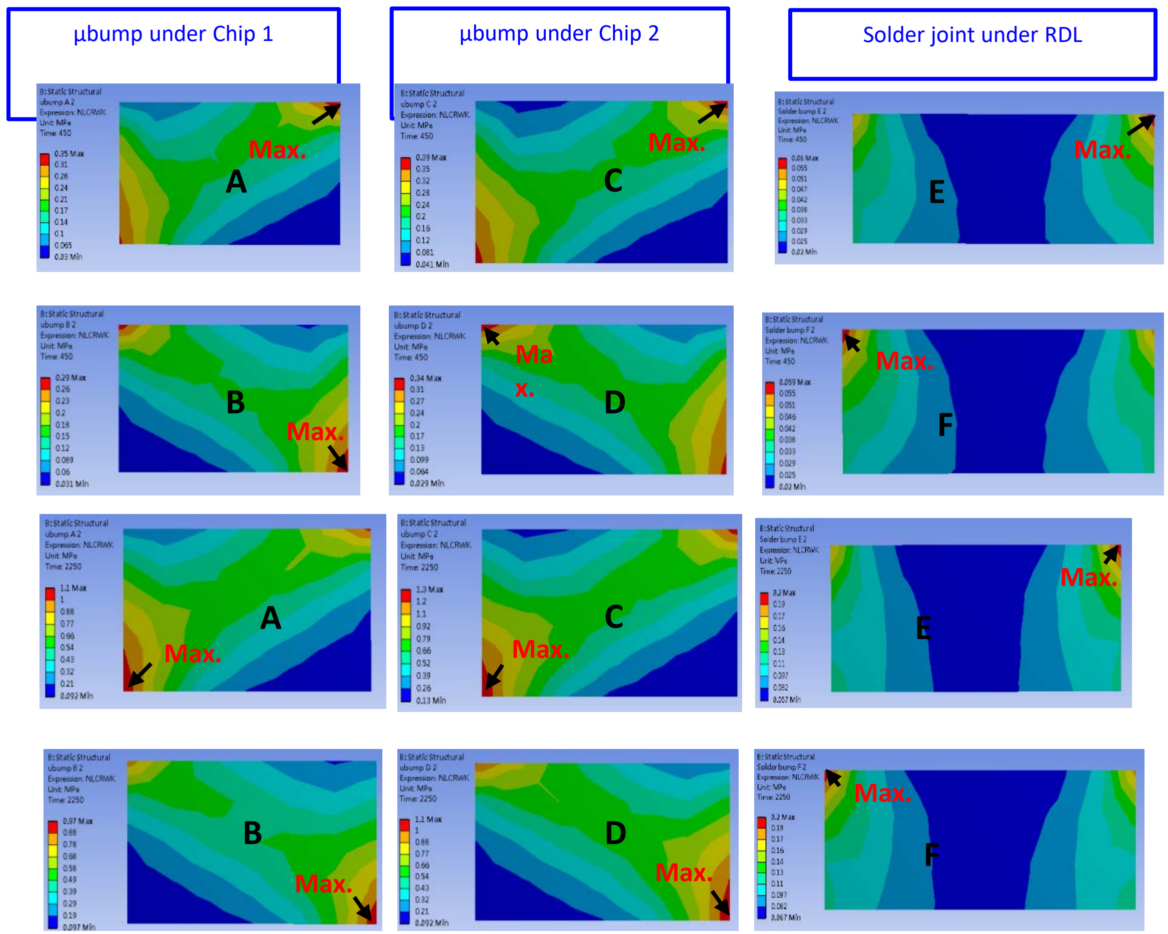
A and B are the µbumps under Chip 1. C and D are the µbumps under Chip 2. E and F are the solder joints under the RDL-substrate.

(a)

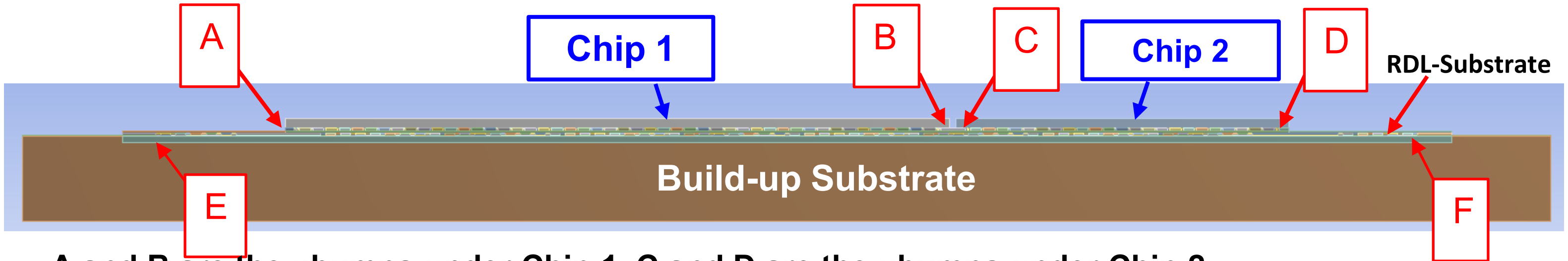
450s (85°C)

(b)

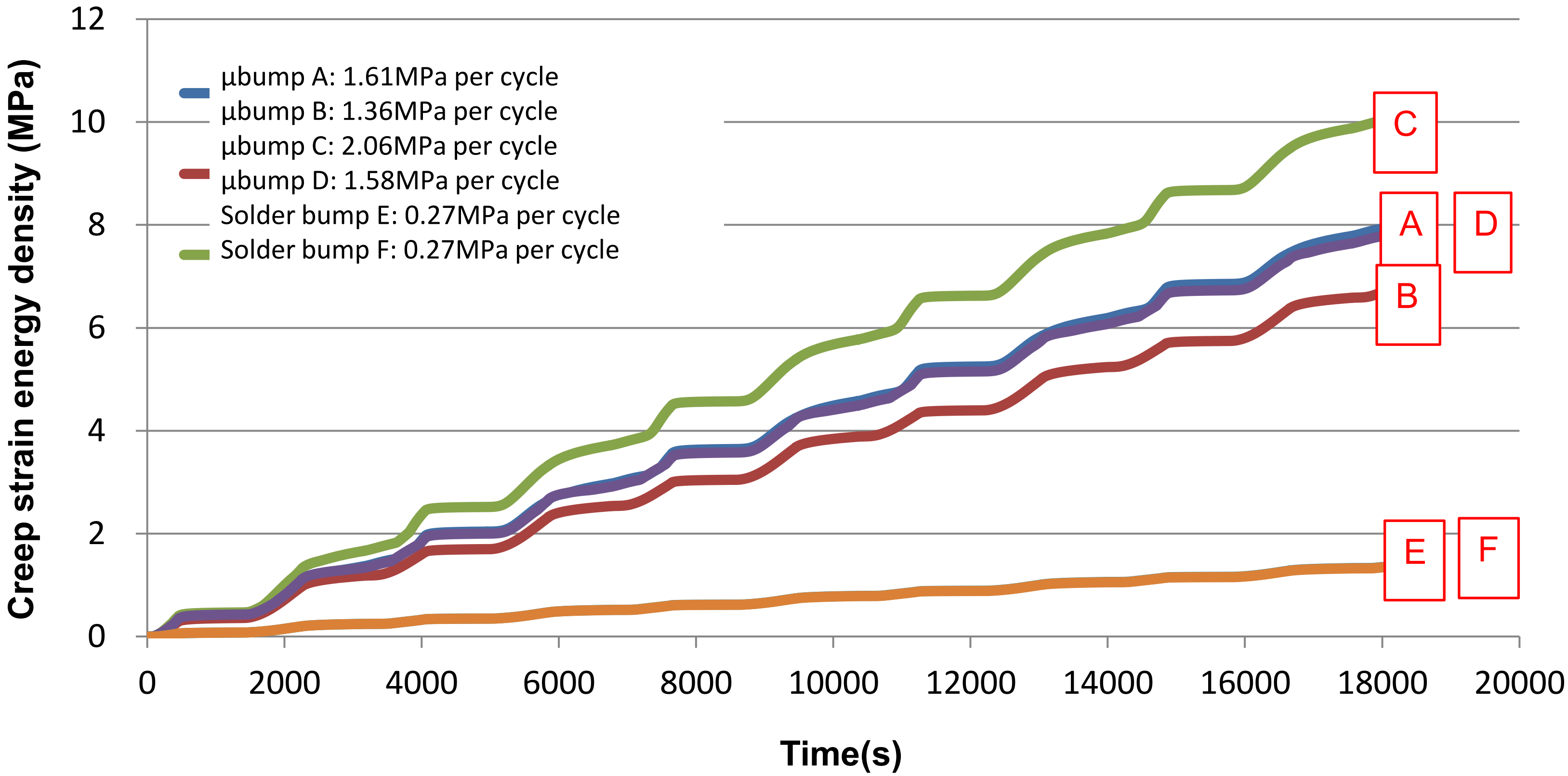
2250s (-40°C)



Creep strain energy density time-history in μbump joints A, B, C, and D, and solder joints E and F.



A and B are the μbumps under Chip 1. C and D are the μbumps under Chip 2.
E and F are the solder joints under the RDL-substrate.



SUMMARY

- The feasibility of the design, materials, process, fabrication, and reliability of a heterogeneous integration of two chips with 50μm-pitch on a hybrid substrate by a fan-out chip-last (or RDL-first) panel-level packaging has been demonstrated.
- In order to increase throughput, the fine metal L/S (2μm/2μm) RDL-substrate has been fabricated on a 515mm x 510mm temporary glass panel.
- The hybrid substrate has been fabricated by soldering the fine metal L/S RDL-substrate on top of a build-up package substrate and underfilled.
- The 50μm-pitch microbumped chips are bonded to the hybrid substrate and underfilled. There is not any carrier transferred.
- Reliability of the heterogeneous integration of two chips on the hybrid substrate assembly has been demonstrated by the thermal cycling simulation. It is found that: (a) the maximum accumulated creep strain pre cycle and creep strain energy density per cycle of the microbump solder joints between the chips and the RDL-substrate is larger than that between the RDL-substrate and the build-up package substrate, and (b) the maximum values of the accumulated creep strain per cycle and the creep strain energy density pre cycle are too small to create reliability concerns in most operating conditions.

Development of High-Density Hybrid Substrate for Heterogeneous Integration

Chia-Yu Peng, John H Lau, Cheng-Ta Ko, Paul Lee, Eagle Lin, Kai-Ming Yang, Puru Bruce Lin, Tim Xia, Leo Chang, Ning Liu, Curry Lin, Tzu Nien Lee, Jason Wang, Mike Ma, and Tzyy-Jang Tseng

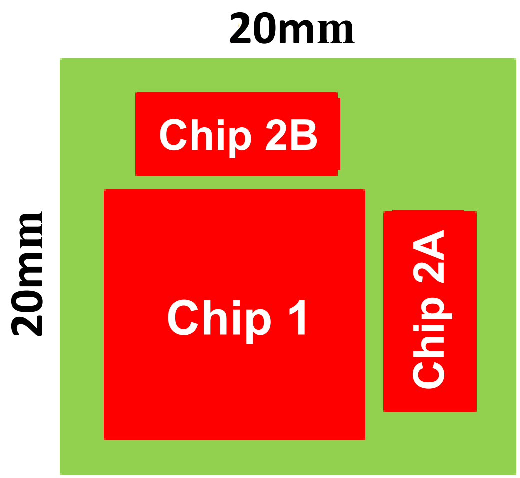
Unimicron Technology Corporation
Tony_Peng@unimicron.com

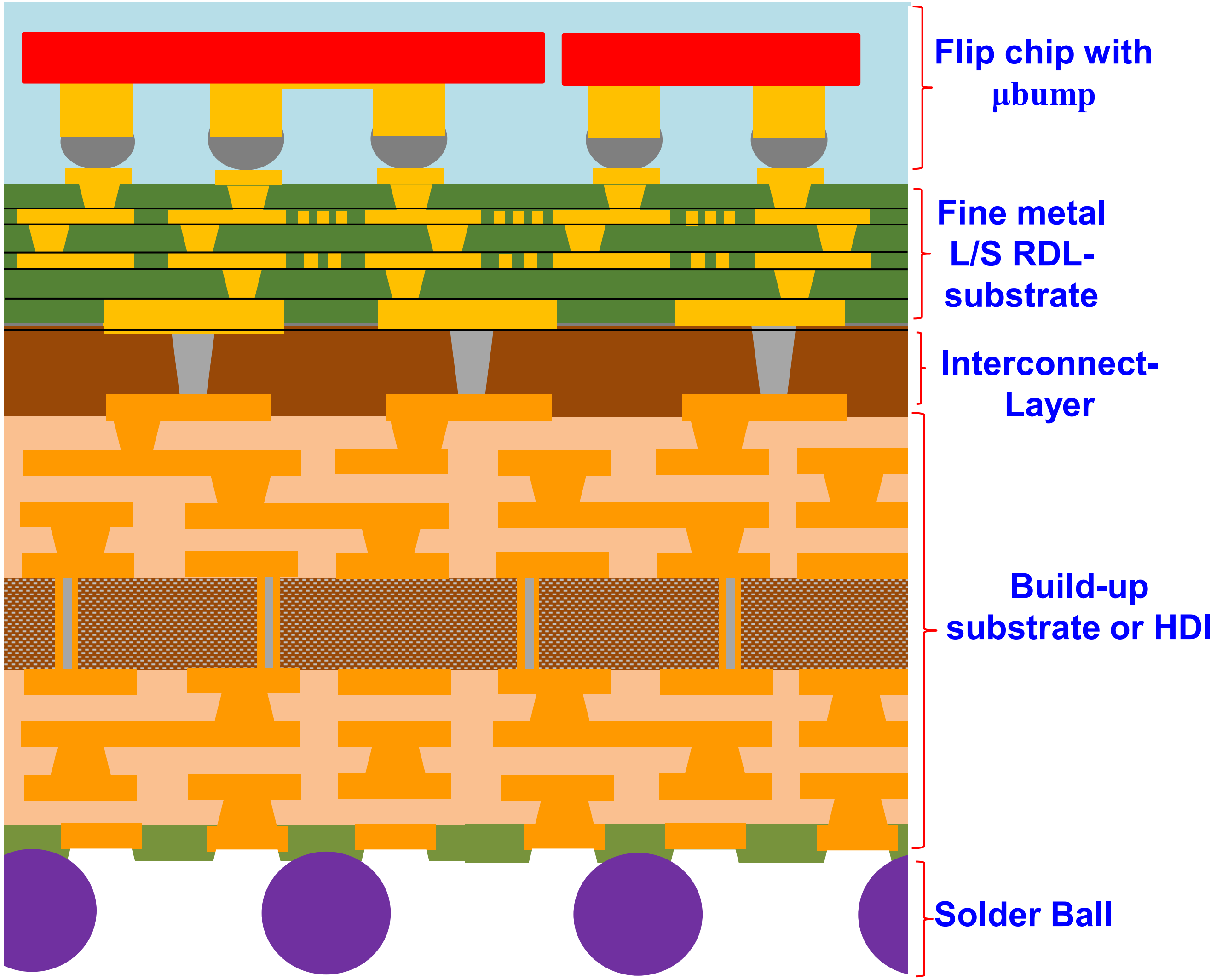
Peng, C., J. H. Lau, C. Ko, P. Lee, E. Lin, K. Yang, P. Lin, T. Xia, L. Chang, N. Liu, C. Lin, T. Lee, J. Wang, M. Ma, and T. Tseng, "High-Density Hybrid Substrate for Heterogeneous Integration", *IEEE Transactions on CPMT*, Vol. 12, No.3, March 2022, pp. 469-478.

CONTENTS

- Introduction
- High-Density Hybrid Substrate for Chiplets Heterogeneous Integration
    - Fine Metal L/S RDL-substrate
    - Interconnect-Layer
    - HDI PCB
- Characterizations of the Hybrid Substrate
    - X-Ray and OM
    - Continuity Check
- Summary

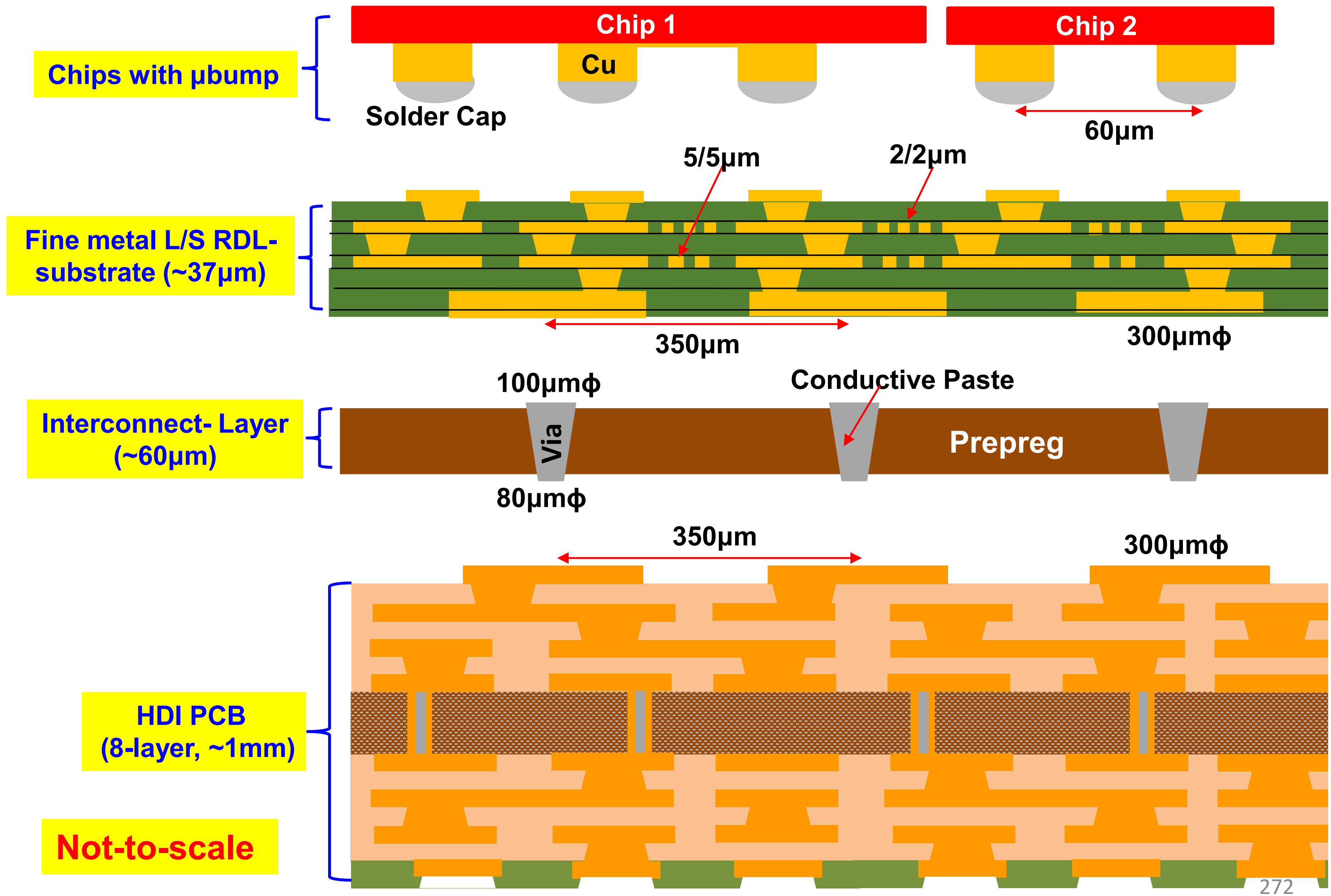
Top-view and cross-section view of chiplets heterogeneous integration on hybrid substrate



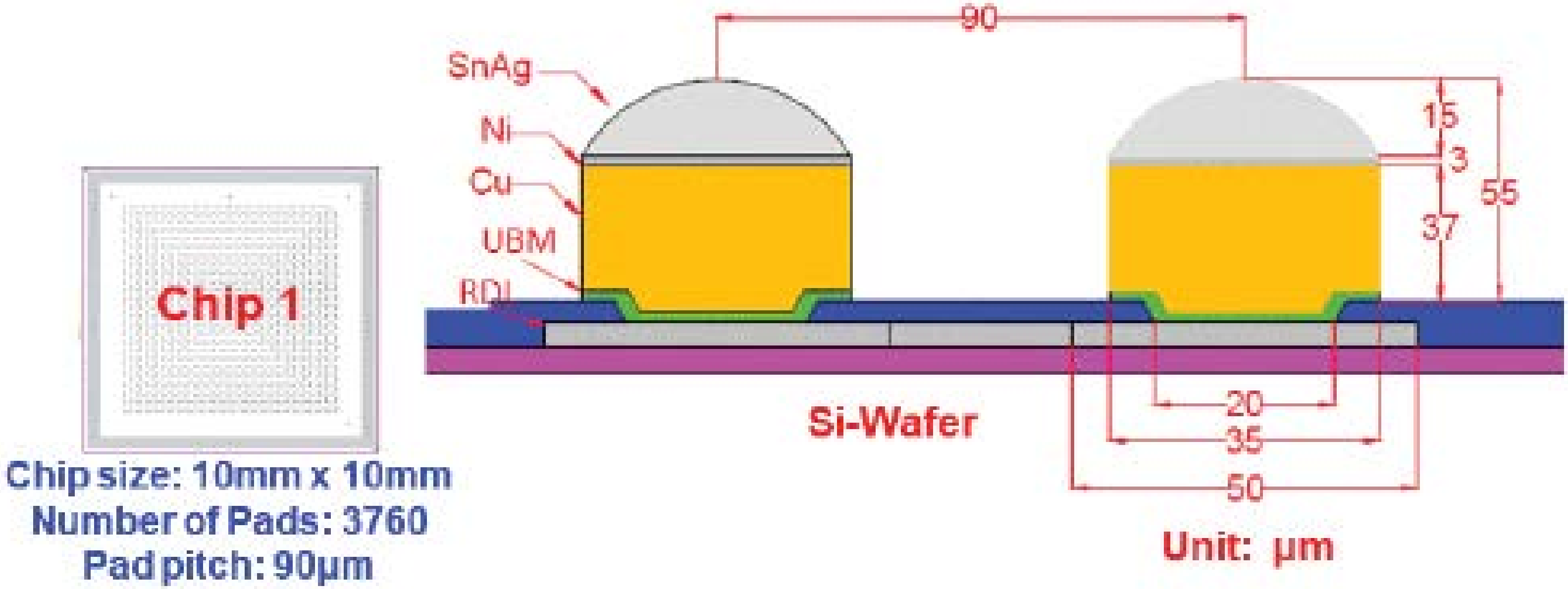


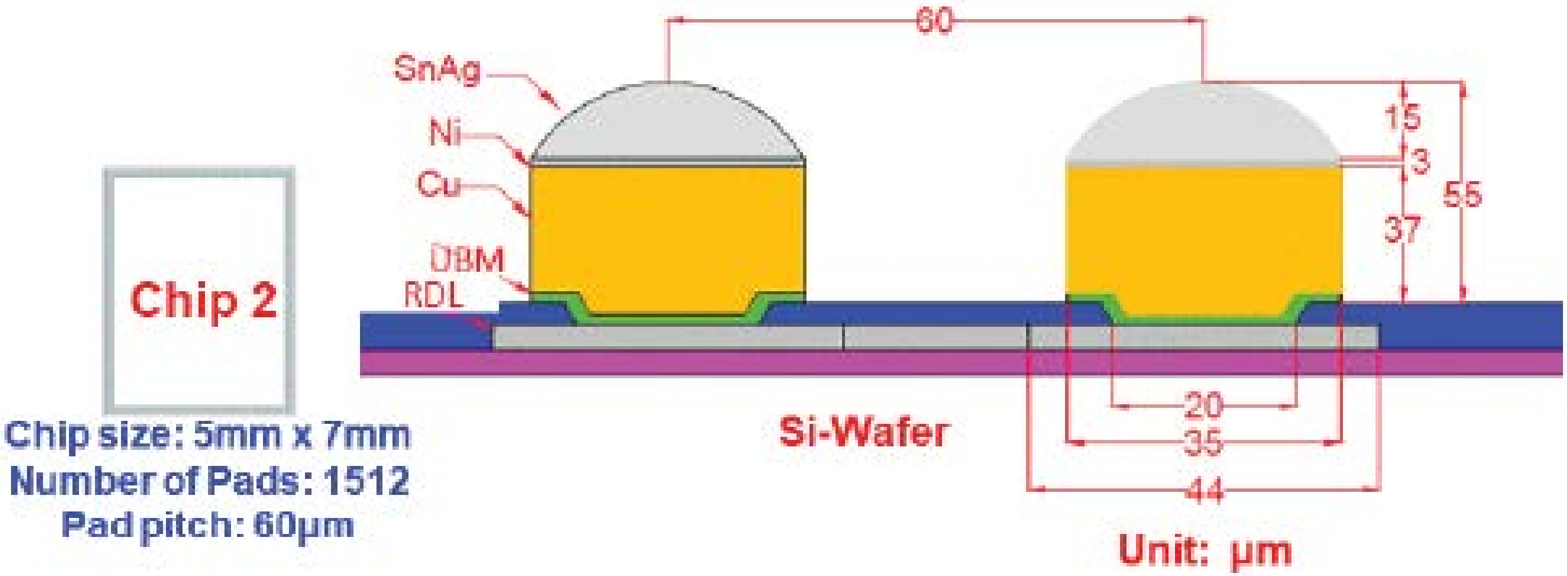
Not-to-scale

Key parts of the test package

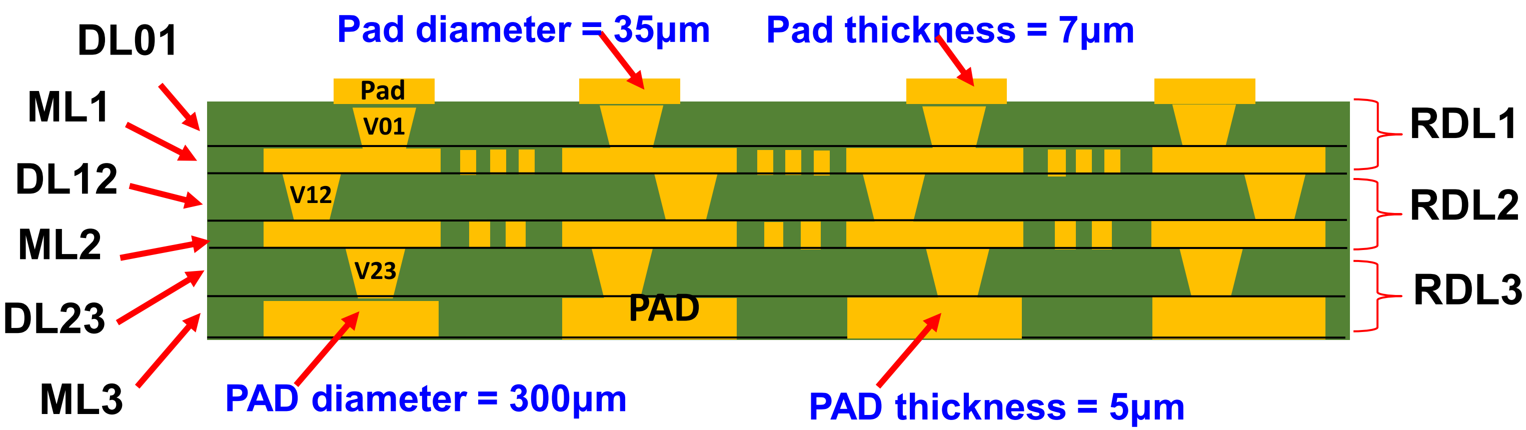


Schematic of the test chips



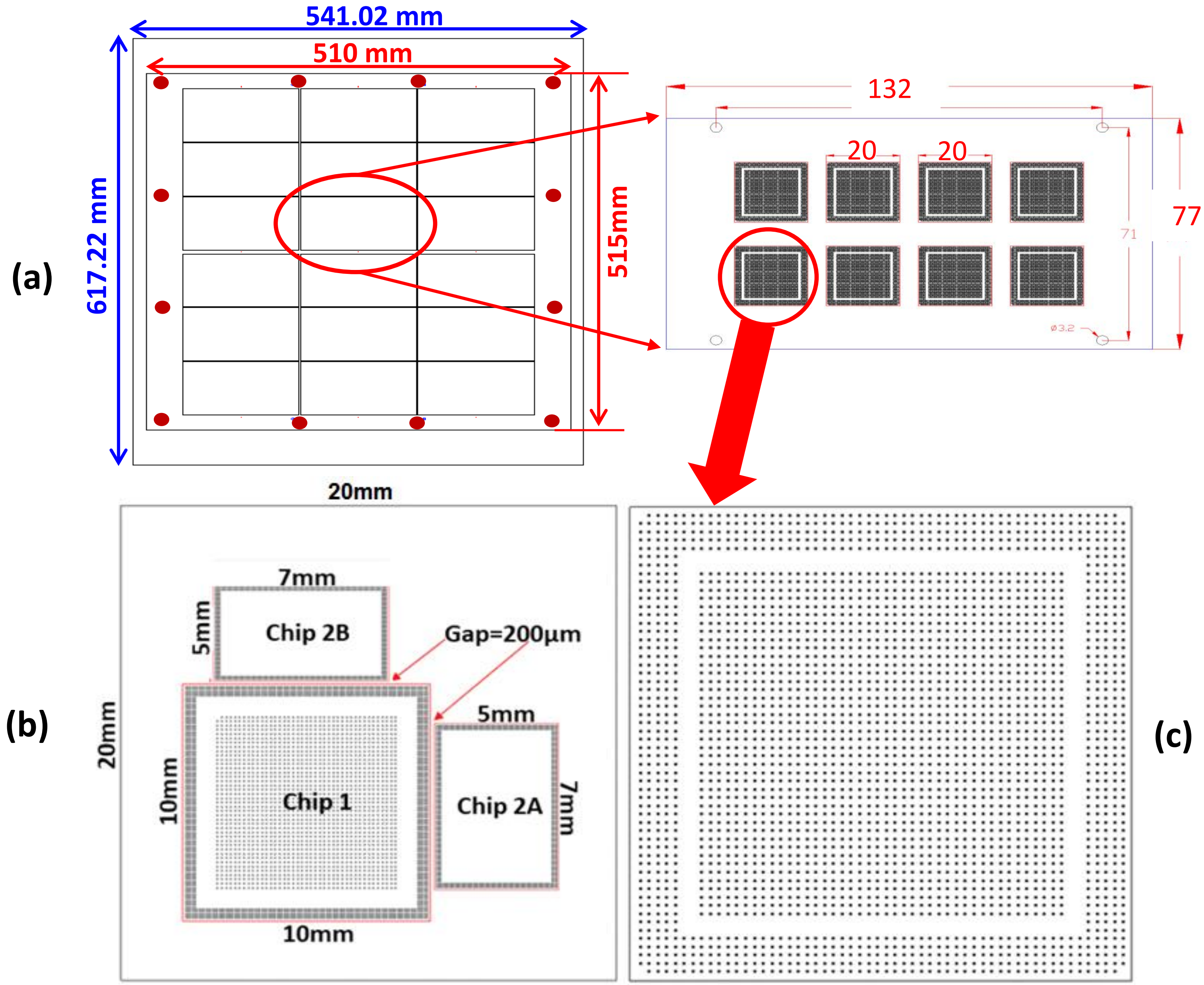


Fine metal L/S 3-layer RDL-substrate

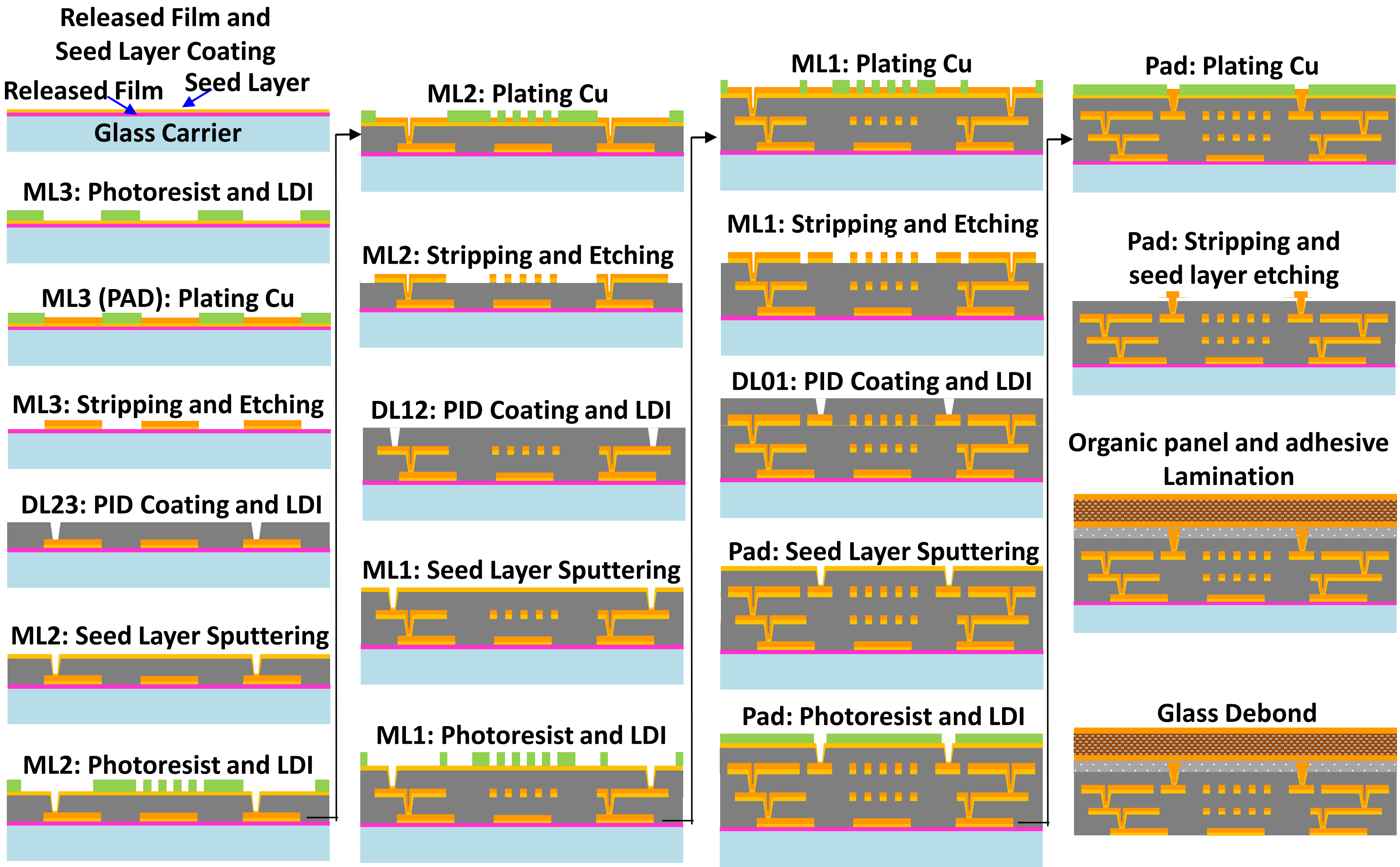


RDLs	Key Elements of RDL	Line width/ Spacing (L/S)	Thickness (H)	Via Dia. (T/B)
RDL1	ML1 (Metal layer 1)	2/2μm	2.5μm	NA
	DL01 (Dielectric layer between Pad and ML1)	NA	7.5μm	NA
	V01 (Via opening between contact Pad and ML1)	NA	NA	17/10μm
RDL2	ML2 (Metal layer 2)	5/5μm	3.5μm	NA
	DL12 (Dielectric layer between ML1 and ML2)	NA	6.5μm	NA
	V12 (Via opening between ML1 and ML2)	NA	NA	32/25μm
RDL3	ML3 (Metal layer 3) (PAD)	NA	5μm	NA
	DL23 (Dielectric layer between ML2 and ML3)	NA	5μm	NA
	V23 (Via opening between ML2 and ML3)	NA	NA	32/25μm

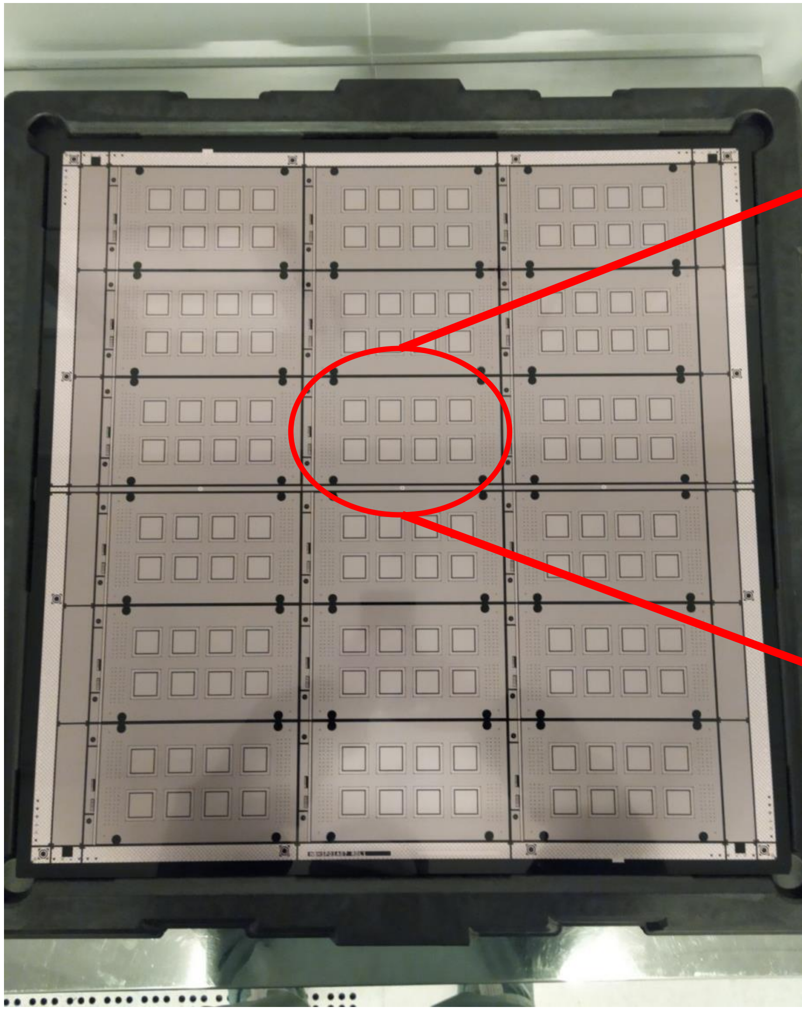
(a) Panel for making the RDL-substrates. (b) Top-view. (c) Bottom-view

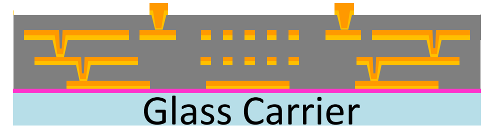


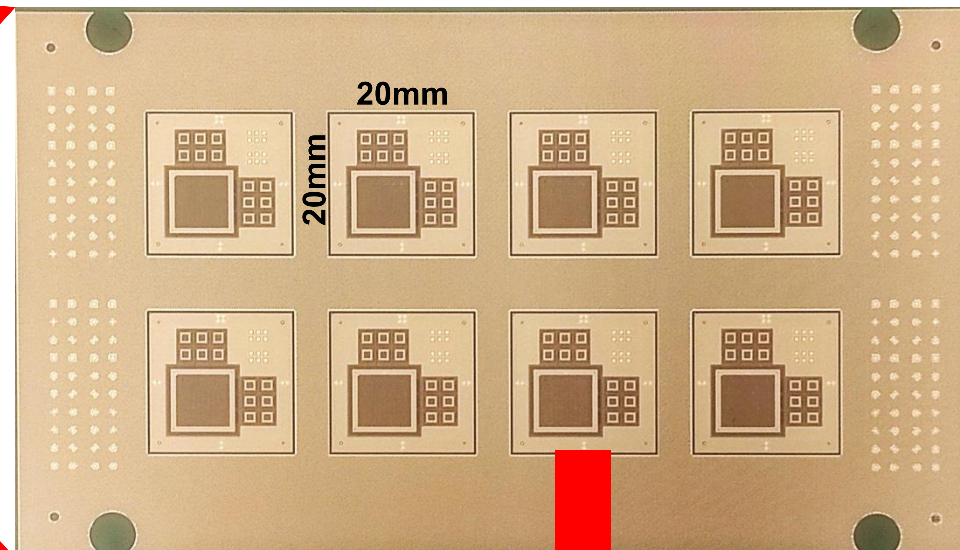
Key process steps in making the RDL-substrate

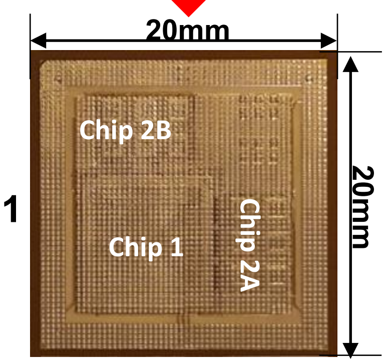


Glass panel for making the RDL-substrate



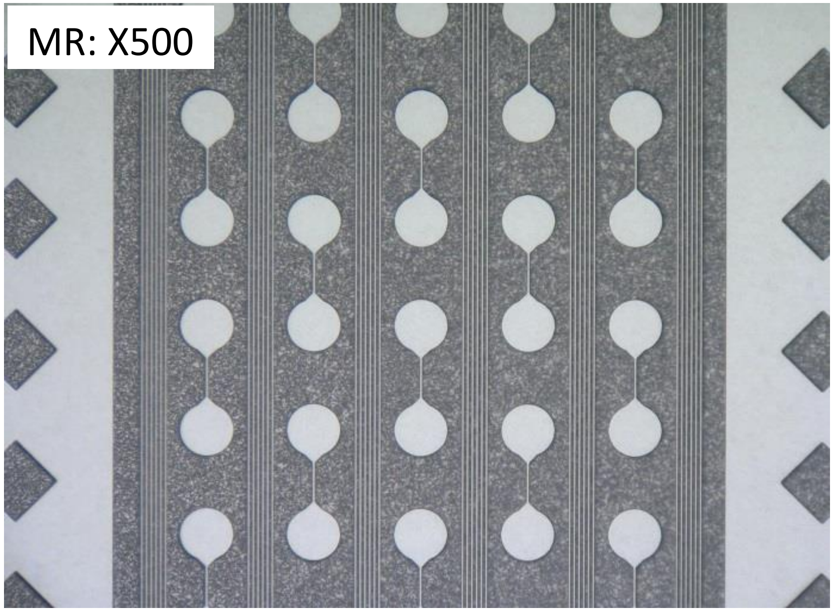


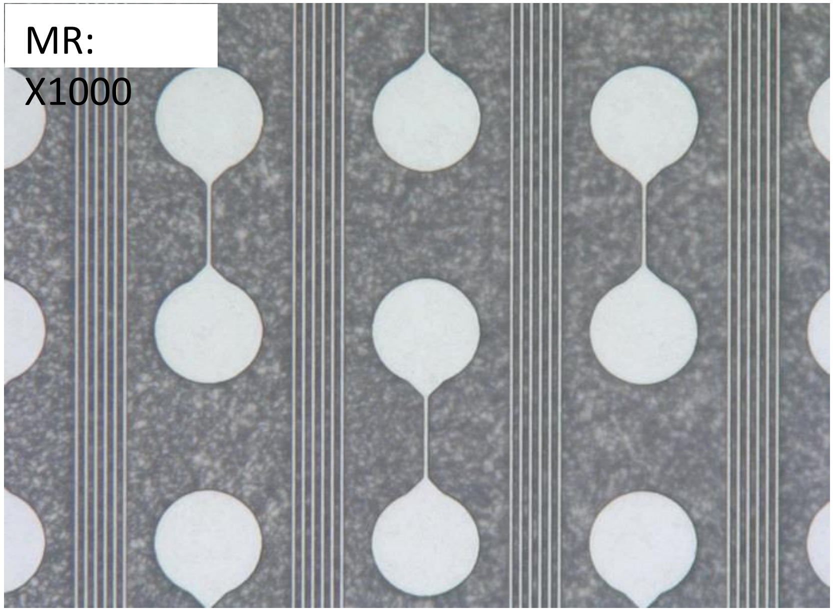


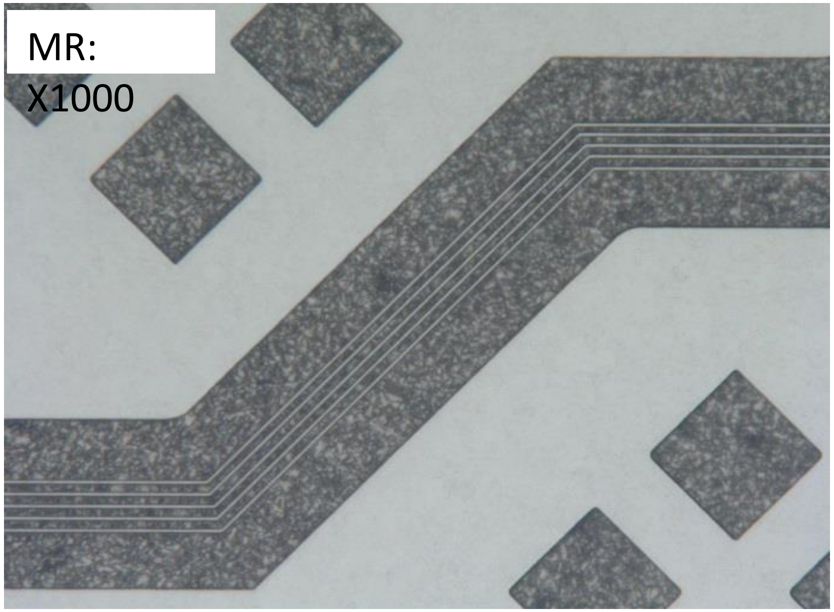


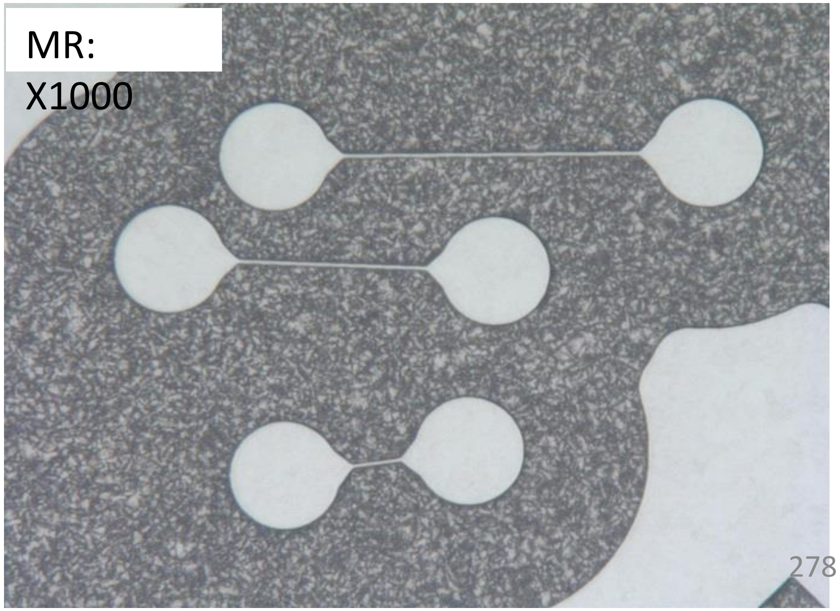
Bonging pads for Chip 1 and Chip 2A & 2B

OM images of the RDL-substrate (top-side)

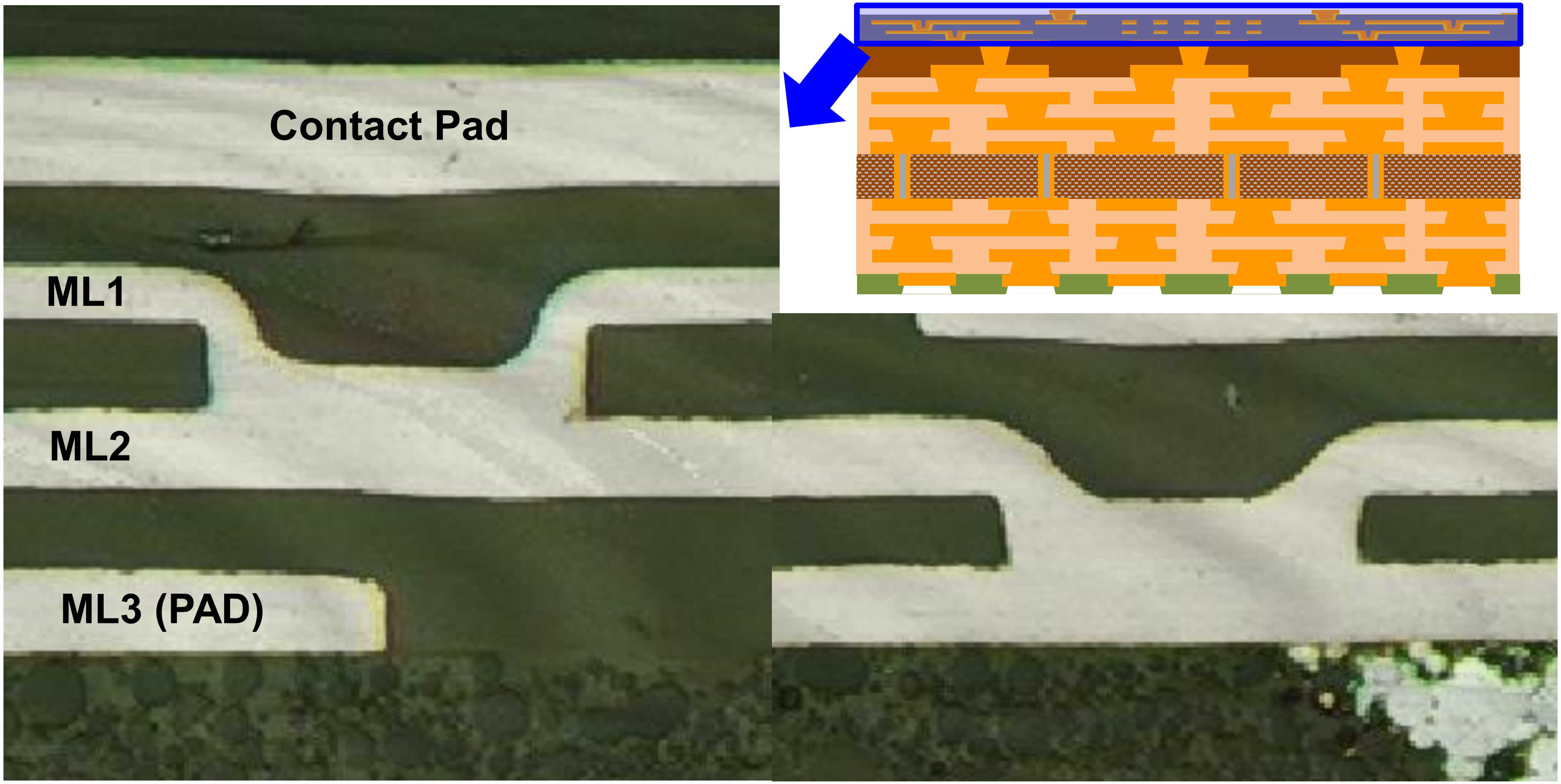




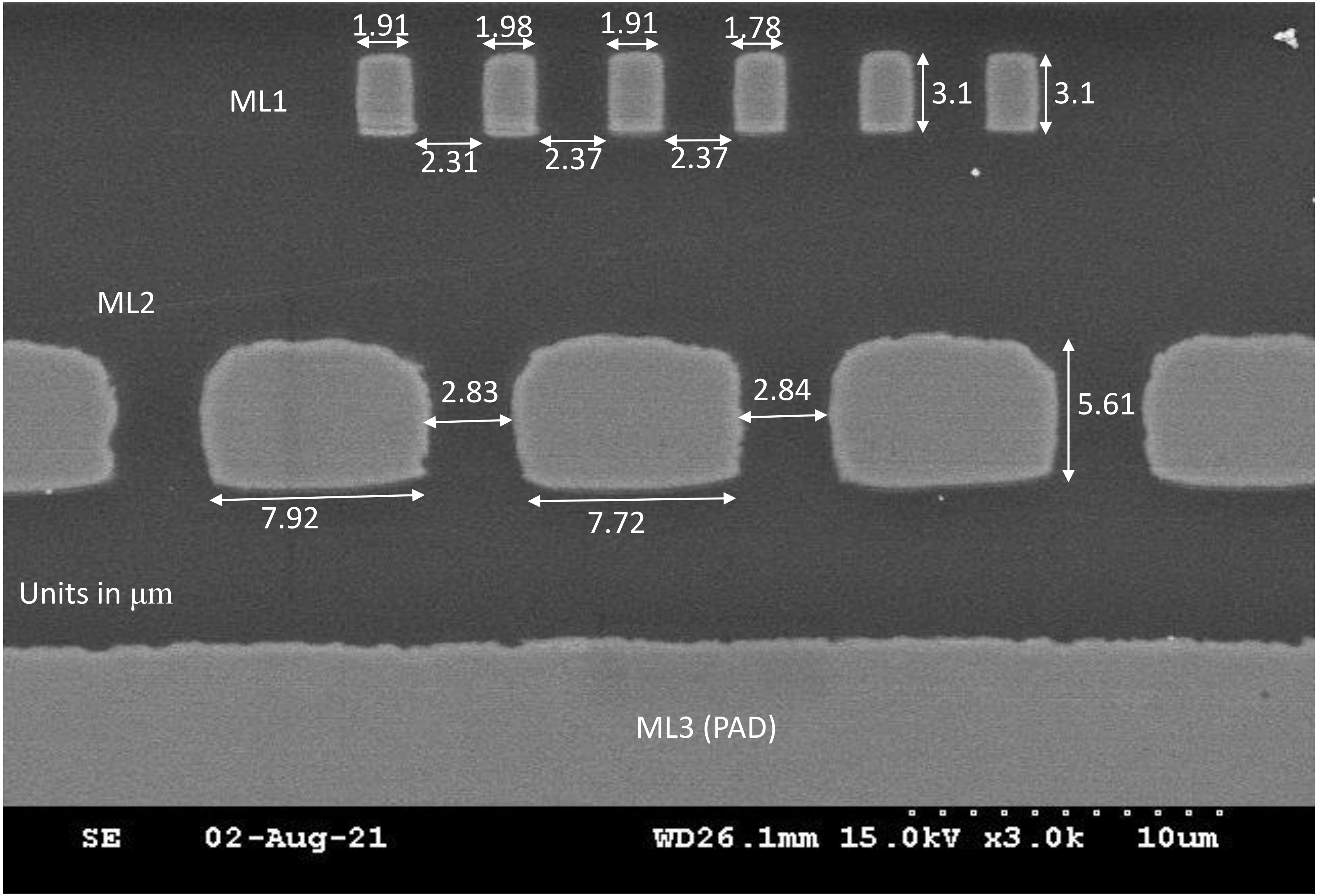




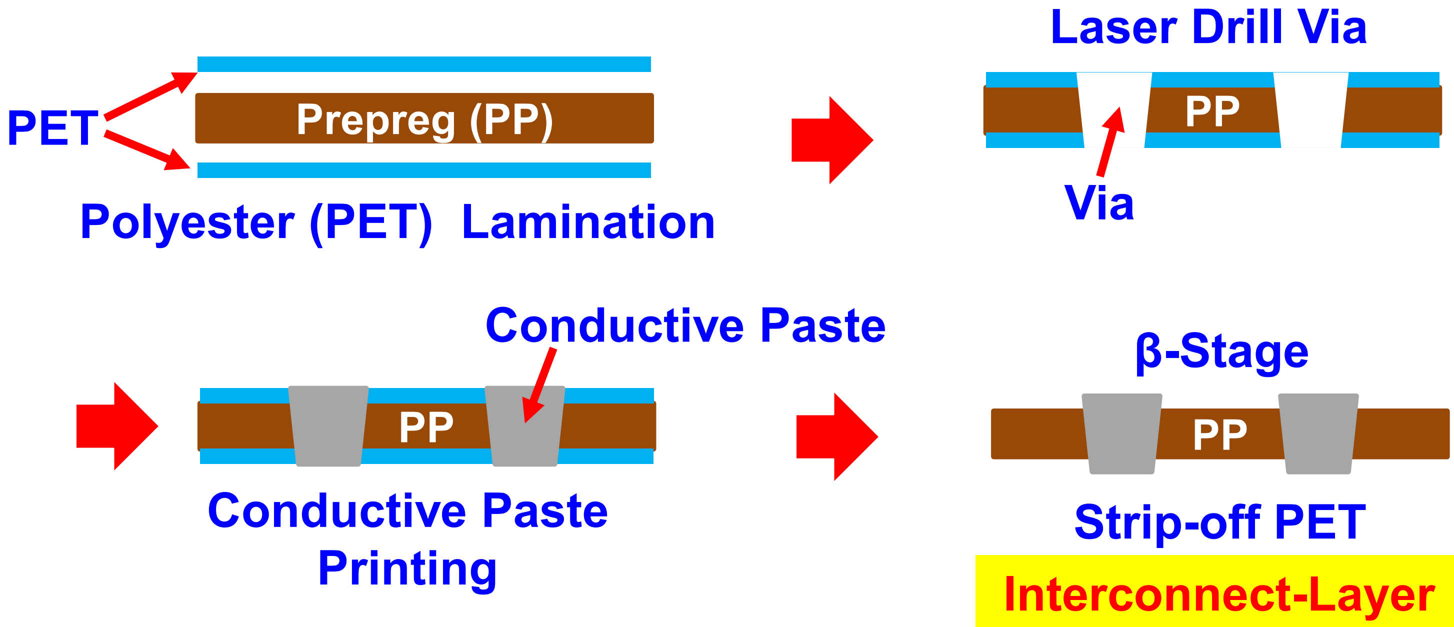
Typical OM image of the Cross Section of the RDL-substrate



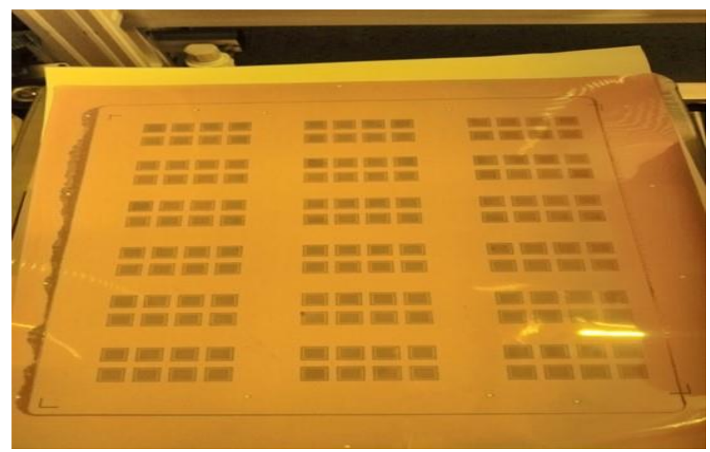
Cross section SEM image of the RDL-substrate



Interconnect-layer (PP and paste are in β-stage)



PP with vias
(no conductive paste)

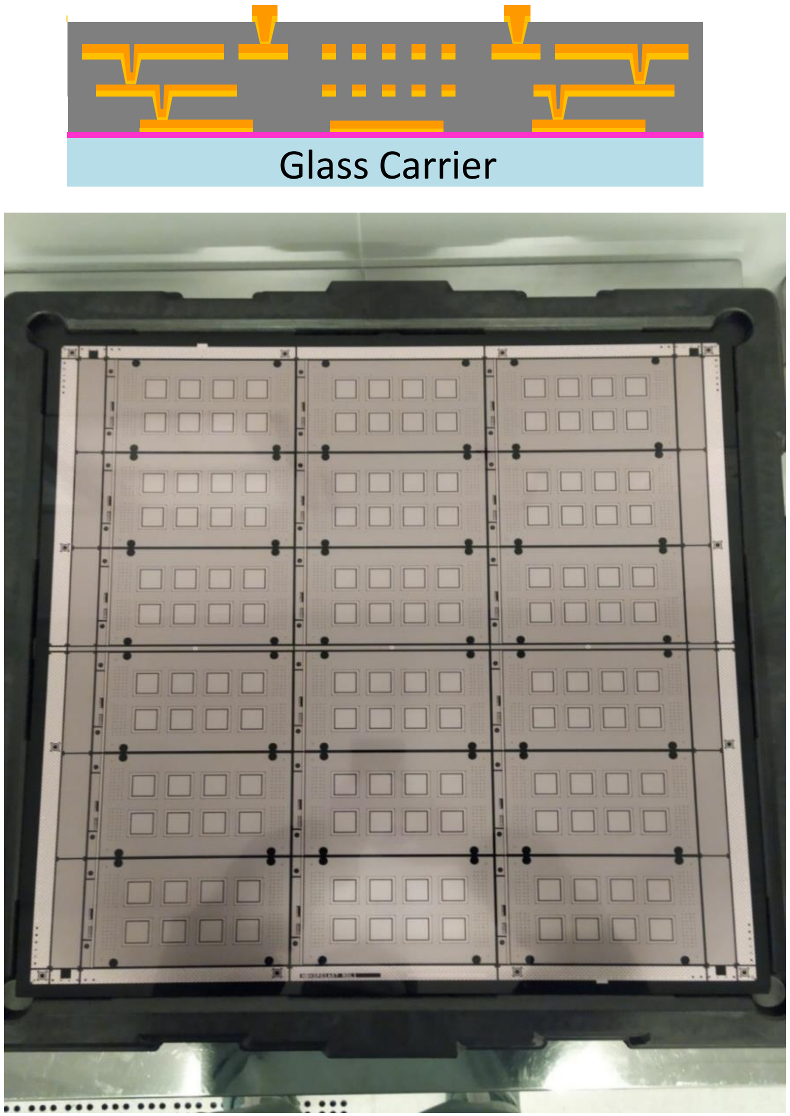


PP with vias
filled with conductive paste

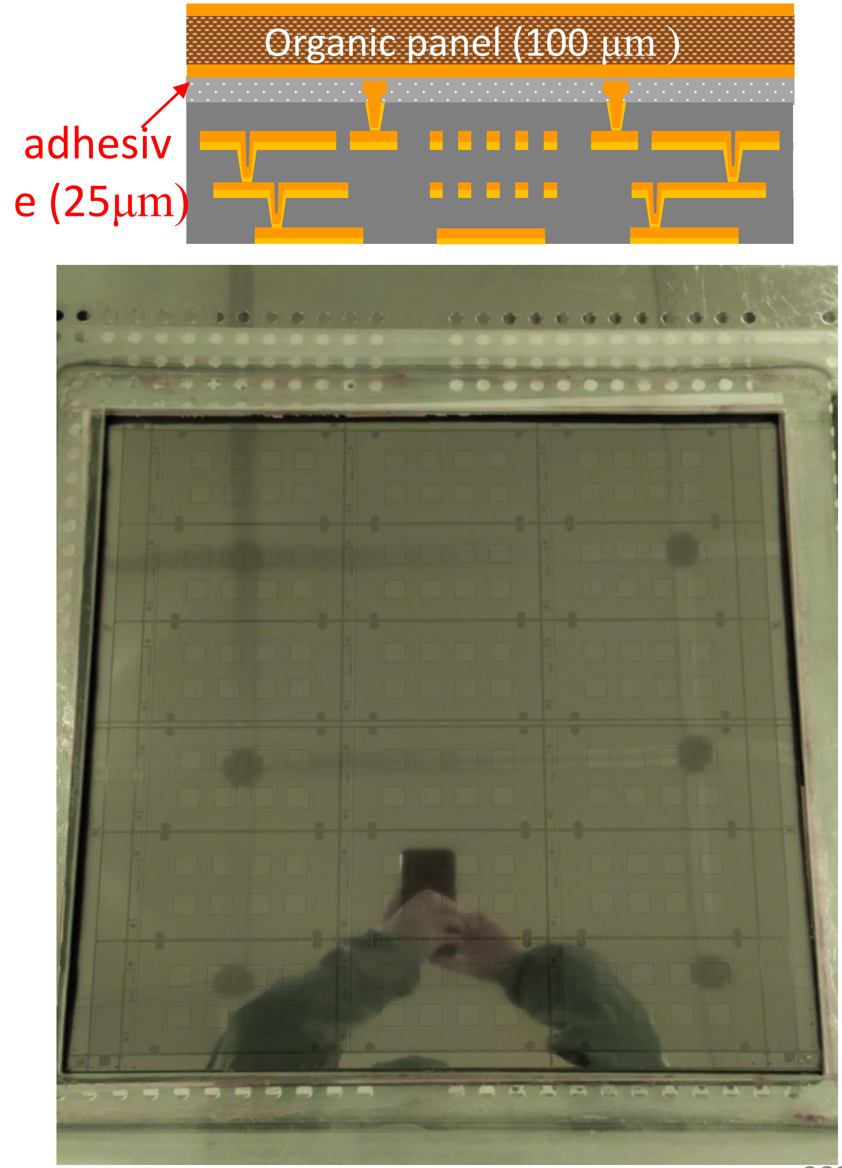
HDI PCB Materials and Specifications

Category	Layer	Material	Item	Diameter/ Width (μm)	Thickness (μm)
HDI	L1	Cu	Pad Dia.	300	22
		PP 1067	Bottom Dia.	100	55
	L2	Cu	Pad Dia.	200/400	25
		PP 1067	Bottom Dia.	250	60
	L3	Cu	Pad Dia.	400	17
		Core	MTH Dia.	250	254
	L4	Cu	Pad Dia.	400	17
		PP 1067	Bottom Dia.	250	55
	L5	Cu	Pad Dia.	400	17
		Core	MTH Dia.	250	254
	L6	Cu	Pad Dia.	400	17
		PP 1067	Bottom Dia.	250	60
	L7	Cu	Pad Dia.	200/400	25
		PP 1067	Bottom Dia.	100	55
	L8	Cu	Pad Dia.	200	22
		SR	Bottom Dia.	600	20
	HDI Total Thickness				975

(a) Glass panel for making the RDL-substrate.
(b) RDL-substrate with organic panel without glass panel.

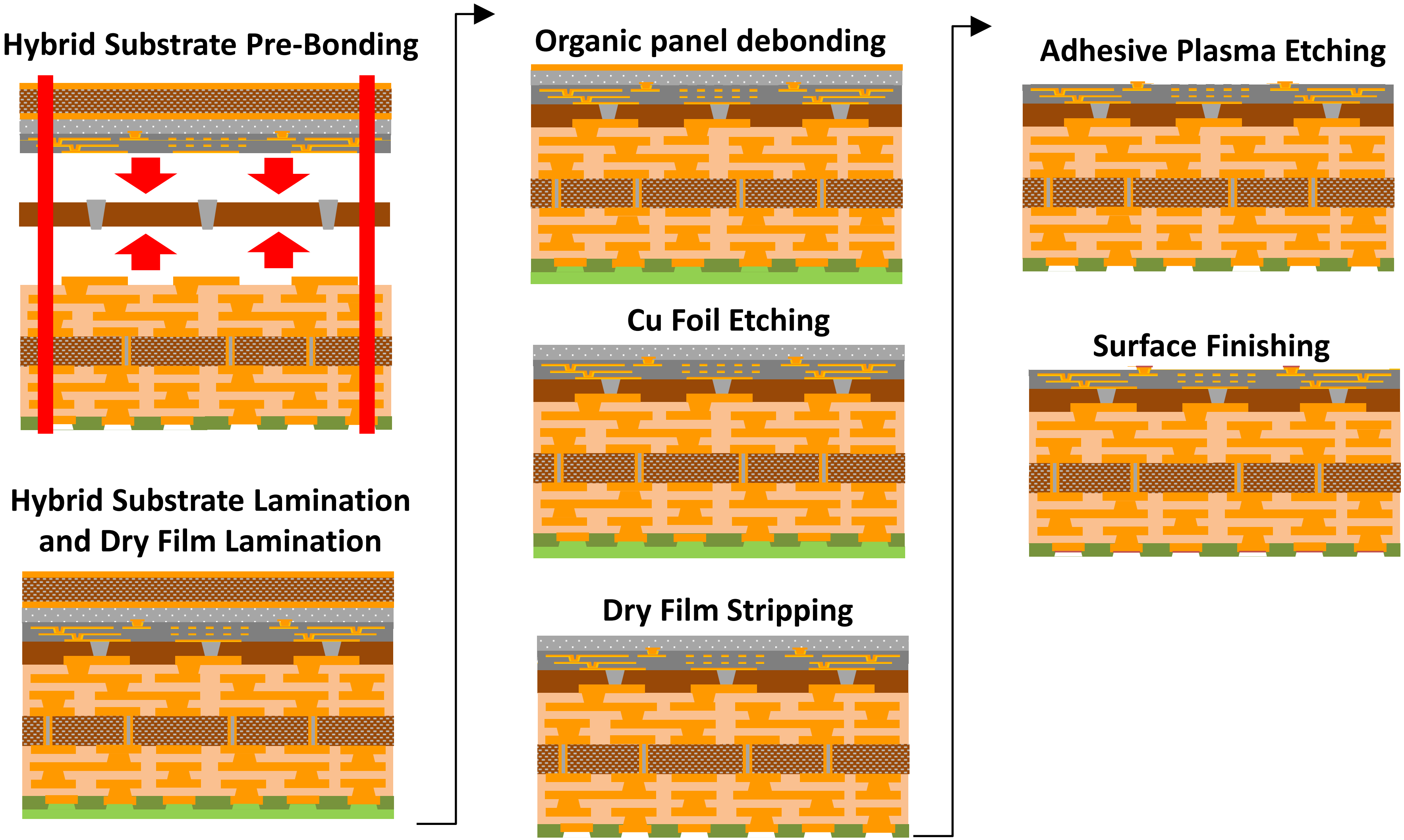


(a)

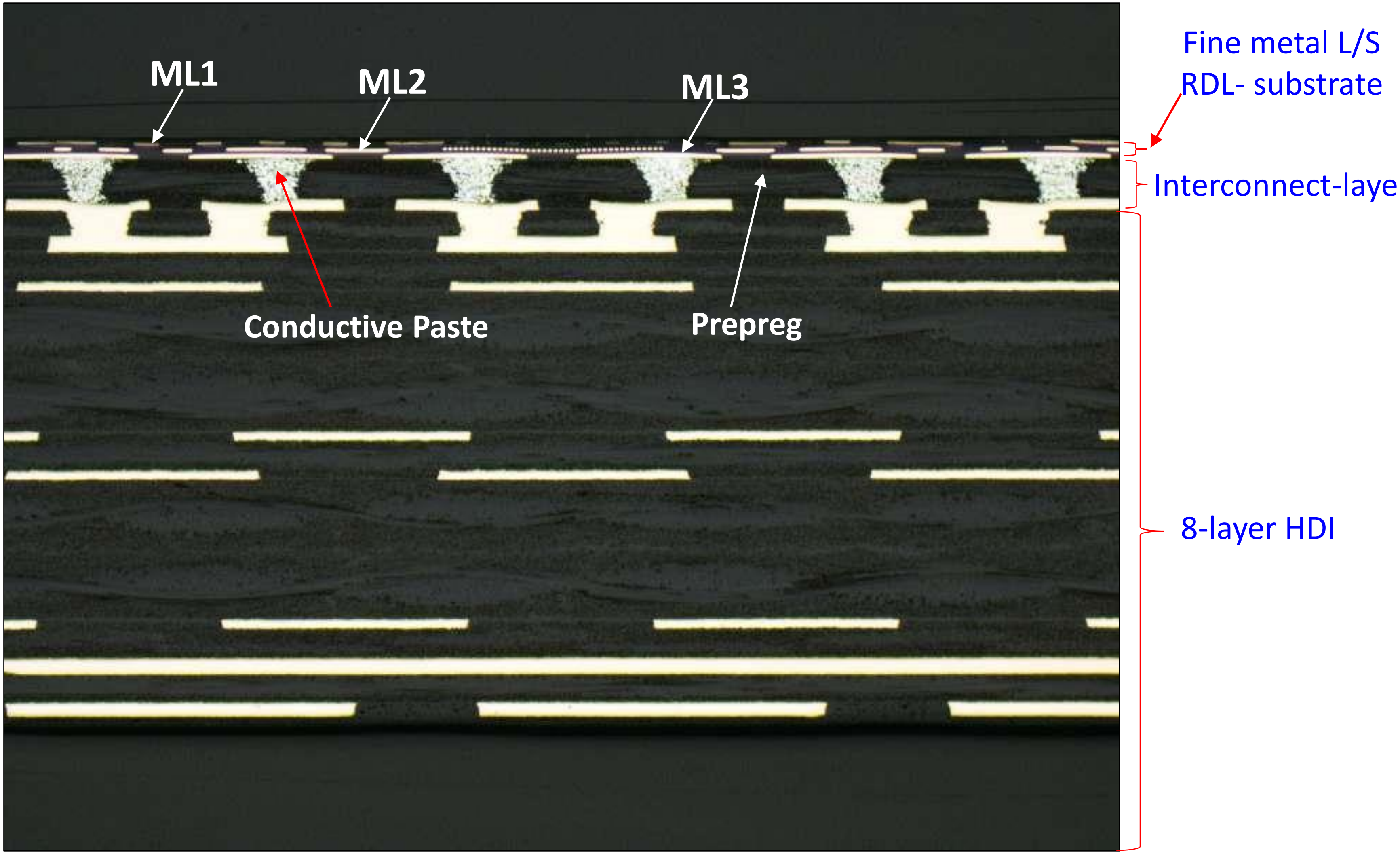


(b)

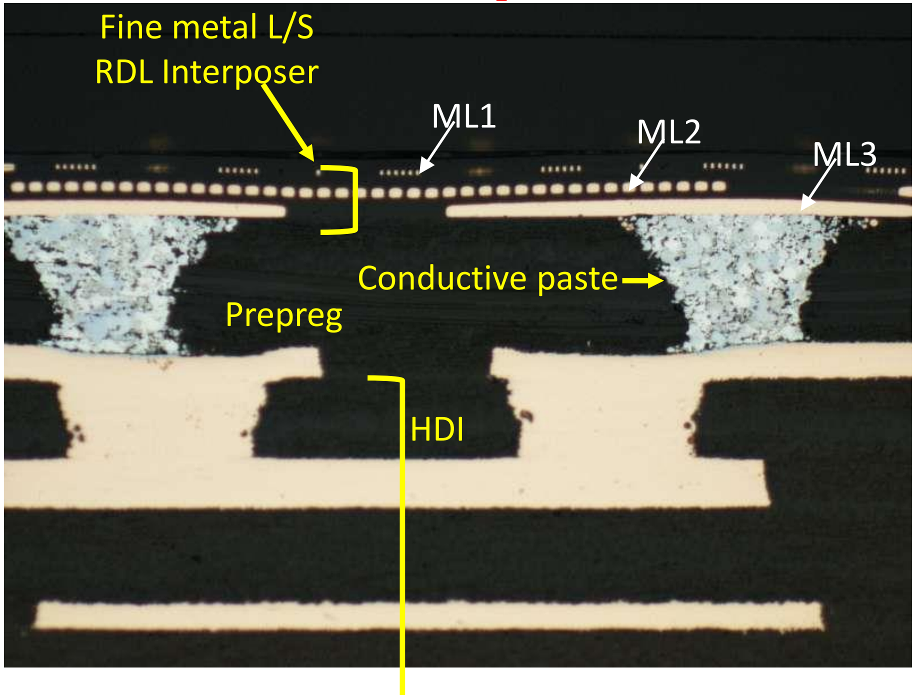
Process steps in making the hybrid substrate

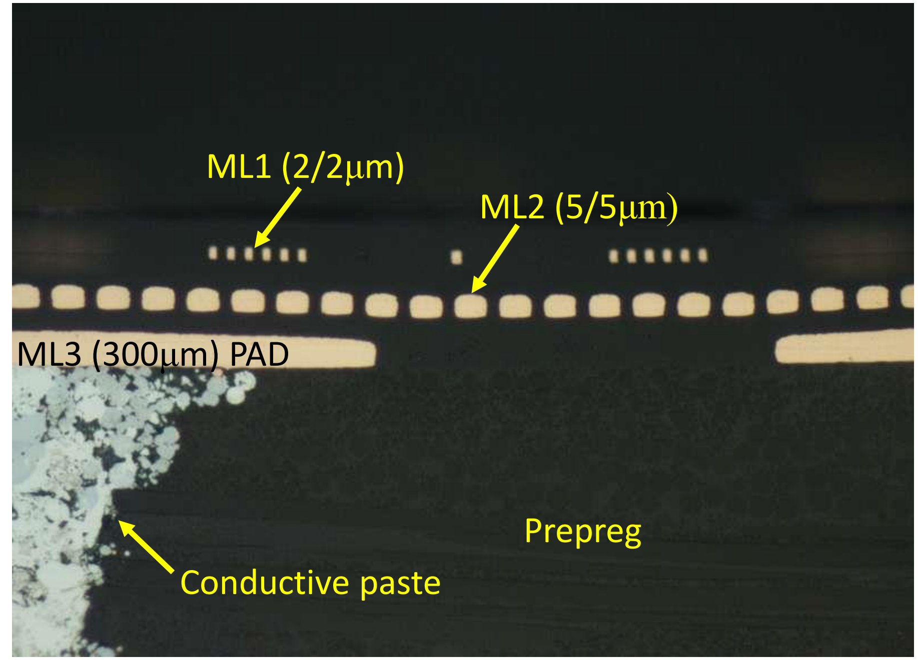


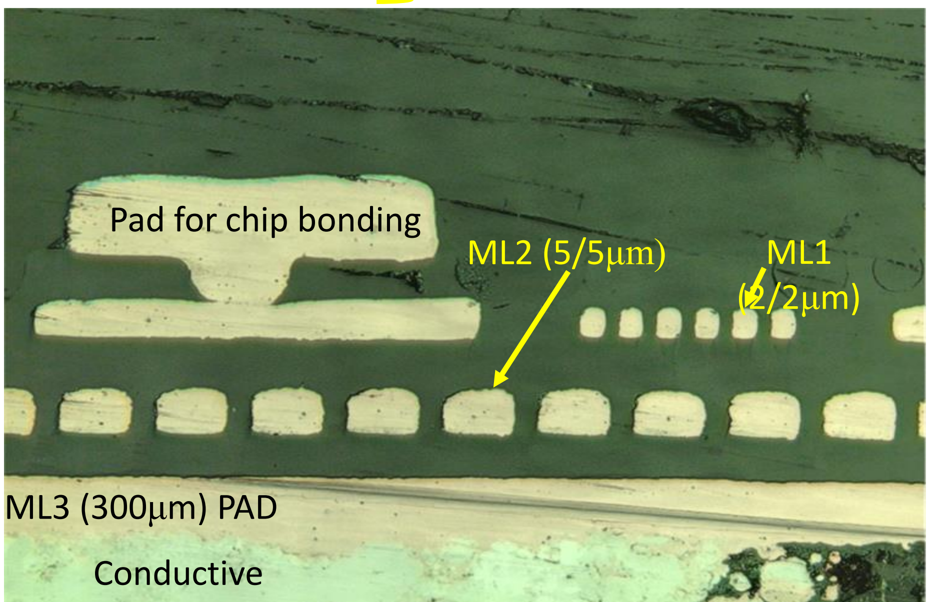
A typical cross section of the hybrid substrate

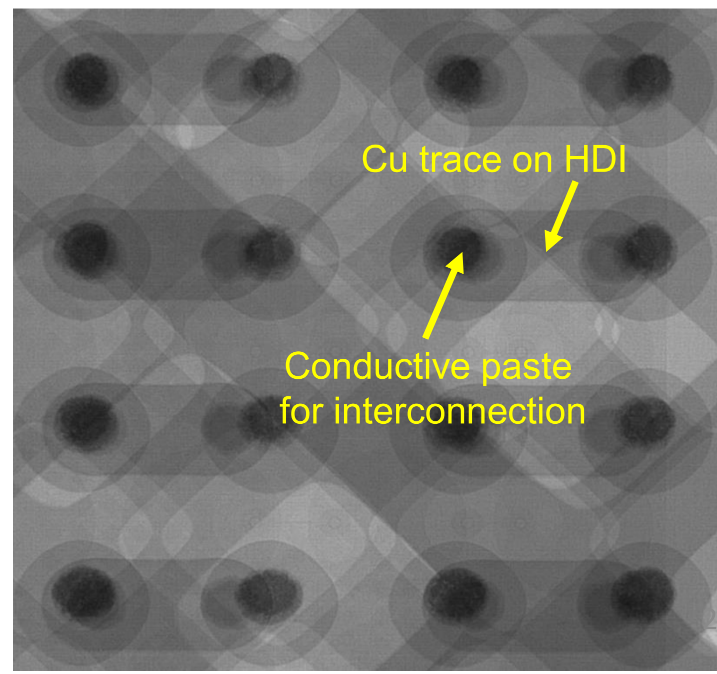


Close-up views of the hybrid substrate

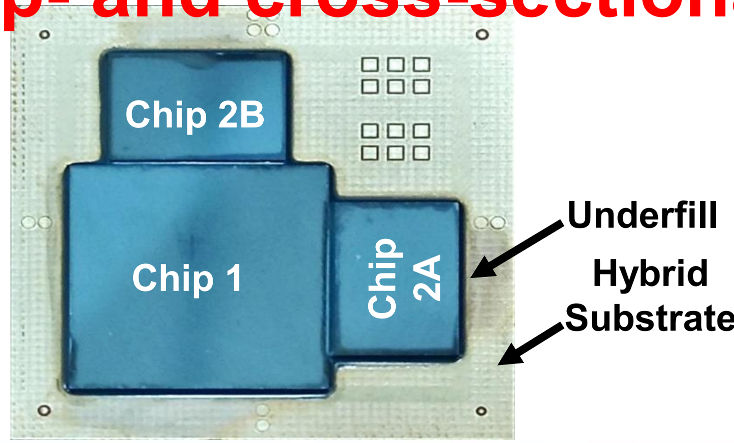


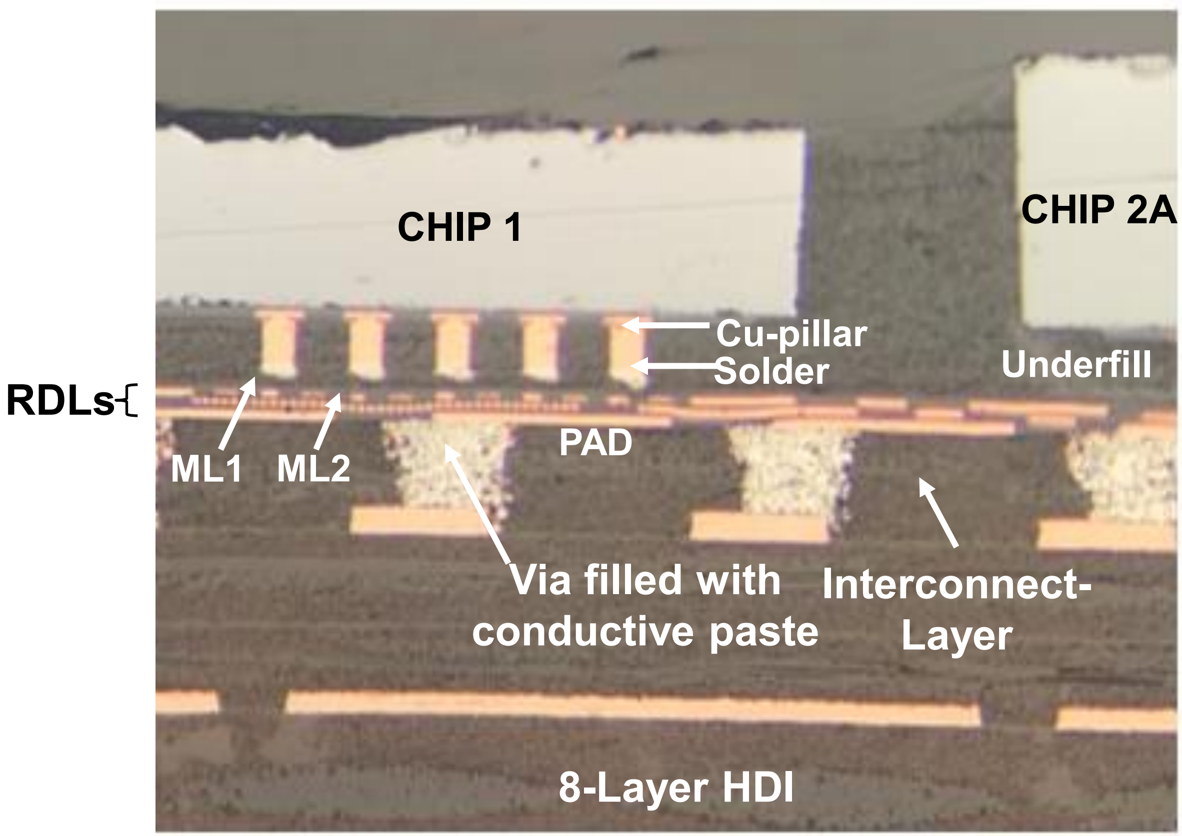




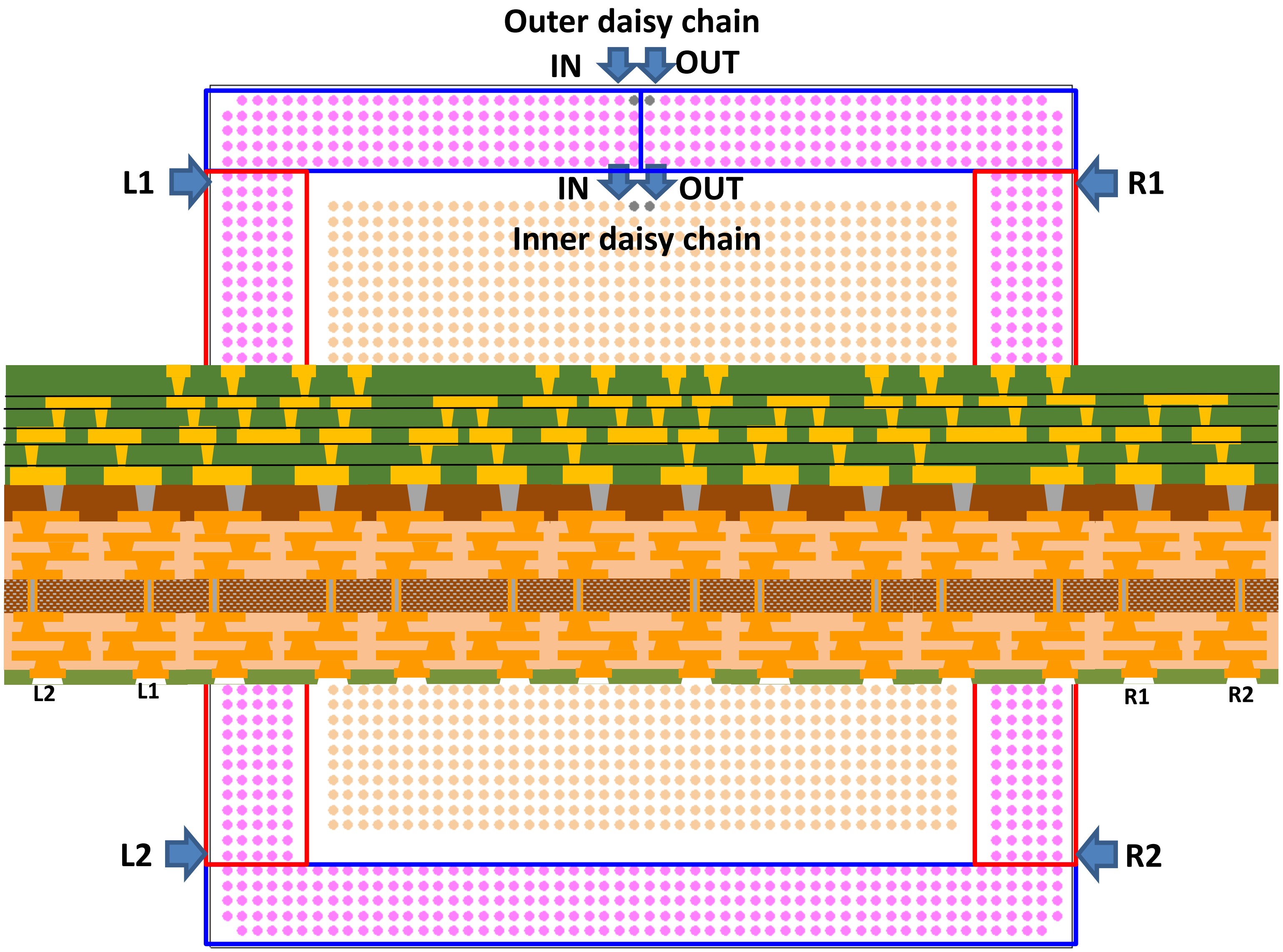


Heterogeneous integration of three chips on the hybrid substrate (top- and cross-sectional views)

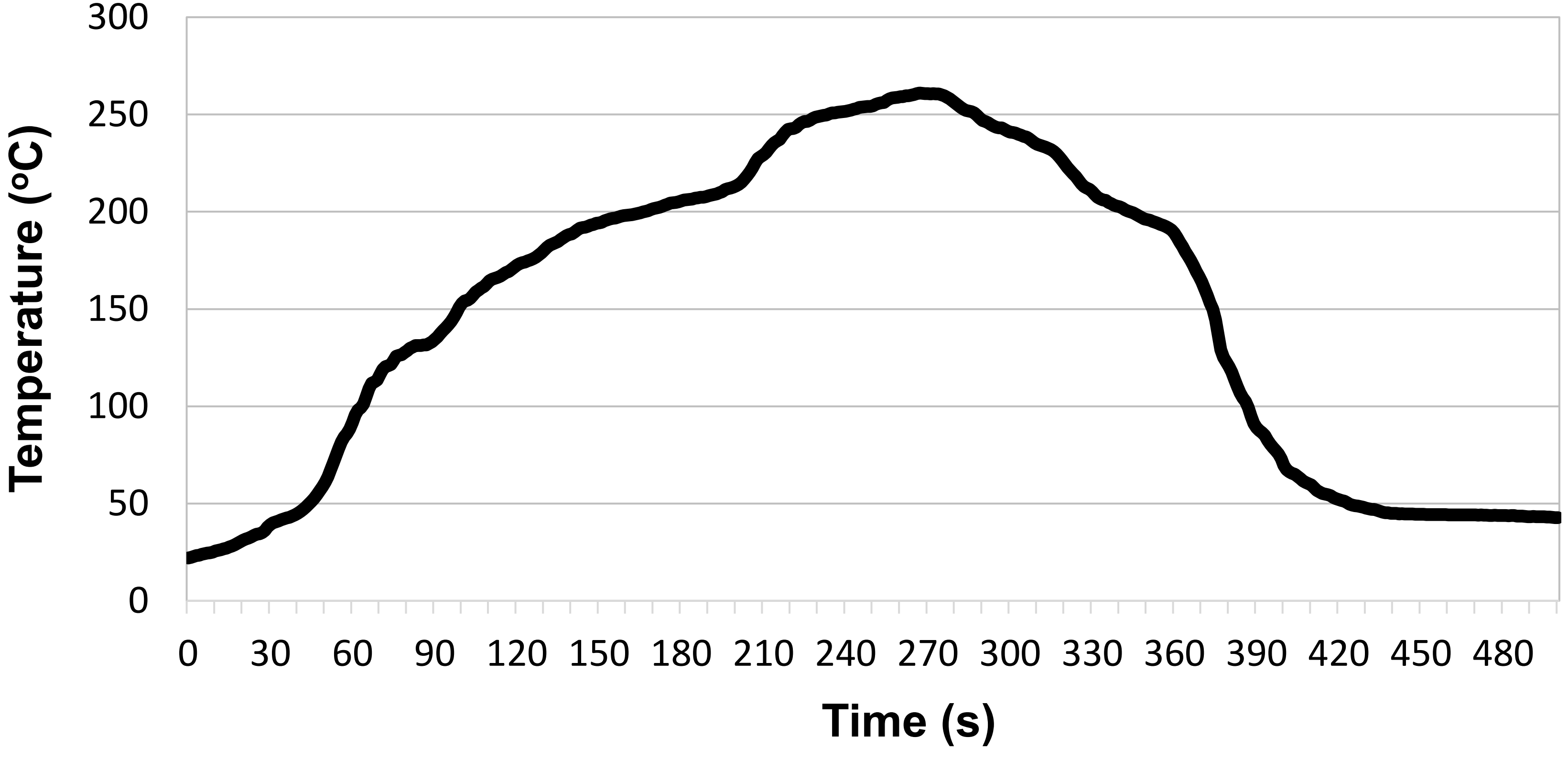




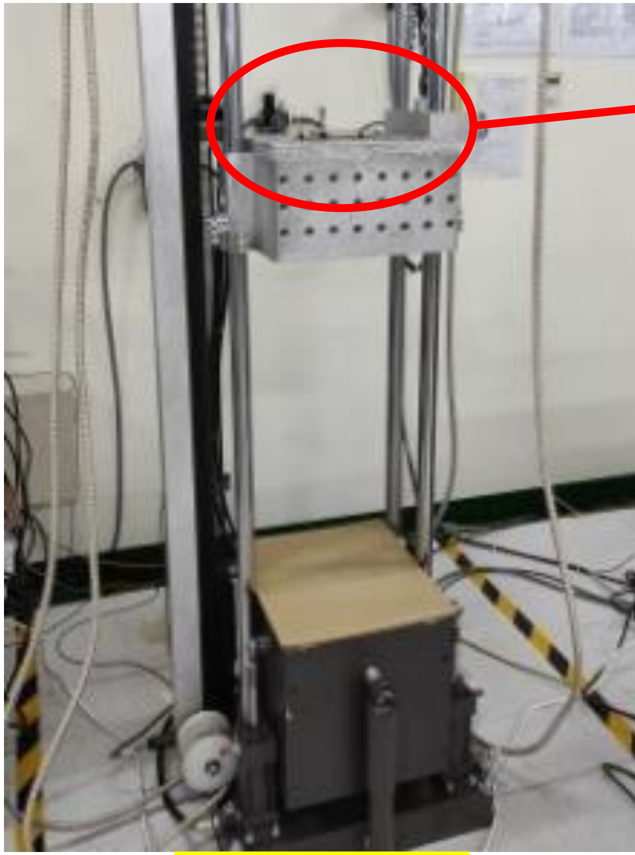
Schematic nets for continuity measurements



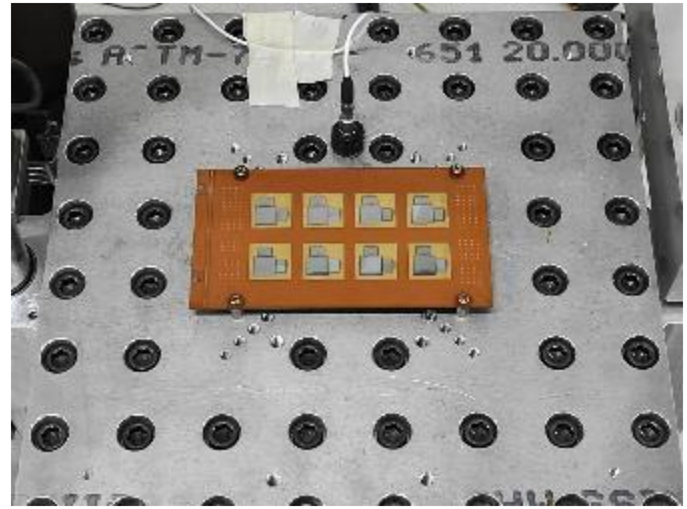
Reflow temperature profile



Drop test set-up and measurement



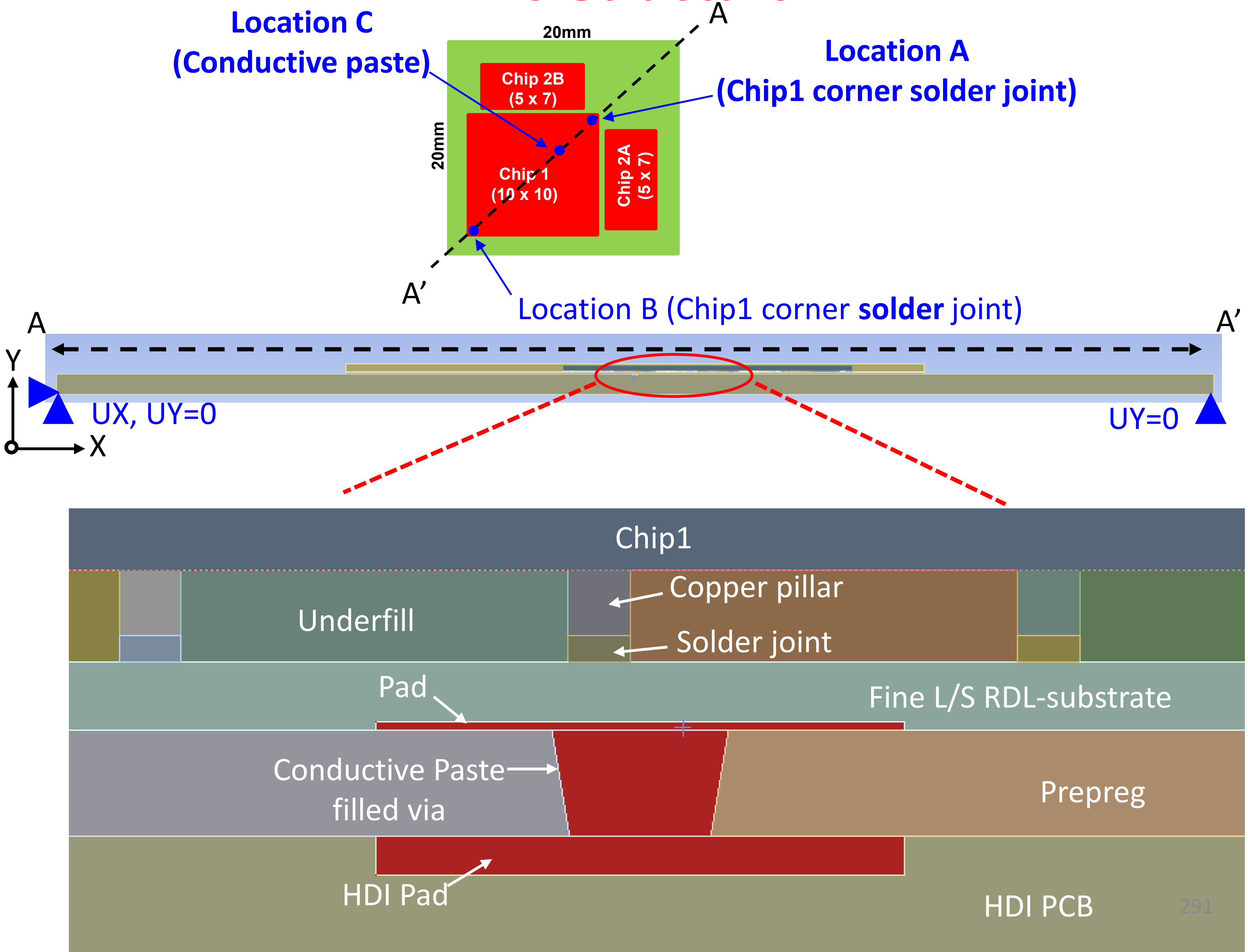
Drop Tower



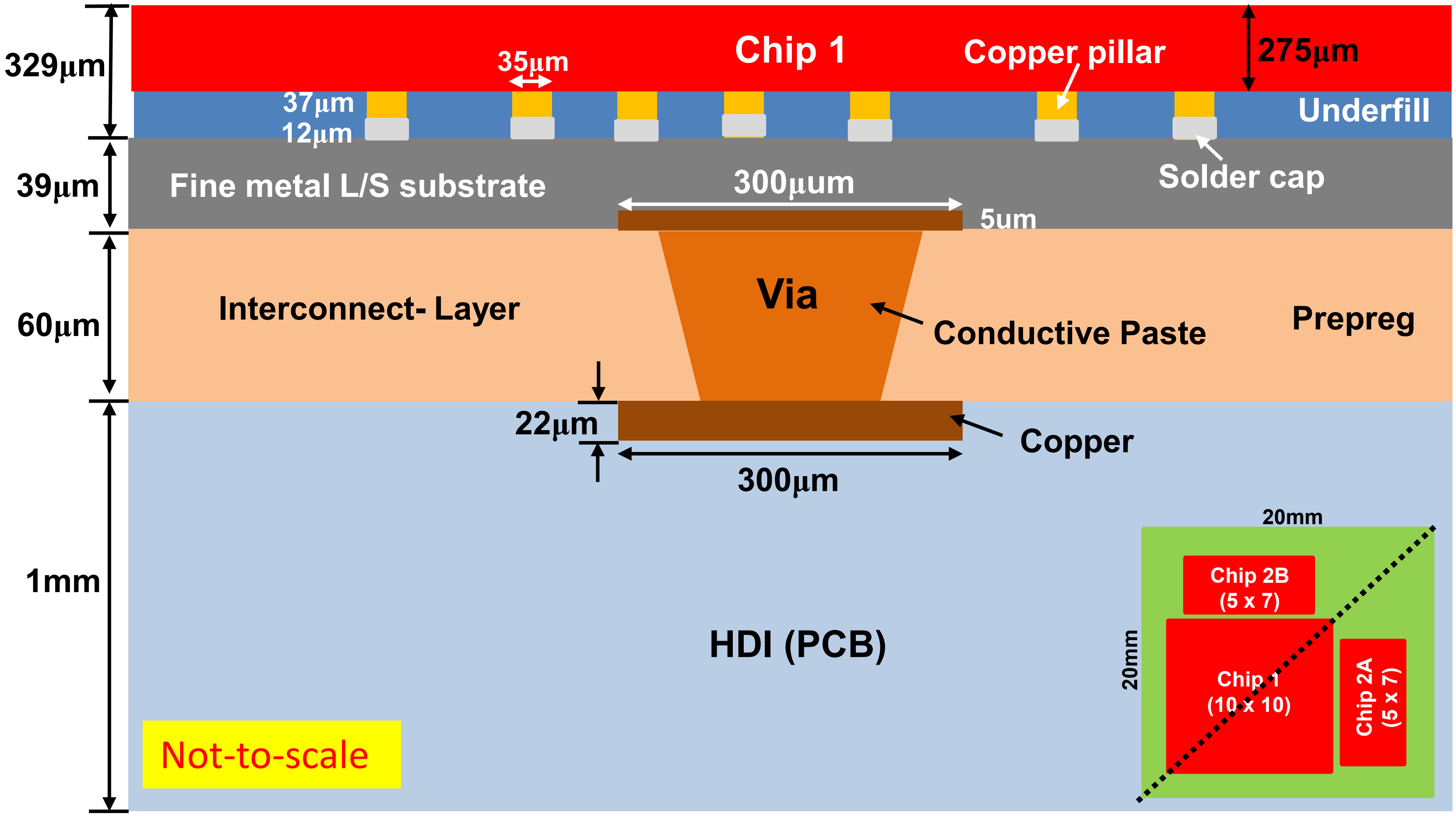
Hybrid Substrate Test Board

4-wire Measurement

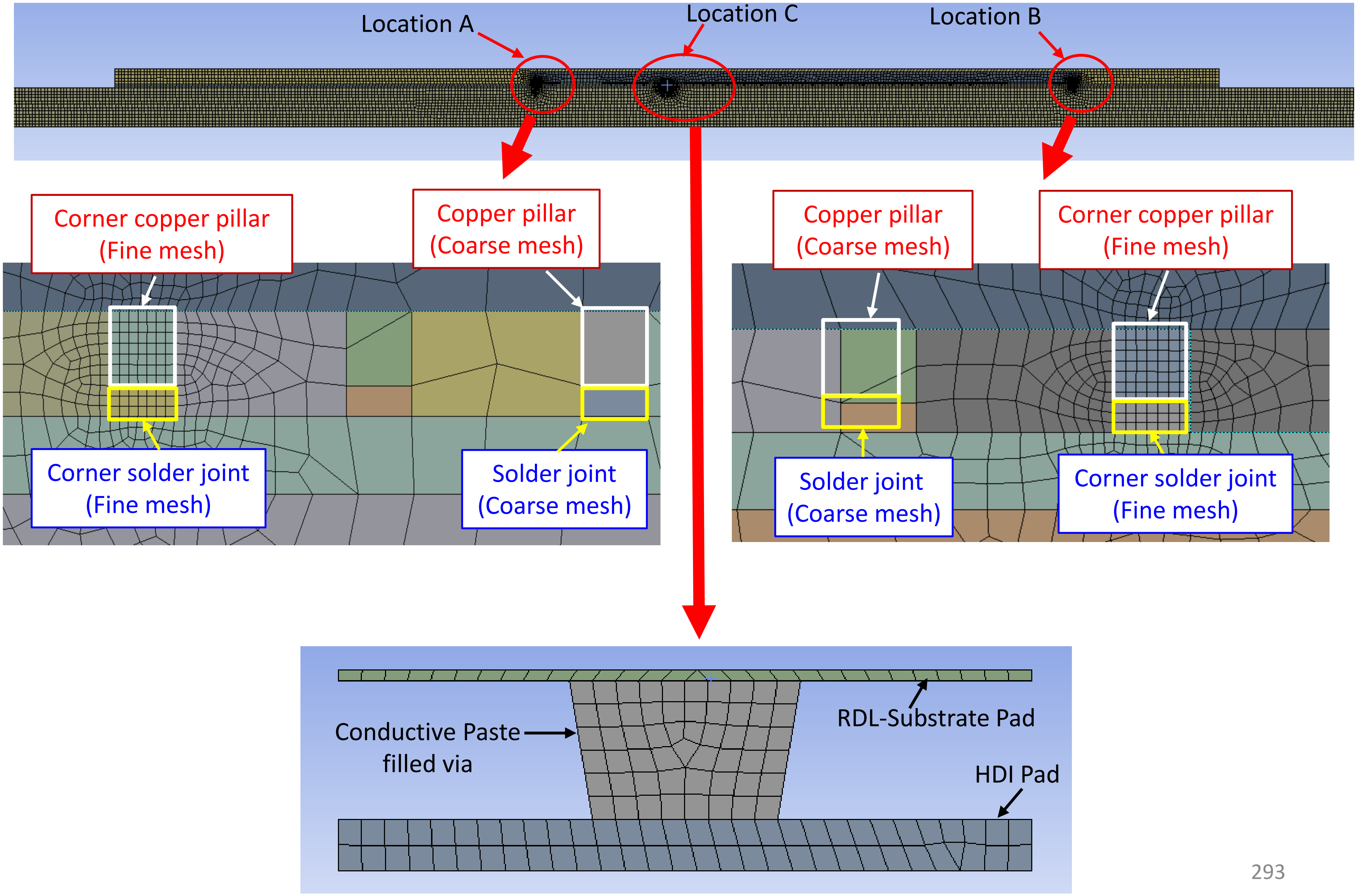
The Structure



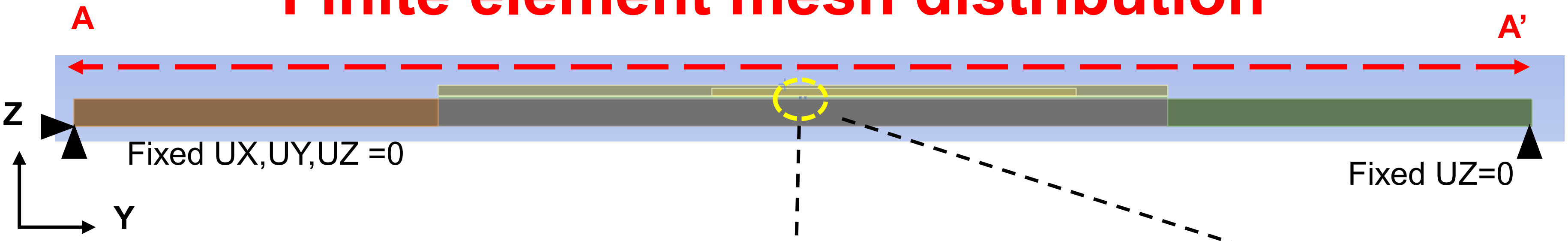
Structural elements for finite element modeling

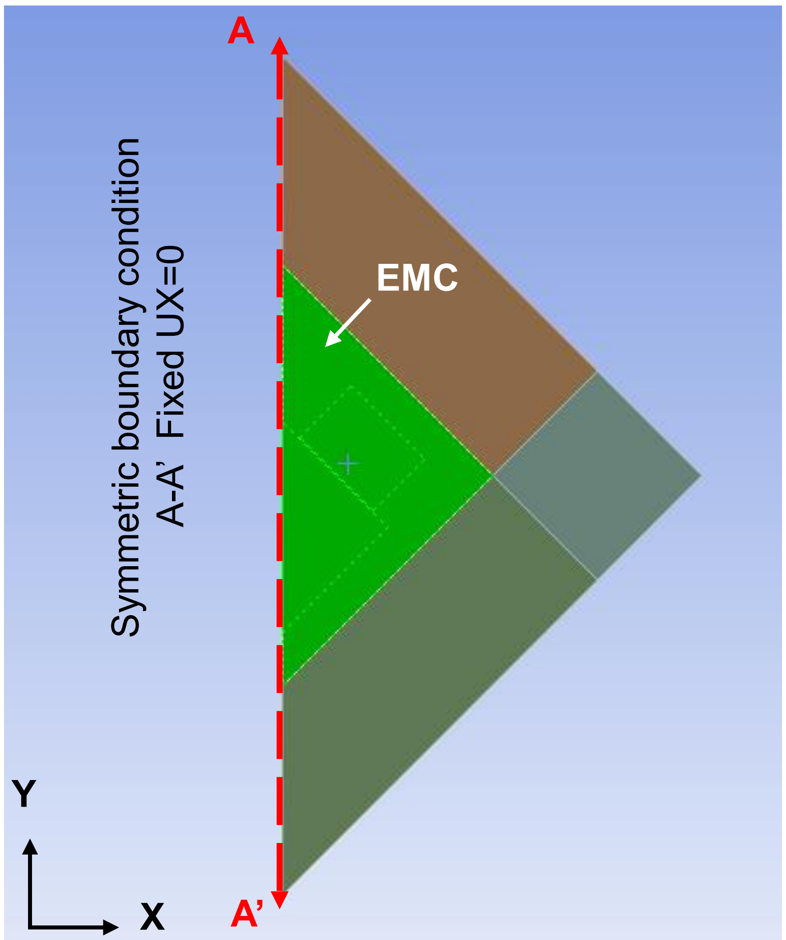


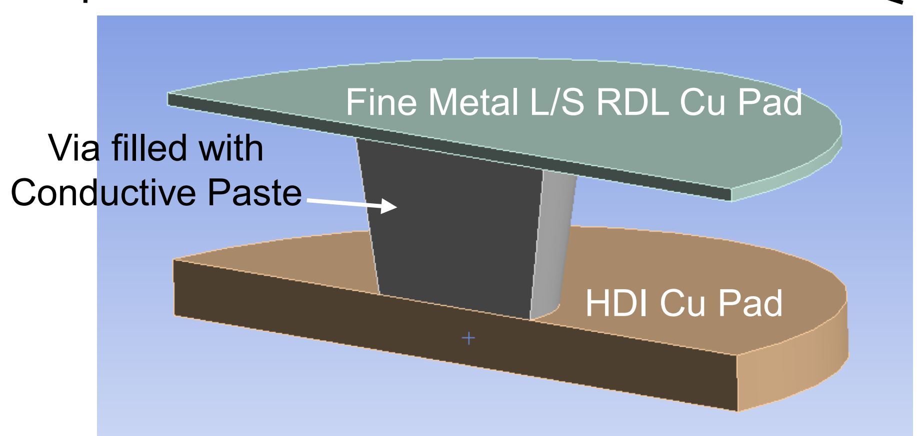
Finite element mesh distribution

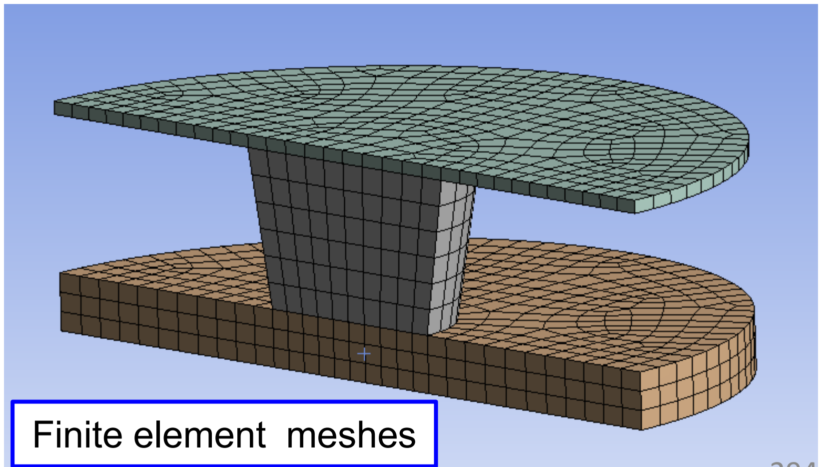


Finite element mesh distribution

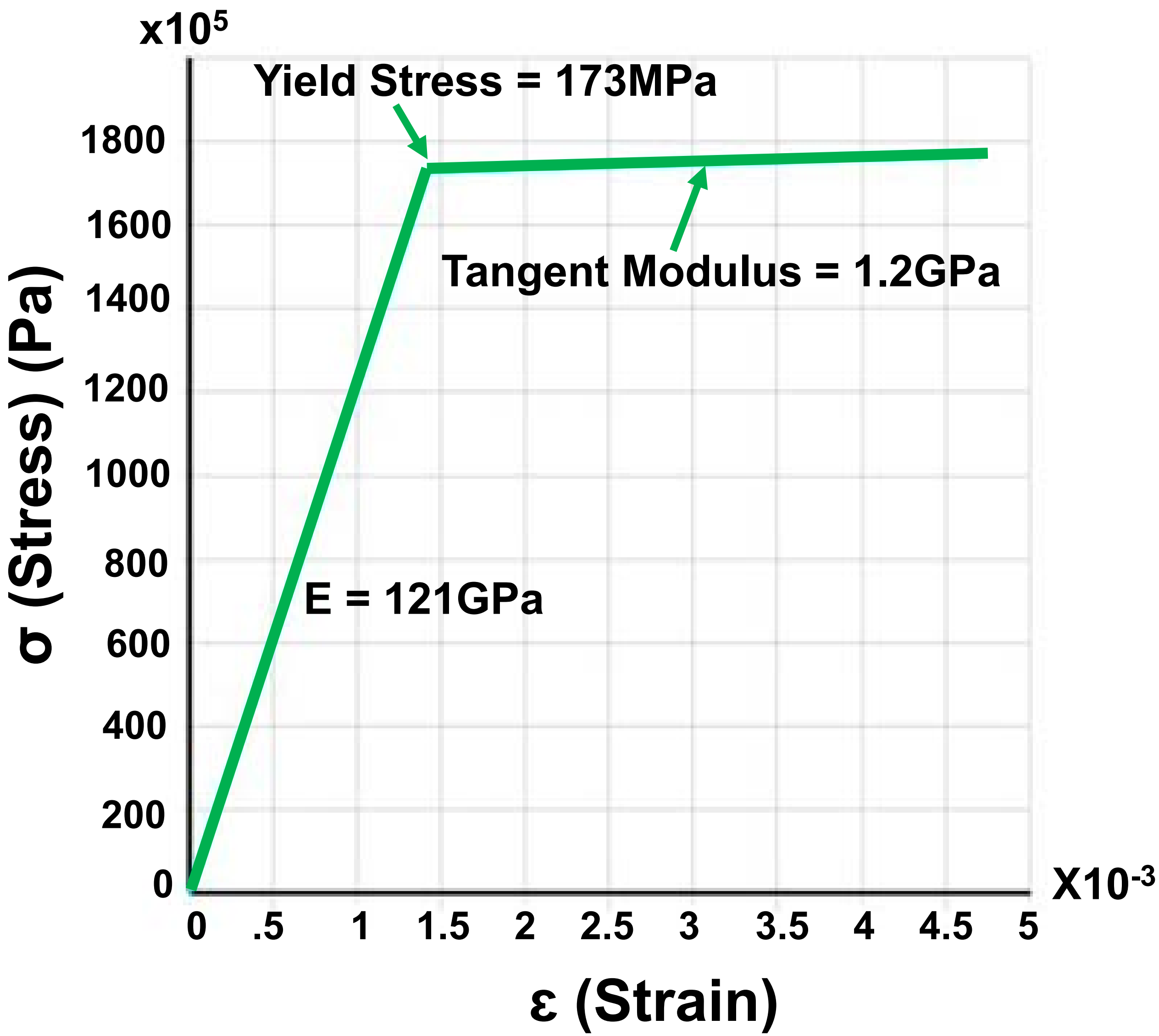








Stress-strain relation for electroplated Cu



- Consider copper Bauschinger effect, Kinematic hardening is used in this material.

MATERIAL PROPERTIES

Materials	CTE ($10^{-6}/^oC$)	Young's Modulus (GPa)	Poison's Ratio
Copper	16.3	121	0.34
HDI PCB	$\alpha_x = \alpha_y = 18$ $\alpha_z = 70$	$E_x = E_y = 22$ $E_z = 10$	0.28
Silicon (Chip)	2.8	131	0.278
EMC	10 (< 150°C)	19	0.25
Solder	21 + 0.017T	49 – 0.07T	0.3
RDL Substrate	27.9	47.8	0.3
Conductive Paste	19.01	20.33	0.3
Prepreg (Interconnect-layer)	15	26	0.39
Underfill	50	4.5	0.35

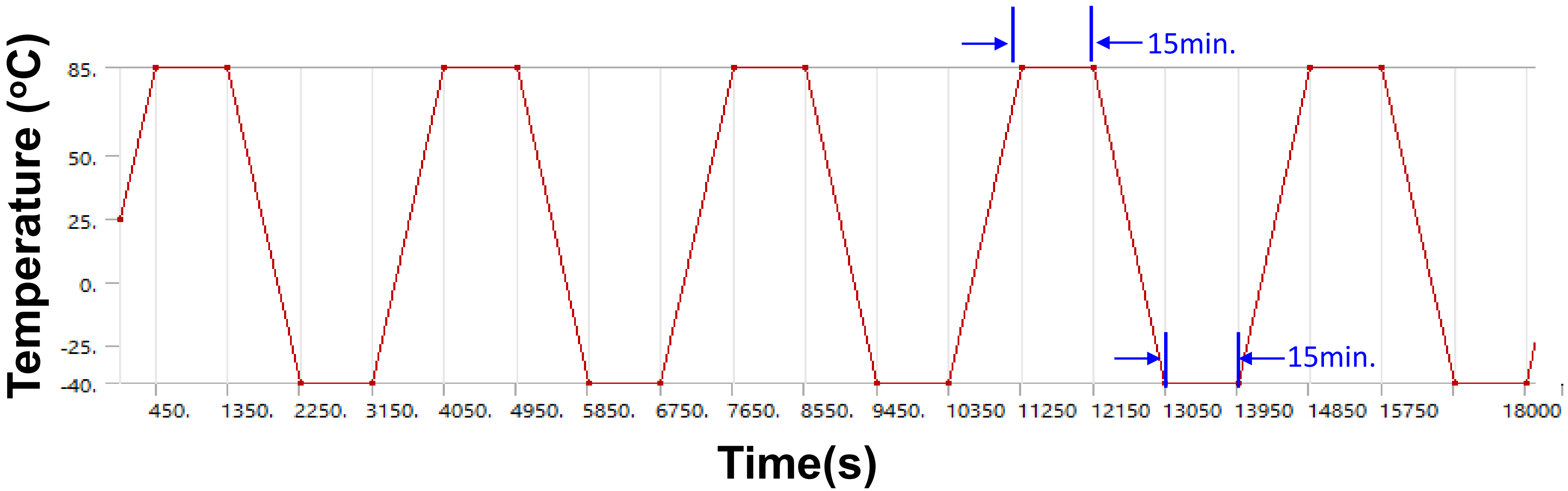
where *T* is in Celsius

The constitutive equation for solder is:

$$\frac{d\varepsilon}{dt} = 500000[\sinh(0.01\sigma)]^5 \exp\left(-\frac{5800}{T}\right)$$

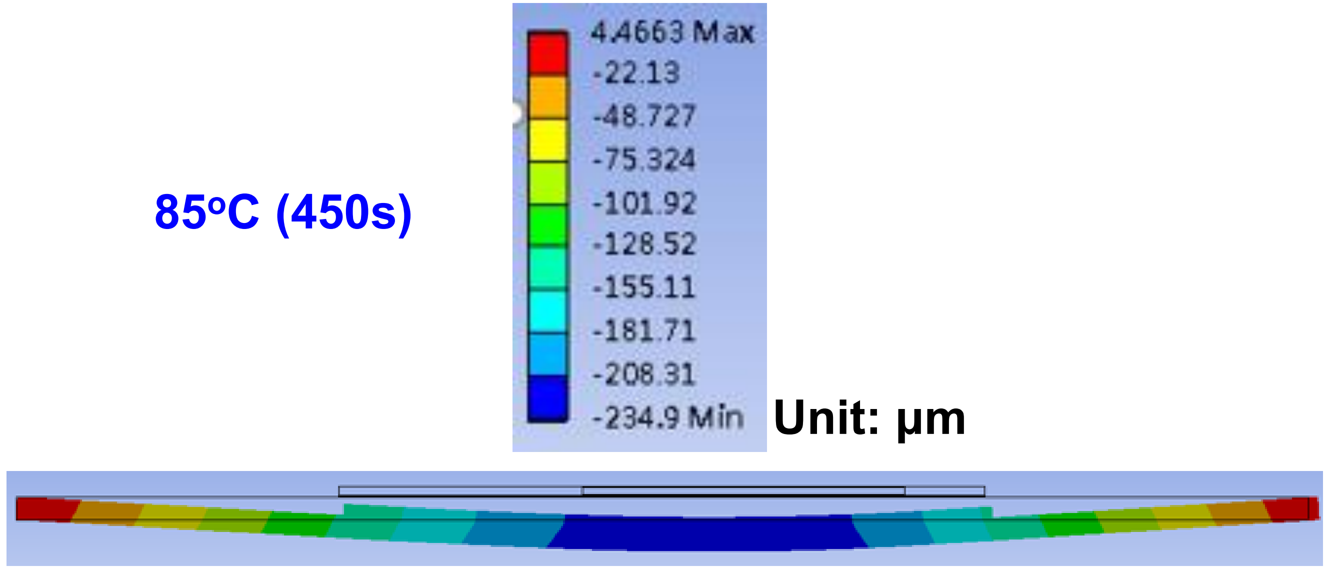
where *T* is in Kevin and *σ* is in MPa.

Temperature boundary condition for simulation

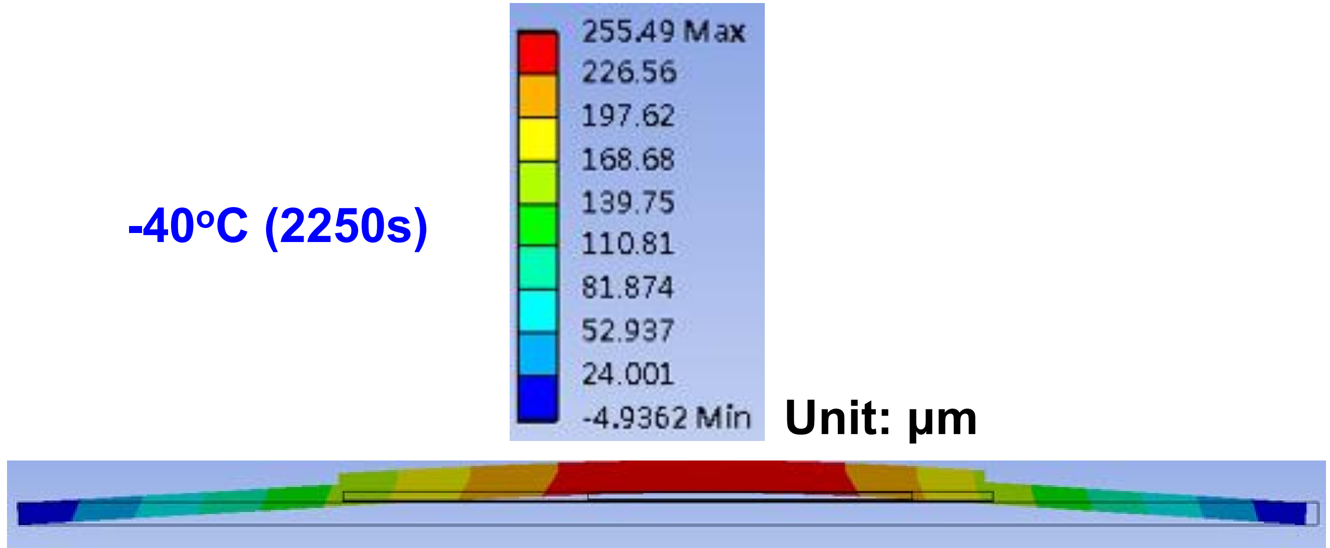


Structural deformation during the first thermal cycle. (a) At 85 ◦C (450 s). (b) At −40 ◦C (2250 s)

(a) 85°C (450s)

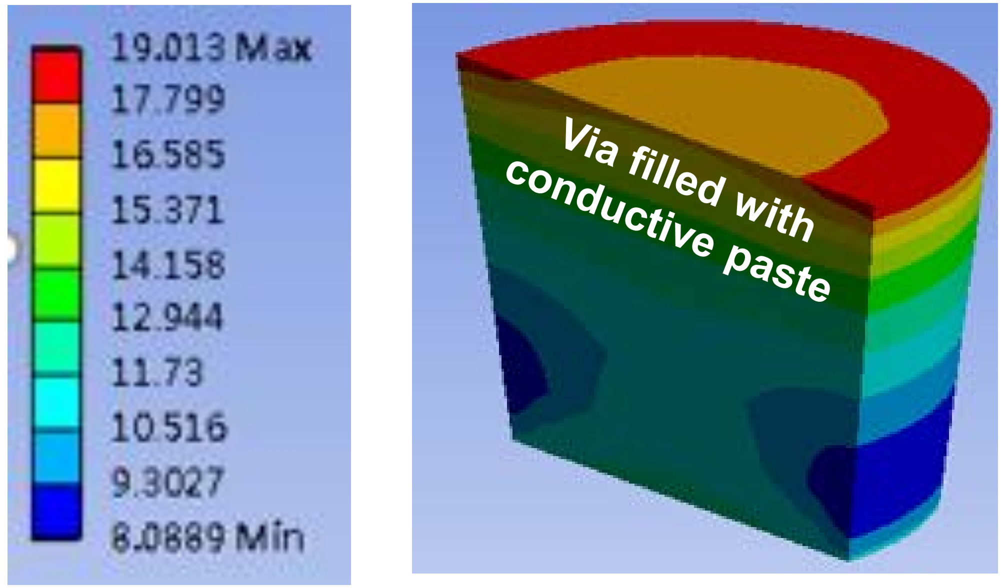


(b) -40°C (2250s)

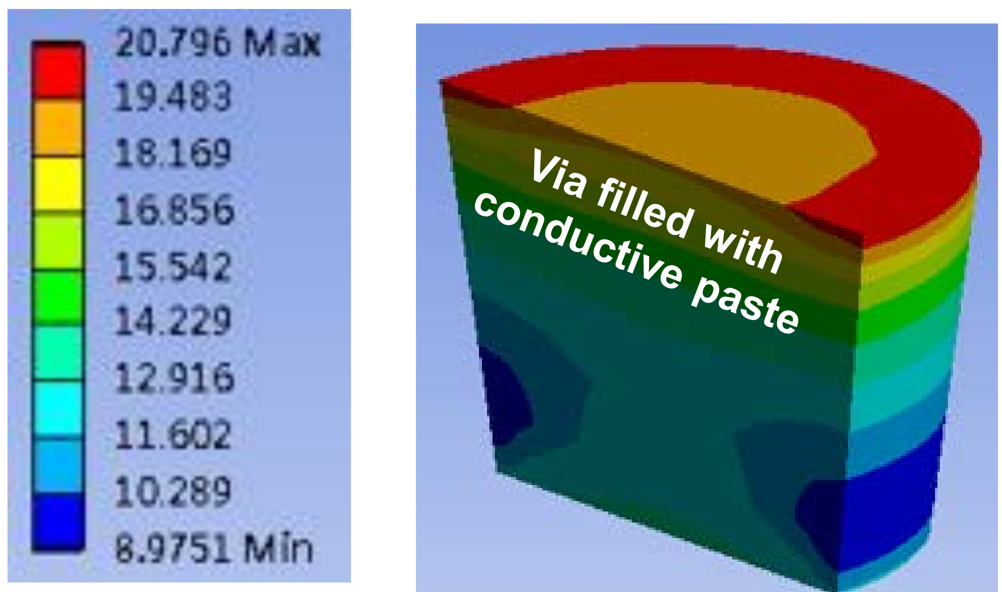


Von Mises stress acting at the via filled with conductive paste. (a) 85 ◦C (450 s). (b) −40 ◦C (2250 s)

(a) 85°C (450s)

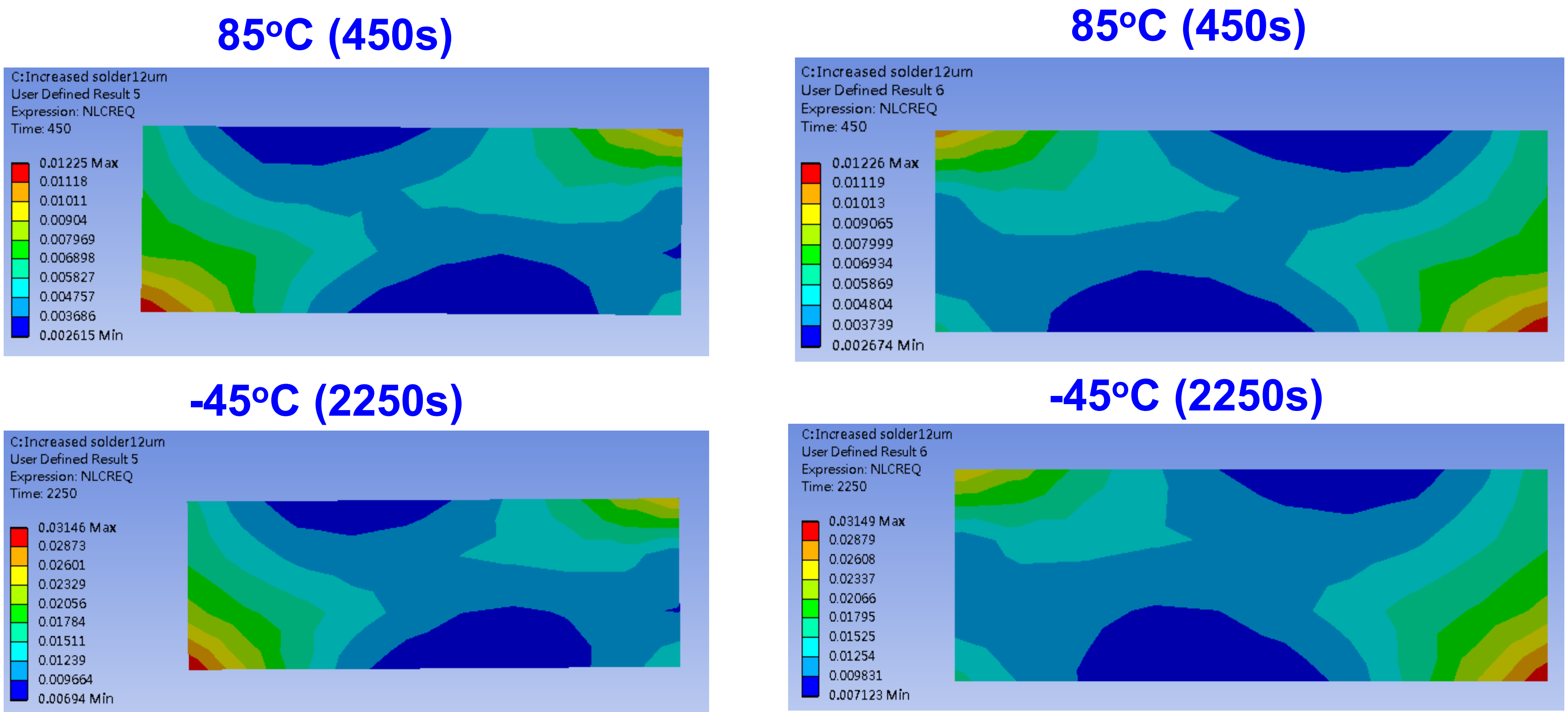


(b) -40°C (2250s)



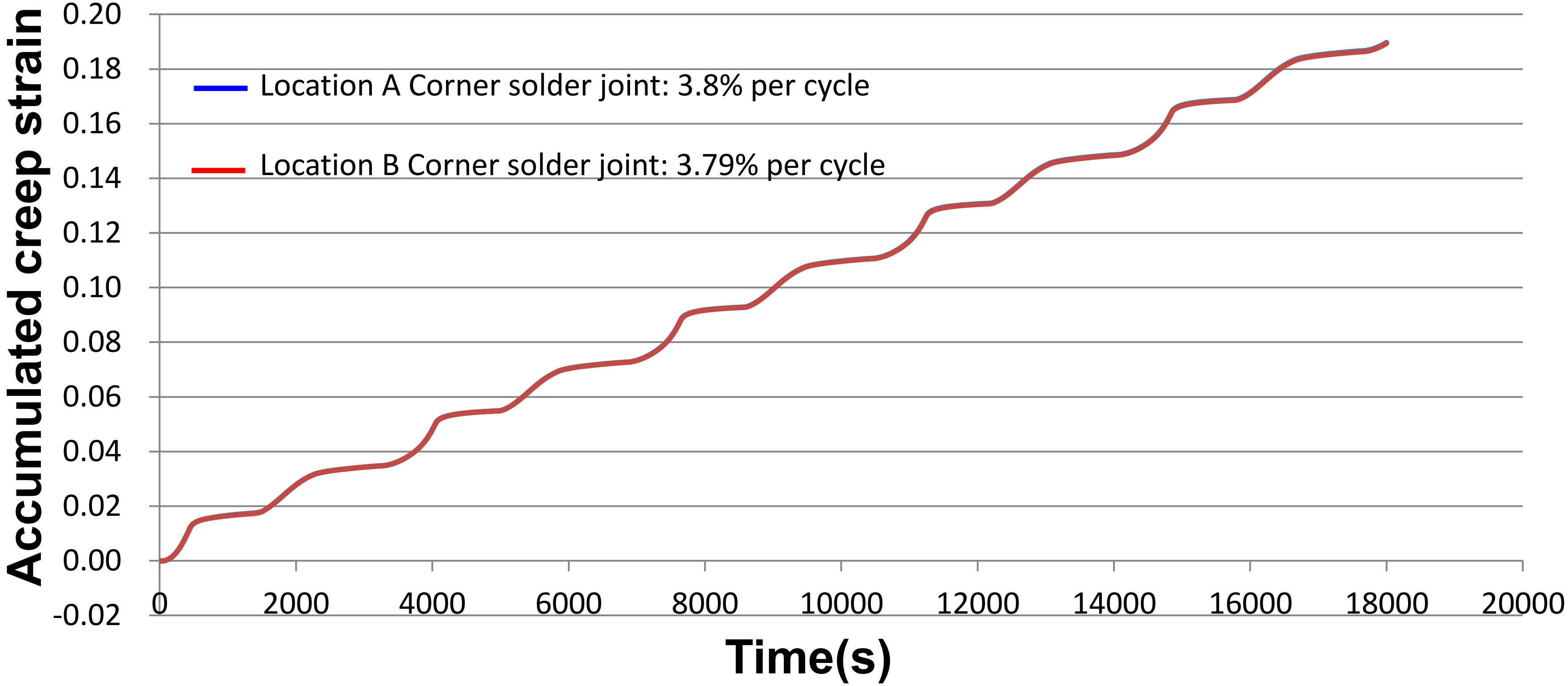
Units: MPa

Accumulated creep strain at solder joint A during the first thermal cycle.
(a) At 85 ◦C (450 s). (b) At −40 ◦C (2250 s)



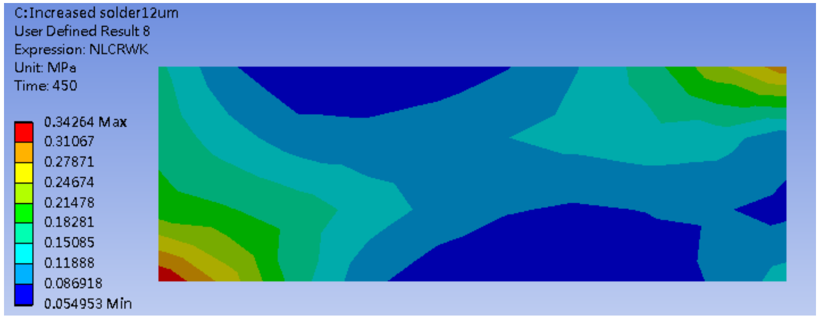
(a) (b)

Accumulated creep strain time-history at solder joints A and B



Creep strain energy density at solder joint A during the first thermal cycle. (a) At 85 ◦C (450 s). (b) At −40 ◦C (2250 s).

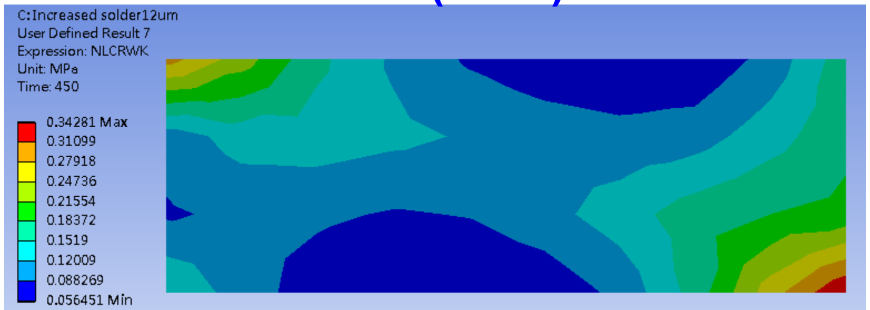
85oC (450s)



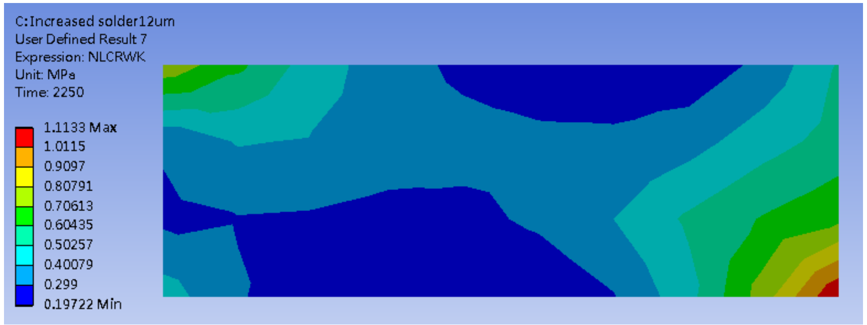
-45oC (2250s)

(a)

85oC (450s)

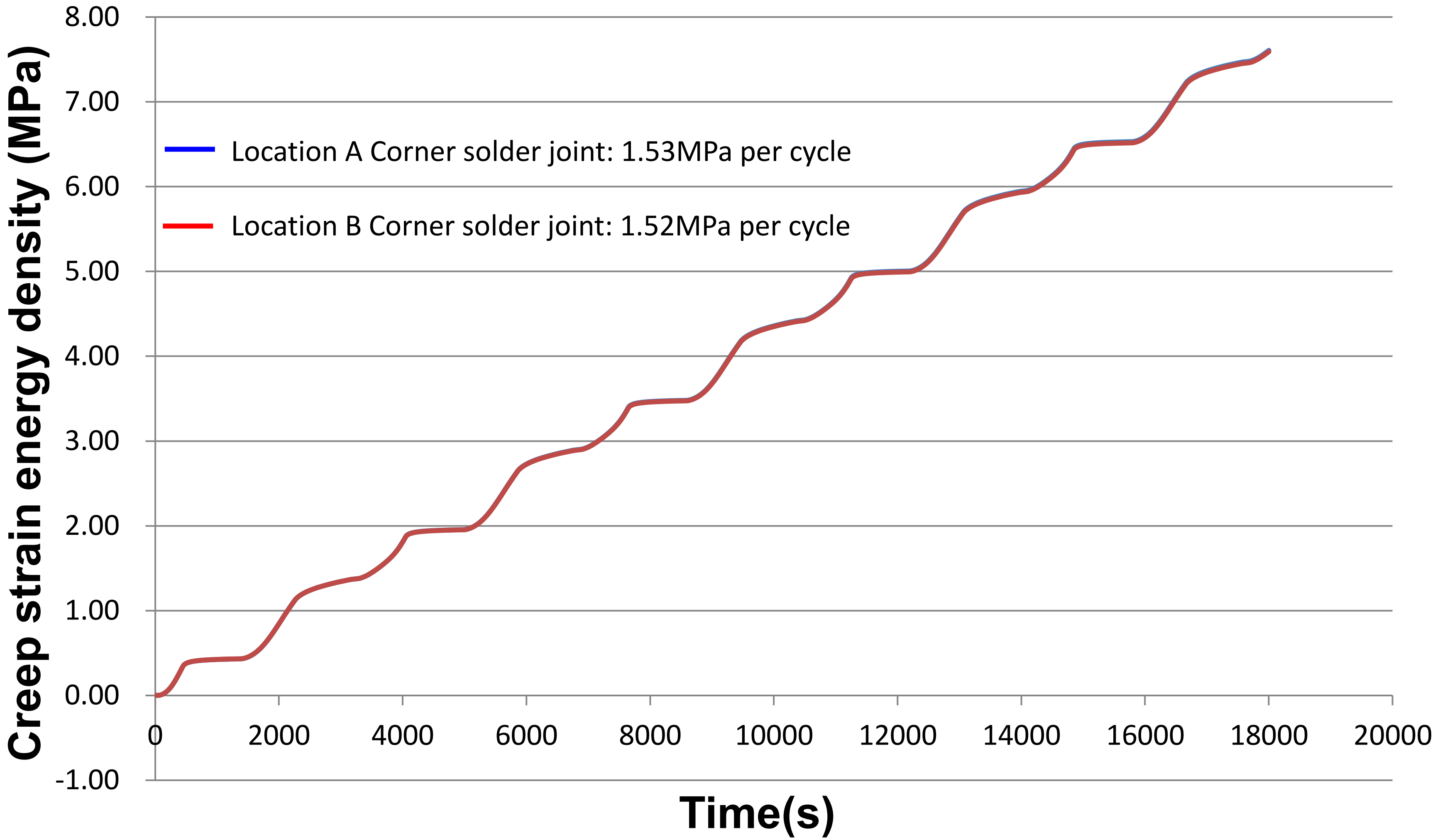


-45oC (2250s)



(b)

Creep strain energy density time-history at solder joints A and B



SUMMARY

- A high-density organic hybrid substrate for chiplets heterogeneous integration has been developed. This hybrid substrate consists of three major parts, namely the fine metal L/S RDL-interposer, the interconnect-layer, and the HDI PCB.
- The fine metal L/S RDL-interposer with a minimum L/S = 2μm has been fabricated by a fan-out panel-level RDL-first process.
- The interconnect-layer has been fabricated by the PP and vias filled with conductive paste in β-stage.
- The 8-layer HDI PCB has been fabricated by the conventional process.
- The hybrid substrate has been formed by thermocompression and the interconnect-layer become in C-stage.
- Hybrid substrate characterizations such as OM, x-ray, and SEM demonstrated that the interconnect-layer (both conductive paste and prepreg), MLs, pad for chip bonding, daisy-chains on PCB, etc. are properly fabricated. Continuity checks of the hybrid substrate have been passed.

Thank You Very Much for Your Attention!

☺