Semiconductor Research Corporation

The Roaring 20s - A Renaissance for the Semiconductor Industry

Todd Younkin
SRC, President and CEO
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Special Thanks

- William Chen, ASE
- Bill Bottoms, 3MTS
- Ravi Mahajan, Intel

- Choong-Un Kim, UT/Arlington
- Ganesh Subbarayan, Purdue
- Carol Handwerker, Purdue
- Amy Marconnet, Purdue
- Justin Weibel, Purdue
- Bahgat Sammakia, SUNY-Binghamton
- Muhannad Bakir, Georgia Tech
- Madhavan Swaminathan, Georgia Tech
- Timothy Fisher, UCLA
- Arijit Raychowdhury, Georgia Tech

- *Other CHIRP Center Faculty*
- *Matthew Johnston, Oregon State*
- *Subramanian Iyer, UCLA*

+ Their amazing partners and students

Insufficient Time to Share More

Semiconductor Research Corporation

BLUF

- The Heterogeneous Integration Roadmap (HIR) is both a **critical reference** and **an innovation community**.
- Academic research related to HIR is crucial, with fruitful areas in both basic & applied research. This includes all 23 HIR chapters, plus growing vectors like quantum, additive manufacturing, & biology.
- SRC has significantly grown its long-standing commitment to heterogeneous integration or advanced packaging at universities worldwide. For example, GRC-PKG has grown **+867% over last 5 years**.
- Academics should familiarize themselves with **SRC's "3 Pillars"** (or 3 Ps), and then…
- Academics should **submit proposals** to these three solicitations (First two are active, Third is planned):

Program	Eligible Performers	Announced	Link
JUMP 2.0	U.S. (DARPA)	Dec. 21, 2021	https://www.darpa.mil/news-events/2021-12-22
NSF REU Program*	U.S. (NSF)	Jan. 26, 2022	https://www.nsf.gov/news/news_summ.jsp?cntn_id=304304&org=ENG&from=news
GRC, Packaging (PKG)	U.S. & International	Q2, 2022	https://www.src.org/compete/

- SRC is pursuing CHIPS ACT funding to revitalize and modernize our mission, aligned to the 3 Ps. **Heterogeneous integration is priority #1** for SRC and its members.

*Administered by NSF. Do not work with SRC or SRC member companies as it is a conflict of interest.

The Future of Semiconductors Is Bright

- I started at Intel in 2001, excited about nanotechnology and Intel's race to the atomic length scale. **It did not disappoint.**
- Recently, the talent pipeline has started to dry up, significantly. The student population is not receptive to the "2D scaling forever" story. **That narrative is not finding a way into their hearts and minds!**
- Together, we must seek a new narrative. One that helps students realize we have **hard yet interesting problems that can't be solved without them**.
- All can see the $2T+ **generational opportunities** in hyperscaled computing, artificial intelligence, 5/6G+, autonomous vehicles, and quantum. We know these emerging frontiers will change the world around us!
- Yet, collectively, we must apply disciplined imagination. Microelectronics is not static! The future we imagine rests on continued, cost-effective, and innovative **breakthroughs in hardware**. Materials, integration, packaging, design, architecture, and security are all critical elements for success.

There is a bright future. Fascinating opportunities for the next 20 - 30 years, the kind you can build a career on as a young scientist or engineer.

Premier Microelectronics Consortium Since 1982

Private Sector and Interagency, Participation and Governance

DARPA NSF NIST

AMD ANALOG DEVICES APPLIED MATERIALS arm ASM INTERNATIONAL

Chemonics EMD ELECTRONICS GlobalFoundries HRL LABORATORIES IBM

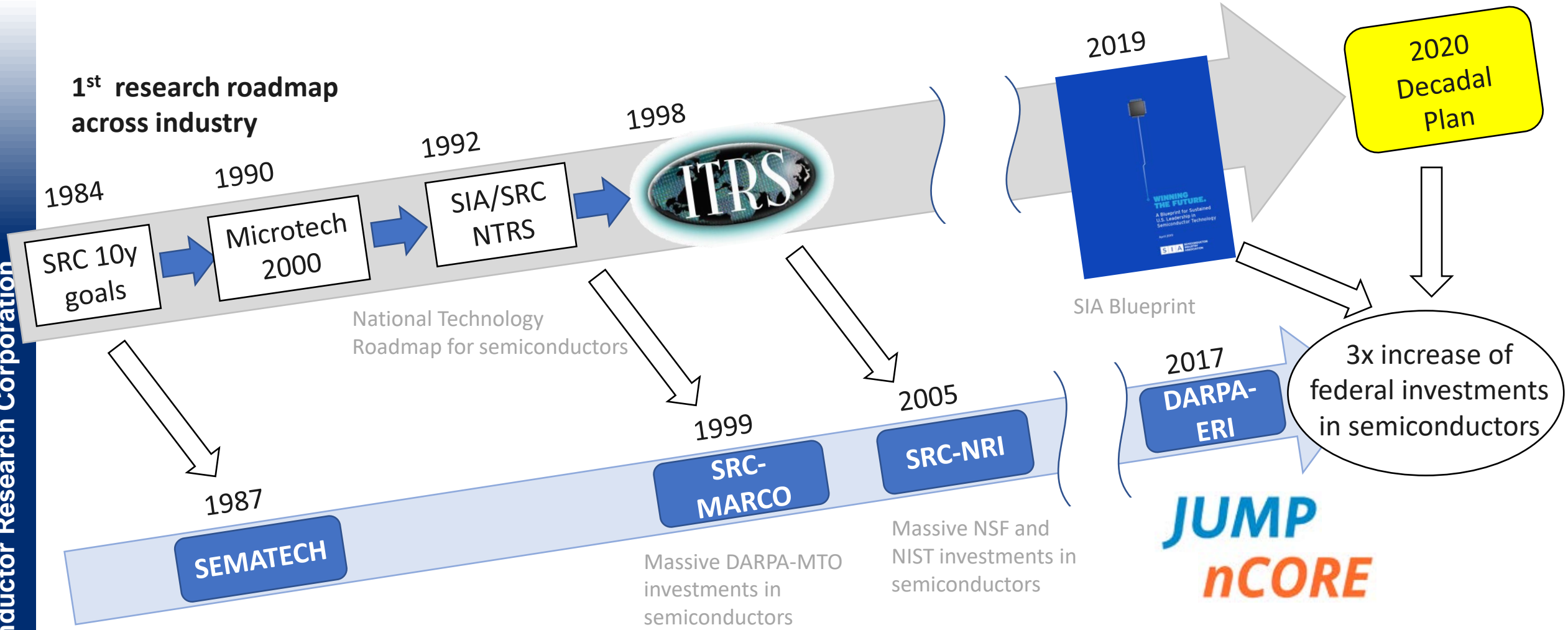
intel LOCKHEED MARTIN MEDIATEK Micron MUBADALA

NORTHROP GRUMMAN NXP QUALCOMM Raytheon Technologies SAMSUNG

SIEMENS SK hynix TEL TEXAS INSTRUMENTS tsmc Veeco

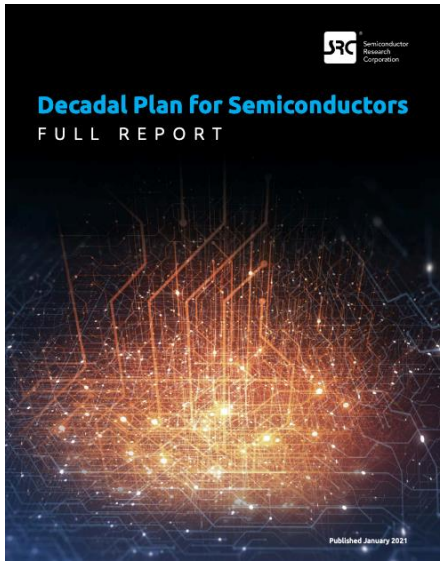
SRC is a neutral, trusted advisor that serves a vast network of engineers. All are dedicated to research, prototyping, and workforce training programs in advanced semiconductor technologies

Thought Leadership That Positions Our Industry



The “3 Ps” - SRC’s Guiding Principles This Decade

Prosperity



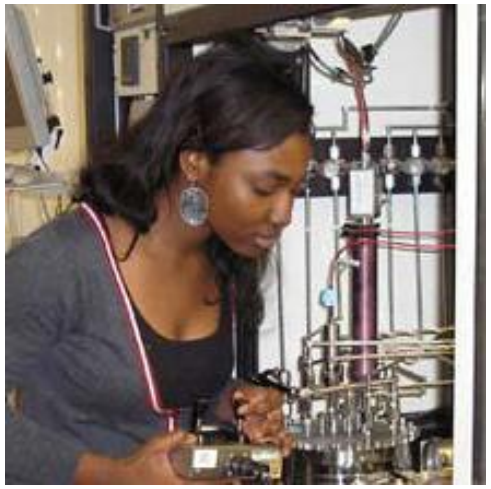
Jan 2021

Published Full
2030 Decadal Plan for
Semiconductors

5 Seismic Shifts, ICT Drivers
Call w/ SIA for ↑ Annual Funding

www.src.org/about/decadal-plan/

The People



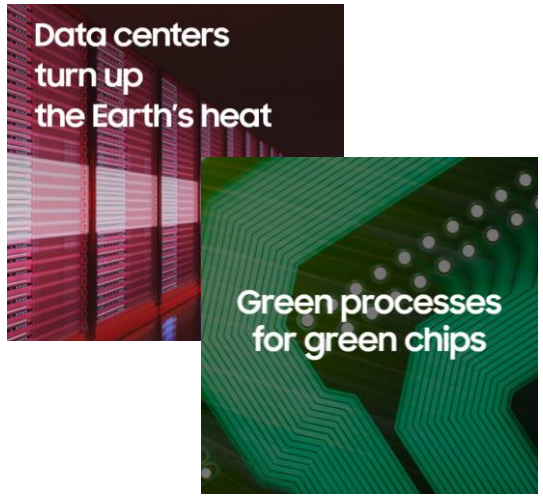
Apr 2021

Released SRC’s Broadening
Participation Pledge

Student Pipeline (AA,BS,MS,PhD)
Greater Diversity, Equity, &
Inclusion
Ignite passion in US Citizens

www.src.org/about/broadening-participation/

The Planet



Images from Samsung

Oct 2021

Released SRC’s
Commitment to Sustainability

Green Materials & Processes
Energy Efficient ICT Systems

https://www.src.org/about/sustainability/

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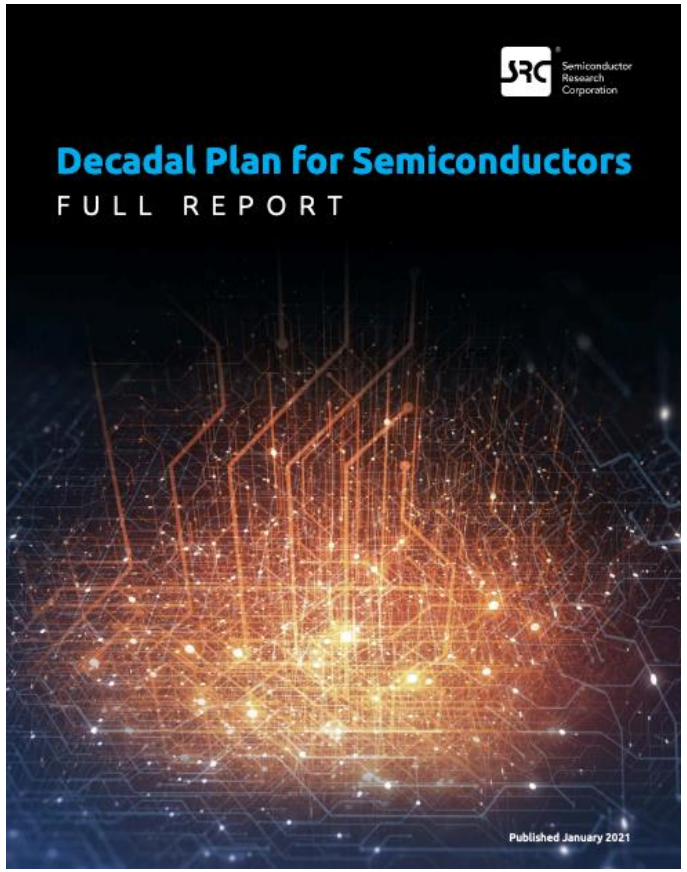
Nov' 20 - Announced $3.4 Billion Plan Aims to Stimulate US Semiconductor R&D

https://www.allaboutcircuits.com/news/newly-announced-3point4-billion-plan-aims-stimulate-us-semiconductor-rd/



https://www.src.org/about/decadal-plan/

Five "Seismic Shift" Research Priorities

- Smart Sensing — **The Analog Data Deluge**
- Memory & Storage — **The Growth of Memory and Storage Demands**
- Communication — **Communication Capacity vs. Data Generation**
- Security — **ICT Security Challenges**
- Energy Efficiency — **Compute Energy vs. Global Energy Production**

Heterogeneous Integration Roadmap Technical Working Groups

HETEROGENEOUS INTEGRATION ROADMAP

HI Market Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Heterogeneous Integration Components

- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G & Beyond - RF and Analog Mixed Signal

Cross Cutting topics

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability

Integration Processes

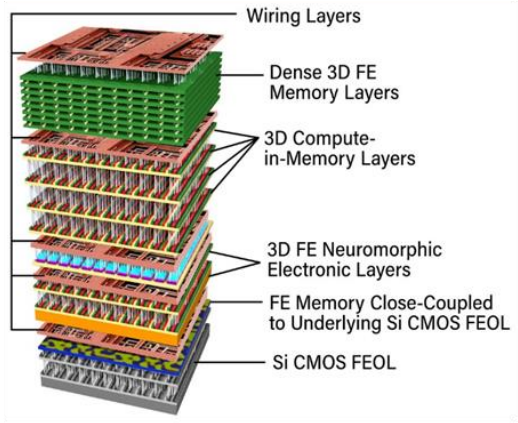
- SiP
- 3D +2D & Interconnect
- WLP (fan in and fan out)

Design

- Co-Design
- Modeling & Simulation

Microelectronics & Advanced Packaging Technologies (MAPT)

We must evaluate market-driven opportunities "side-by-side" to realize lasting innovations



Priority 1

2.5D and 3D Advanced Packaging

Image: DARPA/Intel
https://www.darpa.mil/program/common-heterogeneous-integration-and-ip-reuse-strategies

Priority 2

3D Super Chips

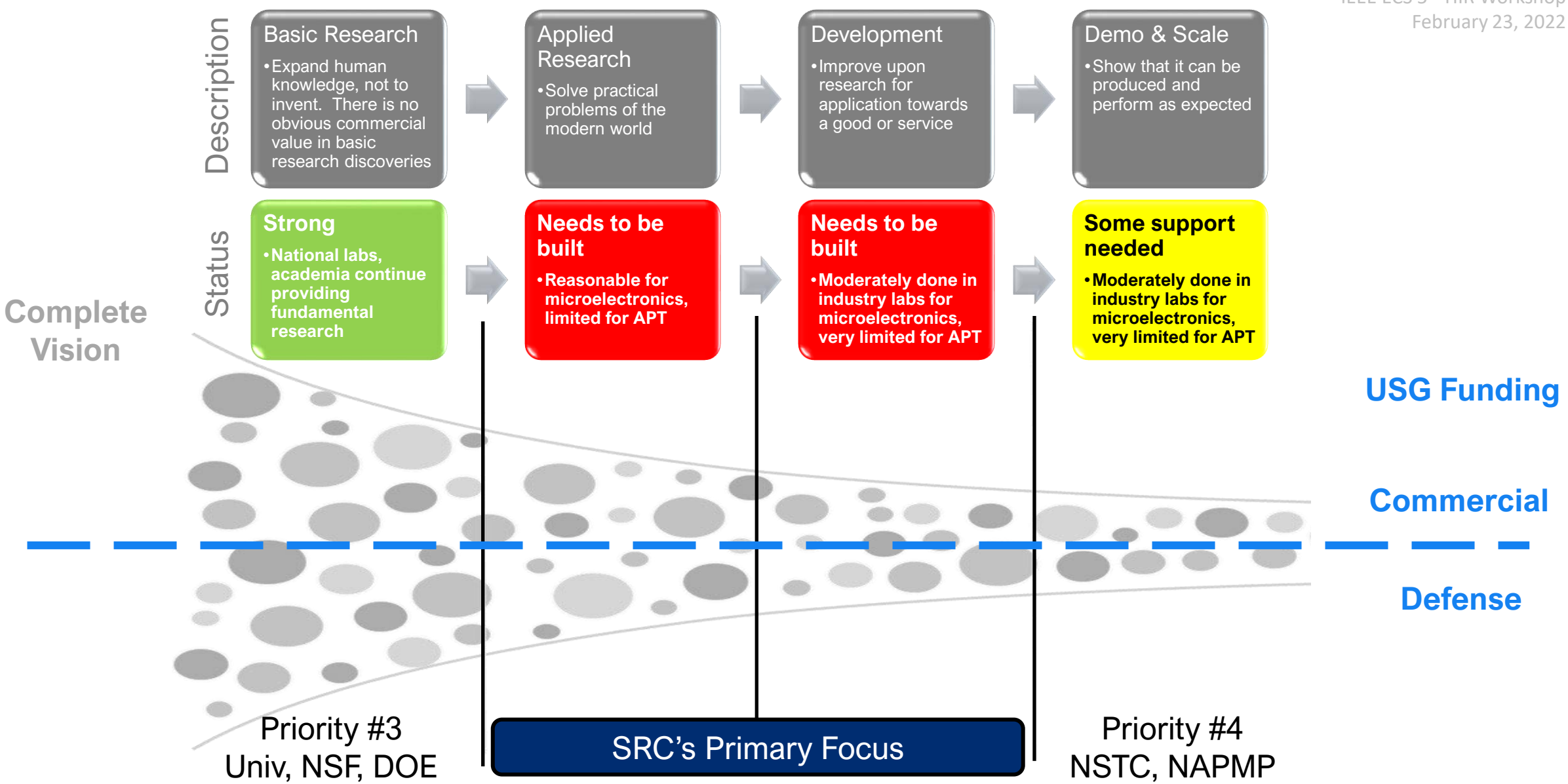
Image: SIRO, Penn State, Prof. Vijay Narayanan
https://news.psu.edu/story/625834/2020/07/15/research/over-10-million-awarded-penn-state-energy-center

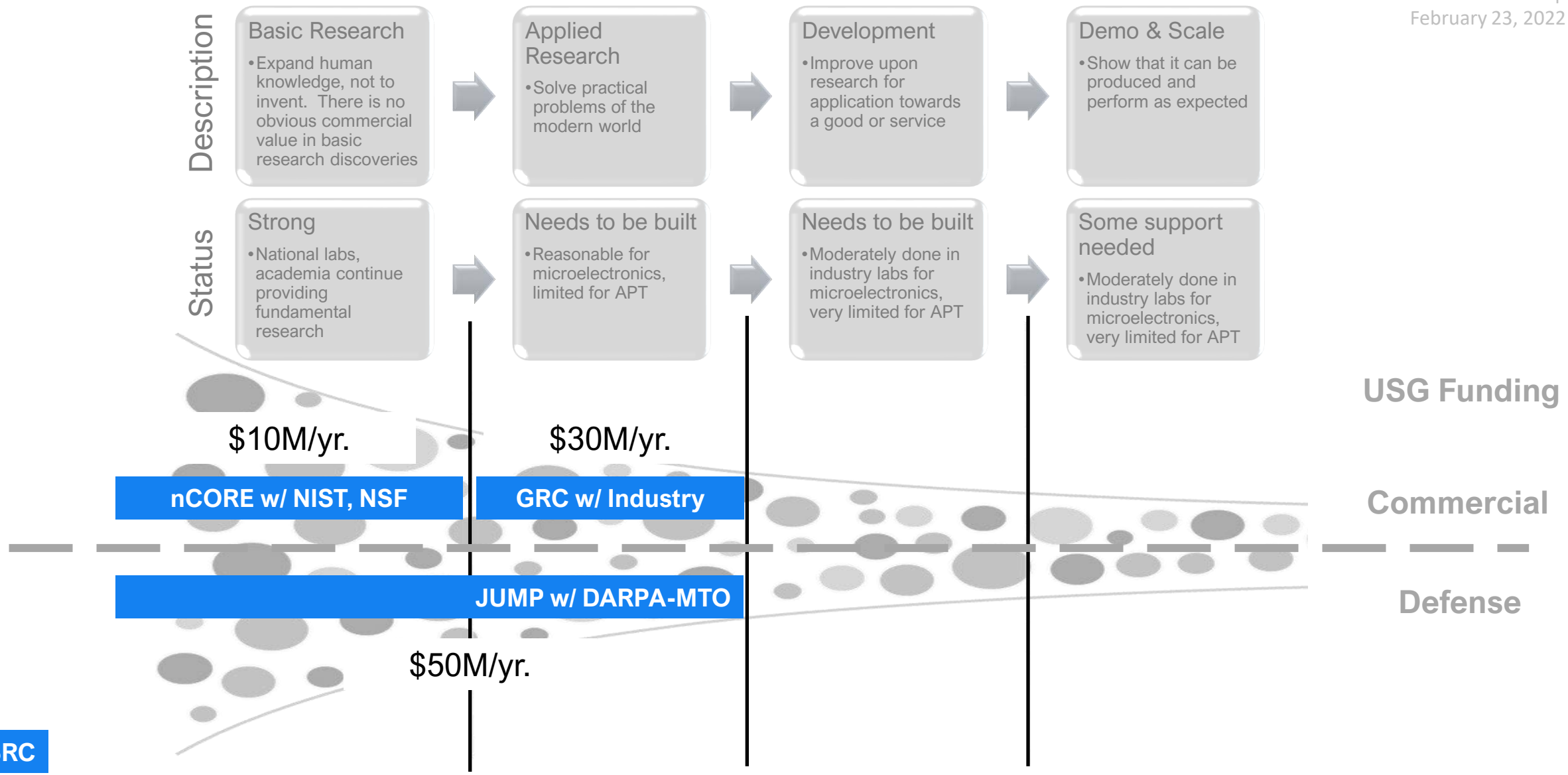
Priority 3

Hardware for New Paradigms

Image: IBM Q system displayed at CES 2020
https://www.fierceelectronics.com/electronics/what-quantum-computing

We need a Lab-to-Fab approach to MAPT Innovation. A robust pipeline from start to finish.
SRC's 2030 Decadal Plan for Semiconductors is the "What" and the HIR is some of the "How."


Description
Basic Research
•Expand human knowledge, not to invent. There is no obvious commercial value in basic research discoveries
Applied Research
•Solve practical problems of the modern world
Development
•Improve upon research for application towards a good or service
Demo & Scale
•Show that it can be produced and perform as expected
Status
Strong
•National labs, academia continue providing fundamental research
Needs to be built
•Reasonable for microelectronics, limited for APT
Needs to be built
•Moderately done in industry labs for microelectronics, very limited for APT
Some support needed
•Moderately done in industry labs for microelectronics, very limited for APT
Complete Vision
USG Funding
Commercial
Defense
Priority #3
Univ, NSF, DOE
SRC's Primary Focus
Priority #4
NSTC, NAPMP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USG Funding
$10M/yr.
$30M/yr.
nCORE w/ NIST, NSF
GRC w/ Industry
Commercial
JUMP w/ DARPA-MTO
Defense
$50M/yr.
SRC
Today

Semiconductor Research Corporation

GRC w/ Industry

PKG

UT/Arlington

33 Research Projects
15 Universities
53 SRC Scholars
37 Faculty Researchers
73 Liaison Personnel

CHIRP Center*

Ganesh Subbarayan

Bahgat Sammakia

13 Research Projects
2 Universities
29 SRC Scholars
15 Faculty Researchers
32 Liaison Personnel

JUMP w/ DARPA

ASCENT

Dir. Suman Datta
(Notre Dame)

AD Sayeef Salahuddin
(UCB)

63 Research Projects
16 Universities
133 SRC Scholars
42 Faculty Researchers
209 Liaison Personnel

ComSenTer

Dir. Mark Rodwell
(UCSB)

AD Ali Niknejad
(UCB)

39 Research Projects
10 Universities
80 SRC Scholars
25 Faculty Researchers
73 Liaison Personnel

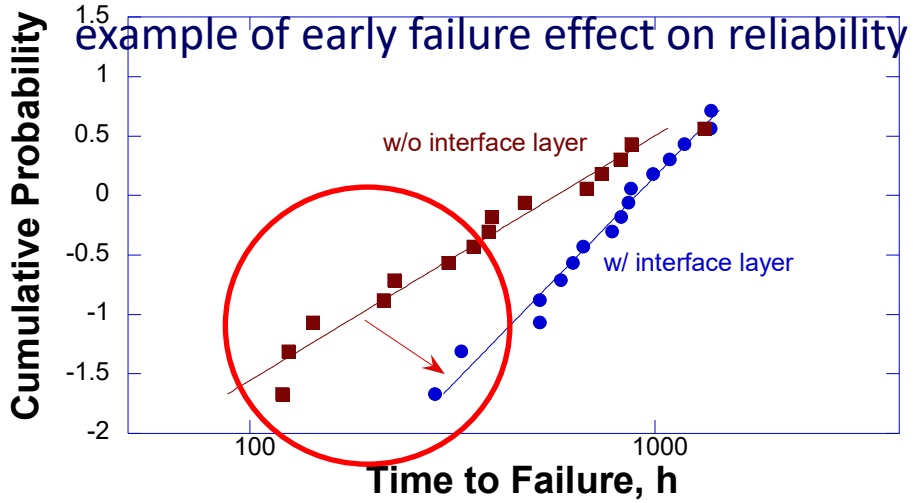
*CHIRP Center statistics are included in the overall GRC/PKG numbers

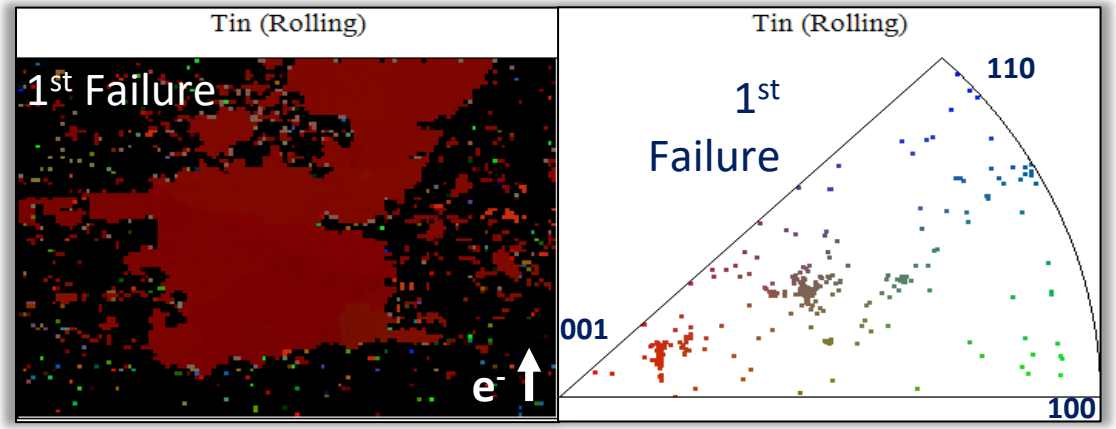
Source of Early Failures and How to Suppress

Prof. Choong-Un Kim,
UT/Arlington

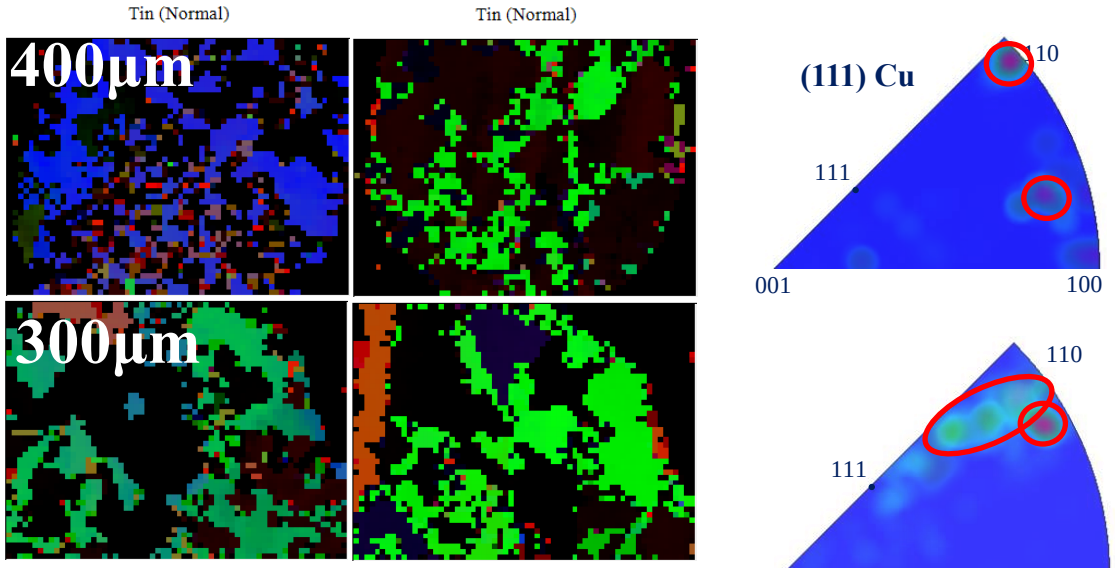
- **Suppression of early failures**
  - may be most effective and practical in improving EM reliability
  - our research finds that the early failures area always related to [001] Sn grain alignment to EM.
- **[001] Sn effect can be suppressed by**
  - using Cu substate with controlled orientation (our study w/ Cu single crystal proven that Sn grain orientation is biased by Cu orientation)
  - fine grain structure (but may not be practical)

example of early failure effect on reliability





EBSD characterization of EM failed samples reveals that early failed joint is with [001] Sn grain alignment.



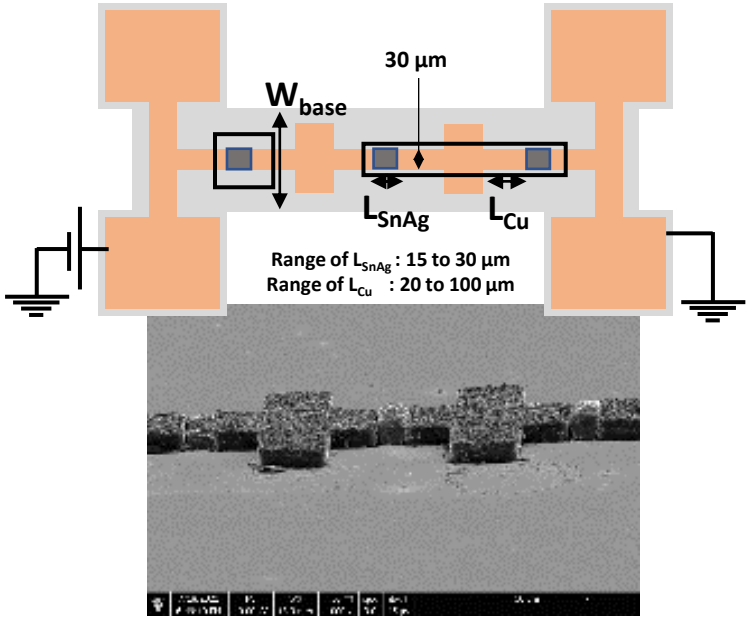
Solder ball reflowed on single crystal Cu reveals that Sn grain formation is biased. The bias effect is more in smaller solder.

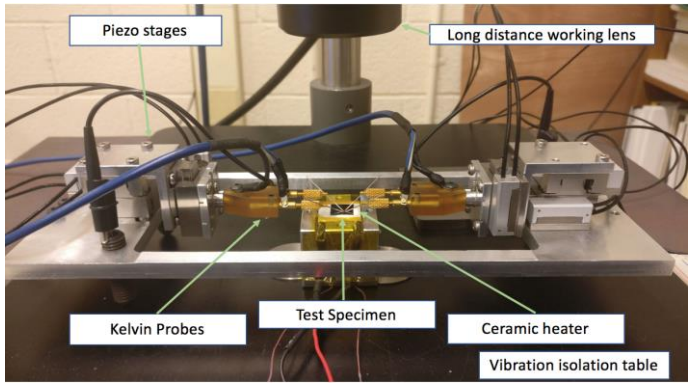
Characterization of Sub-30 μm Pitch μ-Bumps for Next Generation 2.5D Packages

Ganesh Subbarayan and Carol Handwerker, Purdue University

Goals

- Electromigration characterization of sub-30 µm pitch solder µ-bumps
- Characterization of electromigration influenced intermetallic growth and phase segregation

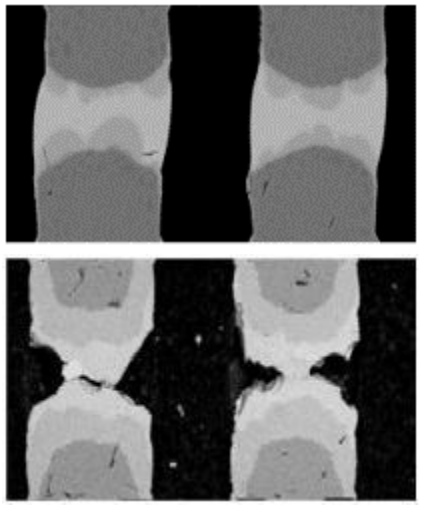


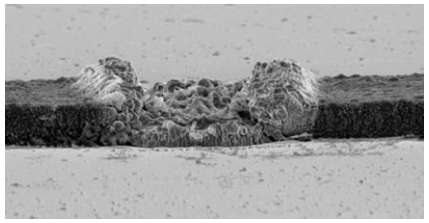


Nano-Resolution Probe Experimental Setup

Significant Results

- Designed and fabricated test device for testing sub-30 µm solder joints
- Developed electromigration test setup for use *in-situ* or *ex-situ*
- Simulated solder voiding using phase field models





High Thermal Interface Conductance Metrology

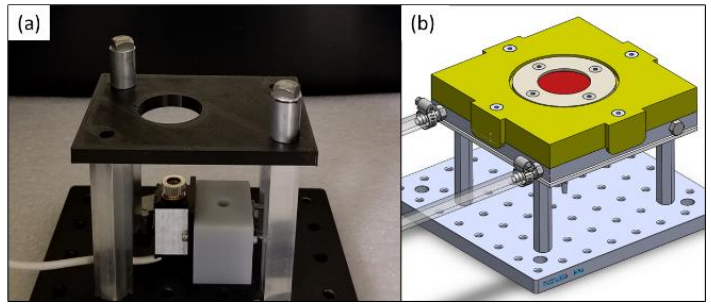
Amy Marconnet & Justin Weibel, Purdue University

Task Objective: Develop, validate, and demonstrate a standardized, versatile, robust method for characterizing low thermal contact resistance interfaces (<0.01°C·cm^2/W) applicable to a variety of different packaging applications

Approach and Goals:

(1) Develop and optimize the experimental test fixture based on target applications

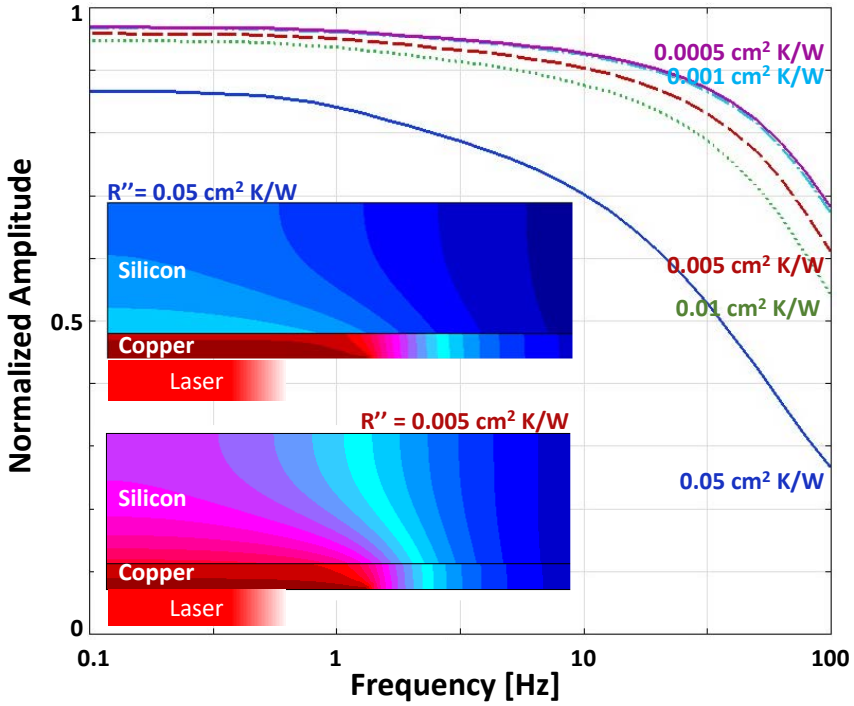
(2) Construct the test fixture and validate the measurement based on benchmark interfaces that can be quantified with standard methods



Prototype test fixture for the radial Angstrom method using single layers samples that forms a starting point for developing the metrology technique for this task.

(3) Demonstrate the low interface resistance measurement capability on application-relevant samples identified by the liaisons.

(4) Develop analytical or hybrid (analytical + finite element) models to determine the thermal resistances for a multilayer stack as a function of the temperature evolution and (separately determined) material properties without measurement of absolute temperatures.

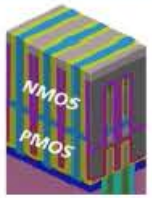
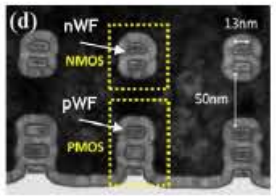
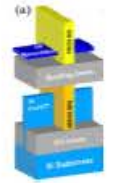
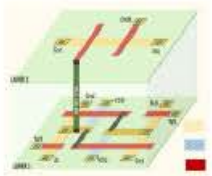
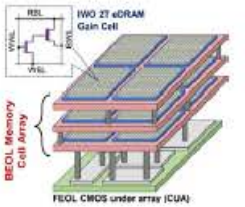
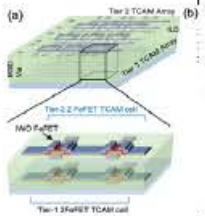
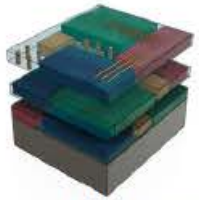
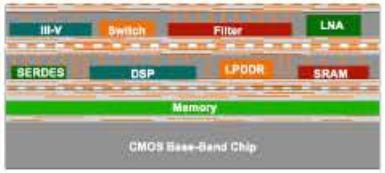
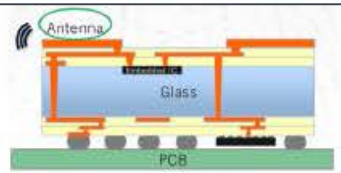


Preliminary COMSOL results for the temperature oscillation amplitude (at the top of the silicon layer) as a function of frequency and contact resistance for a Si-Cu interface. Insets show the amplitude as a function of position within the multilayer structure for two selected interfacial resistances.

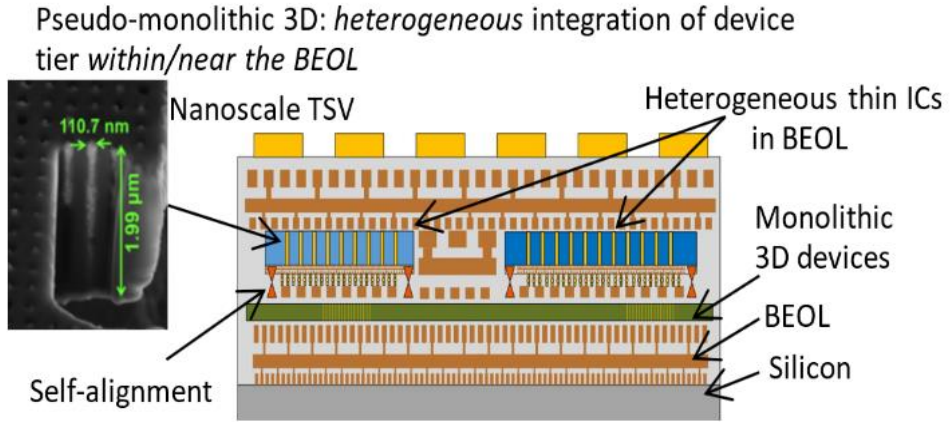
Monolithic, Polylithic and Heterogenous 3D Integration

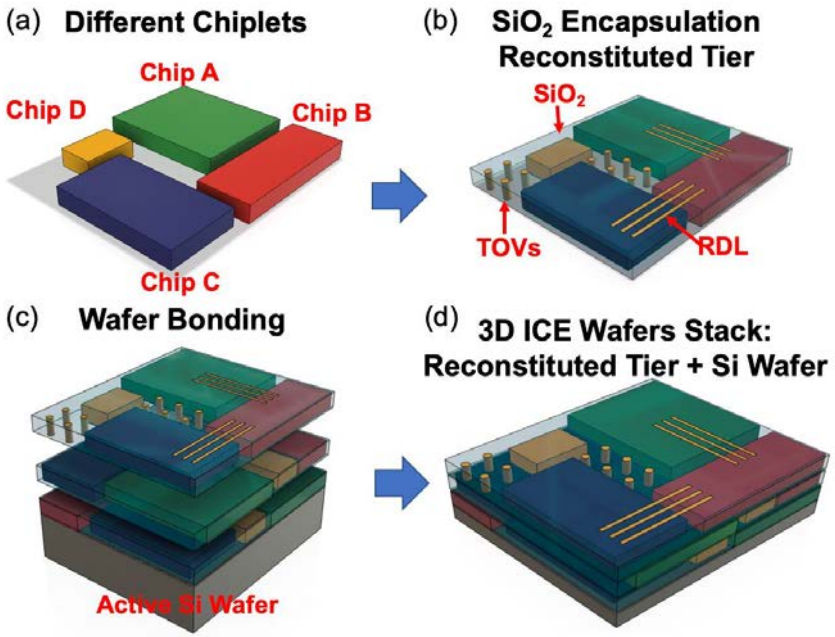
Scaling

Heterogenous integration

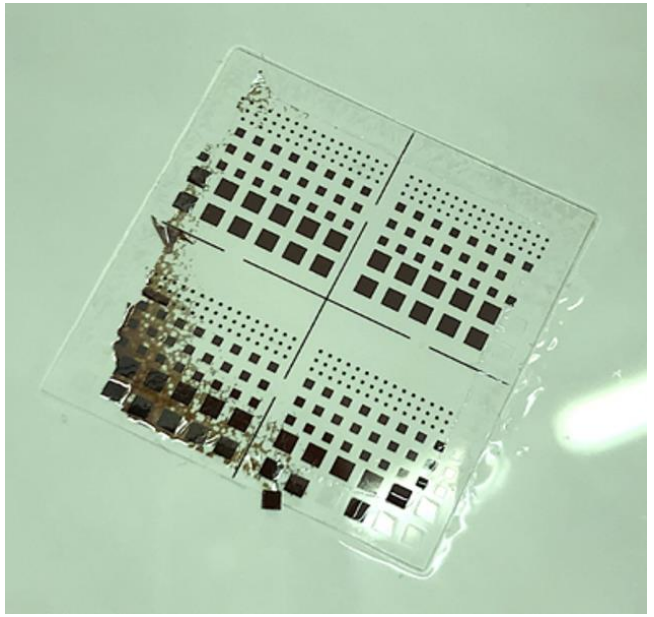
Category	Granularity	Technology	Interconnect Density (mm^{-2})	Examples
3D Transistor (before M1)	Transistor	▪ Epitaxial growth ▪ Stacked nanosheet ▪ Sequential Integration ▪ *in situ* dep and anneal ▪ layer transfer & bonding	10^9	 C-FET  Stacked Nanosheet  Ge nanosheet PMOS on FinFET NMOS
Monolithic 3D (after M1)	**Gate, Block**	▪ **Sequential Integration** ▪ ***in situ* dep and anneal** ▪ **layer transfer & bonding**	**>10^8**	 3D Transpose SRAM  3D RRAM  3D eDRAM  3D FeFET TCAM
Polylithic 3D (W2W bonding)	**sBlock, Chiplet**	▪ **Parallel Integration** ▪ **Hybrid bonding** ▪ **Metal ALD**	**10^6 – 10^8**	 SiO2-reconstituted tier in the BEOL 
Heterogeneous 2.5/3D Integration	**Chiplets, modules**	▪ **3D Packaging**	**10^4 – 10^5**	 Stacked and assembled chiplets on glass interposer

Examples of Heterogeneous Integration Technologies from Georgia Tech's *Integrated 3D Systems Lab (i3DS)*





SiO_2-reconstituted-tier mounted on a glass wafer



Smallest chiplet: 10x10 µm

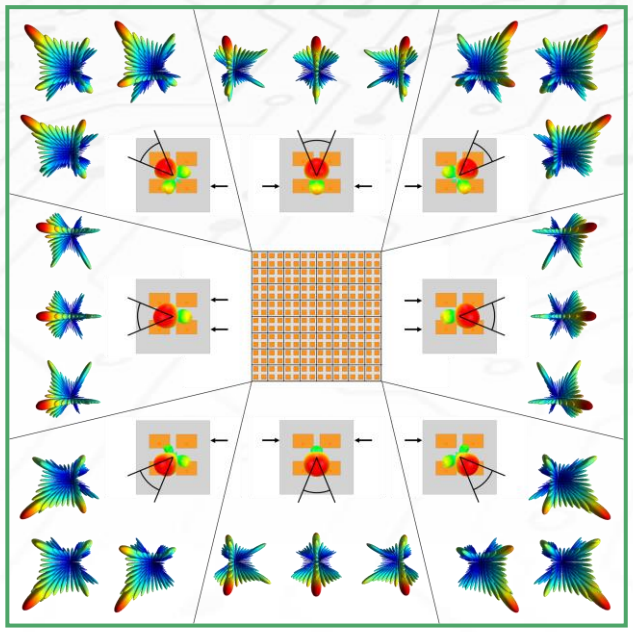
'Sea of Chiplets"

M.-J. Lai and M. Bakir, IEEE TCPMT 2021 (Early Access)

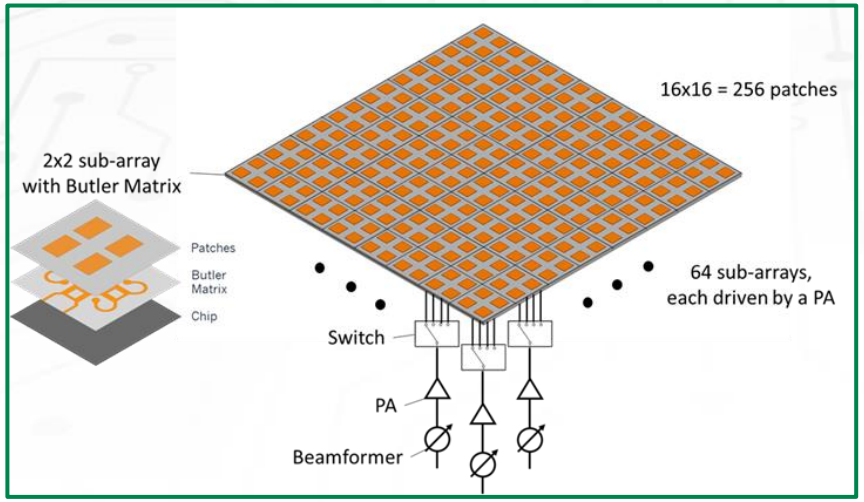
Georgia Tech

Addressing the Three Challenges: Technical Approach

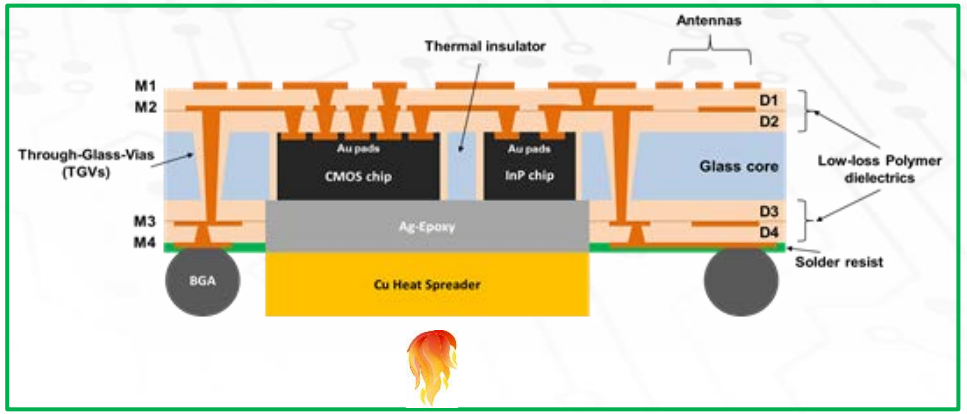
Antenna in Package



Minimizing Package Loss



Heat Removal

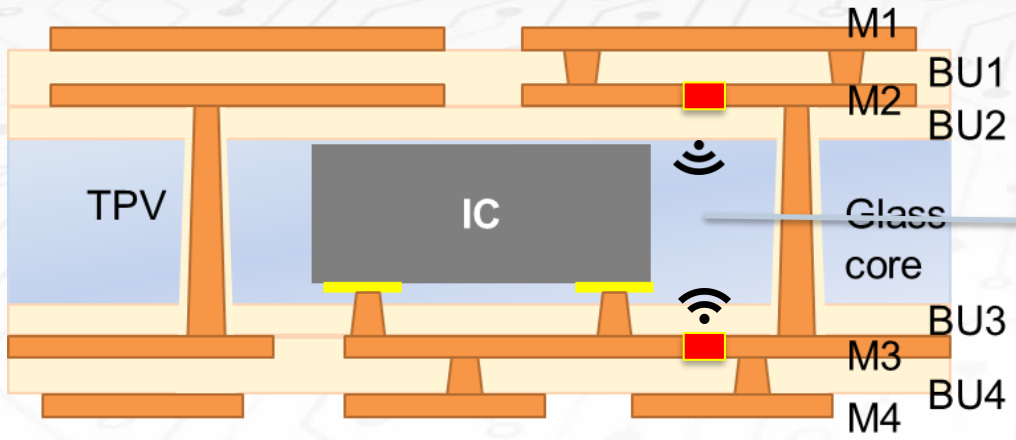


- ❑ Antenna in Package
  - Hybrid Beamforming Architecture
  - Large 2D Array for Full Field of View (Tx)
  - 2x2 Sub-Array
  - 2D Butler Matrix
  - 1D Array for Rx
- ❑ Minimizing Package Loss
  - Embedded IC
  - Eliminate assembly
  - High frequency polymer layers
  - Low loss interconnects
  - Electronics beneath antenna
- ❑ Heat Removal
  - Thru cavities in Glass
  - Exposed IC
  - Thermal Interface Material
  - Heat Spreader
  - Minimize thermal resistance

Outcome of SRC Workshop, Feb '20, Georgia Tech

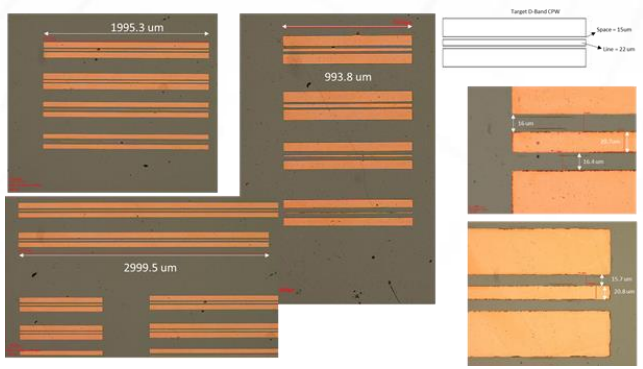
Madhavan Swaminathan | madhavan@ece.gatech.edu

D-Band Interconnects

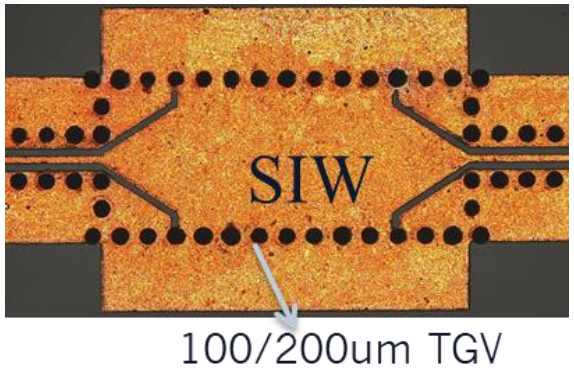


1. Co-planar Waveguide (CPW)
2. Microstrip (MS)
3. Substrate Integrated Waveguide (SIW)
4. Via-less Interconnect
5. Conductor Backed Dielectric Waveguide (CBDW)

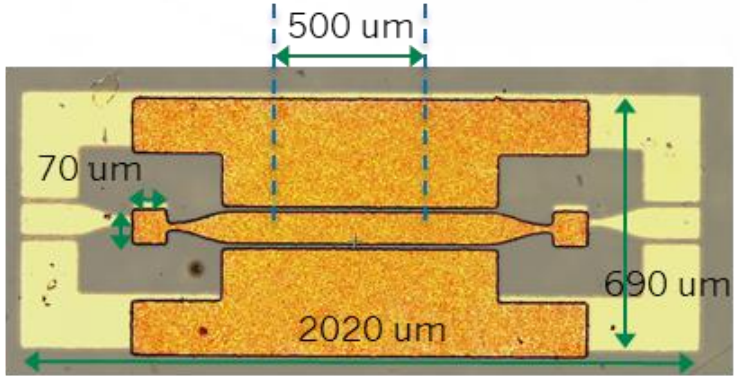
CPW & MS



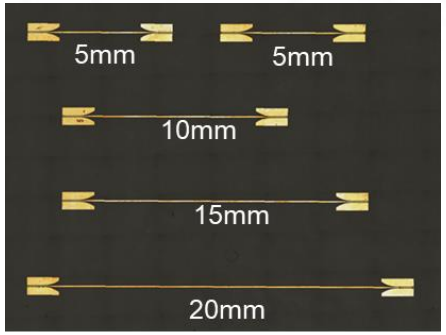
SIW



Via-less



CBDW



CPW Loss: 0.25dB/mm
MS Loss: 0.25dB/mm – 0.43dB/mm

SIW Loss: 0.7dB/mm

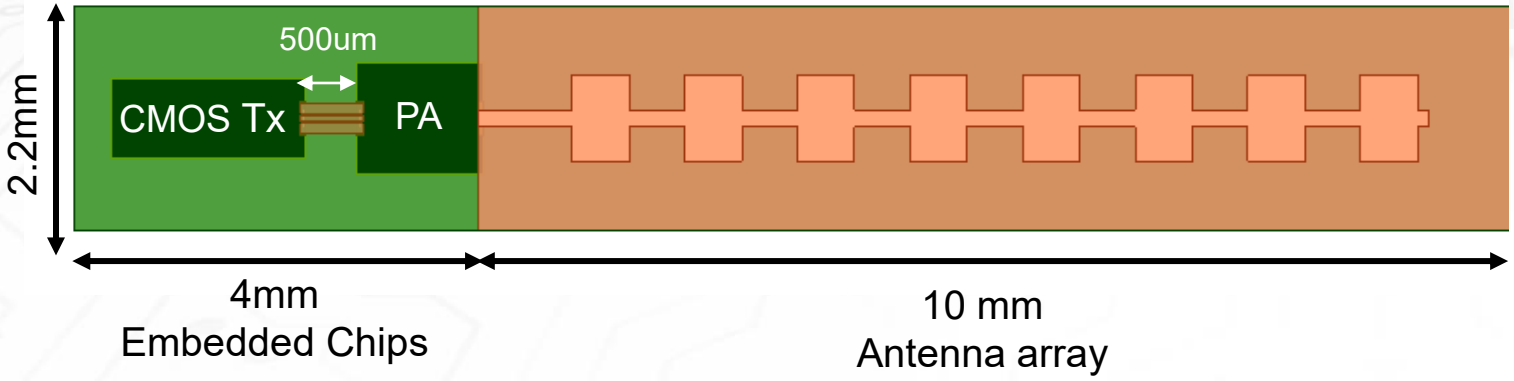
Via-less Loss: 1.8dB

CBDW Loss: 0.34dB/mm

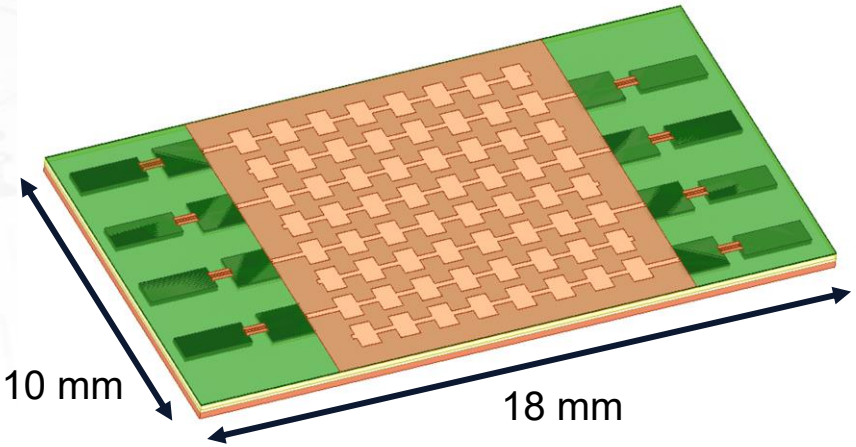
140GHz 8x8 Array Functional Module (w/ ComSenTer)

CMOS Tx 1.9mm *0.76mm *0.150mm
InP PA 1.23mm *1.09mm *0.075mm

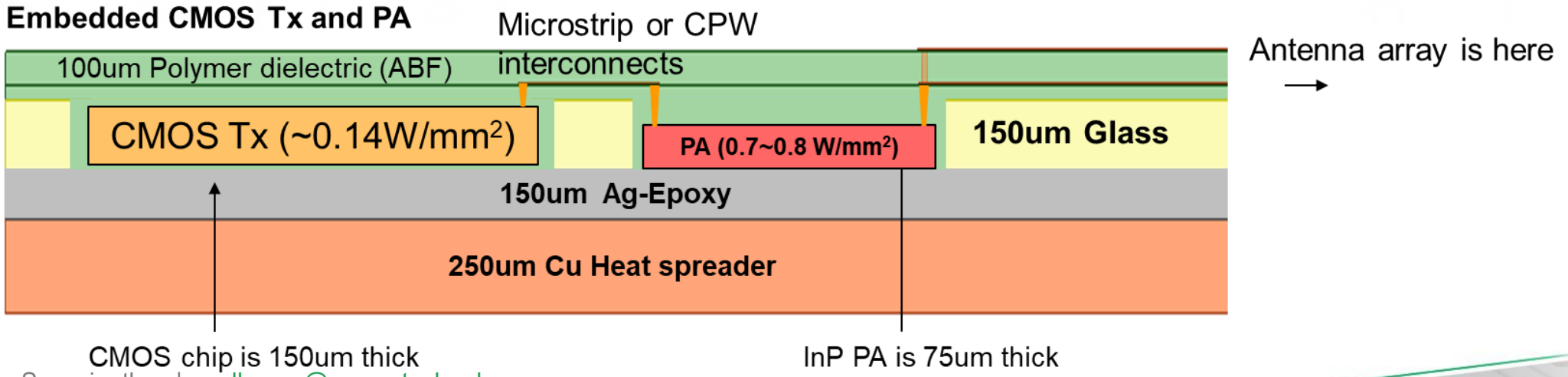
Top view of unit module



8x8 Antenna array module



Cross-section of Embedded module



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Seismic Shift 5. Compute Energy vs. Global Energy Production, Task ID: 2778.044

Thermally Enhanced Organic Substrates for GaN Power Amplifiers

Student: Min Jong Kil, Sam Ellison
Faculty: Timothy S. Fisher – Mechanical and Aerospace Engineering, UCLA

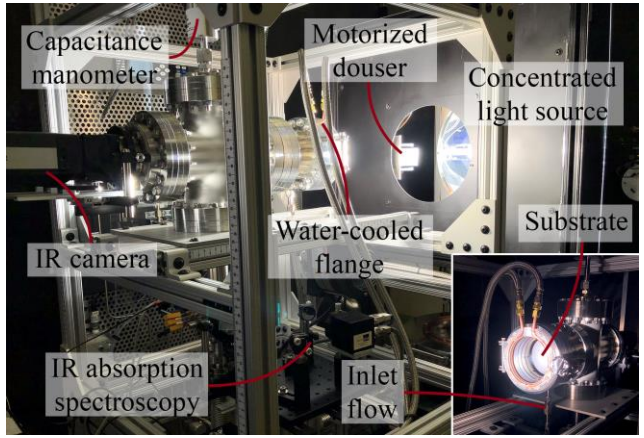
Task Focus and Goal

- Improve heat removal capability of organic substrates in high-power GaN power amplifiers
- Enhance thermal management with a ten-fold reduction in heat spreading resistance

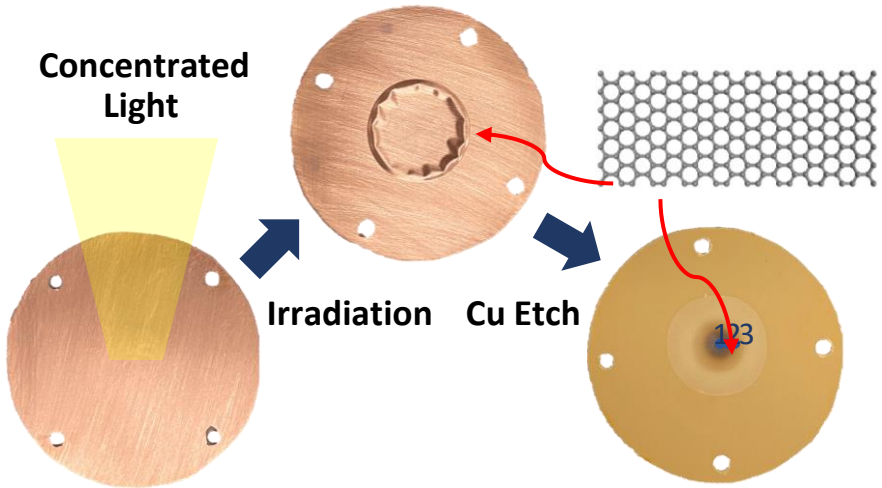
Technical Approach

- Green manufacturing: 10 kW_e concentrated simulated solar source with a maximum controllable peak flux of 4.5 MW/m^2
- Epoxy is converted into graphitized layers by short-duration, high-flux irradiation in vacuum

Overview



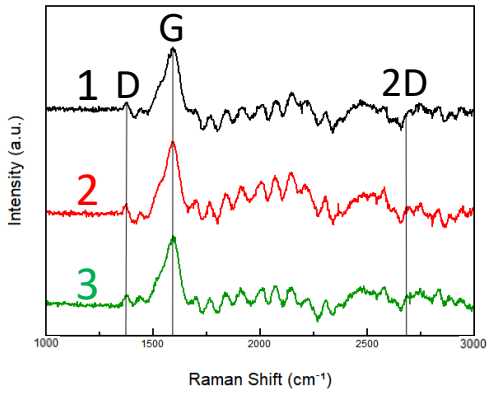
Concentrated Light Source

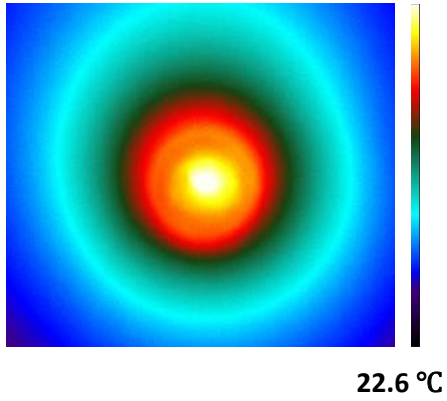


ASTRA MT77 (epoxy with Cu clad)

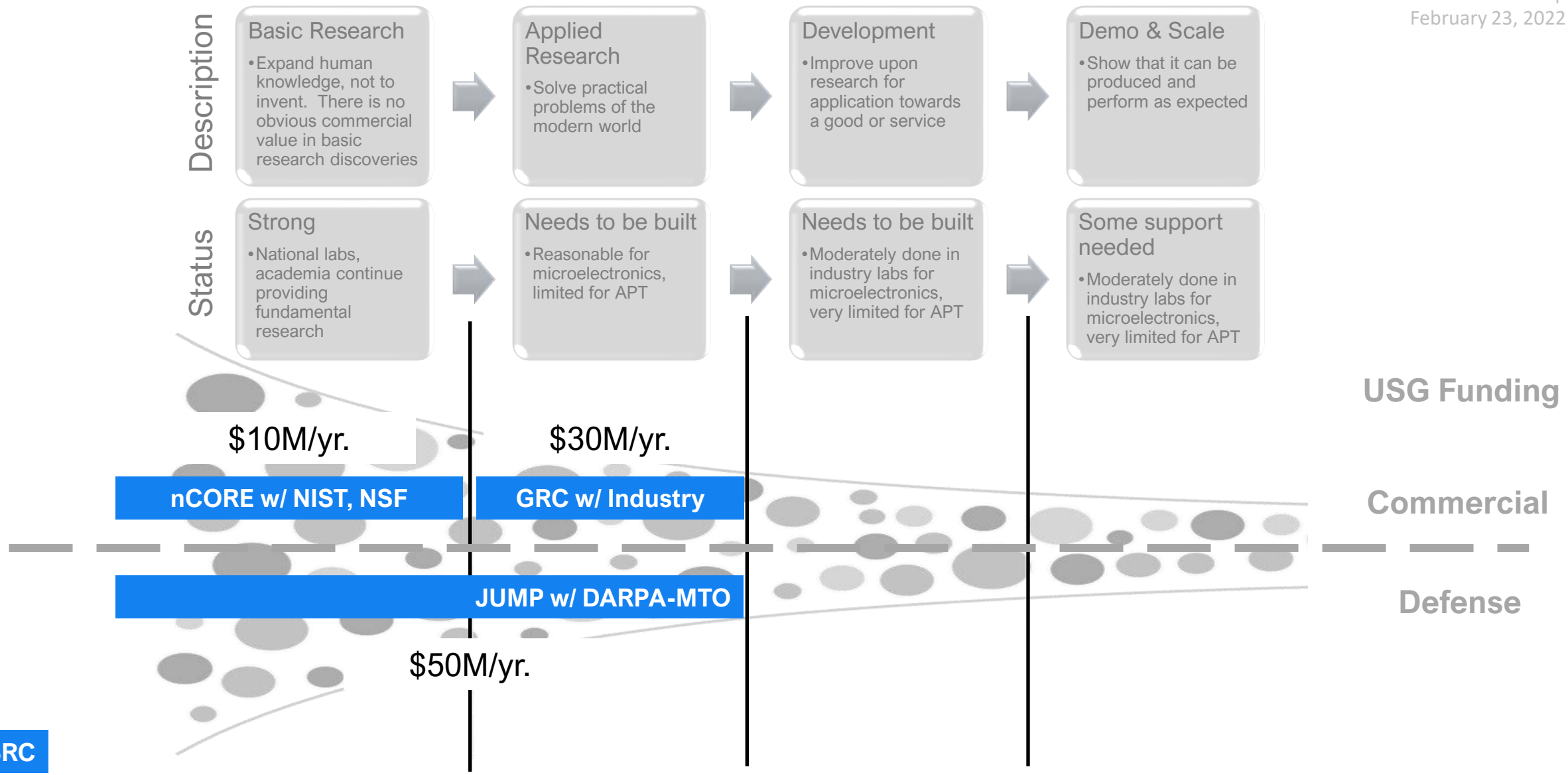
Centrally Graphitized Region

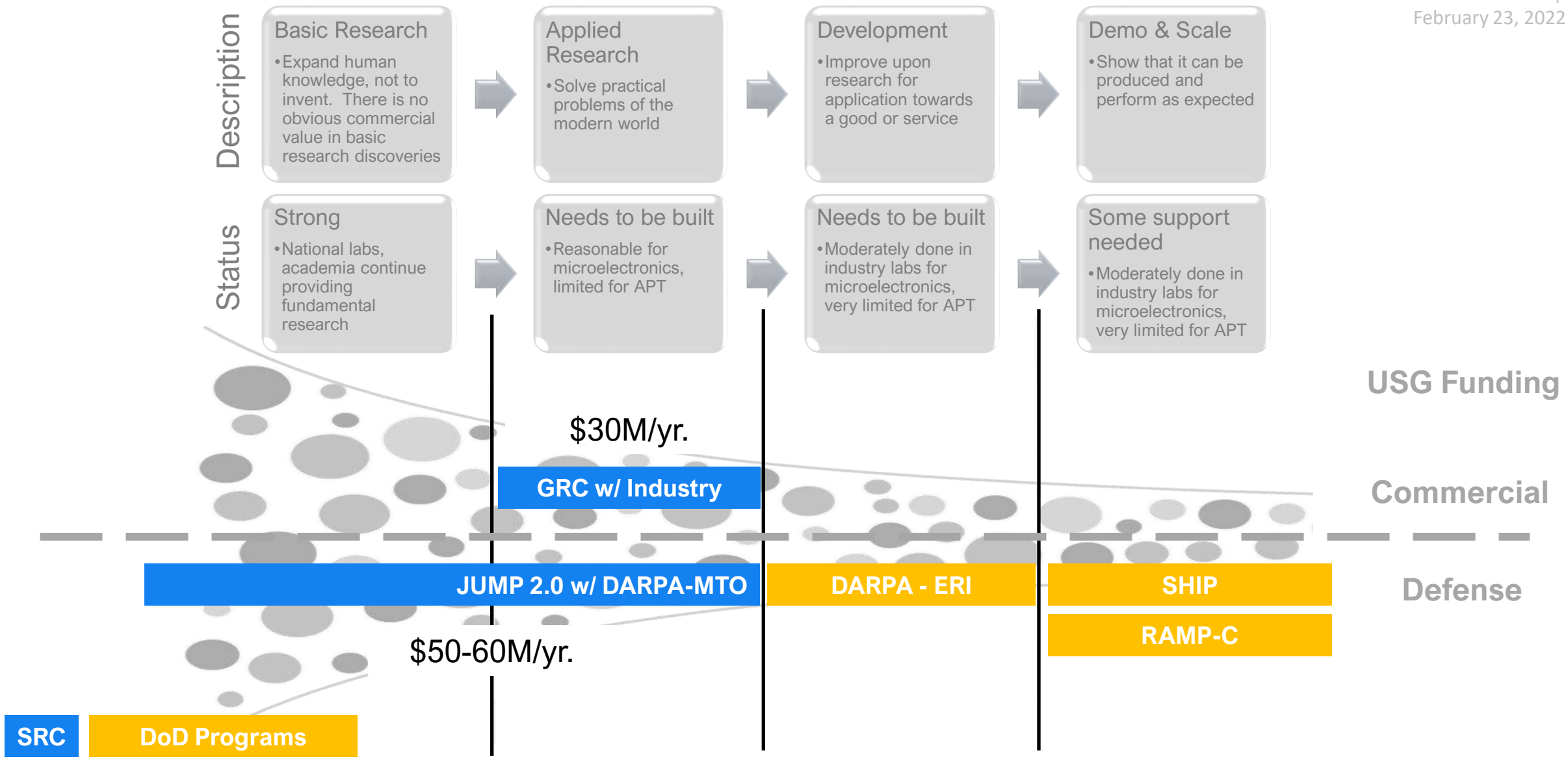
Raman Results





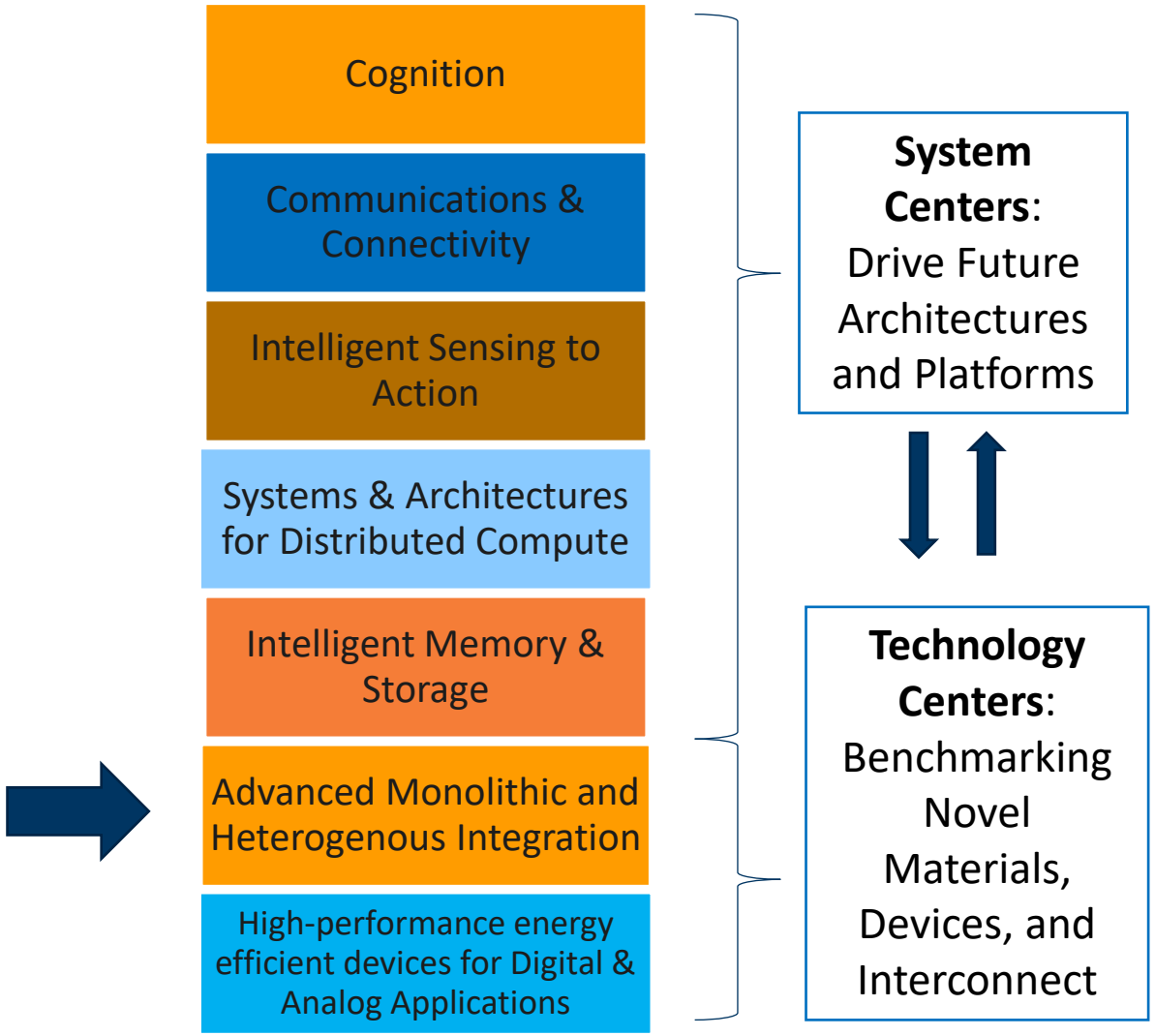
This work was supported in part by the Semiconductor Research Corporation (SRC) and DARPA.


Description
Basic Research
•Expand human knowledge, not to invent. There is no obvious commercial value in basic research discoveries
Applied Research
•Solve practical problems of the modern world
Development
•Improve upon research for application towards a good or service
Demo & Scale
•Show that it can be produced and perform as expected
Status
Strong
•National labs, academia continue providing fundamental research
Needs to be built
•Reasonable for microelectronics, limited for APT
Needs to be built
•Moderately done in industry labs for microelectronics, very limited for APT
Some support needed
•Moderately done in industry labs for microelectronics, very limited for APT
USG Funding
$10M/yr.
$30M/yr.
nCORE w/ NIST, NSF
GRC w/ Industry
Commercial
JUMP w/ DARPA-MTO
Defense
$50M/yr.
SRC
Today



Jan 2023+. Announced JUMP 2.0 with DARPA. Center & individual whitepapers due March 7th, 2022.

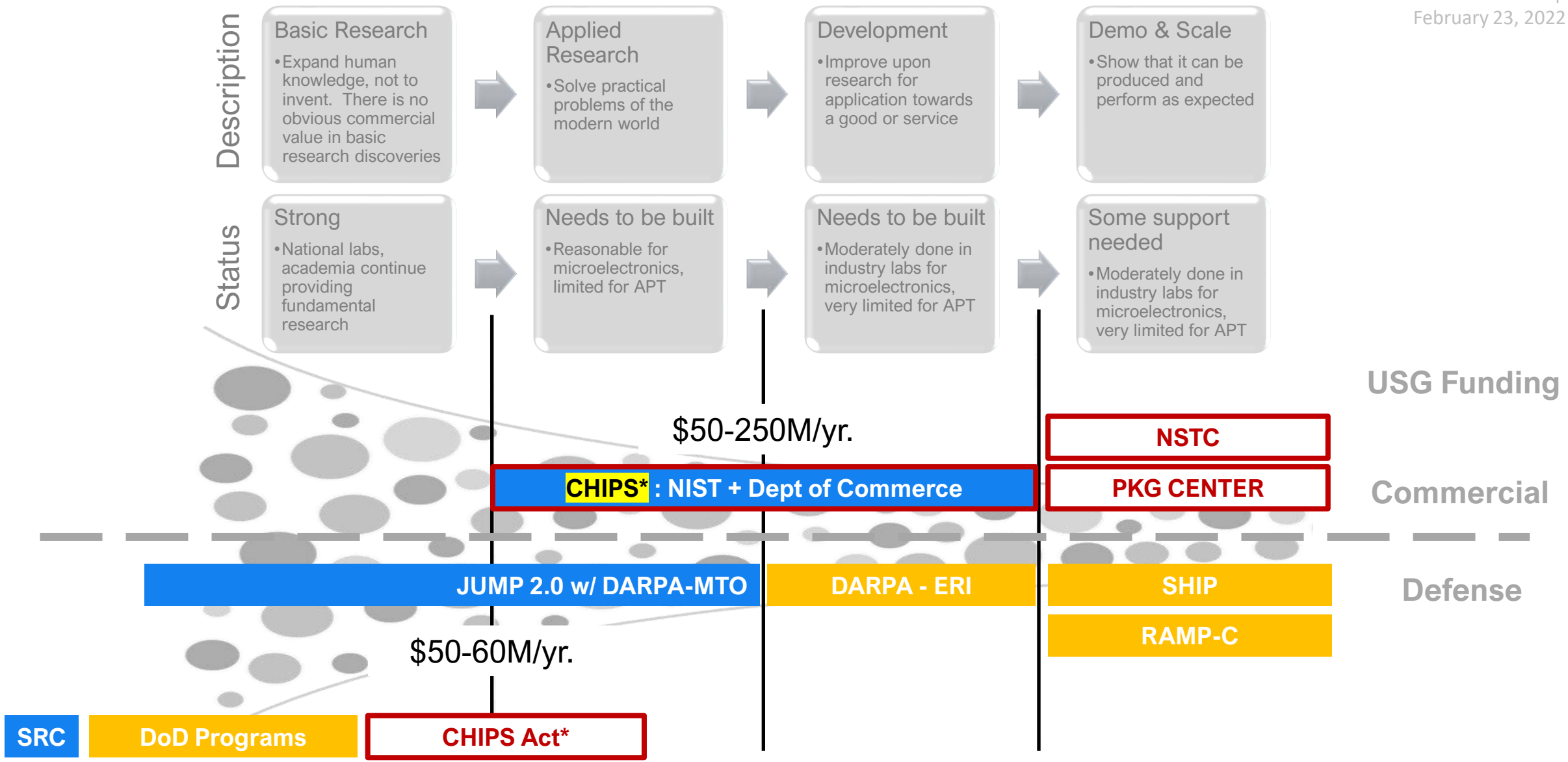
JUMP 2.0 Focus Centers



- System Centers: what are the technology implications?
- Technology Centers: what are the architectural implications?

- Target budget per Center: $5M-$7M/yr.
- Right-size for Critical-mass & Critical Mind Share.
- Recommended:
  - ~20 PIs*
  - Median task size: ~$250k/yr.
- # of Universities not specified; find a balance. (See FAQs, Q4)

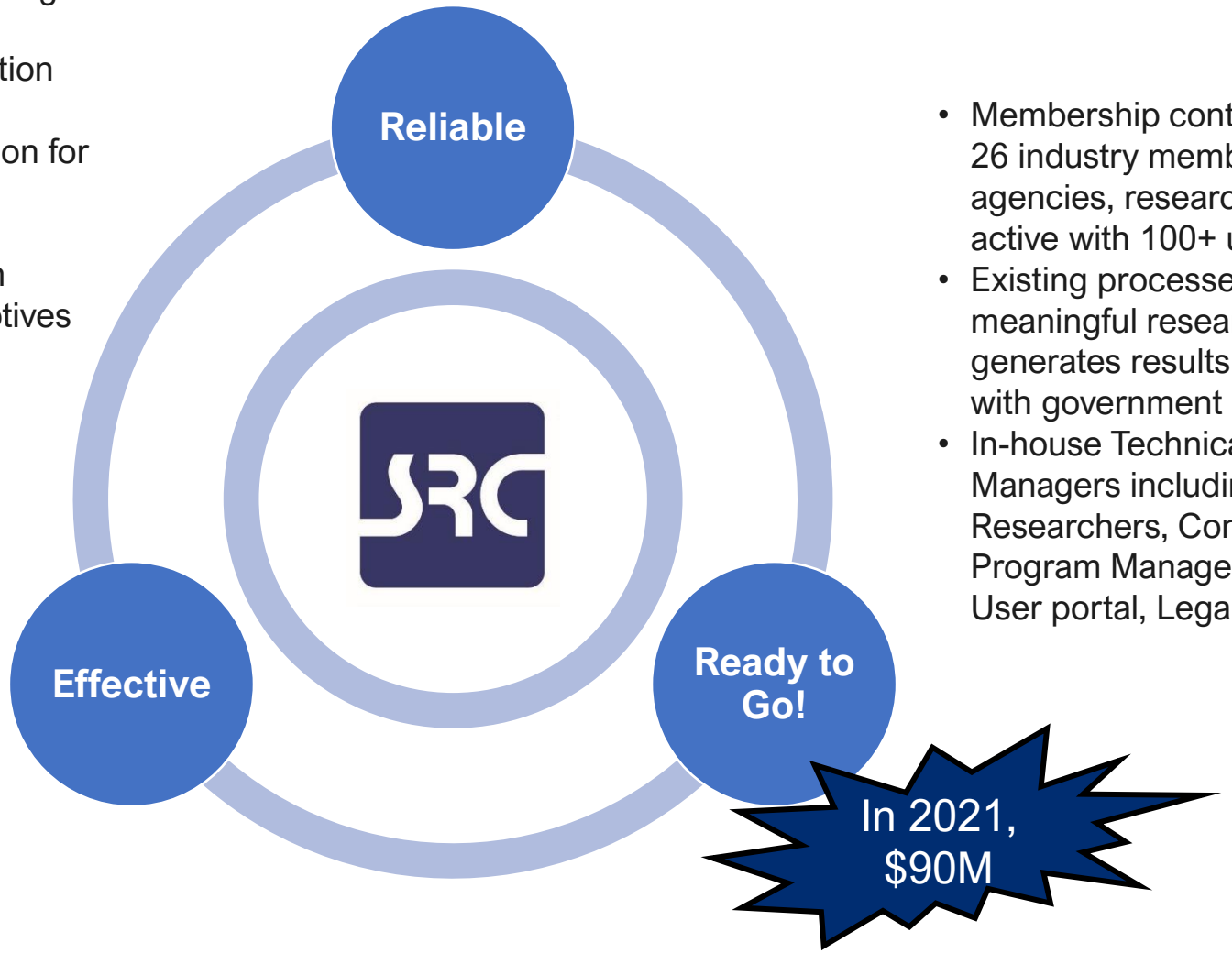
*NOTE: Do not submit whitepaper with full team. See solicitation.



With anticipated CHIPS ACT funding; *Congressional legislation pending

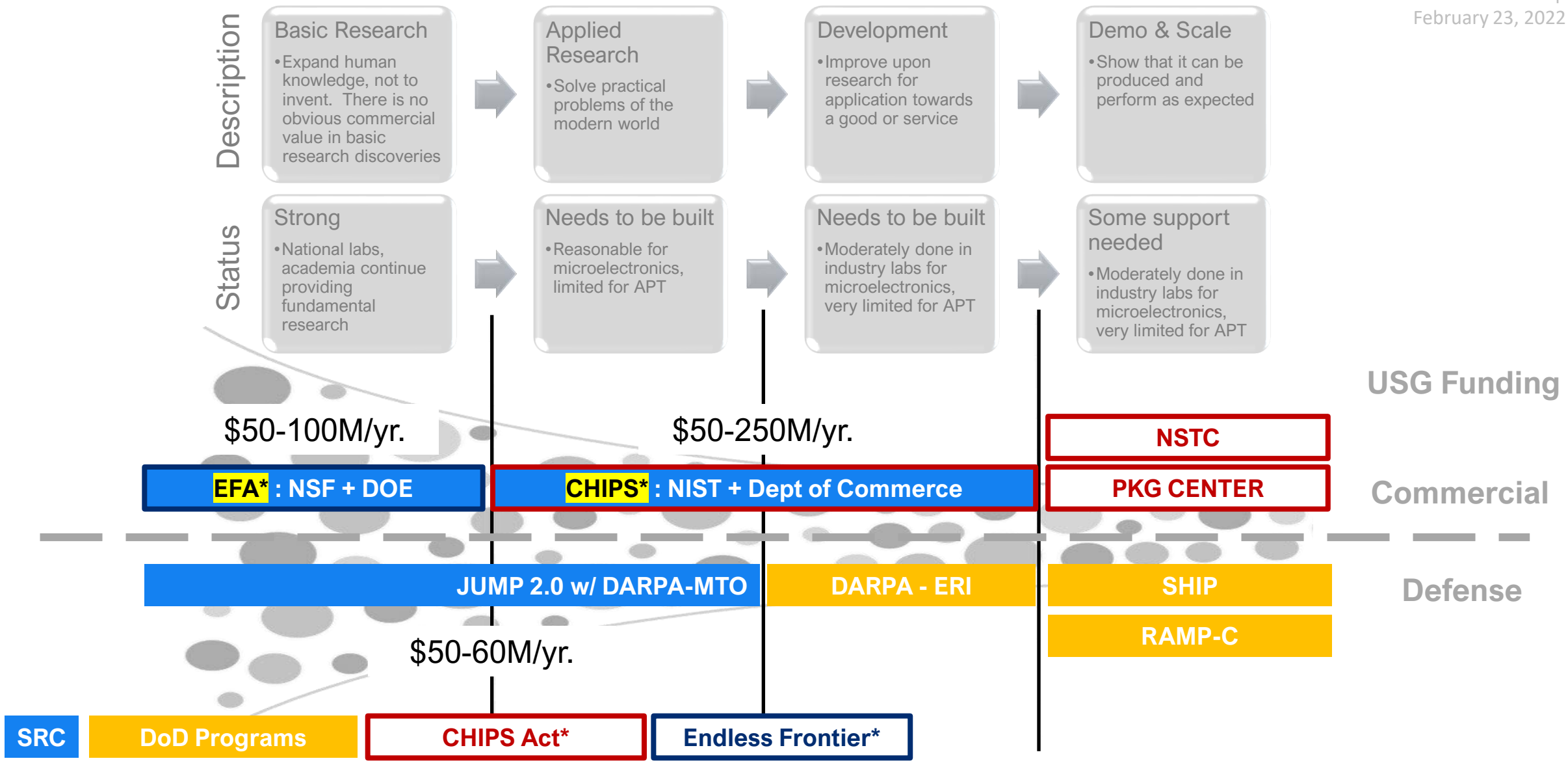
Why SRC is the Right Organization to Lead

- Low risk. A 40-year history of working with companies, universities, and governments across many innovation programs
- Often sited as the go-to organization for Industry- Government- Academic collaboration
- A Non-profit, neutral 3rd party with nothing to gain and no ulterior motives or outside influences



- Membership contracts active with 26 industry members and 3 gov't agencies, research contracts active with 100+ universities
- Existing processes for defining meaningful research agenda that generates results and partnering with government
- In-house Technical Program Managers including Industrial Researchers, Contracting, Program Management, Billing, User portal, Legal, etc.

- Bringing industry for effective technology transfer that benefits the university and the market
- Develop technology that's shaped the industry for 40 years
- Consistently builds communities where they are needed



Ideal Build Out; *Congressional legislation pending

Semiconductor Research Corporation

Future Talent

Drive holistic, optimal solutions in HW/SW through interlocked multidisciplinary research

Help students see we have hard yet interesting problems that can't be solved without them

Convey to students that opportunities are abound for the next 20-30 years

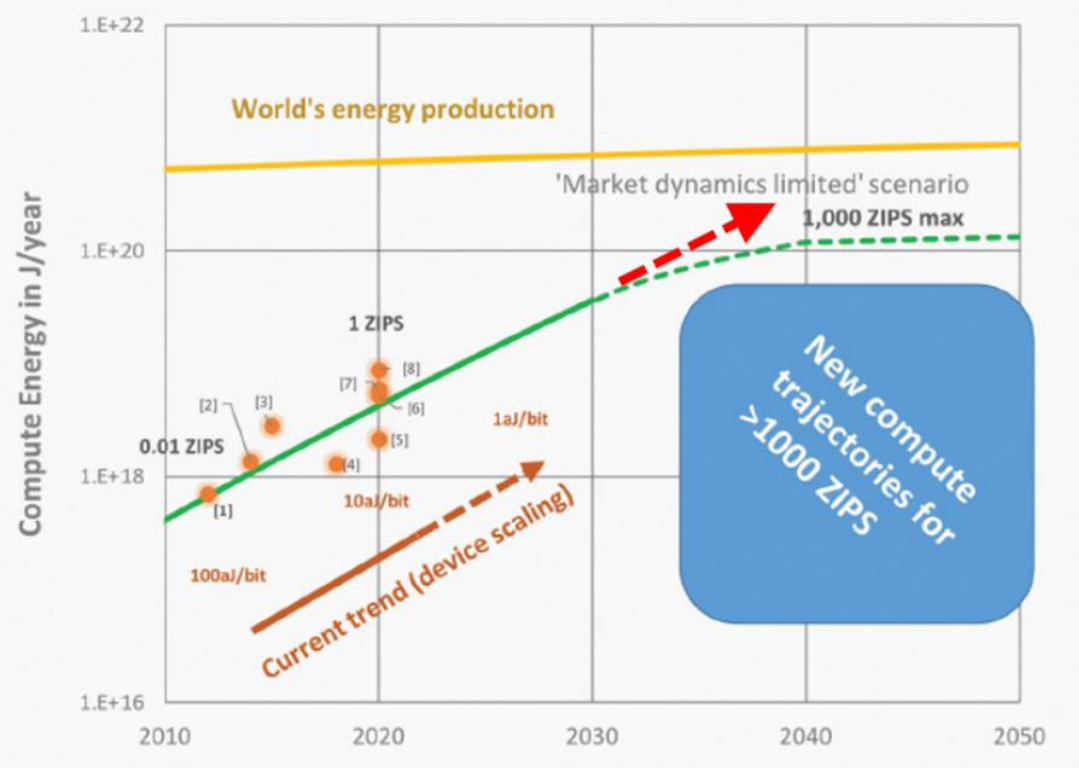
Create industrial relationships and internship experiences that provide insight into SOTA*

*SOTA = State of the Art

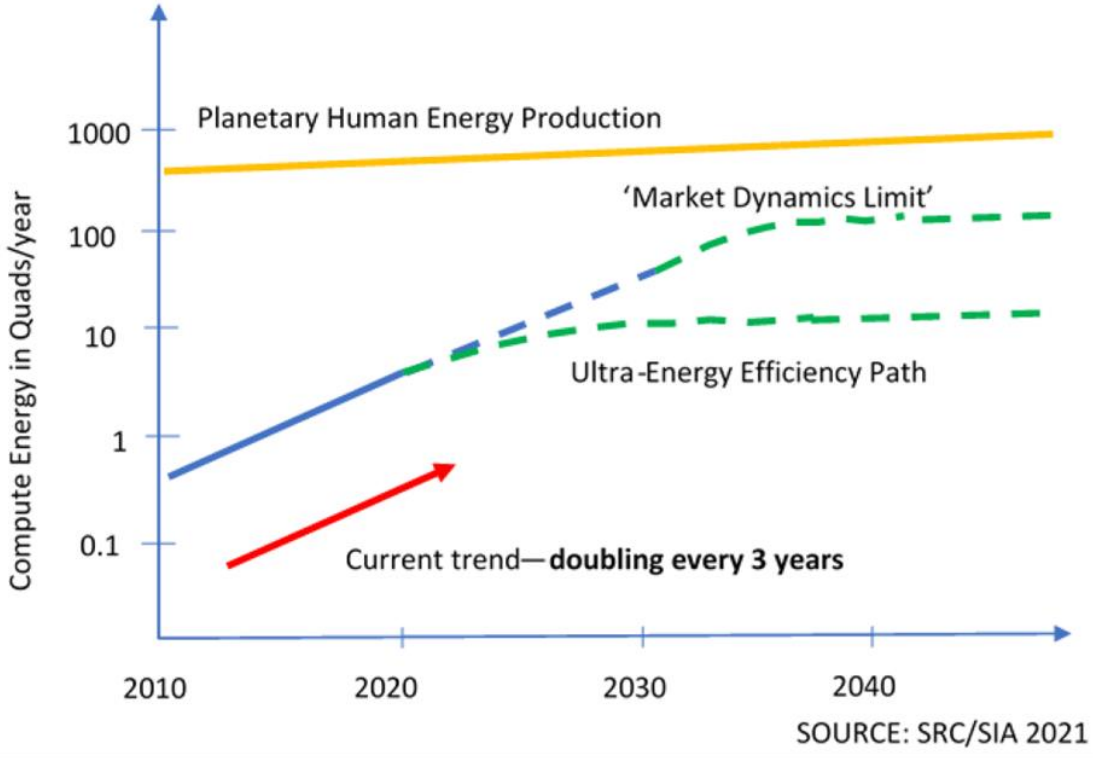
We need an aspirational new narrative that ignites the next generation of talent

Compute Energy vs. Global Energy Production

Seismic Shift #5



2030 Decadal Plan for Semiconductors



DOE-AMO Workshop, Apr 21-23, 2021

This is not only critical for our society and planet, but sustainable microelectronics **can win the hearts & minds of young innovators**.

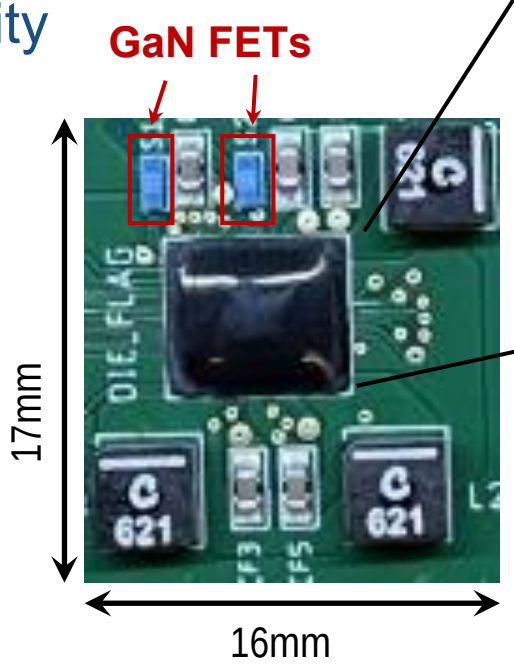
High Voltage DC-DC Converter with Package- and Board-level GaN/Si Integration

- Optimized design with high-performance low-voltage Si devices with high-voltage GaN devices
- Breakthrough efficiencies for 48V-to-1V and 24V-to-1V conversions.
- Compact design for high energy-density

Topology	3-level hybrid Dickson
Area	16mm x 17mm
Input Voltage	48V
Output Voltage	0.7-1V
GaN FETs	Enhanced mode GaN
Inductor	3 x 0.62uH
Peak Efficiency	90.4%@48-1V, 1MHz
Current Density	240/ *955A/inch^3

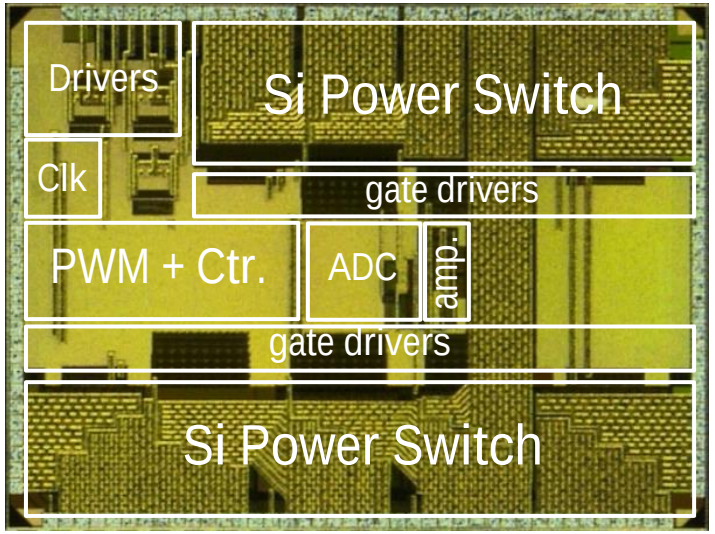
***Component area only**

Latest Prototype



Converter Board

Die shot and characters



Technology	180nm HV BCD
Area	4mm x 3mm
Si Switch	24V/20V/16V/12V/6V N-type LDMOS
V_{DD}	5V

Call to Action

- The ICT opportunities of tomorrow are simply **unachievable with emerging hardware technologies** as the underlying hardware is up against fundamental physical limits.
- A crisis is at hand, where the hardware paradigm must shift to create the desired value with **3D microelectronic** and **advanced packaging technologies (MAPT) as the key driver**.
- To stay at the leading edge of hardware innovation, we must invest in early-stage ideas and tech maturation, exploring options through a **fast-fail** and **tech-transfer mindset**.
- It is equally important that we are **committed to workforce development** and **broadening participation**.
- We must seek and create **energy efficient systems** via **eco-considerate manufacturing**.
- There is a bright future for semiconductors, but we must change our own narratives to win over the hearts and minds of next gen innovators.

Investment in Heterogeneous Integration is priority #1. We must act, now!

SRC's Mission For The Roaring 20s

Semiconductor Technology Leadership

- 2030 Decadal Plan for Semiconductors

Diverse Student Pipeline

- Broadening Participation Pledge

Eco-Considerate Processes and Systems

- Commitment to Sustainability

Learn more at https://www.src.org/about/