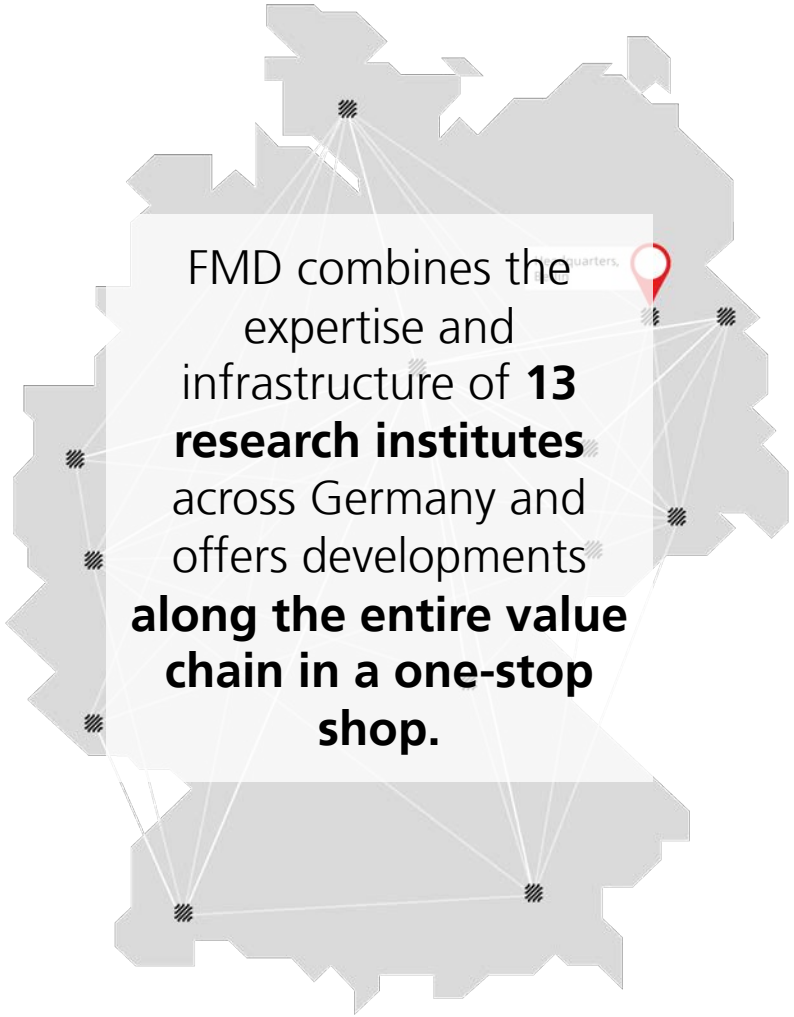
Research Fab Germany (FMD): Bridging Chip Design to Applications Through Heterogeneous Integration

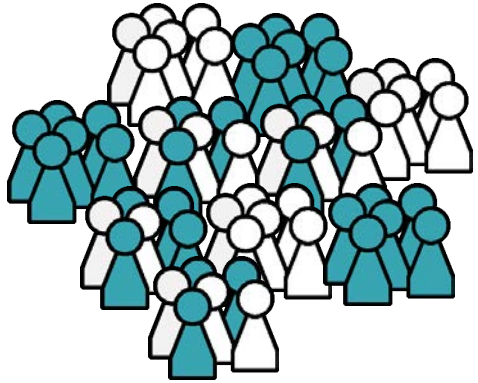
Prof. Dr. Albert Heuberger
- Spokesman of the Fraunhofer Group for Microelectronics and Chairman of the steering committee of the Research Fab Microelectronics Germany
- Executive Director of the Fraunhofer Institute for Integrated Circuits IIS
- Head of the Chair of Information Technologies at the Friedrich-Alexander-Universität Erlangen-Nürnberg

Research Fab Microelectronics Germany

An overview



FMD combines the expertise and infrastructure of **13 research institutes** across Germany and offers developments **along the entire value chain in a one-stop shop.**



FMD at a glance:

3,000 m EUR in assets
3,500 employees FTE,
2,000+ scientists
600 m EUR/yr
250 m EUR/yr from Industry
From TRL2 to TRL8

Total investment of EUR 350 million for additional infrastructure and future developments. (1.4.2017-30.9.2021)

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International establishment of FMD and **cooperation with European partners** (e.g. NGC Alliance).

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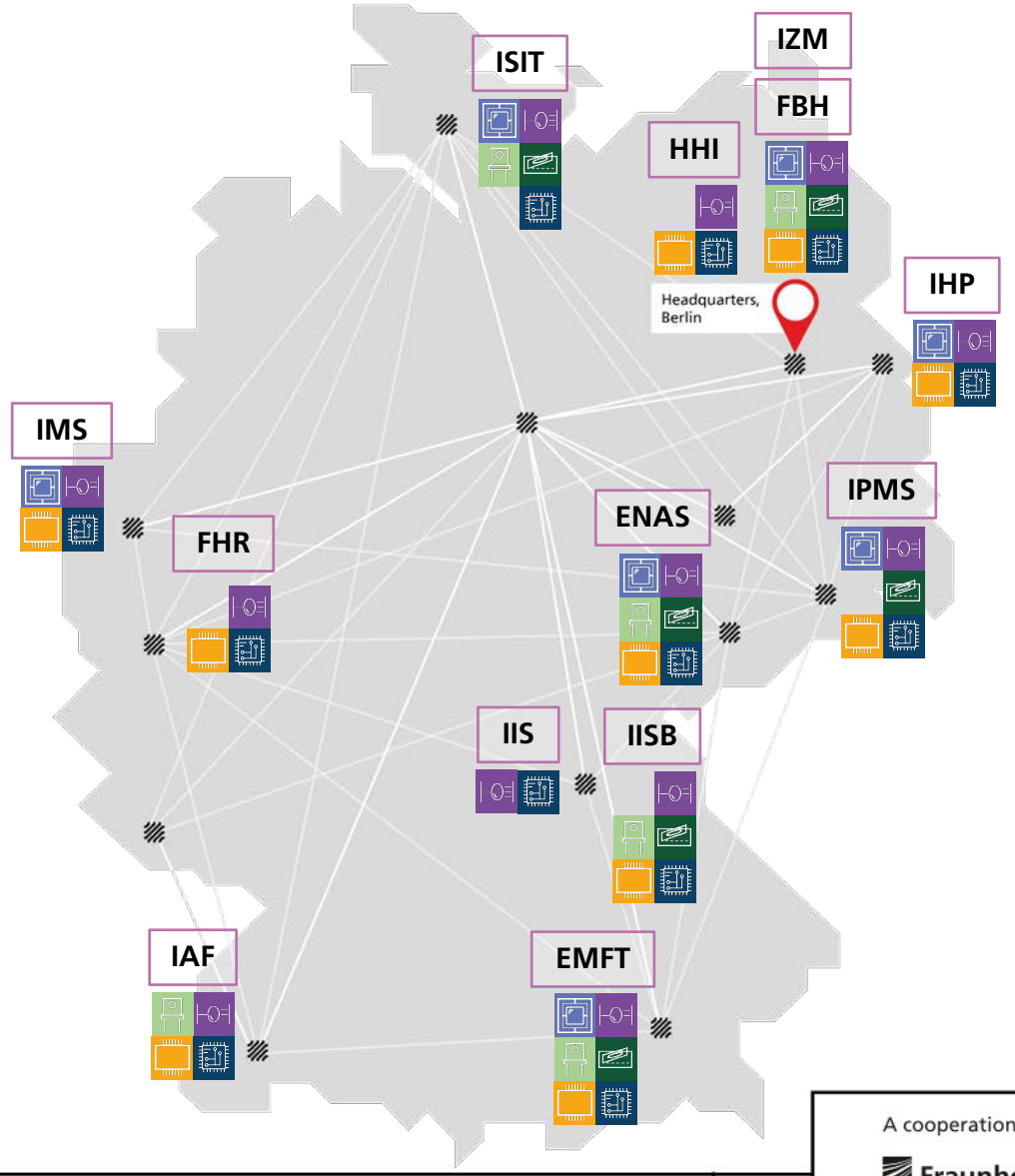
Technology Platforms of FMD

- Extended CMOS
- Optoelectronic Systems
- Power Electronics
- MEMS Actuators
- Microwave and Terahertz
- Sensor Systems

Two other technology platforms are currently under construction:
Advanced System Integration and Advanced System Design



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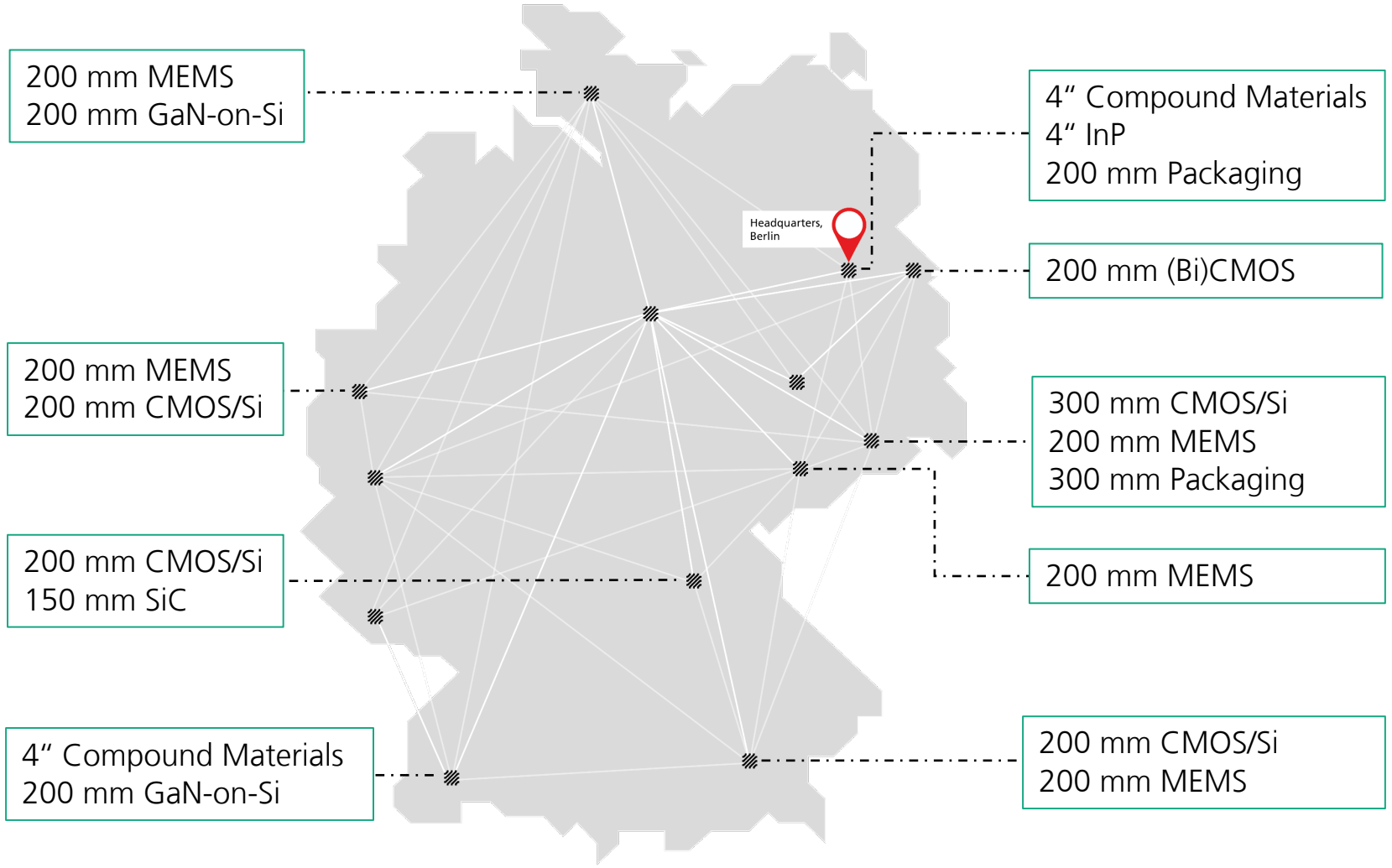
FMD Cleanrooms all over Germany



➢ Operation concepts in alignment

- Over 2.200 equipment in 13 cleanrooms all over Germany
- Over 10 Mio moves per year
- Overall size: appr. 11.000 m^2
- Wafersizes: 2“ till 300 mm

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Organization

Application Specific Solutions

Technology Platforms

FMD as a strong fundament

- 6 specific application topics with collaborative advantage
- 6 technology platforms along the value chain
- 13 member institutes of the Fraunhofer-Gesellschaft and Leibniz-Gemeinschaft all over Germany

- **Transport and Smart Mobility**
- **Digital Industry**
- **Health and Wellbeing**
- **Energy**
- **Digital Life**
- **Civil Security and Occupational Safety**

- **Extended CMOS**
- **Optoelectronic Systems**
- **Power Electronics**
- **MEMS Actuators**
- **Microwave and Terahertz**
- **Sensor Systems**

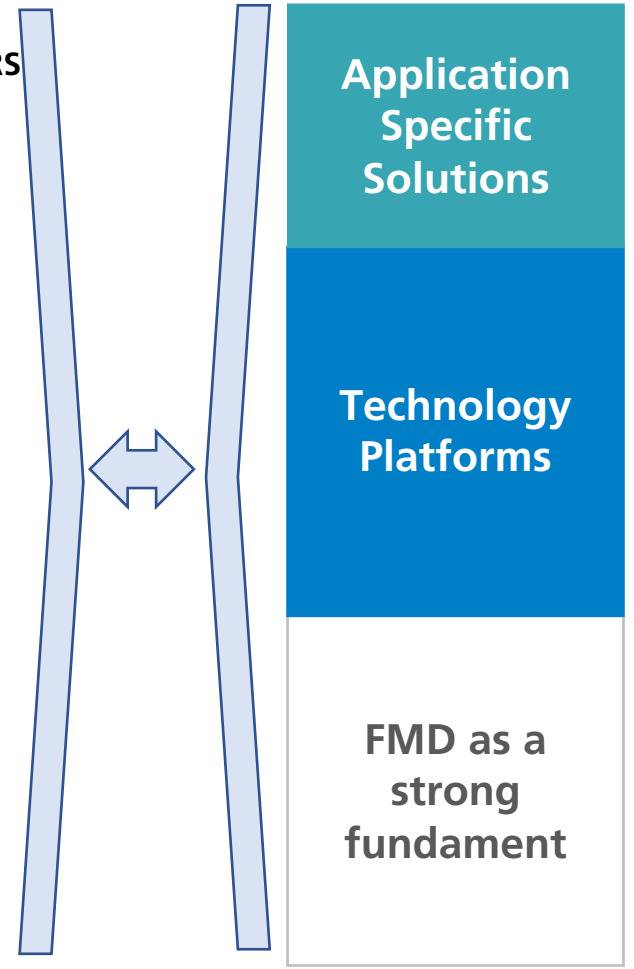
Heterogeneous Integration Roadmap and FMD (Research Fab Germany)

Many synergies between HIR and FMD

IEEE-HIR (Heterogeneous Integration Roadmap)

CHAPTER 2: HIGH PERFORMANCE COMPUTING AND DATA CENTERS
CHAPTER 3: INTERNET OF THINGS (IOT)
CHAPTER 4: MEDICAL, HEALTH & WEARABLES
CHAPTER 5: AUTOMOTIVE
CHAPTER 6: AEROSPACE AND DEFENSE
CHAPTER 7: MOBILE
CHAPTER 8: SINGLE CHIP AND MULTI CHIP INTEGRATION
CHAPTER 9: INTEGRATED PHOTONICS
CHAPTER 10: INTEGRATED POWER ELECTRONICS
CHAPTER 11: MEMS AND SENSOR INTEGRATION
CHAPTER 12: 5G COMMUNICATIONS
CHAPTER 13: CO-DESIGN FOR HETEROGENEOUS INTEGRATION
CHAPTER 14: MODELING AND SIMULATION
CHAPTER 15: MATERIALS AND EMERGING RESEARCH MATERIALS
CHAPTER 16: EMERGING RESEARCH DEVICES
CHAPTER 17: TEST TECHNOLOGY
CHAPTER 18: SUPPLY CHAIN
CHAPTER 19: CYBER SECURITY
CHAPTER 20: THERMAL
CHAPTER 21: SIP AND MODULE SYSTEM INTEGRATION
CHAPTER 22: INTERCONNECTS FOR 2D AND 3D ARCHITECTURES
CHAPTER 23: WAFER-LEVEL PACKAGING (WLP)
CHAPTER 24: RELIABLITY

FMD: Technologies and Applications



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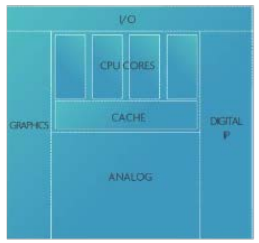
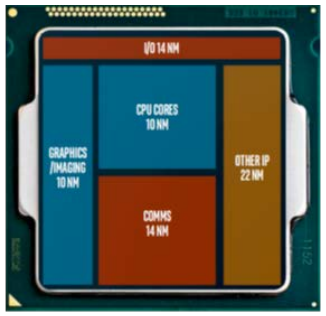
Heterogeneous Integration

Strategy



SoC System on Chip

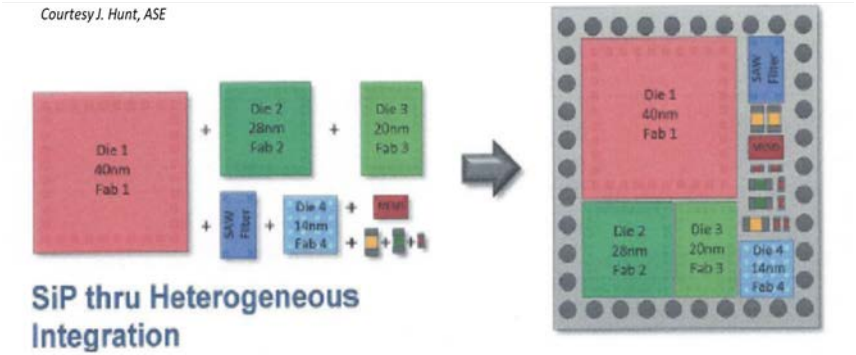


Package Integration

Drivers for Heterogeneous Integration in the HPC Segment

- Die cost per unit area increasing with node shrinks
- Package IO, latency/BW and power constraining

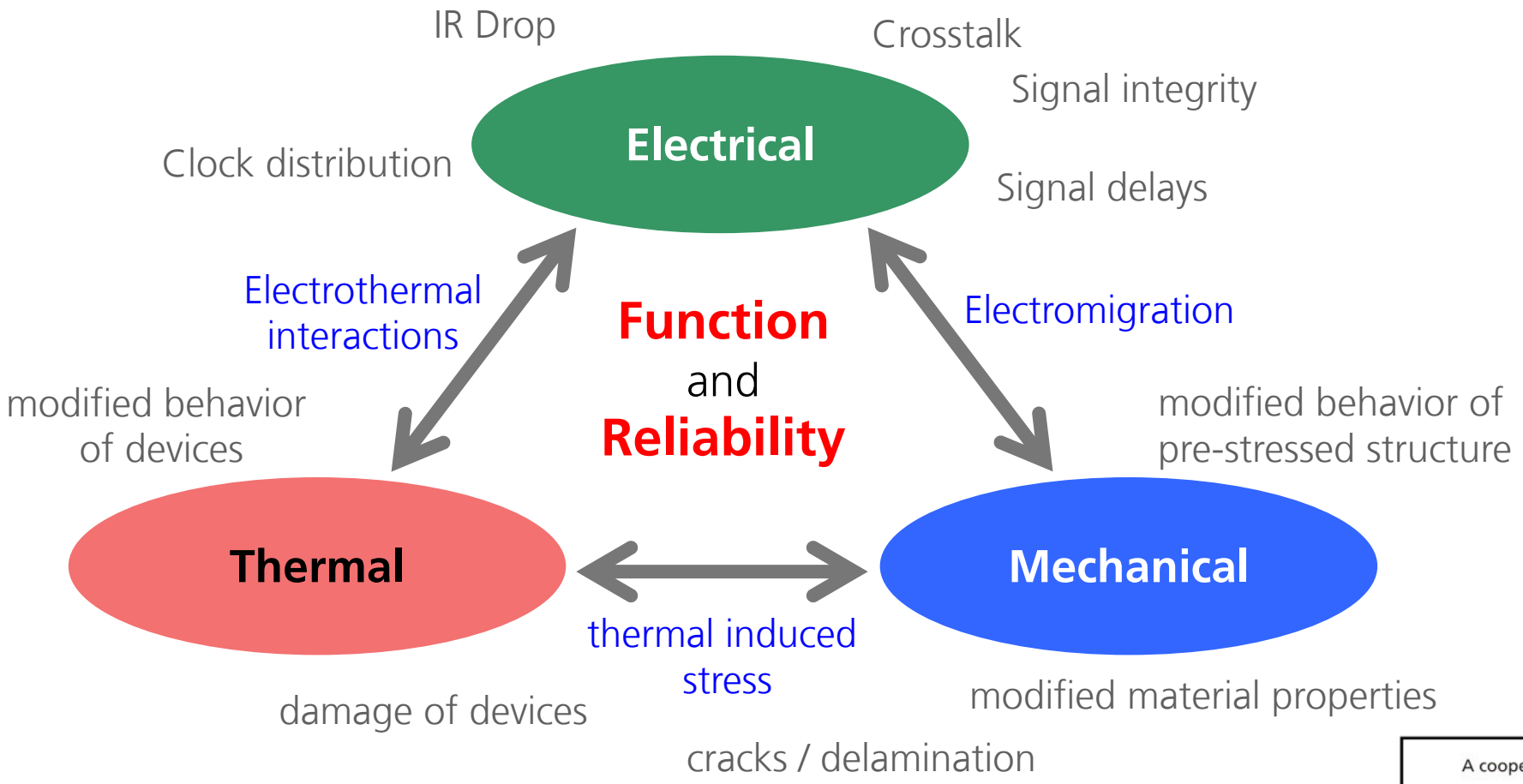
➡ **It is all about transferring data!**



Heterogeneous Integration provides a solution that can be in many formats

- Design
- Wafer-Level Hetero-Integration
- Board-Level Hetero-Integration
- Specific/different applications

Ultra compact miniaturized systems bring new combined physical effects:

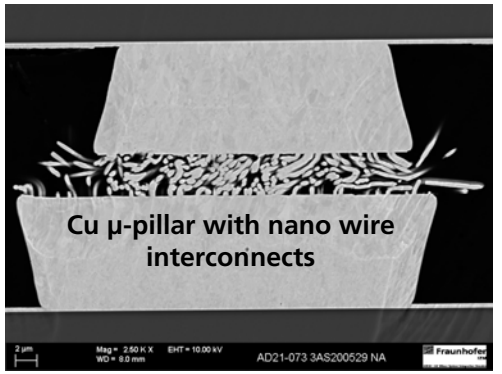


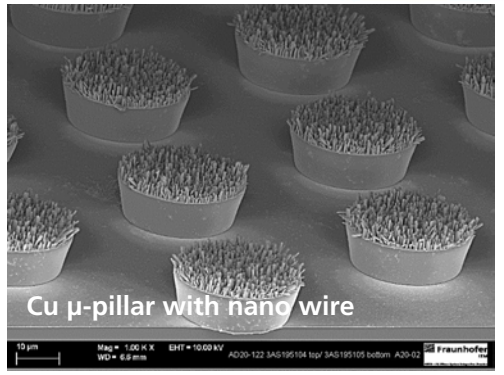
- Influences all design steps across all hierarchy levels
- System design
  - Design space exploration over certain chip and package technologies necessary
  - Chip-package or chip-package-board-co-optimization necessary
    - First tools available to solve parts of the whole problem
- System implementation and system verification
  - Block implementation (analog, digital) can be done by existing flows and tools
  - New methods necessary on the boarder between block implementation
    - Power delivery networks much more complex
    - Interface definition and standardization between different dies

Interconnects for 2D and 3D architectures

Cu-Nano Wire

- Demonstration on 12“ wafer Cu nano wired bumps
- High-density interconnects for D2W and W2W Bonding
- Room temperature bonding, fluxless process, single metal (Cu)

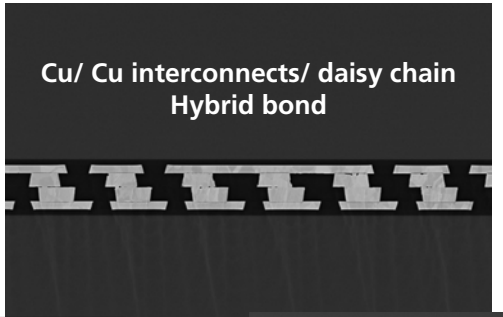


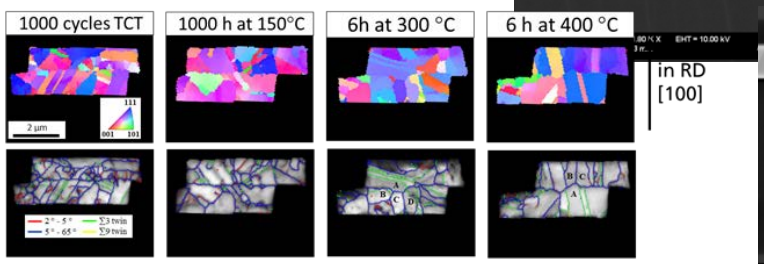


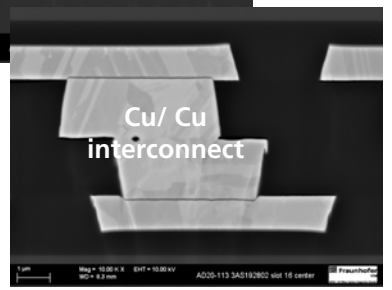
Joint project with NanoWired GmbH

Cu/Cu Hybrid Bonding

- Hybrid bonding on 300mm wafer size qualified
- W2W Bond alignment accuracy (~1µm)
- Bond process established
- Low Temp. processes < 200°C







- EBSD method allows detection of Cu grain intergrowth at interface, which can not be detected only by SEM
- Significant intergrowth of Cu grains after storage at 300 and 400 °C (see interface line, growth of grains at triple points)

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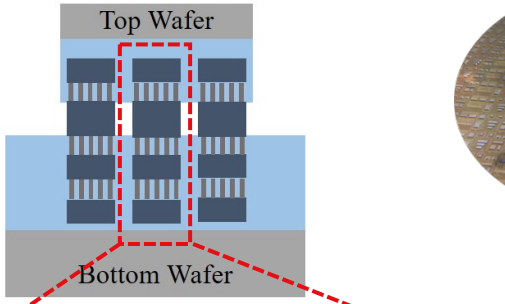
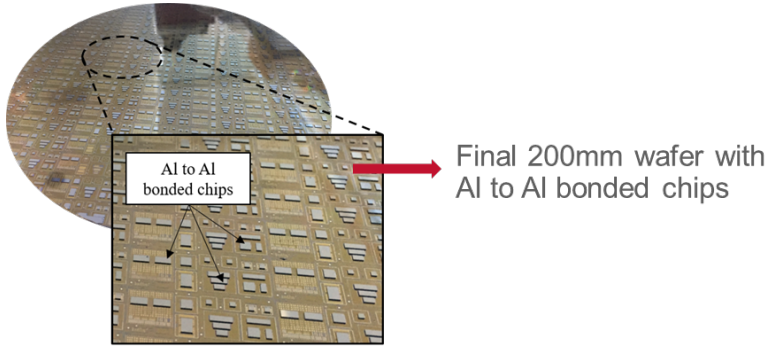
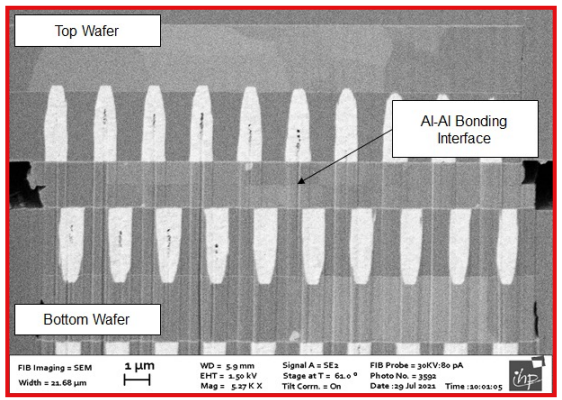
Wafer-Level Hetero-Integration

Wafer-level Heterogeneous Integration for advanced RF applications

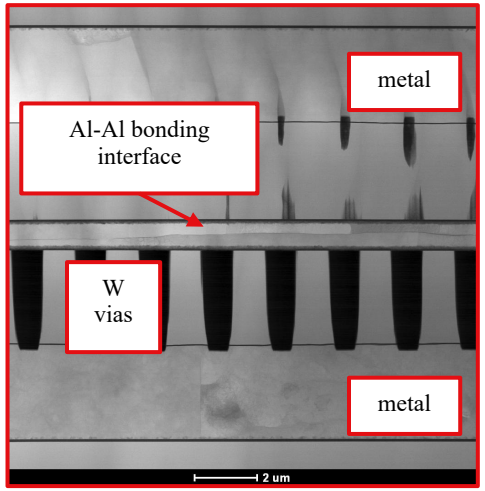
- High-Vacuum Al-Al bonding for 8“ wafer platform
- SiGe-BiCMOS co-integration platform (e.g. on Si-RF-interposer)

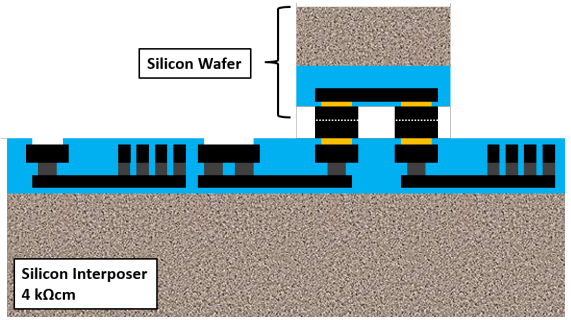




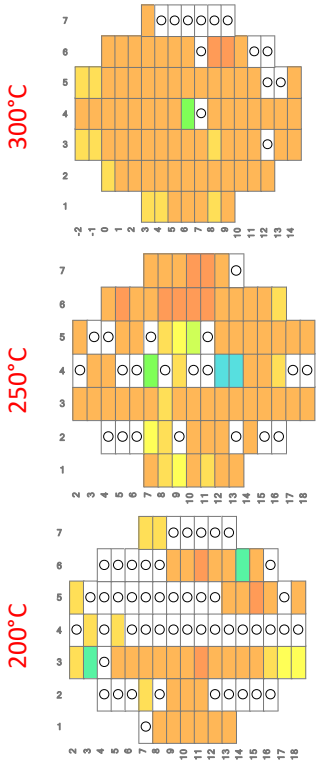


FIB/SEM cross section with 20 µm x 20 µm Al pads bonded at 250 °C for 1 h with 60 kN.





20x20µm² single contacts
Example: Temperature Variation



Yield: 86%
Mean resistance: 35.5mΩ

Yield: 78%
Mean resistance: 37.8mΩ

Yield: 47%
Mean resistance: 38.7mΩ

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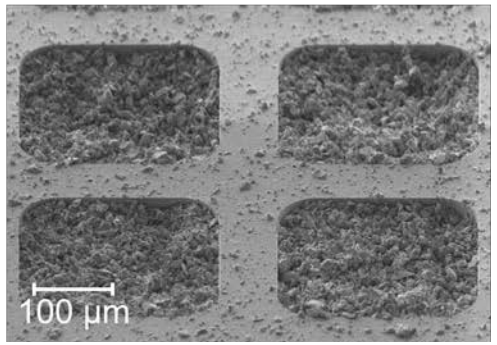
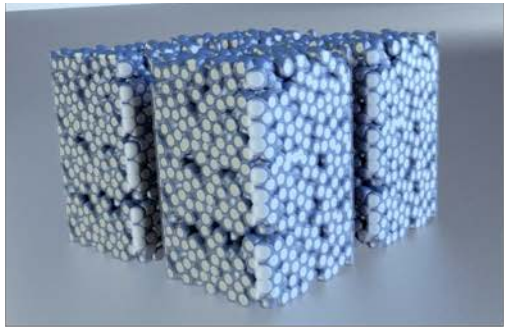
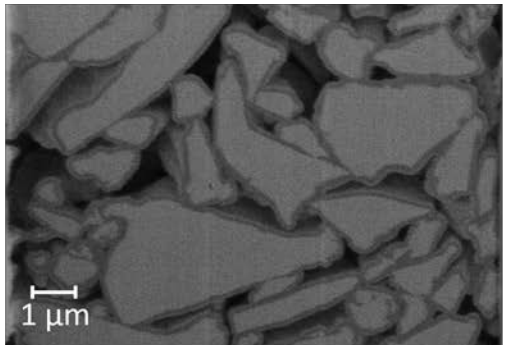
Powder MEMS: substrate-level integration of three-dimensional functional microstructures

1. Dry-filling of micromolds

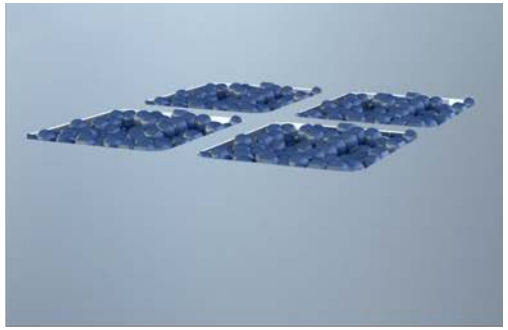


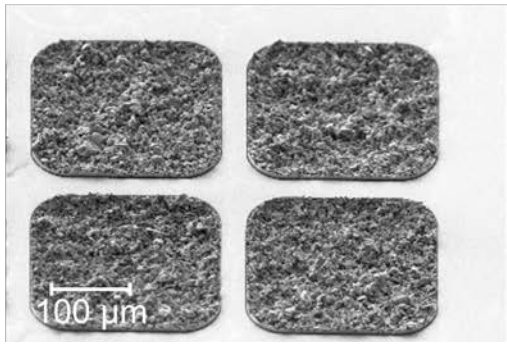
2. Solidification with atomic layer deposition





3. Substrate conditioning for post-processing





Unique set of characteristics:

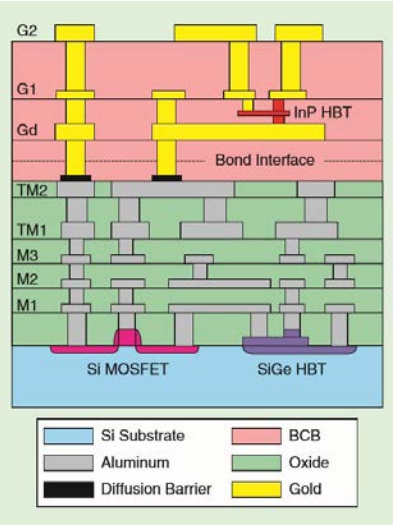
- Wide selection of materials
- Substrate-level integration
- Low process temperature
- No organic binder
- BEOL compatible
- Lateral dim.: 30 – 4000 µm
- Thickness: 30 – 1000 µm

Novel wafer-level integrated microcomponents like 3D micromagnets, porous microfluidic structures etc.

Wafer-Level Hetero-Integration

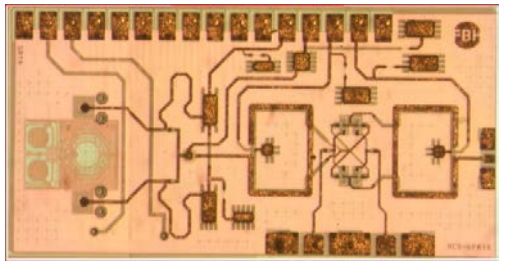
InP-on-BiCMOS

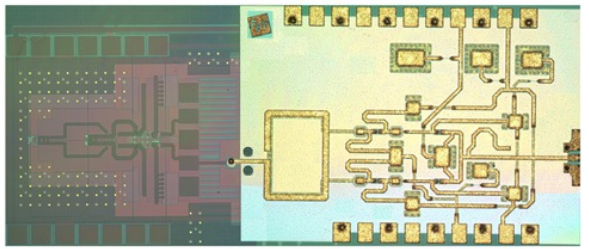
- Combining benefits of III-V technology with BiCMOS
- Integrating InP and BiCMOS circuits on a single chip
  - FBH bipolar InP process
  - IHP BiCMOS process
  - Wafer-bonding and final processing steps in III-V line
- High-frequency performance up to 300 GHz, for 6G and sensors
- Key functions demonstrated
  - Millimeter-wave frequency sources 160 … 330 GHz
  - W-band up-converter and transmitter



Leibniz Ferdinand Braun Institut

innovations for high performance microelectronics





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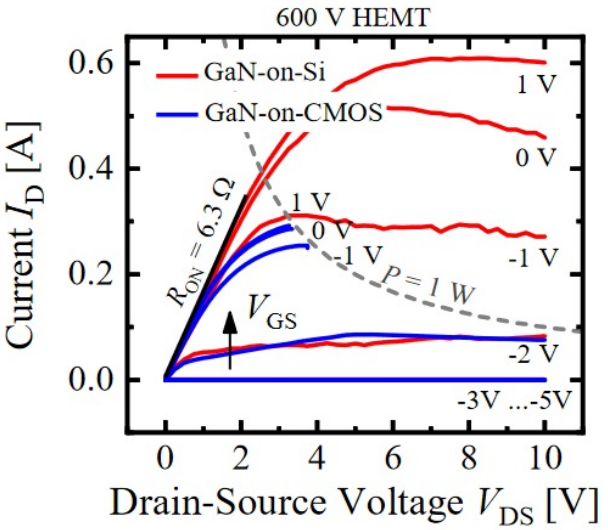
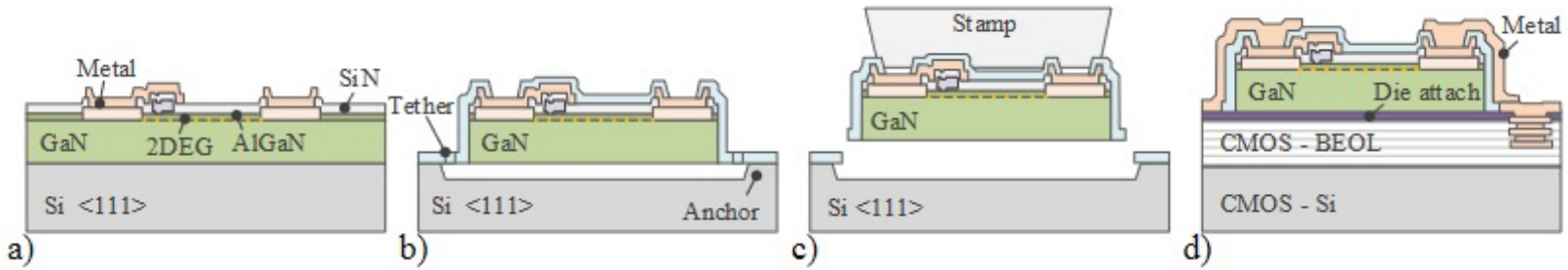
Wafer-Level Hetero-Integration

GaN-HEMTs on CMOS Technology by Micro-Transfer-Printing

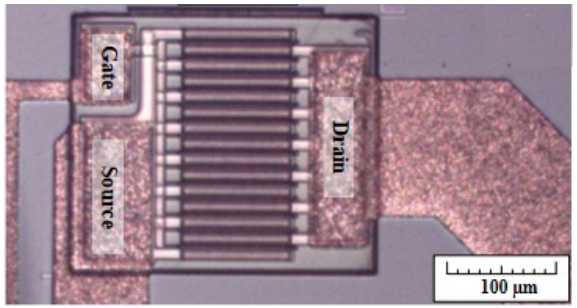
- Monolithic integration of GaN and CMOS devices very challenging due to material and thermal mismatches
- GaN device source wafer, CMOS device target wafer
- Substrate removal of GaN devices and transfer



IV-data on Si and on CMOS



GaN-on-CMOS fabrication steps by transfer printing



Hetero-integrated GaN-HEMT on CMOS

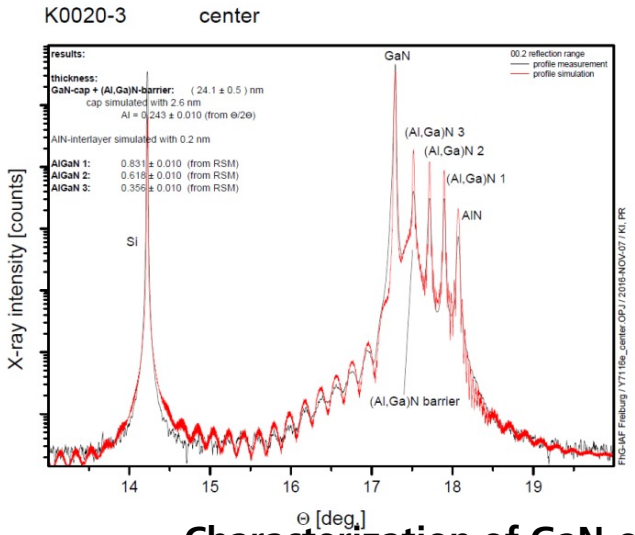
R. Reiner, R. Lerner, P. Waltereit, N. Hansen, S. Moench, A. Fecioru, and D. Gomez, "Characteristics of Hetero-Integrated GaN-HEMTs on CMOS Technology by Micro-Transfer-Printing," 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2021, pp. 323-326

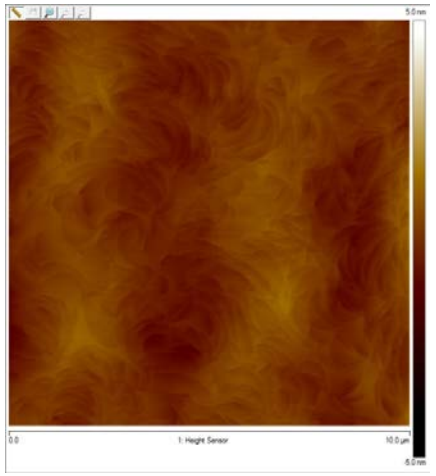
Wafer-Level Hetero-Integration

Epitaxial growth of GaN layers on Si(111) substrates

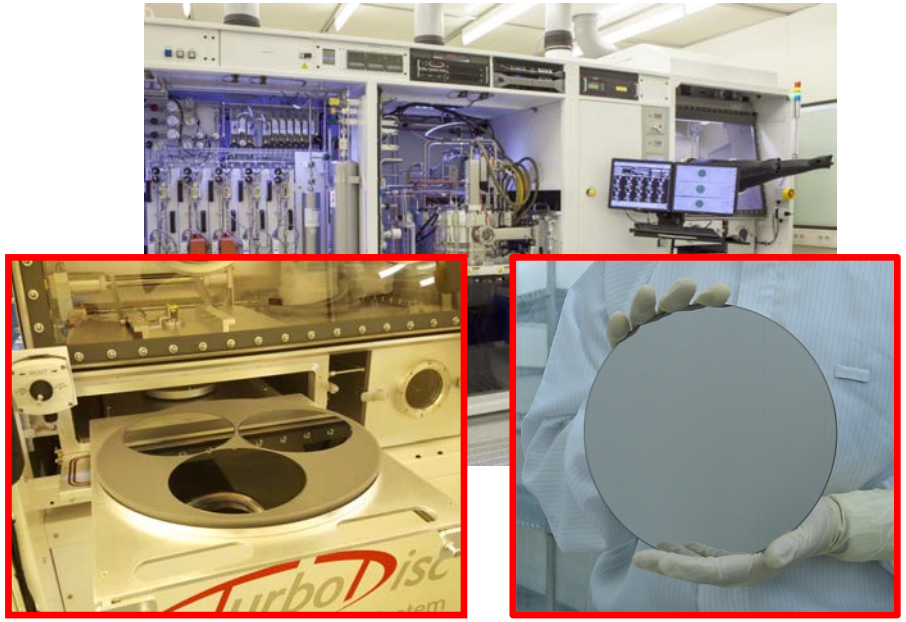
- GaN-based epitaxial films are grown on large area 200 mm Si substrates by MOCVD
- Tuning of growth parameters to compensate lattice and thermal mismatches
- Alternative to expensive high-resistivity SiC substrates
- Integration of III/V material into CMOS fabrication

Layer sequence





Characterization of GaN-on-Si by XRD and AFM

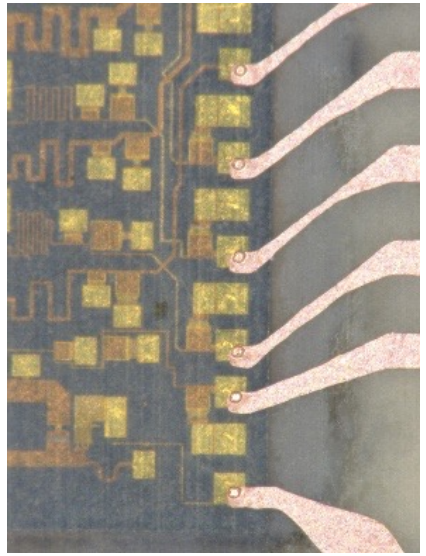


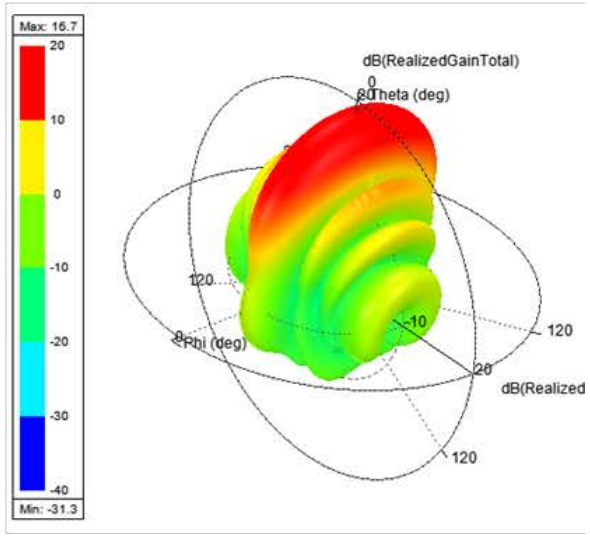
3x200 mm MOCVD reactor for GaN-on-Si devices

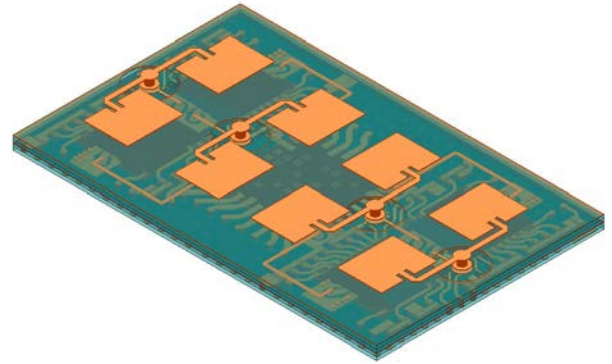
Board-Level Hetero-Integration

PCB Embedding for 5G/Millimeter-Wave Applications

- Integration of antennas with RF front-end enables efficient beamforming and multi-user access at millimeter-wave frequency band
- Approach: PCB embedding of GaN and SiGe ICs in antenna-in-package for scalable 5G front-end module
- RF characterization of embedding technology
- Electrical and thermal design of antenna-in-package modules
- Short interconnect between IC and antenna







TECHNIKON OMMIC innovating with III-V'S EPIGAN ERICSSON Infineon

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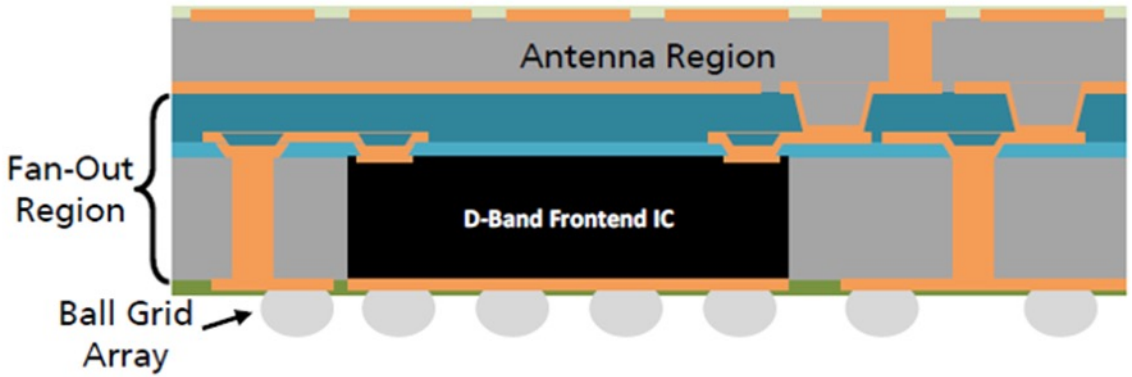
Board-Level Hetero-Integration

Miniaturised HW modules for 6G mobile communication

- **Development of an ultra-broadband and miniaturized massively MIMO D-band HW module with integrated beamforming capability for 6G**
  - Implementation of new baseband architectures taking into account parasitic THz effects in the D-Band module
  - Development of new test procedures and environments for the validation of the modules

D-Band-Module



Industriebeirat

Heraeus, SCHOTT glass made of ideas, isola, contag, Infineon, GlobalFoundries, CREONIC, ROHDE&SCHWARZ, alcan systems, AIRRAYS, TE, ERICSSON, John Deere, Continental The Future in Motion, AIRBUS

Federal Ministry of Education and Research

Technische Universität Berlin, TECHNISCHE UNIVERSITÄT DRESDEN, ihp

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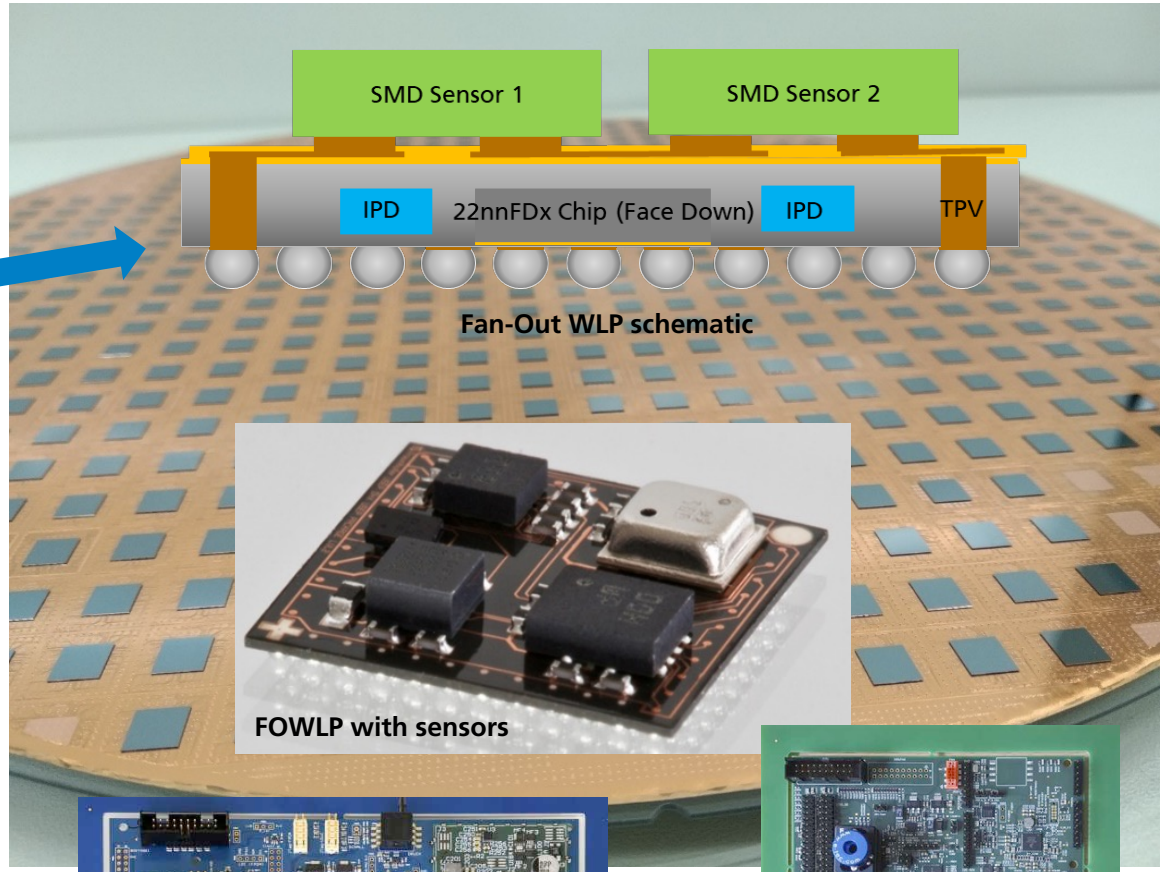
Application: Sensor platform for next generation electronics

Universal Sensor Platform (USEP)

- Development of universal sensor platform (USEP), with which even smaller system providers can shoulder the growing development and production effort for next generation electronics
- Embedded chips
- Package-size: 10mm x 10mm x 0.2mm
- 4 layer thinfilm redistribution
- SMD-assembly of different sensors on top
- Assembly of complete sensor system on evaluation and application boards
- System level validation and functionality demonstration



Fan-Out WLP schematic

FOWLP with sensors

Evaluation board

Application board

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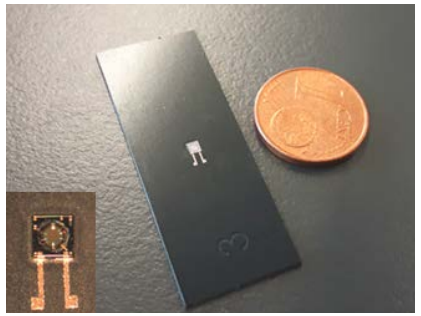
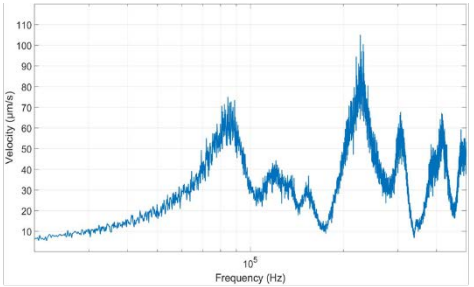
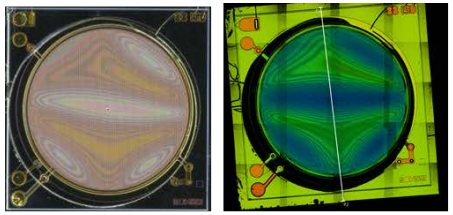
Application: (Ultra)-Sound Interfaces and Low Energy Integrated Sensors

H2020 Project: SILENSE

- Integration of MEMS and ASICs for touchless control and gesture sensing with ink-jet printed conductive tracks
- Adapted process flows under ongoing develoment for
  - MEMS for airborne US with fragile (~300nm thick) membranes

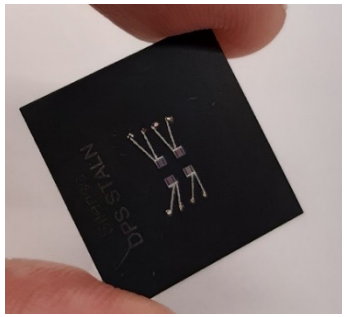


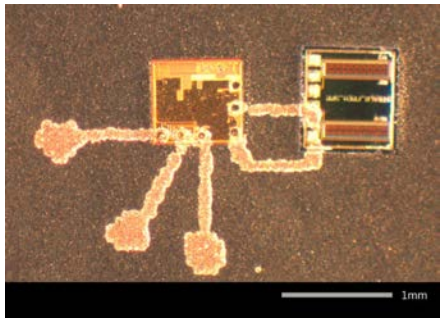




→ Integrity of sensitive membranes demonstrated, stress-decoupling concept under development

  - MEMS for underwater US





→ Adapted process flow demonstrated, performance testing ongoing

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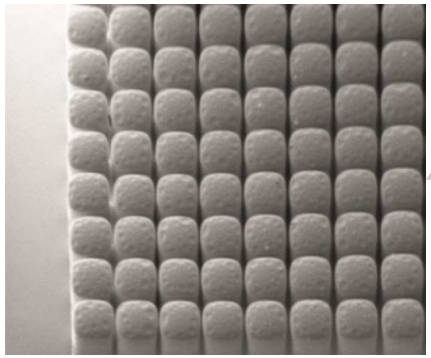
ECSEL Joint Undertaking

A cooperation of

Application: Piezoelectric MEMS Energy Harvester

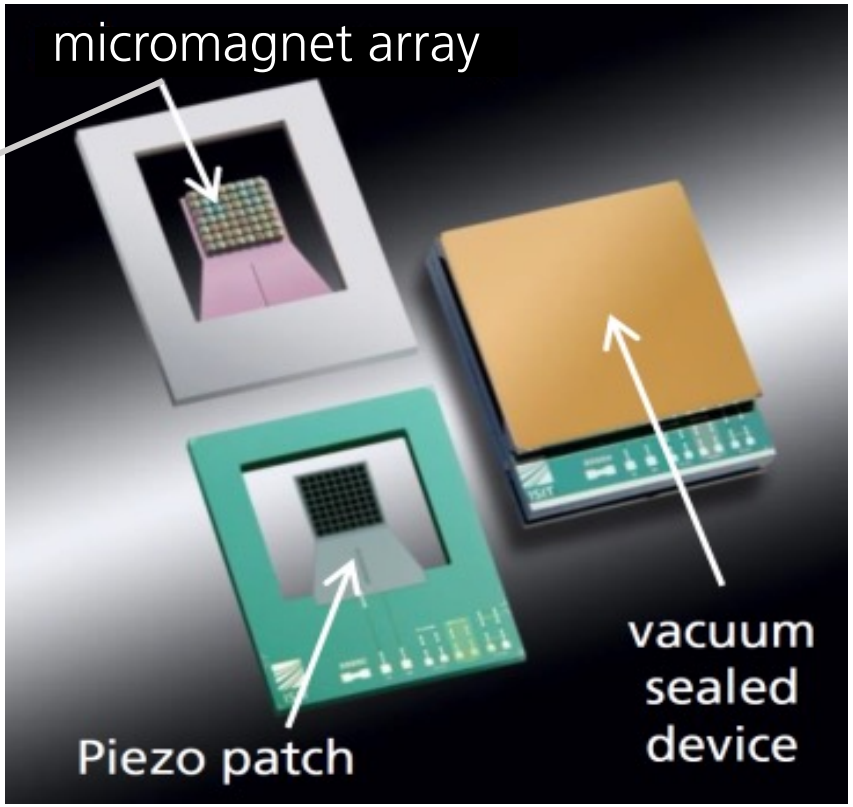
Wafer-level integrated 3D NdFeB micromagnets



NdFeB micromagnet array solidified with Al_2O_3.

Each pixel is 250 x 250 µm² wide and 500 µm high.

Br ≈ 350 mT, Hc ≈ 1 T/μ_0



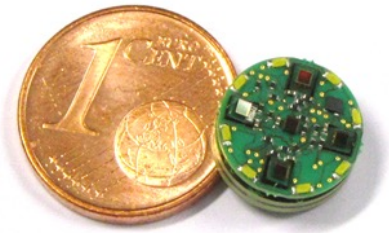
Integrated 3D NdFeB micromagnets allow for

- Contactless magnetic excitation
- Harvesting of rotary and translational movements
- Broadband frequency range (1 Hz – 2 kHz depending on excitation)
- Compact design and high-power density due to high tip density

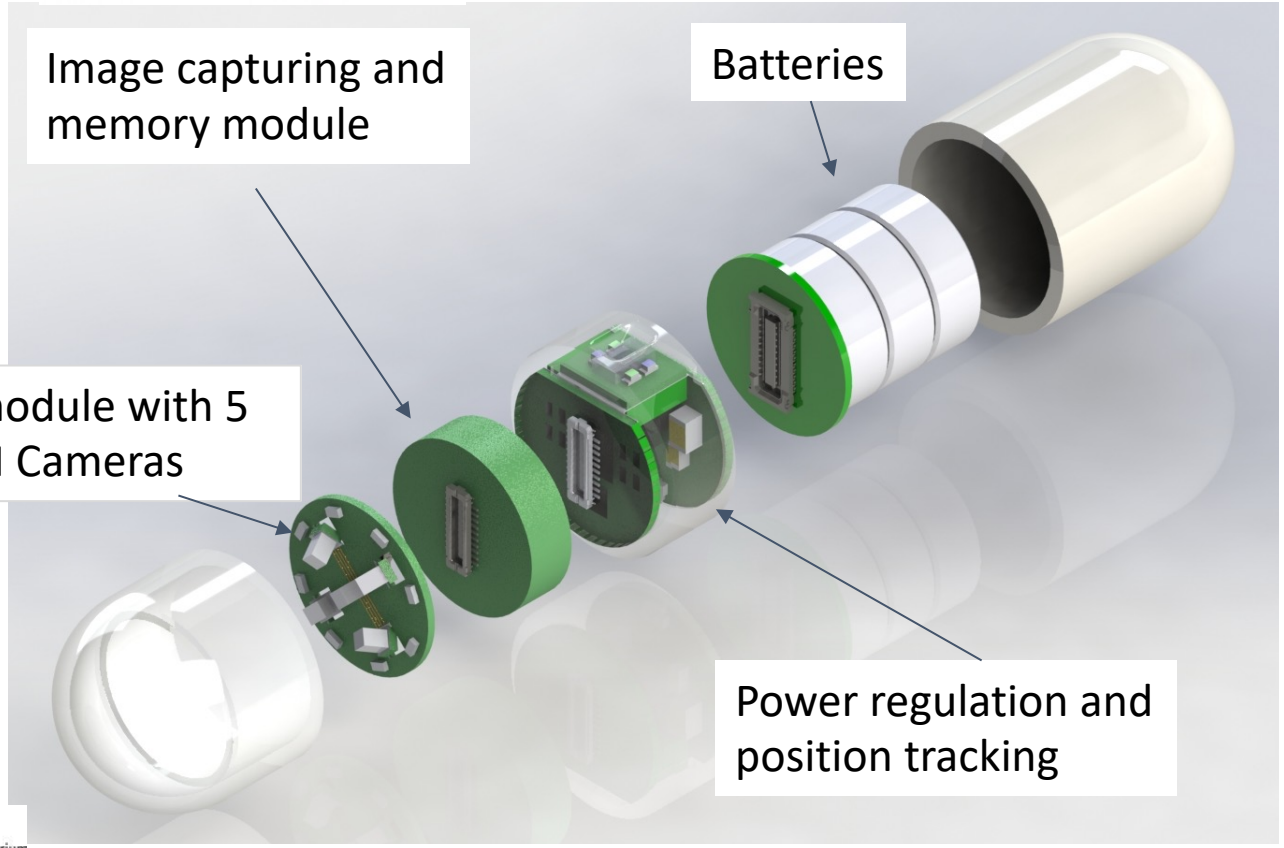
Application: Modular Capsule Endoscopy System

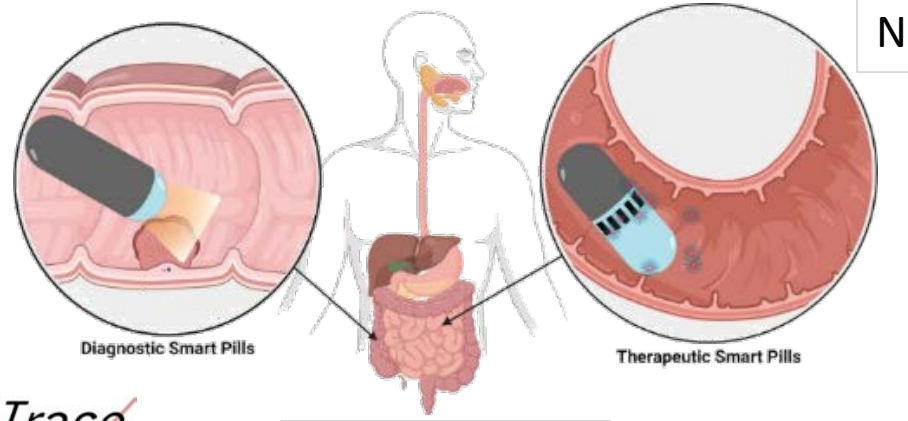
Project EndoTrace

- Use of different miniaturization techniques (e.g. Module stacking, embedding, semi-flex)
- Reduce number of images during the passage through the body (approx. 1/10)
- Onboard image capturing and storage, no external devices needed



Memory / controller module with embedded SMDs





small intestine

endoTrace

GEFÖRDERT VOM Bundesministerium für Bildung und Forschung

amu

ovesco innovation in scope

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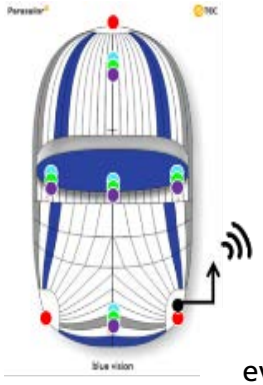
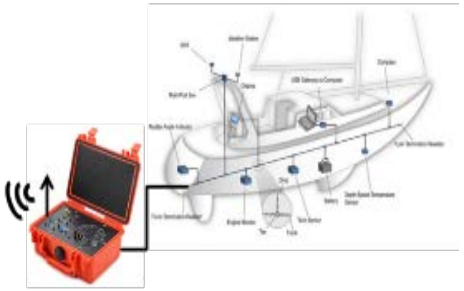
Application: Sensor Systems For High Performance Sails

Project SenSail

- Textile-integrated measuring system (force / pressure / position and orientation in space)
- Development of a bus system adapted to large textiles (~70m²)
- Integration of sensor nodes in a high-performance sail
- Development of a portable and wireless data evaluation unit



sail



portable evaluation unit

Bundesministerium für Wirtschaft und Energie

ZIM Zentrales Innovationsprogramm Mittelstand

Forschungsnetzwerk Mittelstand

ISTEC

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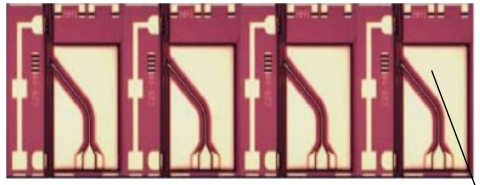
FBH Ferdinand Braun Institut

ihp

Application: Tb/s Transceiver for Intra Data Center Communication

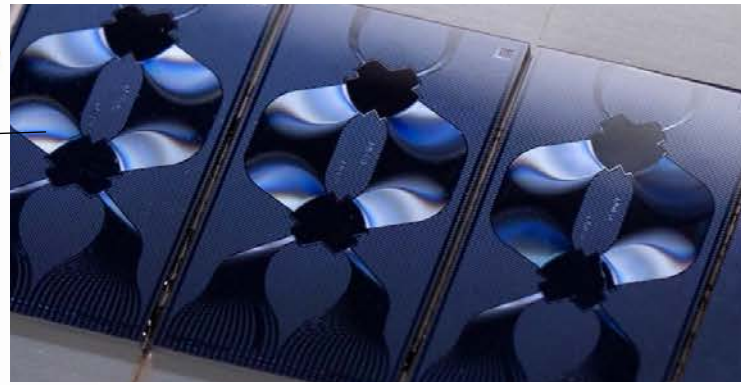
HHI's InP / polymer hybrid integration platform **PolyBoard**

TERIPHIC



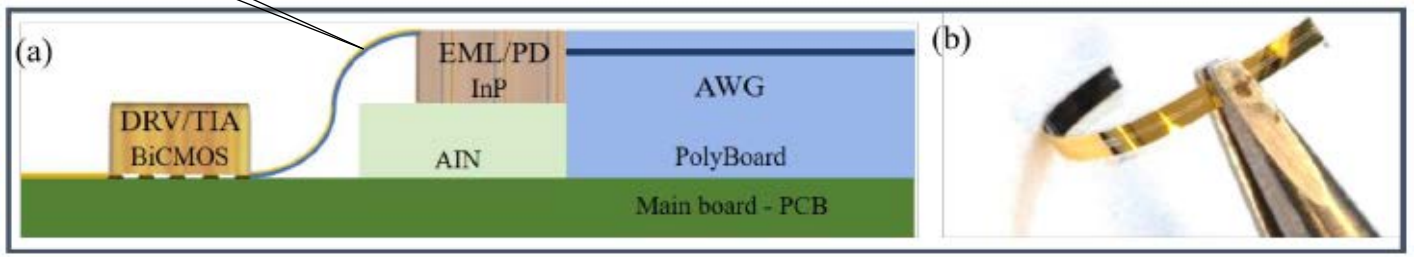
4ch 50 Gbaud EML (electroabsorption modulated laser) array (InP) (O-band)

4ch 50 Gbaud PD (photo diode) array (InP) (O-band)



16ch AWGs (array wave guide) (PolyBoard, O-band))

RF FlexLines for interconnecting PICs with DRVs and TIAs (concept and photo)



TERIPHIC (EU-H2020): Fabrication & assembly automation of terabit optical transceivers based on InP EML arrays and a polymer host platform for optical interconnects up to 2 km and beyond

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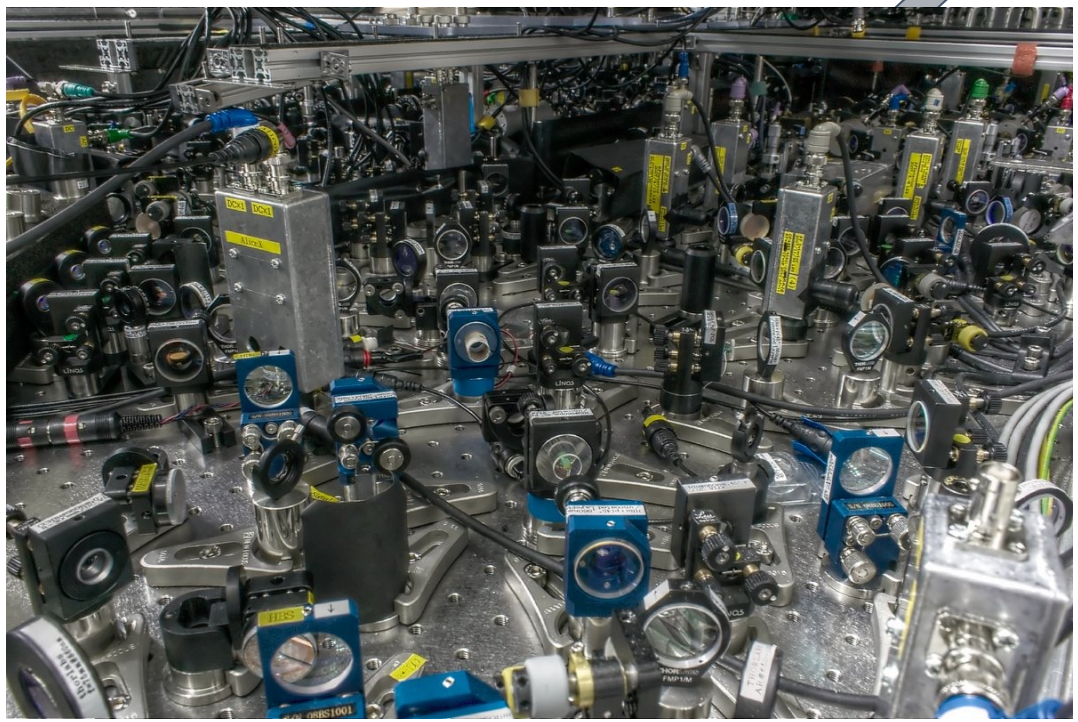
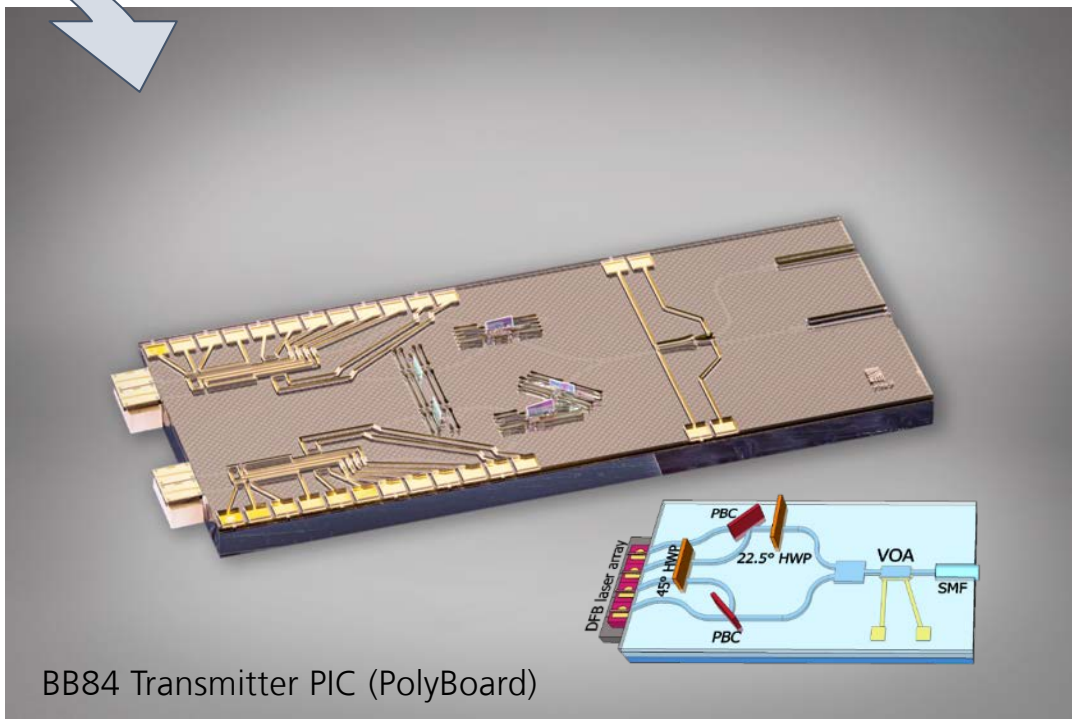
Application: Hybrid qPICs for Quantum Communication

Develop a Quantum System-on-Chip platform (QSoC)





BB84 Transmitter PIC (PolyBoard)

Make Quantum Communication a Commodity

QUANTUM FLAGSHIP

QuNET

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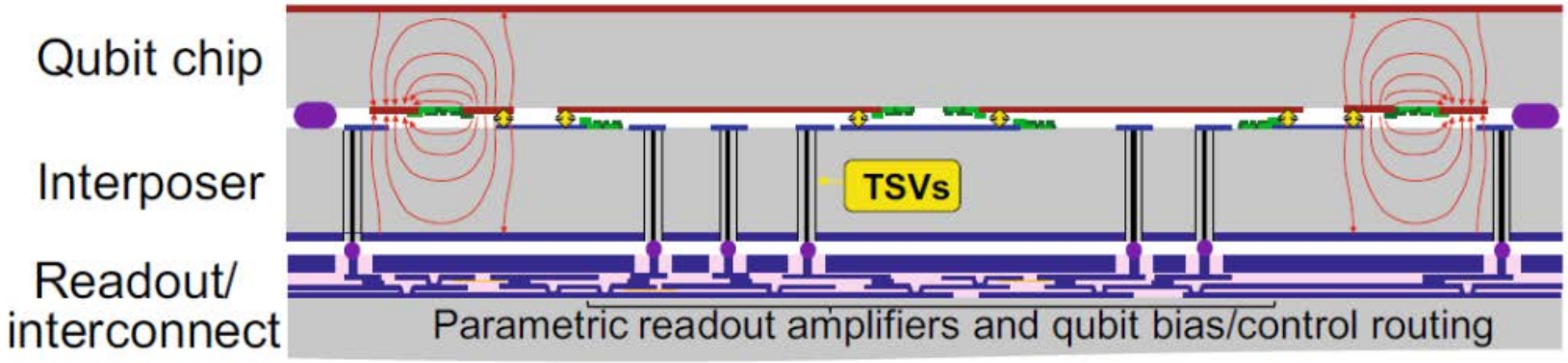
Application: Quantum Computing

Heterogeneous Integration 200 mm

- Heterogeneous Integration for future projects (like MQV Bavaria) at Fraunhofer EMFT
- 3D Heterogeneous Integration for quantum systems



Source: D. Rosenberg et. al; 3D integrated superconducting qubits; npj Quantum Information (2017)

Challenges:

- Introduction of superconducting materials (e.g. In, NbN) for bump and TSV Technology
- Connection to metal lines on flex materials with respect to the cryogenic set-up

Cooperation with EU Partners

TEF Edge-AI Allianz: FMD, IMEC and CEA-Leti

- Building a strong European supply and value chain for new hardware for "Edge AI" applications requires a recognized, strong research alliance
- The Alliance for a "Testing and Experimentation Facility for Edge AI" (TEF Edge AI) provides affordable, fast access for small and medium-sized enterprises and system houses
- Development of necessary hardware technologies and new components to support energy-efficient "green" AI applications ("Get AI off the cloud")
- Open platform for other European partners (excellence and complementarity criteria)
- New European Commission funding programs (2021-2028): "Horizon Europe" (including Key Digital Technologies JU) and "Digital Europe" (program to boost digitalization in Europe)

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Conclusion

- **Co-Design**
  - Chip design needs a close link to the package design to guarantee high performance and reliability
  - Multiple domains with different scaling properties have to be considered
  - Different design libraries are necessary for product development
  - Thermal, mechanical and electrical analysis are the key for high yield
- **New Materials**
  - Mechanical, electrical and thermal interactions of different materials not yet used as default
- **Cost**
  - Complex systems require new packages
    - ➔ Therefore new package platforms like embedding have to be considered
- **Customer Requirements**
  - Reliability and application specific requirements
  - High performance is mostly required in HI-applications
  - Control of temperature requires advanced cooling concepts
- **Test**
  - Application specific tests for complex packages (incl. mixed signal, media, etc.)
  - Electrical, mechanical and thermal aspects are important

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