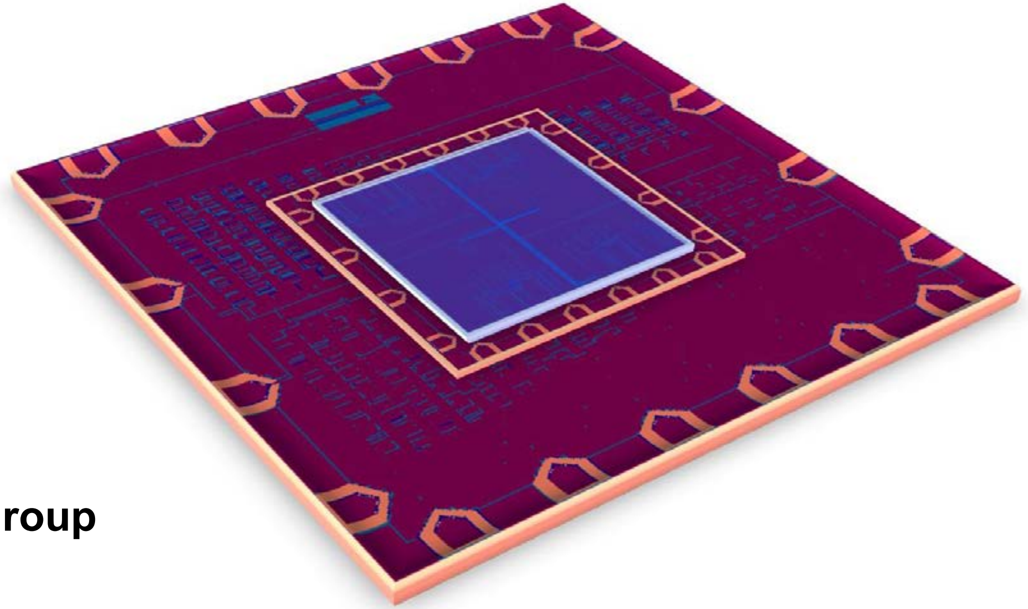
3D Packaging for Superconducting Qubits



Rabindra N. Das

May 13th, 2021

MIT-LL Quantum Information and Integrated Nanosystems Group

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Acknowledgements

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MIT Engineering Quantum Systems (EQuS)

Leadership: John Hybl, William Oliver, Mollie Schwartz, Jonilyn Yoder, Andrew Kerman, Danna Rosenberg, John Rokosz, Michelle Sibiga, Barbara Santorella, Erin Jones-Ravgiala, Lynn Clifford

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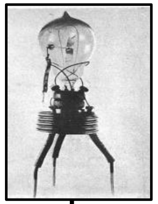
Computing Development Timeline

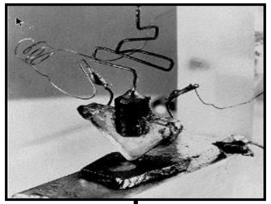
Classical (Electronic) Computing

Vacuum tube (1906)



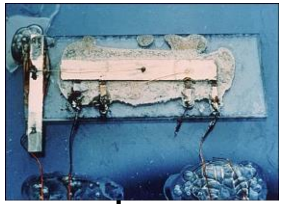
ENIAC (1946)

Transistor (1947)

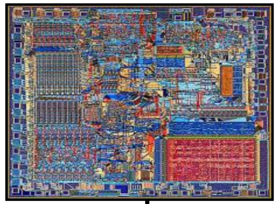


TX-0 (1956)

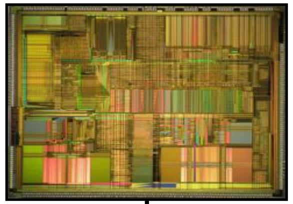
Integrated circuit (1958)



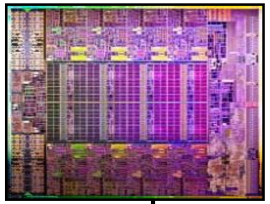
2k transistors i4004 (1971)



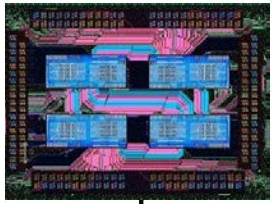
5.5M transistors Pentium Pro (1995)



18 cores 5.5B transistors Xeon Haswell (2014)



32 cores 19.2B transistors Epyc GPU (2017)

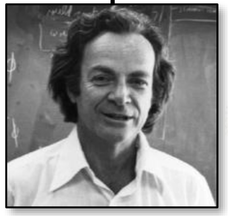


Quantum computing is transitioning from scientific curiosity to technical reality

– Scientific discovery phase (2000-2015)

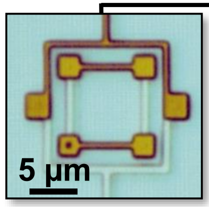
– "Bigger science" & engineering (2015-present)

Quantum Computing

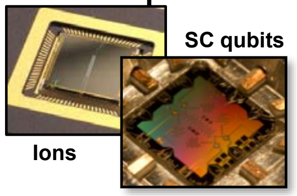


Quantum simulator proposed (1981)

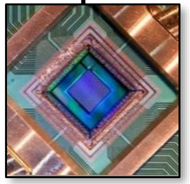
Shor's algorithm (1994)



Initial qubit experiments (1995-2005)



Few-qubit processors & error detection (2012-2016)



Cloud-based quantum computers (2017)

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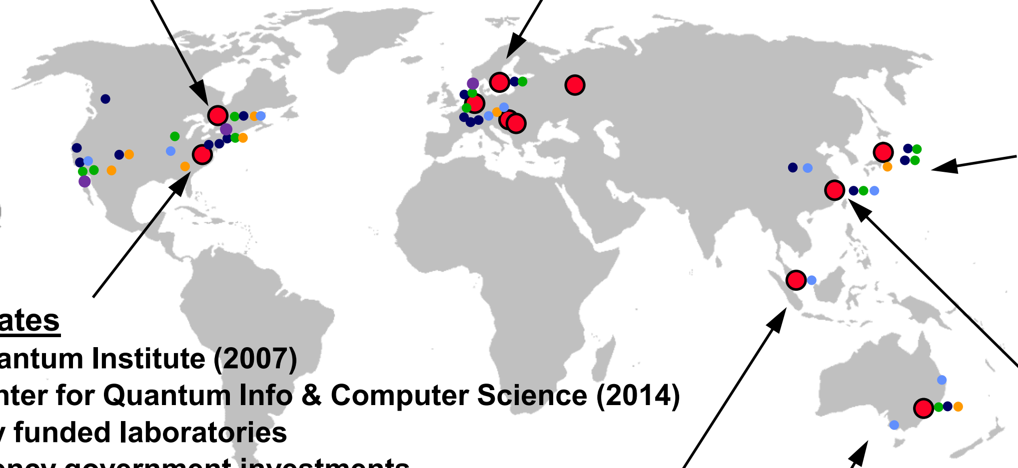
Worldwide Investment in Quantum Computing

(not an exhaustive list)

D-Wave The Quantum Computing Company™ · 1QBit · IBM · Microsoft · qci · intel · IONQ · Google · KEYSIGHT TECHNOLOGIES · rigetti · Raytheon BBN Technologies · NORTHROP GRUMMAN · LOCKHEED MARTIN · Honeywell

Canada
- Inst. for Quantum Computing (2002)
- Inst. Quantique (2015)

Europe
- Austria: Institute for Quantum Optics and Information (2003)
- Netherlands: QuTech (2014)
- United Kingdom: National Quantum Technologies Program (2014)
- EU: Quantum Flagship (2016)



Japan
- Gate-based QC
- Coherent computing: ImPACT program
  - Universities (Tokyo, Osaka, Kyoto, …)
  - Govt. labs (NICT, NII, NTT, RIKEN, …)
  - Industry (Mitsubishi, NEC, Toshiba, …)

United States
- Joint Quantum Institute (2007)
- Joint Center for Quantum Info & Computer Science (2014)
- Federally funded laboratories
- Multi-agency government investments

China
- Key Lab, Quantum Information, CAS (2001)
- Key Lab, Solid-State Microstruct. (2004)
- Satellite quantum communication (2016)

Singapore
- Research Center on Quantum Information Science and Technology (2007)

Australia
- ARC Centers of Excellence
  - Center for Quantum Computing Technology (2000)
  - Engineered Quantum Systems (2011)
- CommBank – Telstra – UNSW (2015)

Zurich Instruments · BlueFors CRYOGENICS · HITACHI · FUJITSU · NEC · Mitsubishi · Baidu · Alibaba.com · Q-CTRL

Potential value of quantum computing for economic and information security is driving significant worldwide investment – currently estimated at $100's Million / year

● Superconducting qubits ● Ion trap qubits ● Semiconducting qubits ● Quantum optics ● NV centers

Outline

- Introduction
- 3D integration Approach
- Superconducting multi-chip module (S-MCM)
- Flip-Chip Qubit
- Semiconductor Vs Superconducting Packaging
- Summary

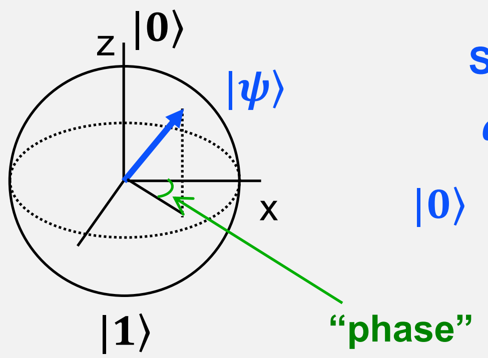
Why is a Quantum Computer Potentially So Powerful?

	Classical Computer	Quantum Computer
Logic element	"Bit" : classical bit (transistor, spin in magnetic memory, …)	"Qubit" : quantum bit (any coherent two-level system)

State

Classical Computer: 0 "Or" 1

Quantum Computer:



Superposition:

$\alpha|0\rangle + \beta|1\rangle$

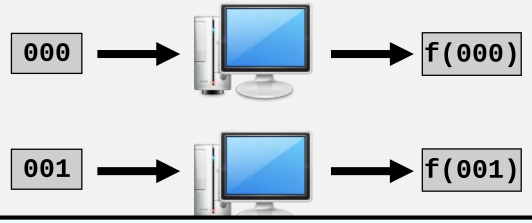
$|0\rangle$ "and" $|1\rangle$

Computing

Classical Computer:

- N bits: *One of* 2^N possible N-bit states

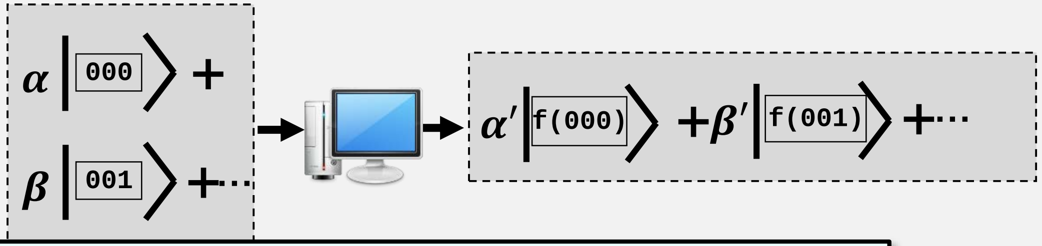
  000, 001, …, 111 (N = 3)
- Change a bit: new calculation (classical parallelism)



Quantum Computer:

- N qubits: 2^N components to one state

  $\alpha|000\rangle + \beta|001\rangle + \cdots + \gamma|111\rangle$ (N = 3)
- Quantum parallelism & interference



Quantum computers encode information in a fundamentally different way than classical computers

Quantum Race

Intelligent Machines

IBM Raises the Bar with a 50-Qubit Quantum Computer

Researchers have built the most sophisticated quantum computer yet, signaling progress toward a powerful new way of processing information.

by Will Knight November 10, 2017

IBM's 50-qubit machine.

11

IBM established a landmark in computing Friday, announcing a quantum computer that handles 50 quantum bits, or qubits. The company is also making a 20-qubit system available through its cloud computing platform.

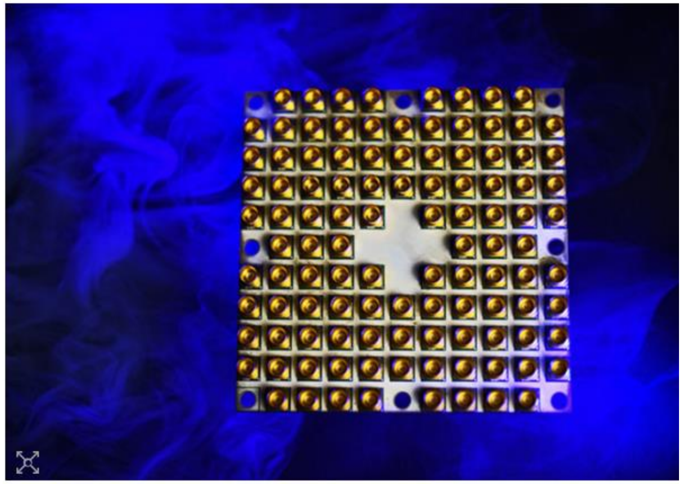
IBM, Google, Intel, and a San Francisco startup called Rigetti are all currently racing to build useful quantum systems. These machines process information in a different way from traditional computers, using the counterintuitive nature of quantum physics.

The announcement does not mean quantum computing is ready for common use. The system IBM has developed is still extremely finicky and challenging to use, as are those being built by others. In both the 50- and the 20-qubit systems, the quantum state is preserved for 90

QUANTUM COMPUTING | NEWS

Intel unveils 49-qubit superconducting chip

18 Jan 2018



Intel's 49-qubit Tangle Lake quantum processor (Courtesy: Intel)

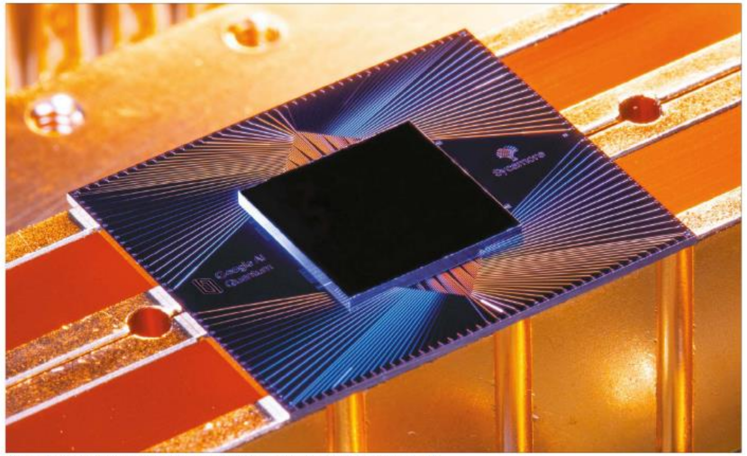
Intel has announced the design and fabrication of a 49-qubit superconducting quantum-processor chip at the Consumer Electronics Show in Las Vegas. Speaking at the conferen Intel chief executive Brian Krzanich introduced "Tangle Lake"; a quantum-processor chip operates at extremely low temperatures. The device takes its name from the Tangle Lake frigid chain of lakes in Alaska, and is a nod to quantum entanglement.

Tangle Lake is designed to store and process quantum information in qubits that are superconducting circuits. Krzanich said that the chip is an important step towards develo quantum computers that could quickly solve mathematical problems involved in some of society's most pressing issues – from drug development to climate forecasting.

Large-scale integration

He also announced progress in Intel's research on spin qubits, which have qubits based c the spin states of single electrons. While superconducting chips tend to be relatively large spin-qubits could be miniaturized using well-established silicon-chip fabrication processes This means that it may be possible to manufacture quantum processors containing large numbers of spin qubits. This large-scale integration would be could be more difficult for

News in focus



ERIK LUCERO

The Sycamore chip is composed of 54 qubits, each made of superconducting loops.

GOOGLE PUBLISHES LANDMARK QUANTUM SUPREMACY CLAIM

The company says that its quantum computer is the first to perform a calculation that would be practically impossible for a classical machine.

By Elizabeth Gibney

Scientists at Google say that they have achieved quantum supremacy, a long-awaited milestone in quantum computing. The announcement, published in *Nature* on 23 October, follows a leak of an early version of the paper five weeks ago, which Google did not comment on at the time.

In a world first, a team led by John Martinis, an experimental physicist at the University of California, Santa Barbara, and Google in Mountain View, California, says that its quantum computer carried out a specific calculation that is beyond the practical capabilities of regular, 'classical' machines (F. Arute *et al. Nature* **574**, 505–510; 2019). The same calculation would take even the best classical supercomputer 10,000 years to complete, Google estimates.

Quantum supremacy has long been seen as a milestone because it proves that quantum computers can outperform classical computers, says Martinis. Although the advantage has now been proved only for a very specific case, it shows physicists that quantum mechanics works as expected when harnessed in a complex problem.

"It looks like Google has given us the first experimental evidence that quantum speed-up is achievable in a real-world system," says Michelle Simmons, a quantum physicist at the University of New South Wales in Sydney, Australia.

The feat was first reported in September by the *Financial Times* and other outlets, after an early version of the paper was leaked on the website of NASA, which collaborates with Google on quantum computing, before being quickly taken down. At that time, the company did not confirm that it had written the paper, nor would it comment on the stories.

Although the calculation Google chose – checking the outputs from a quantum random-number generator – has limited practical applications, "the scientific achievement is

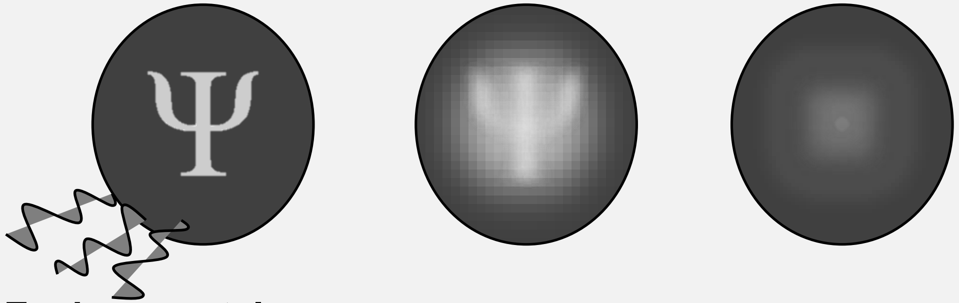
Qubit Quality

Gate time: Time required for a single operation

- All computers require fast logical operations
- Classical processor: ~1 GHz (1 ns per operation)

Coherence time: The qubit's lifetime

Quantum state | State decaying | State lost

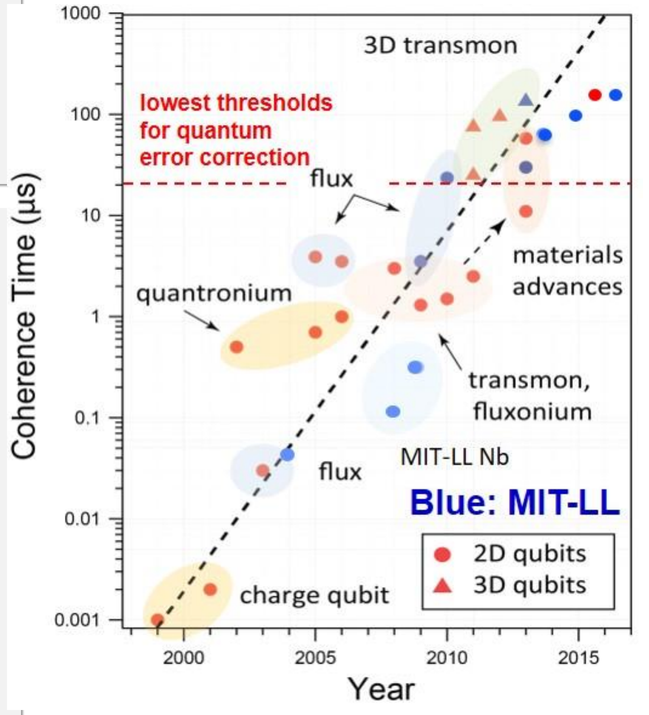


Environmental disruptions

Time →

Figure of Merit: (Coherence time) / (Gate time)

Superconducting Qubit Coherence



Oliver & Welander, MRS Bulletin (2013)

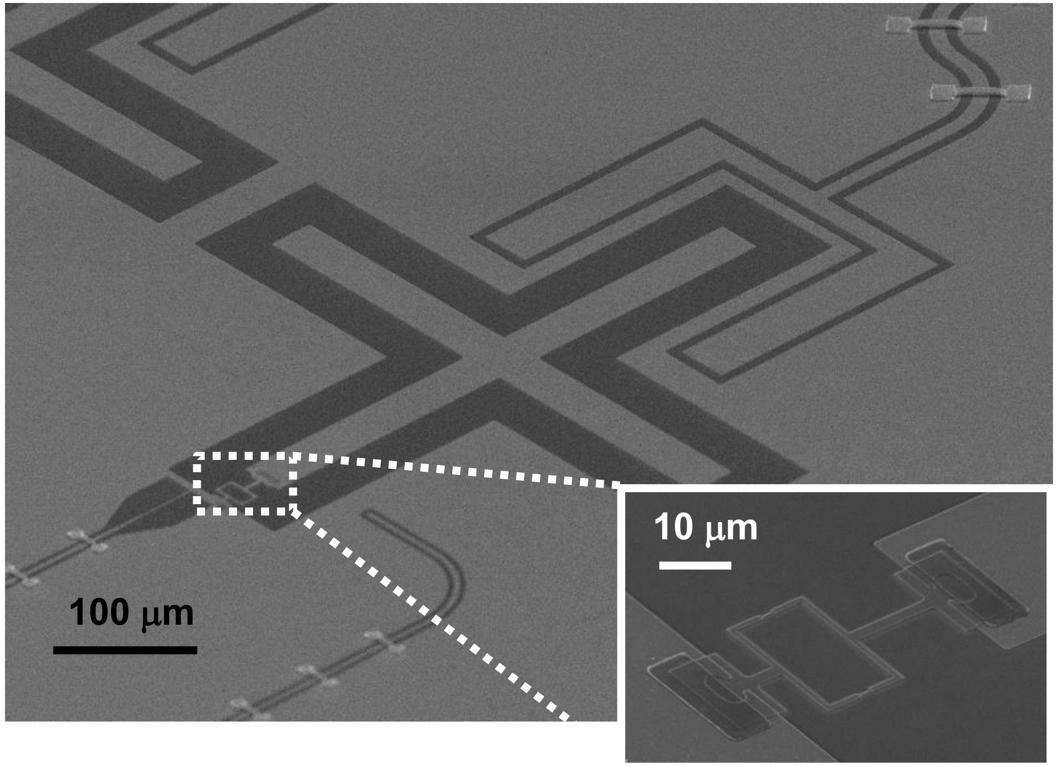
Most lenient threshold for quantum error correction (to sustain computation): $>10^3$ operations per qubit lifetime

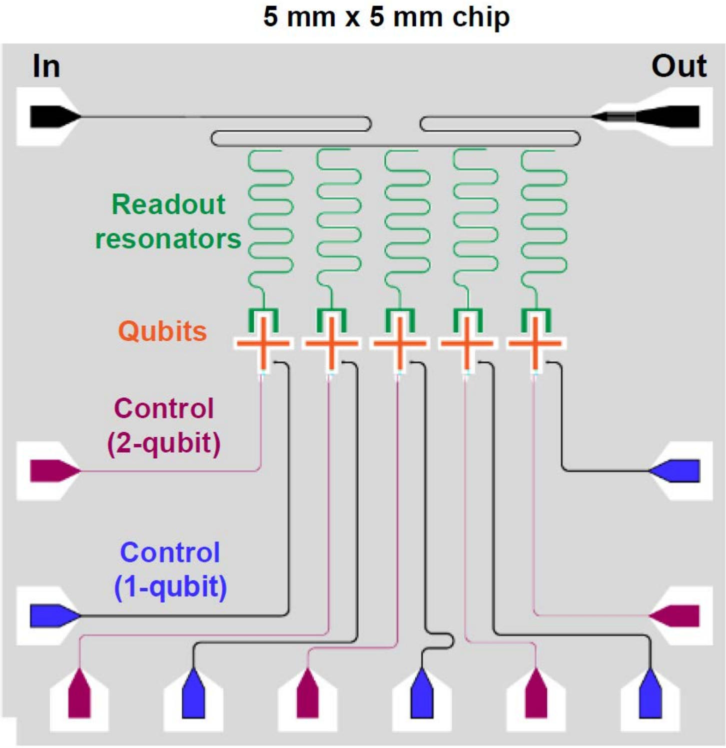
Objectives

Develop 3D qubit integration process with the following attributes:

- Extensible approach
- Compatible with qubit design and fabrication
- Maintain qubit quality

Why 3D Integration Approach?





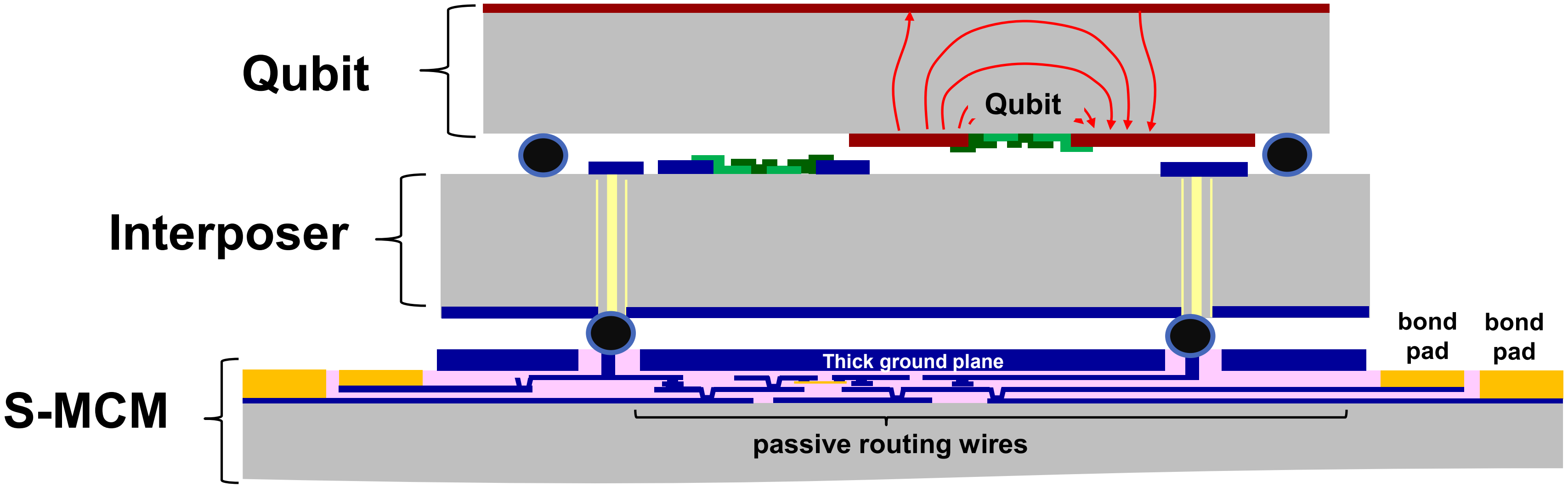
Example:
1X5 transmon-style qubit array

Each qubit requires control bias lines and read out resonator

- **Planar architecture: Increase qubit array by increasing chip size.**
- **3D integration helps to integrate more qubits and connectivity by relegating the routing of readout and control lines to the third dimension.**

M. Kjaergaard, *et al*., Ann. Rev. CMP 2020

3D Integration Approach

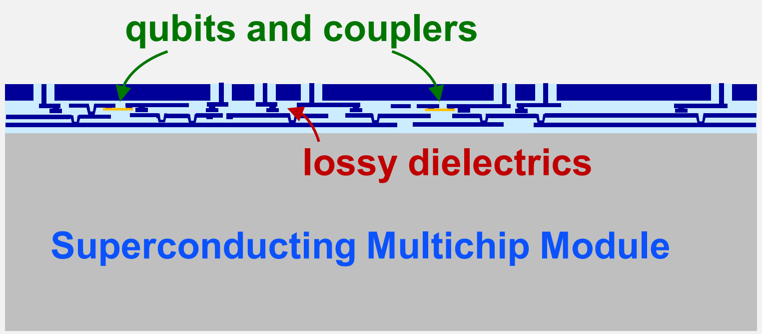


- All Si Technologies
- Fabricate and optimize all layers/chips/devices separately
- Join sequentially and Interconnect with superconducting Indium bumps

3D Integration Approach

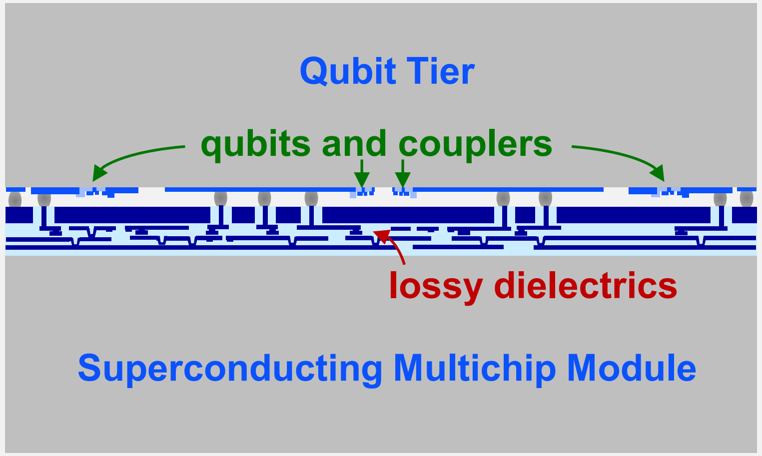
Monolithic Multilayer Wiring with Niobium Trilayer JJs

Qubit coherence limited to <100 ns due to lossy dielectrics



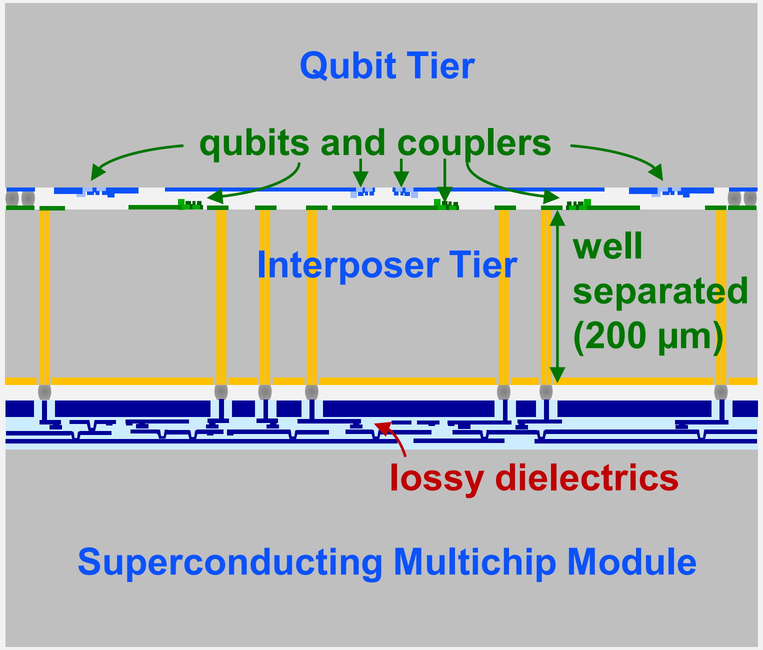
Flip-Chip Integration

Limited mitigation of interactions between qubits and routing-tier dielectrics



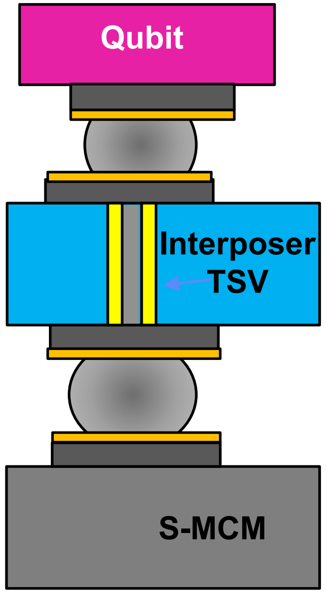
3-Tier Stack

Large qubit mode volume supports high connectivity and maintains high coherence

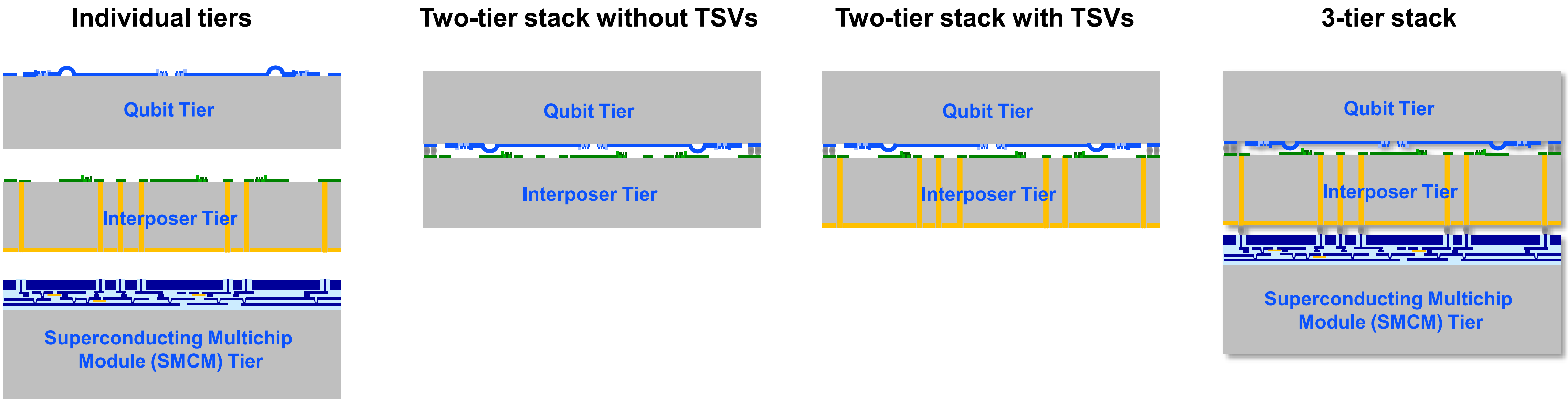


Advantages of 3D Integration Approach

- **Qubits, interconnects, control circuits are optimized separately, independently.**
- **Access to dense wiring layers through the interposer that isolates qubits from lossy surfaces. Thick interposer provides large mode volume to reduce effects of surface losses**
- **3D integration with superconducting TSV interrupted resonator helps to reduce quantum circuit footprint/ form factor.**
- **Possible to integrate best superconducting qubits and components. Possible to combine multiple technologies fabricated using different process.**



Integration Scheme



Enables:

- Rapidly prototype designs
- Validate new fab capabilities

- Off-chip readout and control to reduce cross-talk
- Increased routing and JJ complexity

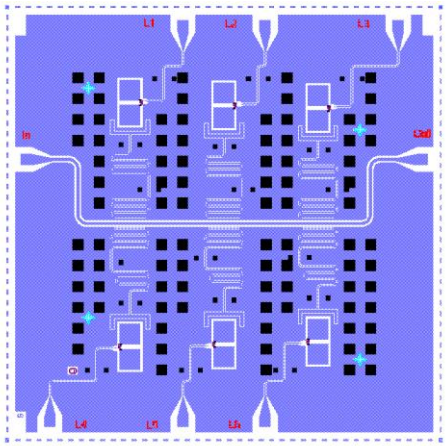
- Additional routing complexity
- Prototype three-tier stack

- High density interconnects
- Trilayer JJs for additional circuit complexity

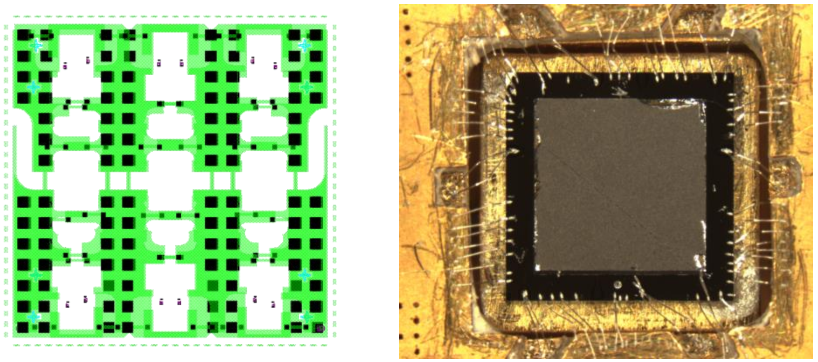
Hirjibehedin, Yost, Yoder, *et al.*, *in preparation* (2021)
Yost, Schwartz, Mallek, *et al.*, *npj Quantum Information* (2020)
Das, *et al.*, *IEEE ECTC* 504-1414 (2018)
Rosenberg, *et al.*, *IEEE Microwave* 21:8, 72-86 (2020)

Key Demonstration for Qubits

Six Identical Qubits Coupled to Quarter Wave Resonators

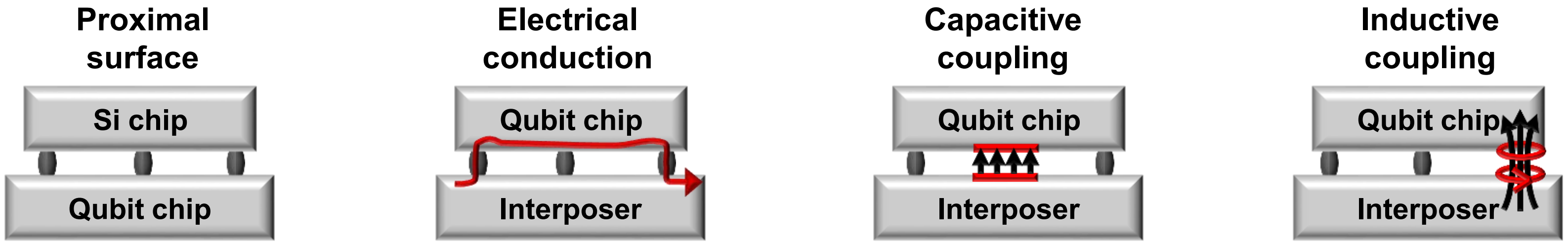


Packaged Qubit with Flip-Chip Bonded on Top



- Characterized effects of proximity of Si surface
- Established low-resistance interconnect path between interposer and Qubit chip.
- Demonstrated capacitive coupling between interposer and qubit chip
- Demonstrated inductive coupling between interposer and qubit chip

Demonstrated Key Flip-Chip Bonding Building Blocks

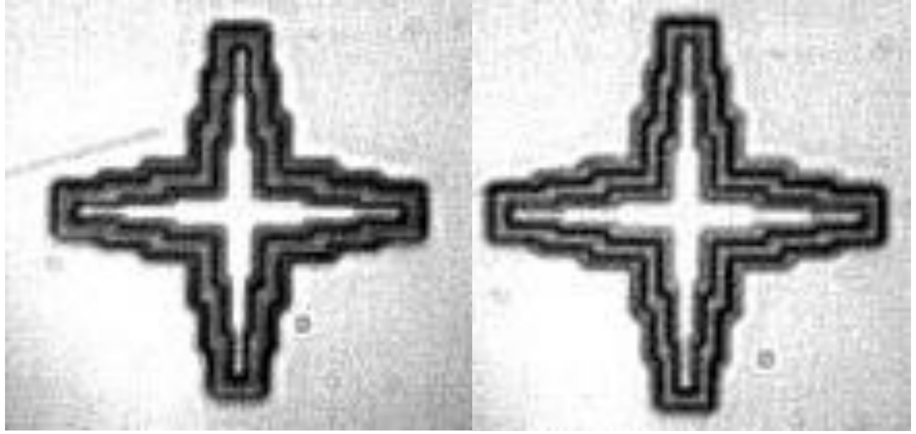


D. Rosenberg, et al. npj Quantum Information 3, 42 (2017)

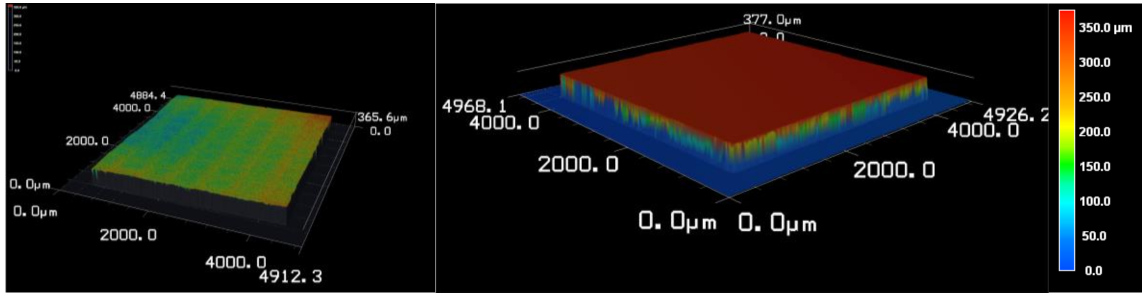
Qubit Flip-Chip Characterization

- **Alignment, bonding and parallelism:**

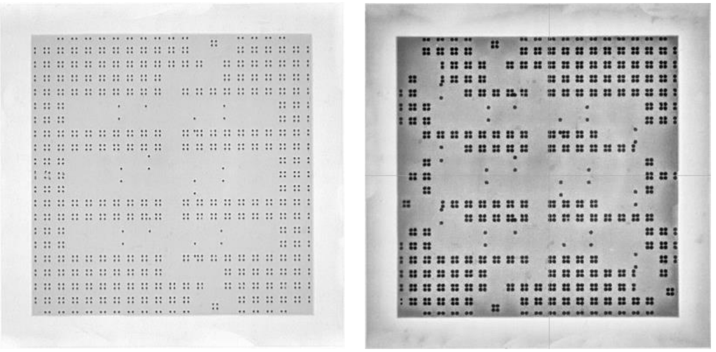
IR transmission image of overlaid alignment fiducials within ± 1 µm post-bond



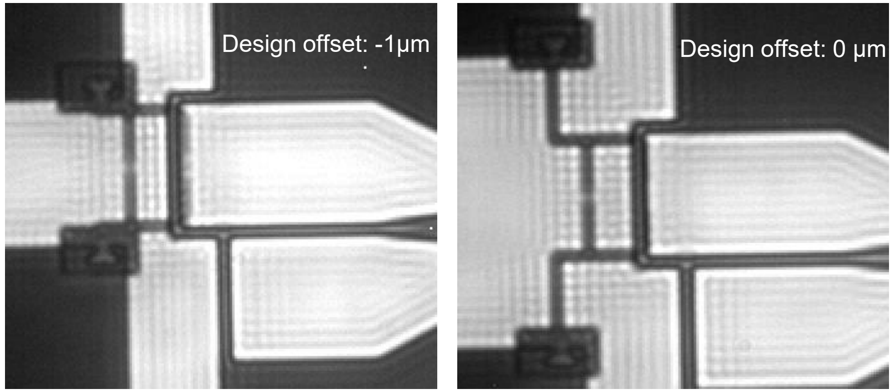
Confocal image for Parallelism



X-ray for bonding optimization



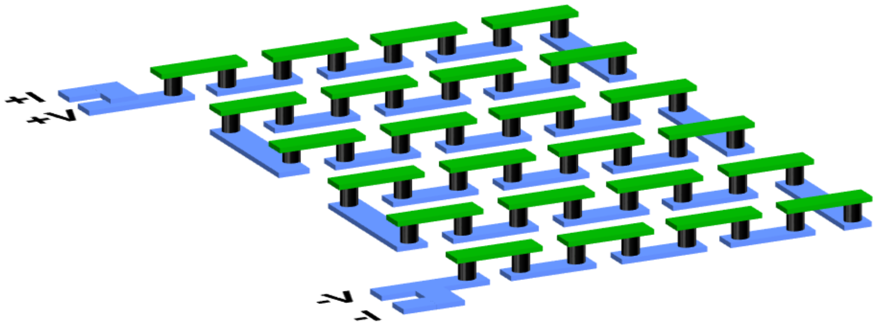
Qubit loop to off-chip bias line alignment



Das, *et al.*, *IEEE ECTC* 504-1414 (2018)

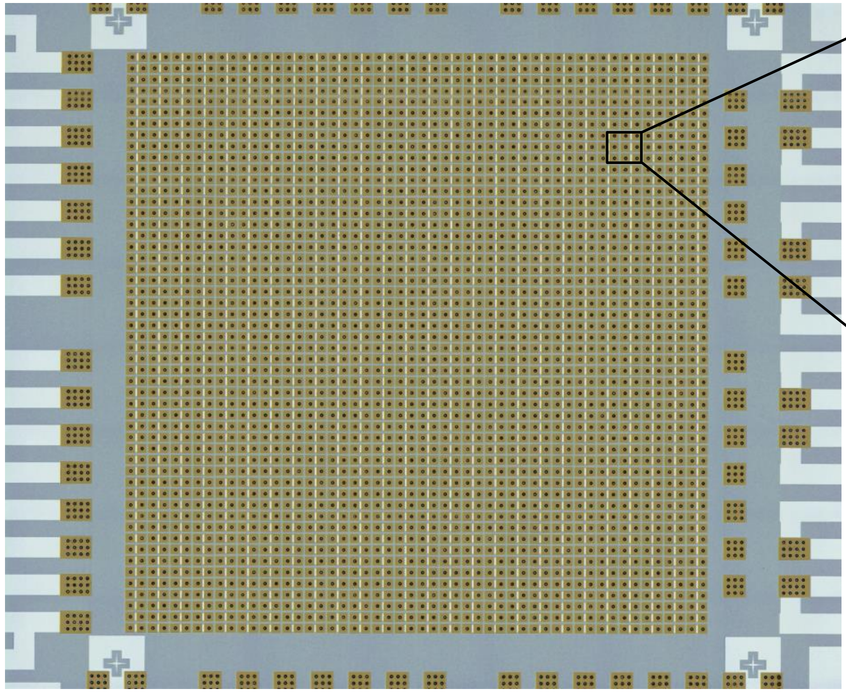
Indium Bump DC Resistance

Four-wire measurement of bump chain

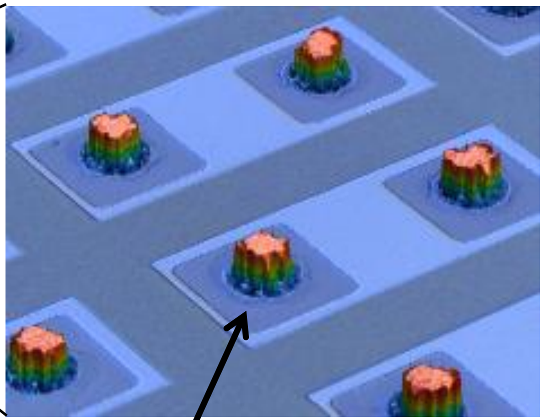


2,704 indium bumps connecting Al traces

Optical micrograph of one side of bump chain structure with 2,704 indium bumps



Confocal image of indium bumps



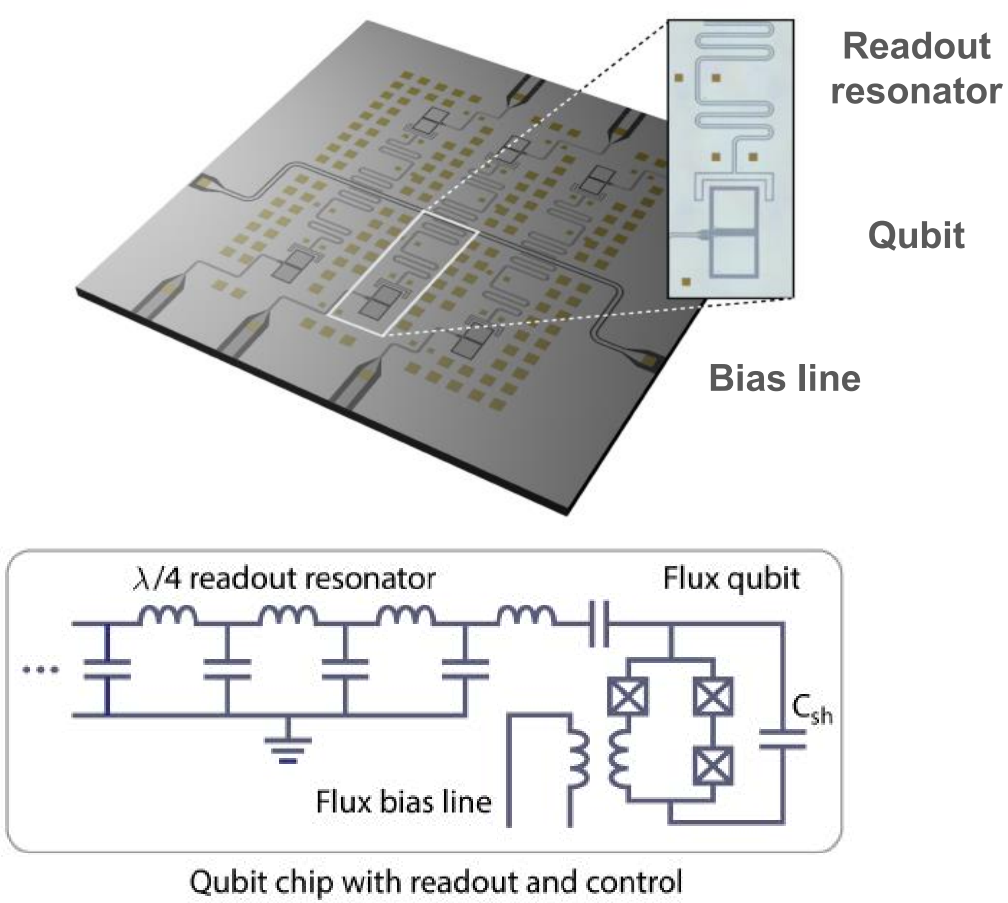
Under bump metal
Ti/Pt/Au

Measured resistance of ~240 nΩ/bump at 10 mK, consistent with underbump metal (UBM) resistance

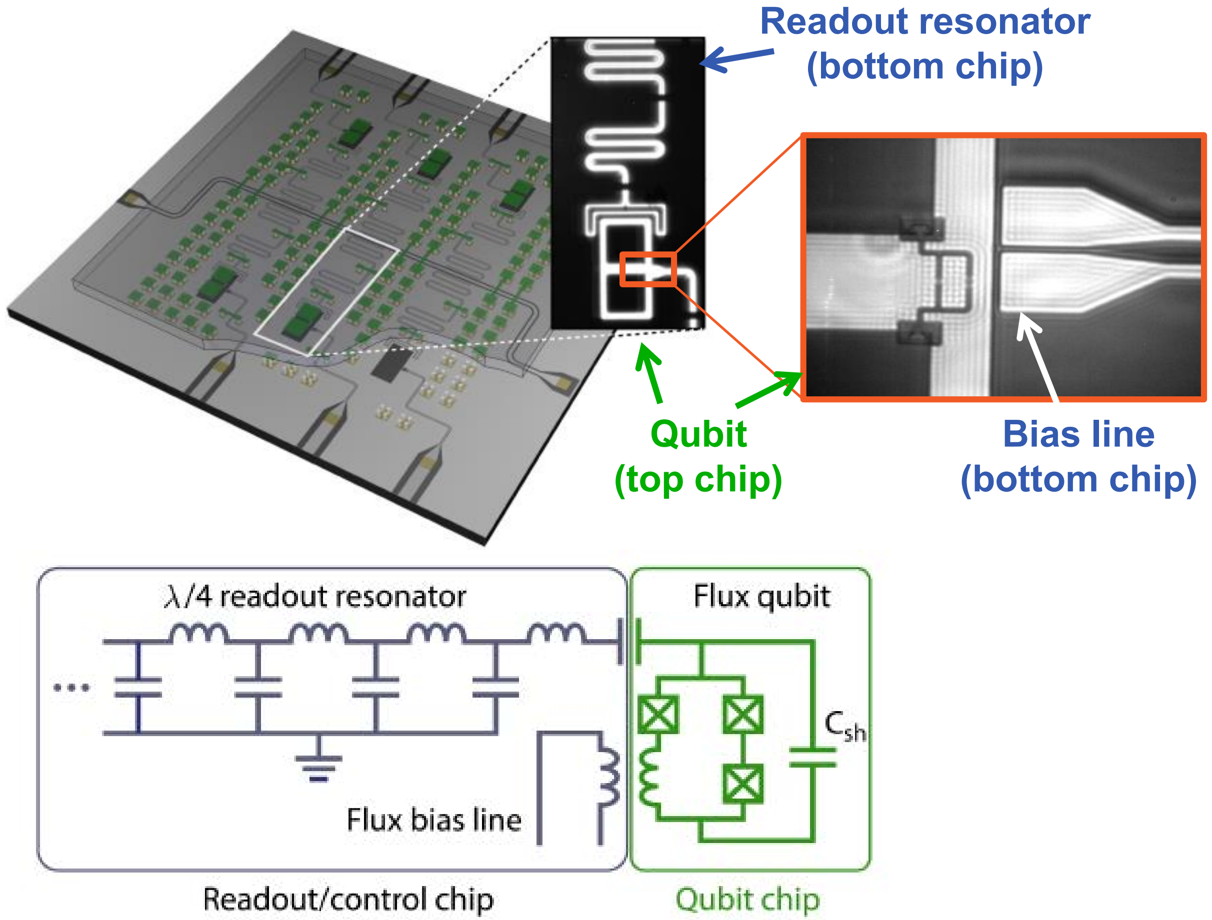
D. Rosenberg, et al. npj Quantum Information 3, 42 (2017)

Effect of Flip-chip integration on Qubit Quality

Single-Chip Qubits



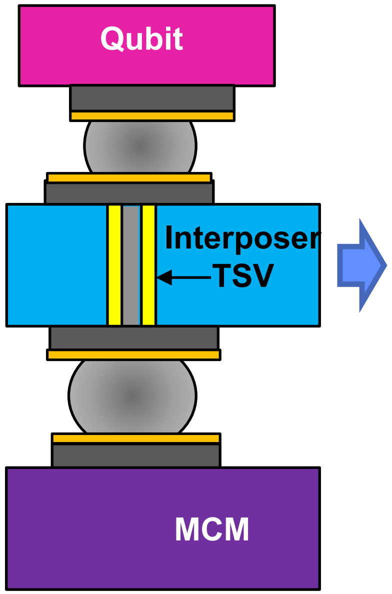
Flip Chip Qubits



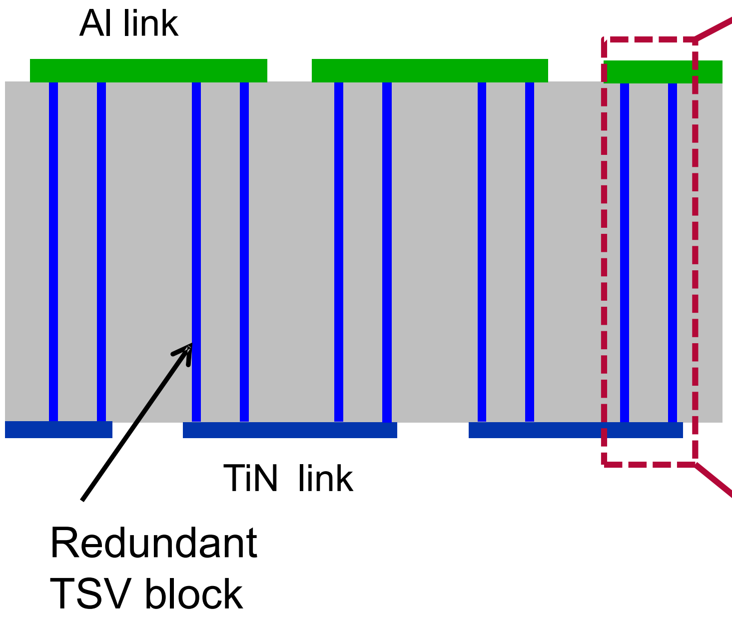
Coherence times comparable to planar qubits of same design

D. Rosenberg, et al. npj Quantum Information 3, 42 (2017)

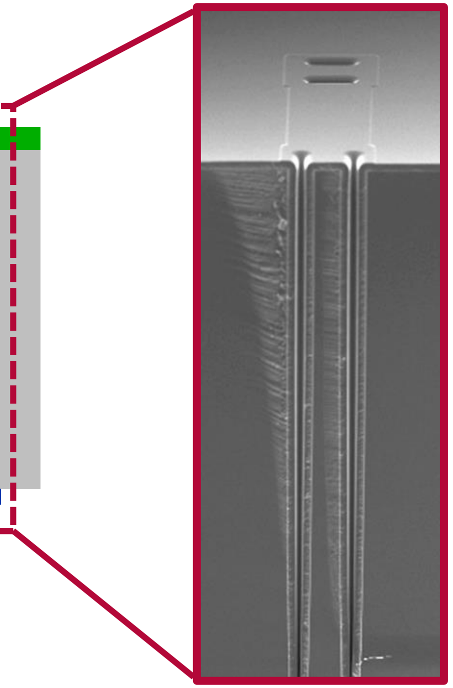
Superconducting TSVs



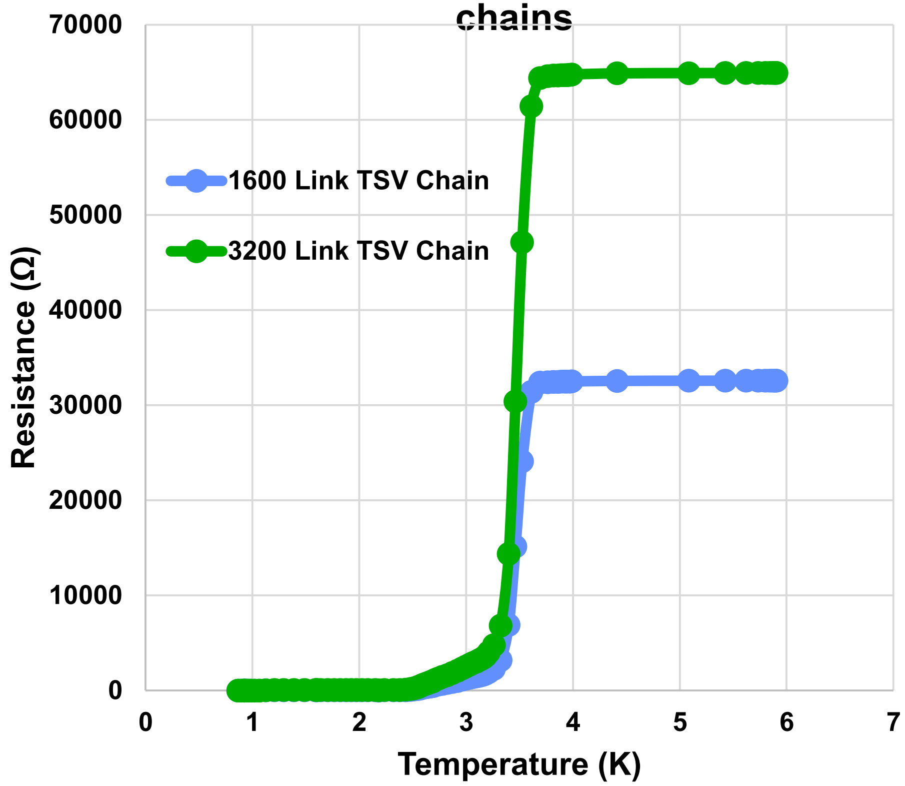
Test structures for four-wire measurements of TSV chains



Cross-section of TSV lined with TiN



Resistance vs. Temperature of TSV chains

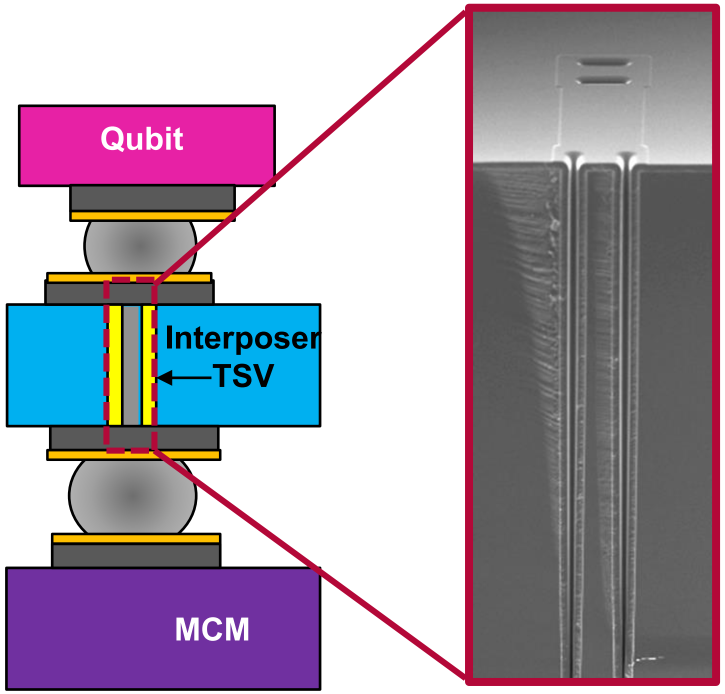


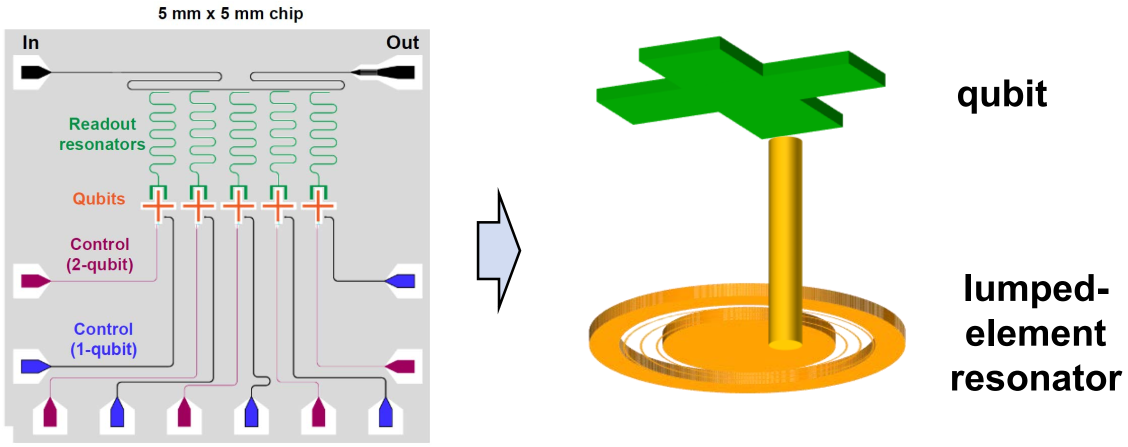
High-yield superconducting TSVs with Ic > 10 mA (>20,000 chain links measured)

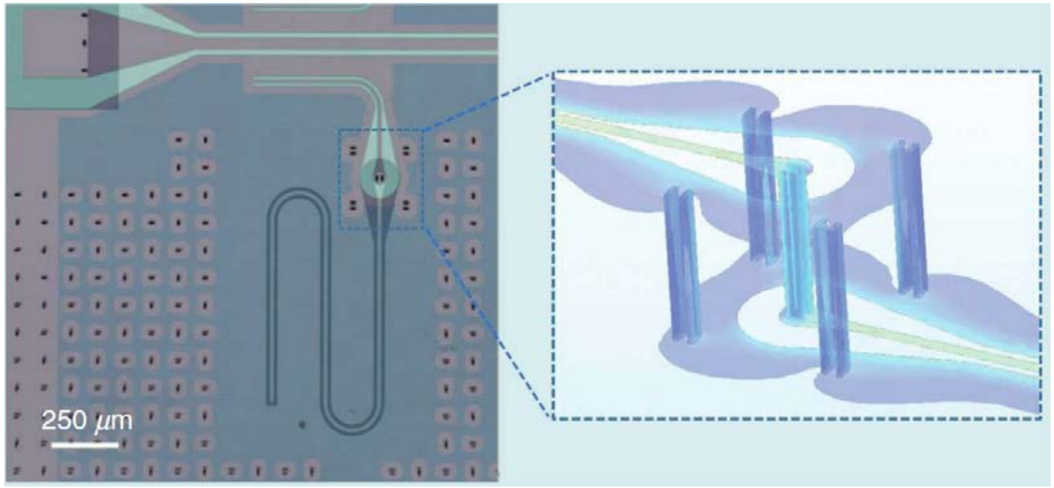
Rosenberg, *et al*., *IEEE Microwave Magazine* 21:8 (2019)
Mallek, Yost, *et al*., *arXiv (2021)*

Reduce Form Factor

Cross-section of
TSV lined with TiN







Superconducting TSV-integrated/ interrupted resonator reduces readout circuit area

Schwartz*, Hazard*, Woods*, *et al., in preparation*

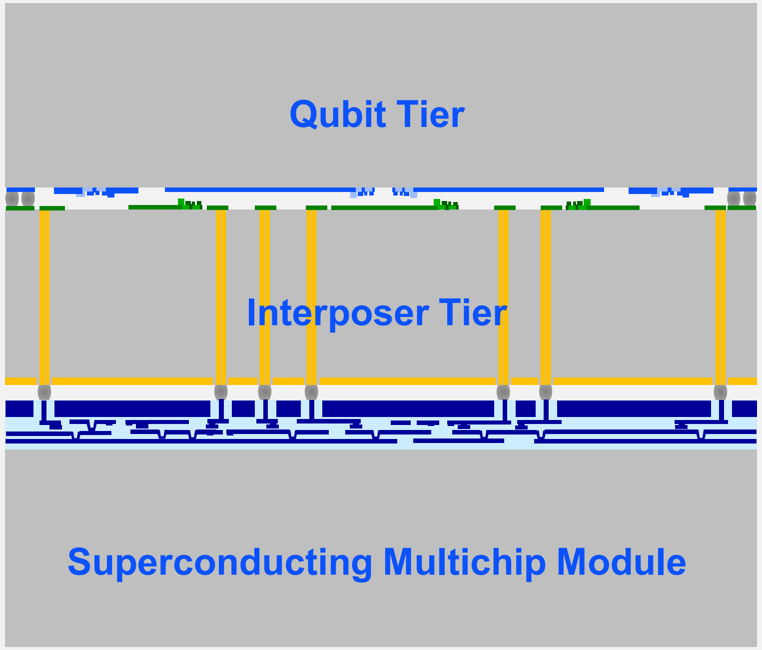
Rosenberg, *et al.*, *IEEE Microwave* 21:8, 72-86 (2020)

3-Tier Stack

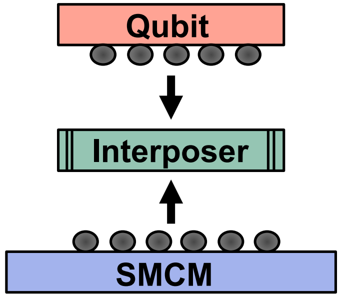
Double Bump Bonding

3-Tier Stack

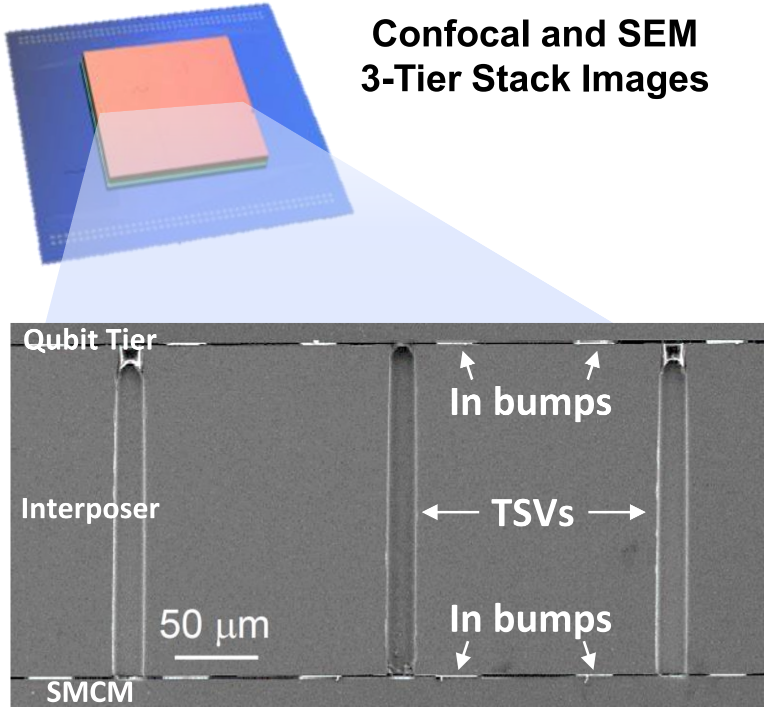
Three interconnect stages between qubit and SMCM tiers



Double-Bump-Bonded 3-Tier Stack



Confocal and SEM 3-Tier Stack Images



Combines high-yield TSV and bump-bond processes to test full 3-tier stack

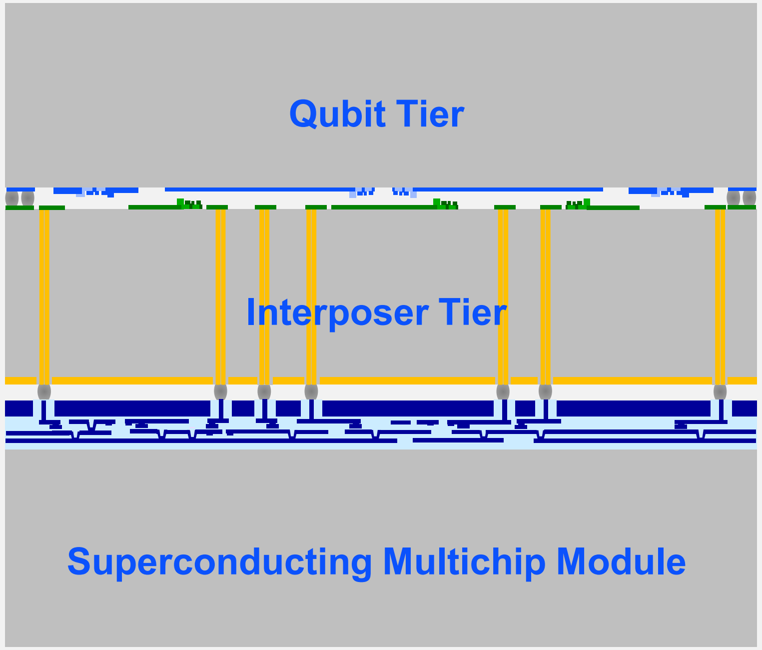
Das, *et al.*, *IEEE ECTC* 504-1414 (2018)
Rosenberg, *et al.*, *IEEE Microwave* 21:8, 72-86 (2020)

Hirjibehedin, Yost, Yoder, *et al.*, *in preparation* (2021)

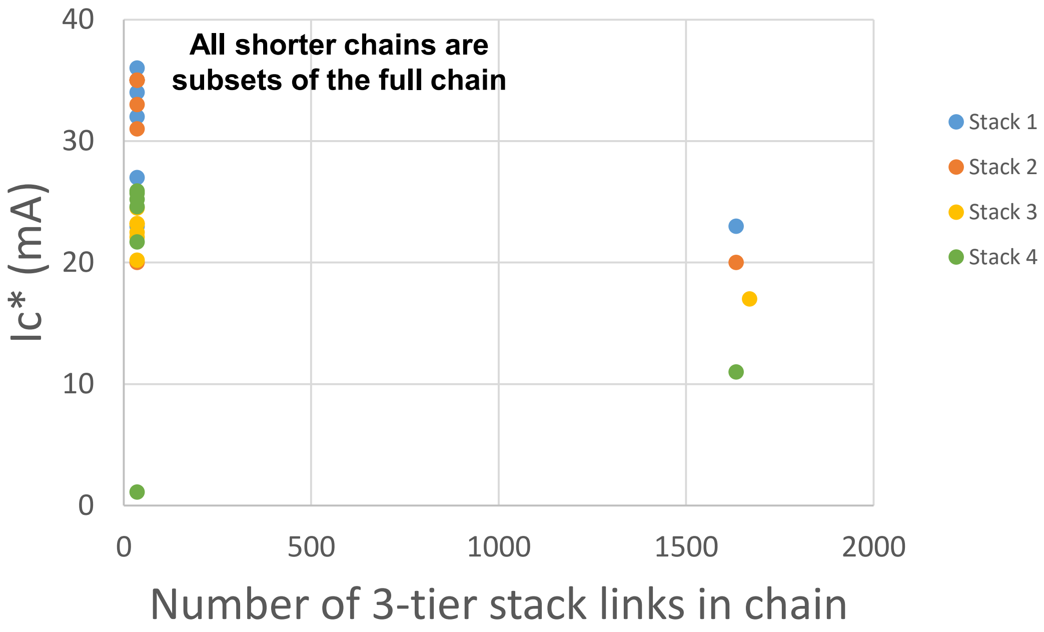
3-Tier Stack
DC Connectivity

3-Tier Stack

Three interconnect stages between qubit and SMCM tiers



3-Tier Daisy Chains



DC connectivity yield of 99.4% to 99.98% (across >6500 measured links)

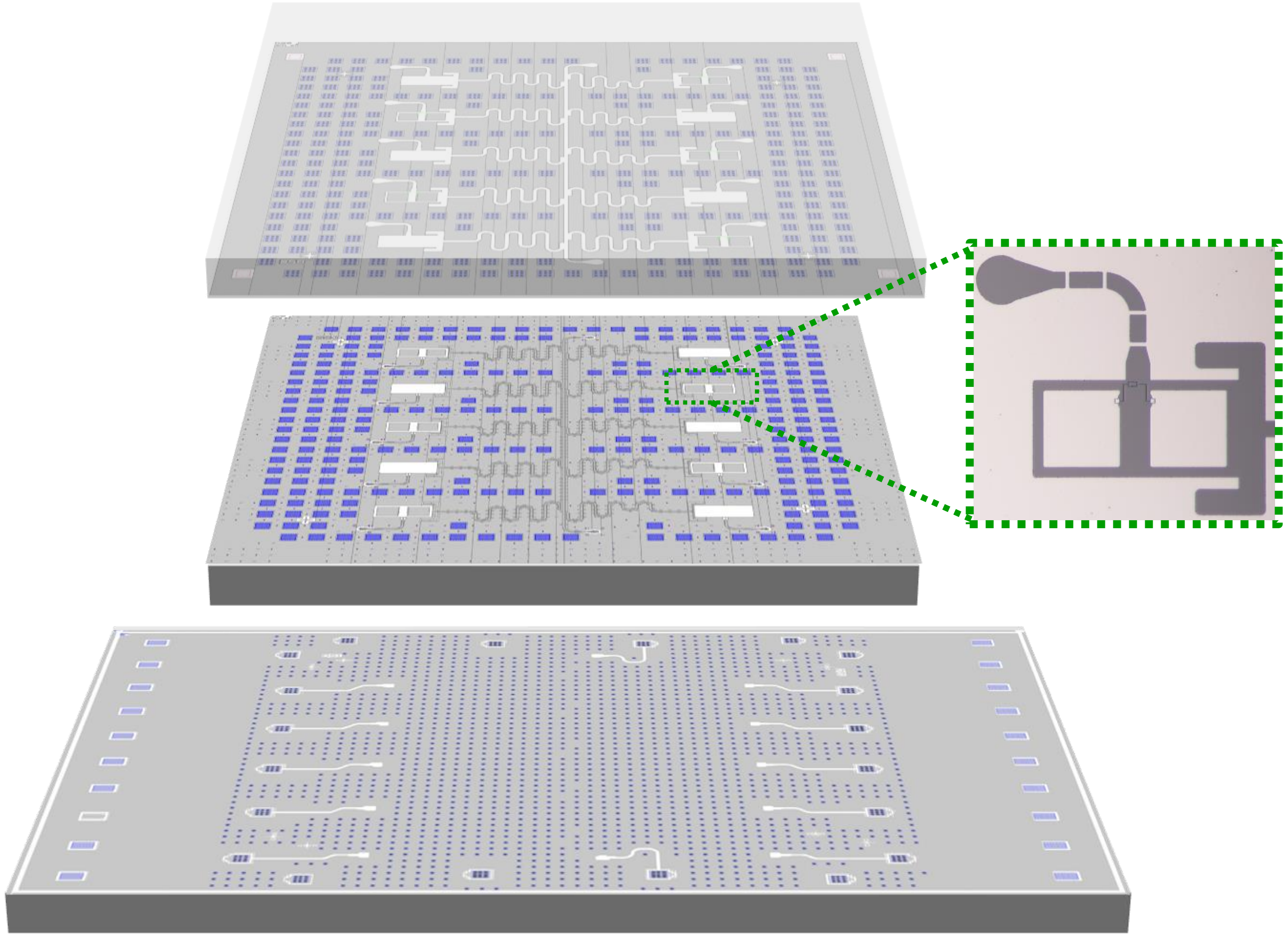
***Normal UBM metal has low residual resistance**

Das, *et al.*, *IEEE ECTC* 504-1414 (2018)
Rosenberg, *et al.*, *IEEE Microwave* 21:8, 72-86 (2020)

Hirjibehedin, Yost, Yoder, *et al.*, *in preparation* (2021)

3-Tier Stack

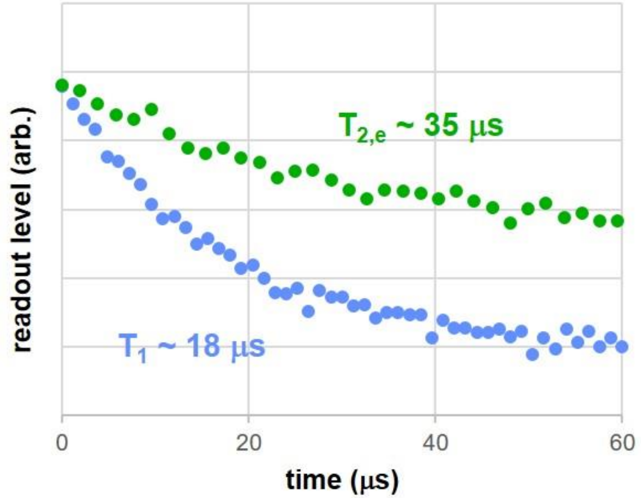
Qubit Performance



Qubit tier
- 5 C-shunt flux qubits

Interposer tier
- transmission line
- 10 resonators
- 10 local flux bias lines
- 5 C-shunt flux qubits

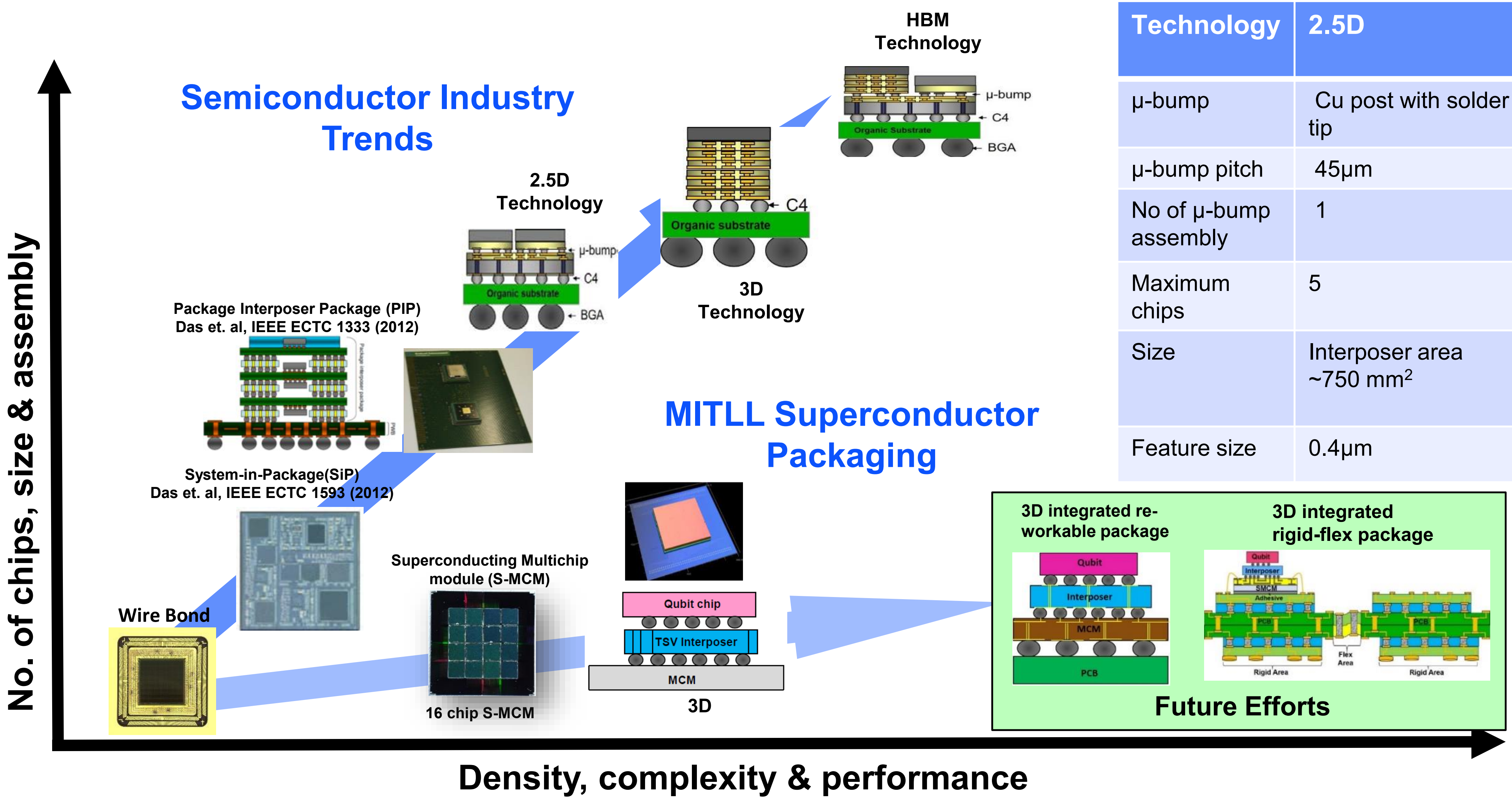
SMCM tier
- RF signal routing
- DC signal routing



3-tier stack qubit coherence times comparable to planar qubits of same design

Hirjibehedin, Yost, Yoder, *et al.*, *in preparation* (2021)

Semiconductor Vs Superconductor Packaging



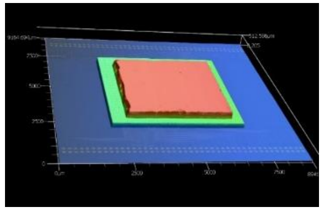
Technology	2.5D	S-MCM
µ-bump	Cu post with solder tip	Indium
µ-bump pitch	45µm	35µm
No of µ-bump assembly	1	2
Maximum chips	5	4(20X20 mm^2) 16 (5X5 mm^2)
Size	Interposer area ~750 mm^2	MCM area ~9200 mm^2
Feature size	0.4µm	0.8µm

Hirjibehedin, Yost, Yoder, *et al.*, *in preparation* (2021)
Yost, Schwartz, Mallek, *et al.*, *npj Quantum Information* (2020)

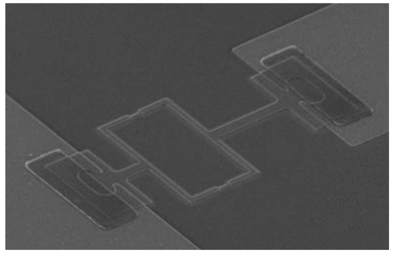
Das, *et al.*, *IEEE ECTC* 504-1414 (2018)
Rosenberg, *et al.*, *IEEE Microwave* 21:8, 72-86 (2020)

A look into the Future: 3D Quantum Vision

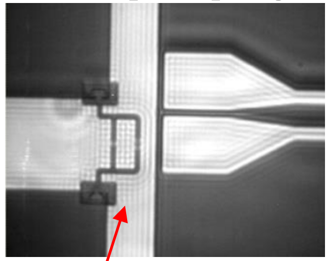
Double bump bonding



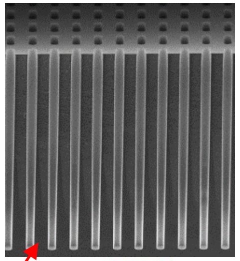
High Quality Qubit

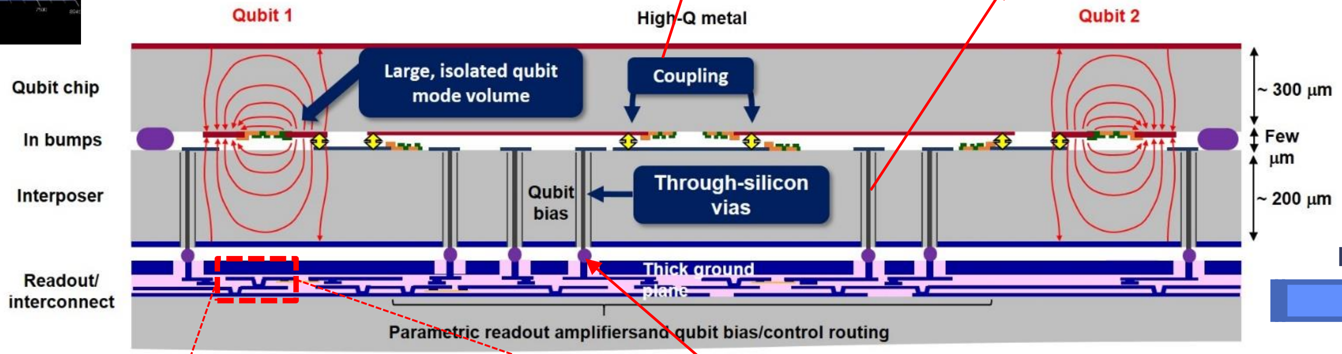


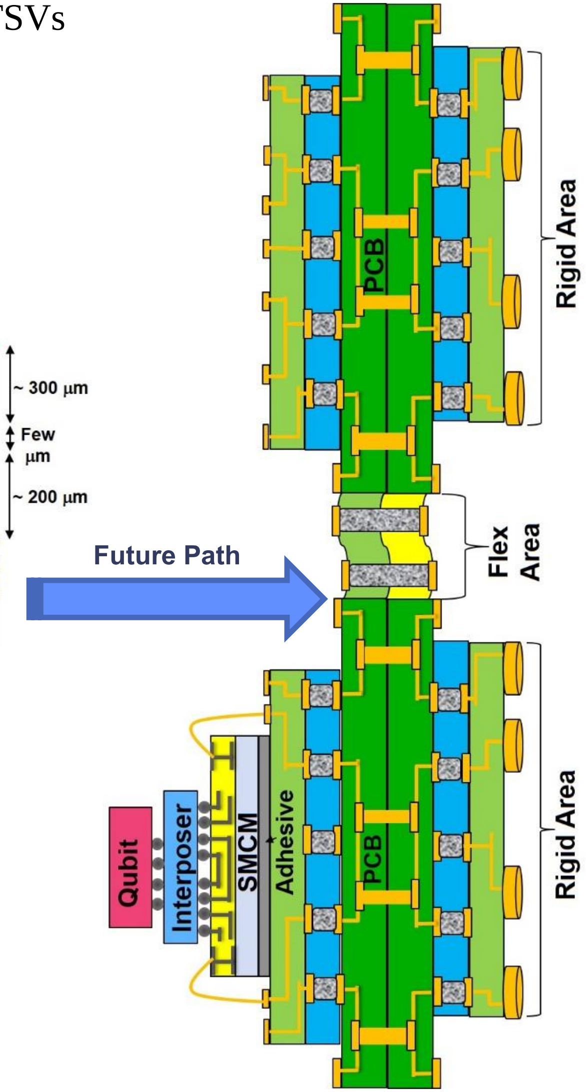
Off chip coupling

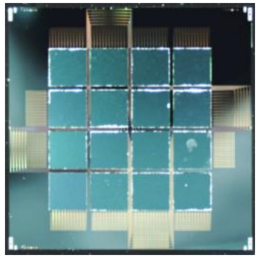


Superconducting TSVs

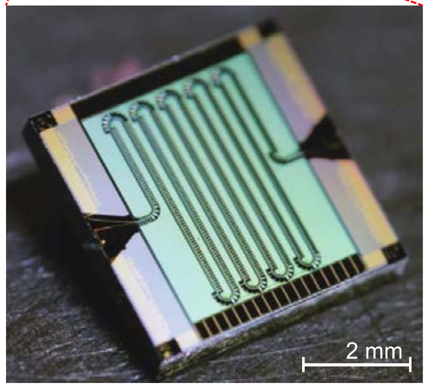




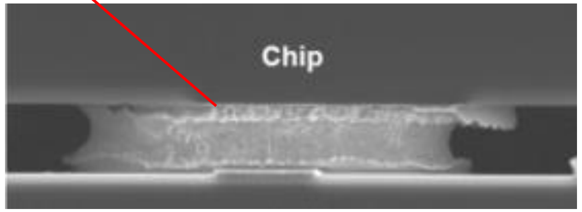




Flip-chip:
16 chip S-MCM



Travelling-wave parametric amplifiers



Superconducting indium bumps

Hirjibehedin, Yost, Yoder, *et al.*, *in preparation* (2021)
Yost, Schwartz, Mallek, *et al.*, *npj Quantum Information* (2020)

Das, *et al.*, *IEEE ECTC* 504-1414 (2018)
Rosenberg, *et al.*, *IEEE Microwave* 21:8, 72-86 (2020)

LINCOLN LABORATORY
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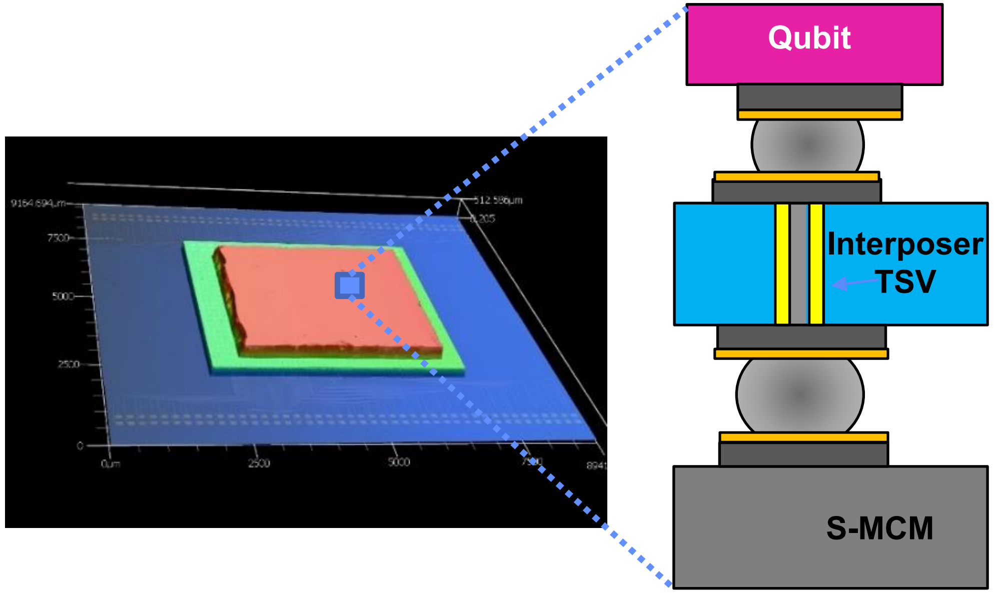
Summary

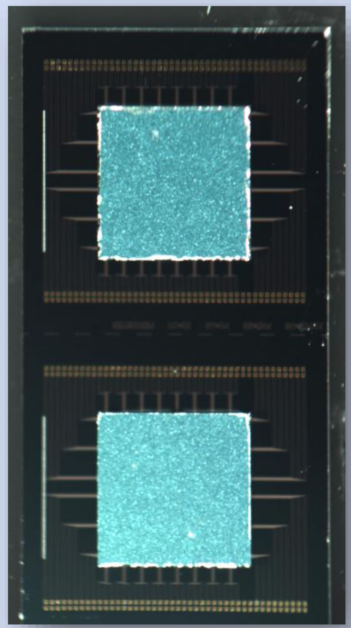
- **An integrated approach to develop 3D constructions on various flip-chip qubit package configurations is demonstrated.**
- **3-tier stack enhances connectivity and functionality while maintaining Qubit performance.**
- **Rigid-flex technology may be attractive for connecting superconducting qubit module to routing, control or amplification circuits.**



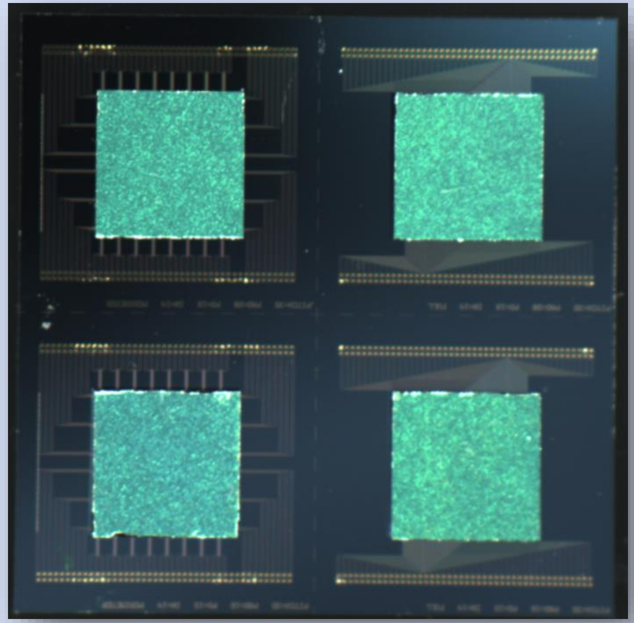
Backup slides

Superconducting Multi-Chip Module (S-MCM)

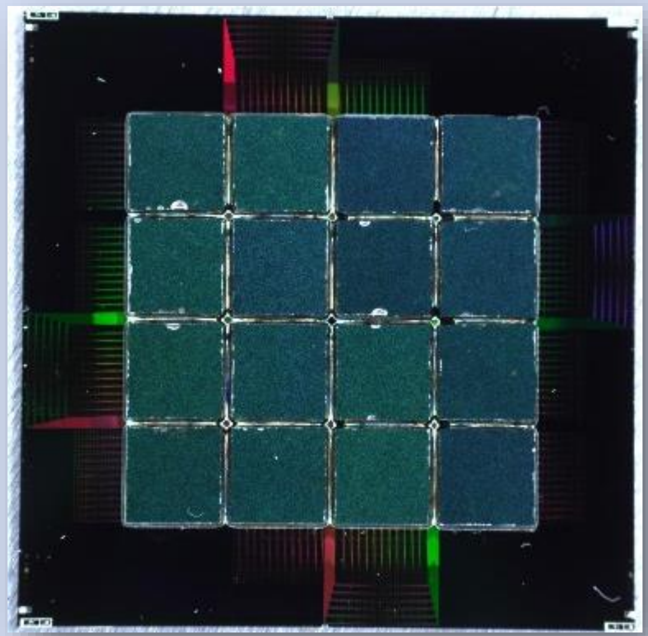
Superconducting chip:5mmX5mm



2 chip S-MCM



4 chip S-MCM



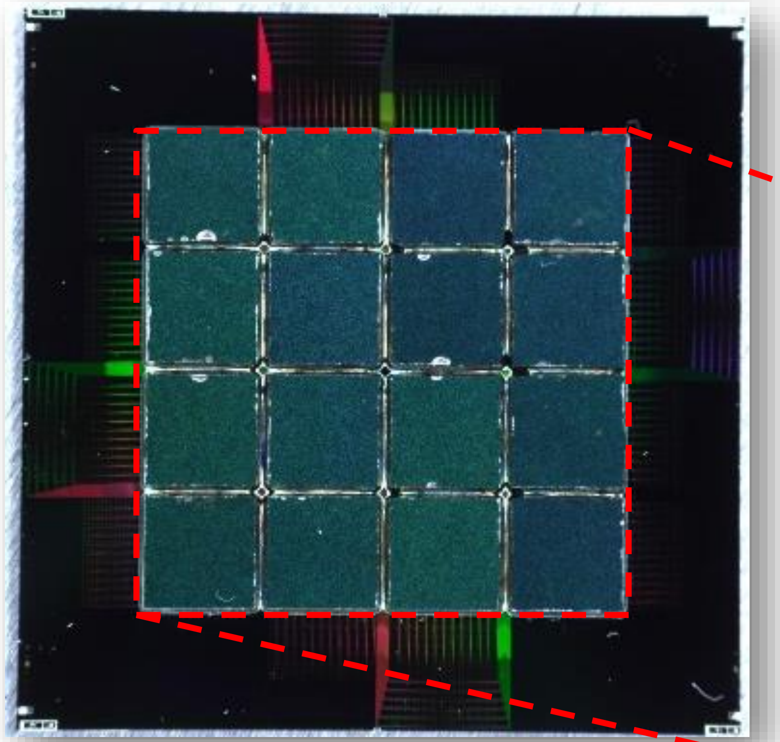
16 chip S-MCM

High-yield superconducting MCMs
(Fabricated up to 96mmX96mm S-MCM)

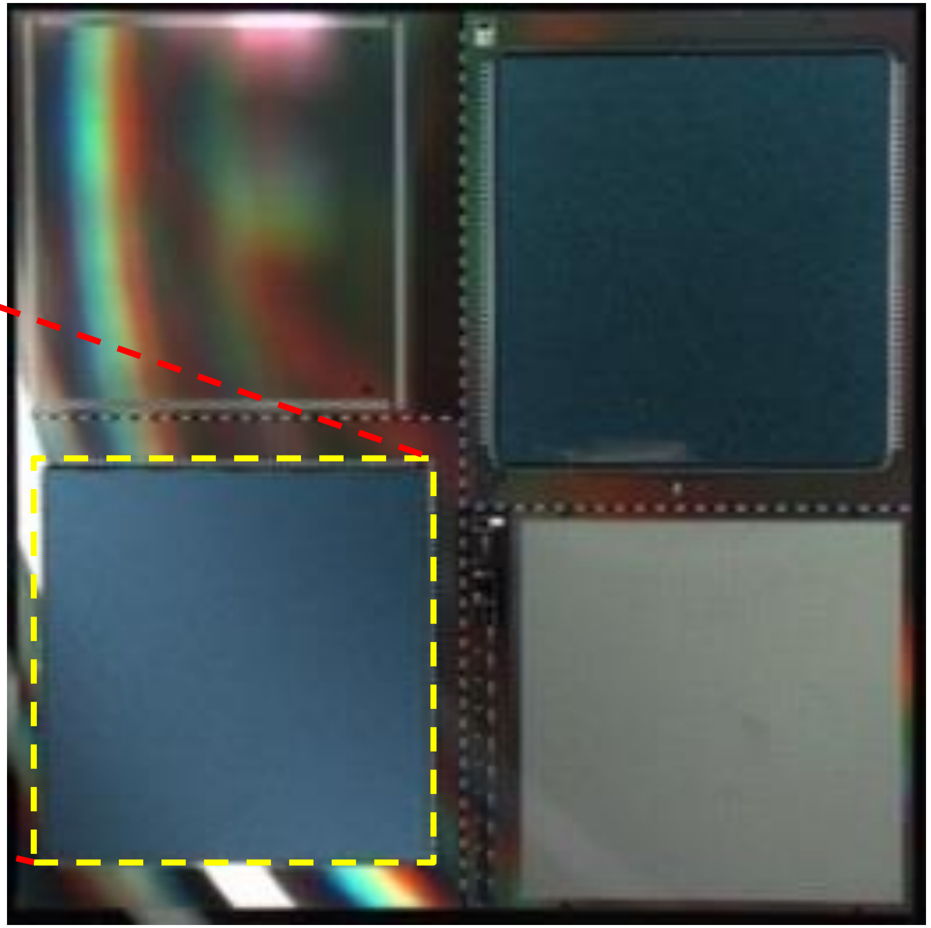
Das, *et al.*, *IEEE ECTC* 675-683 (2017)

Large Superconducting Chip Integration

(Thermocompression bonding capability)



S-MCM:32mmX32mm
16 (5mmX5mm) chips



MCM:48mmX48mm
2 (20mmX20mm) chips

Das, *et al.*, *Chip Scale Review Vol 25 (1)*,18(2021)