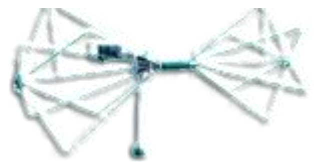

Electrical Design for High-End Computer Systems

Dale Becker, Ph.D.
IBM Corporation, Poughkeepsie, NY

IEEE Distinguished Lecture Series

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Electrical Design

- Signal Integrity
- Power Integrity
- Emissions (EMC)
- Susceptibility (ESD)

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Motivation

- Modern Computing is driven by
  - Big Data and Analytics
- With many data inputs
- Demanding sophisticated analytics
- Sent back to distributed users

➔ More Data Bandwidth

➔ Less Data Latency

➔ Higher integration of computing, networking and storage

- Electrical Design Challenges
  - Higher Bandwidth Density
  - Co-design and Co-analysis across package components
  - Disciplines are not independent (SI, PI, EMC, ESD)

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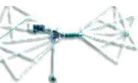
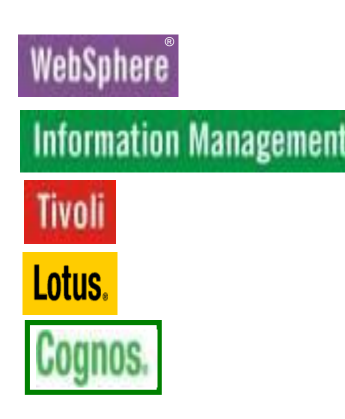


What is Technology? zEnterprise EC12:

Java

Rational



Semiconductor Technology → Microprocessor Design → Systems Design → Virtualization & Operating Systems → Compilers, Tools & Java Virtual Machine → Optimized Middleware

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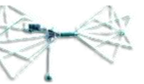
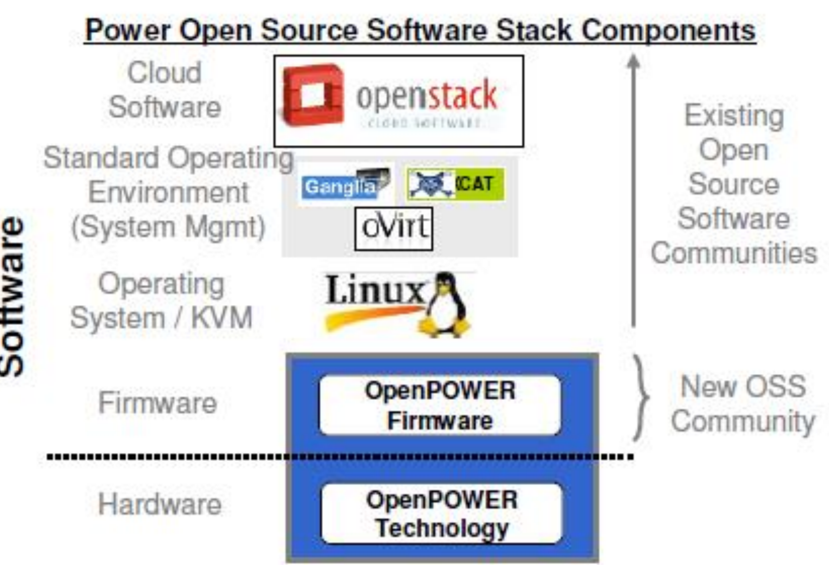


Proposed Ecosystem Enablement



Multiple Options to Design with POWER Technology Within OpenPOWER

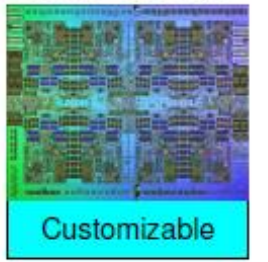
Hardware

POWER8

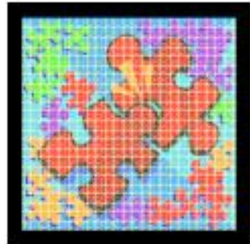
CAPI over PCIe

"Standard POWER Products" – 2014

Framework to Integrate System IP on Chip



Industry IP License Model



"Custom POWER SoC" – Future

http://openpowerfoundation.org/technical/technical-resources/

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50 Years of Mainframe – 1964 IBM S/360

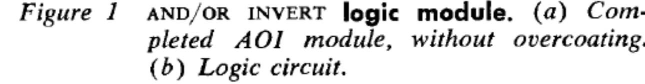
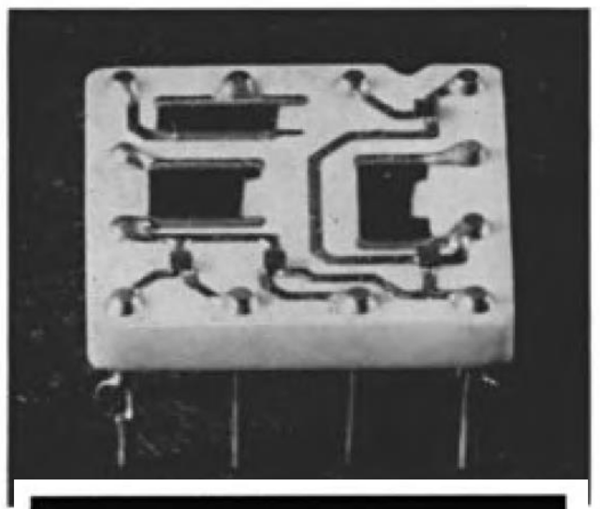


Figure 1 AND/OR INVERT **logic module.** *(a) Completed AOI module, without overcoating. (b) Logic circuit.*



(*b*)

Power dissipation in mW

	On	*Off*	
Resistors	28	19	(All *R*: 5%)
Transistor	7	0	
D_1, D_2, D_3	0	2	
D_4	1	1	
D_5	1	1	
Total	37	23	

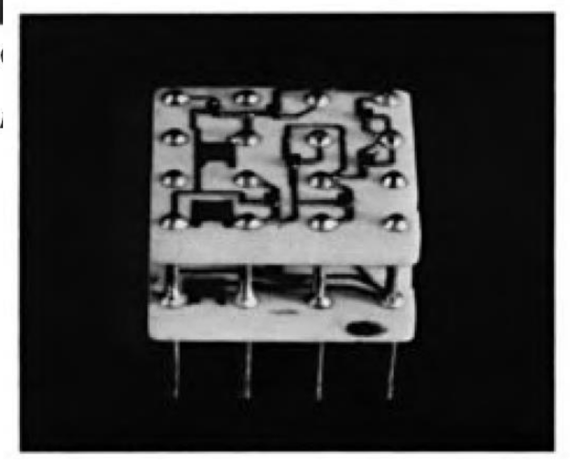


Figure 13 **Stacked module.**

Solid Logic Technology: Versatile, High-Performance Microelectronics Davis, E.M. ; Harding, W.E. ; Schwartz, R.S. ; Corning, J.J.
IBM Journal of Research and Development Volume: 8 , Issue: 2 Publication Year: 1964 , Page(s): 102 - 114

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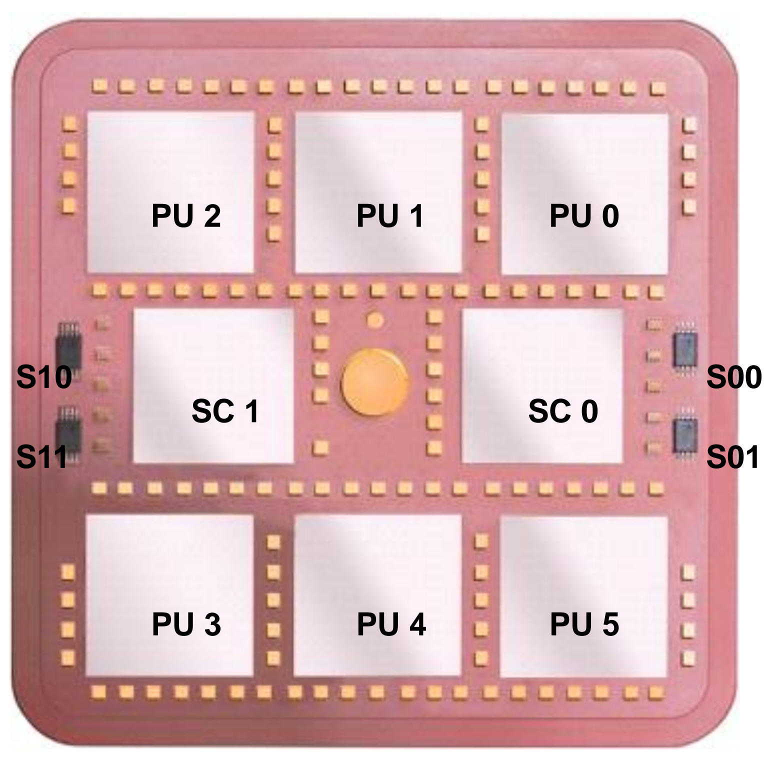
Processor packaging



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POWER Die

Figure 5.1.7: Annotated POWER8 die photo.

[POWER8: A 12-core server-class processor in 22nm SOI with 7.6Tb/s off-chip bandwidth](#)
[Fluhr, E.J.](#) ; et. al. [Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International](#)
Publication Year: 2014 , Page(s): 96 - 97

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Scale-out

PCIe G3 x8

2X SAS Ports

PCIe G3 x16

SAS Cntrl

PCIe G3 x16

Memory

Memory

POWER8

2xHMC Serial USB

PCIe G3 x8

Memory

POWER8

12 SFF Bays

6 SSD Slots

Slim DVD

http://www.ibm.com
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Scale-up

OSC
DCA
DCA
POL
Memory
POL
Memory
POL
POL
Memory
POL
POL
Memory
POL
POL
Memory
POL
Memory
POL
CP
CP
CP
CP
CP
CP
SC
Calypso
SC
5 x PCI-e
5 x PCI-e
3 x SMP
4 x GX
3 x SMP

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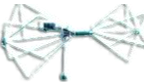

Data rates are increasing

- Today
  - Proprietary – 12.4 GT/s
  - PCIe Gen3 – 8 GT/s
  - DDR3 – 2133 MT/s
  - SAS – 6 GT/s
  - Optics – 10 GT/s
- Soon
  - PCIe Gen4 – 16 GT/s
  - Proprietary 28 GT/s
  - DDR – 3200 MT/s
  - SAS – 12 GT/s
  - Optics – 25 GT/s
- R&D
  - ~50 GT/s
  - PAM4 vs NRZ
  - Tighter optics integration

Processor Frequency
IO speed
Proc Frequency (GHz)
IO speed (GT/s/pair)
18
16
14
12
10
8
6
4
2
0
n-4
n-3
n-2
n-1
n
n+1
N+2
technology node

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PCB Technology Choices
Same speed, different technology

Channel Loss dB/cm

1

0.5

0

4 GHz

8 GHz

12 GHz

Frequency

Scale Out System
Std Loss
4.9 mil 1 oz

Mid-Range System
Mid Loss
5 mil 0.5 oz

Scale Up System
Low Loss
3.5 mil 1 oz

All systems are 8 GT/s meet 20dB total channel loss

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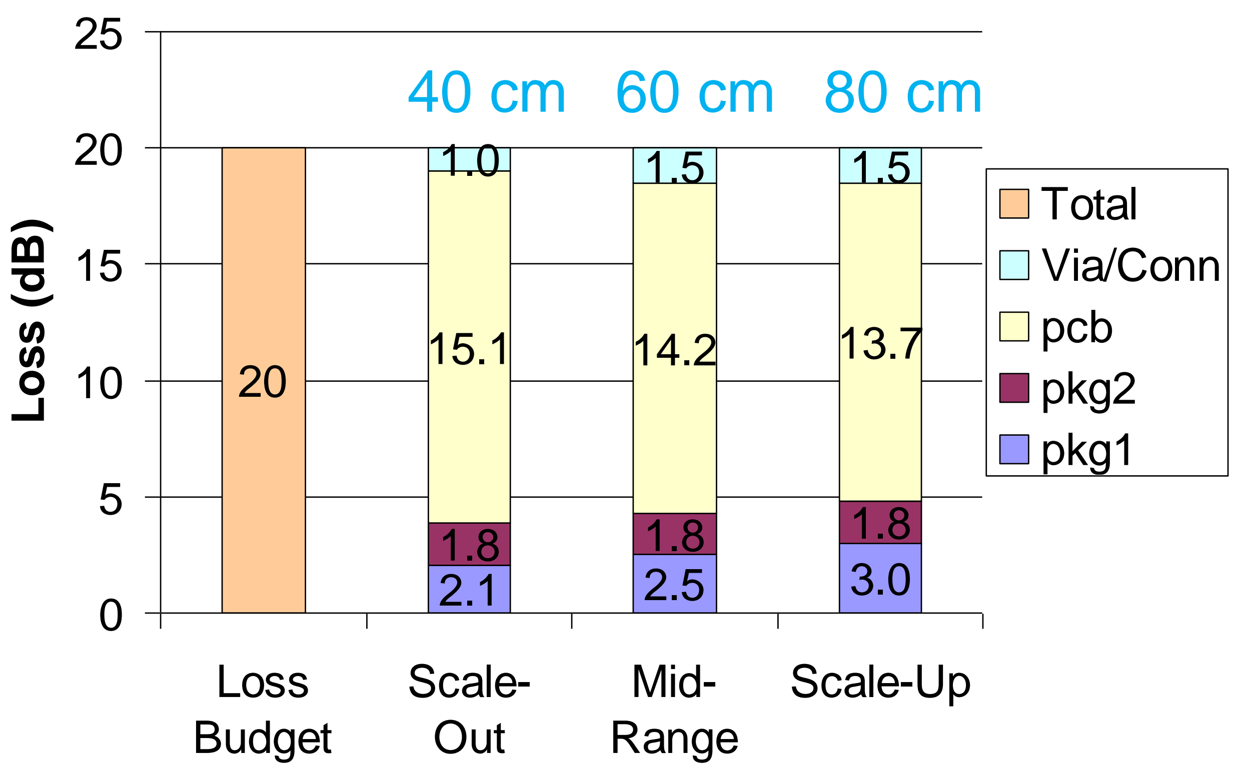
Impact of PCB loss –
Size of system, length of PCB trace



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Reaching a bandwidth breakpoint at the socket level

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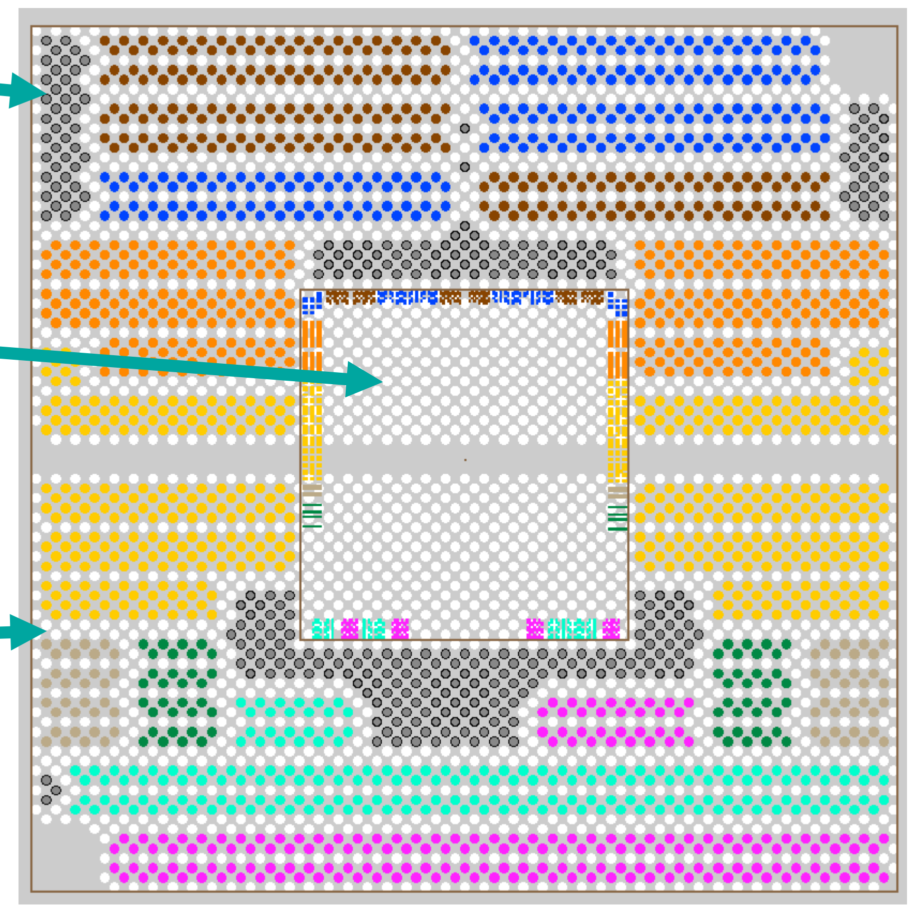
Socket Pin Assignment

- Signal Pins
  - More pins = more bandwidth
- Power Pins
  - Lower voltage levels require more pins
- Reference Pins
  - Higher frequencies require better isolation between signal pins



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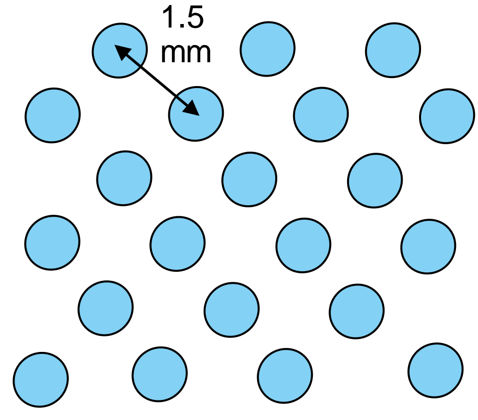
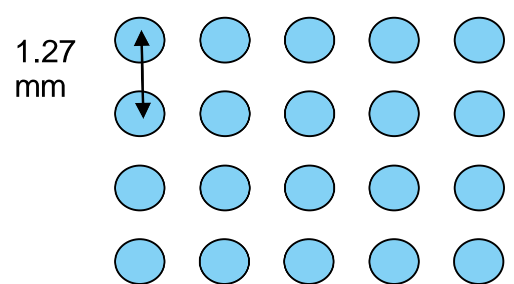
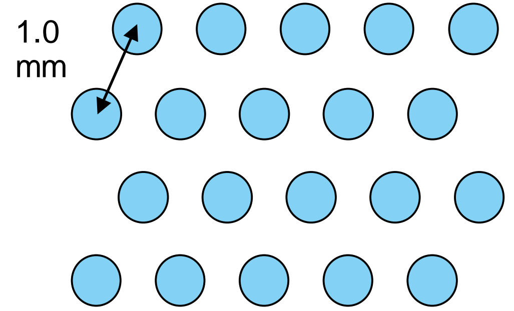
Pin Density Increases Incrementally

- Over 20 years
  - 1.5 mm min pitch interstitial
  - 50 mil (1.27 mm) square
  - 1 mm square
  - 1 mm min pitch hexagonal

- Sockets are pin limited
- Crosstalk needs to be managed







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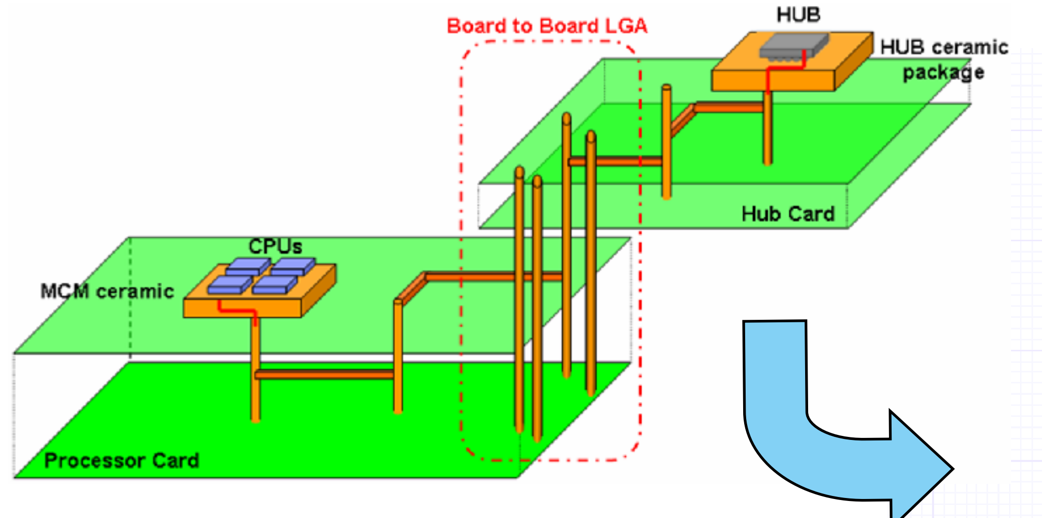
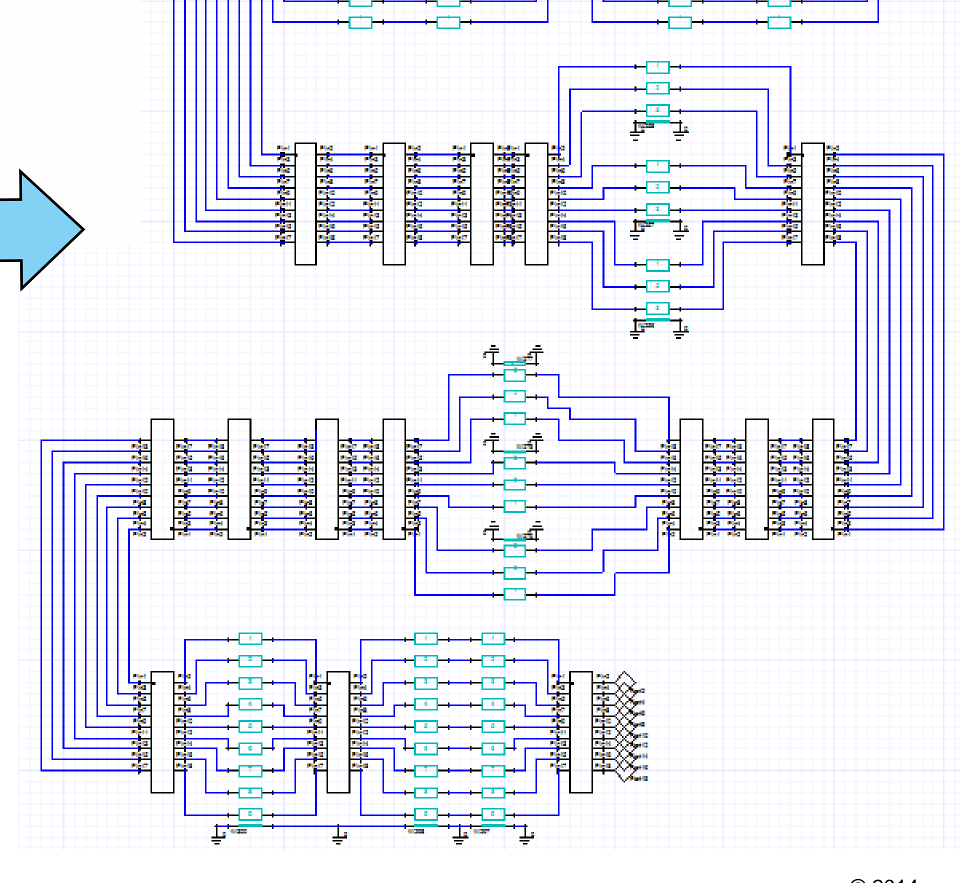
How is integrated SI/PI analysis performed on a channel like this?





- *The system under analysis is composed by two PCBs, two MCMs and three connectors*
- *To represent it adequately 52 models are needed:*
- *1. W-elements to model the TL portions*
- *2. S-parameters (Touchstone) for the 3D parts (Vias and connectors).*
- *3. Mpilog Precompensation Driver macromodel*
- *4. Frequency step for touchstone: 50 MHz*
- Total channel length ~ 70cm

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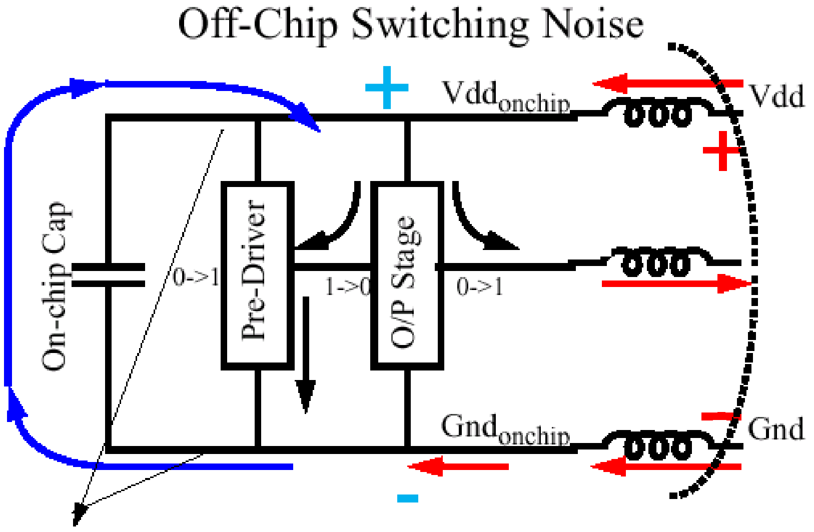
IO switching



- Modeling SSN
  - Current loops include the signal distribution
  - Models need to be modified to include Driver, Receiver and Transmission Lines

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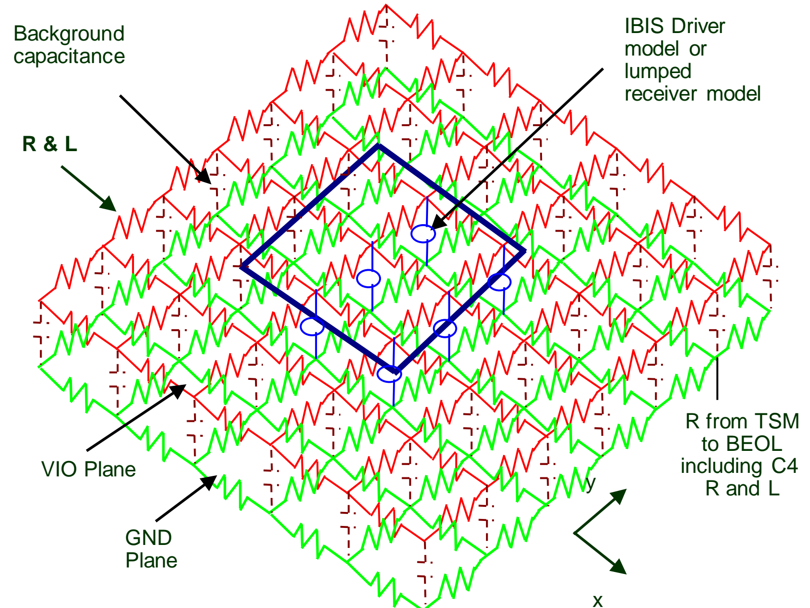
SSN - Simulation methodology

Ideal Power
Ideal Source
C2build X-section
c4gen X-section
Resonator X-section
Tx Data Mac (serializer, predriver, driver)
P
85ohm term
Diff voltage compression
The current into the N output of the driver iis - 1*P output current
Ideal Gnd

- Input data from IO Ckt
  - Location of current sinks
  - SSN Current signatures
  - Delta I currents (Power and Clock Gating)
  - Capacitance on VIO domain

- On-chip power grid model
  - •L has more contribution to SSN when frequency is higher than 3.2 Gb/s
  - •PKG, BRD, decaps



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Grounding for ESD and EMC

Safety Grounds

0-Ohm Resistor Connections

Modeled Area

Comparison of Grounding Schemes

Z_{real} (Ω)

10^{3} 10^{2} 10^{1} 10^{0} 10^{-1} 10^{-2} 10^{-3} 10^{-4} 10^{-5}

10^{7} 10^{8} 10^{9}

KEY 1e+03 1e+02 1e+01 1e+00 1e-01 1e-02 1e-03 1e-04

Connector Flange

Top Side Resistors at Mounting Holes

Board Stiffener

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Susceptibility to external sources (ESD)

- Need understanding of and source – External
- Complex conduction path making quantifying noise difficult.
- Many different circuits making a large task of determining noise margins
- Difficult to define a systematic test plan

Rear
16 DIMMs
100mm High
MCM @ 1800W
Water Cooled
MCM
Memory
Memory
3 DCA Power Supplies
14 DIMMs
100mm High
Cooling
connector

Internal
Batteries
(optional)
Power
Supplies
Support
Elements
I/O cage
Carried
Forward
PCIe I/O
drawer
Processor Books
with Flexible
Support
Processors
(FSPs), PCIe and
HCA I/O fanouts
PCIe I/O interconnect
cables and Ethernet
cables FSP cage
controller cards
N+1 Water
Cooling
Units

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Moving towards system level analysis – Co-design and Co-analysis

- Co-development and co-design
  - New technology brings new tools and methodologies where co-design is more naturally adopted
    - e.g., 3D and TSVs
  - Components with mature technology are more difficult to co-design
    - Distributed teams with tool, methodology, and skill differences
    - More sophisticated specifications and data sharing
- SI/PI co-analysis is developing but challenging
    - Migrating from budget-based methodology,
    - Too many unknowns for one integrated tool
    - Need for both new technology and mature technology

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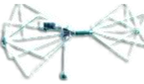

Conclusion

- Big Data and Analytics are driving the growth in high-end computing processor usage
- Signal interconnection is a big challenge
  - –Increasing Frequency
  - –More devices to interconnect
- Resulting smaller timing windows makes power integrity and signal integrity more closely related.
  - –Increased training and awareness of engineers
- Proper power distribution design is needed for EMC and ESD robustness

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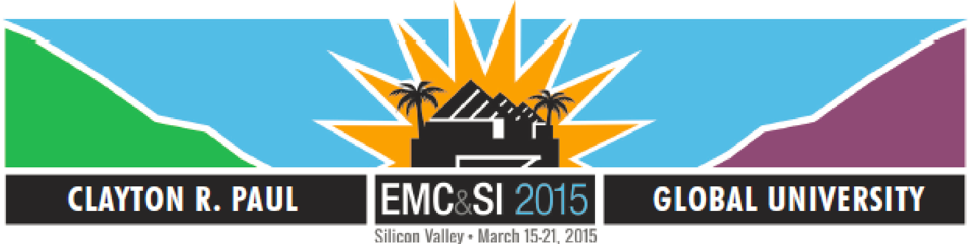

TABLE OF CONTENTS

Tuesday, March 17

1:00 pm - 3:00 pm	Radiated Emissions and Conducted Emissions *Instructor: Lee Hill, Silent Solutions LLC, Amherst, NH, USA*	pg ?
3:30 pm - 5:30 pm	Grounding Essentials *Instructor: Todd Hubing, Clemson U*	pg ?

Wednesday, March 18

1:00 pm - 3:00 pm	Introduction to Signal Integrity *Instructor: Jun Fan, MST*	pg ?
3:30 pm - 5:30 pm	Introduction to Power Integrity *Instructor: Ege Engin, SDSU*	pg ?

Thursday, March 19

1:00 pm - 3:00 pm	SI and EMC Design for High-Speed Differential Signaling *Instructor: Tzong-Lin, NTU*	pg ?
3:30 pm - 5:30 pm	SI/PI Issues and Solutions for High-Speed Single-Ended Signaling *Instructor: Dan Oh, Altera*	pg ?

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