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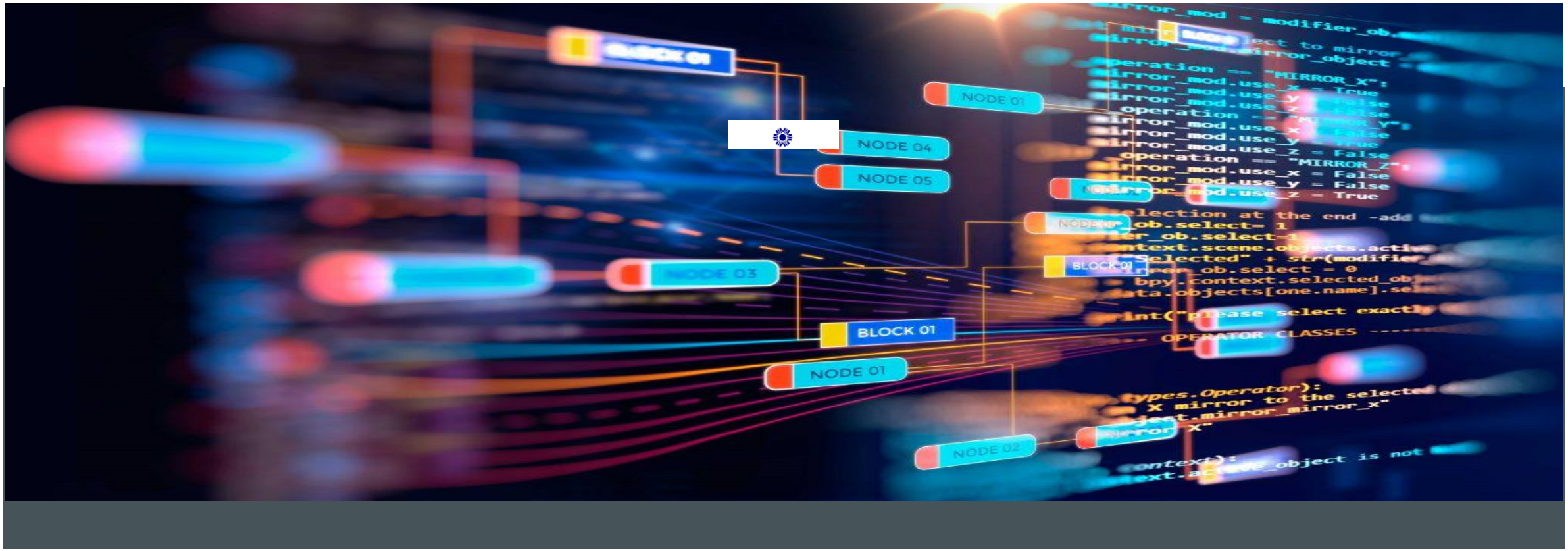
INTERNATIONAL MICROSYSTEMS INCORPORATED

DAC : DISJOINT ARRAY COMPUTER

PATENTED ARCHITECTURE FOR LARGE DATASET AND CLOUD APPLICATIONS



OUTLINE FOR TODAY'S BRIEFING

1. Current STP Architecture Makes Data Transfer A Bottleneck
2. DAC Architecture Basics & its Benefits:
    1. Higher Processor Efficiency
    2. Lower Cost, Lower Power, & Higher Reliability
    3. Resulting in Lower TCO (Total Cost of Ownership)
3. Example: DAC-24 Server with Linear Performance Scaling Using Satellite Ultraviolet Data
4. DAC Architecture Details & Summary

WE NEED A DATA SERVER ARCHITECTURE THAT ADDRESSES TOMORROW'S NEEDS TODAY

DAC is a Paradigm Change in Server Design

DAC Servers Provide the Means for Greatly Increased Speeds in Data Base Processing

EXPERTS SAY CURRENT STP ARCHITECTURE IS BOTTLENECK

"For the last three years we've seen a kind of stagnation. That's bad news for research programs reliant on supercomputers, such as efforts to understand climate change, develop new materials for batteries and superconductors, and improve drug design"

~Horst Simon, Deputy Director, Lawrence Berkeley National Lab

Moore's Law Does Not Seem to Apply to Server Processing Efficiency

Why is This?

EXPERTS SAY CURRENT STP ARCHITECTURE IS BOTTLENECK

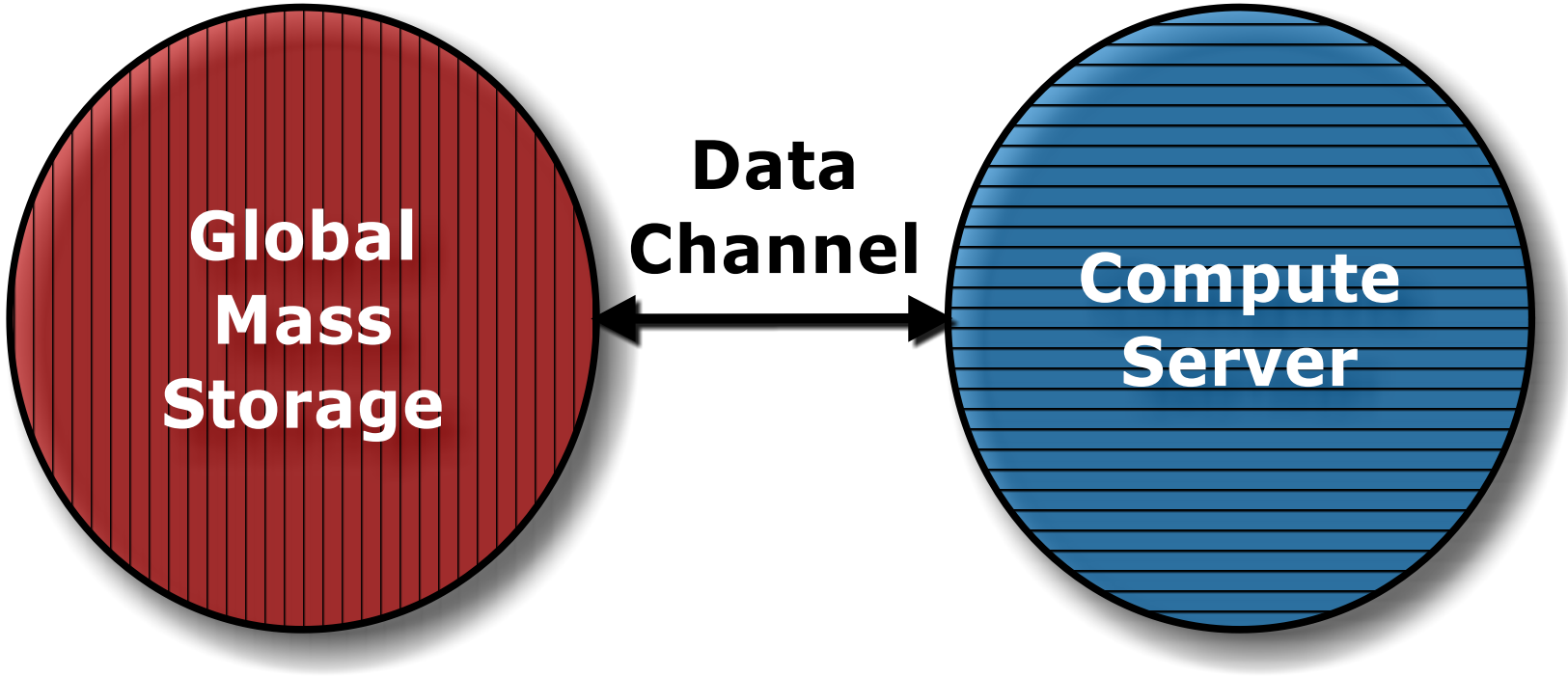
"We've got to start to think about computing architectures, not the CPU, as the central element. You have data where it sits, and you move whatever compute you need closer to the data to be able to do that. *Memory and storage now become the focal point of the system architecture."*

~Steve Pawlowski, VP, Advanced Computing Solutions Micron Technology

The Message From Steve Pawlowski:

We need to Change the Basic Design of our Computers

TODAY'S TYPICAL DATA SERVER MODEL – THE STP MODEL



TODAY'S STP DATA PROCESSING RACK SERVER MODELS

S

T

P

Flash Array
HDD Array

High Speed
Connectivity

Blade Server
CPU Server

Standard 19" Rack

1U = 1.75"

Max Rack Height = 44U

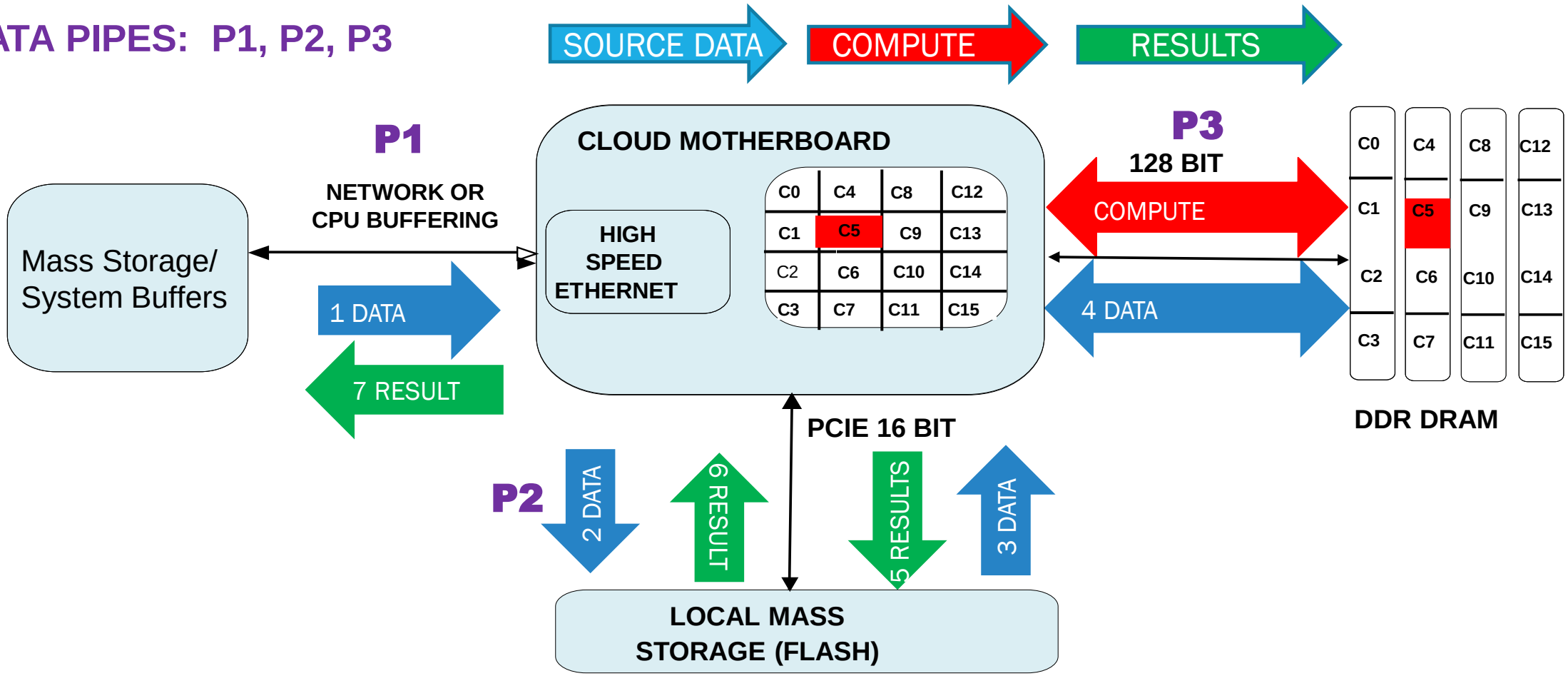
Flash Array = 2/4 U

Blade Server = 2/8 U

- Today's Servers have Optimized Each S T P Function
- Yet the overall Processing Efficiency is 2% --- Why ?
- The cause for this inefficiency is ***Too Much Data Movement!***

Data Movement in a Standard Server – with a 16 Core CPU

3 DATA PIPES: P1, P2, P3



Actual Example: DB Server with NVME Storage: # Data Moves to Compute = 23

!!! Too Much Data Movement for Too Little Result !!!

DAC TRANSFORMS THE STANDARD STP MODEL

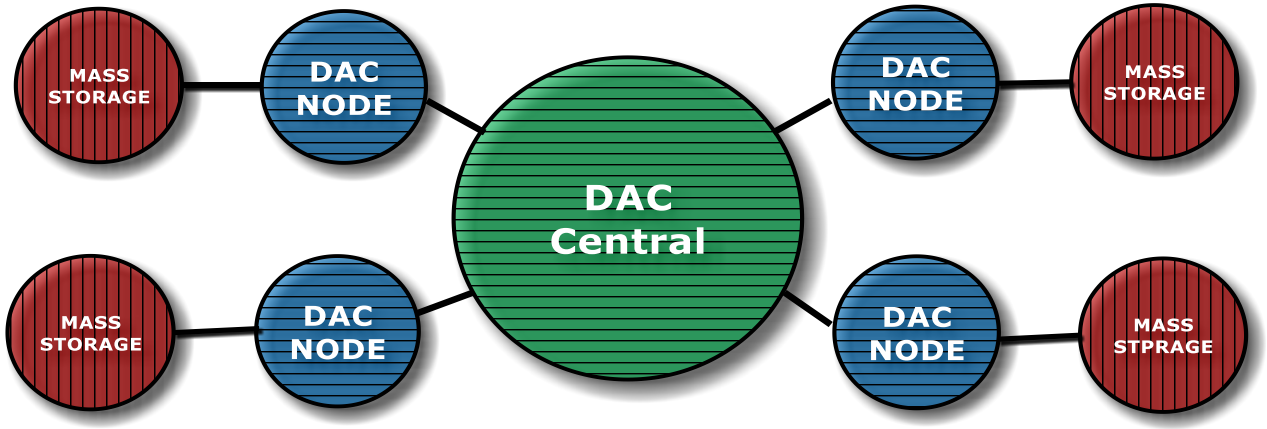
- DAC Architecture breaks the transmission bottleneck in STP
- DAC is a Storage Centric Model Not a STP Processor Centric Model
- DAC Substitutes USB for PCIe Removing Need for Global Clocking
- DAC's Array Based Processing Enables High Fault Tolerance, Lower Power, Higher Processing Efficiency, High Modularity

Note: Today's USB Speeds include 5 GPS, 10 GPS, 20 GPS, and 40 GPS Standards

THE DAC DATA SERVER MODEL

The DAC Hardware Model

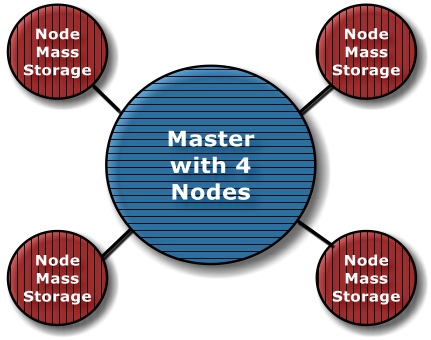
A Four Node DAC Server



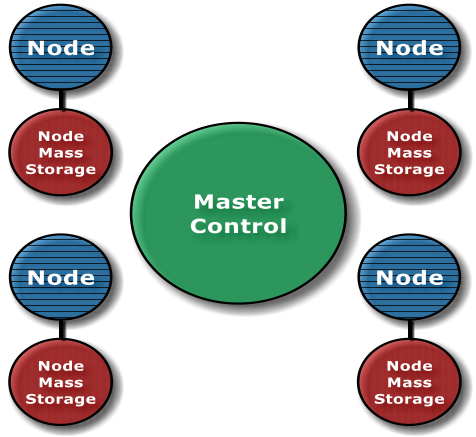
The DAC Software Model

DAC View A: Master with Access to Complete Global Storage

DAC View B: Node Access to Arrayed Global Storage



DAC View A



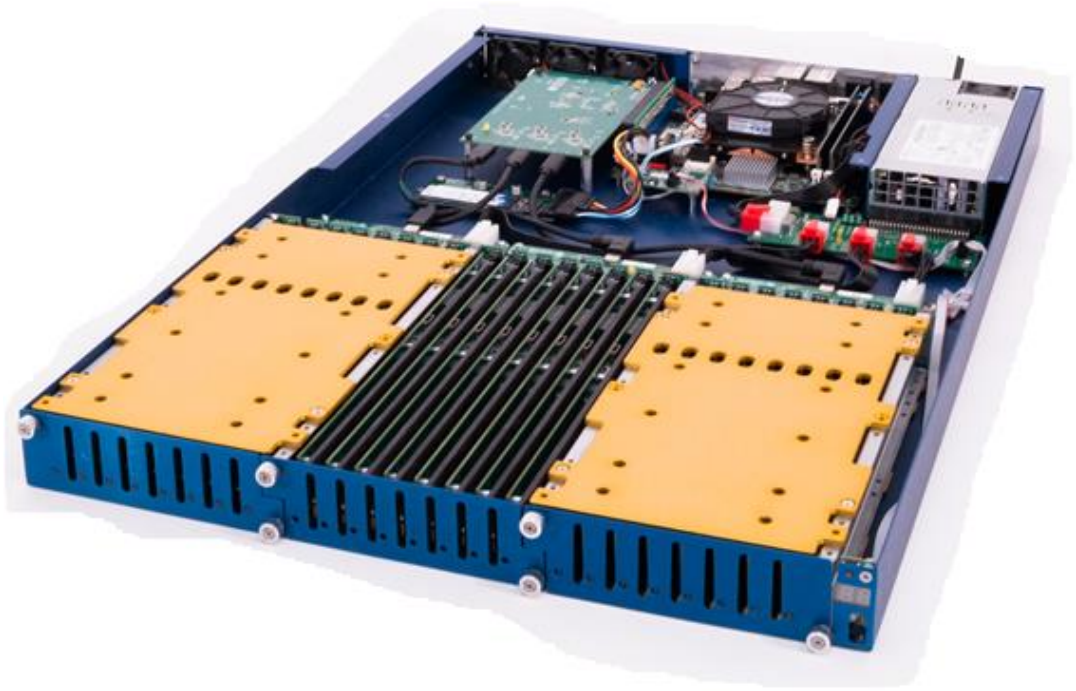
DAC View B

DAC DESIGN PRINCIPLES

- Storage Centric Computer Design
- Low CPU & Data Movement Latency
- Closely Coupled CPU to DDR & Flash Memory
- Minimal CPU I/O
- CPU Global Mass Storage Access with No Arbitration
- Low Power with Minimal Power & Data Transmission Network
- Array Processing

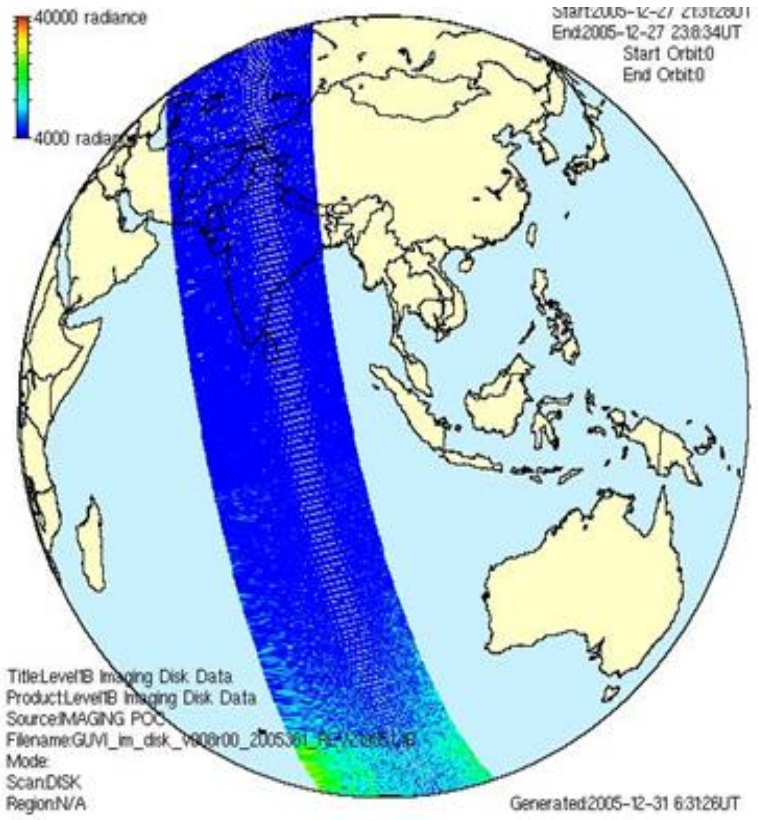
DAC : STANDARD PARTS & PROTOCOLS: 20X PROCESSING

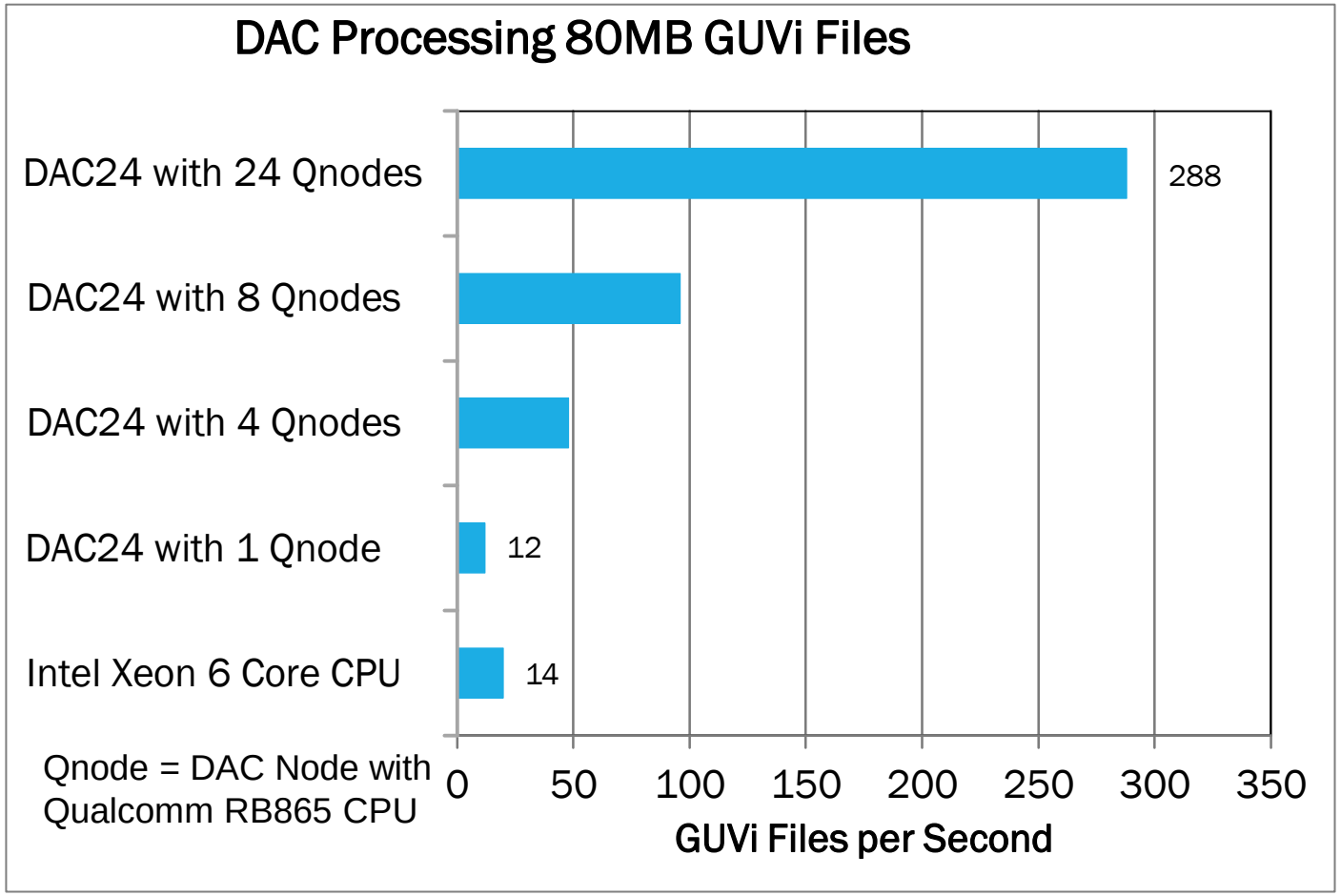
- DAC server is a novel architecture that relies on
  - Off-the-shelf memory and processor
  - Standard protocols like USB
- DAC can provide 20X processing speed in a modular 1U format
  - With low power and cooling needs



The IMI DAC-24 Test Platform

EARTH'S ULTRAVIOLET DATA PROCESSED BY DAC SERVERS





DAC IS A STORAGE CENTRIC SERVER

- DAC Processing is Parallel Array Processing versus STP Multi-Core Processing
- DAC Processing is Closely Coupled to the Data rather than via Long PCIe Channels
- DAC Data is Distributed using USB versus PCIe resulting up to 50% Power Savings
- DAC can use Optimized Hardware in a 1U (1.75”) high 19” Rack Server Case
- DAC Combines Large Data Storage with Fast Data processing in a Single Server Box

Compared to today’s STP Data Servers…

DAC Servers are Significantly Faster, Cheaper and Simpler to Build

DAC VERSUS TODAY'S CLOUD PROCESSING STP SERVER

Attribute	DAC	STP	Winner
Speed with Size	Increasing	Decreasing	DAC
Processing	Distributed	Centralized	DAC
DDR	Distributed	Centralized	DAC
Storage	Distributed	Distributed	-----
Transmission	Short	Long	DAC
Fault Tolerance	High	Low	DAC

The Result....
DAC is a Superior Server Architecture for DATA Processing and Storage

DAC SOFTWARE SUMMARY

Chief DAC Software Engineer: Dr. Jim A. Brown – Nested Computing – Array Storage Processing Expert, Author of APL2

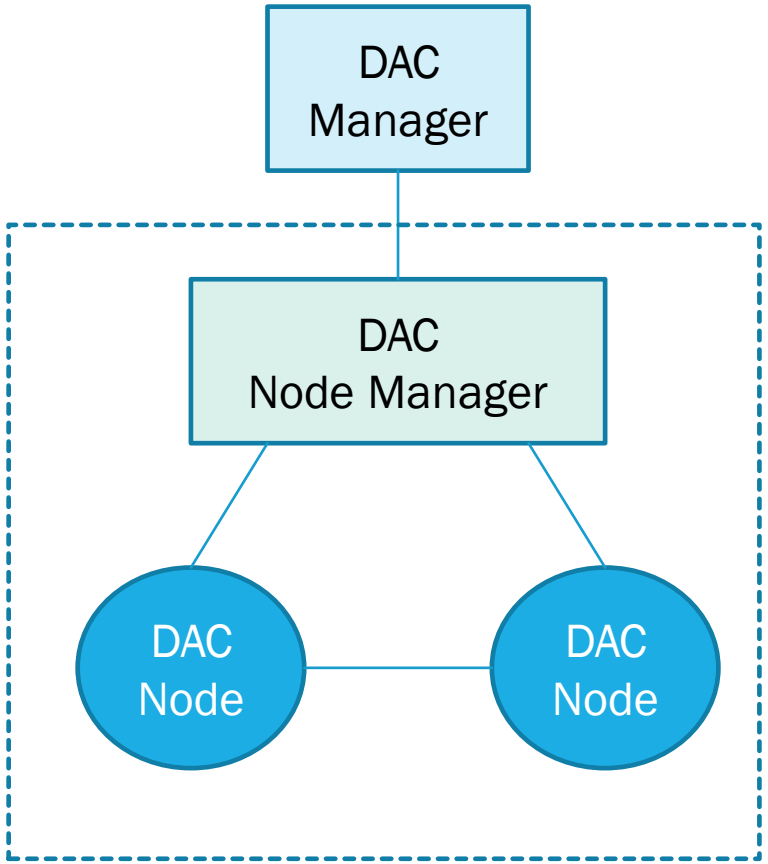
DAC Software:

We use C++ for computation and to implement the interface between the DAC Manager and the nodes.

We use QT for user interfaces to the DAC Manager.

For the GUVI demo we use the NetCDF library.

The DAC Manager has interfaces for C, C++, Java and APL for the end user to access DAC facilities



DAC SERVERS ARE A PARADIGM SHIFT AWAY FROM STP SERVERS

The Fundamental Problem with Modern Computer Systems is Attempting to Process Massive Amounts of Data with the STP Global Storage Computer Model.

The DAC Architecture provides a better solution by moving Mass Storage close to Compute. It does this by using Parallel Computing & Distributive Storage while still providing Singular Computing with Global Storage.

Recap & Questions

- Summary:

A DAC server is a Array Processing Storage Centric Computer Architecture that eliminates data transmission latencies built using of-the-shelf memory, processors, & standard protocol's such as USB & M.2 Storage modules.

For Further DAC Information

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