IEEE SV Tech History Committee June 1, 2015 Meeting:

The pivotal role of EDA in the development of the Fabless Semiconductor Industry

- Panelists:
 - -Suhas Patil, Cirrus Logic
 - -Aart DeGeus, Synopsys
 - -Doug Fairbairn, VLSI Technology
- Moderator: Alan J Weissberger, Fairchild Systems Technology

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IC & EDA Industry- 60s & 70s

- What was the state of the semiconductor industry during the 1960-1970s time frame – technologies, business models, design methodologies, etc? [April 1 2015 panel]
- What was the status of the EDA "industry" during the same time period? PC board layout? ICs?
- What was the role of the chip circuit designer & draftsman?
- Why was it believed that computer layout & cell interconnect coudn't be as efficient as a human?

Questions from Aart deGeus:

- Why did I start with optimization in software?
- Why did synthesis get started in my group in GE?
- Why / how did Synopsys get started?
- What was the impact of the technology on the market creation of an ASIC/semi Fabless world?
- Who had the best place and route tools?
- How has synthesis changed?
- What was the last hold out in using microprocessor?
- What other verification tools did Synopsys have?
- When did IP blocks come along, and what was the evolution path? Where are they now?

Issues from Doug Fairbairn

From 1980-1990 fundamental changes took place in IC/EDA industries:

- Development and widespread utilization of microprocessor based workstations, including Sun and Apollo
- We saw the birth, rapid rise, and subsequent decay of the stand-alone ASIC industry
- The beginnings of the widespread adoption of the IC foundry business model and the directly related growth of the fabless semiconductor industry
- "Birth" and rapid growth of the EDA industry, including Daisy, Mentor, Valid, Cadence, Synopsys, VLSI Technology, Silicon Compilers, and hundreds more.
- The resulting automation of the LSI/VLSI chip design process

Doug Fairbairn (continued)

- The major injection of system design experts into the semiconductor business.
- Chip definition, design time, and complexity become major drivers in the industry

Related ?s for the panelists: 1980s:

- What were the key challenges for the IC/EDA industries as they entered the 1980's?
- What events or developments "set the table" for the rapid changes to both industries, described above?

Questions From 1980-to-1990:

- What was the main focus of the early EDA industry leaders: Daisy, Mentor, Valid (DMV), and others starting in the early 1980's.
- What were the fundamental developments in EDA during the 1980's?
- What issues drove the birth of the ASIC industry? Who were the major players?
- How were the ASIC and fabless semi industries related?
- What fundamental challenges led to the decline of the ASIC industry in the later 1980's and the growth of the fabless semi industry?
- How/why did the term "ASIC tools" evolve?
- How did the EDA industry evolve during this critical decade and how did it fuel the growth of the fabless semi industry?

1980-1990 Continued...

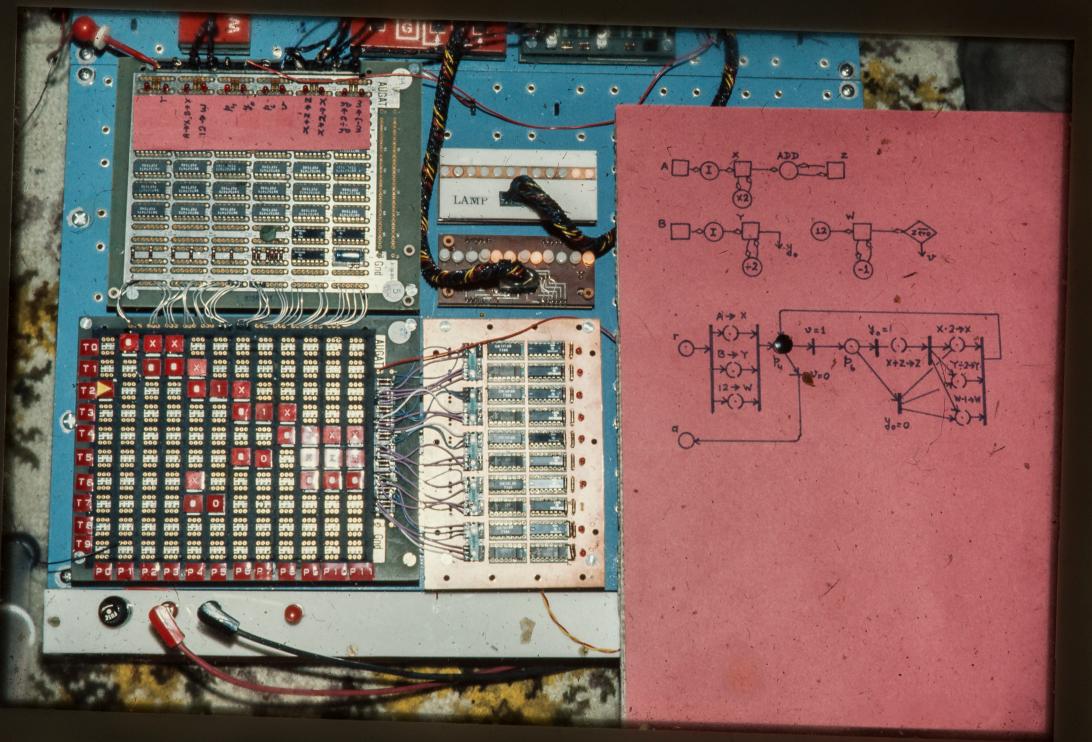
- What was the impact of the Mead/ Conway work during the 1980s?
- What was the role of Silicon Compilers Inc in EDA?
- Compare and contrast the state of the EDA and IC industries in 1990 vs. 1980?

And what about today?

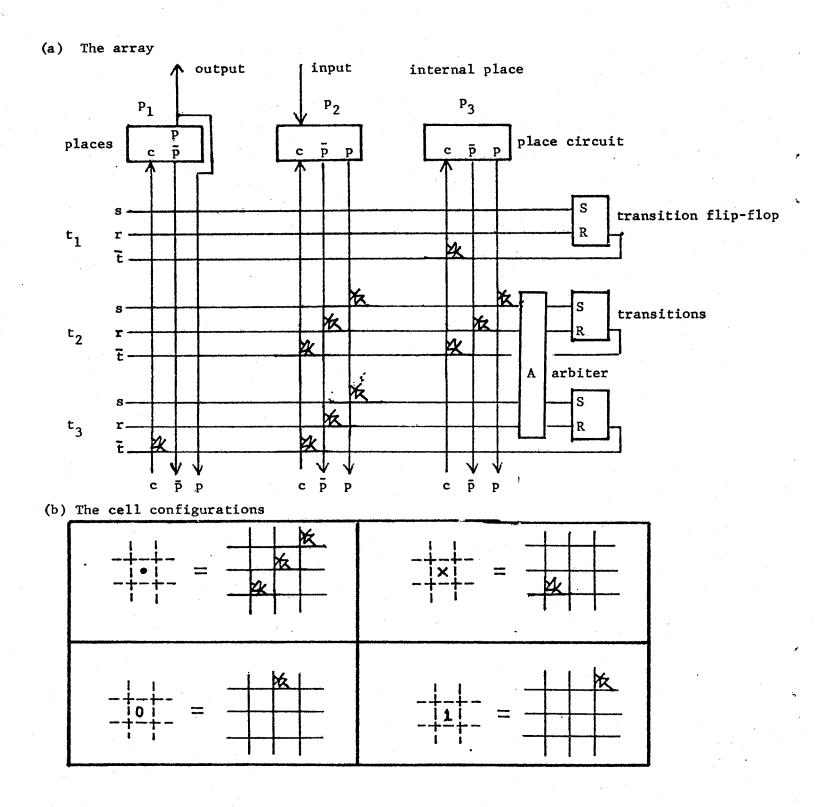
- Status of CAD-LSI tools- generic (e.g. Synopsys, etc) vs company specific (e.g. Intel)
- Why & how did EDA companies get into the business of selling standard cells and SoCs?
- Other questions?

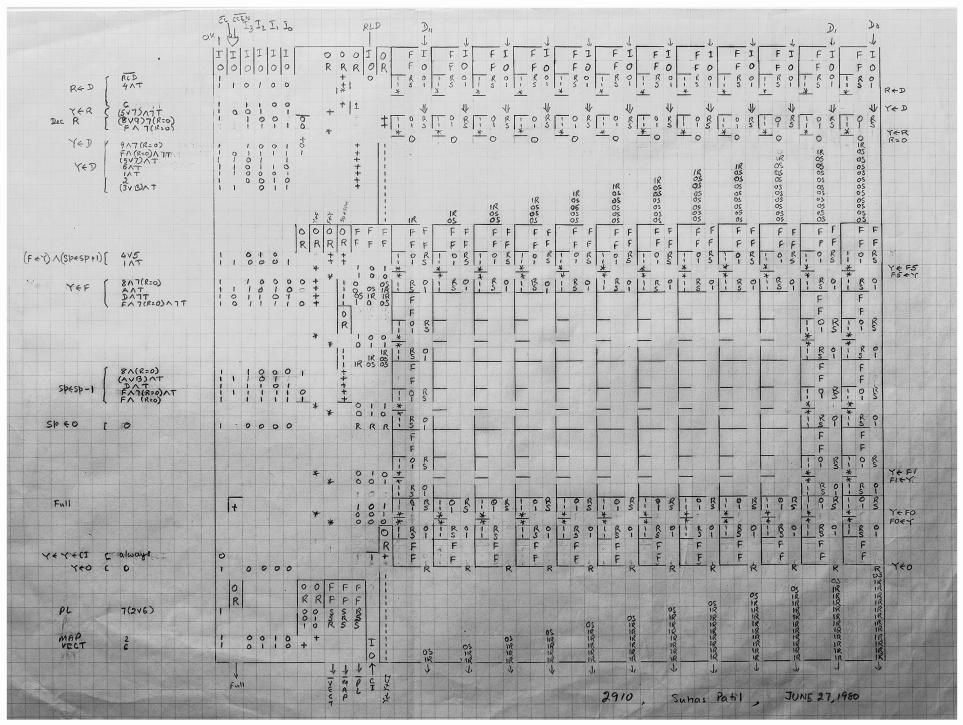
Presentation by Suhas Patil Cirrus Logic

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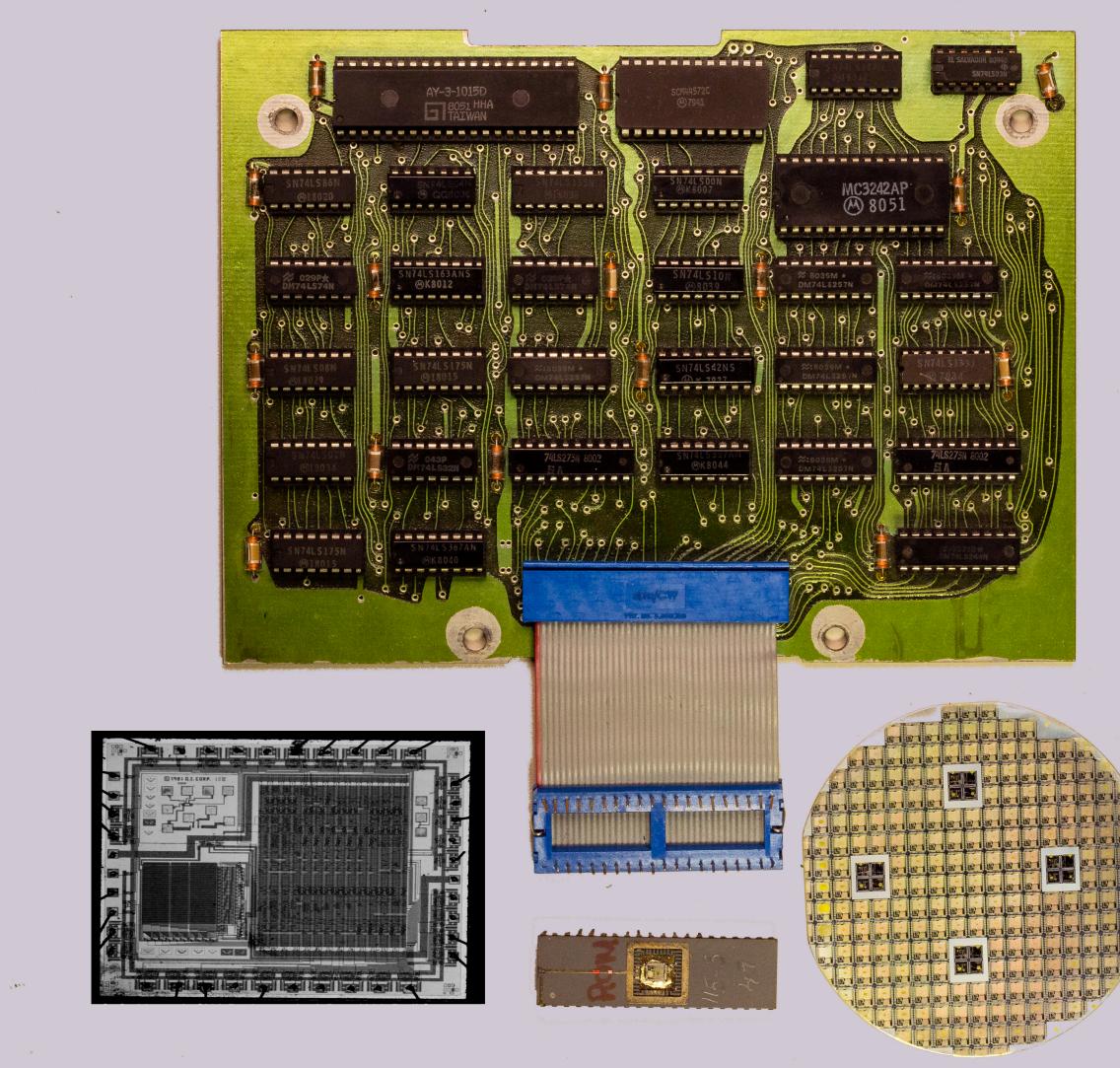
Asynchronus Array 1974-75 MIT





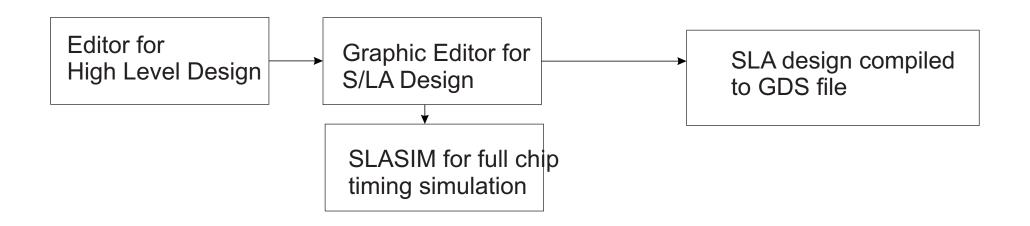
Design of Signatics 2910 chip using SLA symbolic design notation Universiity of Utah 1980

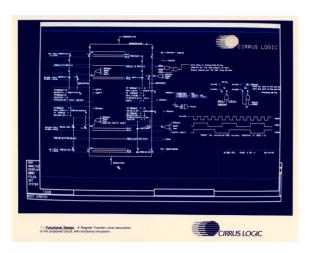
Research supported by The National Science Foundation and General Instrument Corp.

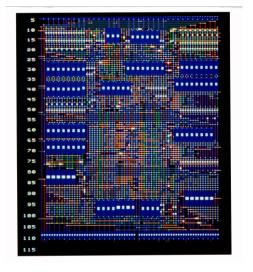


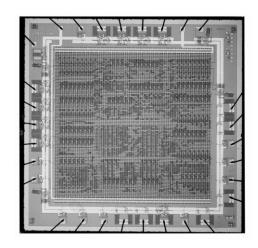
SoC for replacing entire digital electronics of a set top box Designed with Storage Logic Array 1981 Patil Systems, Inc.

STRIDE System for SLA based IC Design





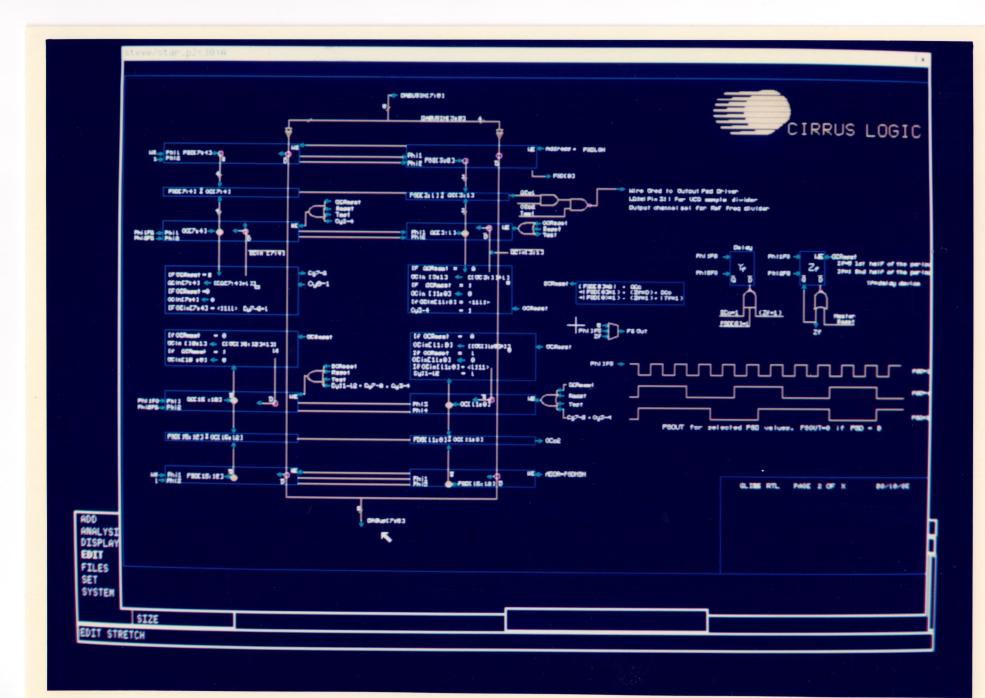




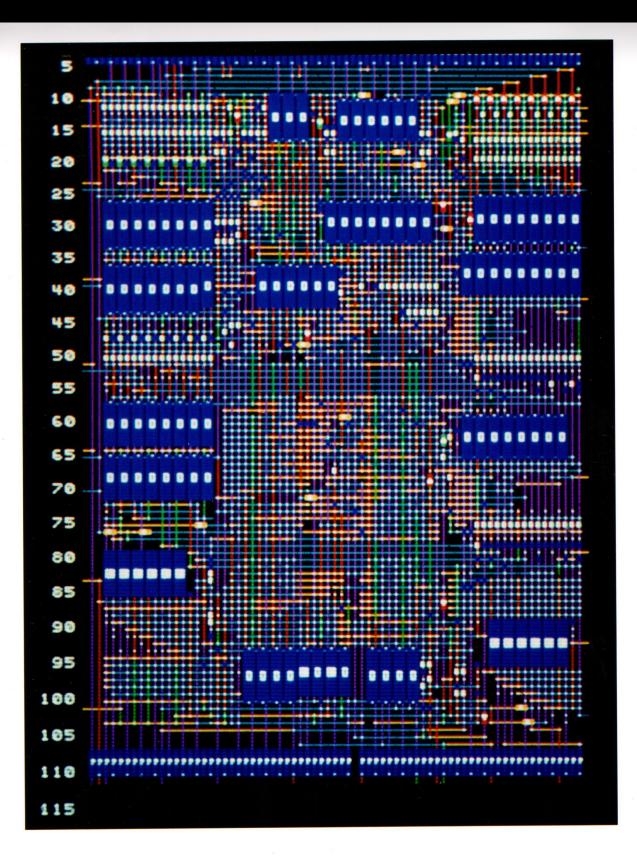
High Level Design

S/LA symbolic Design

Chip made with GDS output of Compilation







Symbolic design entry STRIDE Design System Patil Systyems, Inc 1982

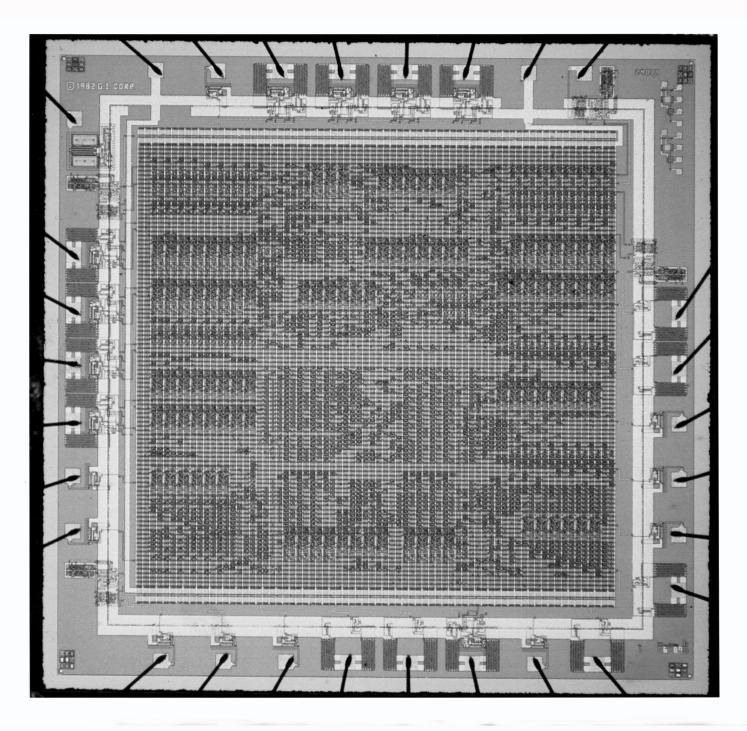
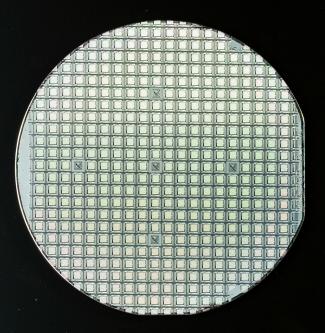


Photo of chip designed with STRIDE System 1982 Patil Systems, Inc

SoC for Set top box STARCOM 5



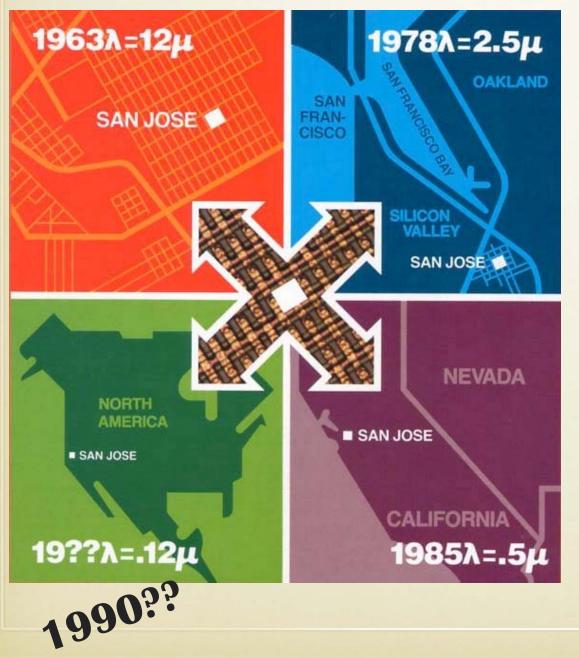
STARFISH 2 MILLION UNITS SHIPPED March 1989

The First Product from CIRRUS LOGIC— A Great Success.

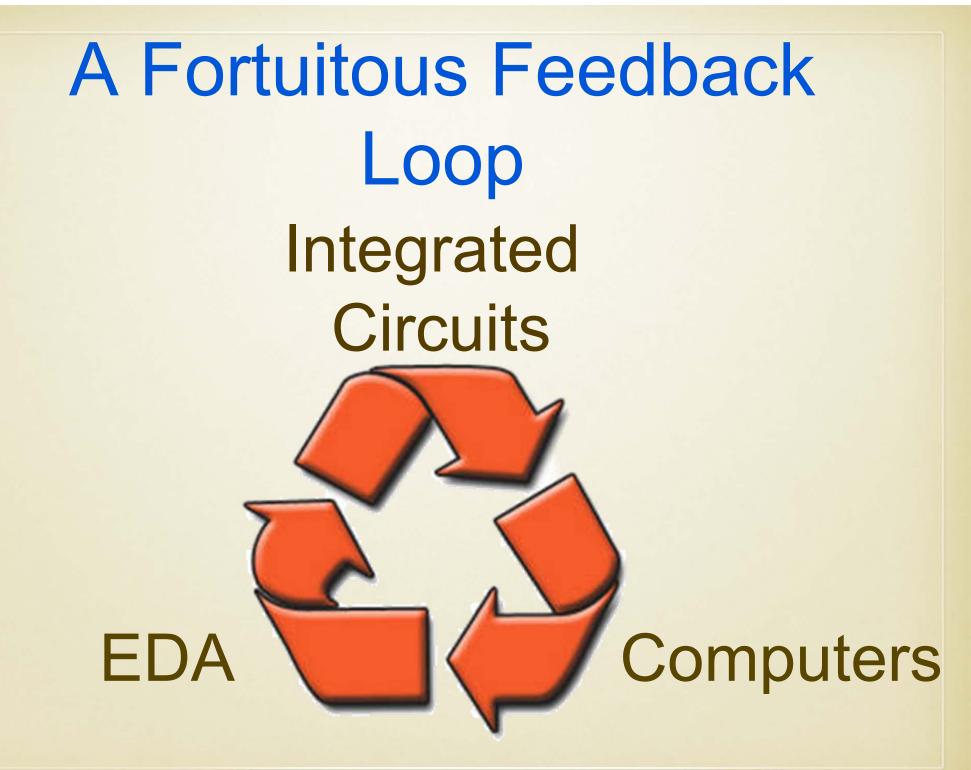
Michael L. Hackworth President and CEO

Presentation by Doug Fairbairn VLSI Technology

Mindboggling Complexity!

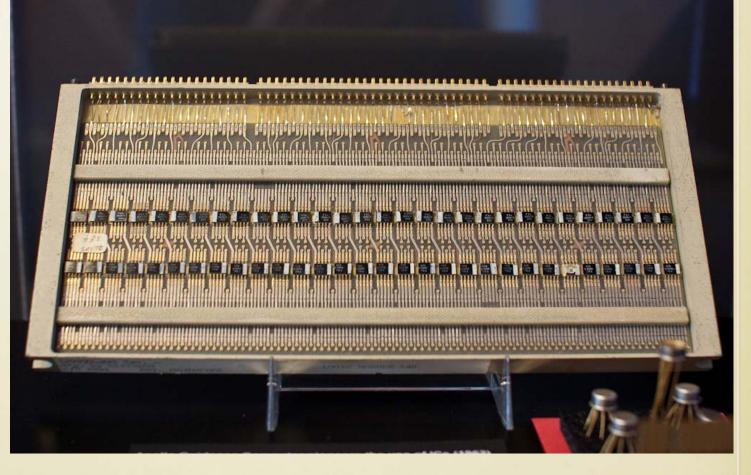


- In 1979, we used Moore's law to draw the map at left.
- Analogy:
 - Metal lines are like roads
 - Metal spacing=1 block
 - At $\lambda = 12\mu$ (25 μ process), chip complexity matched that of a downtown area
 - At 45nm (.045μ!), λ = 22nm and chip would cover Europe/Asia at urban densities - with 9 levels of interconnect!



Apollo Guidance Computer (1962)

First computer to commit to use integrated circuits



Computer History Museum

1960's Highlights

1K

1960 69	61 62	63 6	65	66	67	68
1st Comm. IC	1st Comp Graphics Demo AGC		Moore's Law PDP-8	Early ASIC/CAD	Applicon Intel	Moon Landing

Semiconductors

- Basic process technologies and circuit configurations developed
- Early applications: Apollo Guidance Computer (1962), Minuteman (1963)

Computers

- Mainframe dominates
- Apollo Guidance Computer for moon program first to use ICs
- Design Tools: Focus on back-end design
 - Early R&D and first tools at IBM, Bell Labs, and RCA
 - Early application to IC design



The Mead-Conway Timeline

- 1967 Conversation with Gordon Moore sparks Carver Mead's interest in how we will design 1M transistor VLSI
- 1971 First VLSI design class
- 1976 Beginning of Caltech/Xerox PARC collaboration

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- 1978 = Introduction to VLSI Systems introduced MIT
- 1979 VLSI class spreads to a dozen universities
 - 100+ universities within 2-3 years.
 - Chips fabricated for students
 - Workforce for the 1980's and beyond



Lambda Magazine

LAMBDA/VLSI Design Magazine was a place to share ideas among the new group of VLSI designers



Important Contributions of M/C Methodology

- Opened the world of IC design to a whole new generation
 - Fuel for the design revolution of the 1980's
 - Attracted involvement of system architects and software engineers.
- Moved the design focus from optimizing at the transistor level to optimizing the system for IC implementation
- Fostered the creation of a whole new generation of design tools
- Laid the foundation for the productivity growth required by Moore's law

1970's Highlights ^{30K}



- Semicordatictors
 - Moore's law in driver's seat: design explosion
 - The name "Silicon Valley" is coined and becomes center of IC explosion
- Computers

1K

- Mainframes dominate, minicomputers grow rapidly, personal computers appear
- Modern personal computer born: Xerox Alto incorporates bit-map display, mouse, windows, ethernet, and laser printing
- Design Tools
 - IC CAD industry takes hold: Calma and Applicon digitizers dominate
 - 1970: 4004 designed with custom logic simulator with layout on rubylith
 - 1979: New VLSI Design Methodology launched

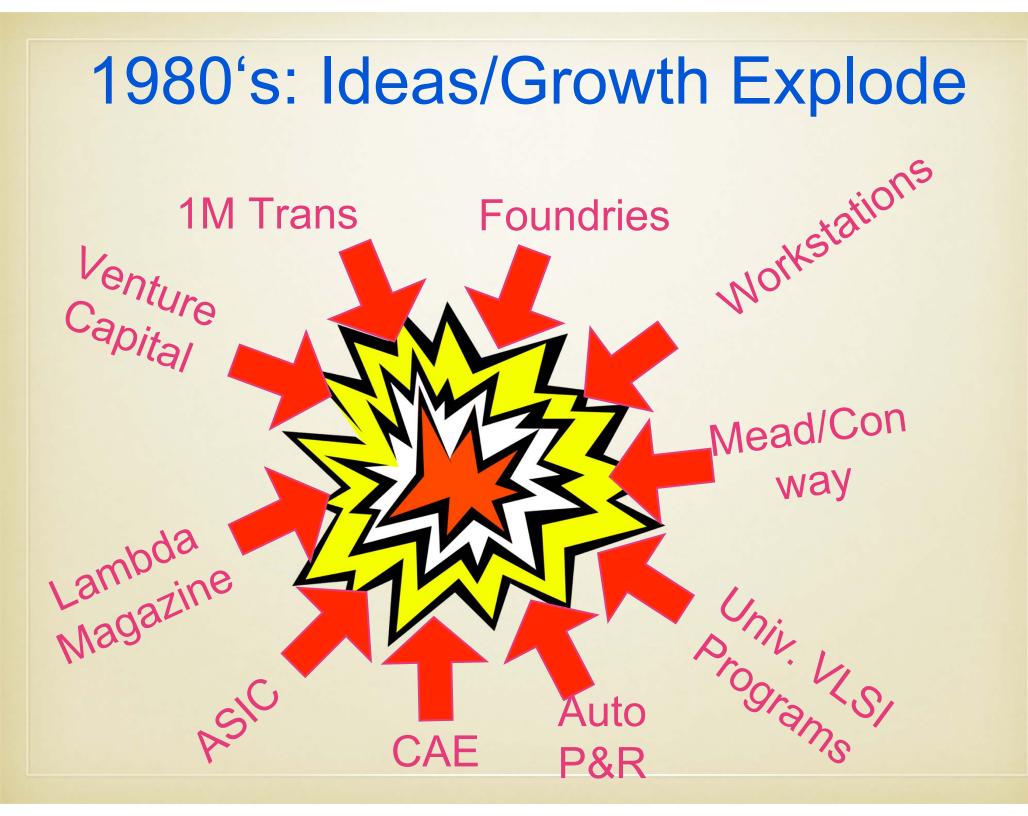
1980's Highlights 1M

1980 89	81	82	83	84 8	35	86	87	88
Apollo Comp	Daisy Mentor Valid VLSI Tech,	SUN	"ASIC" Coined DRACULA DRC Intro	Gateway / Verilog	Synops ys	TSMC	Cadenc e Daisy/C adnetix	Cadenc e acquires Gatewa y

- Golden Age of EDA and ASIC great synergy
- DAC exploded in size and importance First Exhibits in 1983
- Many transitions/advancements

30K

- Mainframe to workstation based design
- Design capture moved from paper to graphic-based to languagebased
- Automated layout finally replaced manual placement and routing
- Major players and methodologies in place for the 1990's and beyond



Background paper prepared by Suhas Patil for Alan Weissberger moderator of IEEE Silicon Valley History panel June 1, 2015

Cirrus Logic

Cirrus Logic started out as Patil Systems, Inc. in Salt Lake City, Utah on January 6, 1981. Patil Systems moved to Silicon Valley in Dec. 1983 and changed its name to Cirrus Logic in 1985. Mike Hackworth joined Cirrus Logic as CEO in January 1995.

Cirrus Logic is a fabless semiconductor company that depended on Storage Logic Array based EDA system STRIDE developed by Patil Systems. Without this EDA system Cirrus Logic would not have been a viable company.

The STRIDE design system was used by system engineers with no prior experience in chip design to design complex high volume consumer IC chips such as for set-top boxes, Hard Drive, PC and Laptop graphics and communication chips for consumer and PC industry.

STRIDE was unique in that its technology base could be retool a new fab or a new process in less than a month allowed Cirrus Logic flexibility to switch fab as necessary. This was so because the tiles (cells) used by compiler in Storage Logic Array (STRIDE) made use of only fewer number cells compared to ones in Standard Cell design of industry. Also the cells were much smaller in area compared to a cell in a standard cell design.

In early days Cirrus Logic sourced wafers from General Instruments, Atari, Sharp, Sanyo and Toshiba. Once TSMC came on line Cirrus Logic became a major customer of TSMC. At one time Cirrus Logic was sourcing wafers from 12 different fabs. Cirrus Logic used to manufacture same part in multiple fabs.

First commercial chip of Patil Systems was a SoC for set-top box of General Instrument Corp.(Jerrold division) completed in 1981 using partly developed STRIDE EDA system. Second commercial chip was designed as a standard part for semiconductor division of GI in 1982. Third commercial chip was a set-top SoC for GI designed in 1983. This chip was designed using STRIDE system by two system designers in 4 months and working in set-top box in less than 6 months.

Stories

When did you get interested in design EDA tools for IC? I became interested in EDA tools for IC design around 1979 to be able to design IC based on Storage Logic Array methodology of building an IC.

Suhas Patil at MIT 1970 to 1975: Concept of Storage Logic Array was born from work done on efforts to find a systematic way for designing self timed (clock less) digital circuits that would be correct by construction. Intel had already built 4004 and number of gates available on an IC chip was doubling every 18 months. This quest let me to propose a architecture for IC that was called Storage Logic Array.

Patil at University of Utah From 1976 to 1970: I went to University of Utah to prove viability of Storage Logic Array by building IC using this method of design. At university of Utah I had access to advanced semiconductor lab of General Instrument Corporation. This effort was supported by both by National Science Foundation and by General Instrument Corporation. First experimental IC based on Storage Logic Array was build at University of Utah using I2L process. Second IC was built using NMOS process.

Patil Systems Inc. Patil Systems Inc. was founded in January 1981 with funding from General Instrument Corporation. Jerrold division of GI was in set-top network business. To reduce the cost of set-top box they wanted a single chip solution for the digital portion of the set top box. In effect they wanted SoC (system of a chip) solution for set-top boxes. Set-top being a consumer product the IC needed to be low cost and the design time of the IC from concept to working in the system had to be less then one year. This was year 1980 and there were no commercially available design tools or technology that provided this capability. General Instrument believed my team could do this with Storage Logic Array mythology of design. To use this method an EDA system to do the design had to be built. Patil Systems, Inc. was formed to first build the needed EDA system and then to be a fabless semiconductor company. Semiconductor fab at General Instrument was ready to offer foundry service to Patil Systems.

By end of 1982 STRIDE EDA system built by Patil Systems was a complete and system engineers with no traditional IC chip design experience could design digital VLSI chips. It provided for symbolic input of the design using graphical editor, full chip timing simulation and some verification tools and a silicon compiler to output GDS file ready to be handed over to the manufacturing department.

First chip designed with STRIDE system was an SoC for set-top box that was taped out in December of 1981. It was made in 5 micron NMOS process. Even though originally this chip was viewed only as a test of the STRIDE system and regarded as a back up design to chip that was being designed as a custom chip, this chip is the one that went into production as the custom design was not ready when the production of set-top boxes had to be stated.

STRIDE EDA system was intended to be used by system designers with knowledge of the functionality of the system to be implemented as a VLSI chip.

STRIDE system ran on UNIX operating system. Until SUN Microsystems came out with SUN workstation STRIDE was run on PDP 11. In 1995 STRIDE was ported to run on SUN workstations. All tools in STRIDE ran on SUN workstation including chip level simulation and the silicon compiler for generating GDS file.

System designers specified/designed the chip at a symbolic level using a graphic editor in a table like manner using symbols such as 0, 1, + and D (for storage).

At any time in design one could produce net list that could be simulated using SLASIM a timing simulator capable of full chip simulation. One unique feature of SLASIM is that it had an embedded LISP with ability to patch up defects by putting rappers around circuits or modules and continues the process of simulation and verification with out having to create a new net list.

Synopsys

- 1. Aart when and were did you start Synopsys?
 - Aart worked in GE in Research Triangle in North Carolina. Founded in 1986 by Dr. <u>Aart J. de Geus</u> and a team of engineers from General Electric's Microelectronics Center in Research Triangle Park, North Carolina, Synopsys was first established as "Optimal Solutions" with a charter to develop and market ground-breaking synthesis technology developed by the team at General Electric.
- 2. What opportunity did you see in building new EDA tools when you started Synopsys?
- 3. I understand that Synopsys offer products for both synthesis as well as logic optimization. Which product gained traction first and why?
- 4. Who were your first customers? Who did they use Synopsys tools? What other tools did they use?
- 5. Which fabless semiconductor companies were first to adapt use of synthesis tools and how critical were the tools in success of those fabless companies as semiconductor companies.
- 6. Did you work on formal

Chips and Technologies

Chips and Technologies (C&T) was founded in Milpitas, California in December 1984 by Gordon A. Campbell and Dado Banatao.

Its first product, announced September 1985, was a four chip EGA chipset that handled the functions of 19 of IBM's proprietary chips on the Enhanced Graphics Adapter. This was followed by chipsets for PC motherboards and other computer graphics chips. Ravi Bhanagar was founding engineering VP. His group designed the products of the company within 9 months form the start of the company. I spoke with him in person.

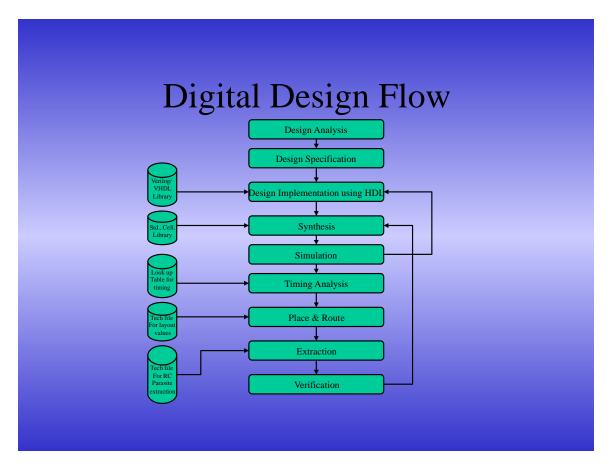
Tools: To start with they has access to tools provided by Toshiba as provider of gate array and standard cell. They designed their own standard cells. Toshiba's tools were really LSI logic tools obtained though strategic alliance with LSI logic. Chips and Technology built their own logic simulator because commercially available simulator was too expensive. Simulator ran on Amdahl computer (main frame computer).

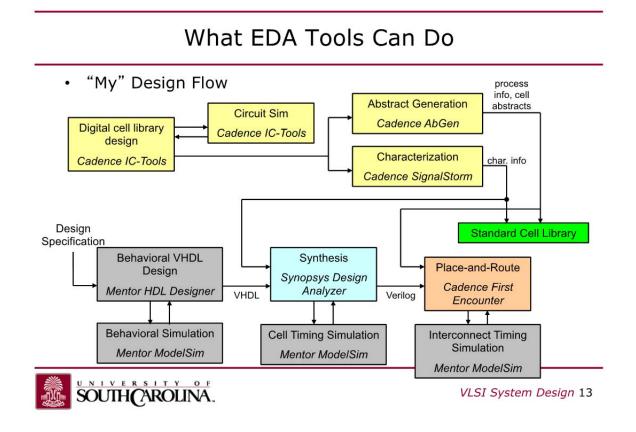
Altera

Altera was founded in 1983 by Robert Hartmann, Michael Magranet, Paul Newhagen, and Jim Sansbury, visionaries who capitalized on the research of the day. They believed that semiconductor customers would benefit from a userprogrammable standard product alternative to gate arrays. To address these market needs, Altera's founders pioneered the first reprogrammable logic device, the EP300, giving birth to an entirely new market segment in semiconductors. This new, flexible solution beat traditional standard products to market and launched Altera's reputation as a semiconductor innovation leader.

I spoke with Bob Hartmann about how they designed their early chips. The designed their first set of chip using handcrafted full custom IC method to achieve highest density of chip possible. Chip layout drawings were digitized to create GDS files. SPICE was used to simulate and optimize the design. Tools for customers to program the FPGA were built in house. Design Flow:

A good summary of the design flow of VLSI design is Power Point slide from Cadence and another from University of Southern Carolina.





These two slides show major tools that are needed.

- Tools are generally referred to as front end tools and back end tools.
- Back end tools deal with physical layer of design including design rool checking tools. They are also used for creating Standard Cell Library and simulation model for the library. Place and route tools also are generally considered to be back end tools.
- Front end tools are used by system designers to specify the system and implement it using high level register transfer level language such as VERILOG or VHDL. Ideally same simulation tolls allows engineers to simulate the high level design and the resulting gate level design. Static timing analysis tools are used to find timing of critical paths and help designer speed up the design and improve tolerance of the design to variations in speed of processed chips.
- As EDA has evolved and chips have become larger and larger a host of tools for analyzing design has emerged. Checking differences between two designs is an example of it. Tools for signal integrity and power consumption and heat distribution as also example of these tools.
- Tools for generating design of components inside IC such as memory and other well defined structure have emerged.

Major issues/problems that had to be solved for CAD/EDA

1970's

- CALMA and Computer Vision: Early in 1970's the mask layers were prepared by hand drawing and cutting of rubylith sheets. Masks for processing wafers were made by photographing the rubylith sheets. Making masks by cutting rubylith was very tedious and unforgiving if any mistakes were made. This problem was solved by companies such as CALMA and Computer Vision provided digitizing systems and layout entry systems to provide more flexibility and directly produce GDS files representing layout of the mask layer.
- SPICE circuit simulator: To properly design even small scale IC it was necessary to characterize the behavior of the transistor a well as the circuit at the circuit level. This need was fulfilled by SPCE program that was designed by Laurence Nagel in UC Berkley. SPICE1 was completed in 1973, SPICE2 in 1975 and SPICE3 in 1989. Spice remain key simulator for accurate simulation at device and component level.
- Zilog was started in California in 1974 by Federico Faggin and Ralph Ungermann,^[4] as a fabless semiconductor company but they built a fab in 1977.

1980's

1980's was period of rapid development of EDA tools for design of VLSI.

- Number transistors available for logic design on IC were going from 10,000 to several hounded thousand. Designs needed to be done by system designers. The transistor count allowed one to implement SoC chips and ASIC chips were now possible.
- It was necessary to design chips are logic level as well as suing high level design language
- Clock speeds were also were heading towards Gigahertz. Chip level simulation as well as static timing analysis tools were needed.
- Place and route tools were needed to automate layout of the IC.

To address these needs many EDA companies were formed to address these needs.

- Daisy Systems, Mentor Graphics, and Valid Logic Systems were all founded around 1981 and collectively referred to as **DMV**. They provided schematic capture tools for gate level design of digital systems. These tools were used for both board level designs using SSI, MSI and processor chips sold by semiconductor companies as well as for capturing digital design to be converted to IC chips.
- Design rule checking: ECAD produced Dracula in 1983 for design rule checking.

- Physical IC design tools: Around 1983 Solomon Design Automation (SDA) System provided tools for physical design of IC. Standard cell design could also be dine with tools from UC Berkley.
- Cadence Design Systems was founded in 1988 by James Solomon, Alberto Sangiovanni-Vincentelli and Jiri Soukup, and was a merger between Solomon Design Automation (SDA) and ECAD. Joseph Costello was appointed as CEO from 1988–1997, and Cadence became the largest EDA company during his tenure. Cadance was primary provider of backed EDA tools for the industry.
- High Level Design Language: With initiative of DoD industry came up with VHDL language for functional design of digital systems. VHDL took time for being adapted because of its complexity.
- Gateway Design Automation came up with alternative high level design language called VERILOG along with Simulator for VERILOG designs as well as the logic level designs that representing the high level design.
- Logic optimization and synthesis tools: Founded in 1986 by Dr. Aart J. de Geus and a team of engineers from General Electric's Microelectronics Center in Research Triangle Park, North Carolina, Synopsys was first established as "Optimal Solutions" with a charter to develop and market ground-breaking synthesis technology developed by the team at General Electric. Synopsys adapted VERILOG as high level language for synthesis of digital gate level circuits.
- Tools for Gate Array and Standard Cell design. Semiconductor companies that offered gate array and standard cell design products had their own place and route tools in early 1980's.
- Cirrus Logic (Patil Systems) had their own design methodology based on Storage Logic Array. Patil Systems by 1982 had a complete set of EDA tools to do systems on a chip A for large price sensitive consumer market ASIC chips. System designers without any prior experience in chip design were able to design the SoC.
- Another effort in building successful silicon compiler was made by Silicon Compilers Inc. Johannsen, Mead, and Edmund K. Cheng subsequently founded Silicon Compilers Inc. (SCI) in 1981. Edmund Cheng designed an Ethernet Data Link Controller chip in 1981-1982 using structured design methodology, in order to drive the software and circuit-library development at SCI. The project went from concept to chip specification in 3 months, and from chip specification to tapeout in 5 months. Fabricated using a 3-micron NMOS process, the chip measured 50,600 square mils in die area, and was being marketed and manufactured in volume-production by 1983 under license from SCI. Not too many chips were made using methodology developed by SCI.
- Started in 1979 by a trio from Fairchild Semiconductor by way of Synertek – Jack Balletto, Dan Floyd, and Gunnar Wetlesen – and by Doug Fairbairn of Xerox PARC and Lambda (later VLSI Design)

magazine. VLSI Technology was unique company in that it developed both EDA tools and it built a fab for use by systems companies. (Doug will have more about VLSI Technologies).

Impact of EDA on development of fabless semiconductor companies.

- In the late 60's and most of 70's the challenge for semiconductor companies was at device and semiconductor process level. Traditional semiconductor companies which had fabs had developed design and analysis tools that were very closely tied to their semiconductor fabrication process. To be a successful semiconductor company the company had to have advance process and be able to make semiconductor devices of better performance specification. As they started making medium scale and large scale chips they built tools to meet their specific needs as they arose to support the design of the chips.
- Fabless semiconductor companies could be successful only when the process semiconductor process technology had matured and was stable and critical factor in having product was not just having fab capacity but to have products to run in the fab. As the chip complexity increased to 10,000 and 100,000 transistors the critical factor became having product design to run in the fab.
- Critical factor in designing a chip became knowledge of the system representing the application specific integrated circuits. The designs had to be done by system designers which out having to work at the device level. These companies invested not in fab or tool development but in development of IP in form of application specific chips.
- Early fabless semiconductor companies that provided FPGA products such as Xilinx and Altera initially used traditional full custom method to design FPGA but built their own EDA tools for customer to program the FPGA.
- Fabless chip companies such as Chip and Technology used EDA tools provided by foundry that supplied gate array or standard cell based chips. The complexity of the chip was limited by gate array technology but they were able to do business as they sued their system knowledge to design the chips.
- Companies such as LSI logic is interesting in that they made it possible for system companies such as DEC to use their system knowledge to build IC for their products. LSI logic initially built its own tools including logic simulator.
- Cirrus Logic was an exception to other fabless semiconductor companies. It had complete tool set needed by system engineers to chips. Its designs were also easily portable to different available fabs.
- In second half of 80's and early 90's as entrepreneurs saw the concept of fabless company working, many fabless semiconductor product

companies got formed using specific system knowledge. The companies fully depended on commercially available EDA tools. Without commercially available EDA tools only few fabless companies would have succeeded in the market.