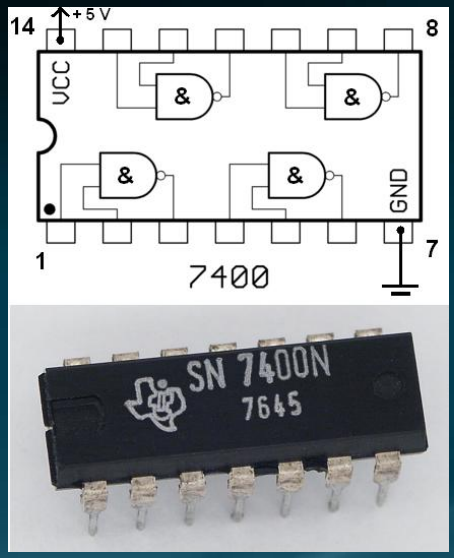
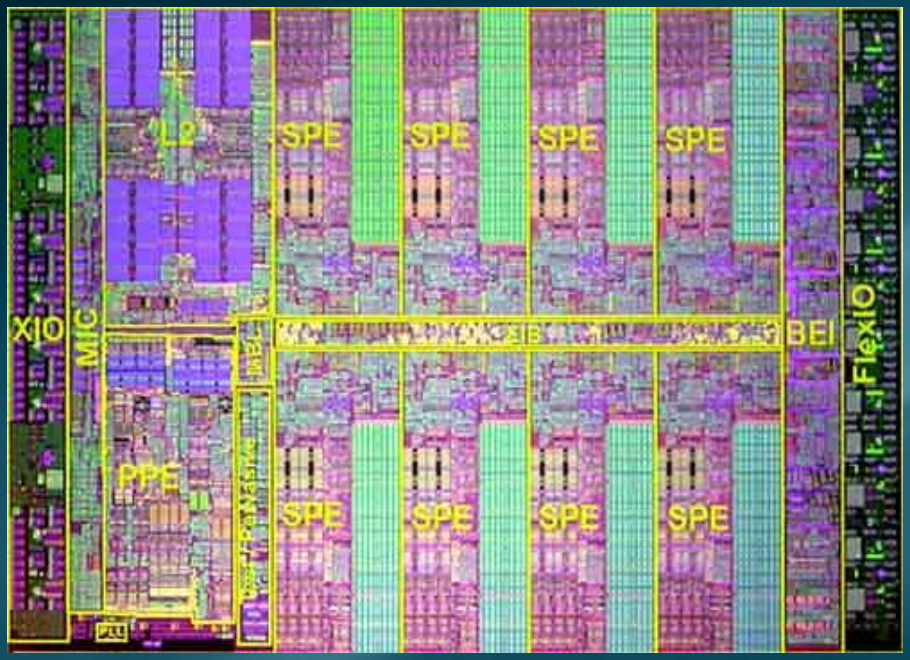
Rethinking Analog: Digital Driven Analog Design

Mark Horowitz

Chip Design Is Growing Up

- We have come a long way
  - From op amps and SSI components
- To today's mega SOC





IBM Cell Processor

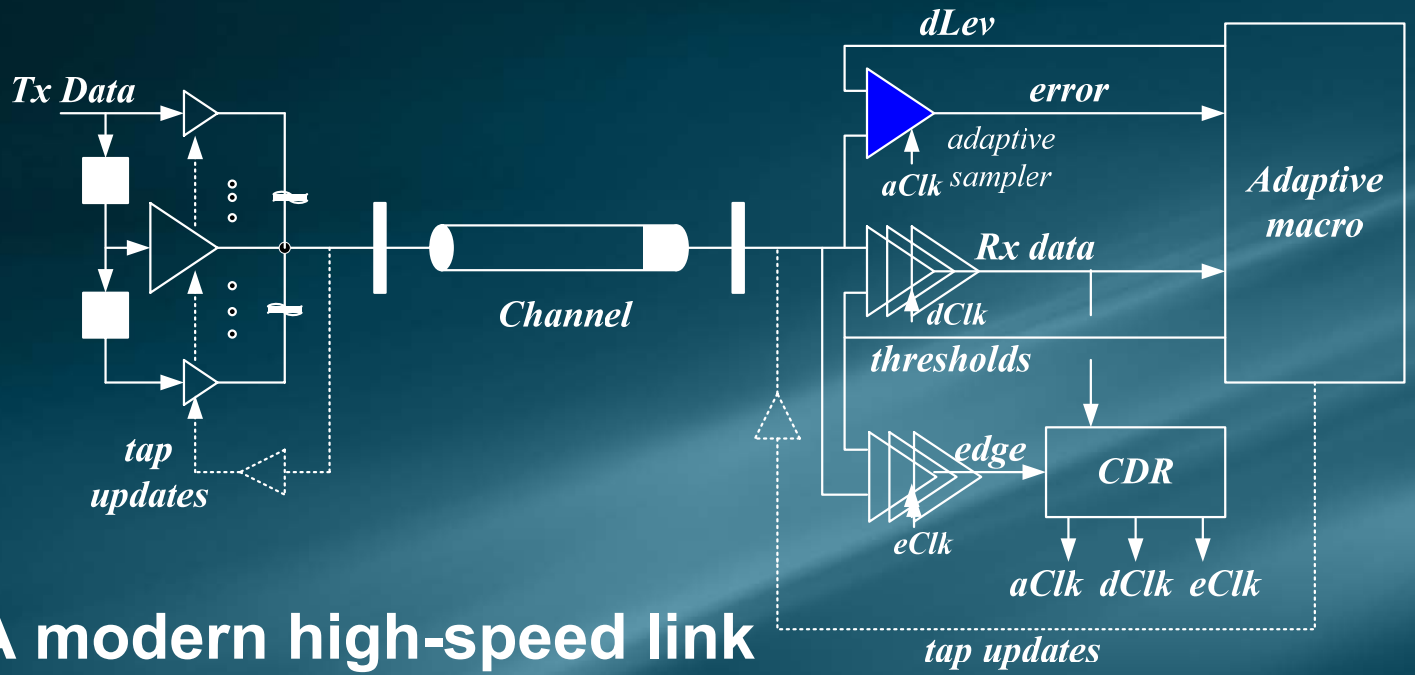
And Analog Design Is Getting Harder

- Requirements are growing
  - More bits, higher speeds, lower power
- Transistors are getting less precise
  - Ft might be better
  - Matching is worse
  - Vdd range smaller

- Analog a component in a larger system

Our Current Solutions …

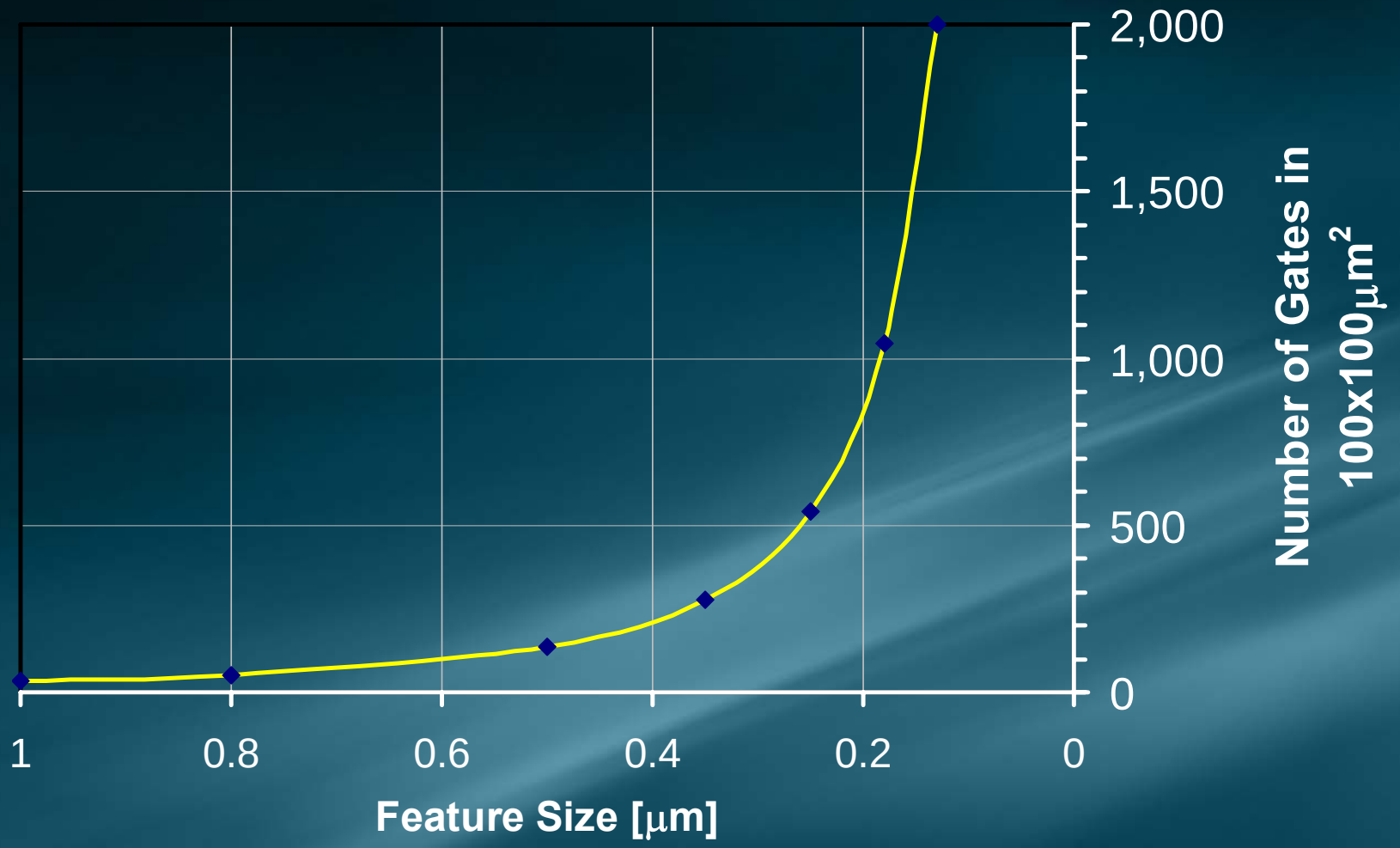
- Digitally assisted analog
  - ADC calibration, PA and DAC pre-distortion, mostly digital PLLs, …



A modern high-speed link

Why Are We Moving This Way?

- Digital logic is small



Why Are We Moving This Way?

Digital power scales better than analog

- Digital
  - Energy/gate transition CV^2
    - (NAND2) in 0.13μm CMOS is order 10**fJ**
- Analog
  - State-of-the-art 10-bit Nyquist ADCs is order 1nJ
  - 1nJ/10fJ= 100,000

- For energy
  - Tens of thousand gates are "free"

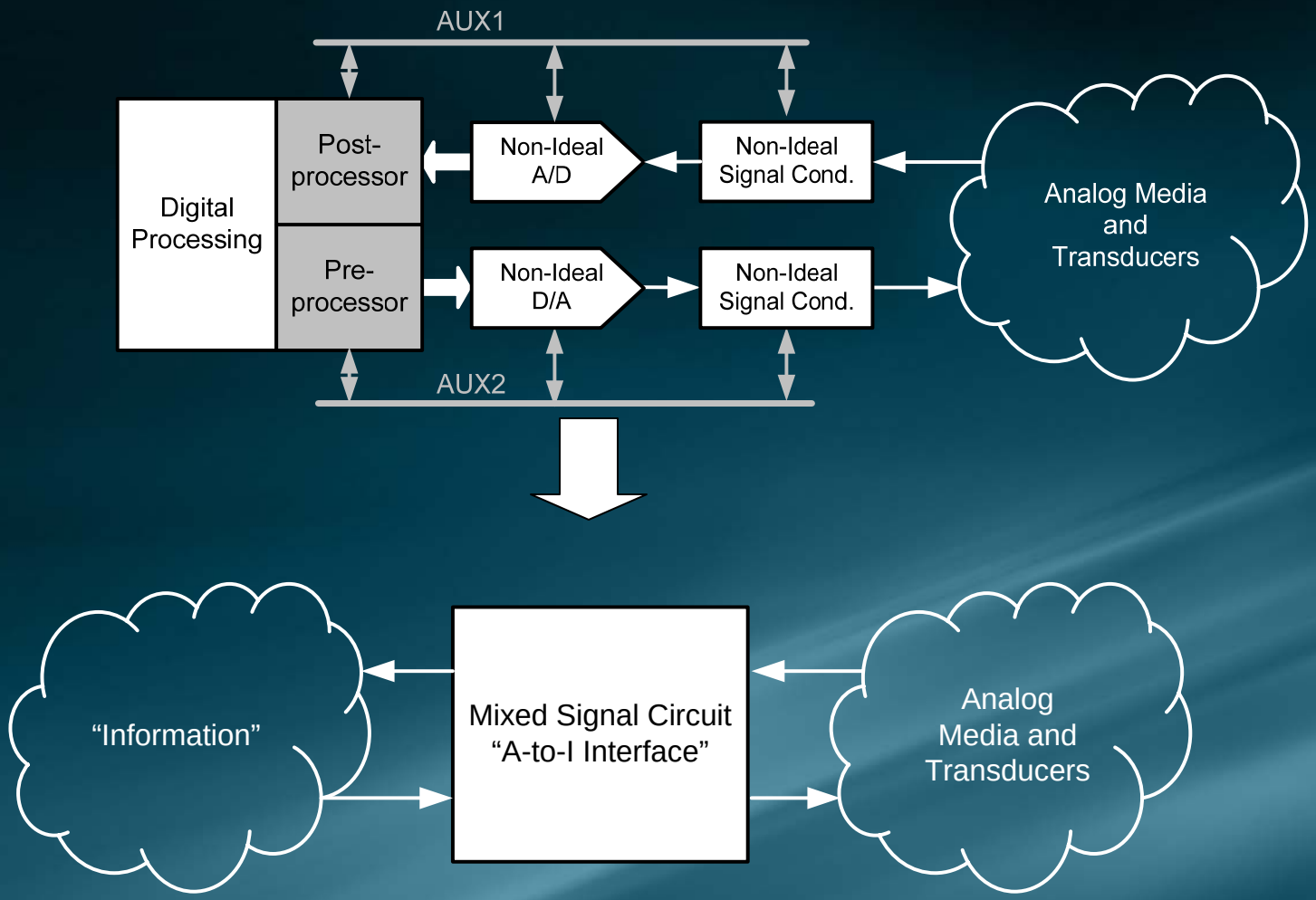
What Is the Problem?

- Today’s integrated chips need analog
  - > 50% of all chips have some analog
- Only 2% of transistors are "analog"
  - Analog/digital design times are comparable
- Average number of re-spins grows from one to three when analog is on board
  - Big impact on cost and time to market

Embracing Change:

- Rather then using digital logic to fix stuff
  - And incrementally change design
- Ask the question:
  - Given nearly unlimited digital processing power, what analog operations are essential to preserve the information in the analog signals?
  - Does this provide a new set of building blocks for analog designs

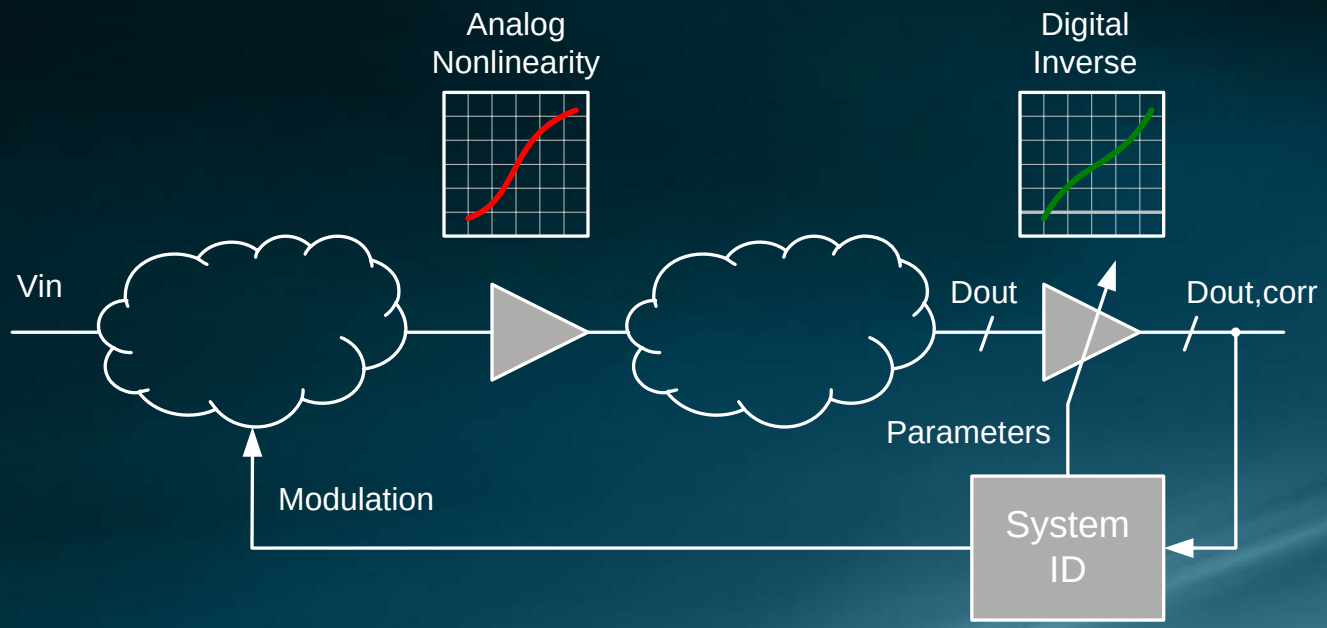
Rethinking Analog



New System Level Analog Approach

- What does the system really require
  - Is there a way to change the system?
- What is the minimal requirements
  - For measuring signals, might only need resolution
  - Accuracy, linearity, etc can be corrected
  - Digital logic is much easier to design
- Look at three examples
  - ADC, link front end, supply noise measurement

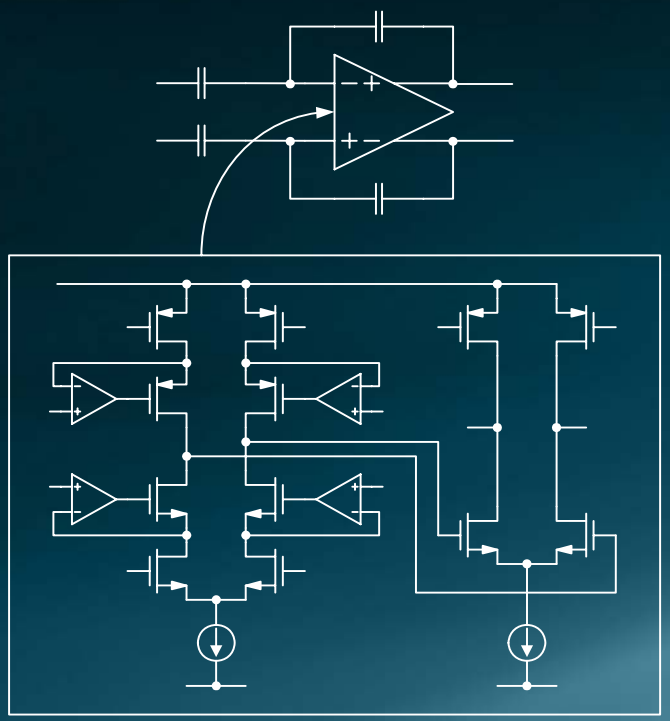
Digital Nonlinearity Compensation



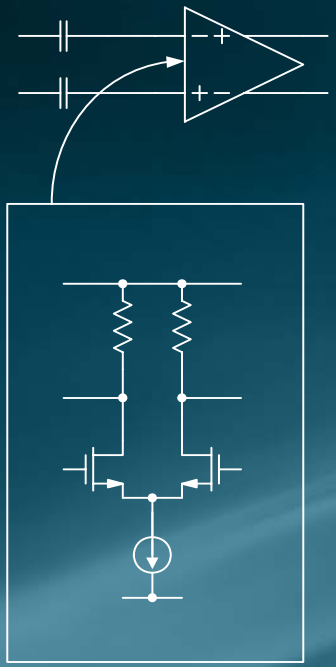
- Use gates to measure and correct distortion
  - Not analog circuits
- Must track changes overtime
  - Correct for analog drift

Back to the Future

Precision Amplifier

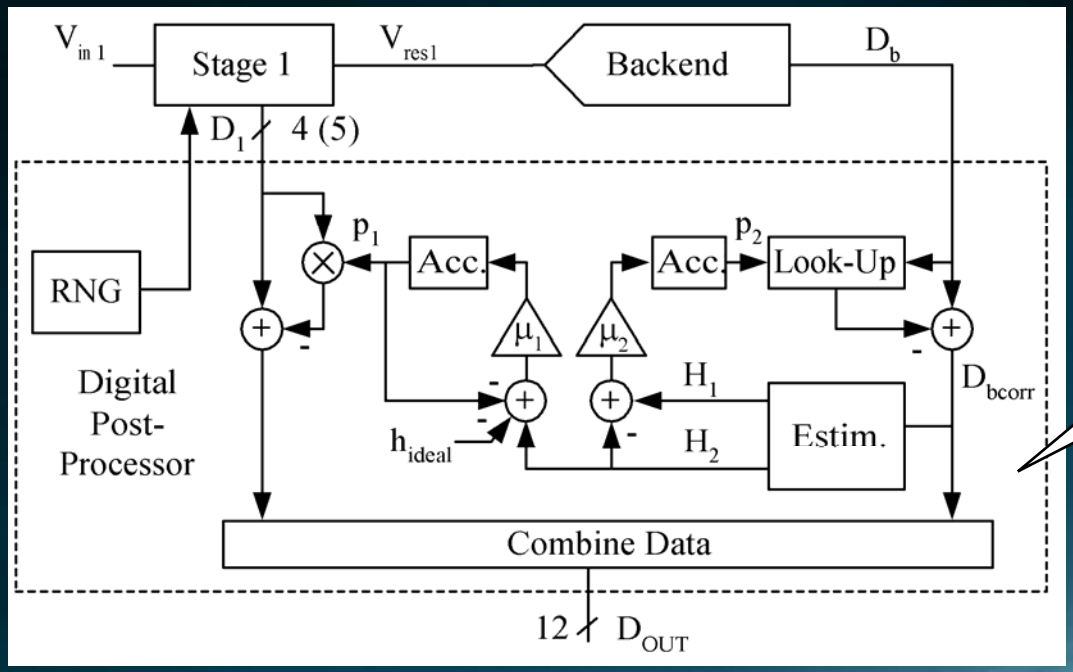


“Open loop“



+ Lower Noise
+ Increased Signal Range
+ Lower Power
+ Faster
- Nonlinear
  - Use DSP to linearize!

Example: Pipeline ADC Prototype

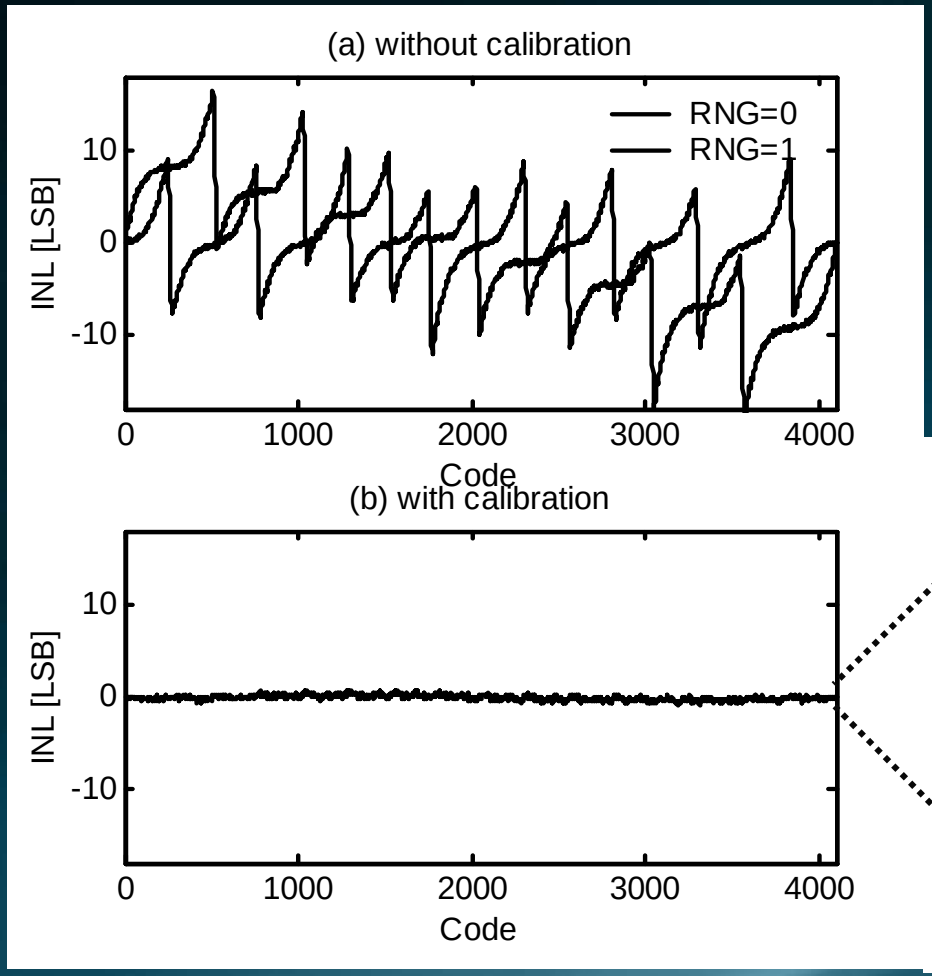


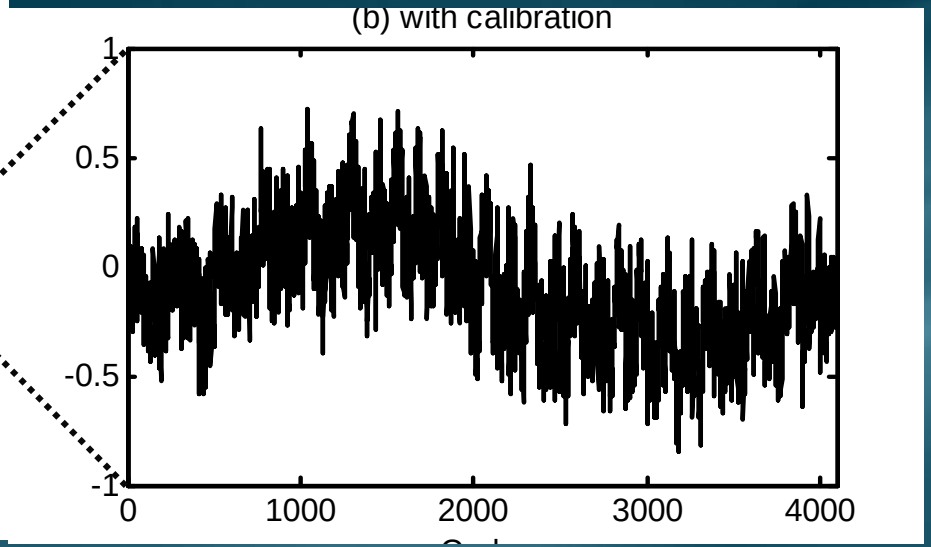
~8400 Gates (0.042mm² in 0.13µm)

[Murmann, Boser, JSSC 12/2003]

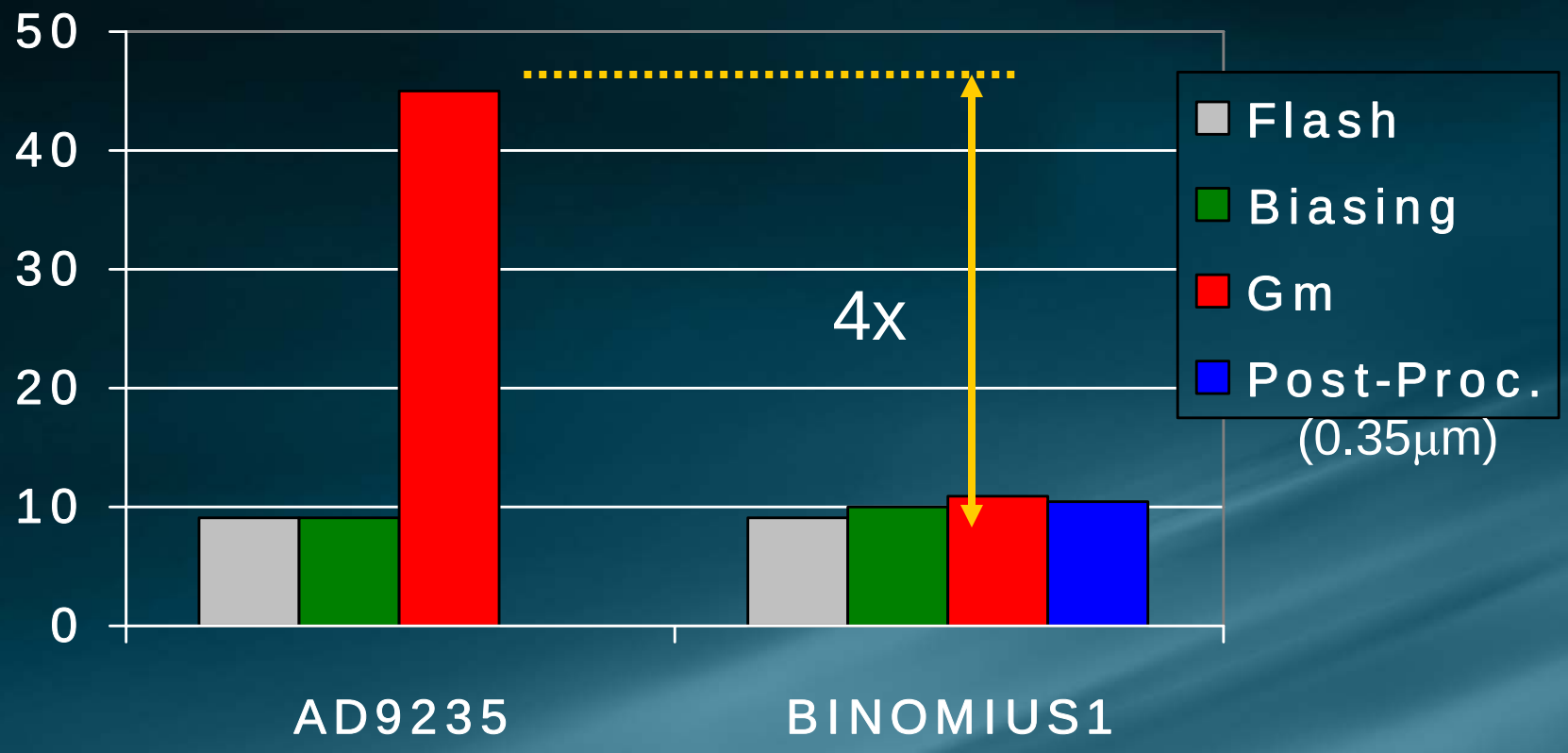
- Open-loop amplifier in first, most critical stage
- Statistics based system ID
  - allows continuous parameter tracking
- Judicious analog/digital co-design
  - Only two correction parameters (linear and cubic error)

Measurement Results



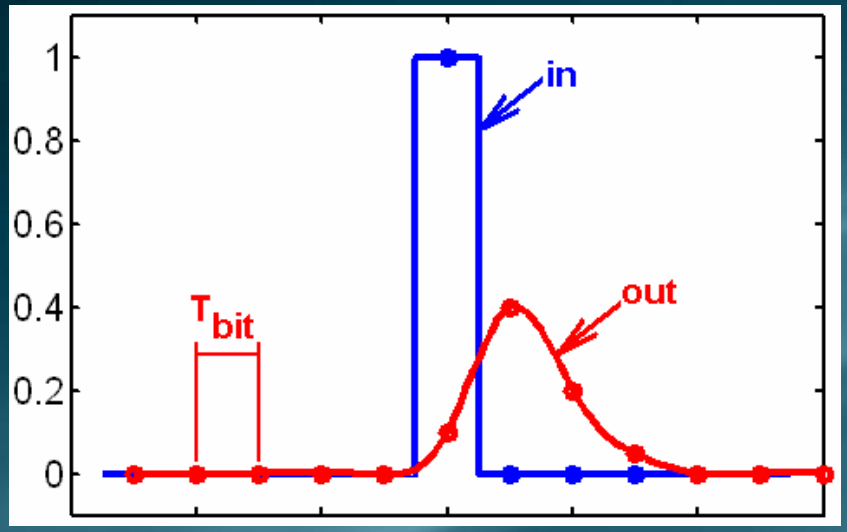


Stage1 Power Breakdown



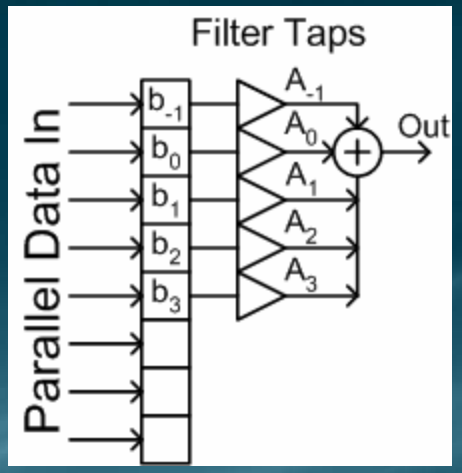
High-Speed A/D for Wireline Links

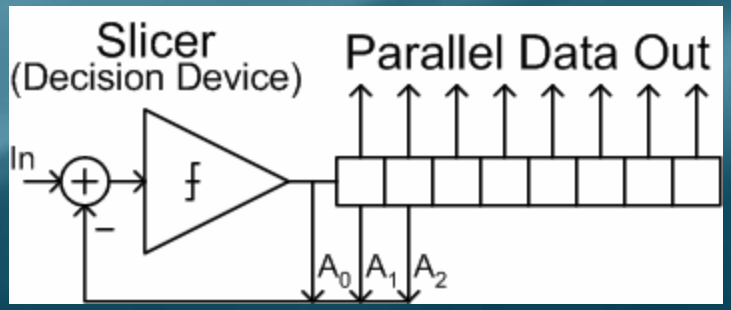
- Real cables have high-frequency loss
  - And reflections
- So data pulses get filtered



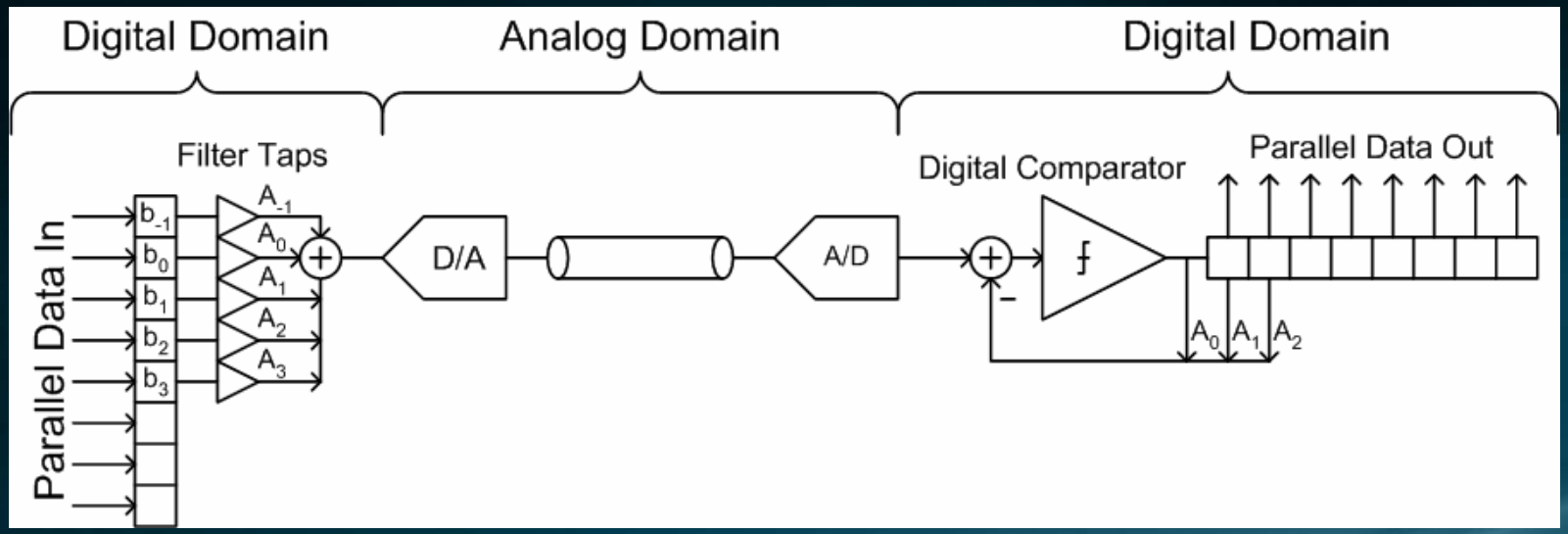
Equalization

- Create inverse filters to compensate
  - FIR transmitter filter popular
    - Attenuate low freq to flatten freq
    - Cleaner signals, but smaller as well
    - Can take many taps
  - DFE input filter
    - Subtract off residual error
    - Number of taps limited if done in analog domain





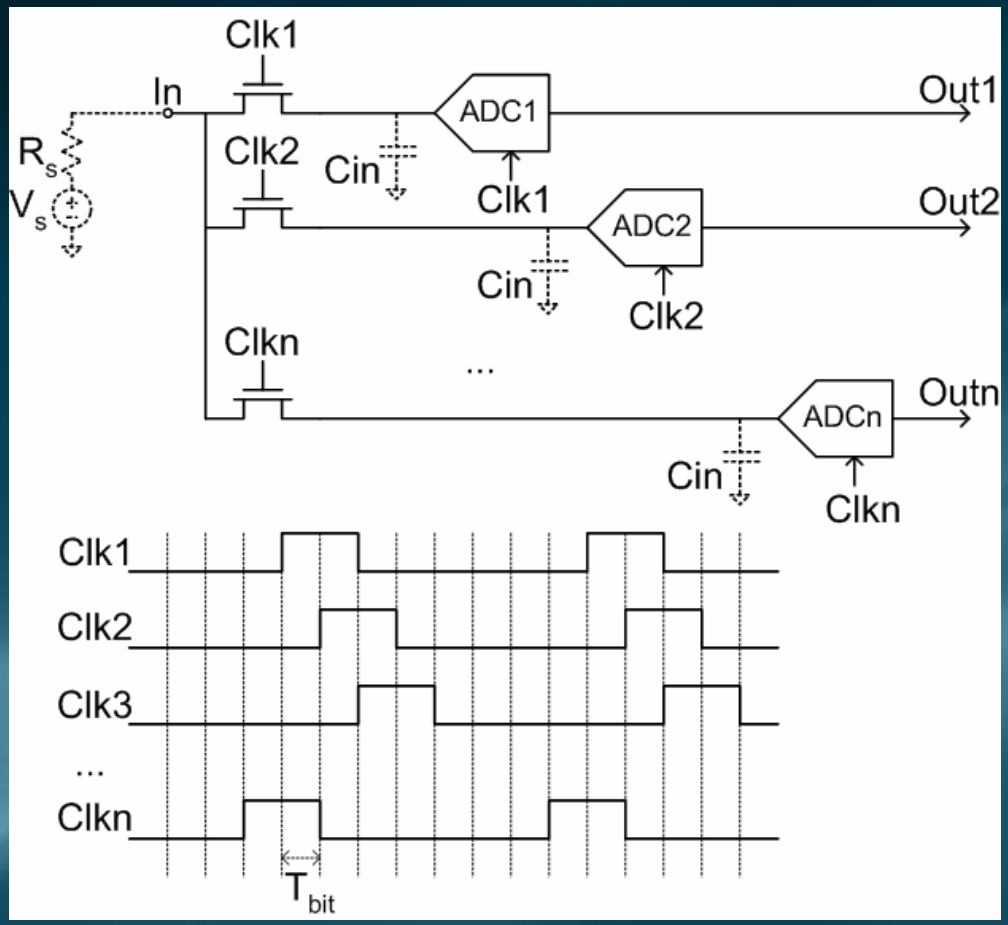
Complex Equalization Implies Digital



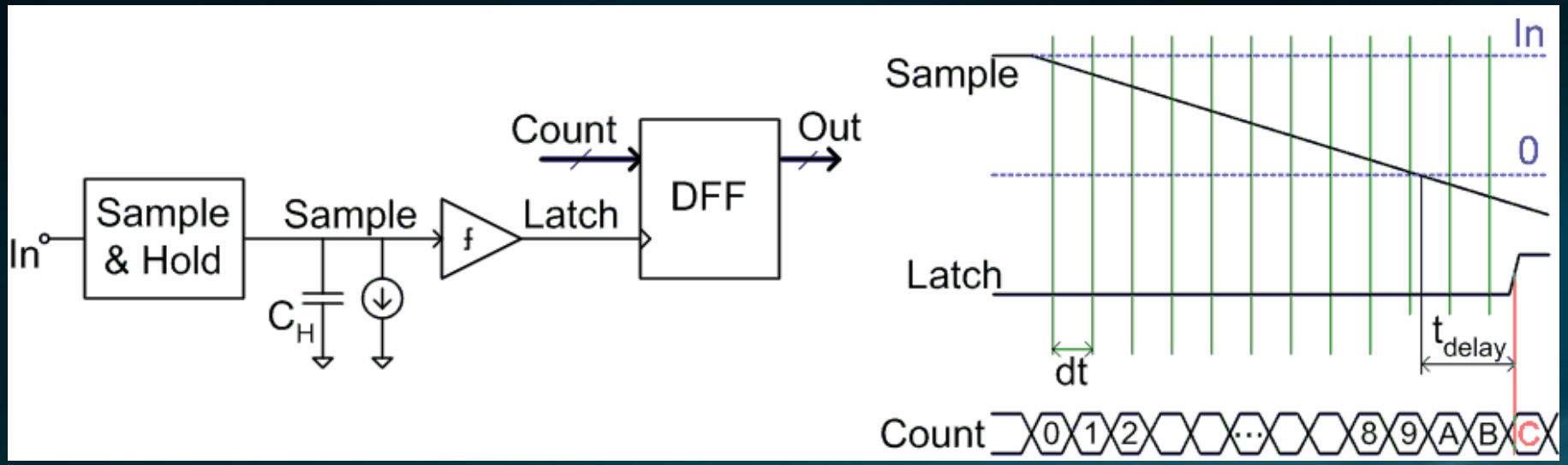
- But a high-speed links needs a very fast ADC
  - And power efficiency is key
- Target 25Gsps, ~100mW, 4-5bit performance
  - Leverage system environment, constraints

System Will Have Great Clocks

- And lots of transistors
- Interleave ADC
- Leverage clocks
  - To simply ADC



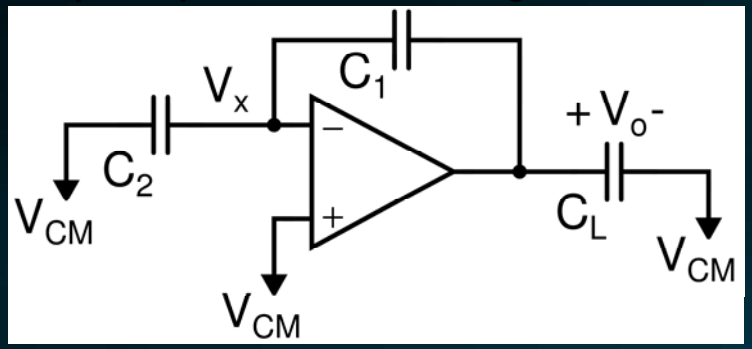
Use Single Slope Converter

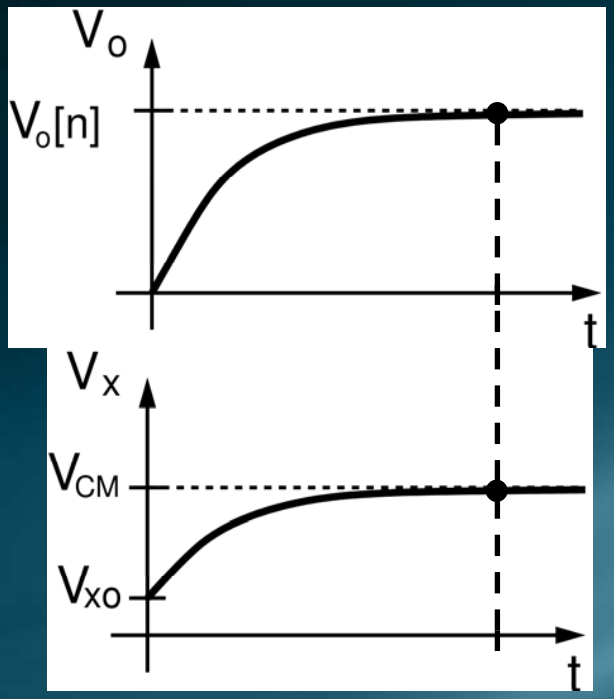


- No linear amplifiers
  - Only a comparator (almost digital element)
  - Creates a number to voltage conversion
    - Need not be linear
- Tconv = dt * 2^{Nbits}, but dt and N are small

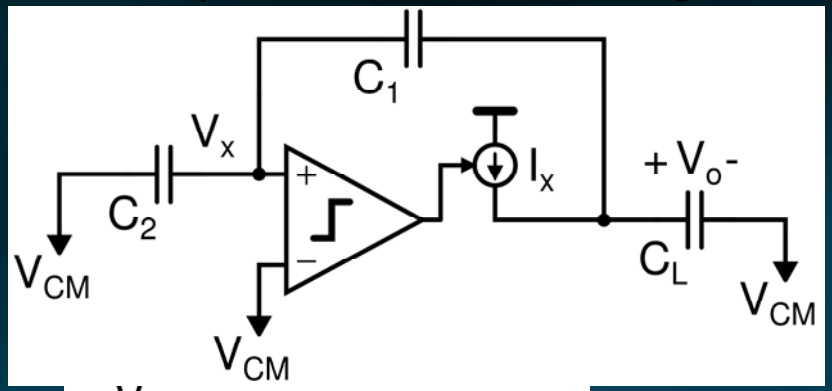
New Paradigm For Charge Transfer (Aside)

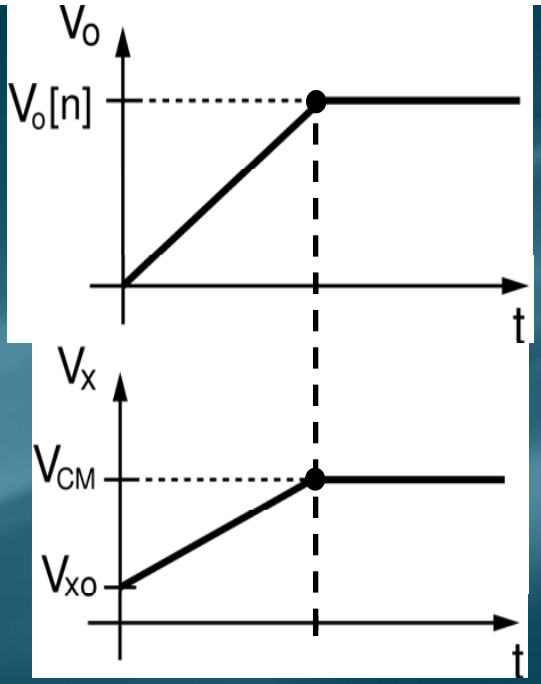
Op-amp forces virtual ground





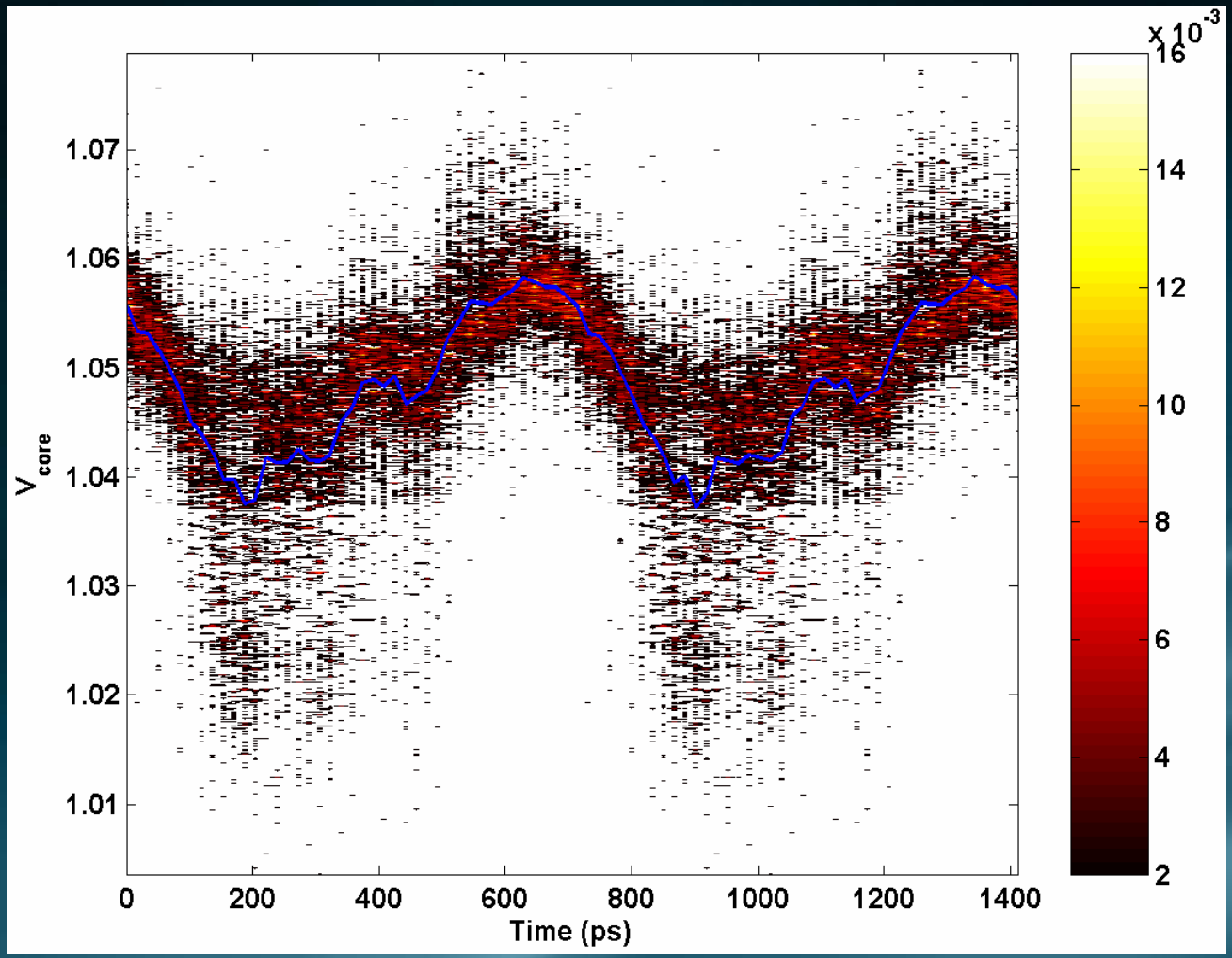
Comparator detects virtual ground





[Lee, Sodini, MIT]

90nm Itanium Microprocessor Noise

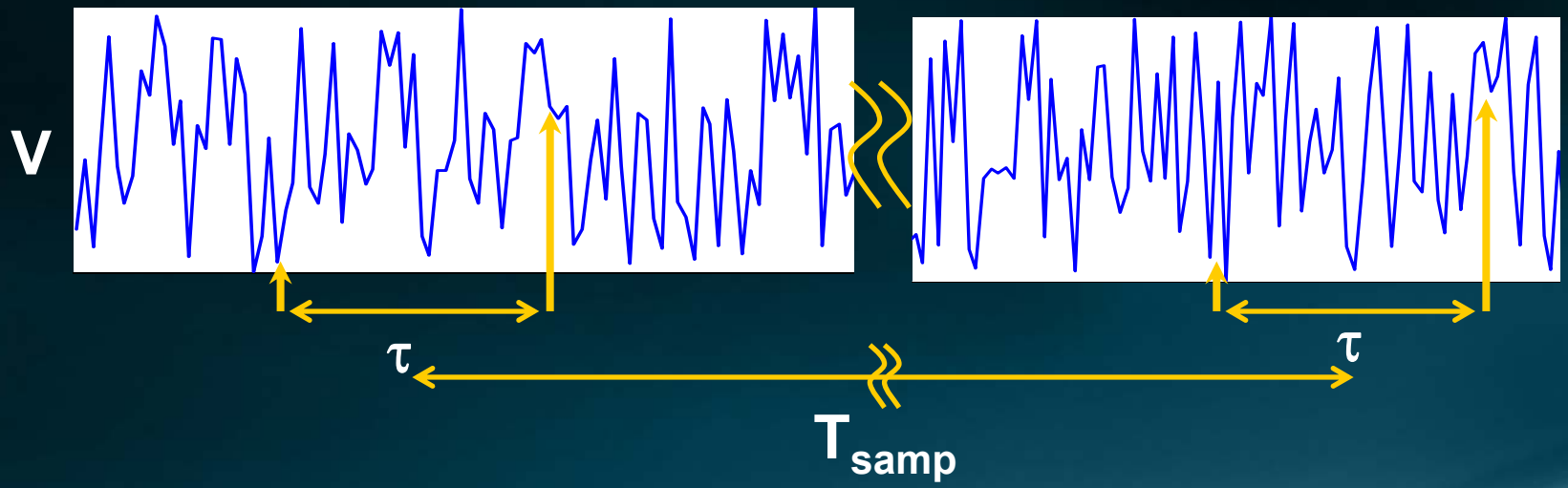


S. Naffziger, B. Stackhouse, T. Grutkowski, D. Josephson, J. Desai, E. Alon, and M. Horowitz, "The Implementation of a 2-Core, Multi-Threaded Itanium Family Processor," *Journal of Solid-State Circuits*, Jan. 2006.

Measuring “Random” Supply Noise

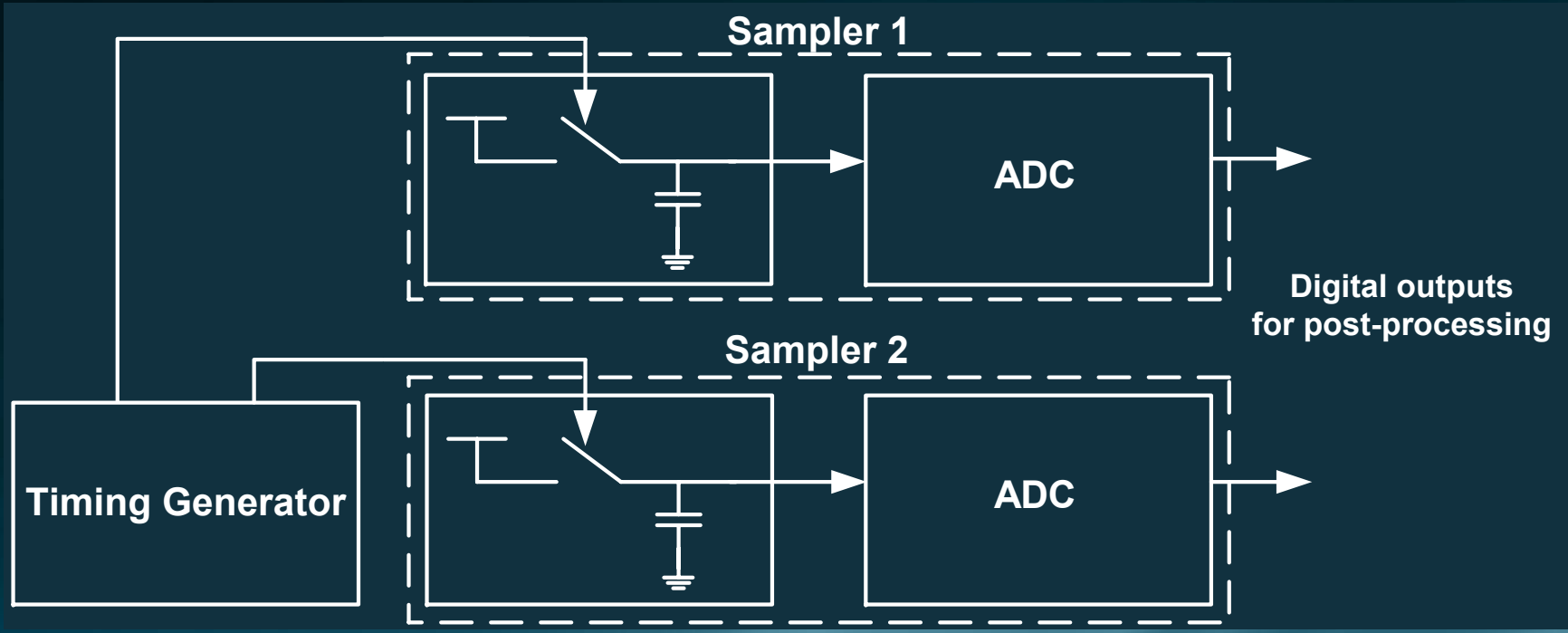
- Supply noise is basically deterministic
  - But extremely complicated to calculate
- “Noise” is a label for a random process
  - Can be characterized by its frequency spectrum
- Measure autocorrelation to find spectrum of supply noise
  - Extension of sub-sampling technique
  - Only needs 2 low rate samplers

Measuring Autocorrelation



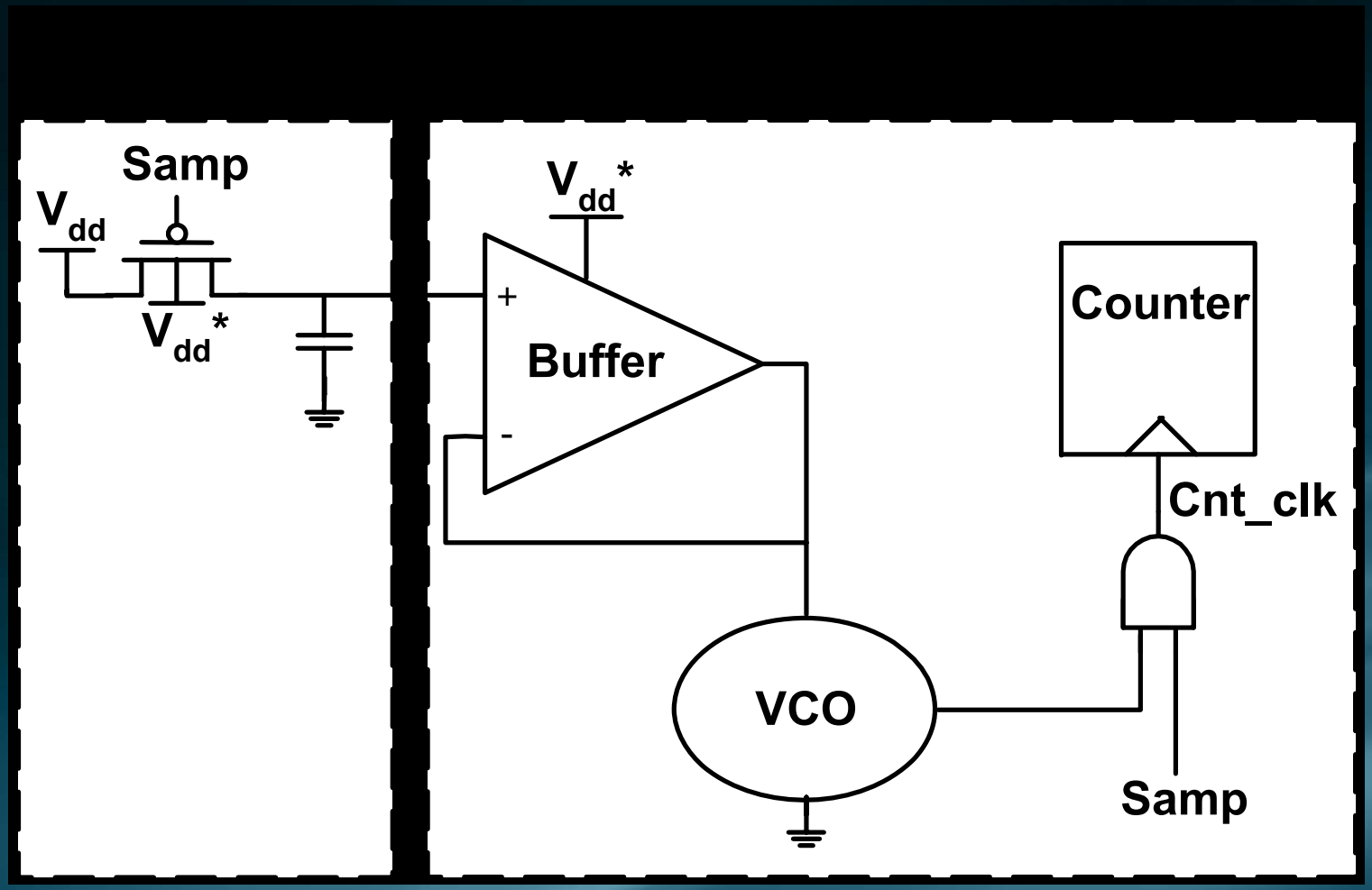
- Don't need V for all t – just need sample pairs
- Autocorrelation is an average property
  - Nyquist frequency set by minimum τ
  - Not by sampling rate
- Supply noise is cyclostationary
  - With extra processing, easy to extend measurement technique to this too

Measurement System Block Diagram

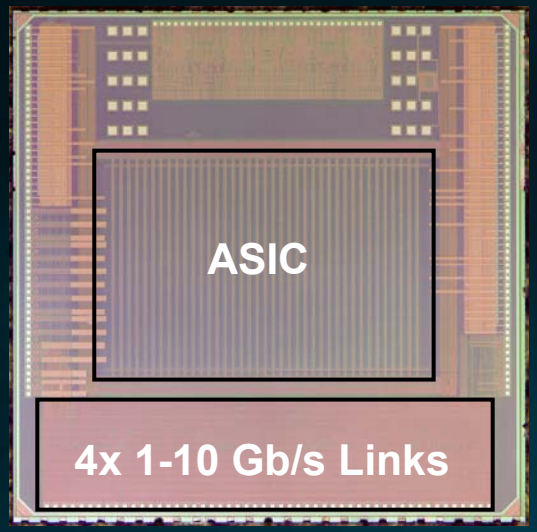


E. Alon, V. Stojanović, and M. Horowitz, "Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise," *Journal of Solid-State Circuits*, April 2005.

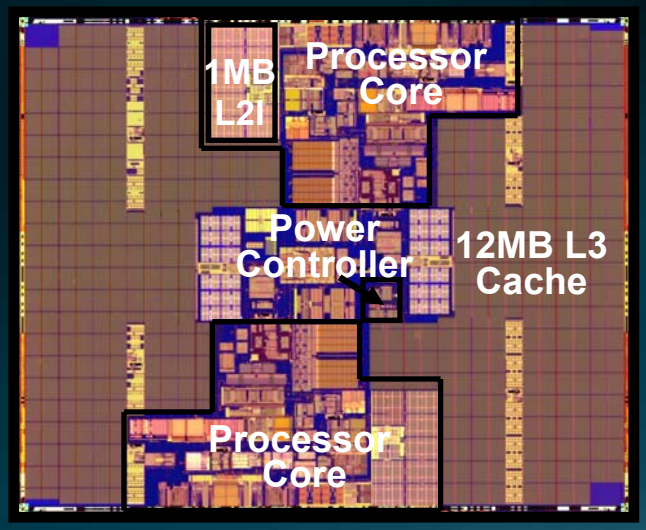
“ADC” Implementation



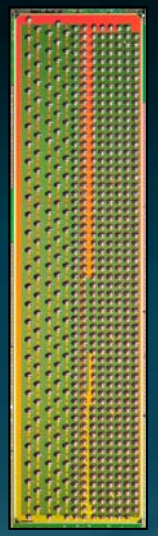
Chip Designers Like Measurements…



0.13 µm Link,



90nm Itanium,



90nm SOI I/O, …

- Measurement circuits included in several chips:
  - Rambus (0.13 µm, 90 nm SOI),
  - Intel/HP (90 nm, 45 nm),
  - AMD (65 nm SOI),
  - TI (90 nm),
  - NEC (90 nm)

Great! Are We Done?

- Is system optimized analog it?
  - Depends on how hard it is to design.
  - System optimized analog will still have some analog

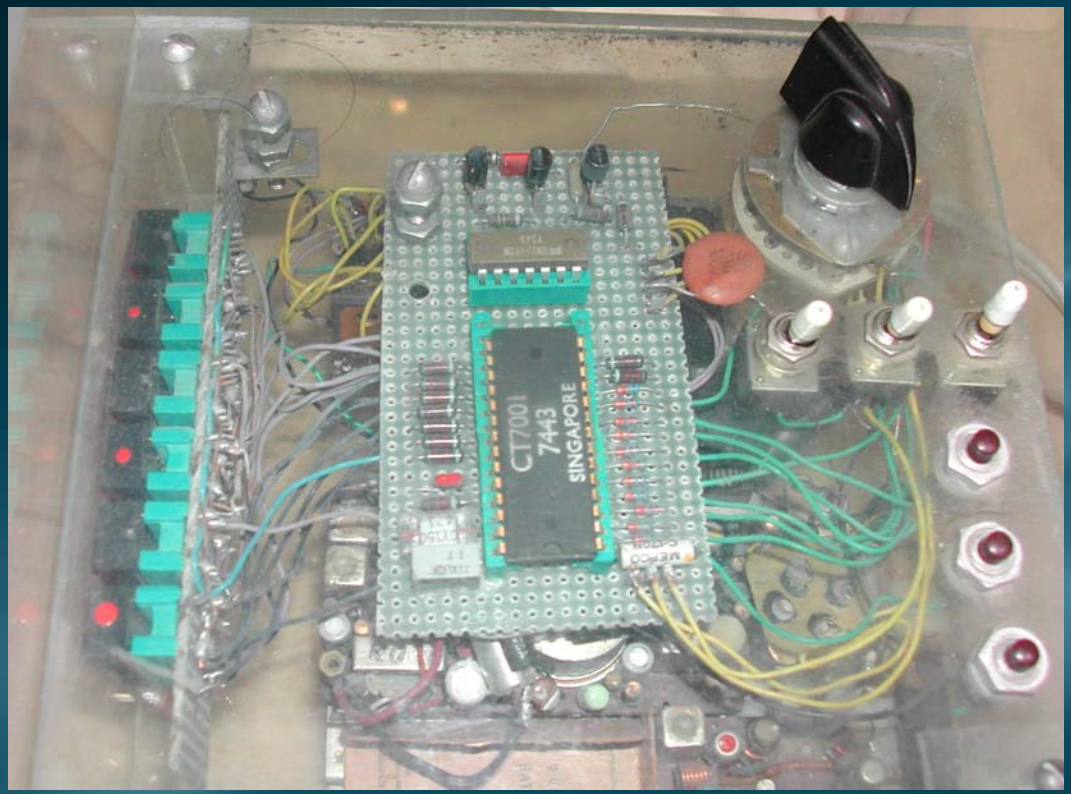
- Let’s do a brief trip through memory lane …

My Misspent Early Teens 70-74

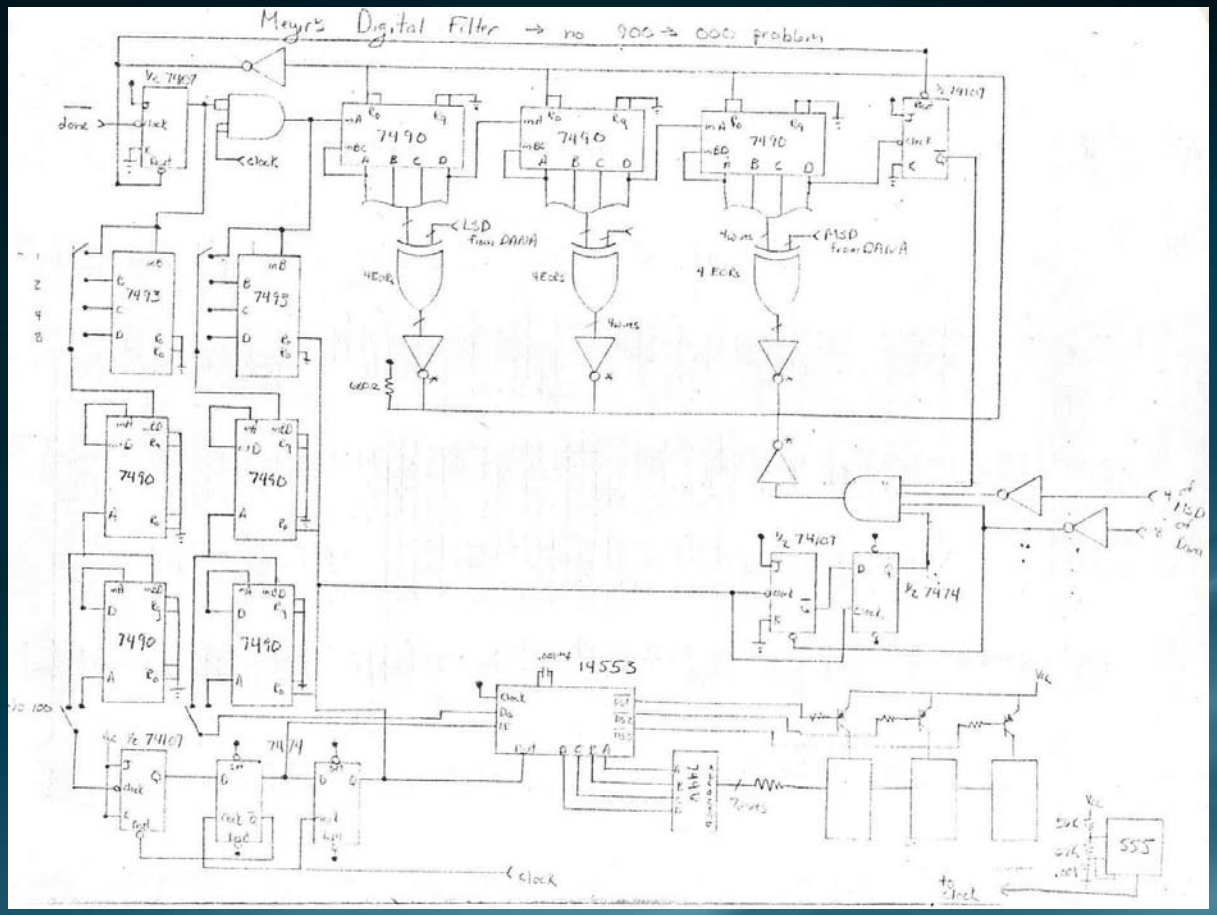
- Got my first IC around 71
  - Uncle was an EE
  - Signetics 8T80? (pre 7400)
  - Thought it was very cool, but never used it

The MIT Years 74-78

- Built lots of stuff at home
  - Calculator - 3 pMOS chips, incandescent 7-seg
  - Digital clock – 1 pMOS chip, LED 7-seg



Design Tools



- Chips: 7400 TTL, and pMOS LSI

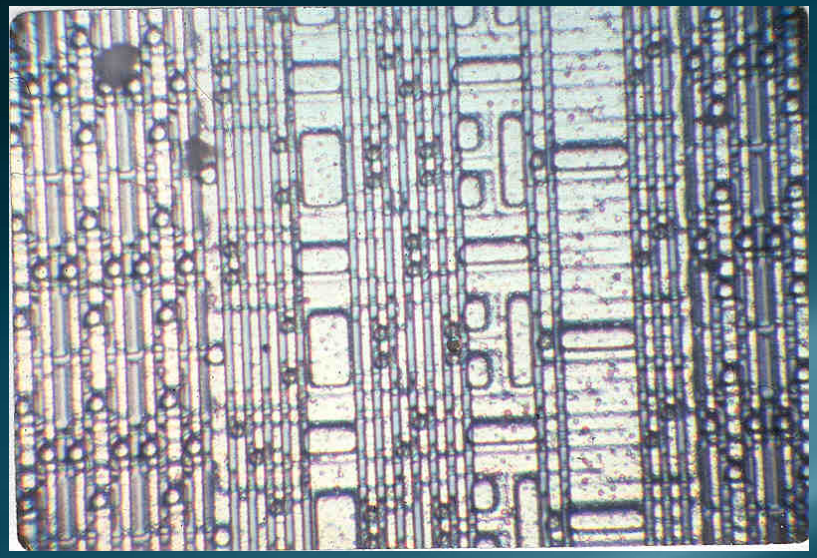
Fabrication Tools

1978 – Hello Silicon Valley

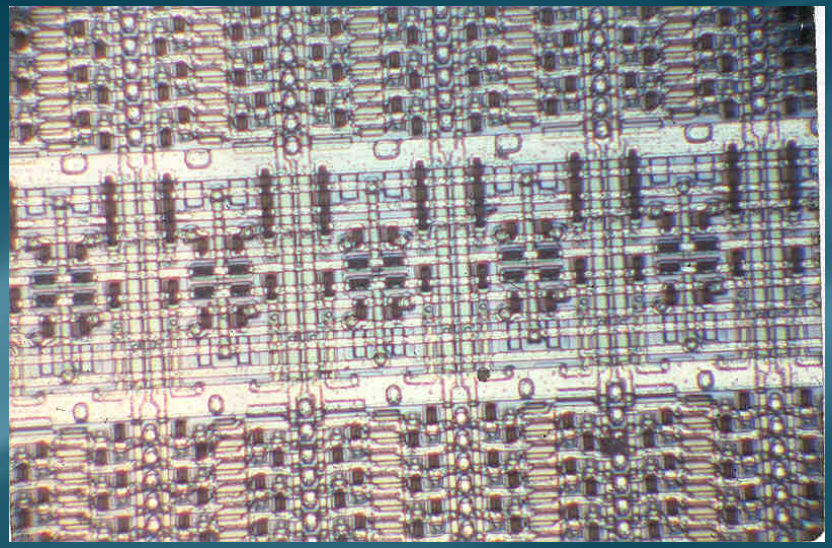
Hot new technologies

- 3µ nMOS
- Depletion loads and 5V operation, TTL I/O

HMOS –2147 at Intel

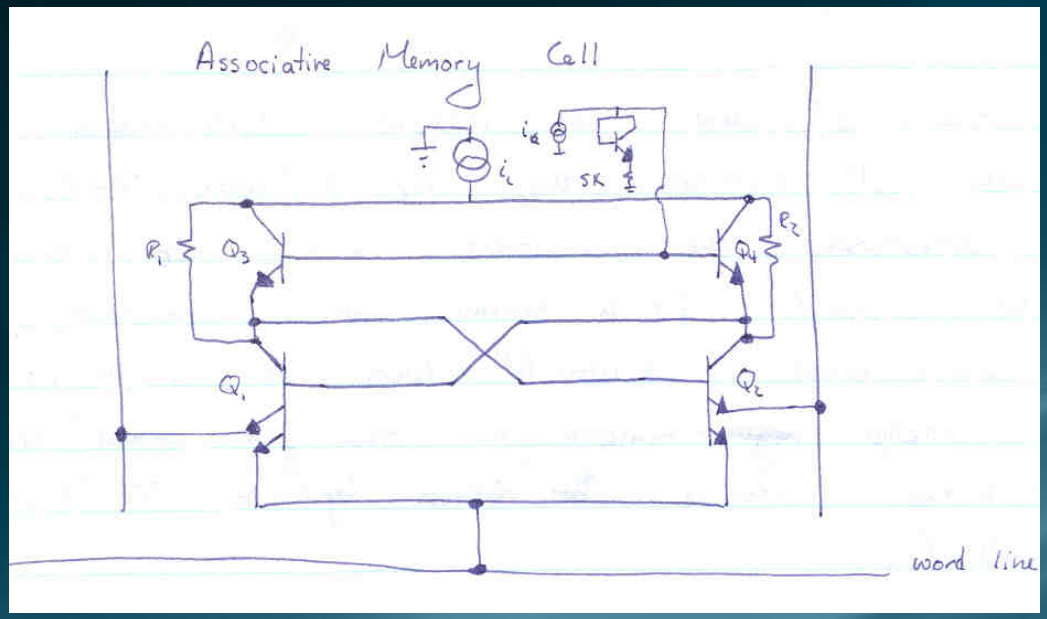


VMOS at AMI



Worked at Signetics

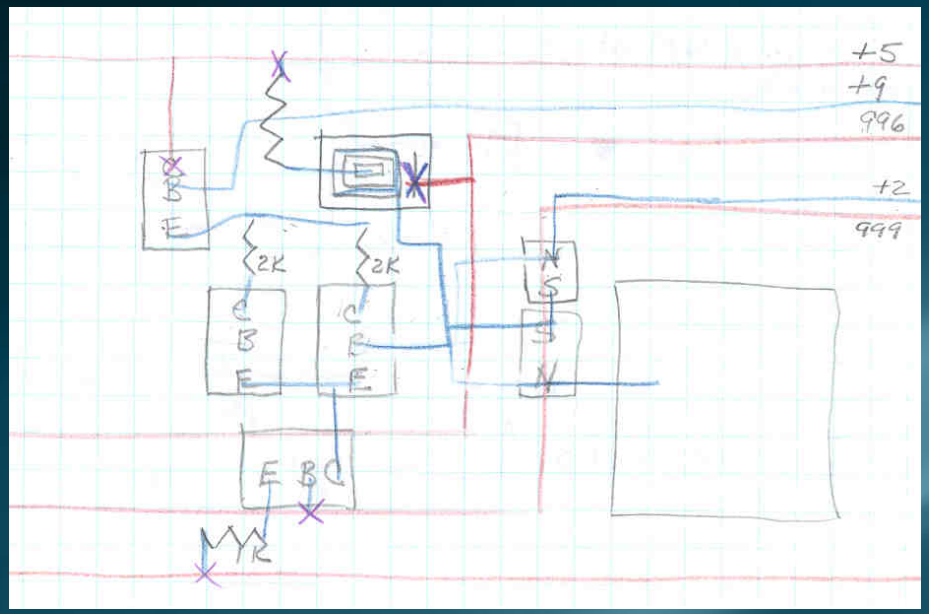
- Worked on bipolar designs
  - 1 kbit ECL CAM, ISL gate array

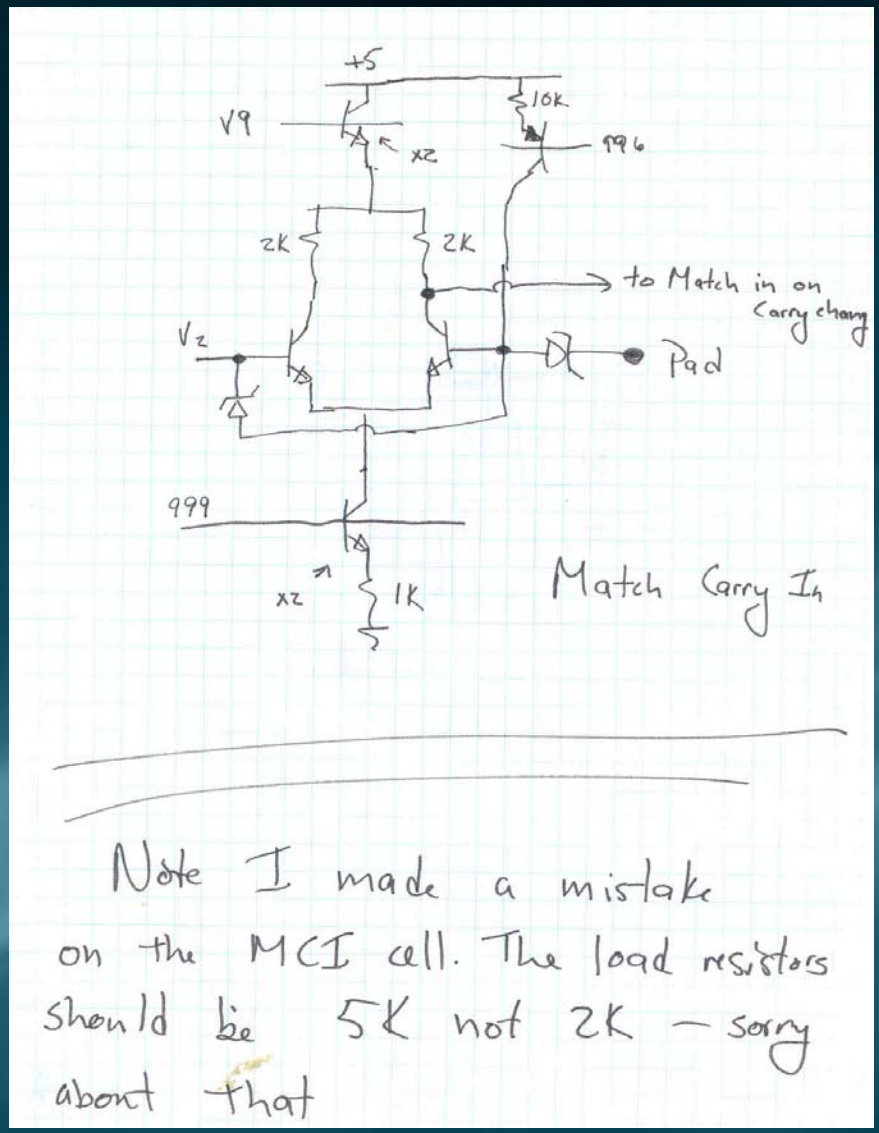


- Design Flow
  - We did have circuit simulation

Backend (Layout) Flow

- Handed schematic to layout designer
  - She produced stick diagrams to check





Layout Flow Cont'd

- She drew it with color pencils on mylar
  - A central group digitized it,
  - Plotted results on large flatbed pen plotters
- Manually checked DRC and ERC
- Computer DRC only before tape-out

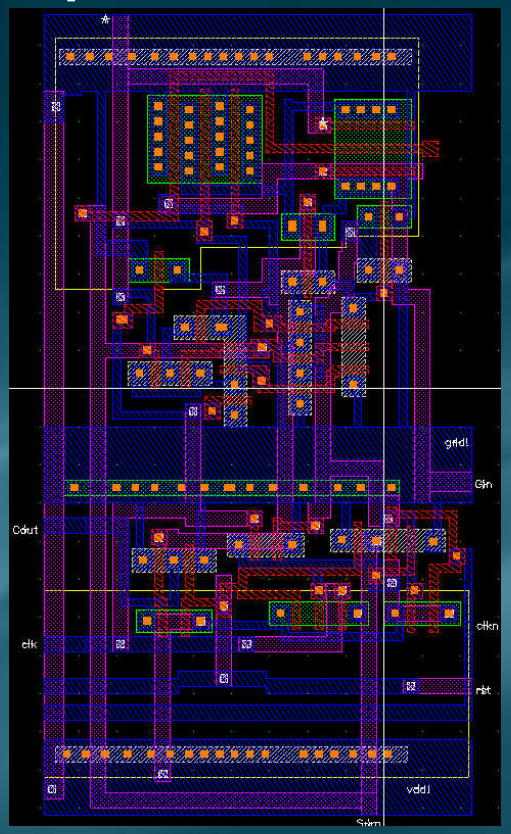
We Have Come A Long Way,

- Digital chip design today is very different
  - Verilog input, with some external IP
  - Floorplan information
  - Tools generate the chip
    - But you need to be expert in using the tools
- Design moved through many phases
  - Spice, custom layout
  - Logic, Std cells manual placement/routing
  - Synthesis, automatic placement/routing
  - SOC design – macro block reuse

Well, Maybe Not (for Analog)

- Now draw schematics on a computer
- And layout is done directly on computer too
- But the process is still manual

John - Layout designer at Micron



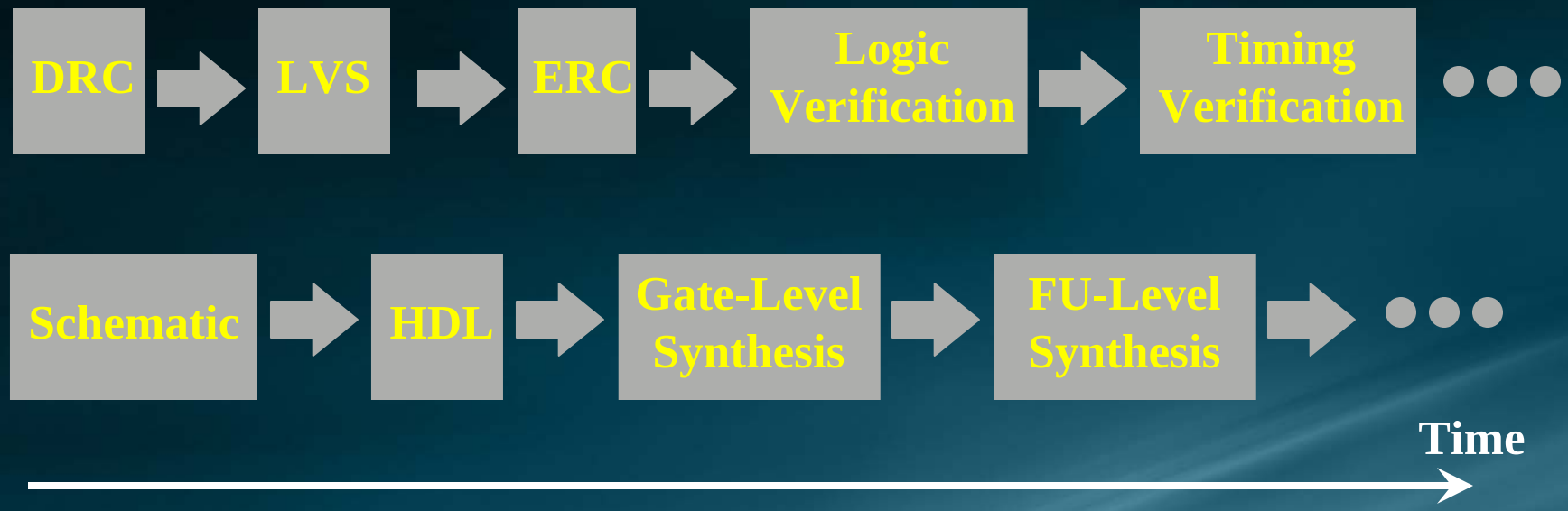
Analog Design Tools Still Primitive

- Basically a custom flow
  - With no ERC, SI checks
- Problem likely to get worse not better
  - As scaling slows, more technology options
    - Many transistor types, capacitors, resistors, etc.
  - Using these features ties design to fab
  - RET techniques make layout “interesting”

Digital Analog Design

- Don’t just use more digital gates
- Make analog design more like digital
  - Better encapsulation of function
  - Methods for system validation
  - Automatic electrical rules checking
  - Better reuse of components
- Reduce time to port design

Digital CAD Tools



- Digital design leverages automation
  - Binary logic abstraction
  - Similar constraints and goals for each circuit

Analog CAD Tools

- Analog circuits are custom designed
  - Wide range of functionalities
  - Implicit goals and constraints
  - Different checks/objectives for each circuit

Analog Design

- Analog design tool scaling
  - SPICE and custom layout
  - Better SPICE and custom layout
  - Matlab, SPICE, and custom layout
  - Not much change
- Basic Problem
  - Little/no encapsulation of functional blocks
    - No abstraction / ERC pairs
  - Leads to large amount of analog redesign

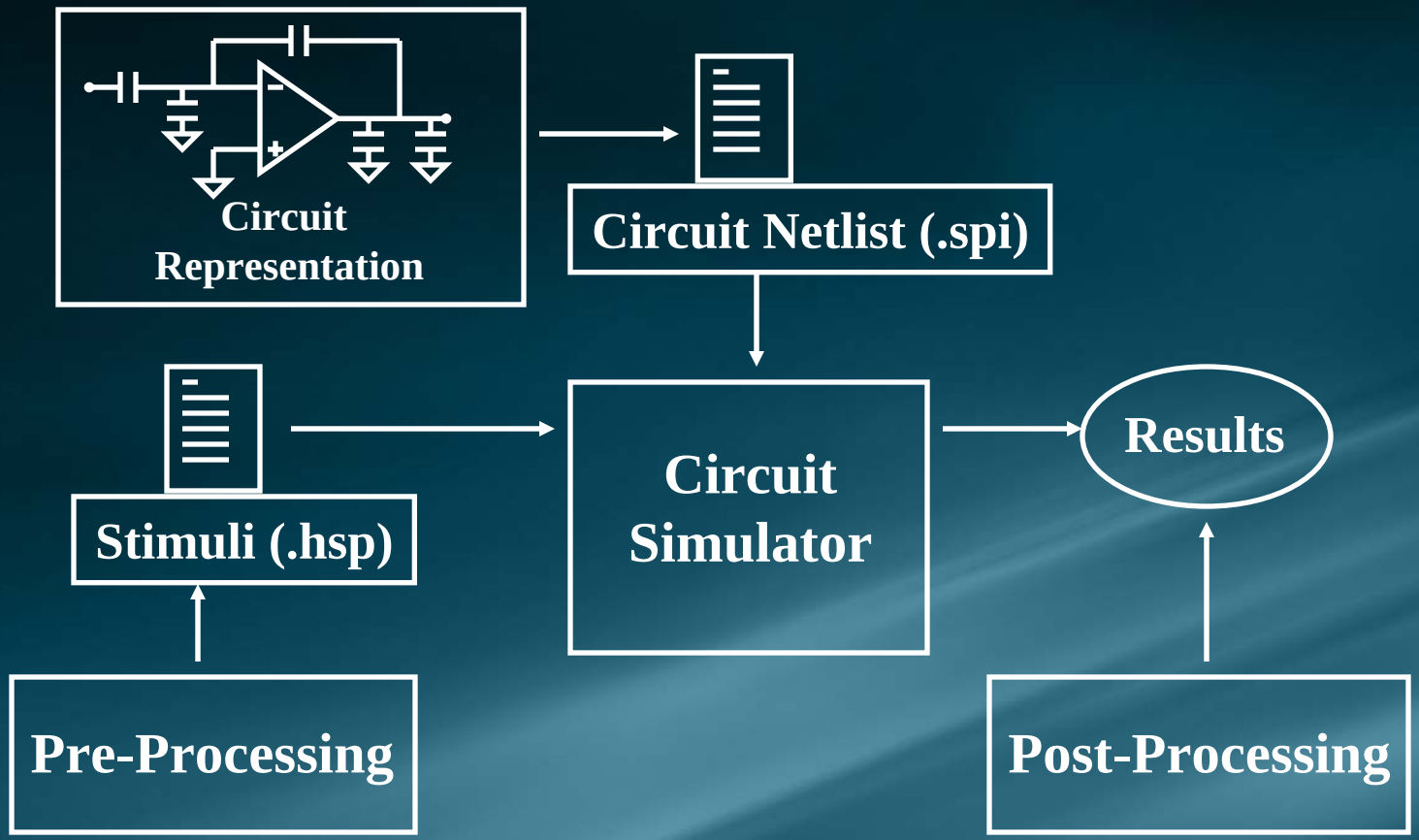
Management Problem

- Must port a mixed signal block to new fab
  - Old design is great
  - But former design is not working on the port
- New designer looks at block
  - And doesn't like the way it was designed
    - It is not the way that she would do it
- There is little validation documentation around
  - So you trust the new designer
  - You need to redesign the block

Need to Capture Goals/Constraints For Each Analog Circuit

- Need to record designer's intention
  - Circuit topology and sizes records answers
  - Need to know what questions were asked
    - What problems were tested
- Only (good) designers know this
  - Needs to be captured as part of the design
- Offer incentives to encourage capture
  - Make the documentation benefit the current designer

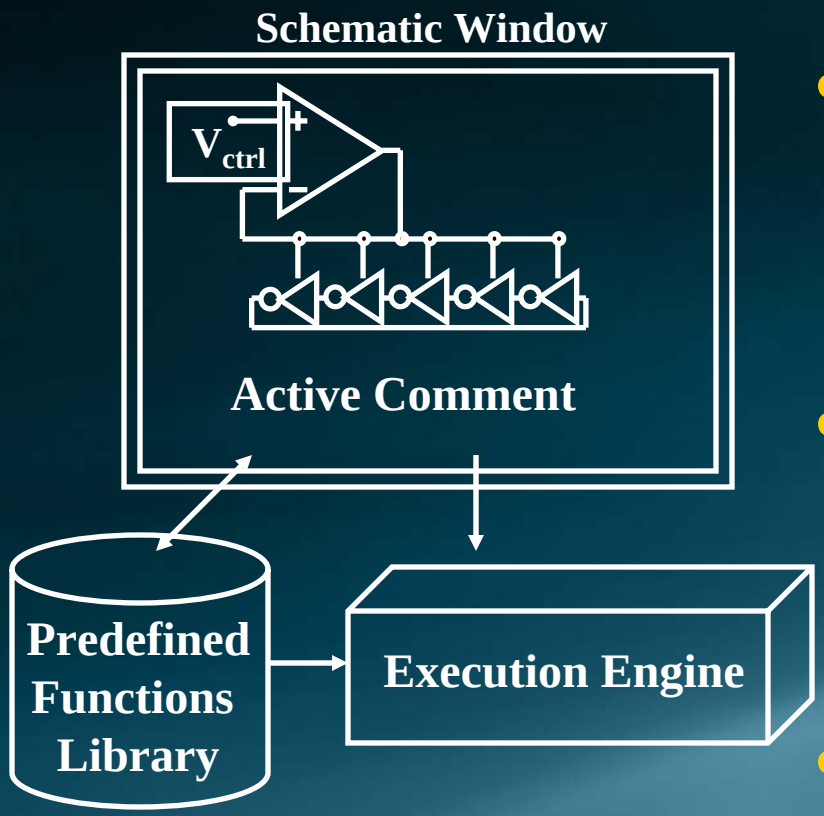
Design: Circuit Simulation



Annotated Schematics

- Annotate specifications and goals
  - For each circuit on the schematic
- Annotate constraints on schematic
  - Requirements for correct operation
- Annotations create simulation files
  - And data collection routines

Active Comment Operation



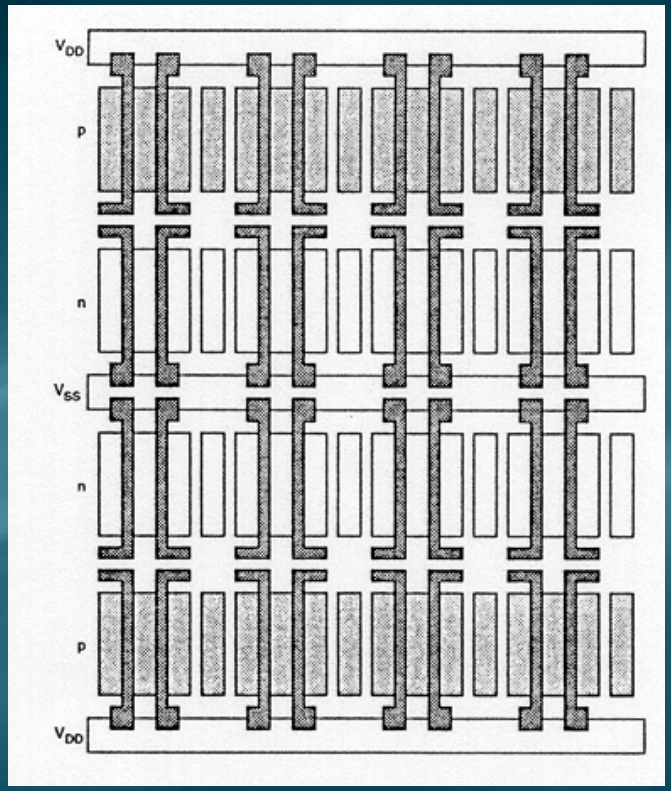
- Written on circuit's schematic
- Composed of predefined functions
- Executed by a prototype engine

Next Link To Functional Simulation

- In mostly digital systems
  - Need to simulate many cycles to validate system
  - This is usually to slow to run in SPICE
    - To slow even in fast SPICE engines
  - Write functional model for analog block
    - How to validate this model?
    - How to make the system simulation worst-case?
- Once you have intent, and tests
  - Need to link these to functional models

Layout: The Final Frontier

- Layout rules are getting ridiculous
  - RET creates many issues
  - DRC decks are not complete
- Proximity effects:
  - Feature dimensions
  - Strain variations
- Regularity is key
  - Move to gate matrix designs?



Conclusions

- The nature of design is changing
  - Basic CMOS circuit forms are maturing
  - Scaling has changed cost ratio of analog/digital
- Creates an opportunity to rethink analog design
  - Stanford RAD Project
- Two main research directions:
  - Leveraging system constraints and digital gates
  - Making analog design more like digital design