Fundamentals of Time-Based Circuits

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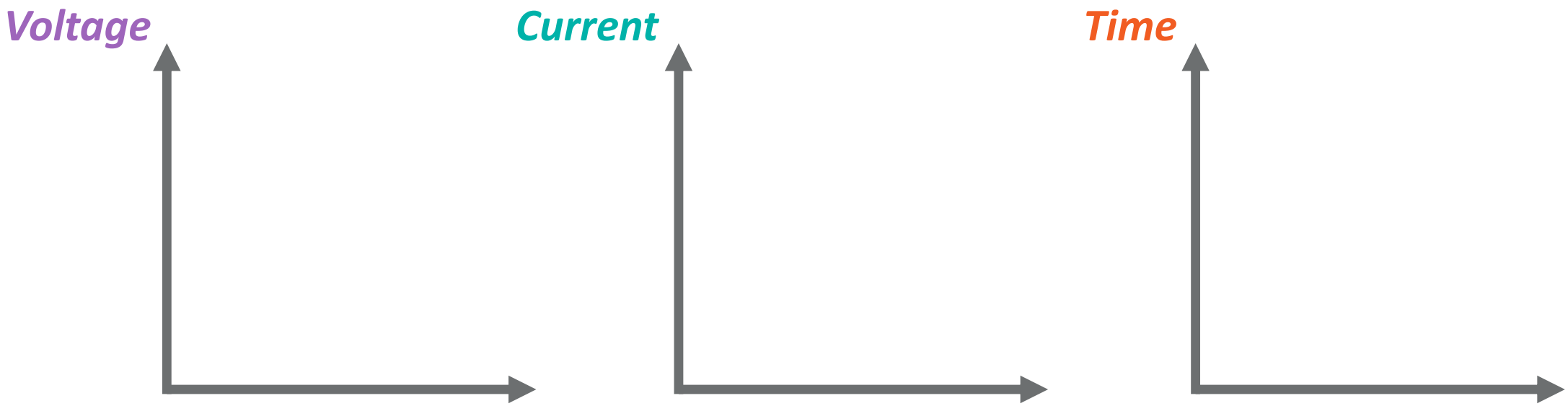
Maxim Integrated Products

Acknowledgements to Mike Perrott and Pavan Hanumolu
for assistance with presentation content.

What are Time-Based Circuits?



Time-based circuits use ***time*** as the primary signal domain

Why Time-Based Circuits?

- Time-based signals translate to binary levels, and process technology benefits binary signal processing
  - > Small area
  - > Low power
  - > High speed

- Potential benefits for many applications
  - > Frequency generation
  - > Analog-to-digital conversion
  - > Switched-mode power using PWM

Why Time-Based Circuits?

- Time-based signals translate to binary levels, and process technology benefits binary signal processing
  - > Small area
  - > Low power
  - > High speed

First, we will look at basic time-based circuits and how they work

- Potential benefits for many applications
  - > Frequency generation
  - > Analog-to-digital conversion
  - > Switched-mode power using PWM

Second, we will look at application examples that leverage time-based circuits

Outline

- *Introduction to Time-Based Circuits*
- *Basic Signal Conversion to Time-Domain*
- *Time-to-Digital Converters*
- *Applications of Time-Based Circuits*
- *Summary and Conclusions*

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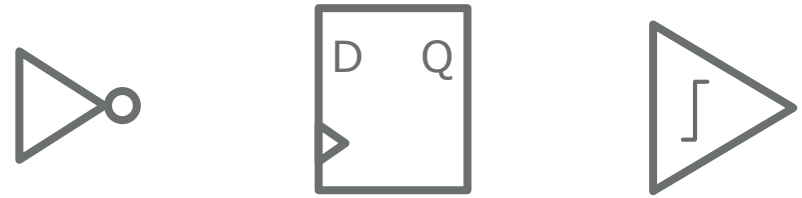
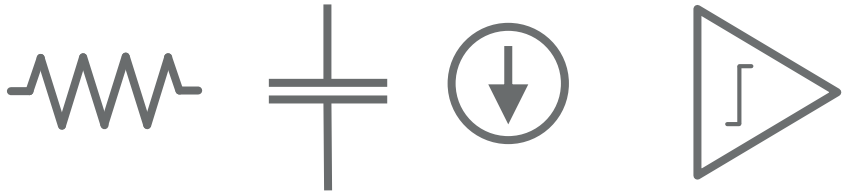
Kinds of Time-Based Circuits

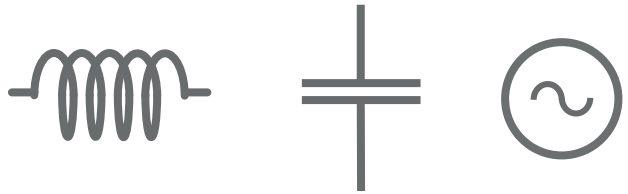
- Classical digital (0th order)



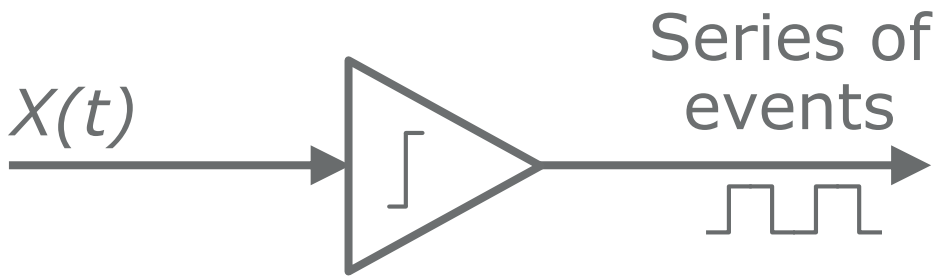
- RC-based or I/C-based (1st order)



- LC-based (2nd order)



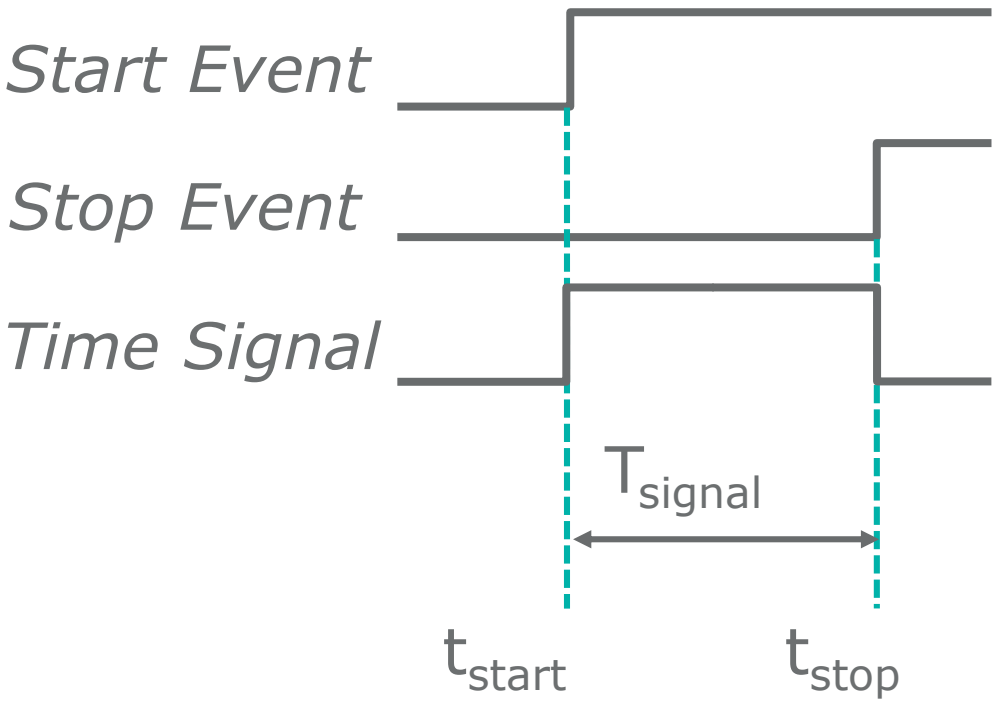
Voltage or Current (V&I) Time Events



- *X* is input to a comparator that outputs time-based events
  - > Comparison is typically single threshold, can be more complex
  - > Can be discrete-time or continuous-time comparator
- *X(t)* can be any kind of voltage or current function:
  - > Random process, e.g. photon counter
  - > Periodic function, e.g. sin wave
  - > Low-frequency signal, e.g. thermal shutdown

Sampling implicitly happens at event detection

Time Events and Signals



$$T_{signal} = t_{stop} - t_{start}$$

Events:

- Are points in time
- Map to binary transitions
- Noted here in lower case ‘t’

Signals:

- Difference between 2 events
- Map to binary levels
- Always sampled in time
  (i.e. discrete-time)
- Noted here in upper case ‘T’

Time vs. Voltage/Current

	V&I signals	Time signals
Dynamic Range	Limited by supply	Limited by patience
Noise	Function of power, BW	Function of power, BW
Domain	Continuous time or discrete time	Discrete time only
Amplification	BW is function of gain	Latency is function of gain
Polarity	Bipolar	Unipolar → binary Bipolar → ternary
Simple operations	1. Amplification 2. Addition 3. Subtraction	1. Integration 2. Quantization 3. Switch

Time-Based Signal Challenges

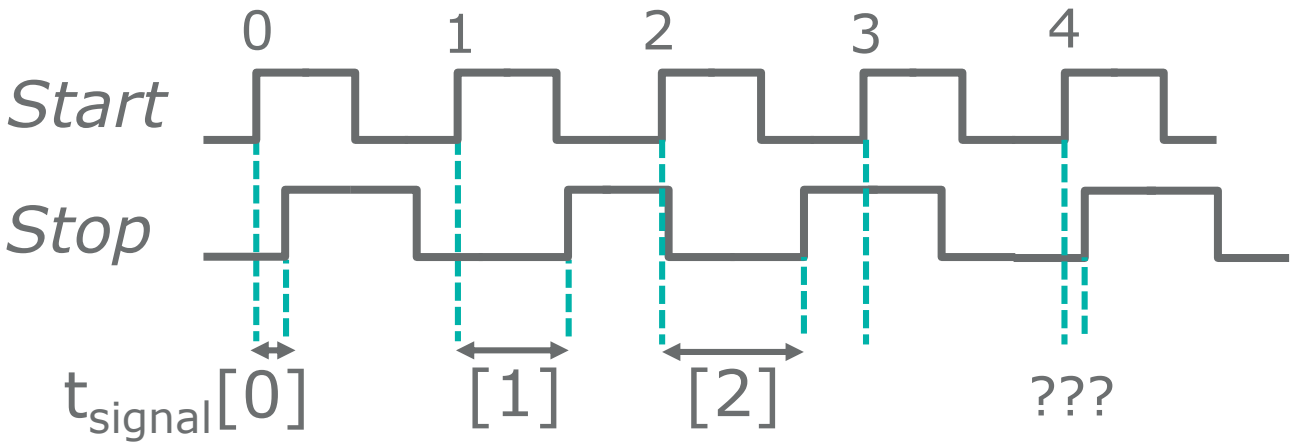
Traditional Challenges:

- Input-referred voltage noise
  - > Low power and noise especially challenging at high-speed
- Linearity
  - > Conversion process is generally non-linear
- Power supply rejection
  - > Lack of truly differential operation impacts PSRR, CMRR

Special Challenges:

- Signal wrapping and clock domain crossing

Synchronous Time-Based Systems



$$T_{signal}[k] = t_{stop}[k] - t_{start}[k]$$

- Assume that *Start* is a synchronous reference clock
- *Stop* is then a series of events that defines the signal of interest,
  - > But not always a 1:1 mapping between *Start* and *Stop* events
  - > For a missing or extra *Stop* event, typically can use *Start* indices and assign $T_{signal}[k]$ an appropriate value
  - > Cross domain signals require attention!

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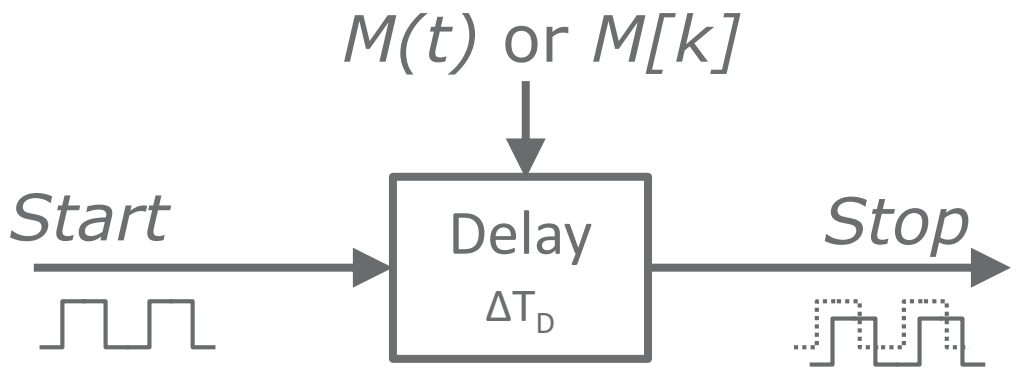
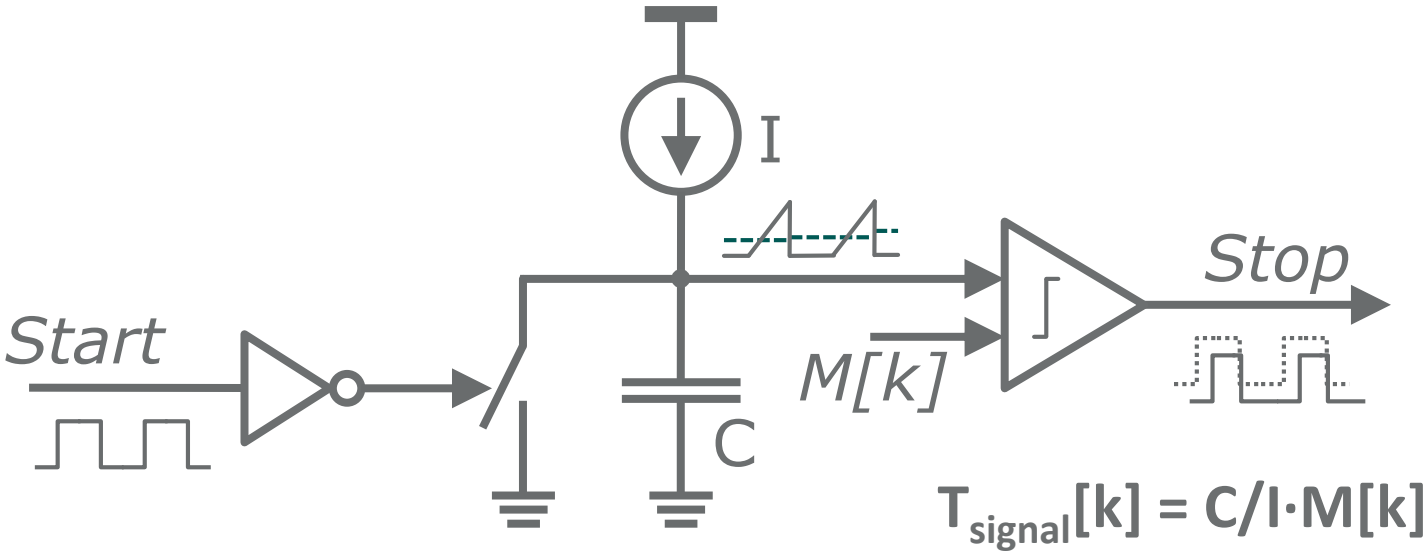
V&I to Time Signals



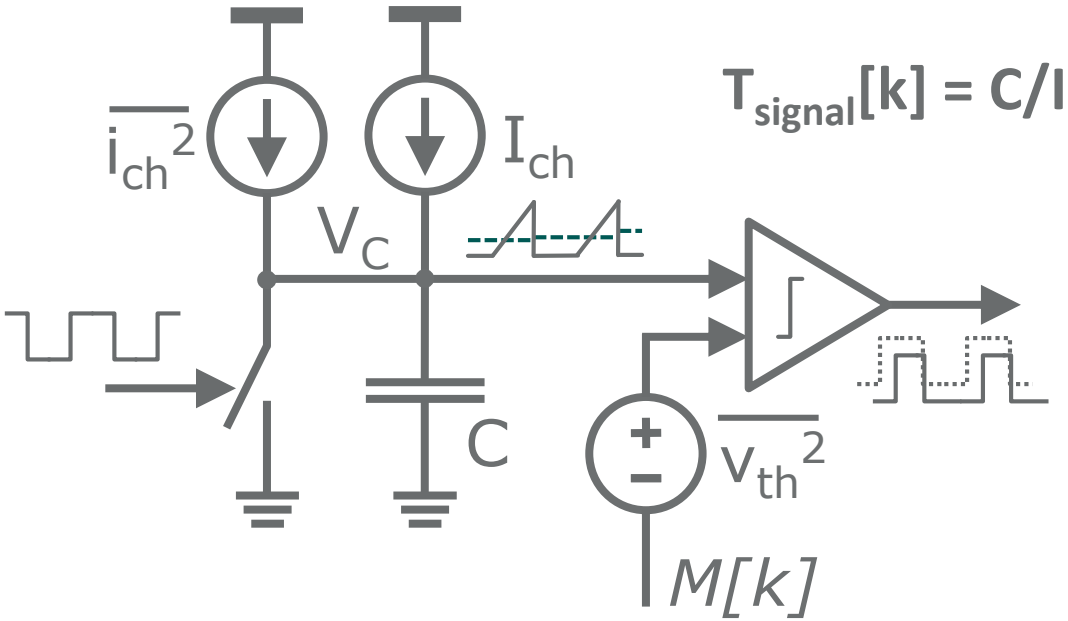
- *Start* is input to a delay function that outputs *Stop*
  - > 1:1 mapping between *Start* events and *Stop* events
- Delay is a function of *M*
  - > *C*an vary continuously or in discrete time
- Delay function translates signal from *M* to T_{signal}
  - > M[k] → T_{signal}[k] is a traditional discrete-time operation
  - > M(t) → T_{signal}[k] is a sampling operation, windowed with ΔT_D

Example: Voltage to Time



- When switch closes (Start = 0), capacitor is reset
  - *Stop* output is low
- When switch is open (*Start* = 1), capacitor charge *integrates* to *M[k]*
  - *Stop* output transitions high after comparator trips
- Rising delay $\Delta T_{D\text{-}rise} = T_{signal}$, simply a linear function of I, C, M[k]
  - Note: Requires large enough ramp rate for given *Start* waveform

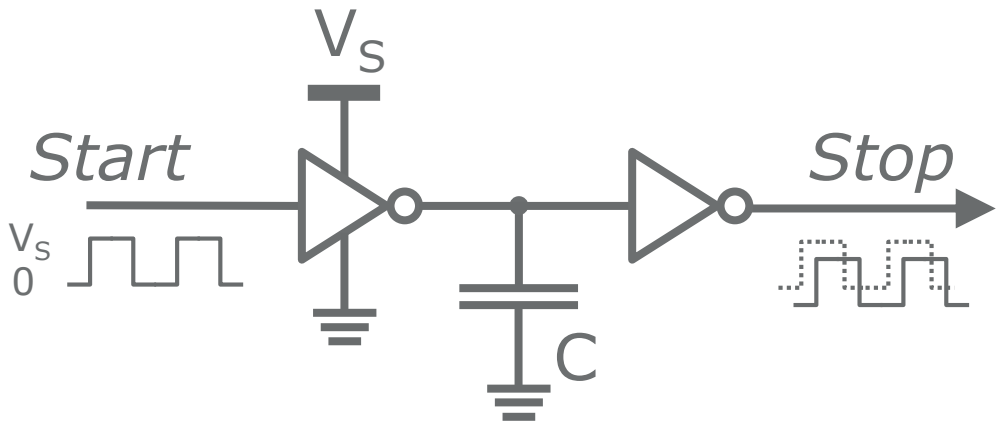
Example: Time-Based Circuit Noise



$T_{signal}[k] = C/I \cdot M[k]$

- $\overline{i_{ch}^2}$ white noise integrates onto V_C as a Wiener process, W_i
  - > Brownian noise
  - > Expected value $E[W_i] = 0$
  - > Variance $Var[W_i] \alpha T_{signal}$; **$std[W_i] \alpha sqrt(T_{signal})$**
- $\overline{v_{th}^2}$ noise, independent of T_{signal}, adds to W_i

‘Digital’ Used to Create Time Signals



$$\Delta t = \Delta V \cdot C / I$$

- Multiple ways to modulate delay depending on application:
  - > Supply voltage (for good or for bad)
  - > Switching current (e.g. current starved inverter)
  - > Load capacitance (e.g. varactor or switched bank)
  - > Charging resistance (e.g. array of parallel inverters)

Leveraging Integration

1) V&I to time: Integrating charge onto capacitors is a simple way to convert from traditional V&I domain to time-based domain

2) V&I to frequency: Integrating analog signals with oscillators is an inherently simple operation with multiple benefits

3) Time to V&I: Integrating binary time signals is a simple way to move between time-based circuits and traditional analog

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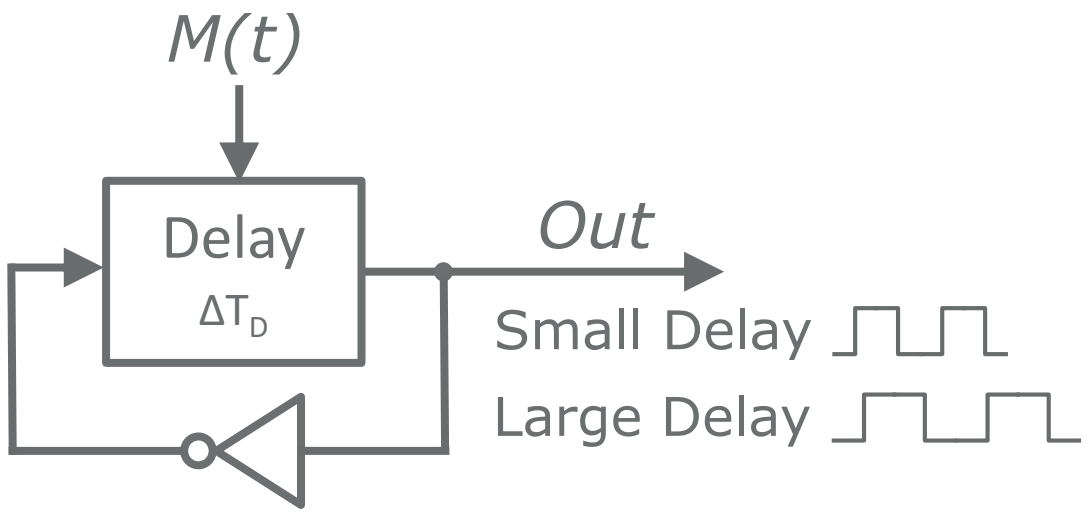
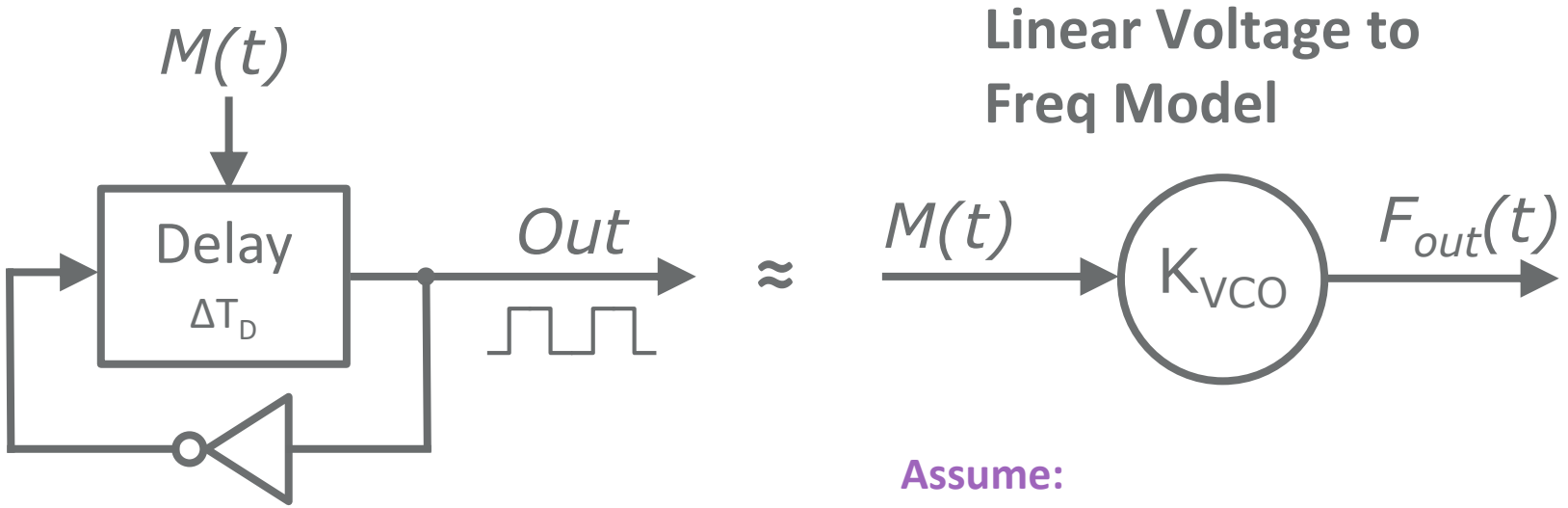
V&I to Time With Feedback



- Voltage *M(t)* modulates *Delay* input to create *Out*
- *Out* is inverted and fedback to input of *Delay*

Simple oscillator integrates analog input in time!

Voltage-Controlled Oscillators (VCO)



Assume:

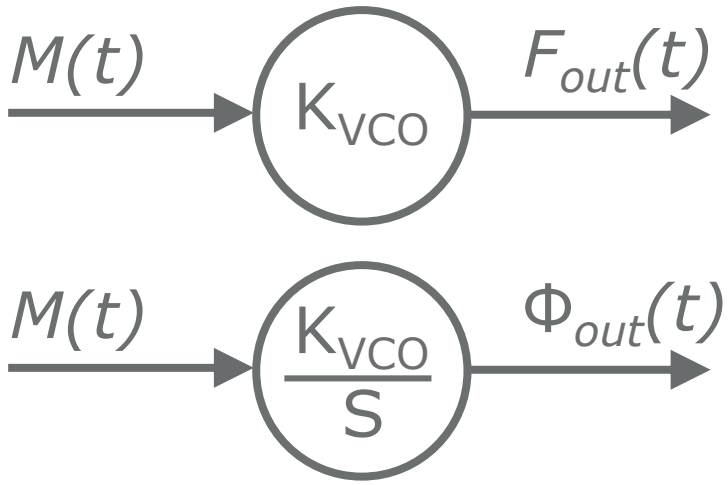
1) M(t)* is bandlimited with *1/BW << ΔT_D

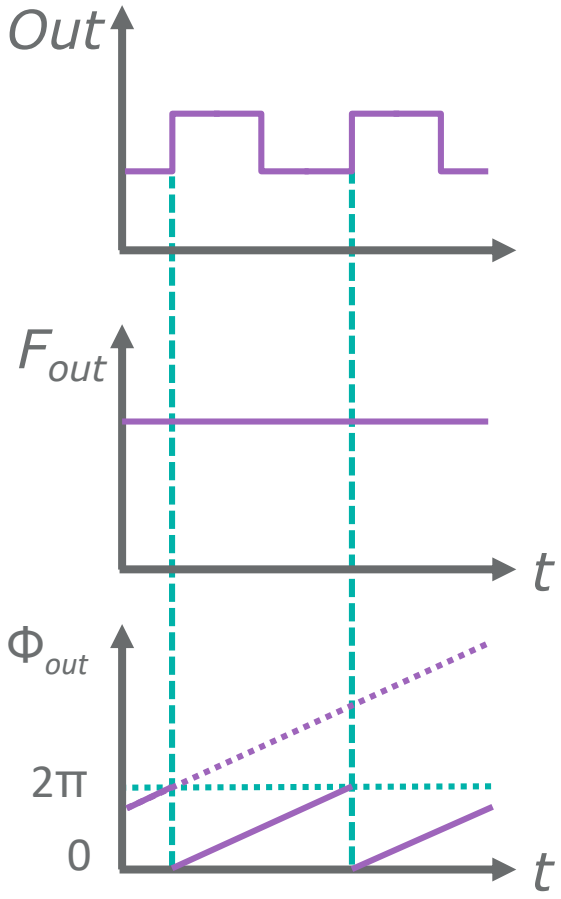
Sampling then looks like impulse trains

2) dF_{out}/dM is approximately linear

$$F_{out}(t) \approx F_O + K_{VCO} \cdot M(t)$$

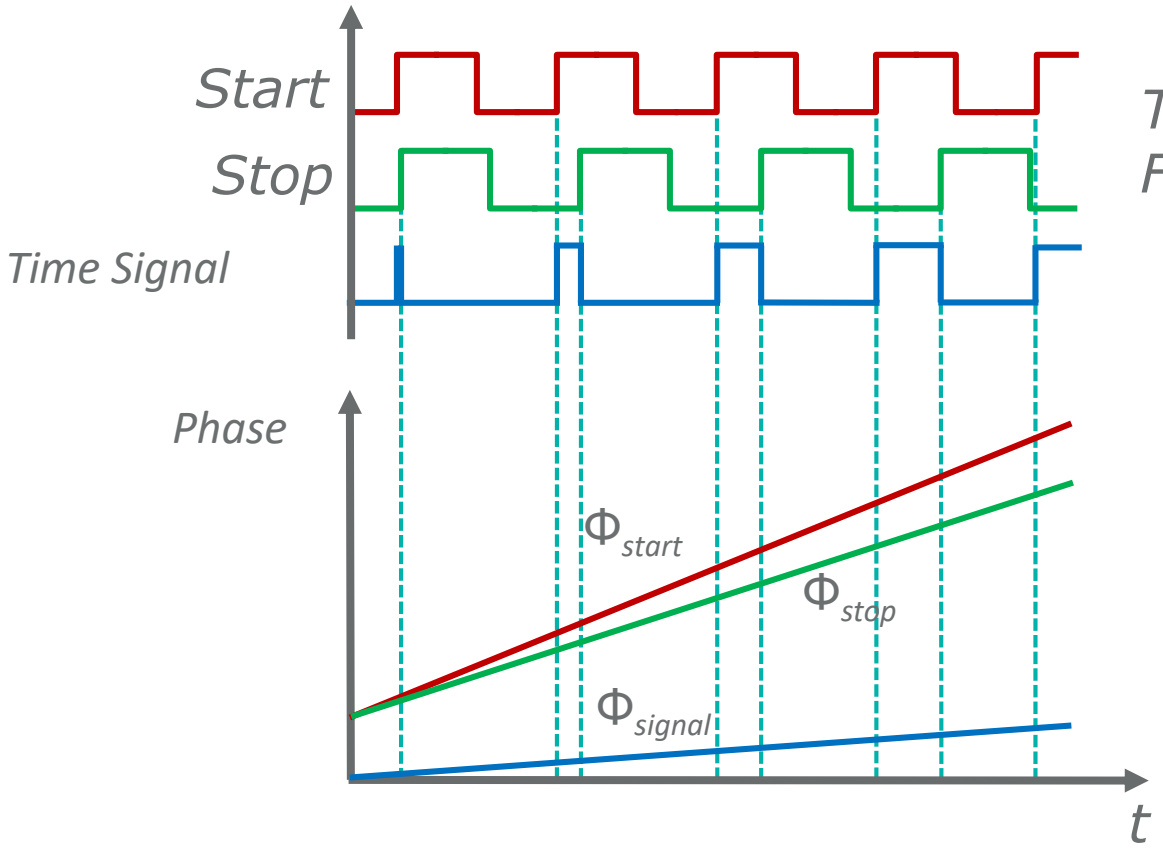
Recall: Phase/Frequency Relationship





- $\Phi_{out}(t) = \int_0^t F_{out}(t) \cdot dt$
- Phase wraps every 2π
  - > Use a linearized continuous-time model of a discrete-time system
  - > Easier to conceptualize linear model without wrapping

Phase and time signal relationship



$T_{start} = 1/F_{start}$

$F_{start} > F_{stop}$

Key points:

1) For linear analysis of time-based systems utilizing oscillators, it is convenient to think in terms of phase rather than time.
2) 2π boundary needs to be treated carefully

$$\Phi_{signal}(t)|_{t=k\cdot Tstart} \approx 2\pi\cdot T_{signal}[k]/T_{start}$$

Ring-oscillator VCO (or CCO)

- Ideal integration function
  - > Infinite DC gain
- Output is already in binary
  - > Easy/fast to sample with digital registers
- Multiple phases can easily be added for improved resolution
  - > Guaranteed monotonicity
- Benefits from scaling
  - > Power
  - > Area
  - > Speed

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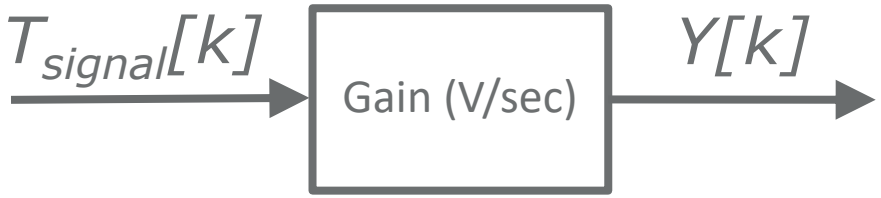
Time to V&I Waveforms

- *Start* and *Stop* define binary *Signal*
- 1-bit asynchronous DAC generates analog output
- But *U(t)* is not the same as $T_{signal}[k]$

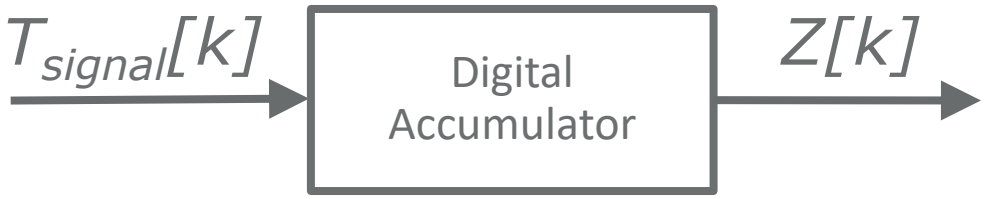
To Be Complete…Time to V&I Signals

Equivalent to

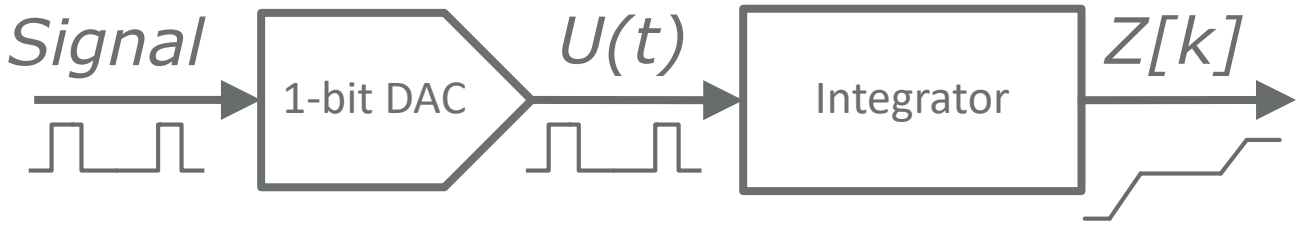


Not very practical…

Time to V&I + Low-Pass Filter



Equivalent to



Much more efficient…

- **PLL charge pumps, where U(t) is a current**
- **Class D amplifiers, where U(t) is a voltage**

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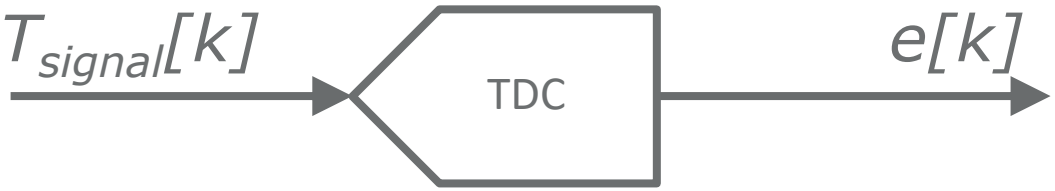
TDC Basics

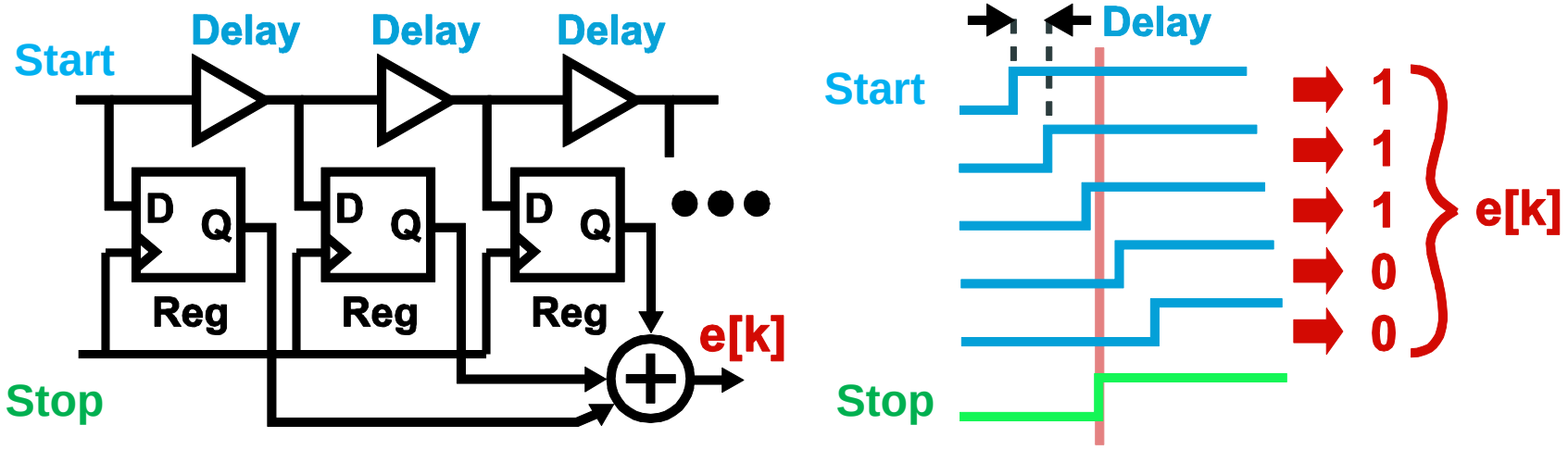
TDC functions to quantize a time-based signal



- e[k] = Quantized TDC output = floor($T_{signal}[k]/\Delta T_{del}$)
- Δt_{del} is equivalent to:
  - > Minimum TDC delay
  - > Raw resolution
  - > Quantization step size

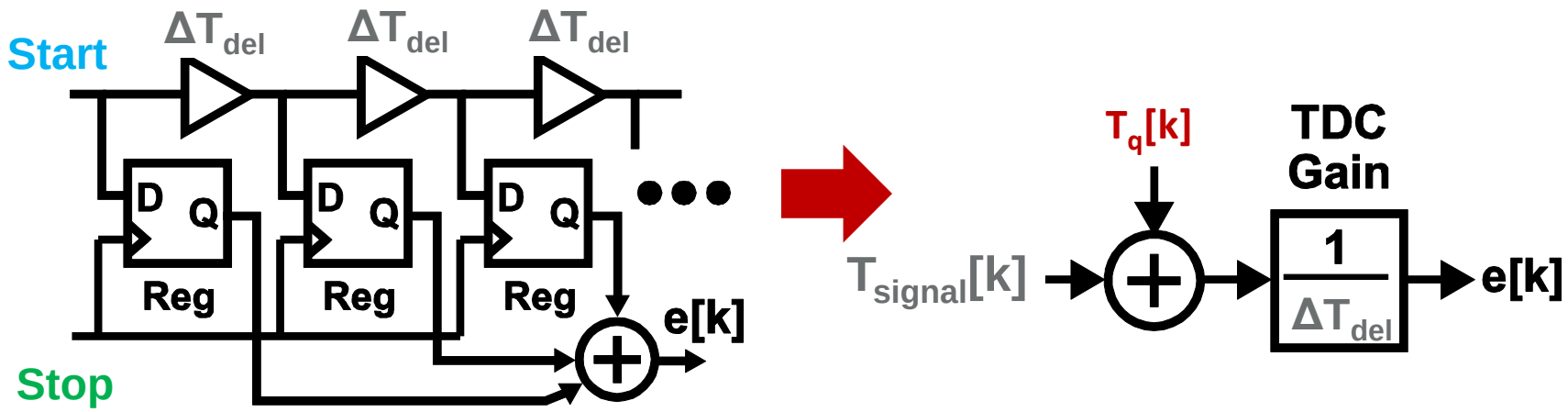
As the reference voltage sets ADC gain, Δt_{del} generally sets the gain for a TDC

Classic Linear TDC



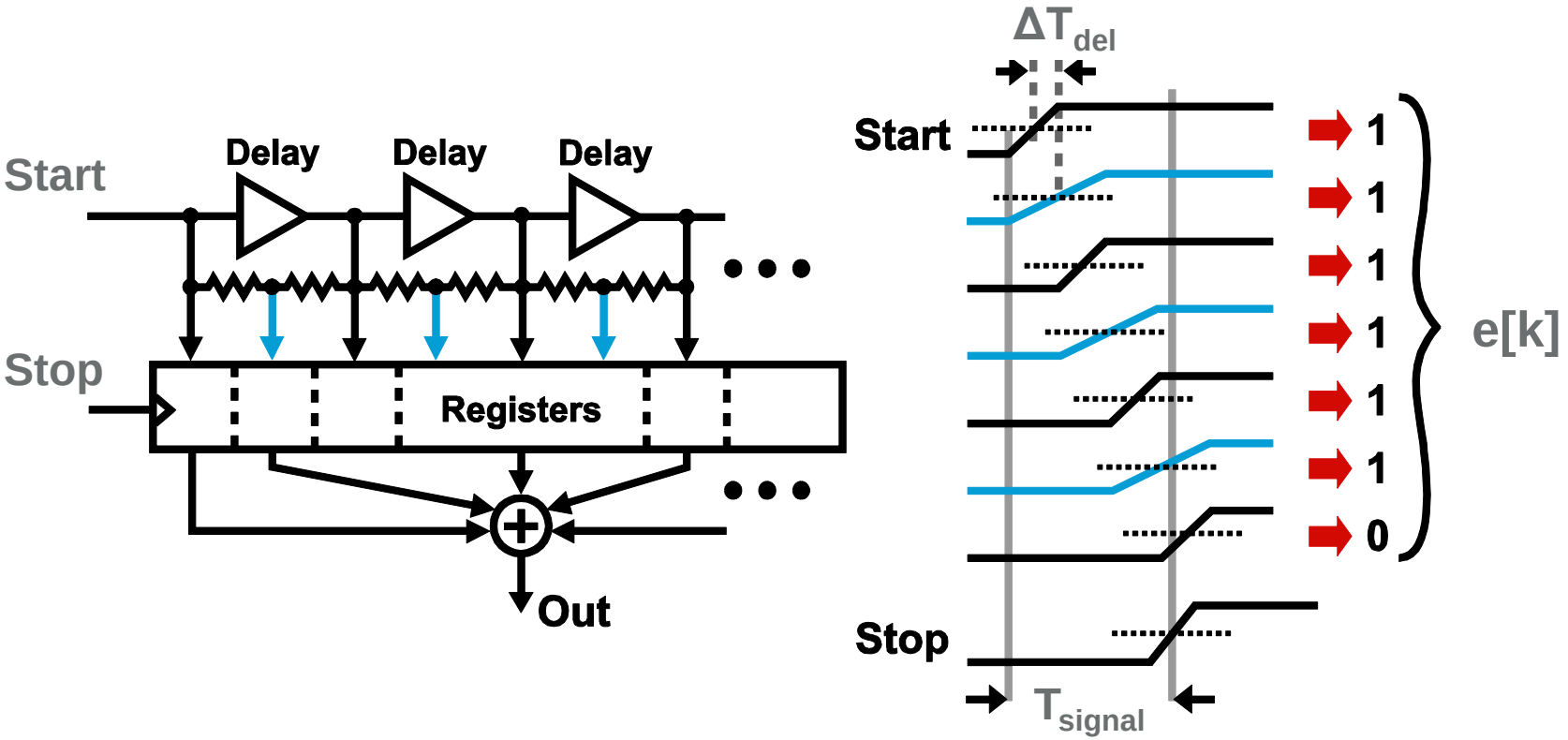
- Number of delay transitions are registered and added
- Resolution is set by a gate delay (multiple picoseconds)
- Maximum range is limited
  - > Number of registers scale with 2^N, where N is number of bits

Linear TDC Model



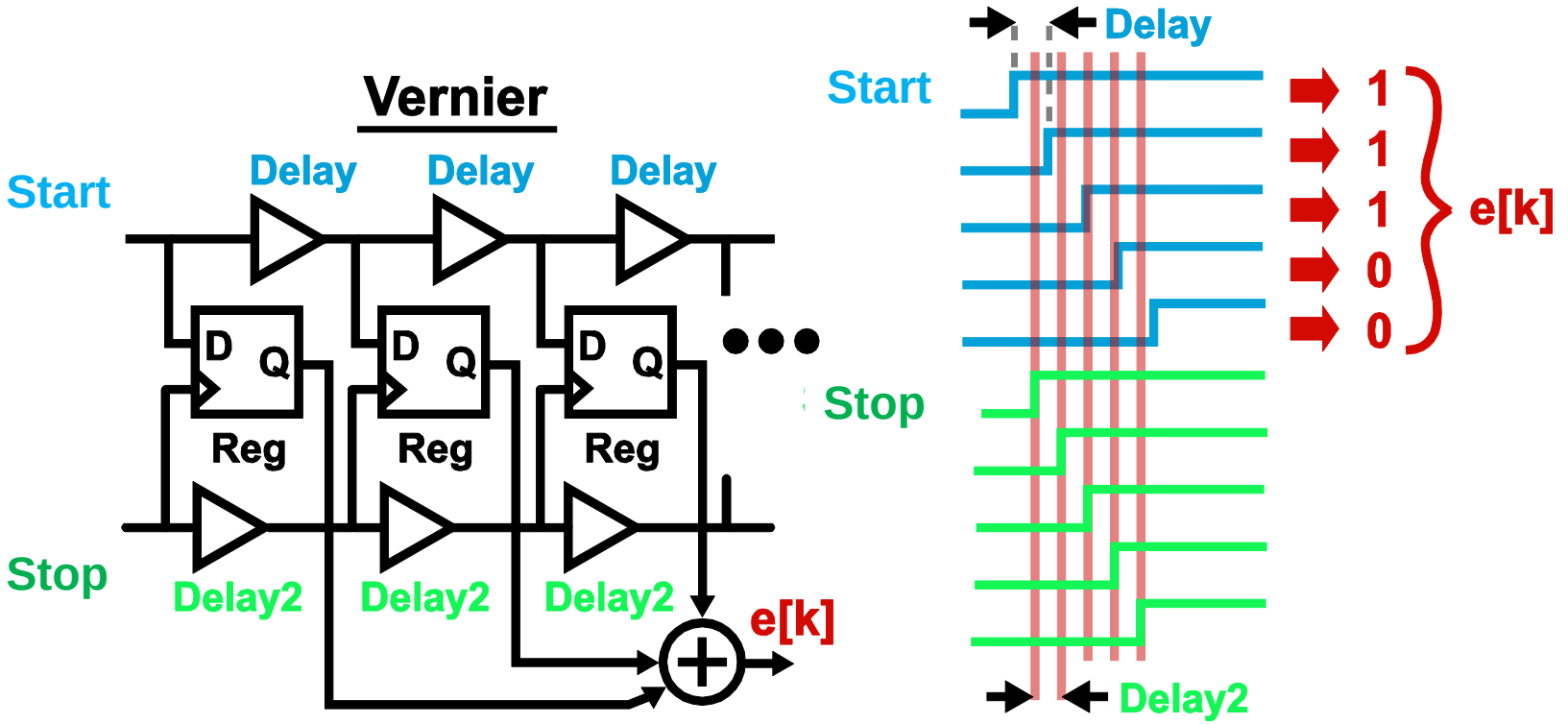
- Discrete-time input ($T_{signal}[k]$) is the difference in time between positive transitions of **Start** and **Stop**
- Quantization noise ($T_q[k]$) is the measurement error
- Quantized integer output (**e[k]**) is the number of transitions

Interpolating Linear TDC



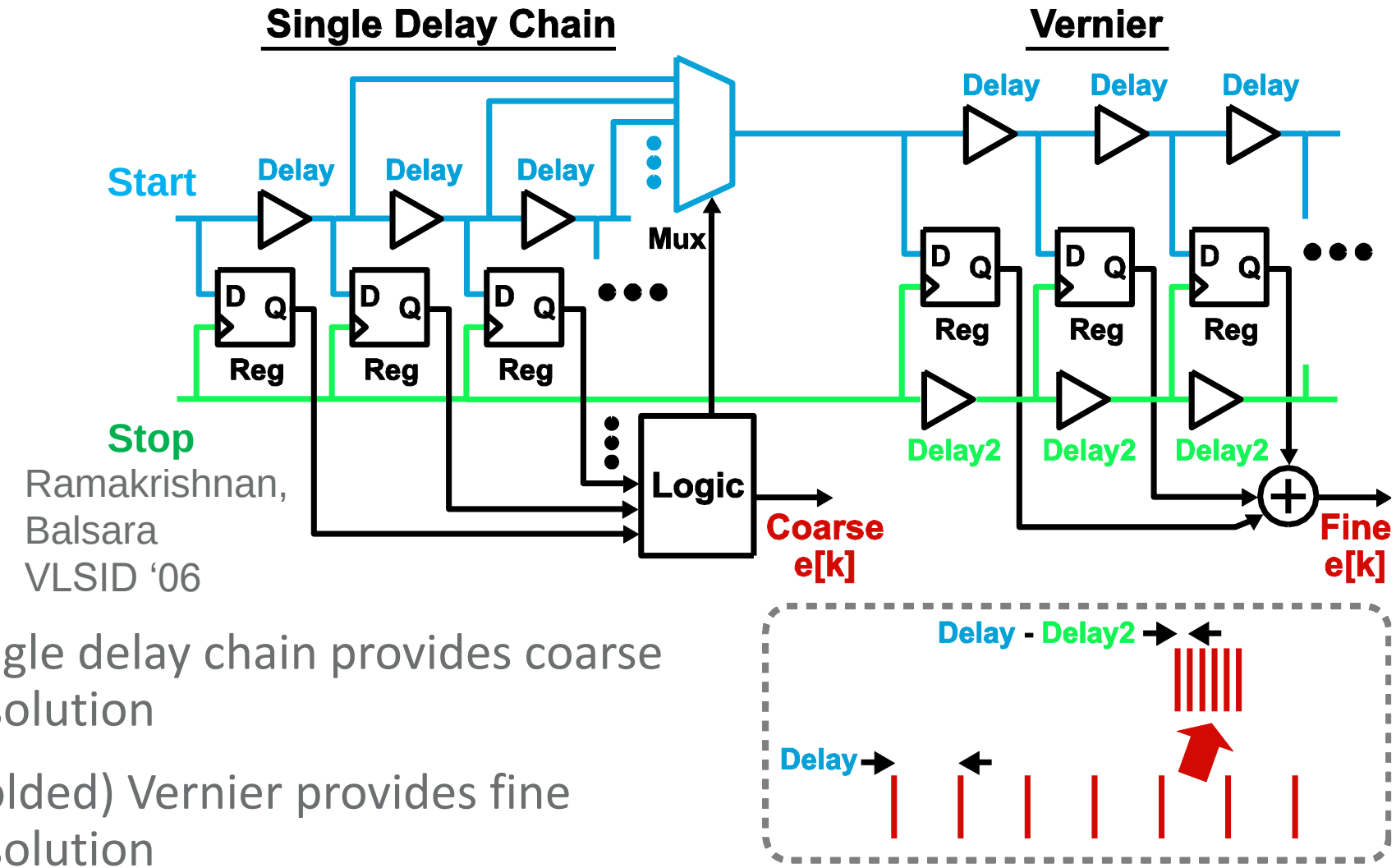
- Resolution can be improved with resistive interpolation
- Range is still limited (Scaling with ~2^{N-1})
- Interpolation technique is also applicable to FLASH ADC

Vernier TDC



- Quantization step size (resolution) is the ***difference*** of delays
  - > ΔT_{del} = Delay – Delay2
- Range is still limited, area is large (Scaling with ~2^N)
- Latency increases significantly due to propagation of both edges

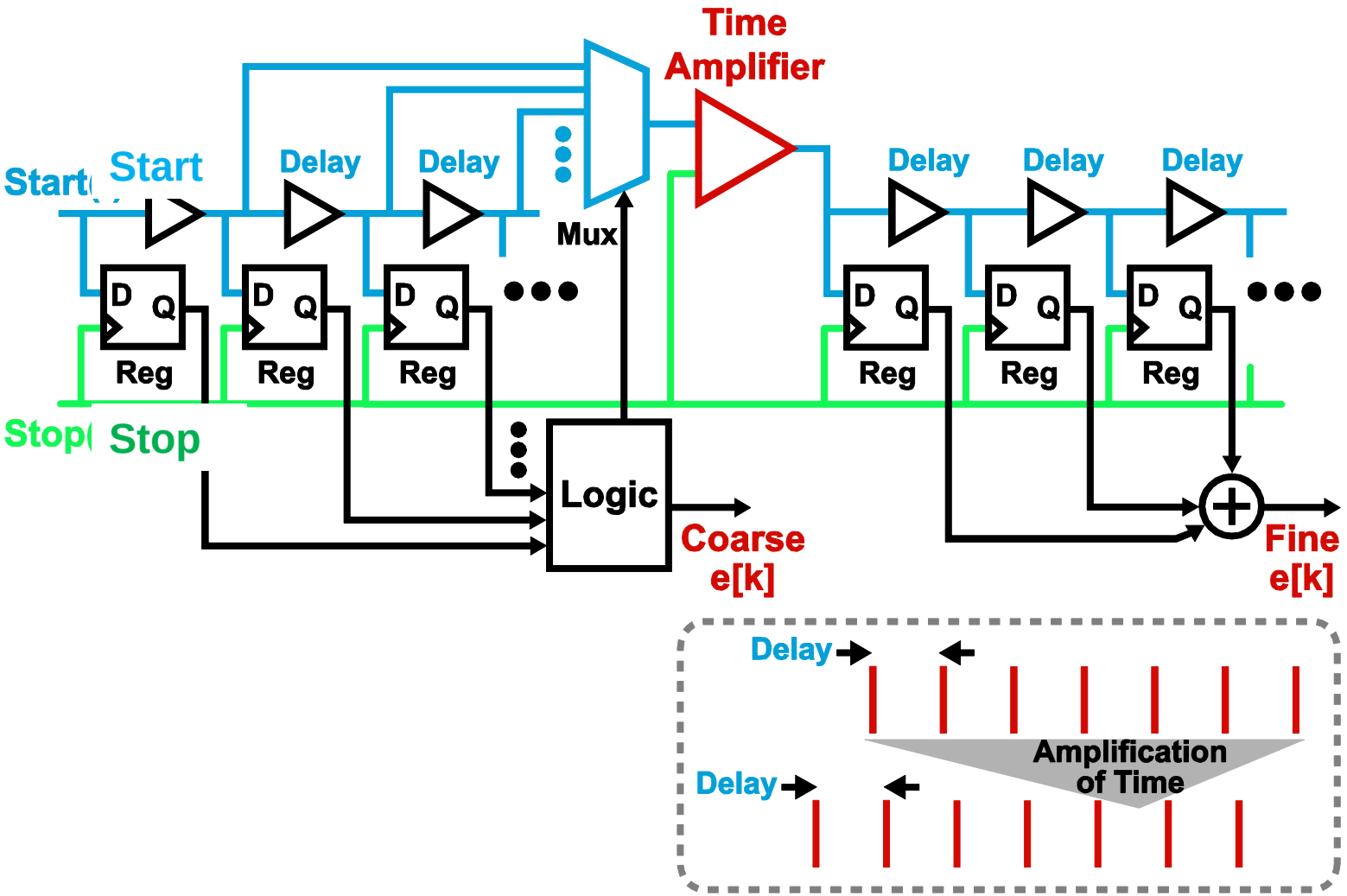
Two-Step TDC to Reduce Area



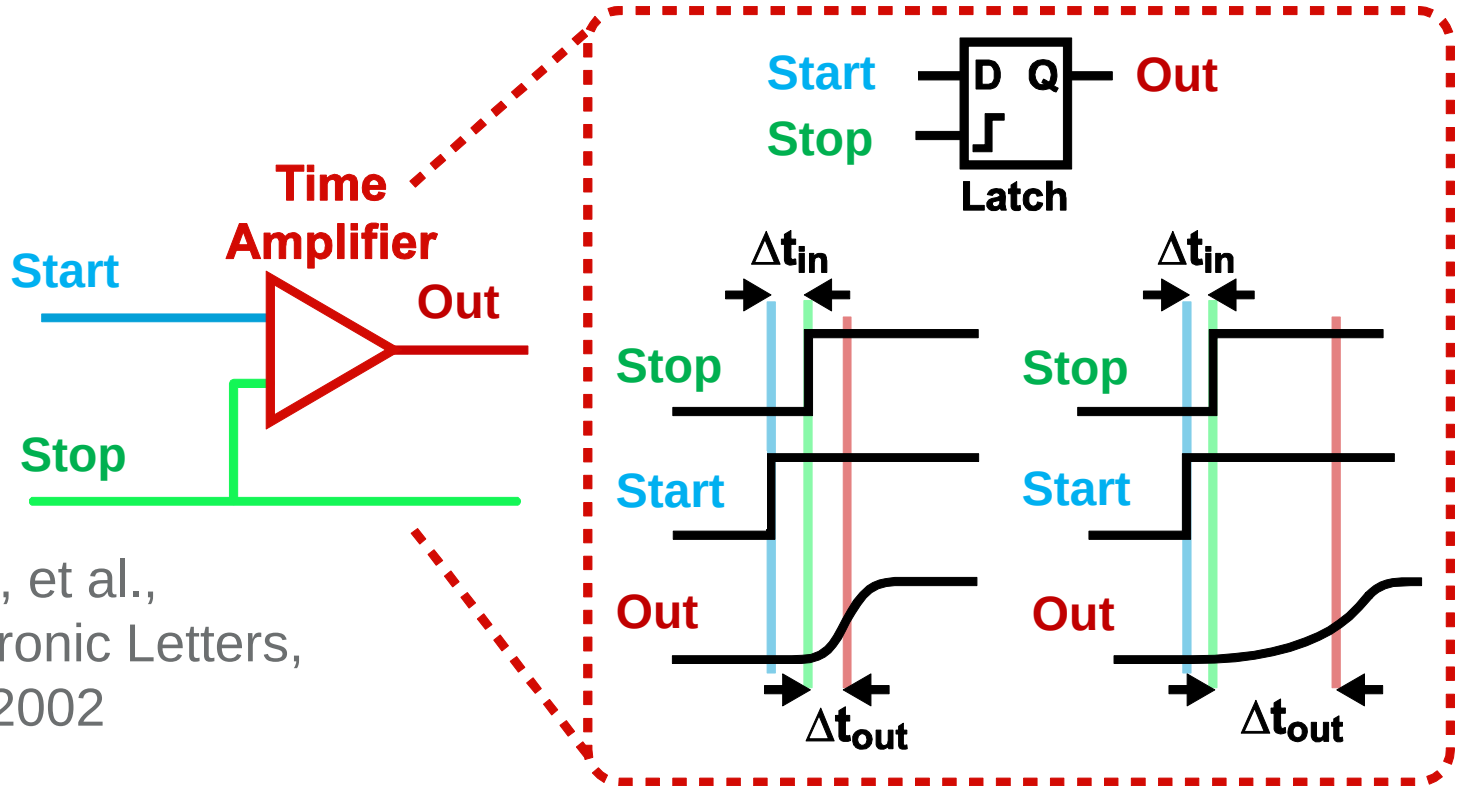
Ramakrishnan, Balsara VLSID '06

- Single delay chain provides coarse resolution
- (Folded) Vernier provides fine resolution

Two-Step TDC with Time Amplifier



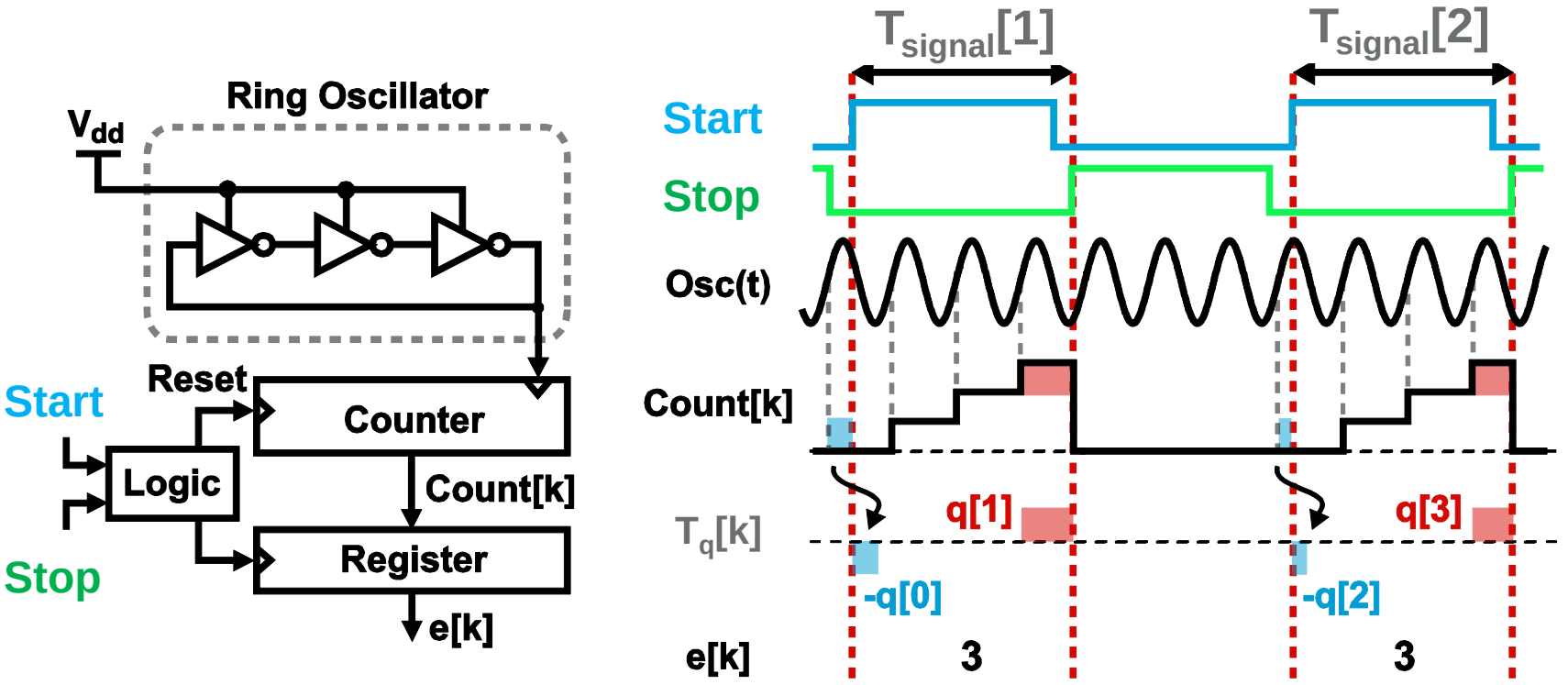
Time Amplifier Example



Abas, et al.,
Electronic Letters,
Nov 2002

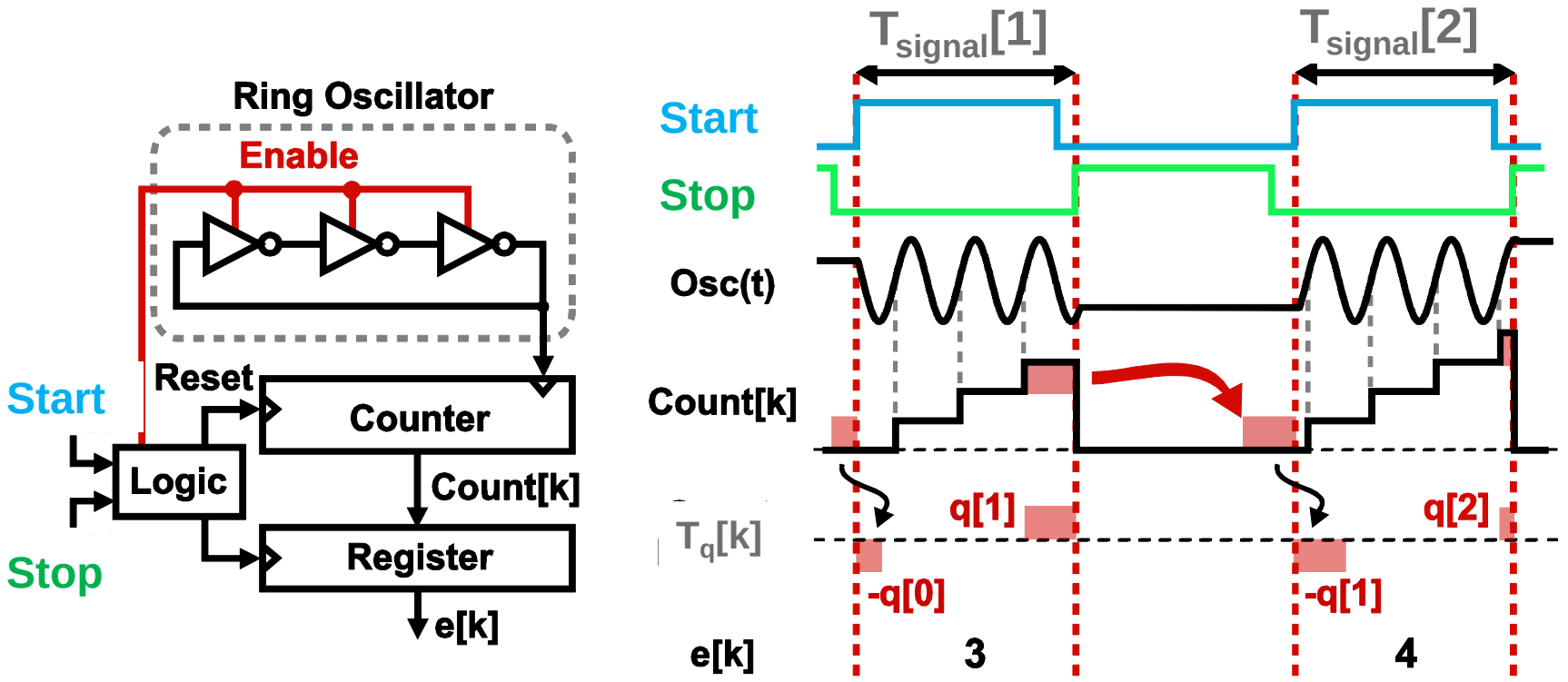
- Time amplifier leverages latch metastability
  - > Highly non-linear (no equivalent to continuous-time feedback)
  - > Requires calibration for precise converters

Ring Oscillators Increase TDC Range



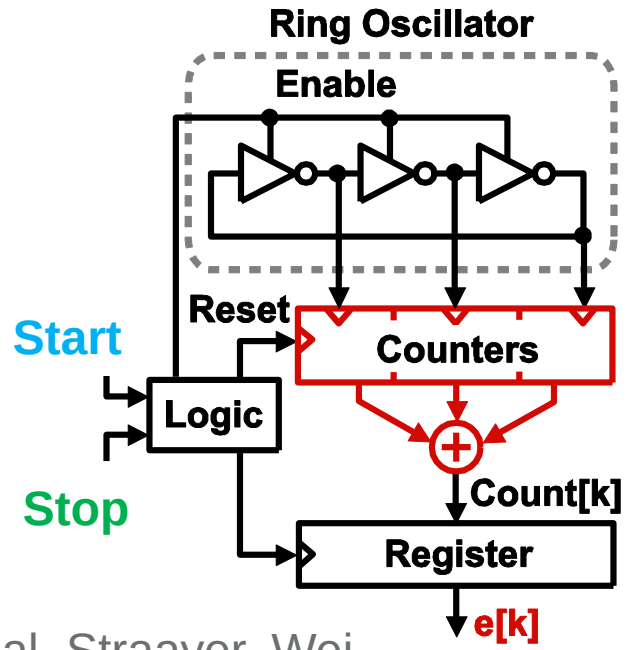
- TDC range has been improved to an arbitrarily large value
  - > Counter scales linearly with N
- But notice that quantization error is added at both the start and the stop of each measurement

Gated Ring Oscillator (GRO) Concept

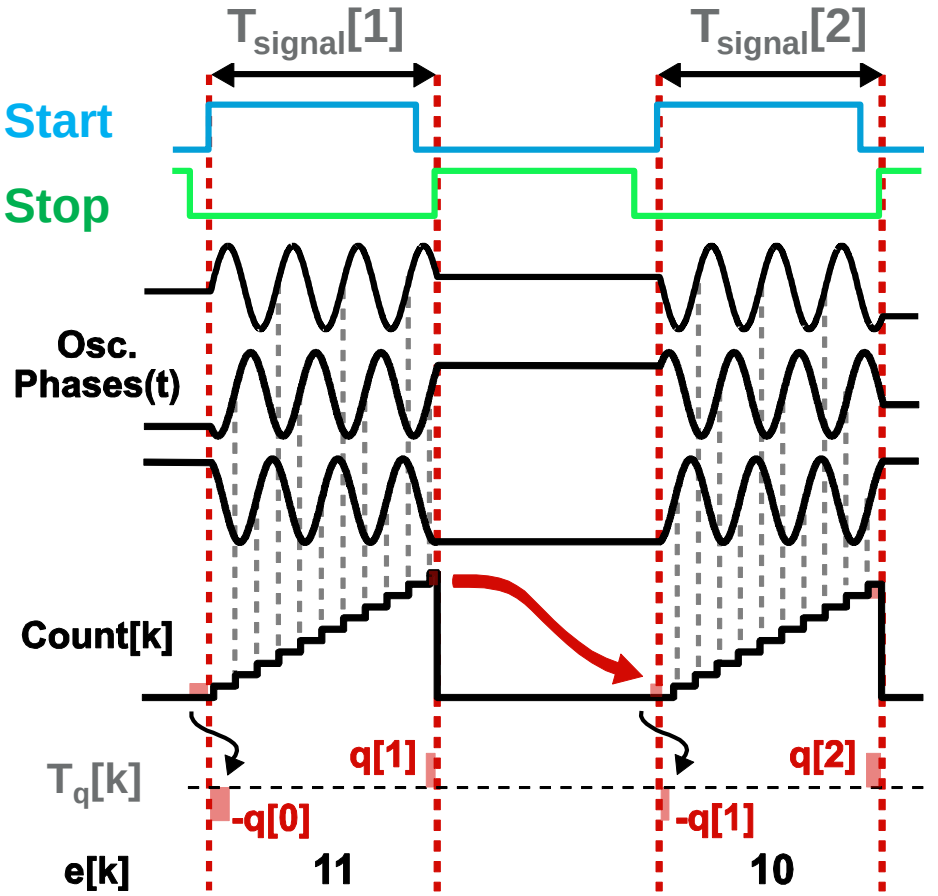


- Gate the oscillator in between measurements
  - > Holds the phase in the 'off' time
  - > Subtracts the previous measurement error from current sample
- Results in first-order quantization noise shaping

Improve Resolution By Using All Oscillator Phases

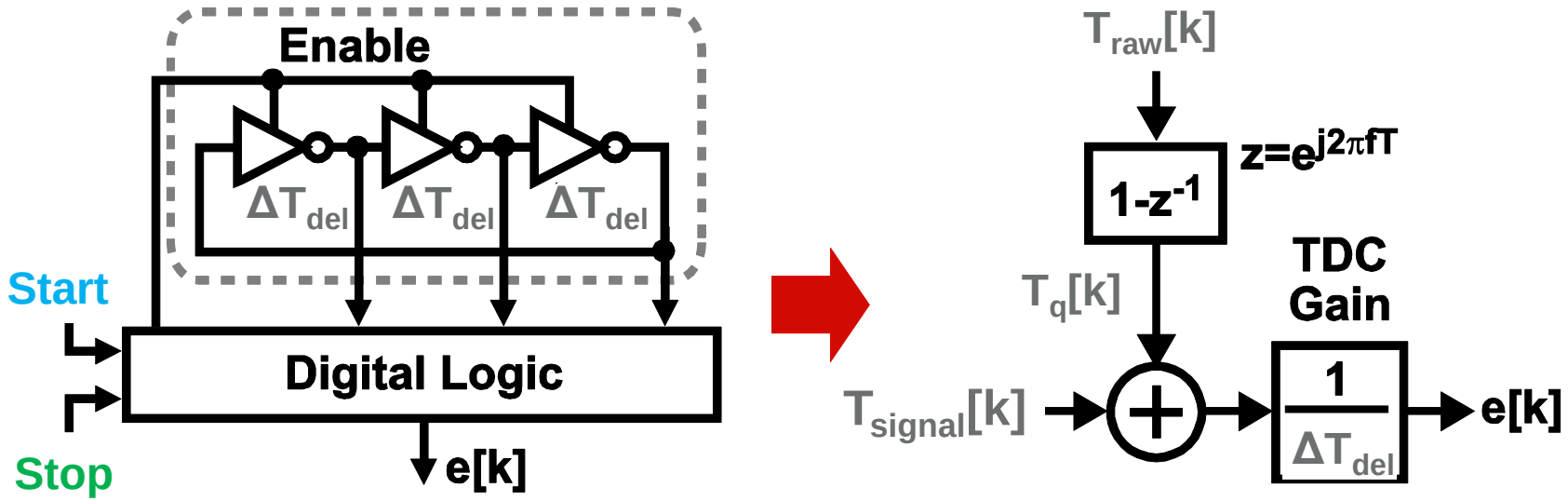


Helal, Straayer, Wei, Perrott VLSI 2007



- Raw resolution is set by inverter delay
- Effective resolution is dramatically improved by averaging

Gated Ring Oscillator Model

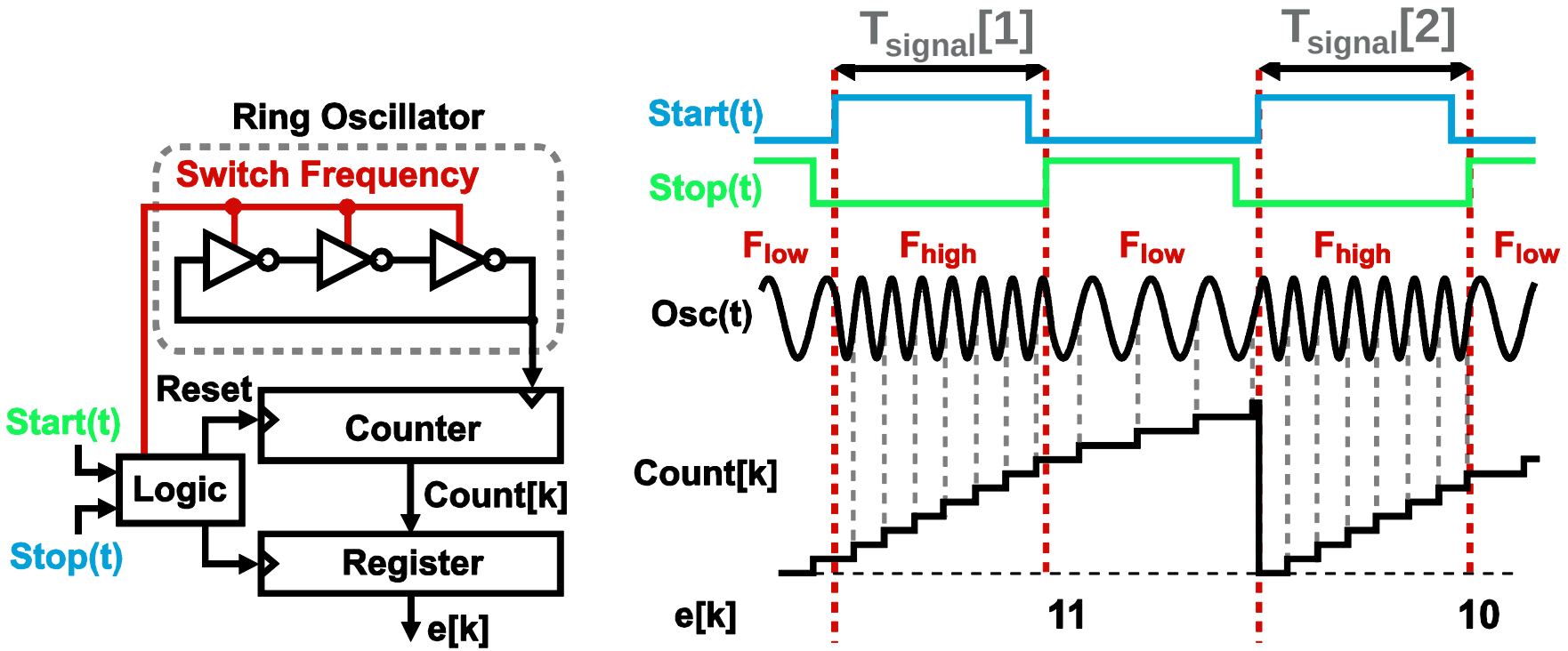


- New transfer function is equal to a 1st order difference:

  $T_q[k] = T_{raw}[k](1-z^{-1})$

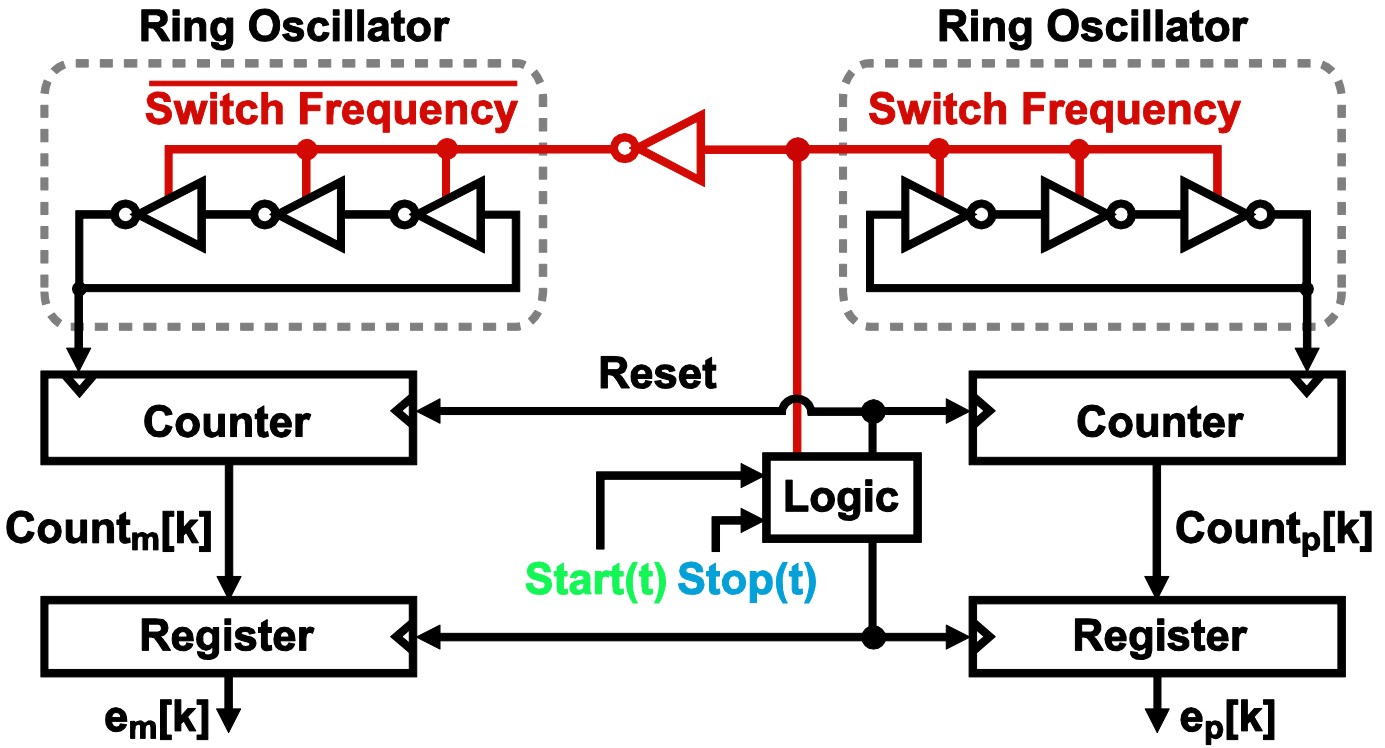
- Note:
  - > Raw error is both mismatch and quantization error
  - > Both error sources are first-order shaped

Another Oversampling TDC: Switched Ring Oscillator



- Frequency is switched between F_{high} and F_{low}
- GRO is special case of $F_{low} = 0$
- A bleeder current when 'off' can improve on/off transitions
  - > Requires a synchronous **Start**

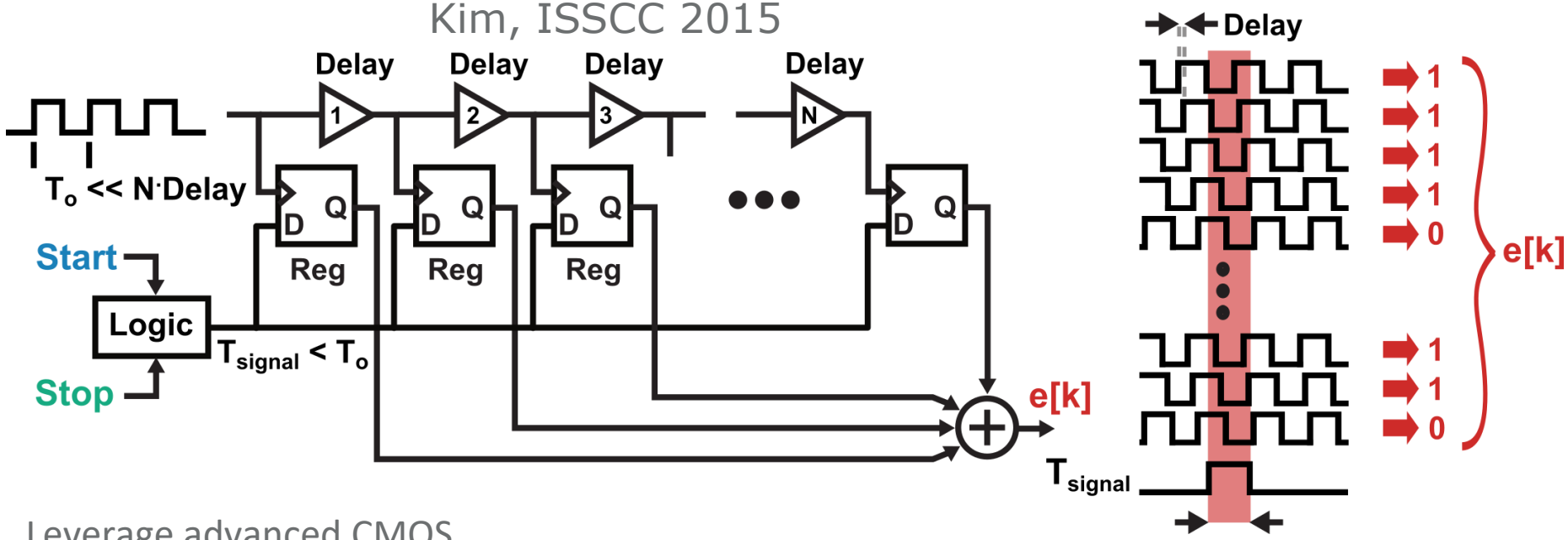
Constant Current Improves Power Supply Coupling



- Significant current when running at F_{high}
  - > Causes supply bounce and ringing that affects TDC linearity
- Switching between 2 oscillators maintains constant supply
  - > Additional noise (or wasted power) for small inputs

Stochastic TDC

Kim, ISSCC 2015



- Leverage advanced CMOS
  - > T_o period << accumulated delay → uniform probability of edges
  - > Mismatch and jitter randomizes edge distribution function
- On average, e[k] = floor(N·T_{signal}/T_o)
  - > N positive edge transitions in each T_o period, e.g. $\Delta T_{del} = T_o/N$
- Gain is proportional to clock frequency, not delay
  - > Noise is not a function of delay, either! But it is a function of T_o jitter…

TDC Metrics

- **Resolution (s)**
  - > Many definitions for resolution
  - > Often misquoted and misunderstood
- **Noise (s^2/Hz)**
  - > Includes thermal and quantization noise
- **Power (W)**
  - > Not necessarily linear with 1/resolution
  - > Superlinear with 1/PSD
- **Sampling rate (Hz)**
  - > Power is a linear function of sample rate
- **Range (s)**
  - > Very dependent on application, only needs to meet a minimum requirement
  - > Delay thermal noise typically increases as square root of T_{signal}
  - > Power also increases linearly with time interval or range, for same resolution
- **Area (mm2)**
  - > Often a strong function of process, but architecture matters
- **Latency (samples)**
  - > For some applications low latency is critical (PLL)

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Orange are fundamental metrics

TDC Resolution

‘Raw’ resolution:

- Quantization step size = fullscale range / number of levels
  - > For a linear TDC, equal to an inverter delay

‘Single-shot’ resolution: *not commonly used*

- Error bound of a single measurement, how many sigma is often not clear
  - > Includes thermal and quantization noise
  - > Does not typically include large-signal integral non-linearity
  - > More often used for detecting physical events

‘Effective’ resolution:

- RMS error including thermal and quantization noise (σ_{err})
  - > Nyquist TDC where bandwidth is half the sampling rate can use a histogram can be helpful to determine standard deviation Metric can be a function of input, or specific points on the transfer characteristic
  - > Oversampling TDC can use integrated Power Spectral Density

TDC Figure of Merit

Be very careful - not the same as ADCs!

No agreed-upon standard for TDC FOM

Potential option #1: Quantization noise limited TDC

- FOM = $10 \cdot \log_{10}(P \cdot \sigma_{err} / BW / T_{signal})$ dB W-s

Potential option #2: Thermal noise limited TDC

- FOM = $10 \cdot \log_{10}(P \cdot \sigma^2_{err} / BW / T_{signal})$ dB W-s^2

Where σ_{err} is measured with T_{signal} input, both in seconds
Note that T_{signal} ≠ maximum TDC input range

Outline

- *Introduction to Time-Based Circuits*
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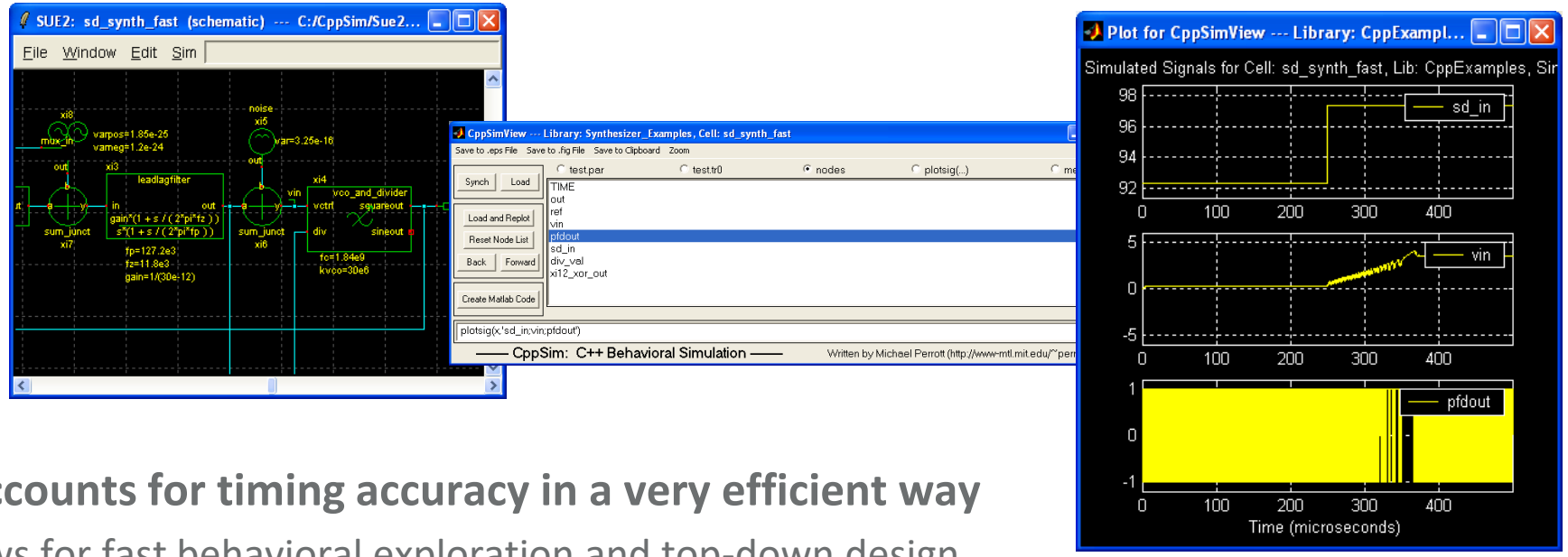
- *Summary and Conclusions*

Design Tool Considerations

Time-based signals have different time resolution requirements than typical voltage or current-based circuits

- > Verilog can be challenging to integrate analog circuits
- > SPICE/Spectre take a long time, difficult to design architectures



CPPSIM accounts for timing accuracy in a very efficient way

- > Allows for fast behavioral exploration and top-down design
- > Analog can be combined with digital for a unified flow

Examples and tutorials at:

http://www.cppsim.com

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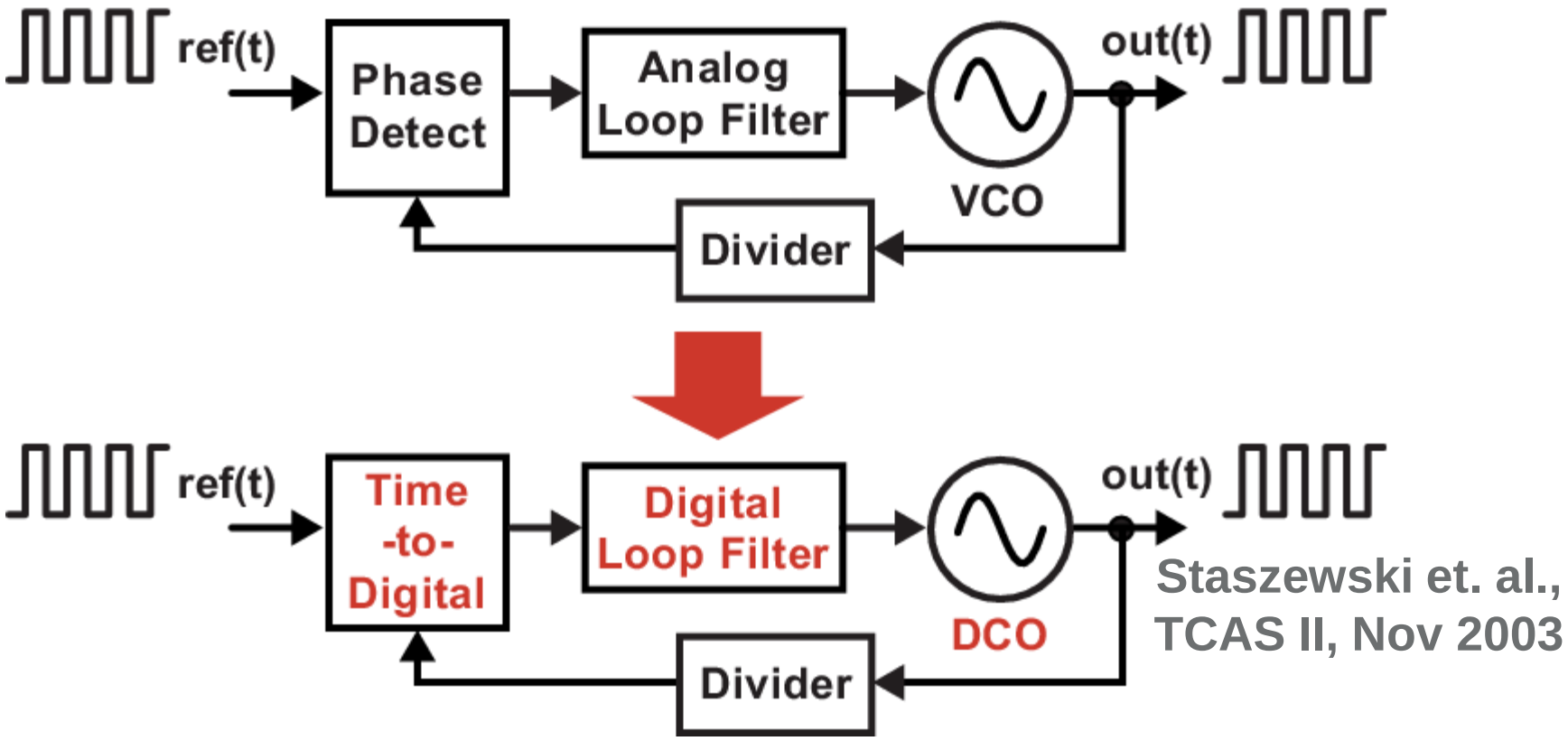
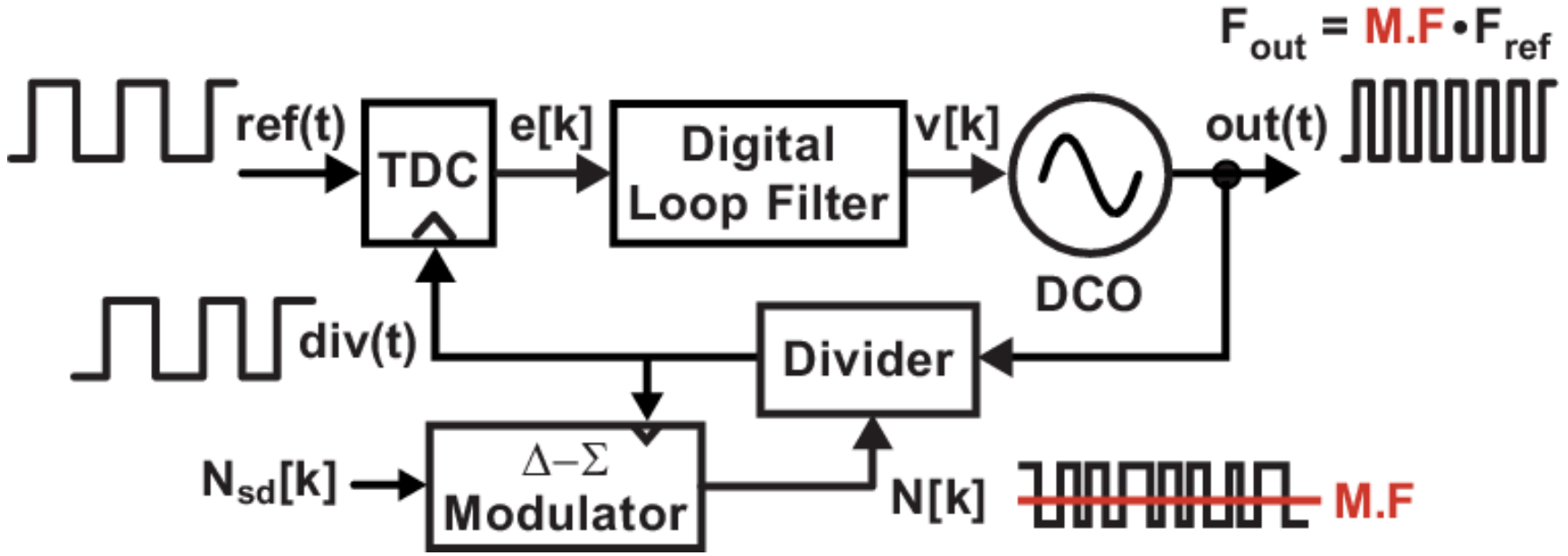
Analog and Digital PLL



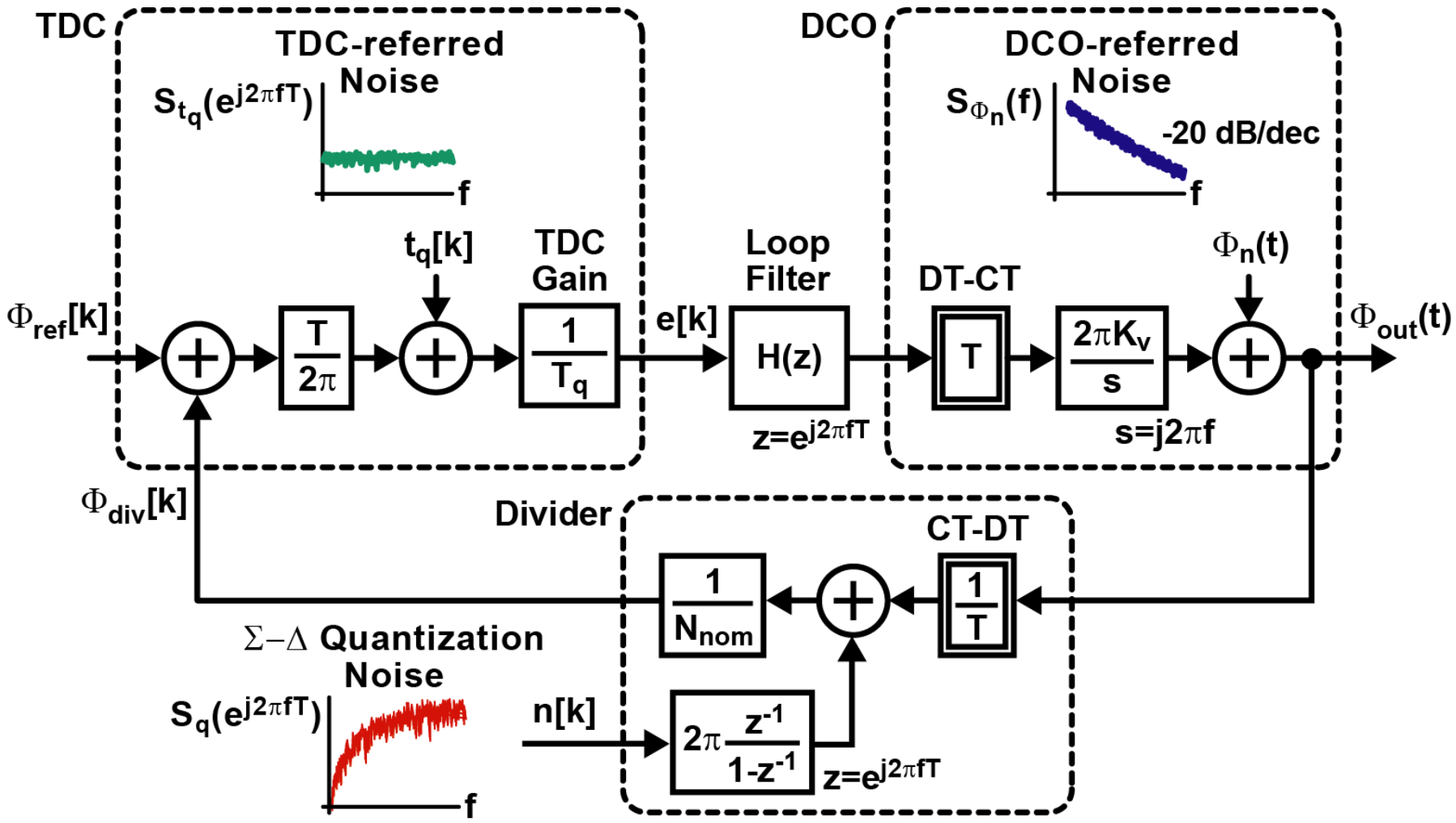
Staszewski et. al.,
TCAS II, Nov 2003

Fractional-N DPLL Block Diagram



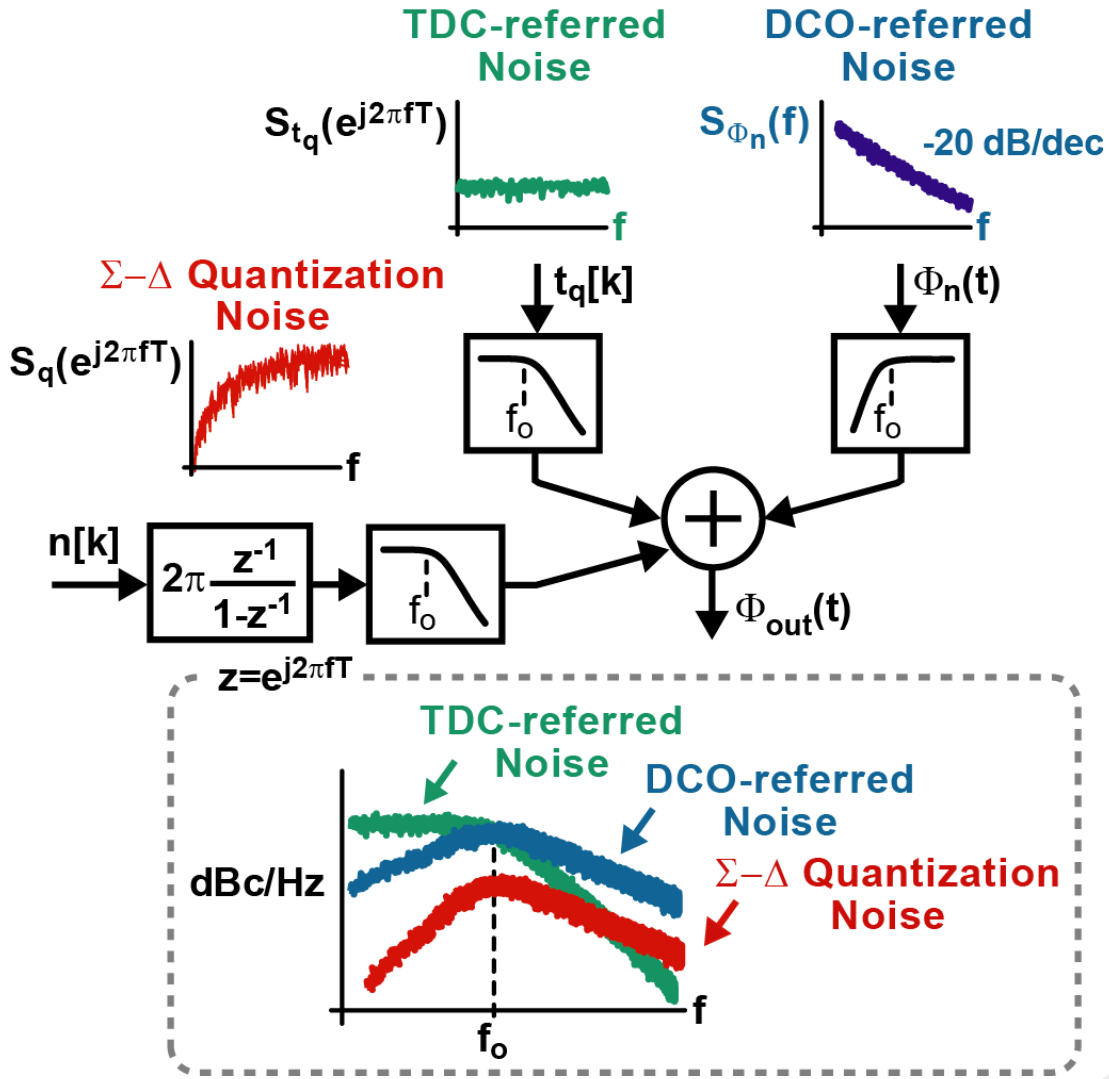
- Frac-N PLL has challenging TDC requirements:
  - > Low latency
  - > Low thermal noise
  - > Even lower quantization noise

Fractional-N DPLL Model



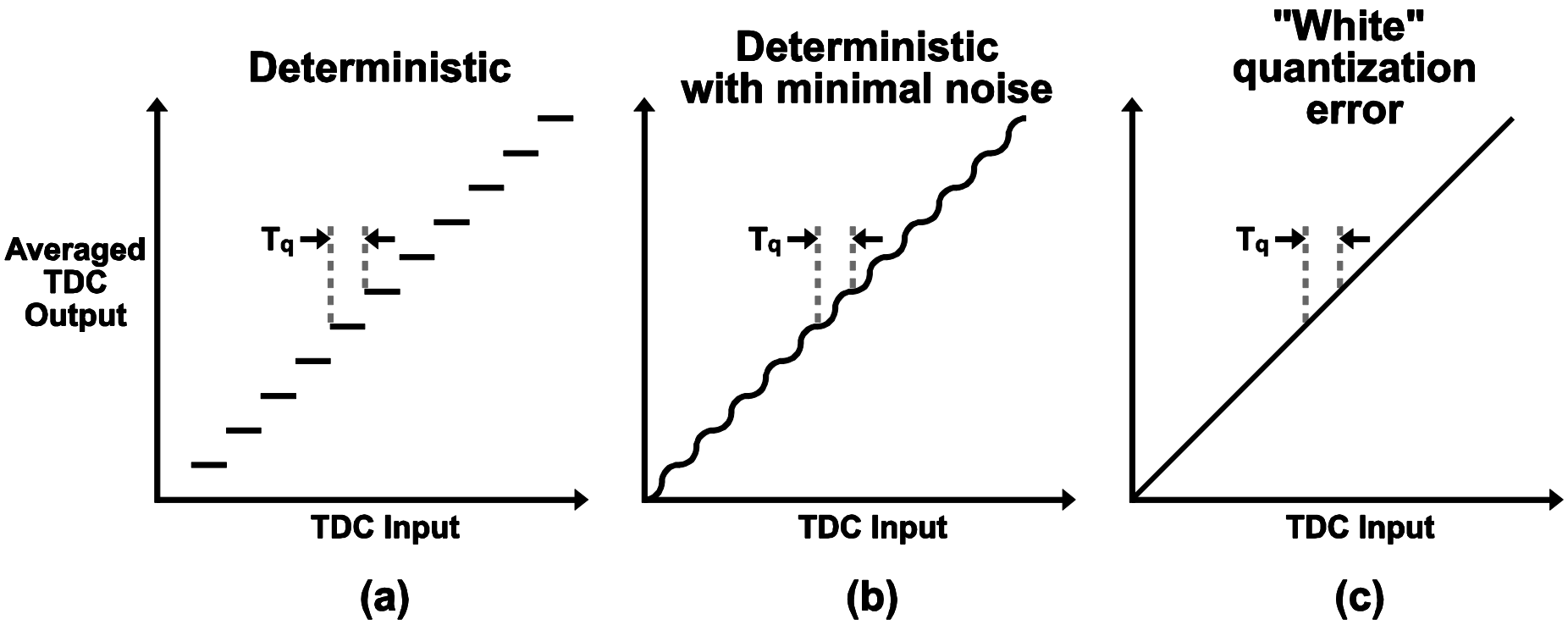
DPLL Closed-Loop Noise Contributions

- TDC noise dominates in-band at low frequency
  - > High-frequency TDC noise is low-pass filtered
- TDC non-linearity folds back in-band and can cause limit-cycles or spurs
  - > Deadzones in TDC transfer characteristic
  - > ‘Staircase’ quantization
  - > Power supply coupling

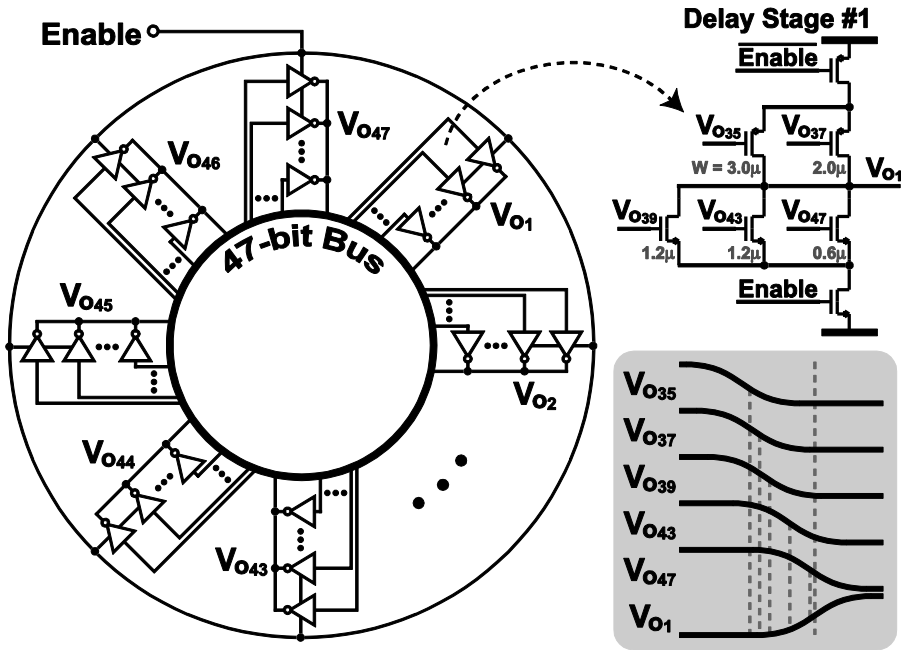


TDC Transfer Characteristics

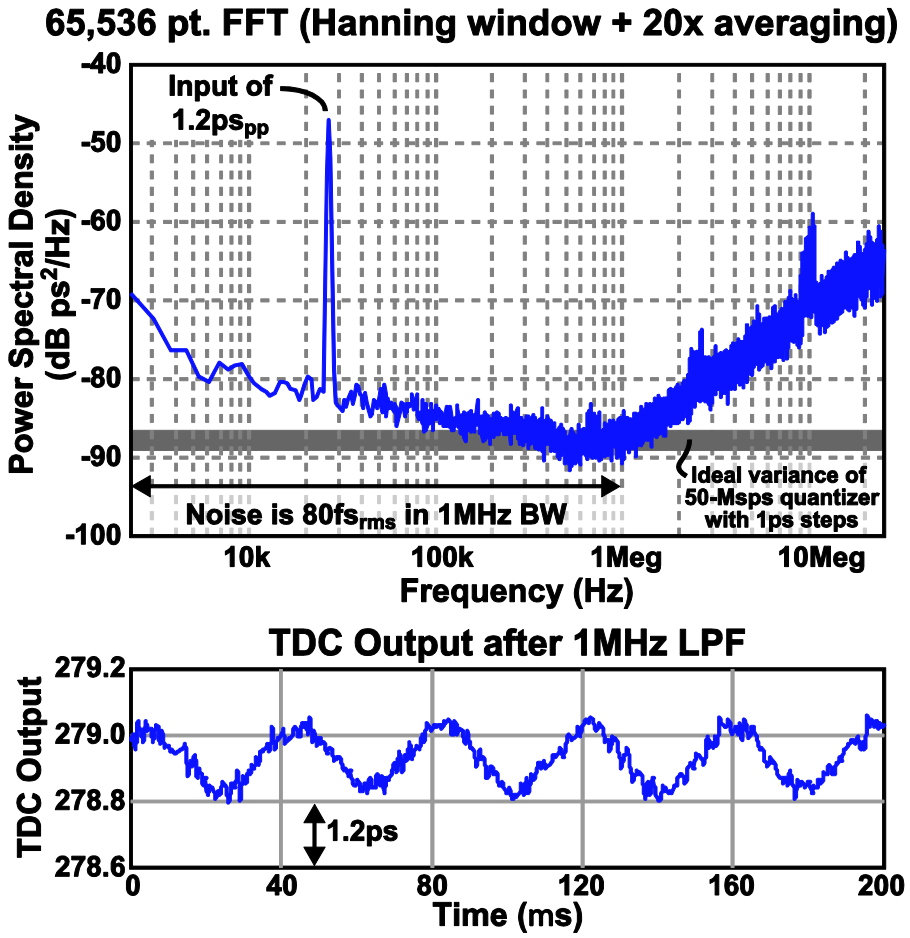
- Ideally TDC transfer characteristic is linear
- Deterministic quantization can be a problem if the thermal noise is less than the quantization step



Example GRO TDC



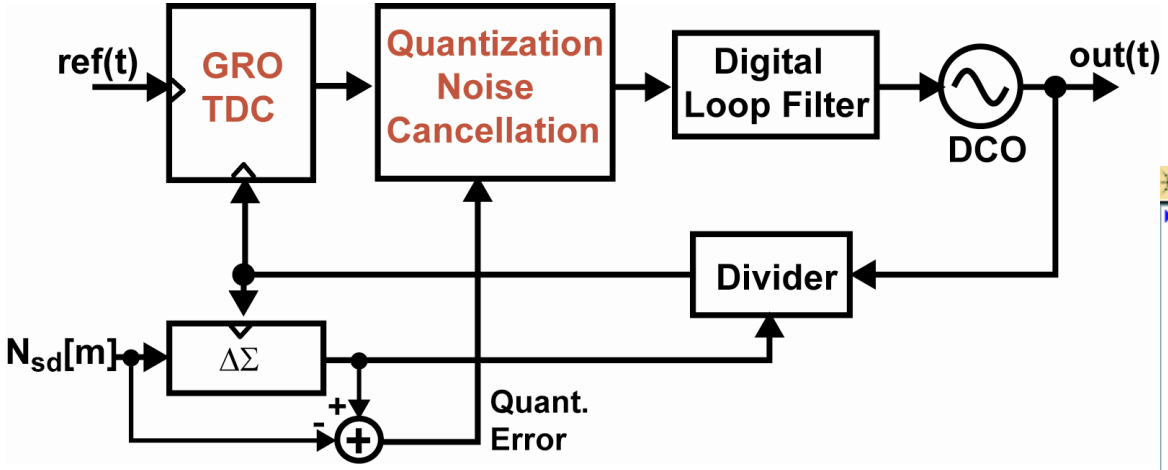
Straayer, Perrott, JSSCC 2009



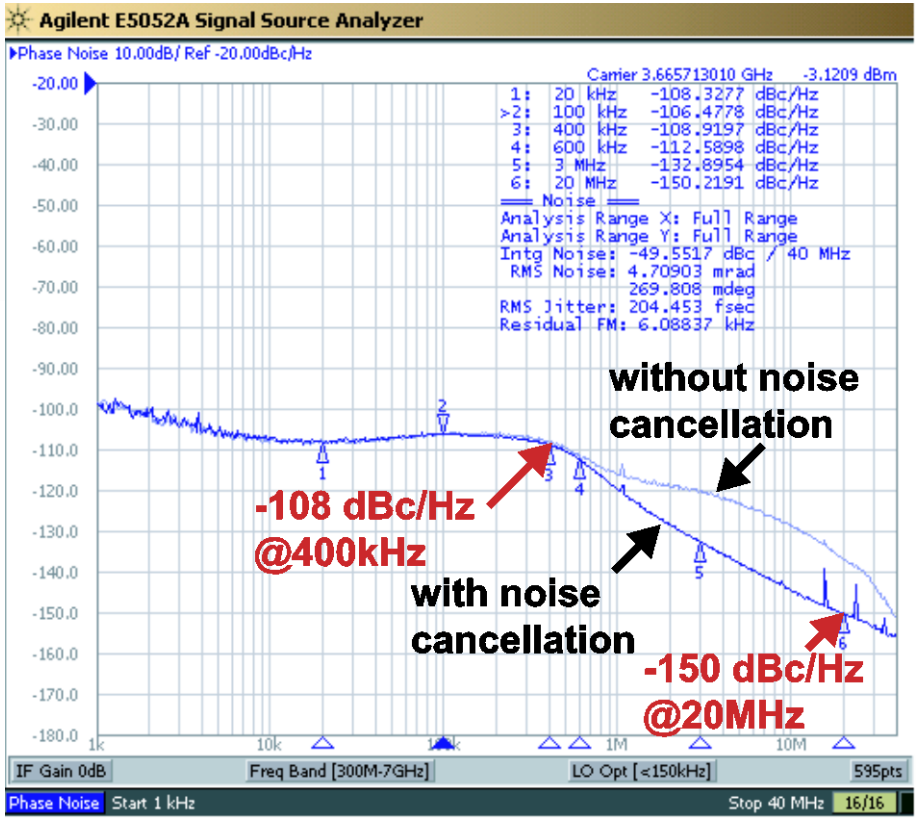
Noise shaping GRO TDC optimized for low frequency noise performance

- Limited by 1/f noise to 600kHz
- Linear transfer characteristic

Example DPLL utilizing GRO TDC



Hsu, JSSCC 2008



- Gated-ring-oscillator (GRO) TDC achieves low in-band noise
- All-digital quantization noise cancellation achieves low out-of-band noise

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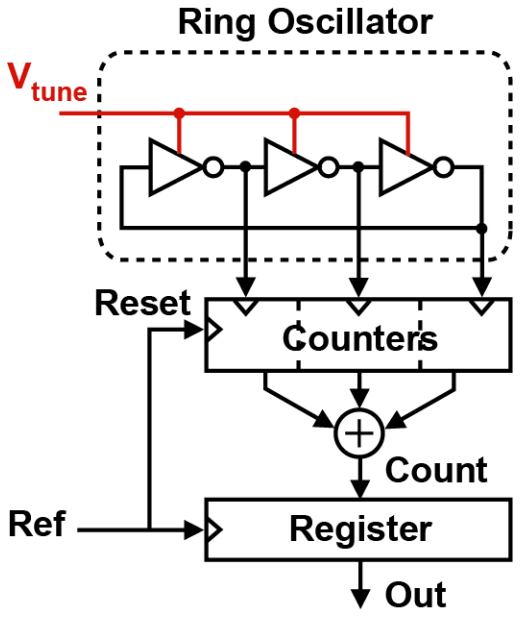
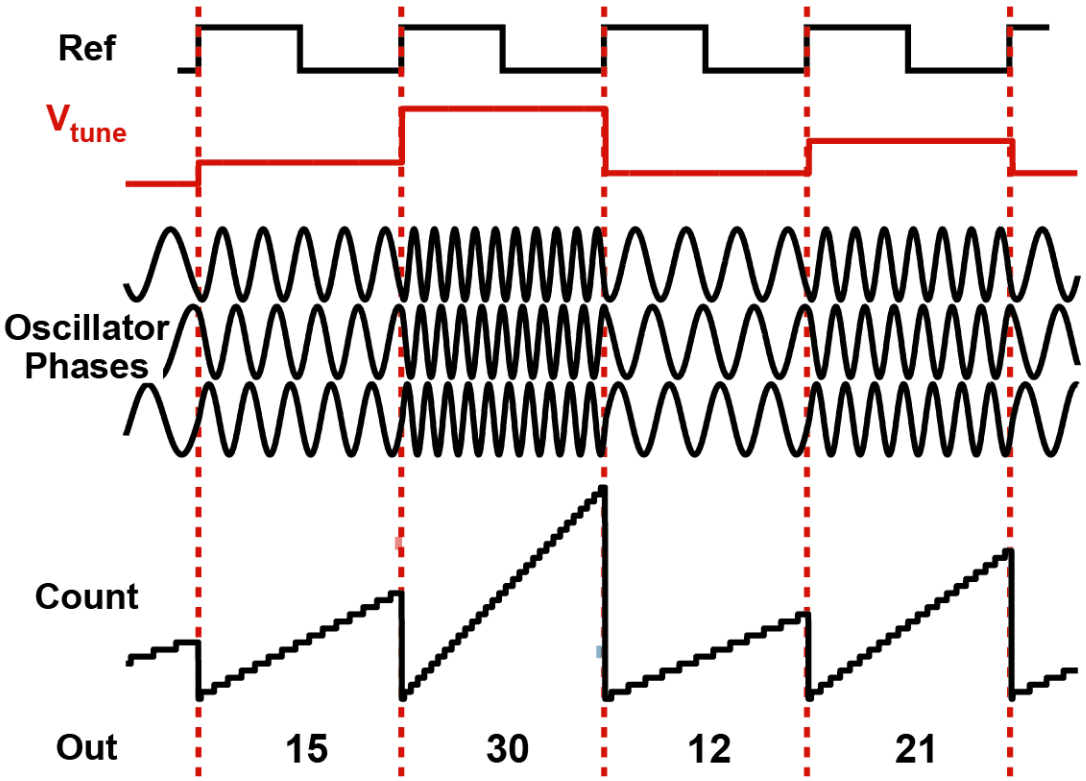
Using a VCO as an ADC

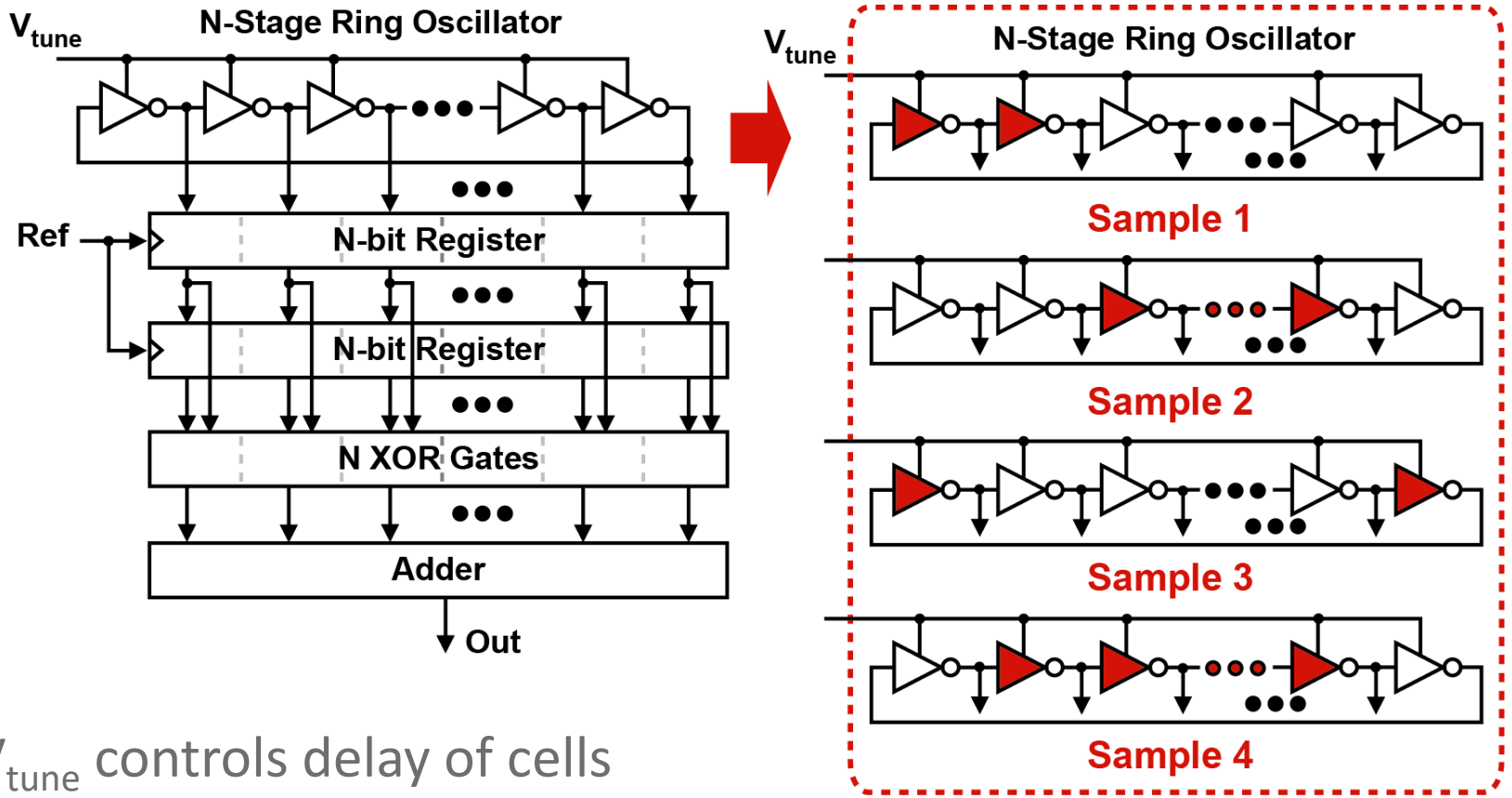




Wismar, ESSCIRC 2006
Kim, ISCAS 2006
Alon, JSSC 2005

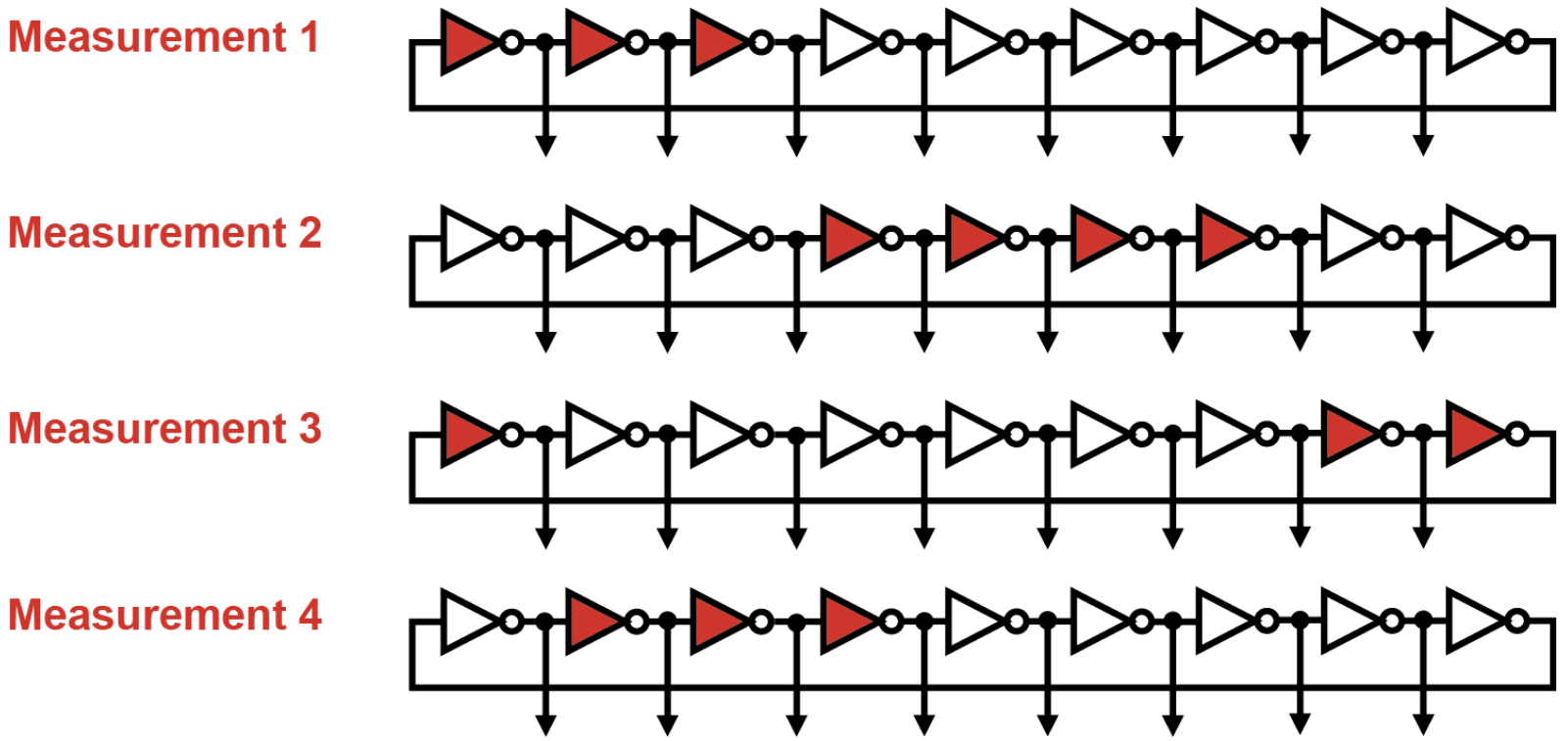
- Input: analog tuning of ring oscillator frequency
- Output: count of oscillator cycles per Ref clock period

Phase Sampling Can Be More Efficient than Counting



- V_{tune} controls delay of cells
  - > Alters the number of transitions per ref clock period
- Digital circuits compute transition count at each sample

VCO-based Quantizer Shapes Delay Mismatch



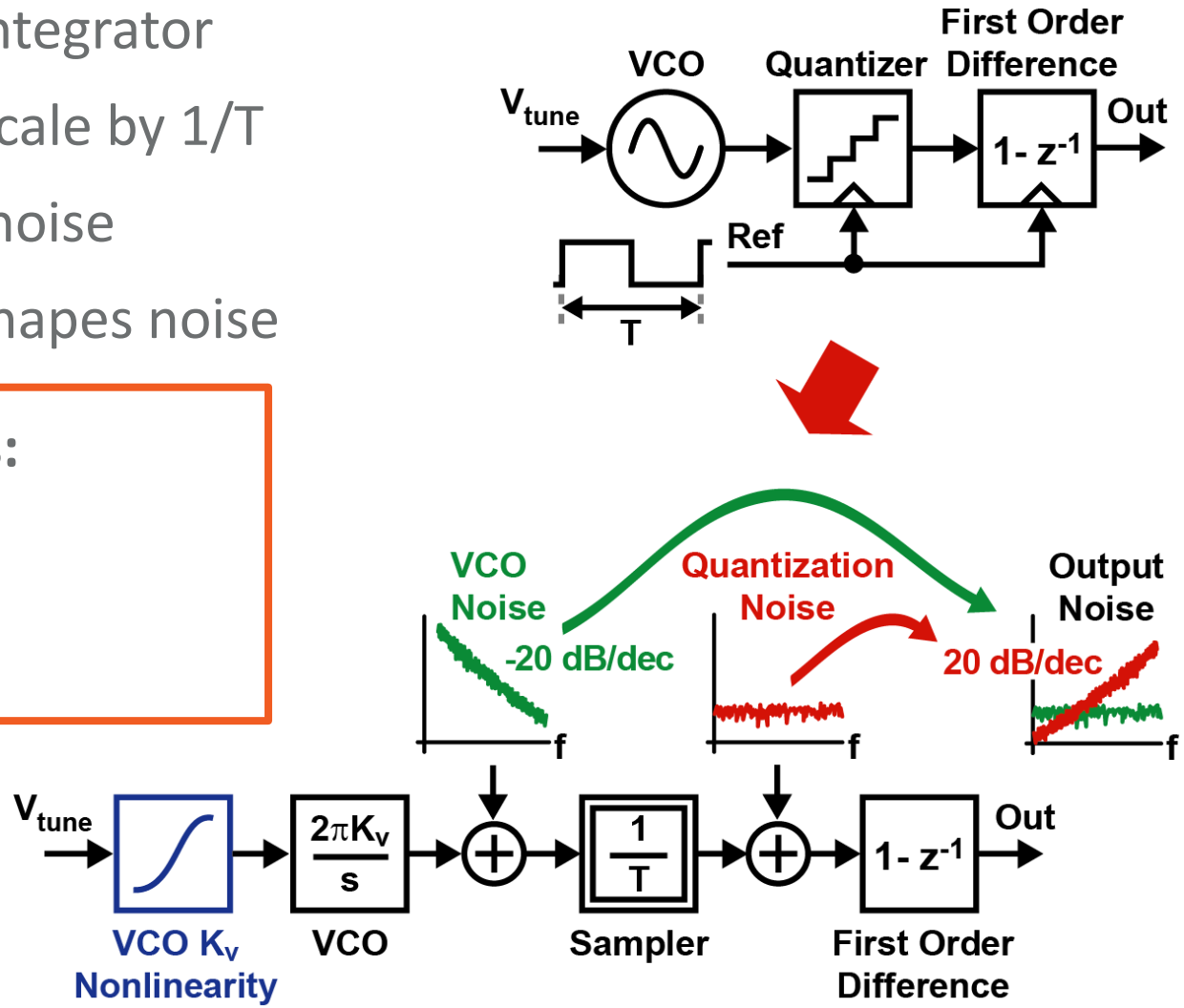
- Barrel shifting through delay elements
  - > Mismatch between delay elements is first order shaped

VCO-based Quantizer Model

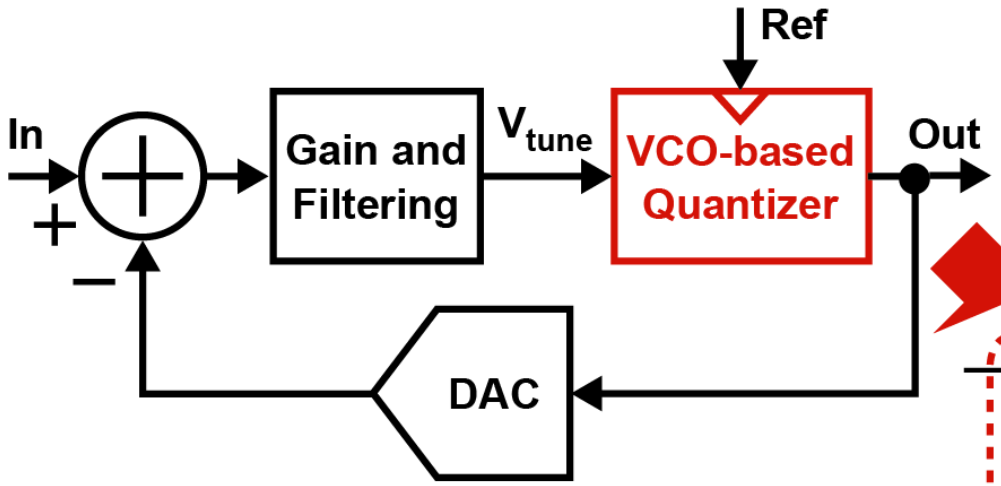
- VCO: nonlinear integrator
- Phase sampler: scale by 1/T
- Quantizer: adds noise
- First order diff: shapes noise

Key non-idealities:

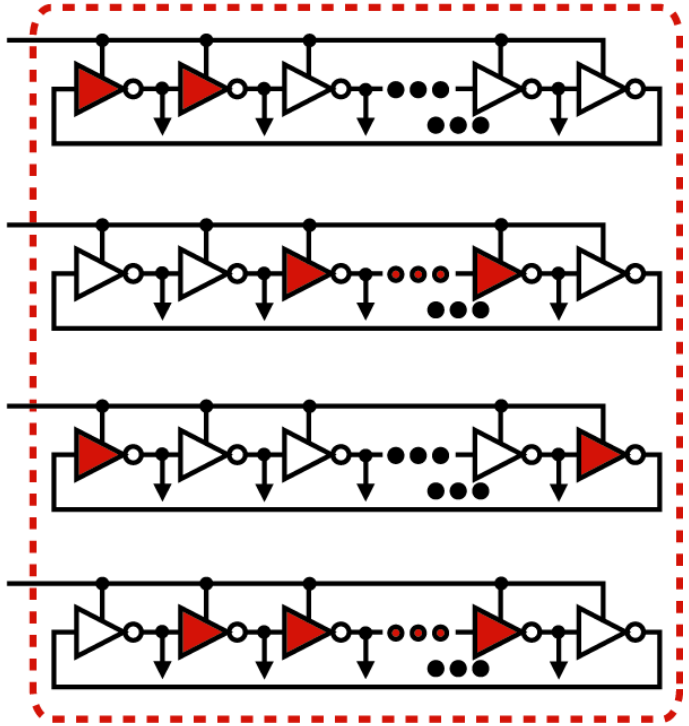
- VCO K_v nonlinearity
- VCO noise
- Quantization noise



Reducing the Impact of Nonlinearity using Feedback

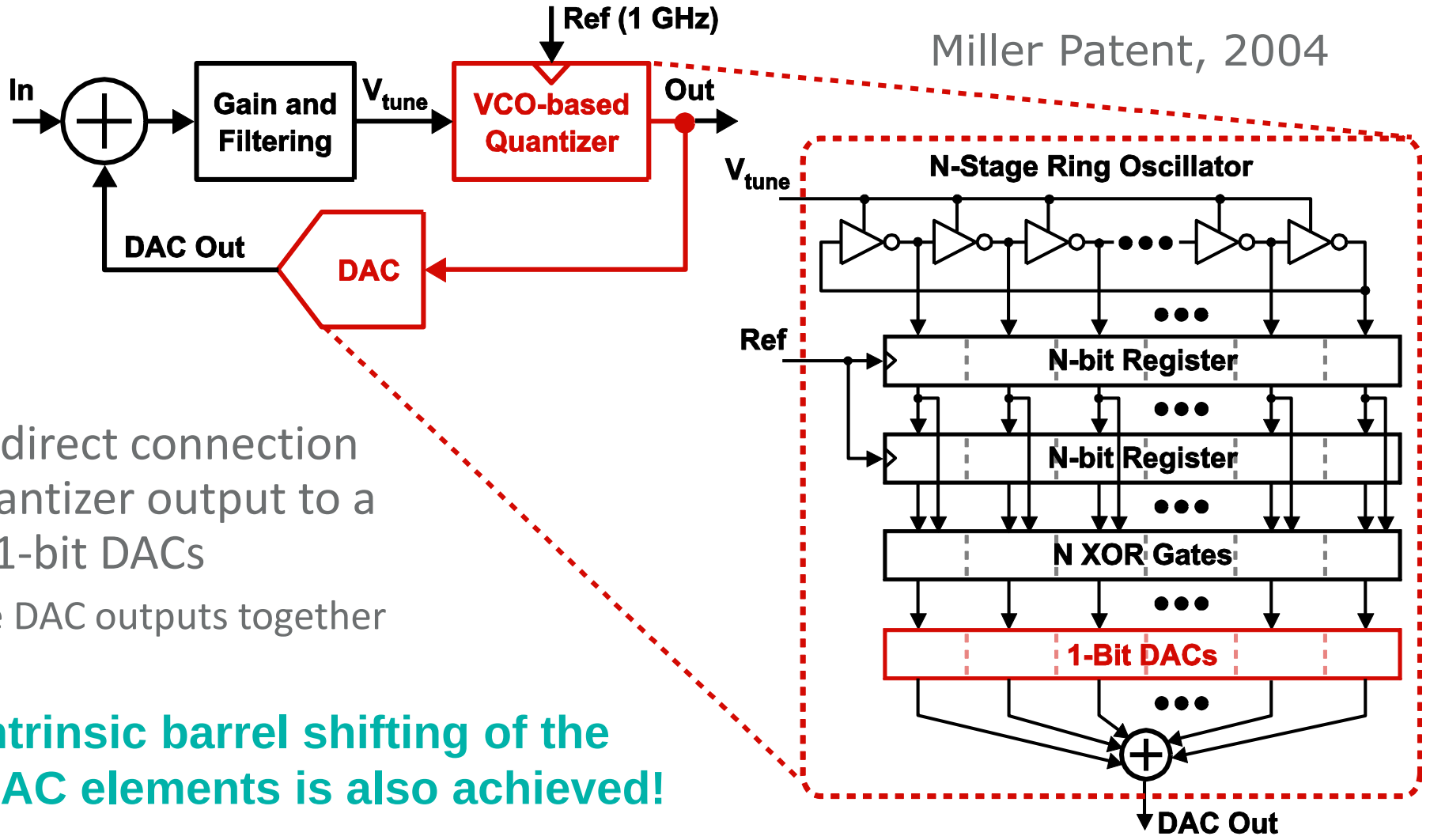


Iwata, Sakimura, TCAS II, 1999
Naiknaware, Tang, Fiez, TCAS II, 2000



- Continuous-time $\Delta-\Sigma$ ADC
  - > VCO-based quantizer provides multi-bit implementation with first order noise shaping
- Gain before VCO quantizer
  - > Suppresses VCO nonlinearity
  - > Suppresses VCO phase noise

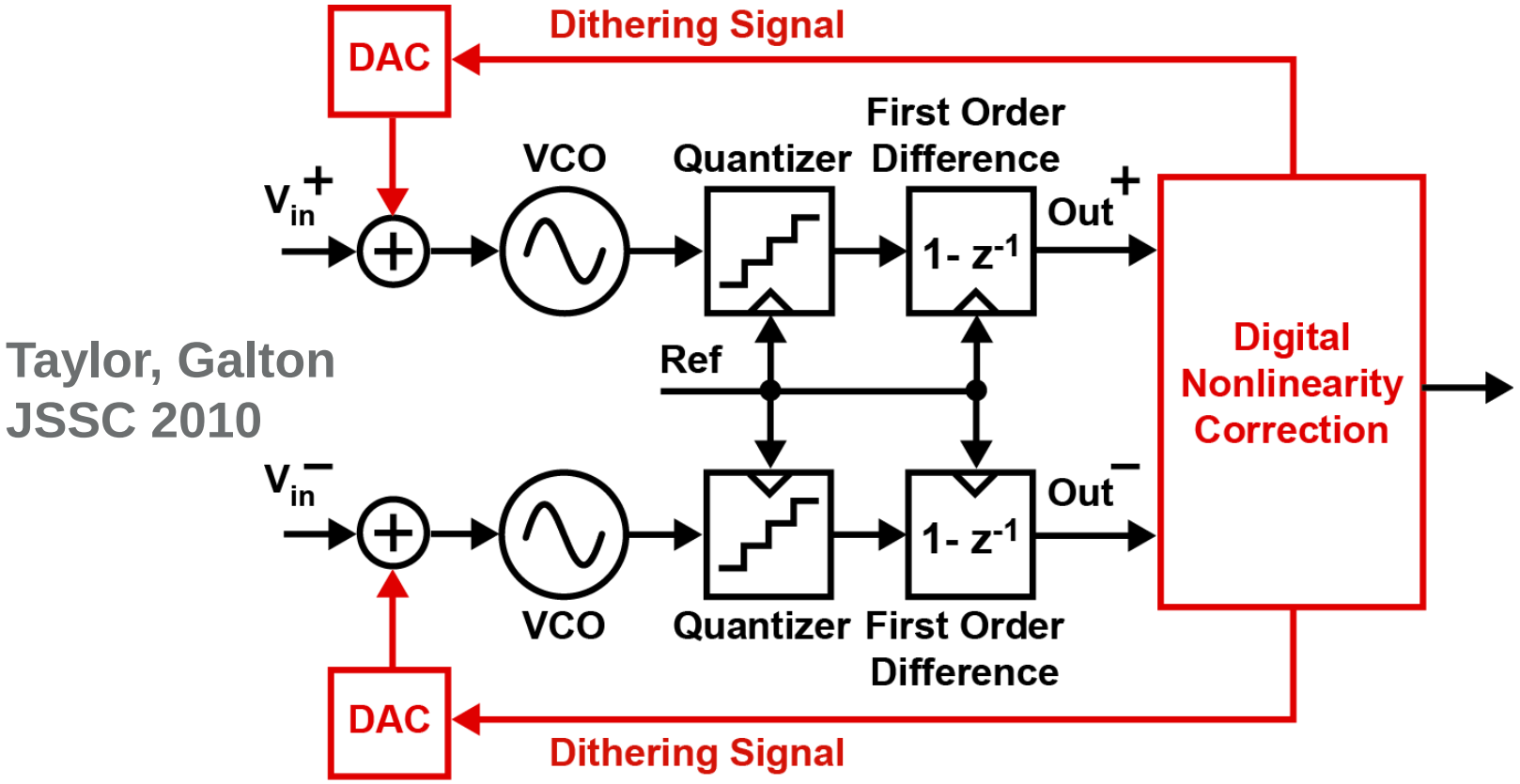
Leveraging Barrel Shifting



- Consider direct connection of the quantizer output to a series of 1-bit DACs
  - > Add the DAC outputs together

Intrinsic barrel shifting of the DAC elements is also achieved!

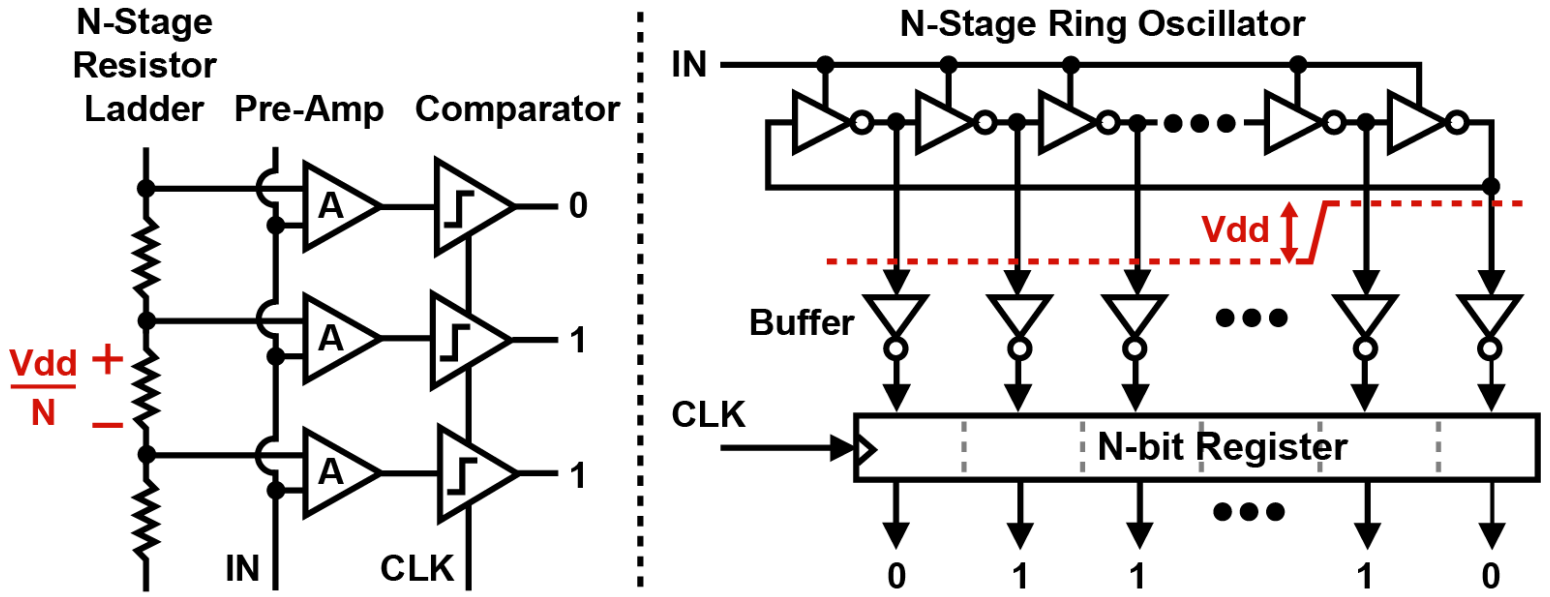
Reducing the VCO Nonlinearity with Digital Correction



Taylor, Galton
JSSC 2010

- Highly digital implementation (65nm CMOS)
- Issues: calibration time, only first order noise shaping

Advantages of VCO-based Quantizers

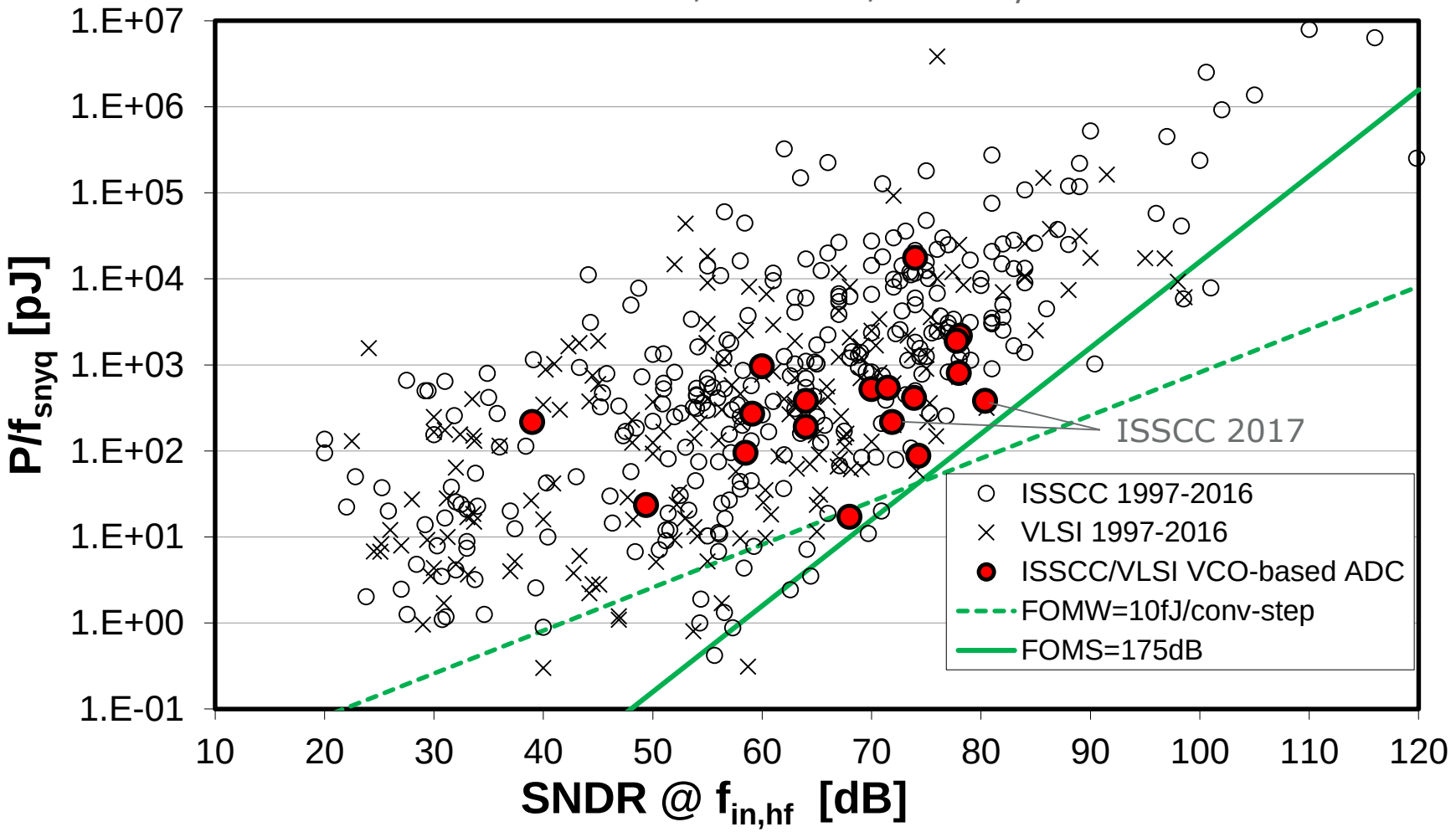


- Highly digital implementation
- Offset and mismatch is not of critical concern
- Metastability behavior is potentially improved
- SNR improves due to quantization noise shaping

Implementation is high speed, low power, low area

Performance of VCO-based ADCs

Based on: www.stanford.edu/~murmann/adcsurvey.html



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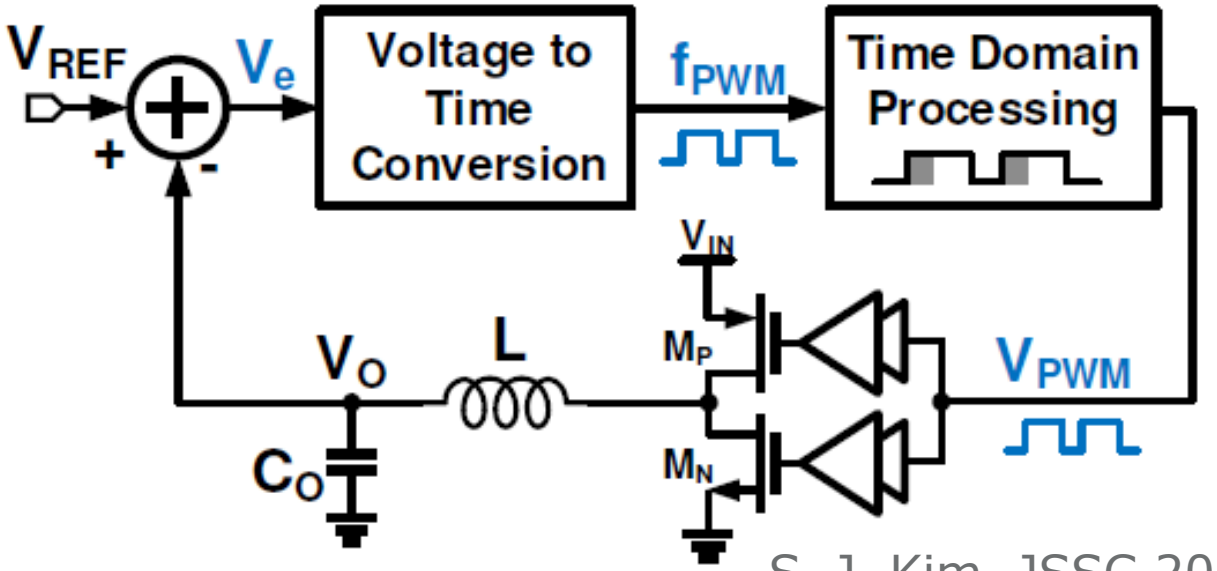
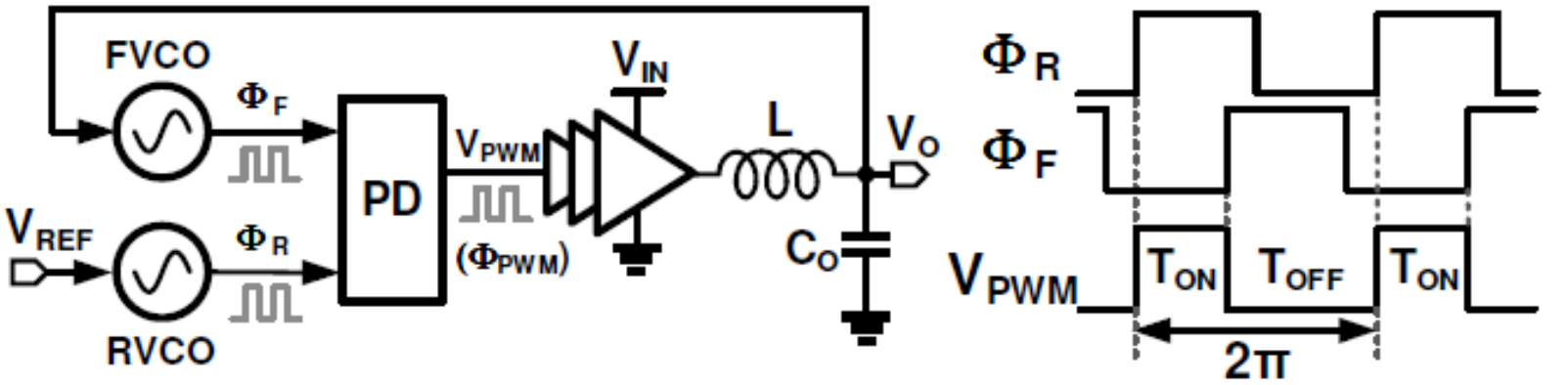
Switched Mode Buck Converter with Time-based Control



S.-J. Kim, JSSC 2015

- No quantization error
- Implicit PWM generation
- Area and power efficient

Time-based Type-I Buck Converter

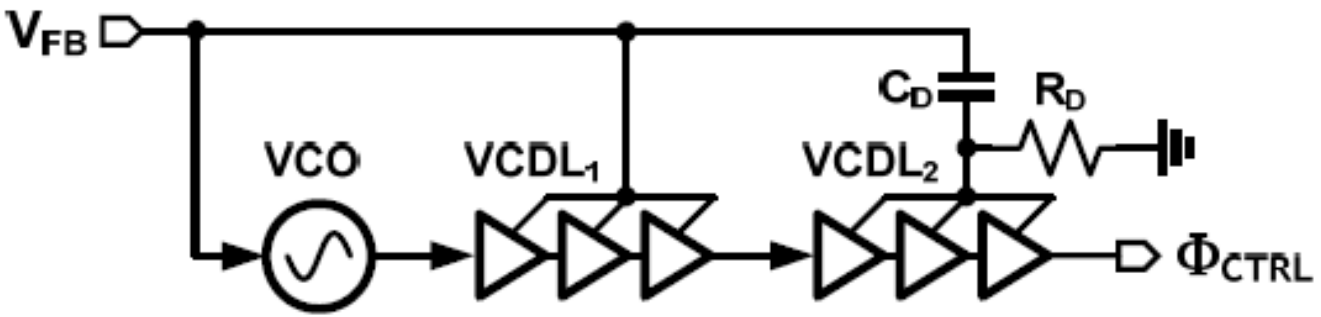


Q. Khan, VLSI 2014

- Behaves as a frequency-locked loop
- In steady-state $F_{FVCO} = F_{RVCO}$
  - > → $V_O = V_{REF} = DV_{IN}$
- Area and power efficient

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{(\Phi_{CTRL} - \Phi_{REF})}{2 \cdot \pi} = \frac{V_O}{V_{IN}}$$

Time-based PID Controller



$$H^T{}_{PID}(s) = K_{VCDL} + K_{VCO}\frac{1}{s} + K_{VCDL}R_DC_Ds$$

$$K^T{}_P = K_{VCDL_1} \qquad K^V{}_P = G \cdot \left(1 + \frac{\omega_{z1}}{\omega_{z2}}\right)$$

$$K^T{}_I = K_{VCO} \qquad K^V{}_I = G \cdot \omega_{z1}$$

$$K^T{}_D = K_{VCDL_2}R_DC_D \qquad K^V{}_D = \frac{G}{\omega_{z2}}$$

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2017 Time-Based Circuit Presentations at ISSC, CICC

Not including 43 papers with timing applications (PLL, DLL, oscillators, etc.)

ISSCC

T5: Fundamentals of Time-Based Circuits
T8: Fundamentals of Class-D Amplifier Design
F6: Quantizing Time: Time-to-Digital Converters
5.1: A 5x80W 0.004% THD+N Automotive Multiphase Class-D Audio Amplifier with Integrated Low-Latency SD ADCs for Digitized Feedback
5.2: An 8ohm 10W 91% Power-Efficiency 0.0023% THD+N Multi-Level Class-D Audio Amplifier with Folded PWM
5.10: A 1A LDO Regulator Driven by a 0.0013mm2 Class-D Controller
9.2: A 0.6nJ -0.22/+0.19C Inaccuracy Temperature Sensor Using Exponential Subthreshold Oscillation Dependence
13.6: A 2.4GHz WLAN Digital Polar Transmitter with Synthesized Digital-to-Time Conv. in 14nm Trigate/FinFET Tech. for IoT and Wearable Applications
15.1: Large-Scale Acquisition of Large-Area Sensors Using an Array of Frequency-Hopping ZnO Thin-Film-Transistor Oscillators
15.6: A 30-to-80MHz Simultaneous Dual-Mode Heterodyne Oscillator Targeting NEMS Array Gravimetric Sensing Applications with a 300zg Mass Resolution
16.5: 5 An 8GS/s Time-Interleaved SAR ADC with Unresolved Decision Detection Achieving -58dBFS Noise and 4GHz Bandwidth in 28nm CMOS
28.2: An 11.4mW 80.4dB-SNDR 15MHz-BW CT Delta-Sigma Modulator Using 6b Double-Noise-Shaped Quantizer
28.3: A 125MHz-BW 71.9dB-SNDR VCO-Based CT ΔΣ ADC with Segmented Phase-Domain ELD Compensation in 16nm CMOS

CICC

2.2: Channel Adaptive ADC and TDC for 28Gb/s 4pj/bit PAM-4 Digital Receiver
5.4: A 256kb 6T Self-Tuning SRAM with Extended 0.38V-1.2V Operating Range using Multiple Read/Write Assists and VMIN Tracking Canary Sensors
7.1: A 6-bit 0.81mW 700-MS/s SAR ADC with Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration
7.7: A 73dB SNDR 20MS/s 1.28mW SAR-TDC Using Hybrid Two-Step Quantization
12.4: A Time-based Inductor for Fully Integrated Low Bandwidth Filter Applications
16.2: A 10MHz 2mA-800mA 0.5V-1.5V 90% Peak Efficiency Time-Based Buck Converter with Seamless Transition between PWM/PFM Modes
17.2: A Scalable Time-based Integrate-and-Fire Neuromorphic Core with Brain-inspired Leak and Local Lateral Inhibition Capabilities
21.3: Design of Tunable Digital Delay Cells
22.3: A 50 MHz BW 73.5 dB SNDR Two-stage Continuous-time ΔΣ Modulator with VCO Quantizer Nonlinearity Cancellation
25.3: Digitally Controlled Voltage Regulator Using Oscillator-based ADC with fast-transient-response and wide dropout range in 14nm CMOS
26.3: Time-Based Circuits for High-Performance ADC
26.4: Time-based encoders and digital signal processors in continuous time

Summary

Time-Based Signals are Everywhere

- Timing circuits
- Sensors
- Pulse-Width Modulation

Alternative to V&I Circuits

- CMOS friendly
- Small
- Simple

Unique Time-based Circuit Attributes

- Ideal integration with infinite DC gain
- Simple, high-speed quantization
- Natural fit with oversampled systems

Potential for Innovation

- Some analog functions can potentially be implemented smaller or in a simpler way
- Many new ideas for time-based circuits

Suggested References

- V. Ramakrishnan, P.T. Balsara, “A wide-range, high-resolution, compact, CMOS time to digital converter” Proc. IEEE International Conference on VLSI Design. (Vol. 2006, pp. 197-202).
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