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March 22, 2012

The Evolution of Oversampling Analog-to-Digital Converters

Bruce A. Wooley

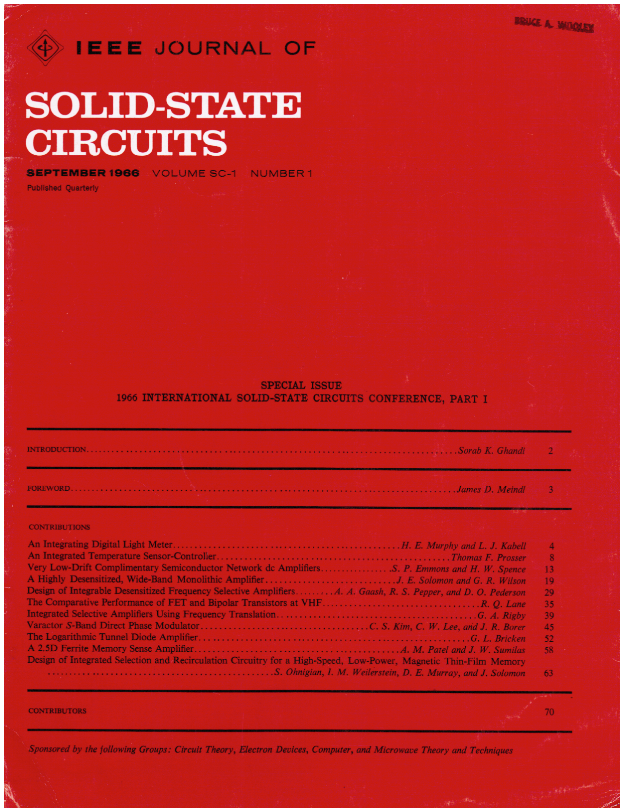
Stanford University

Solid-State Circuits Council

- Established in May 1966, the Council preceded the Solid-State Circuits Society
- Founded to sponsor the Journal of Solid-State Circuits (**JSSC**) and the International Solid-State Circuits Conference (**ISSCC**)
  - ISSCC was first held in 1954, sponsored by the Philadelphia Section of the IRE and the University of Pennsylvania
  - But prior to the formation of the Council, there was no archival record dedicated to electronic circuit design

Solid-State Circuits Council

- Initially sponsored by four IEEE Societies: Circuit Theory, Computer, Electron Devices, Microwave Theory & Techniques (later added COM, CHMT and LEOS)
- First issue of the JSSC was published in September 1966.



BRUCE A. WOOLEY

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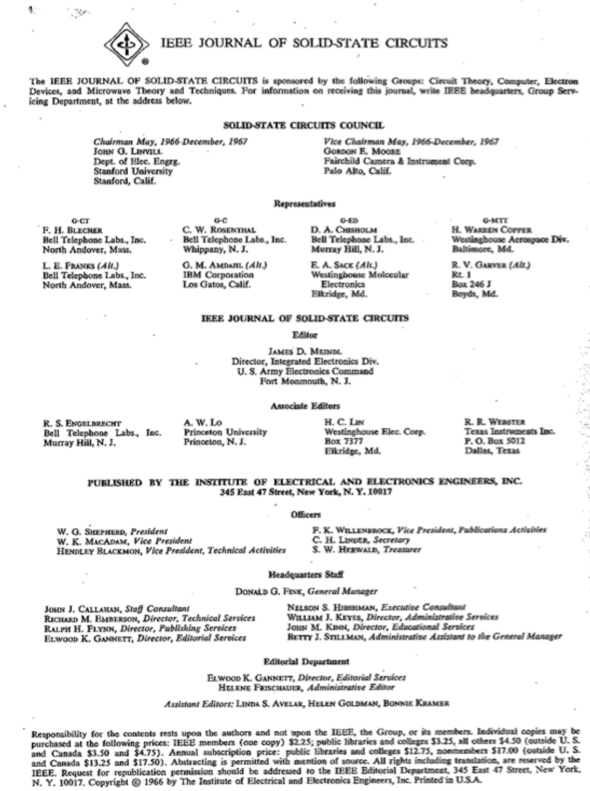

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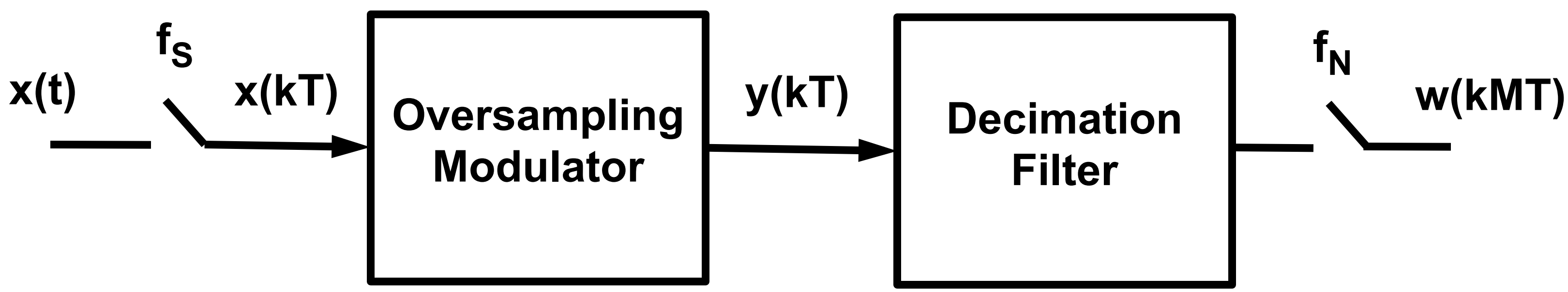
IEEE Solid-State Circuits Society

- Established January 1, 1997
- **Santa Clara Valley Chapter**
  - Jonathan David was instrumental in forming the chapter and served as it's first chair
  - First meeting was held in March 1997
    - Speaker was Ken Kundert
    - But not yet enough signatures to formally establish the chapter
  - Second meeting April 1998
    - Speaker was Tom Lee
  - Chapter was officially established on May 6, 1997
    - One of the first **two** SSCS chapters; the other was Yugoslavia
- Now 75 chapters worldwide
  - SCV is the largest (>2,000 members out of ~10,000 Society members)

Oversampling A/D Conversion

Basic concept:

Exchange resolution in **time** for that in **amplitude** through the use of **oversampling**, **feedback** and **digital filtering**



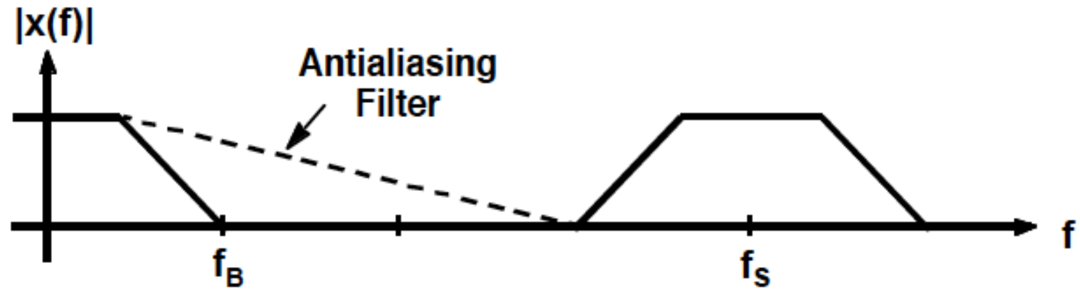
f_S = 1/T = sampling rate

f_N = 1/MT = Nyquist rate

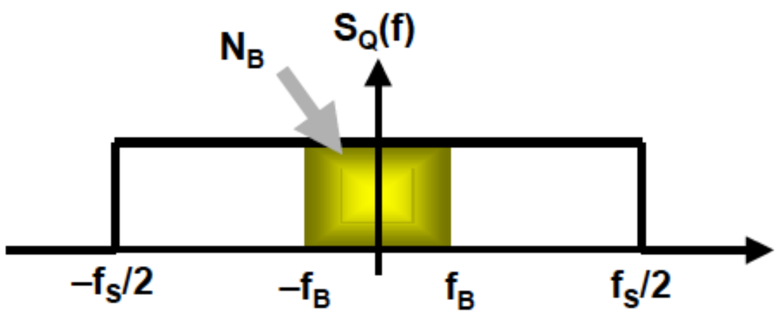
M = oversampling ratio

Oversampling

- Increasing the sampling rate (f_S) of an A/D converter relaxes the **antialiasing** filter requirements



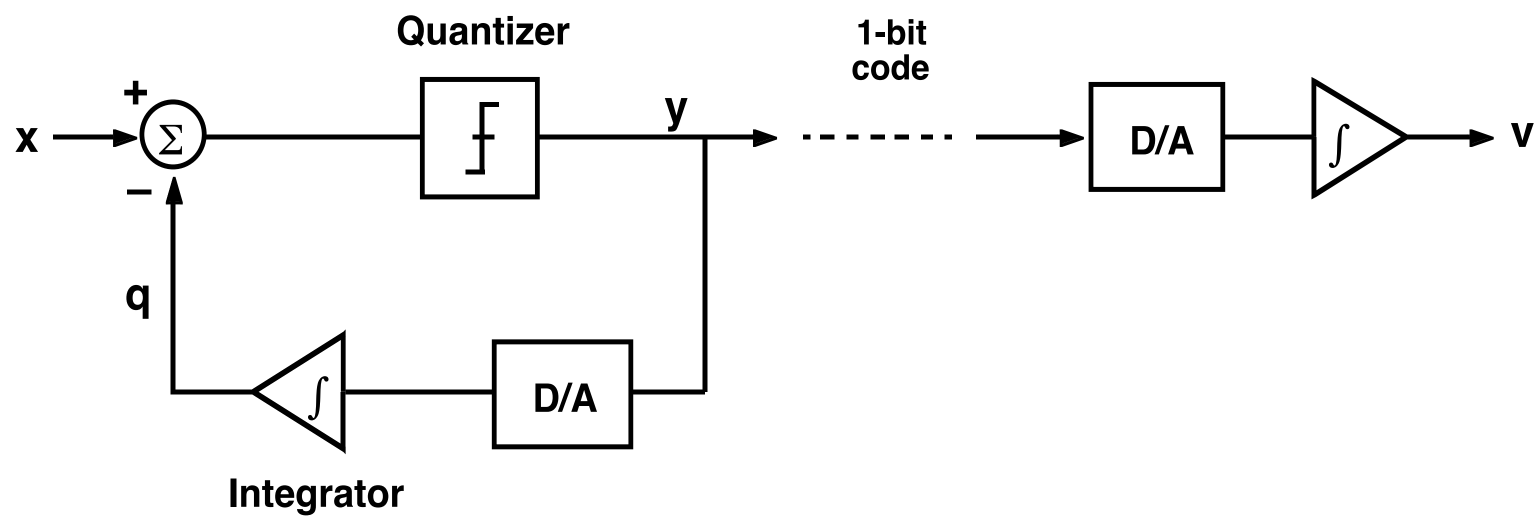
- Increasing f_S also reduces the in-band quantization noise (N_B); but only gain 3 dB in resolution per octave increase



- Can combine **feedback** with **oversampling** to improve the resolution gained by oversampling

In the Beginning

- Combining **feedback** with **oversampling** to achieve an increase in resolution began with **delta modulation**

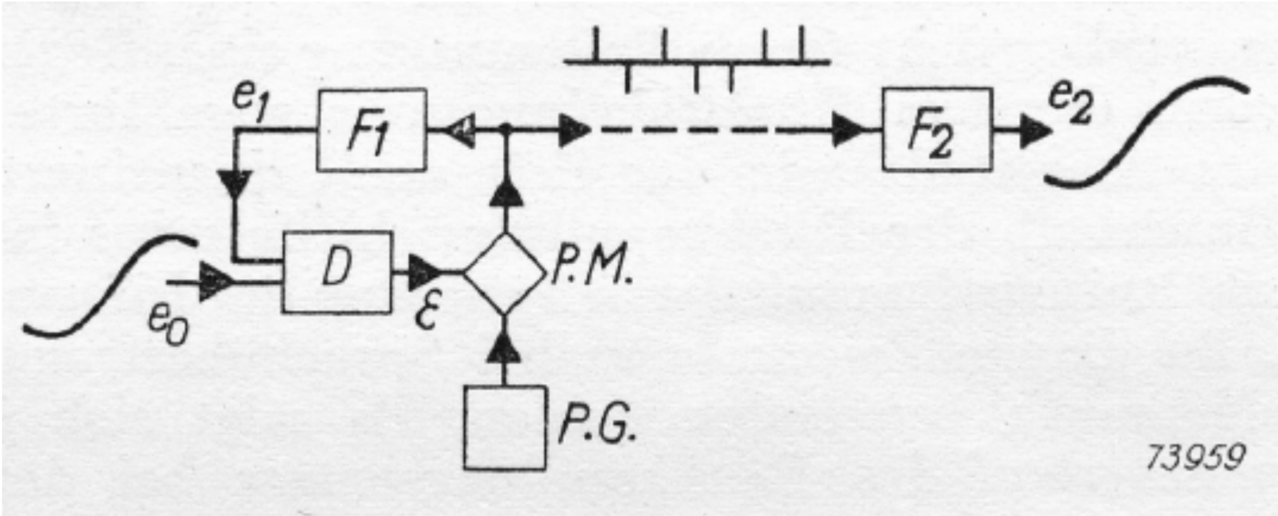


- Driven by telecom applications – the digital encoding of voice signals
- A delta modulator encodes the **rate of change** of its input signal; typically use a 1-bit quantizer with small step size

Delta Modulation

Seminal paper (from Philips Research):

F. de Jager, "Delta Modulation: A Method of PCM Transmission Using the One Unit Code," *Philips Research Reports,* vol. 7, 1952.

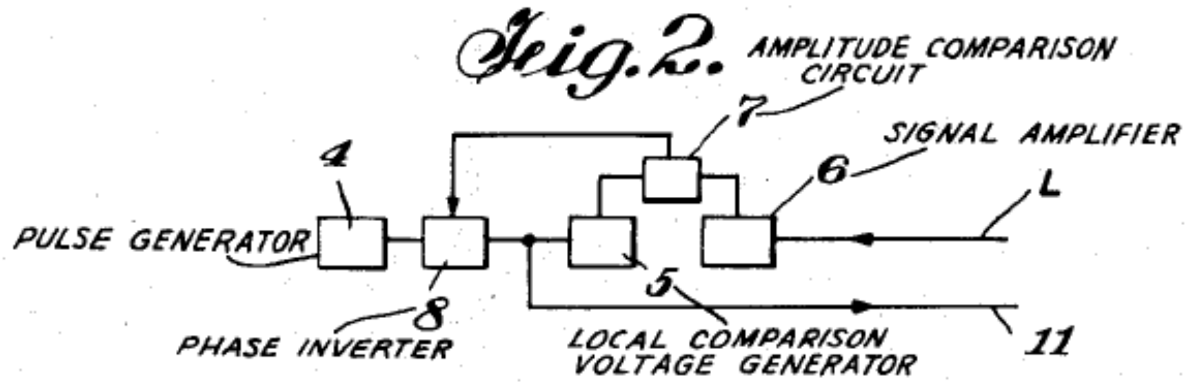


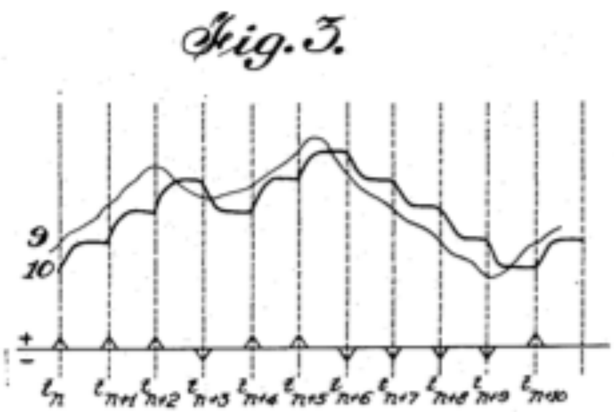
Envisioned applications included:

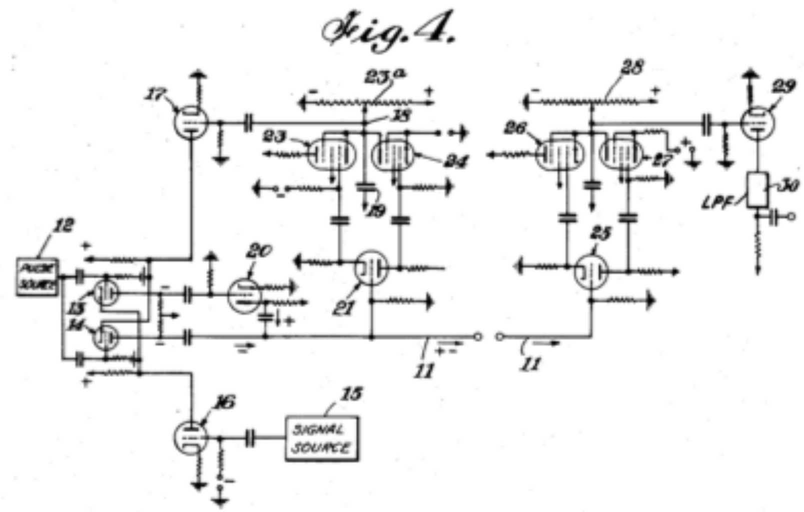
- Per-channel encoding of analog signals for digital switching and transmission in voiceband telephone systems
- Speech coding

Initial Delta Modulation Patents – Deloraine

- E. M. Deloraine, et al., “Communication System Utilizing Constant Amplitude Pulses of Opposite Polarities” (French patent issued in 1946, U.S. patent filed in 1947).

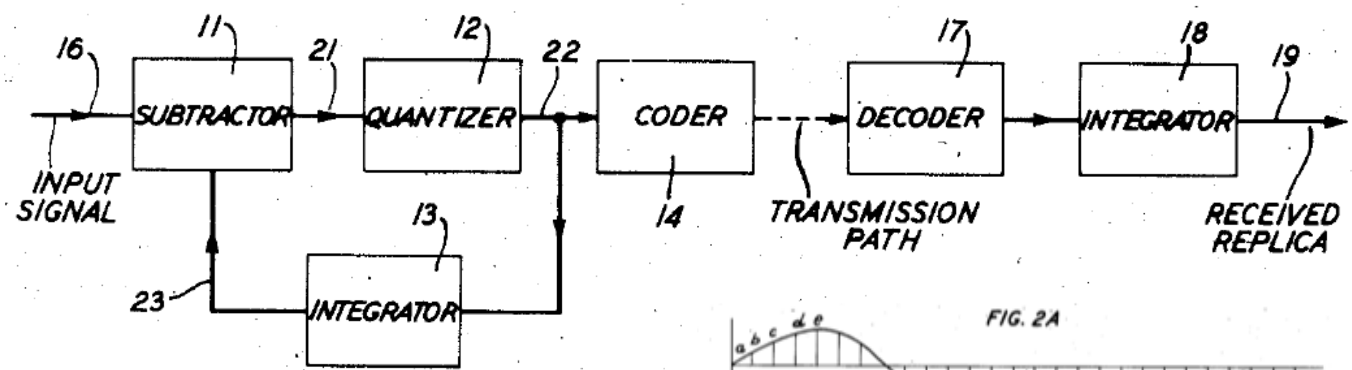


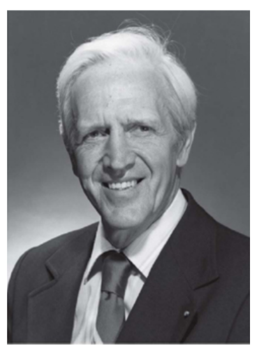


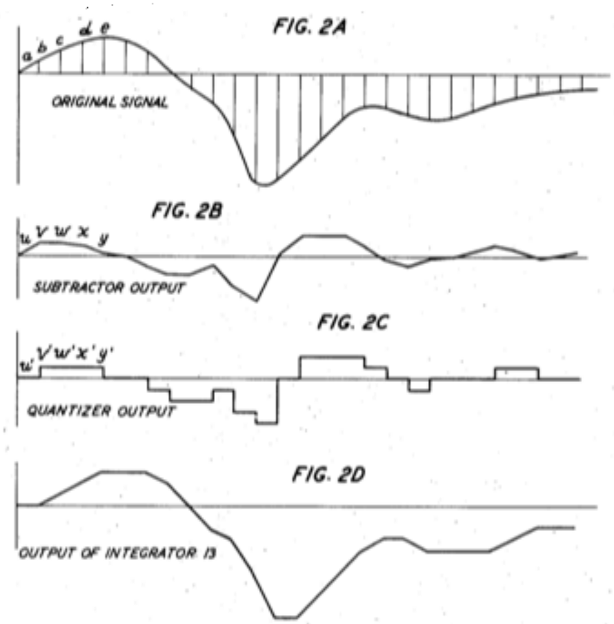


Initial Delta Modulation Patents - Cutler

- C. C. Cutler, "Differential Quantization of Communication Signals," *U.S. Patent 2,605,361* (filed June 29, 1950, issued July 29, 1952).
  - Describes differential PCM & **delta-modulation** (1-bit DPCM)



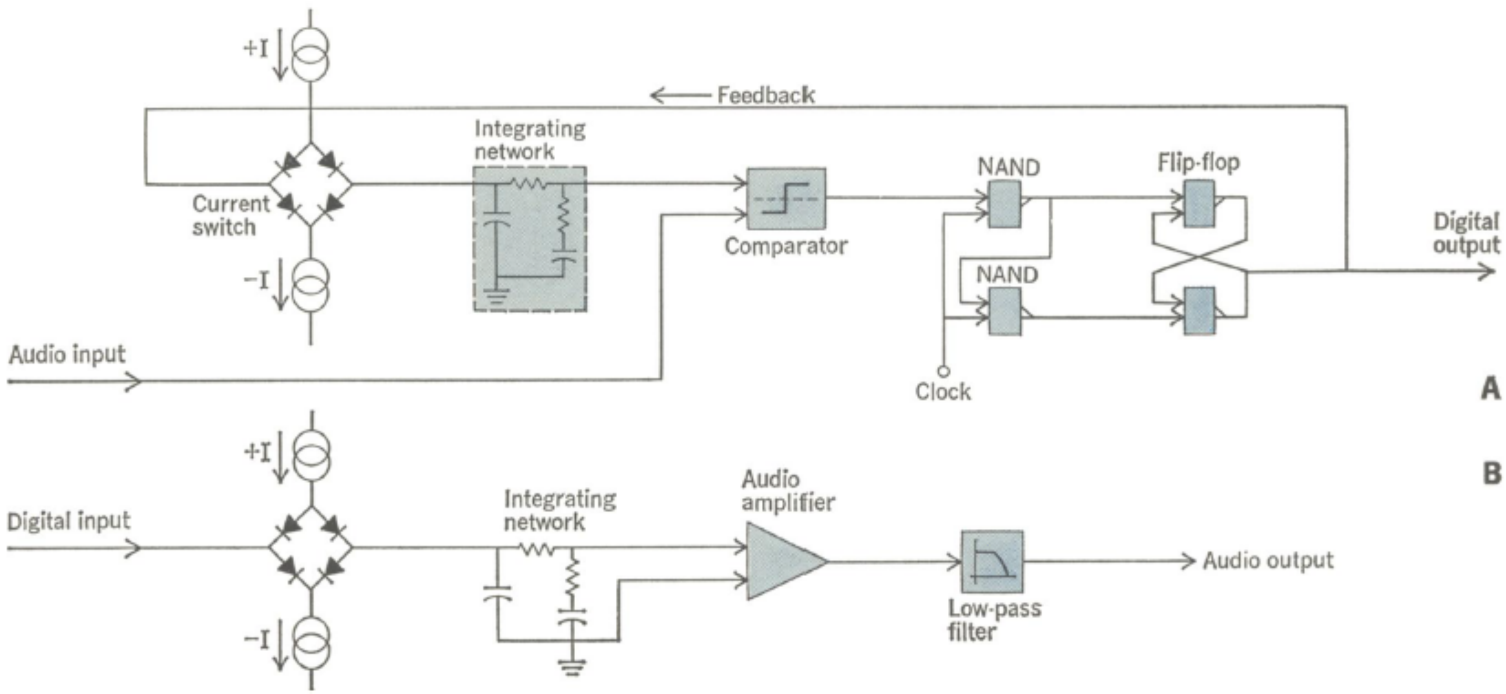




An “Early” Δ Modulator Circuit

- H. R. Schindler, “Delta Modulation,” *IEEE Spectrum,* Oct. 1970.

FIGURE 4. A—Circuitry for the basic delta-modulation encoder. B—Circuitry for the decoder.



Δ Modulation in Digital Switching

- H. S. McDonald, "Pulse Code Modulation and Differential Pulse Code Modulation Encoders" *U.S. Patent 3,526,855* (filed Mar. 18, 1968, issued Sept. 1, 1970).

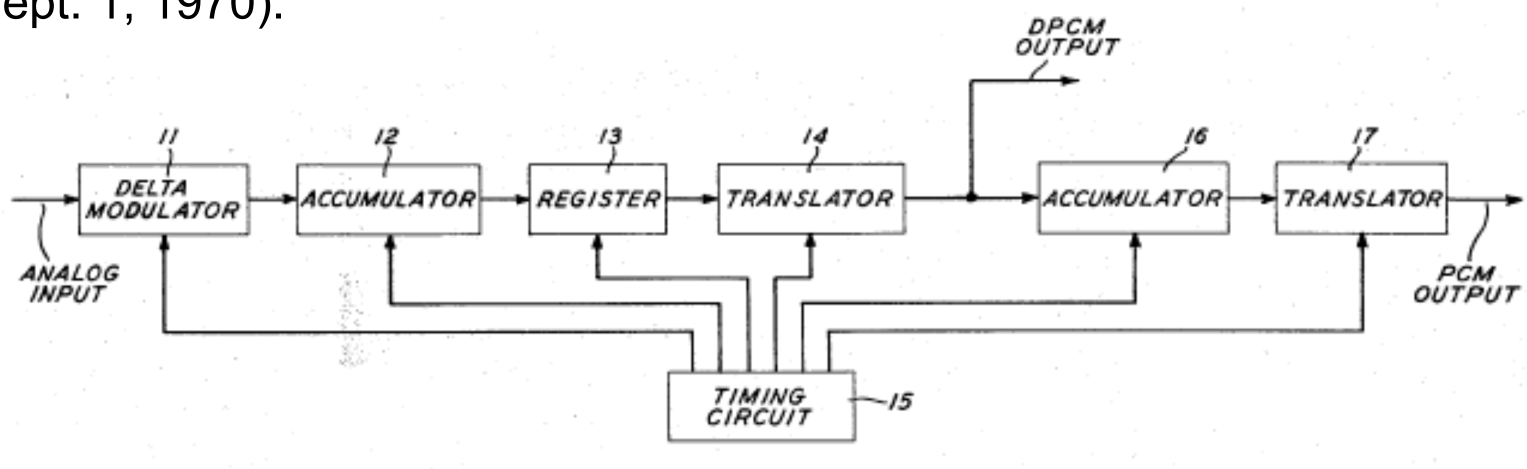
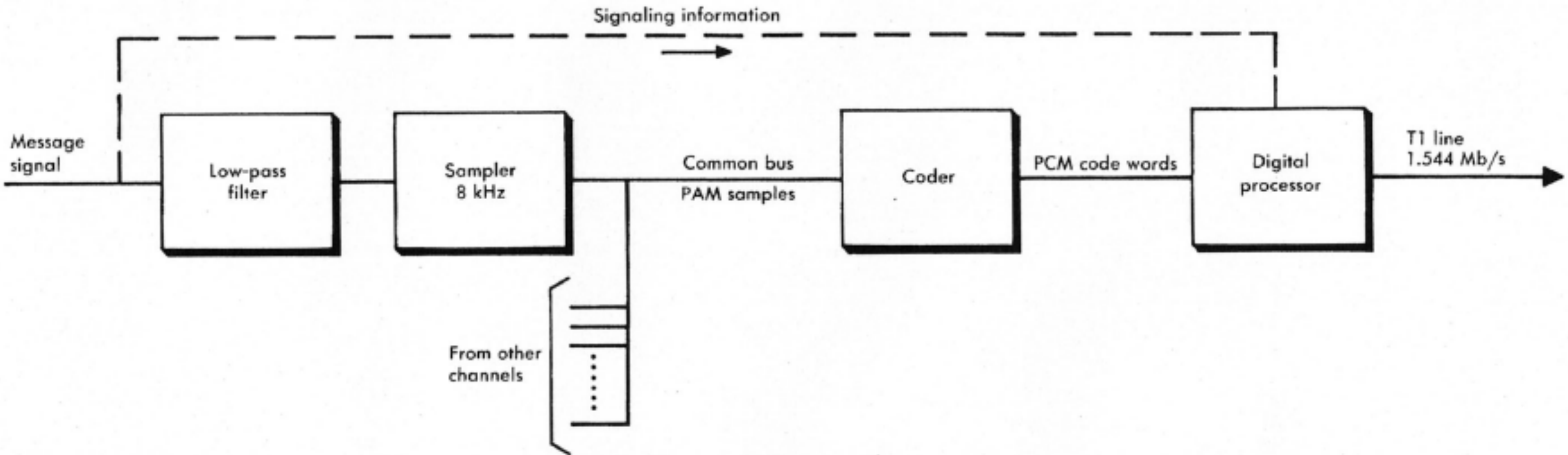


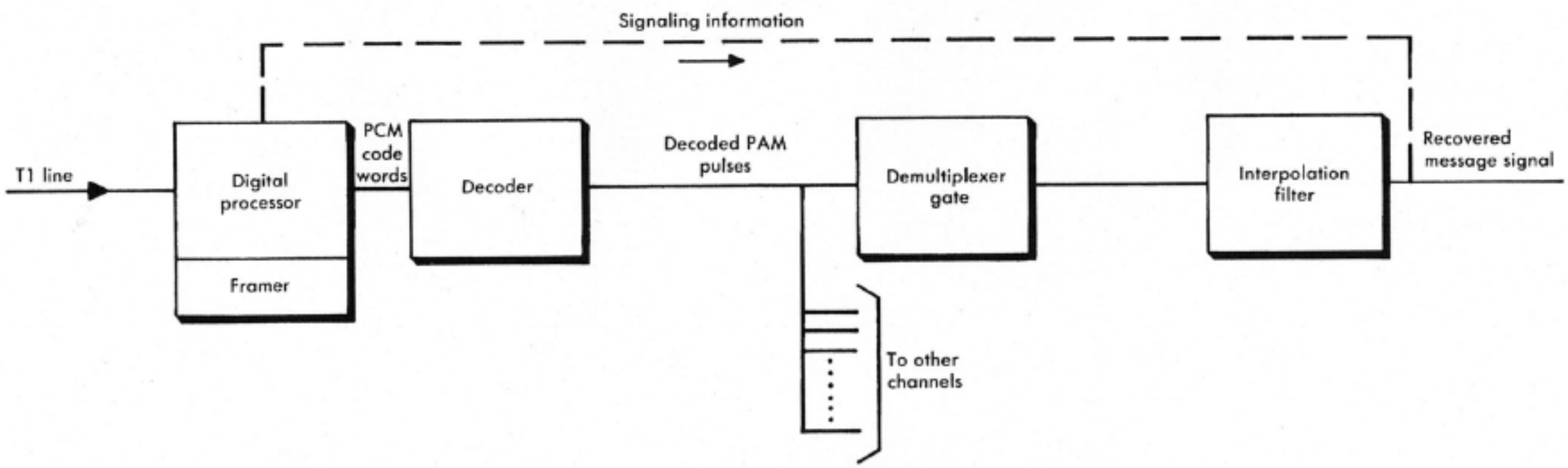
FIG. 1

- An early application of delta modulation to voice encoding for digital electronic switching in telephony
- Motivation, for both switching and transmission, was to enable the **per-channel encoding** of voice signals, in order to eliminate PAM busses

Digital Channel Bank

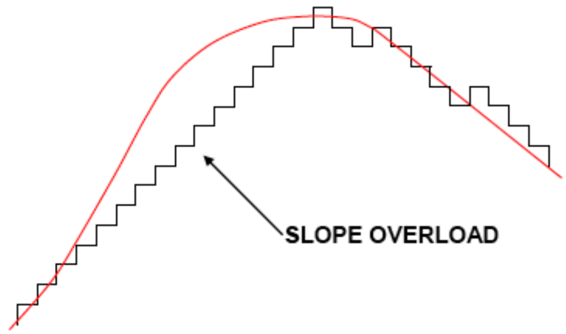


(a) Transmitting portion

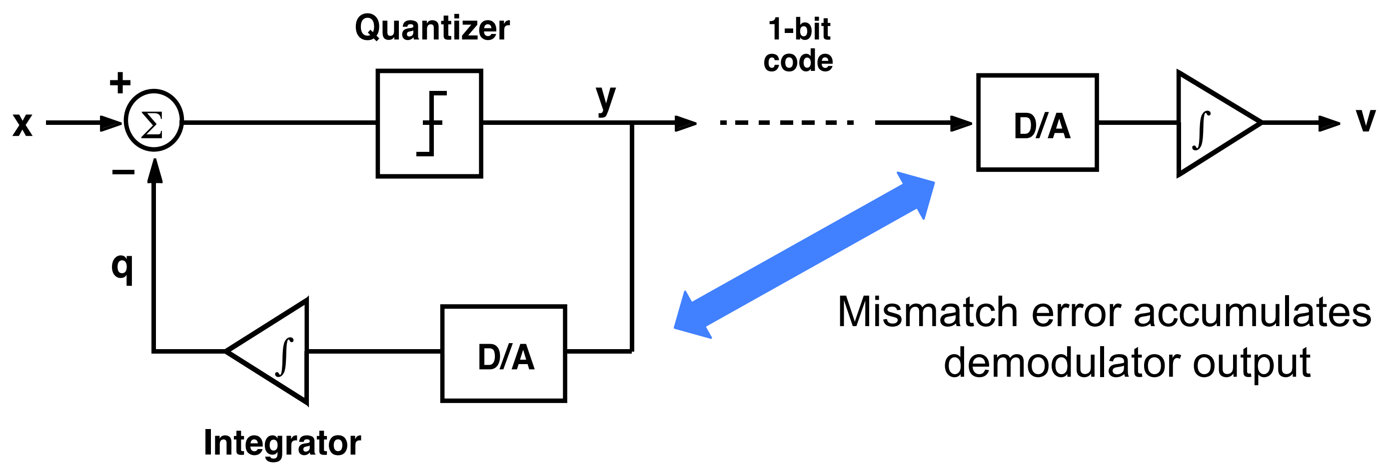


Δ Modulation Challenges

- Slope overload



- DAC mismatch between modulator and demodulator



- Spurious pattern noise ("Iwersen noise")

An Alternative – Noise Shaping

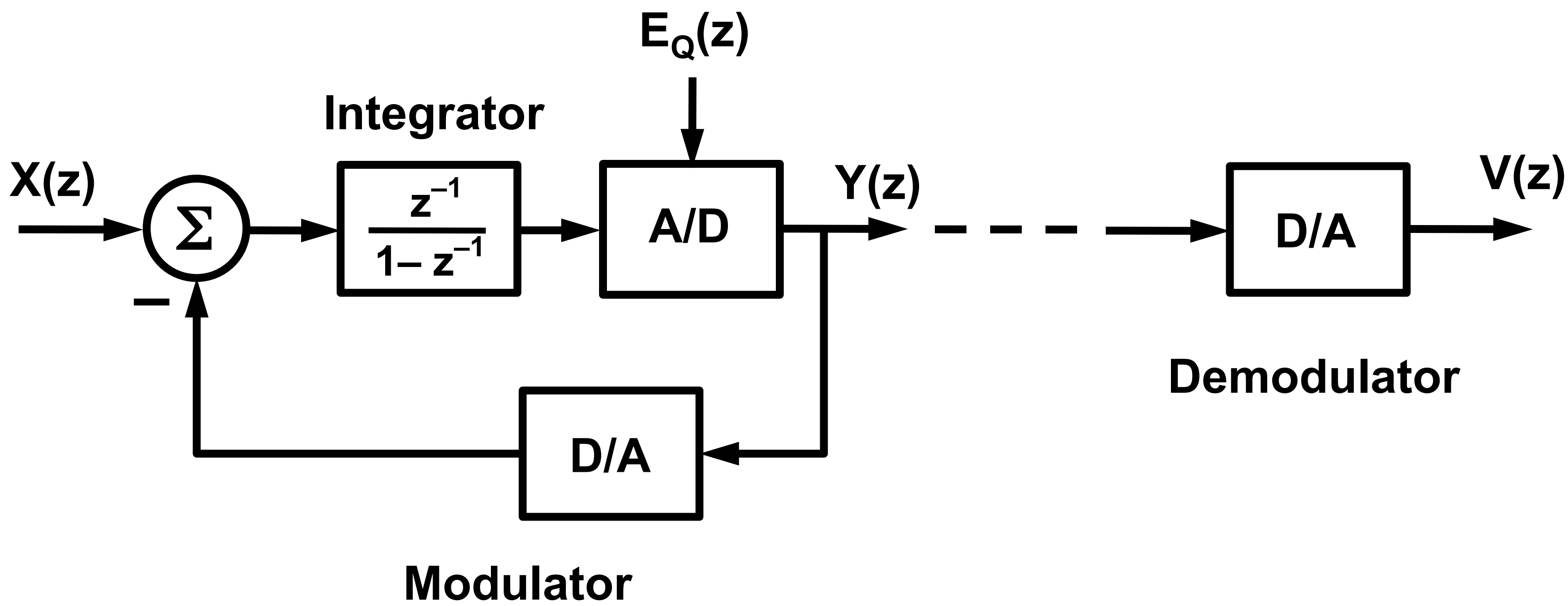
- In delta modulators feedback is combined with oversampling for **prediction**
- But feedback can also be used for **noise shaping** via **sigma-delta** (= delta-sigma) modulation
- Noise shaping modulators are more robust and easier to implement than predictive modulators

Seminal papers (from Univ. of Tokyo):

H. Inose, Y. Yasuda and J. Murakami, "A Telemetering System by Code Modulation – **Δ-Σ Modulation**," *IRE Trans. Space Electronics and Telemetry,* Sept. 1962.

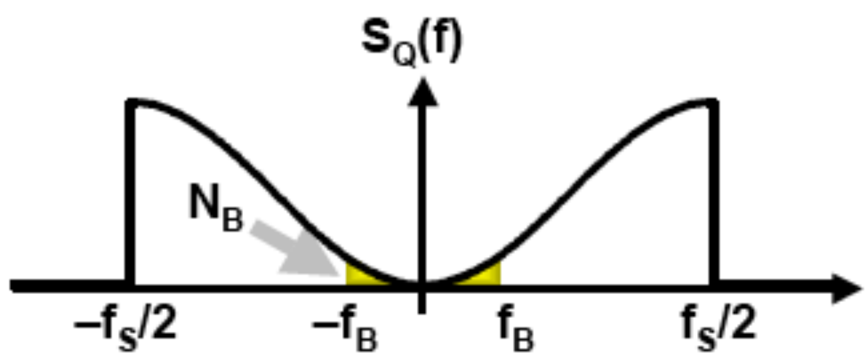
H. Inose and Y. Yasuda, "A Unity Bit Coding Method by Negative Feedback," *IEEE Proceedings,* Nov. 1963.

Sigma-Delta (or Delta-Sigma) Modulation

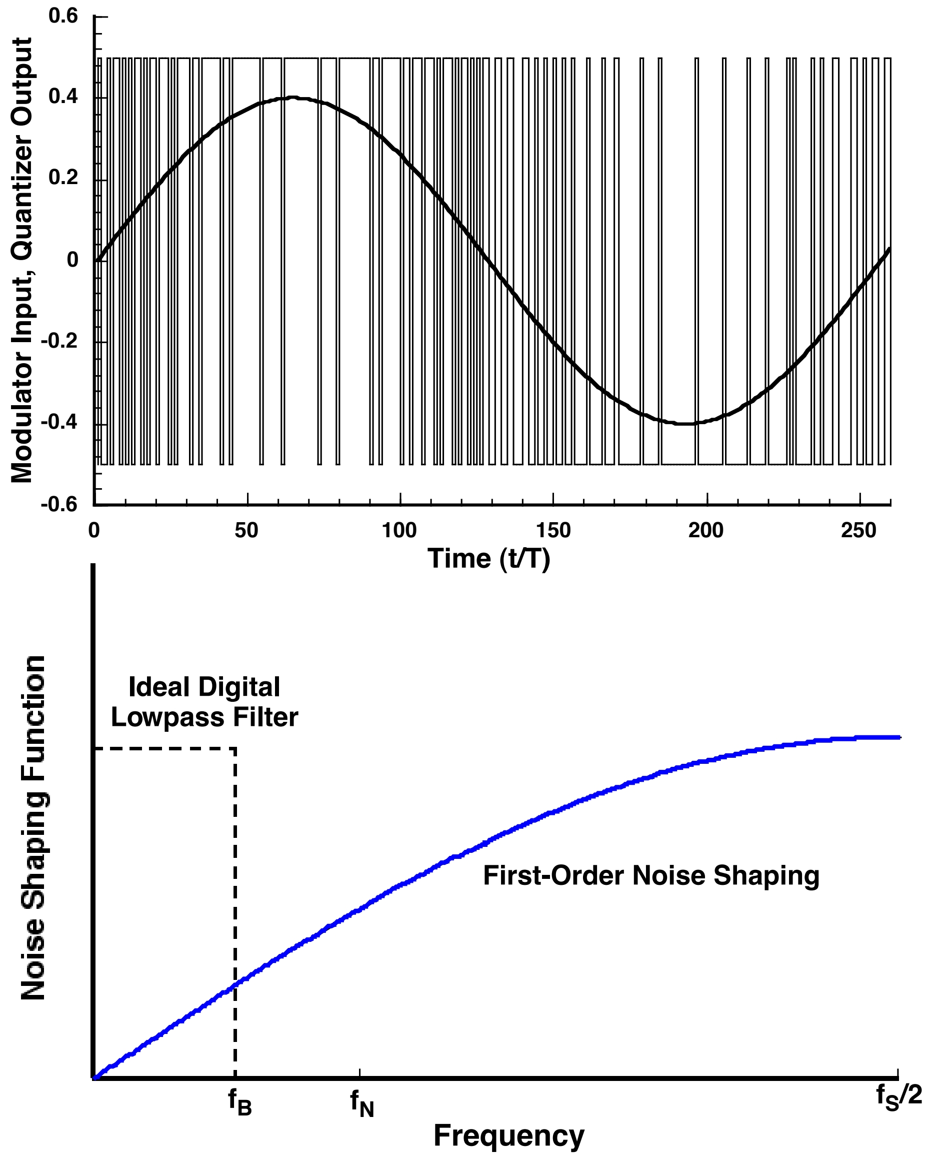


$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E_Q(z)$$

$$N_E(f) = \left[2\sin\left(\pi f / f_S\right)\right]^2 N_Q(f)$$



ΣΔ Modulator Response

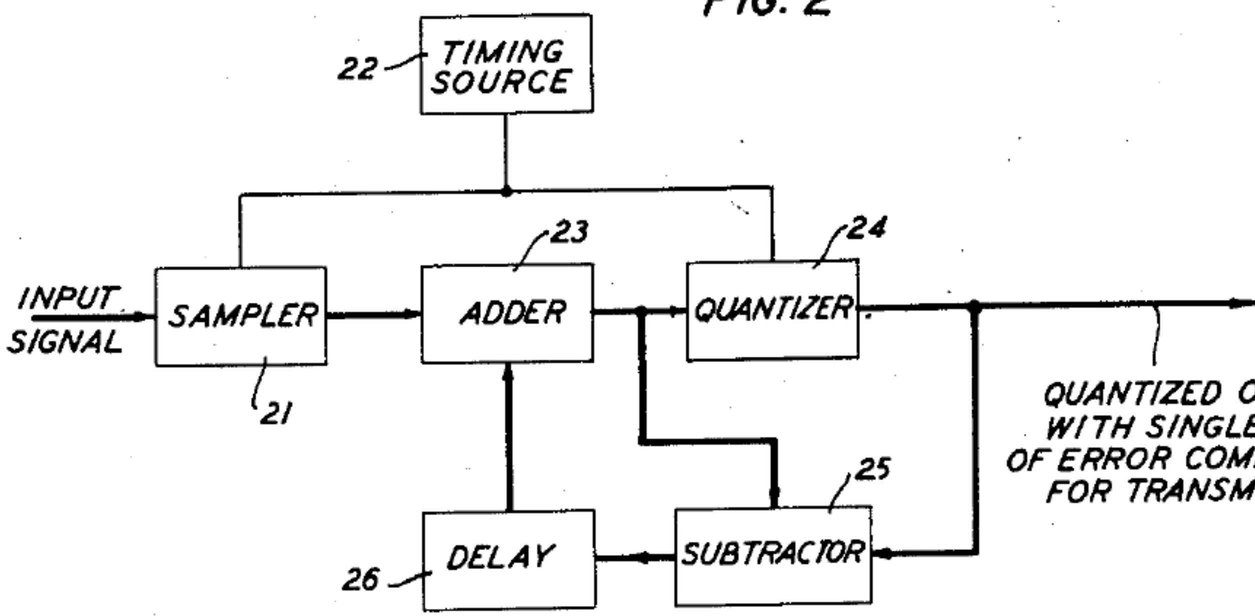


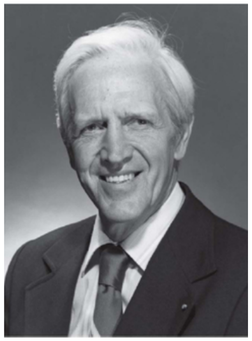
Initial Patent on Noise Shaping Modulators

Using oversampling and feedback to shape the spectrum of quantization noise first appeared as an **error feedback** oversampling modulator:

C. Cutler, "Transmission Systems Employing Quantization," *U.S. Patent 2,927,962* (filed Apr. 26, 1954, issued Mar. 8, 1960).

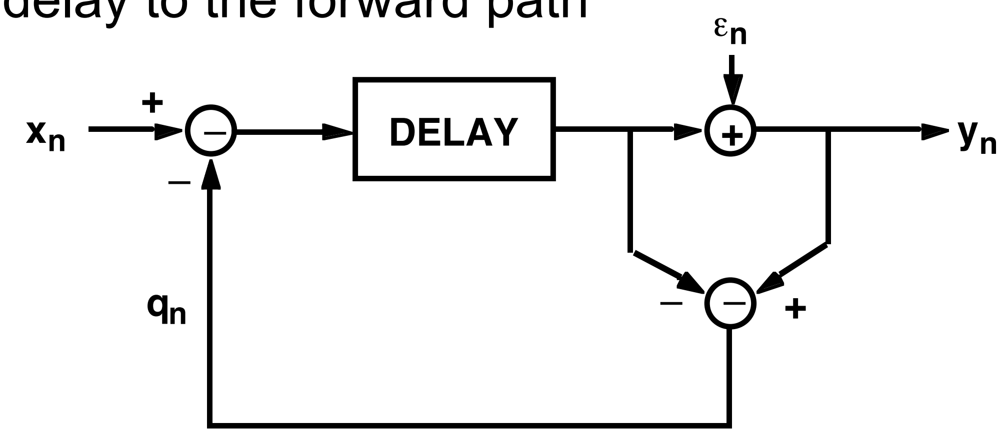
FIG. 2



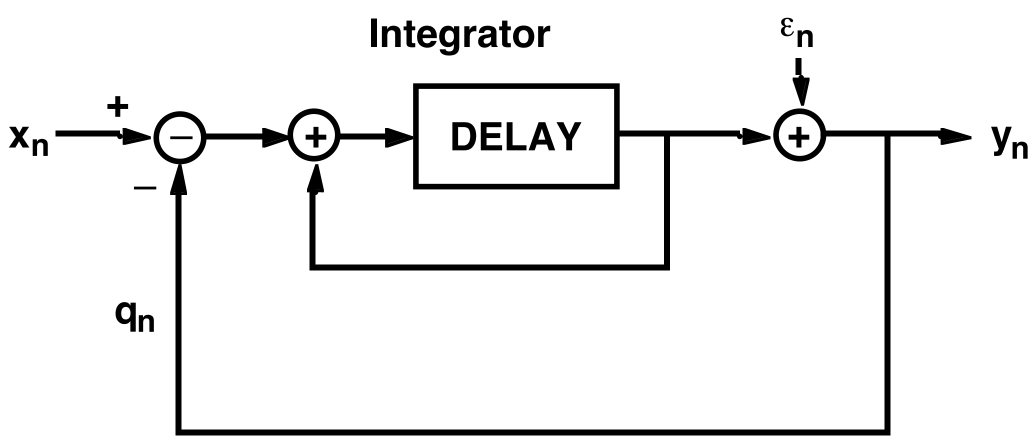


Error Feedback ⇨ ΣΔ Modulation

- Move the delay to the forward path



- Separate feedback from input and output of quantizer



Limits of 1st-order ΣΔ Modulation

- Ideally a 9dB/octave increase in dynamic range with an increase in oversampling ratio (f_S/f_N)
- Improvement much less than ideal owing to pattern noise (**"Iwersen" noise**), i.e., spurious tones that result from correlation between the quantization error and the input

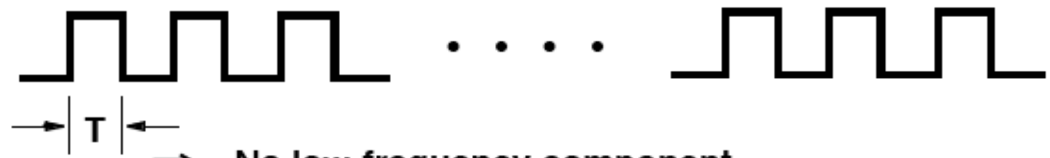
  J. E. Iwersen, "Calculated Quantizing Noise of Single-Integration Delta-Modulation coders," *Bell Syst. Tech. J.*, Sept. 1969.

- Alternative oversampling approaches:
  – Multi-level quantization
  – Modulators based on **interpolation**
  – Higher order modulators
    • Single quantizer with multiple loops or single loop with multi-order filtering
    • Cascaded (multi-stage) ΣΔ modulators (MASH)

“Iwerson” Noise in ΣΔ Modulators

$x(kT) = 0$ (midrange input; full scale = $\pm \Delta/2$)

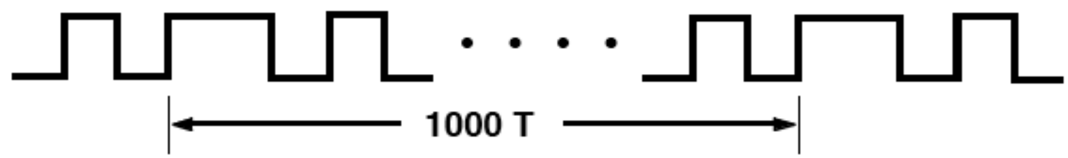
y(kT):



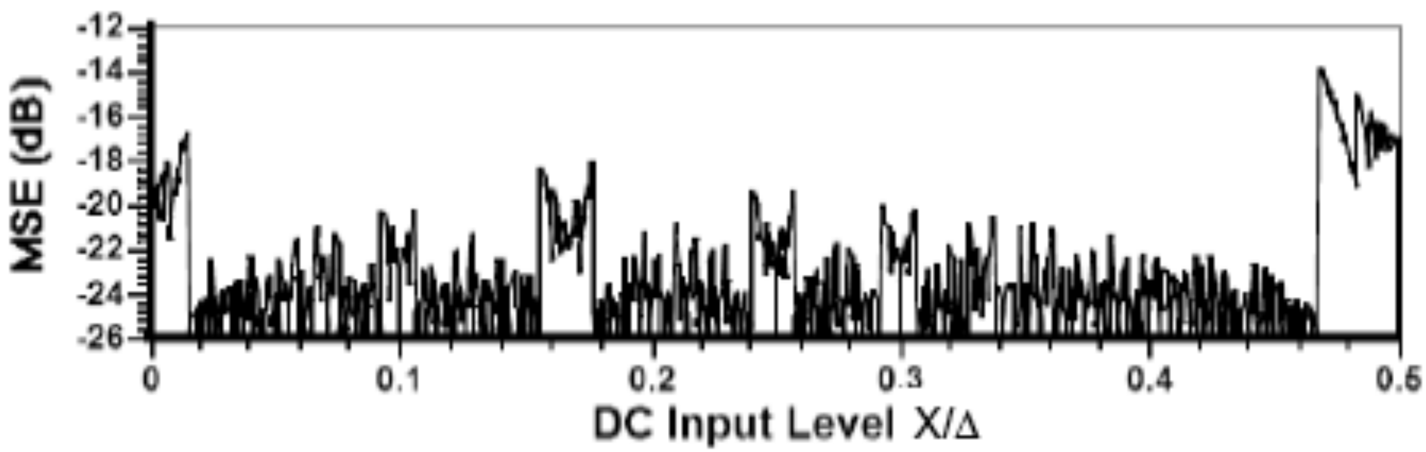
⇒ No low-frequency component

$x(kT) = (0.001)\Delta/2$

y(kT):



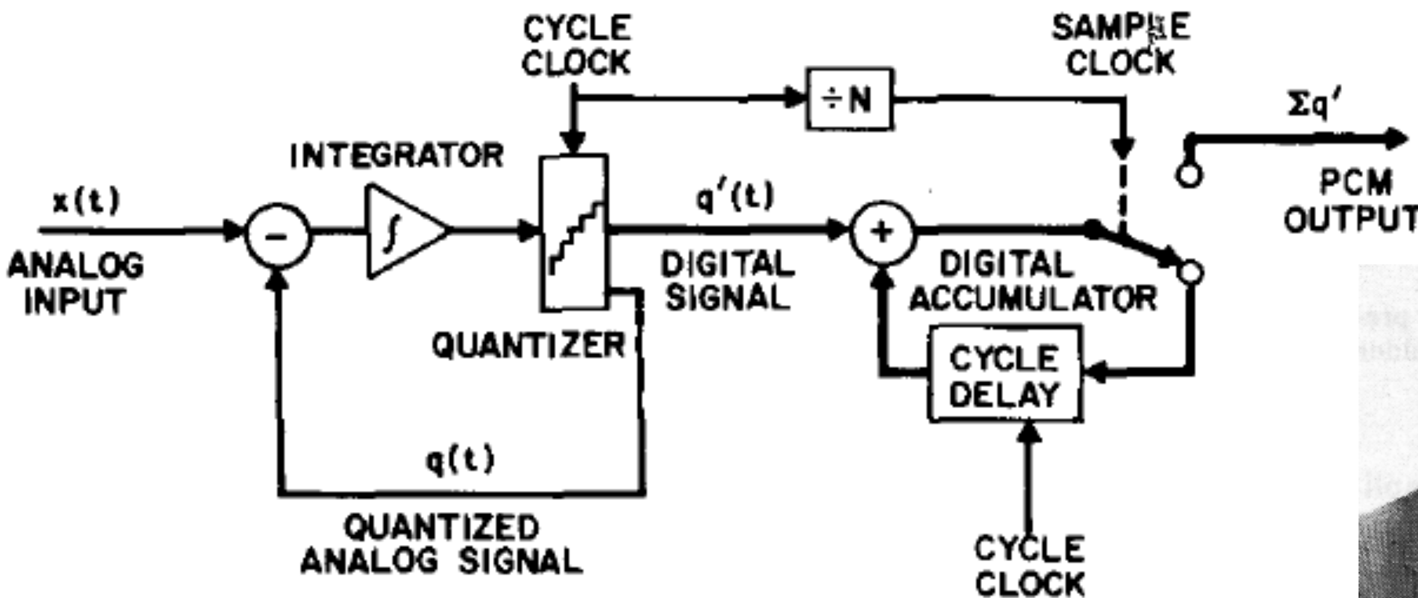
⇒ Frequency component in baseband



Multi-level ΣΔ Modulation for PCM

Jim Candy introduced a circuit for generating PCM using a ΣΔ modulator with <u>multi-level</u> quantization in the following classic paper:

> J. C. Candy, "A Use of Limit Cycle Oscillations to Obtain Robust Analog-to-Digital Converters," *IEEE Trans. Commun.*, Dec. 1974.



This circuit includes a simple accumulator for **decimation**

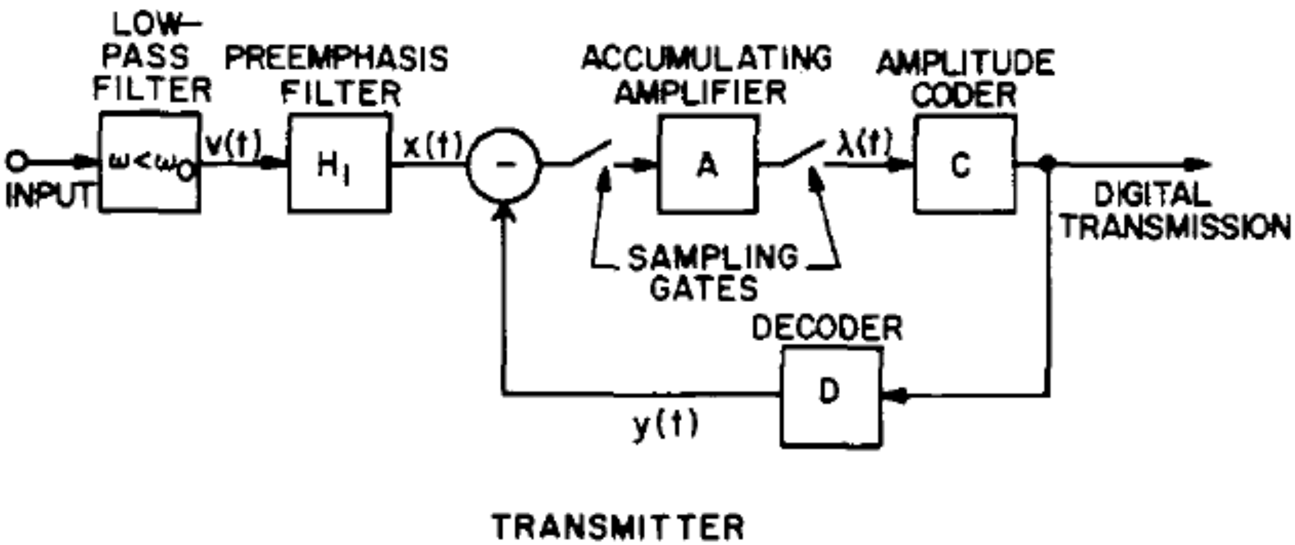
Decimation Filtering

- **Decimation** is the process of resampling a digitally encoded signal at a lower rate, typically the Nyquist rate
  - D. Goodman and M. Carey, "Digital Filters for Decimation and Interpolation," *IEEE Trans. ASSP,* Nov. 1963.
- At the output of a ΣΔ modulator, a digital decimation filter preceding resampling
  - suppresses out-of-band quantization noise that would be imaged into baseband by resampling
  - provides antialias filtering of out-of-band signals and noise
- Decimation, and interpolation, filters are now commonly implemented as FIR, rather than IIR, filters
  - but this was too "expensive" (= 7,000 gates) in the 1970's

An Earlier Noise-Shaping Coder for Video

Candy’s first work on noise shaping was also for encoding video :

R. C. Brainard and J. C. Candy, “Direct-Feedback Coders: Design and Performance with Television Signals,” *Proc. IEEE*, May 1969.



(a)

(b)

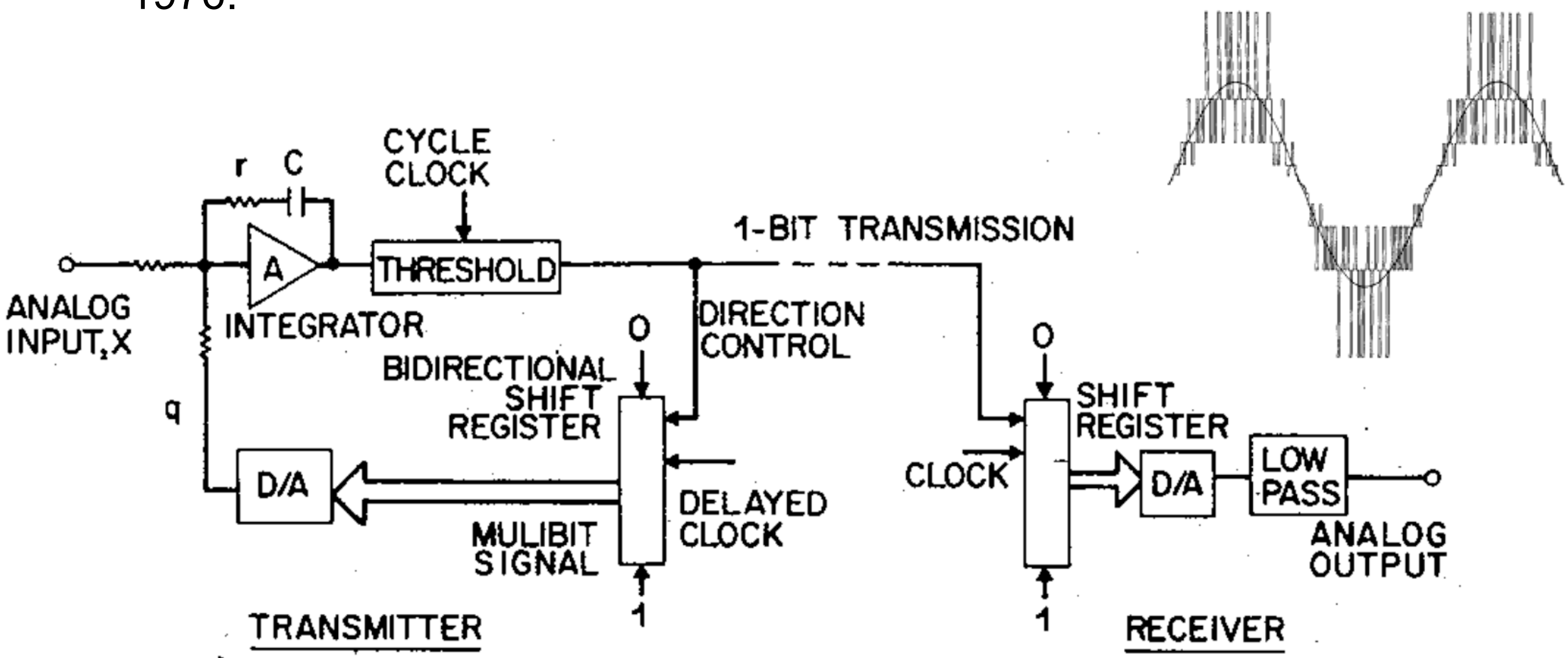
(c)

Fig. 11. Some coded television pictures; (a) original scene, (b) direct-feedback coding at 5 MHz, (c) delta coding at 5 MHz.

Interpolating Modulator

Candy next introduced the idea of an **interpolating modulator** for per-channel **companded** voiceband A/D conversion:

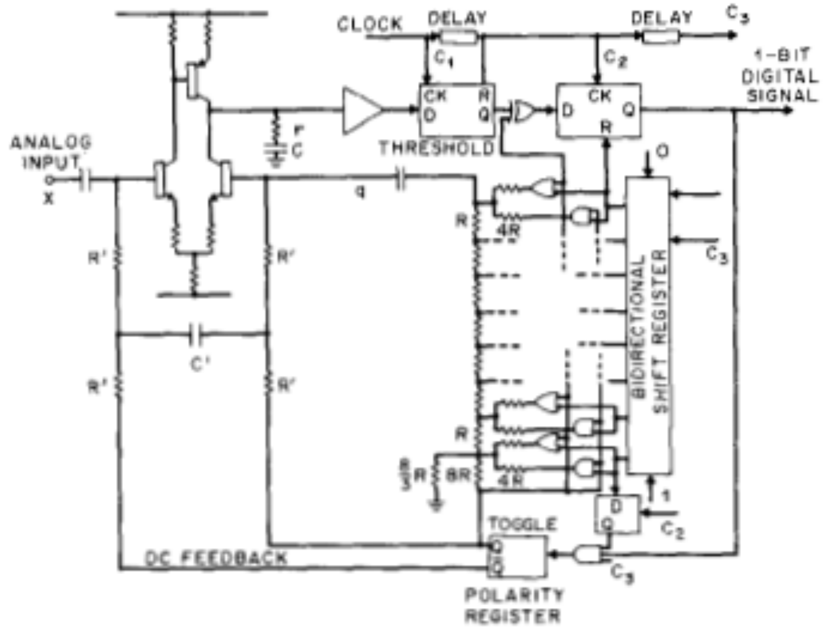
J. Candy, W. Ninke and B. Wooley, "A Per-Channel A/D Converter Having 15-Segment μ-255 Companding," *IEEE Trans. Commun.,* Jan. 1976.

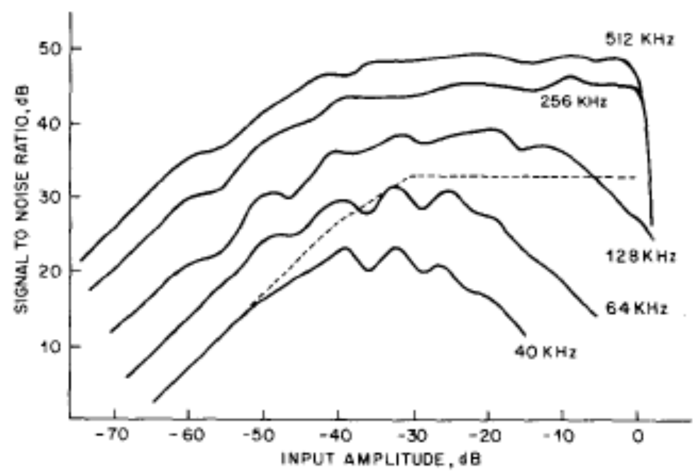


Testing an Interpolating Modulator

Digital Encoding for Local Telephone Service
Analog-to-digital and digital-to-analog converters are essential elements for connecting digital switches and digital transmission links with existing analog telephone equipment. In 1974 Bell Labs researchers developed new types of converters that generate a very simple code. This code may be useful for local transmission or switching, and can be easily converted to D3 format for connection with existing digital facilities. Indeed, the new coders and decoders may some day prove inexpensive enough to incorporate into a telephone set. Such a step would hasten growth toward an all-digital Bell System network, with its advantages of simple, reliable digital hardware replacing analog equipment.

Bell Labs' researchers Bruce Wooley (left) and Jim Candy in Holmdel study signal waveforms while exploring new digital encoding techniques.

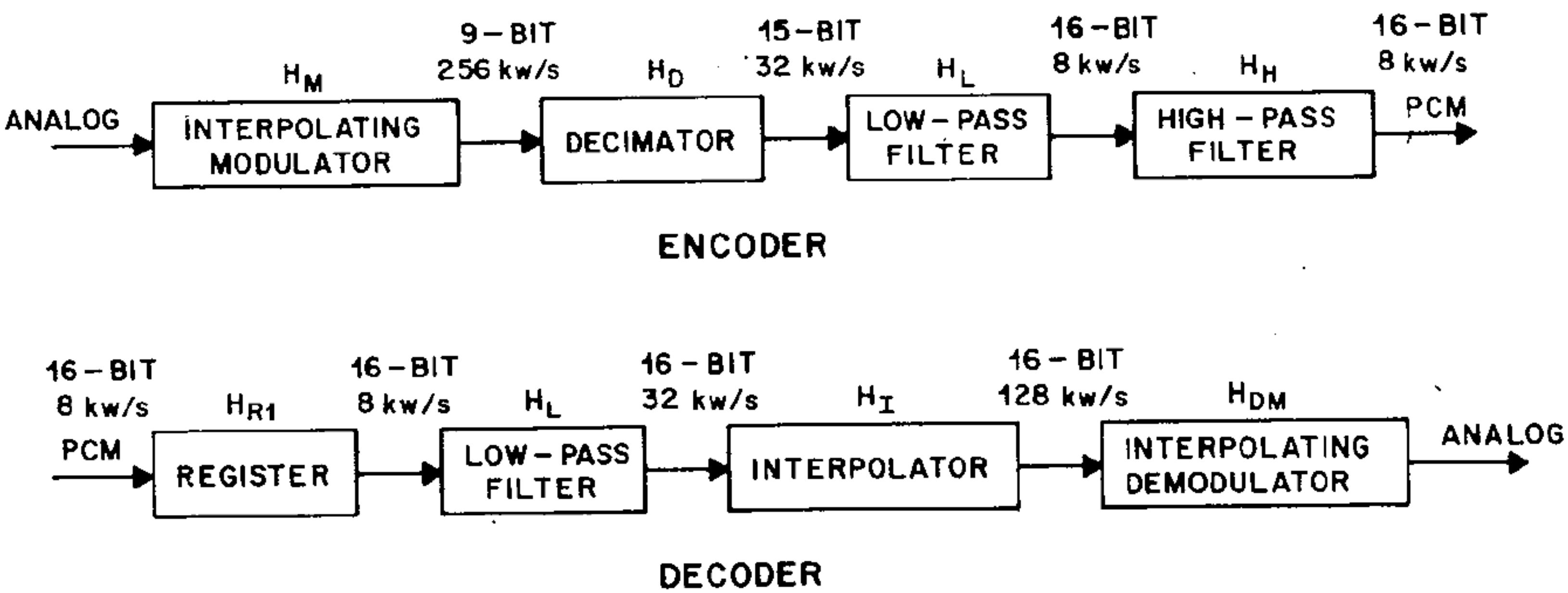




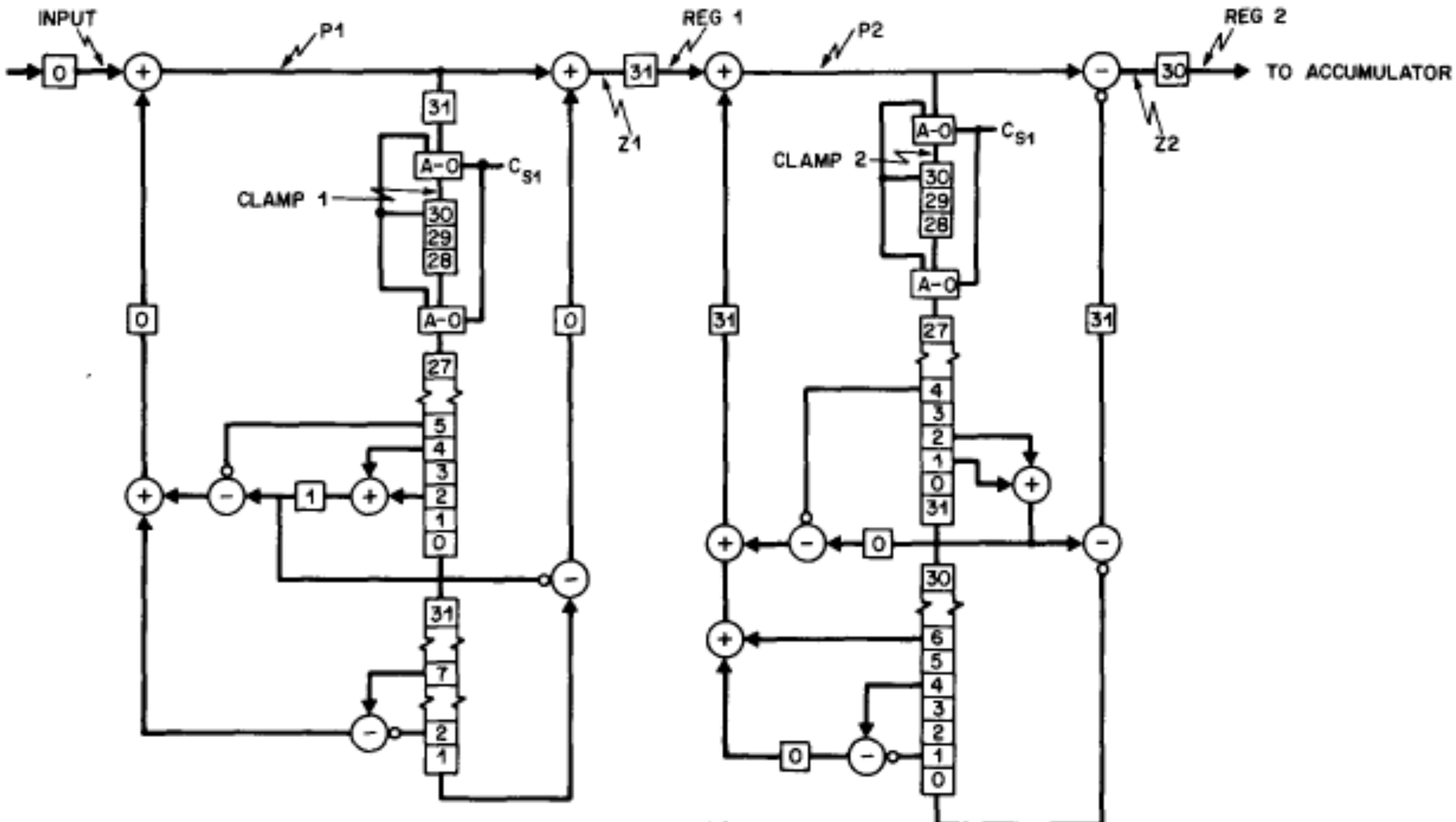
Voiceband Codec with Digital Filtering

Voiceband codec combined with decimation and interpolation filters:

J. Candy, B. Wooley and O. Benjamin, “A Voiceband Codec with Digital Filtering,” *IEEE Trans. Commun.,* June 1981.



Low-Pass Filter for Final 4x Decimation

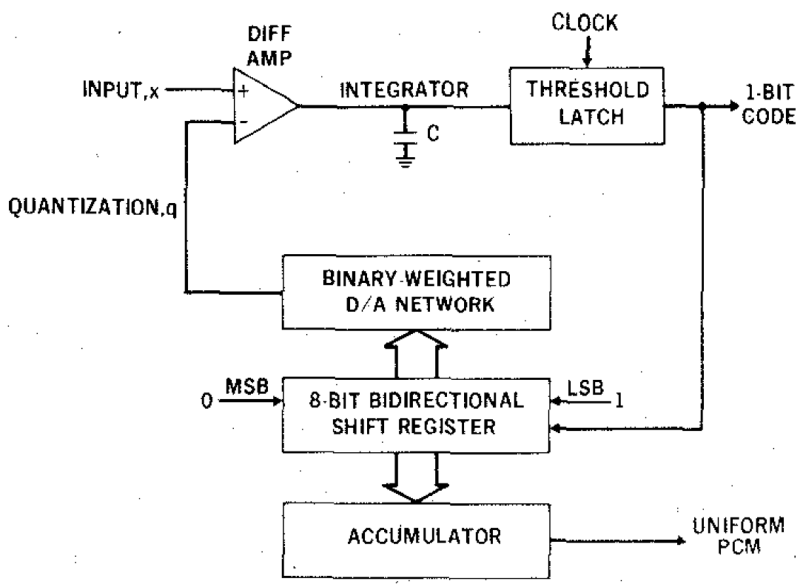


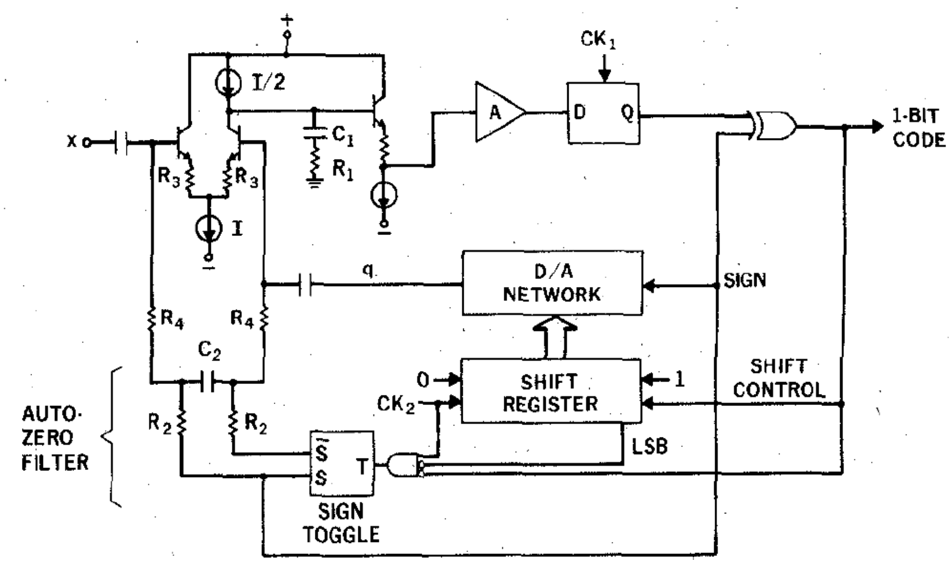
(a)

Integrated Voiceband Encoder

An early integrated interpolating modulator for digitizing voiceband signals:

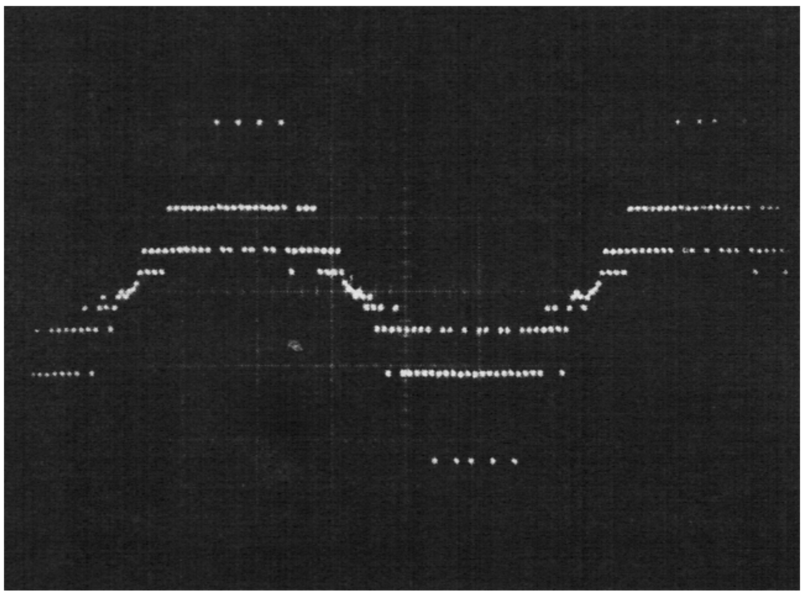
J. Henry and B. Wooley "An Integrated PCM Encoder Using Interpolation," *ISSCC Dig. Tech. Papers,* Feb. 1978.



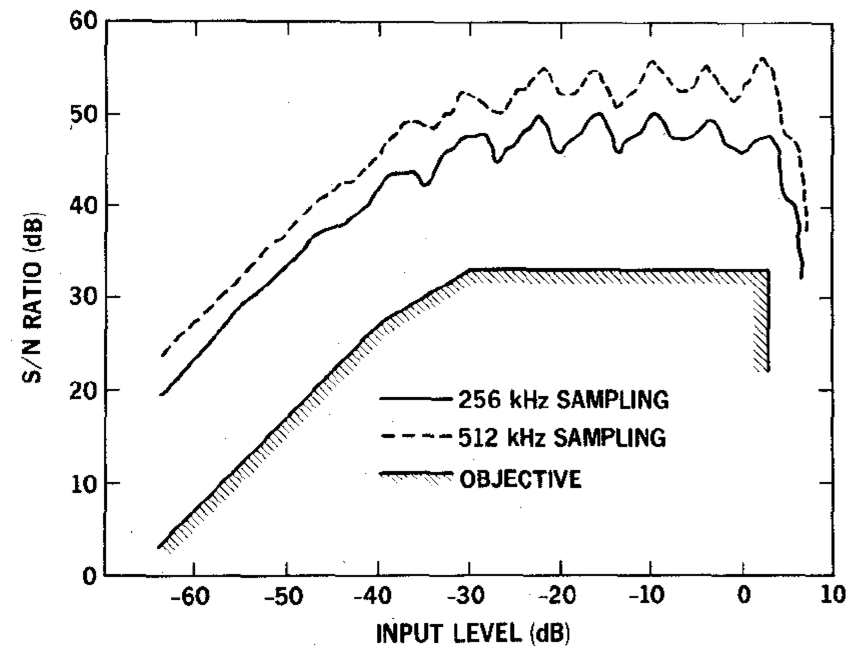


Integrated Interpolative Encoder Response

Quantization signal and SNDR of integrated voiceband encoder based on interpolation:



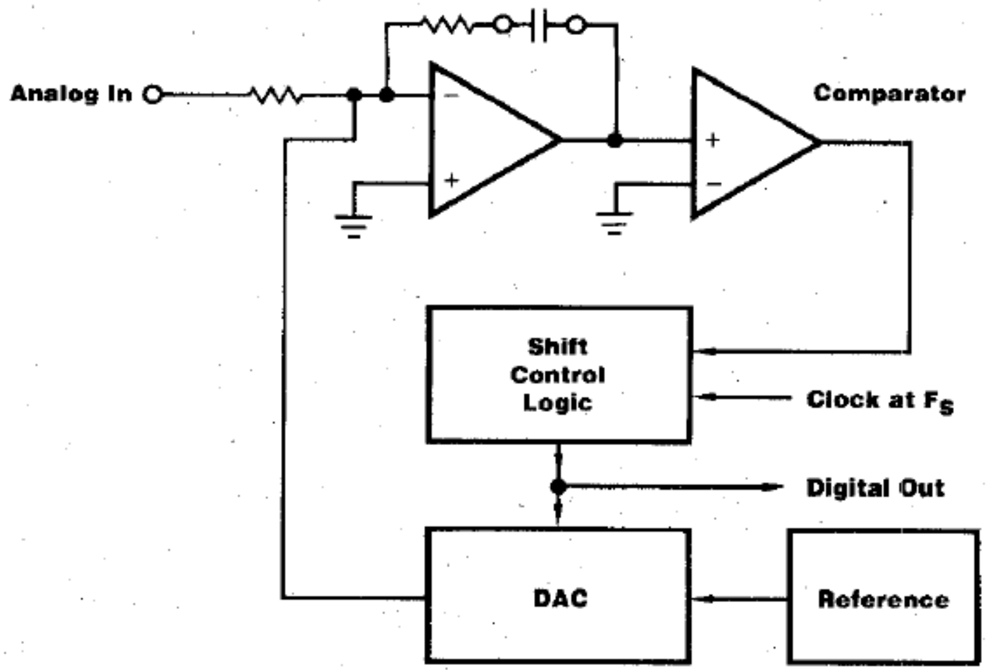
Quantization Signal



SNDR for 1-bit Output

Commercial Application of Oversampling

- First large-scale commercial application of oversampling was an interpolating modulator used by AMD in a Subscriber Line Audio Processing Circuit (SLAC) and an FSK Modem
  - Am7901, Am7905 and Am7910

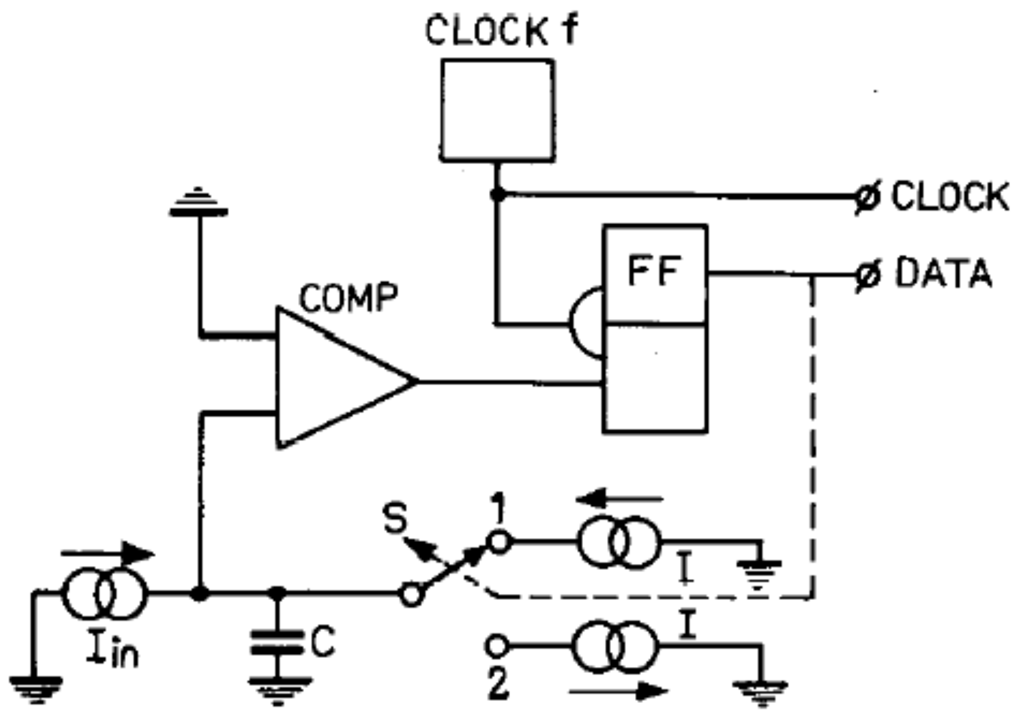


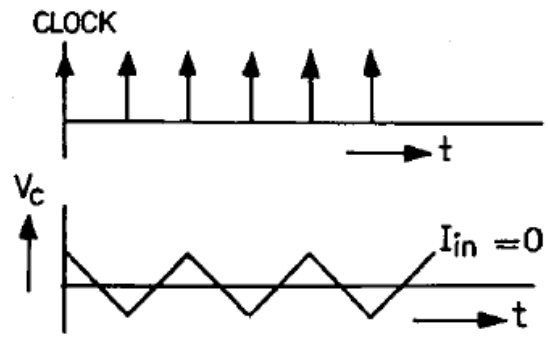
R. Apfel, et al., "A Single-Chip Frequency-Shift Keyed Modem Implemented Using Digital Signal Processing," *IEEE J. Solid-State Circuits*, Dec 1984.

Another Application

Rudy van de Plassche looked for applications in instrumentation and control as an alternative to dual-slope conversion:

R. van de Plassche, "A Sigma-Delta Modulator as an A/D Converter," *IEEE Trans. Circuits and Sys.,* July 1978.

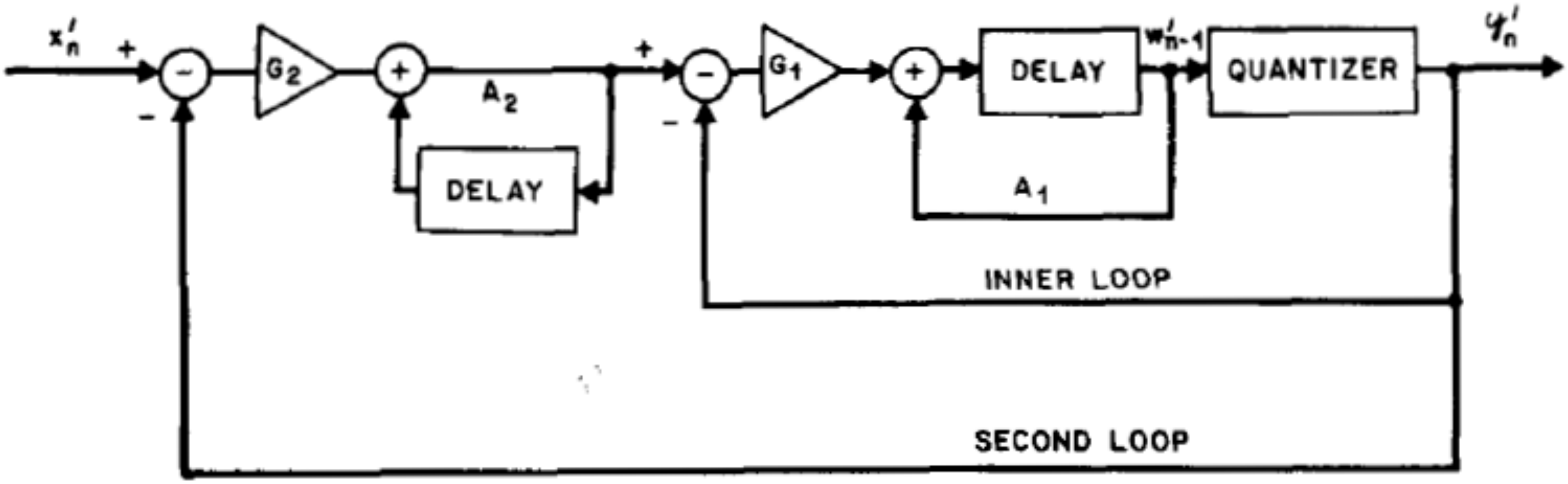




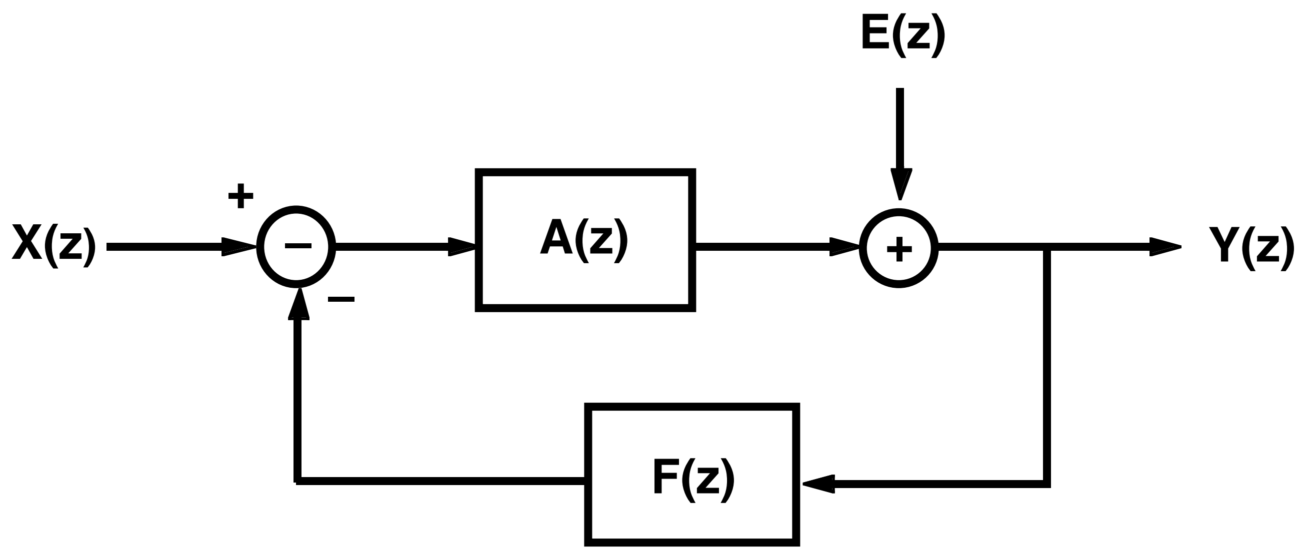
2nd-Order ΣΔ Modulation

In 1985 Candy described the use of double integration to achieve second-order **noise differencing**:

J. Candy, "A Use of Double Integration in Sigma-Delta Modulation," *IEEE Trans. Commun.*, Mar. 1985.



Single-Quantizer Oversampling Modulators



$$Y(z) = H_X(z)X(z) + H_E(z)E(z)$$

where

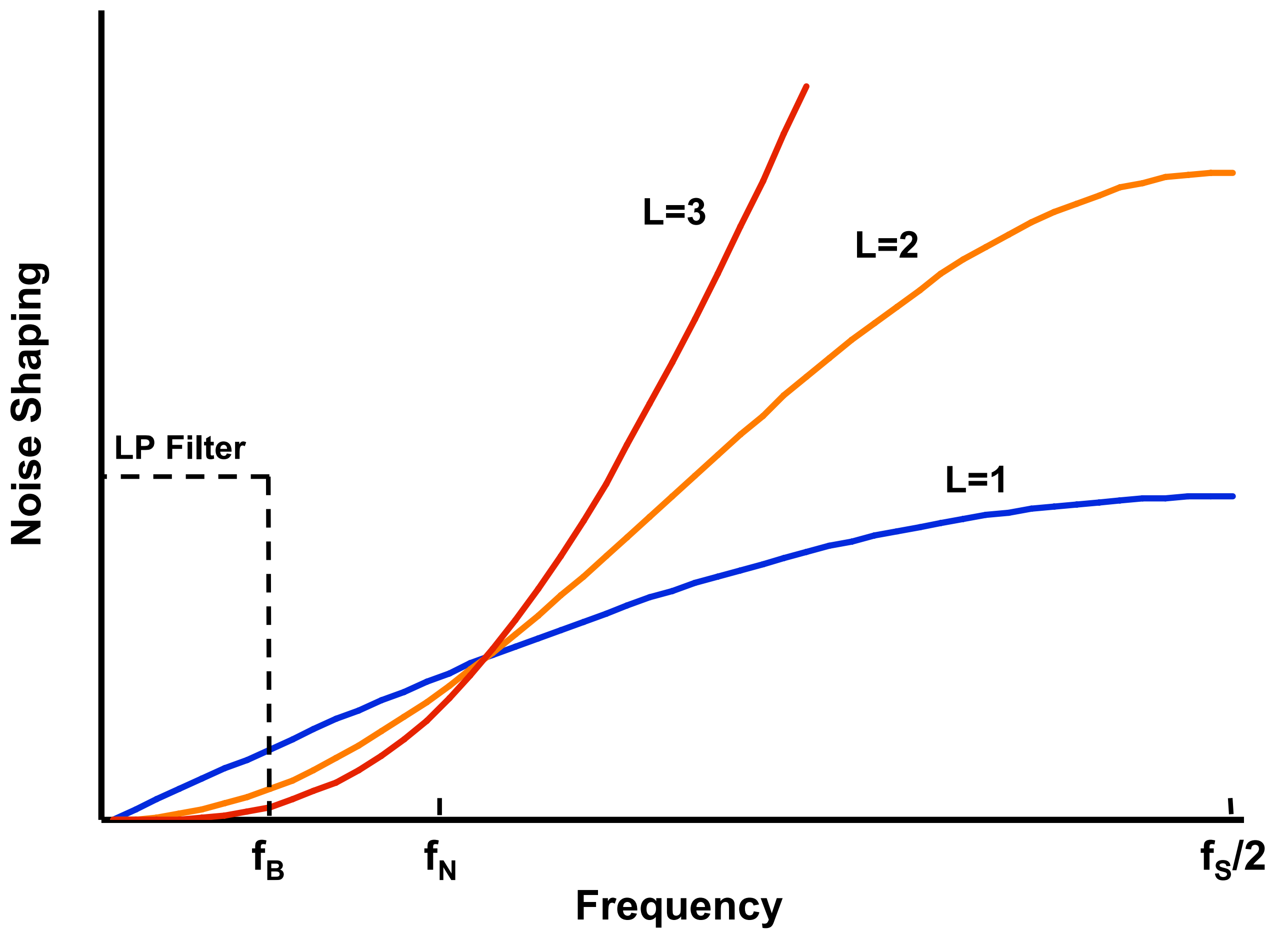
$$H_X(z) = \frac{A(z)}{1 + A(z)F(z)} \quad , \quad H_E(z) = \frac{1}{1 + A(z)F(z)}$$

and

$$A(z) = \frac{H_X(z)}{H_E(z)} \quad , \quad F(z) = \frac{1 - H_E(z)}{H_X(z)}$$

Noise-Differencing ΣΔ Modulators

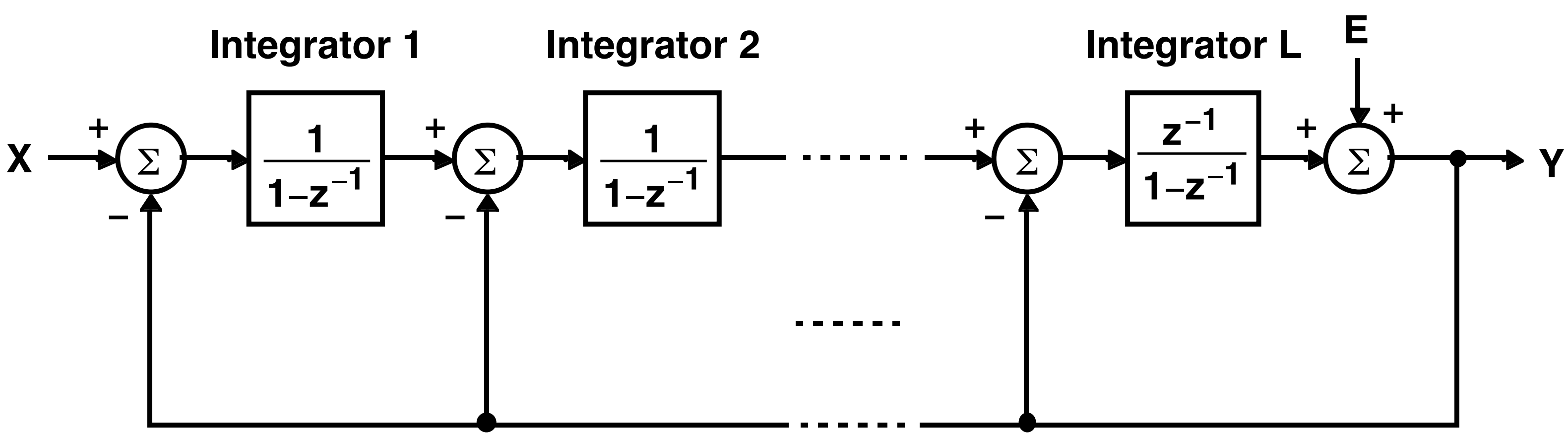
$$Y(z) = z^{-n}X(z) + (1 - z^{-1})^{L}E(z) \quad \Rightarrow \quad S_B \cong \frac{\pi^{2L}}{(2L+1)}\left(\frac{1}{M}\right)^{2L+1} S_Q$$



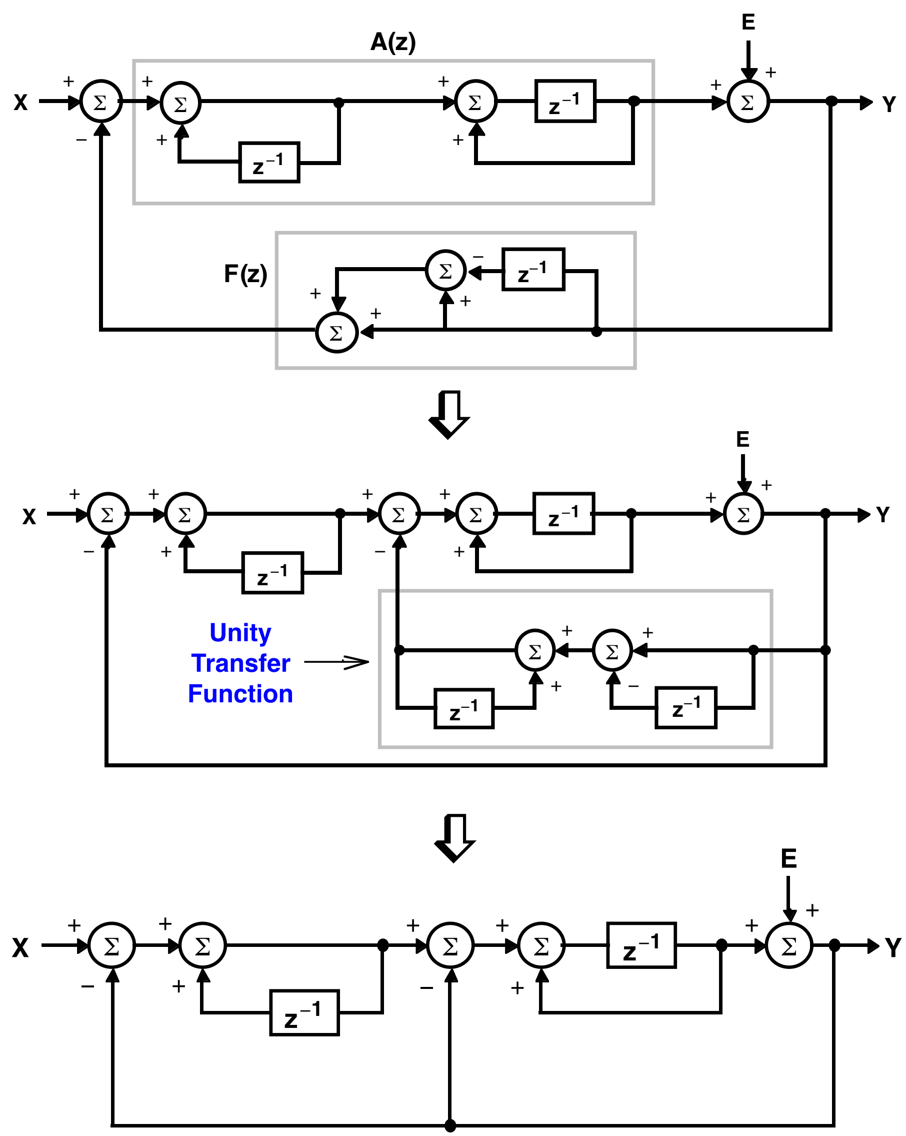
Noise Differencing Modulators

- $Y(z) = z^{-1}X(z) + (1 - z^{-1})^{L}E(z)$
- Can implement with a single quantizer and L nested loops
- Limit cycle instability for L > 2
- For L = 2

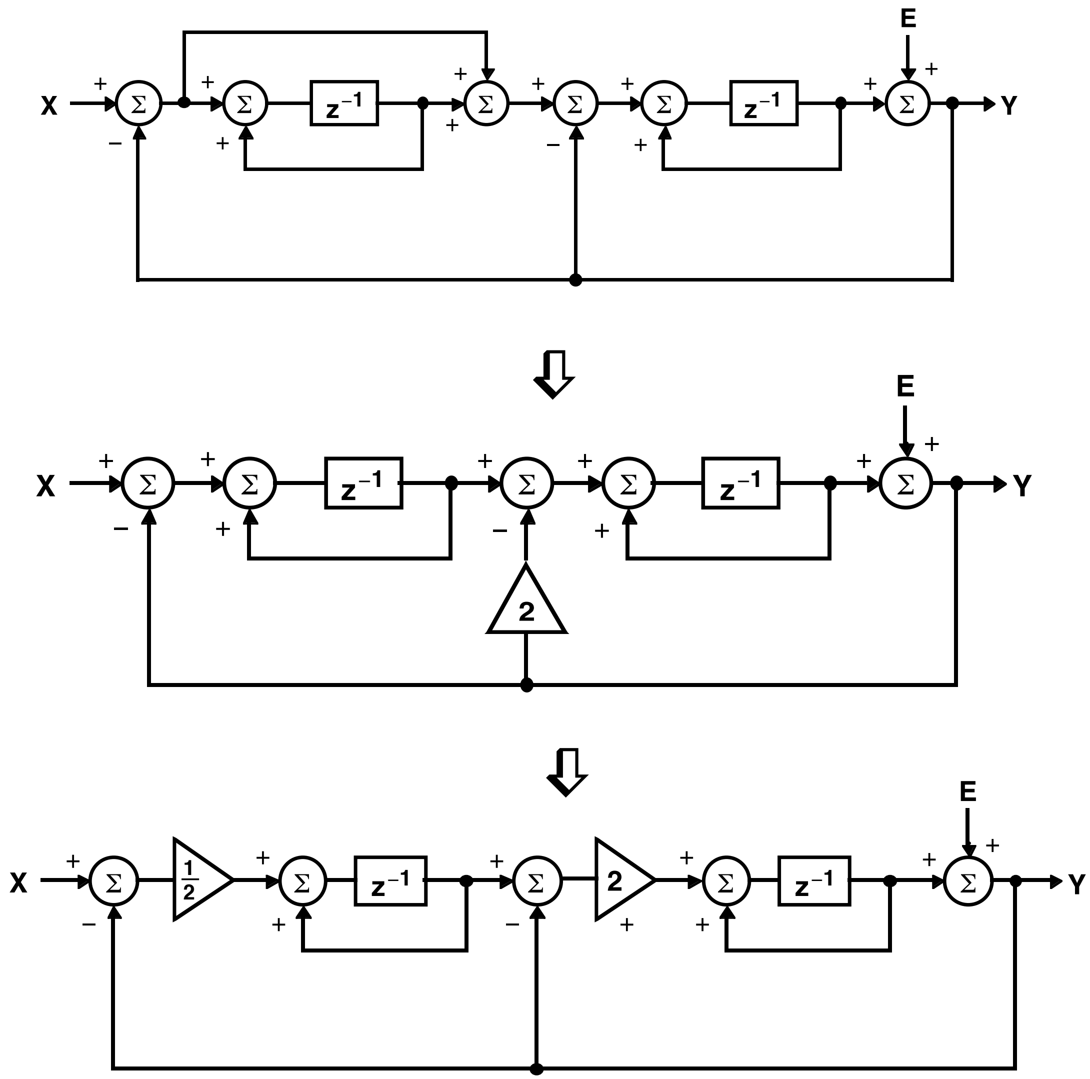
$$A(z) = \frac{z^{-1}}{(1 - z^{-1})^2} \quad \text{and} \quad F(z) = 2 - z^{-1}$$



2nd-Order Noise Differencing

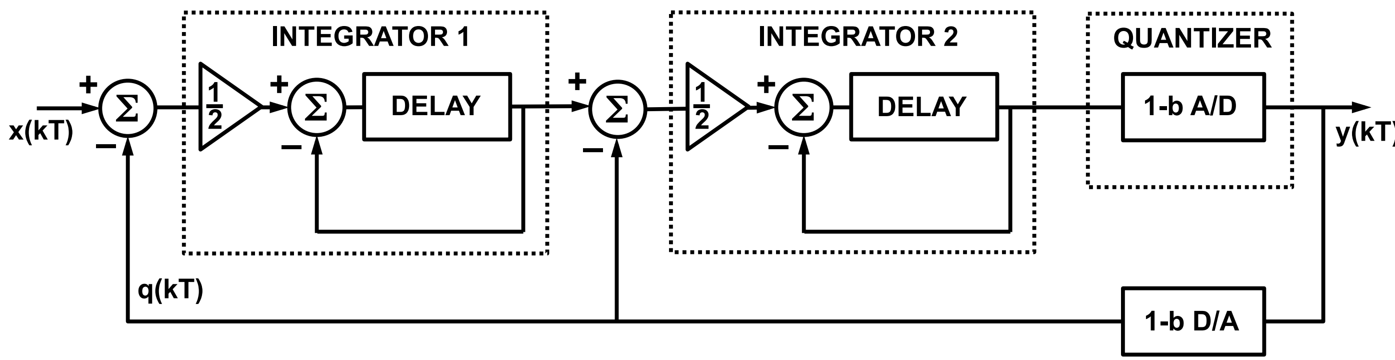


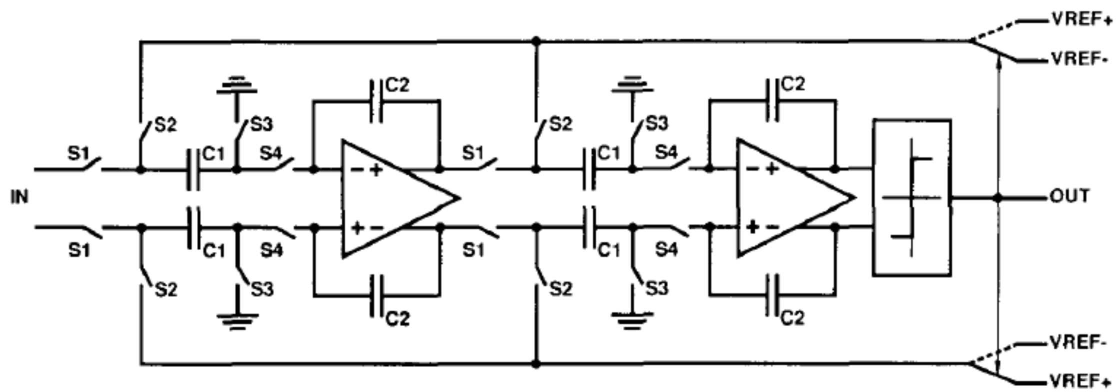
2^{nd}-Order Noise Differencing

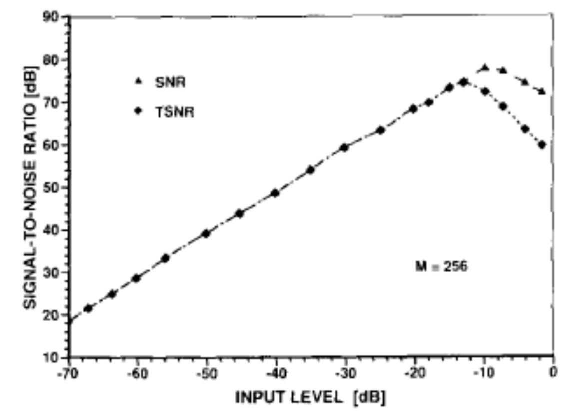


A Switched-Capacitor 2^{nd}-Order Modulator

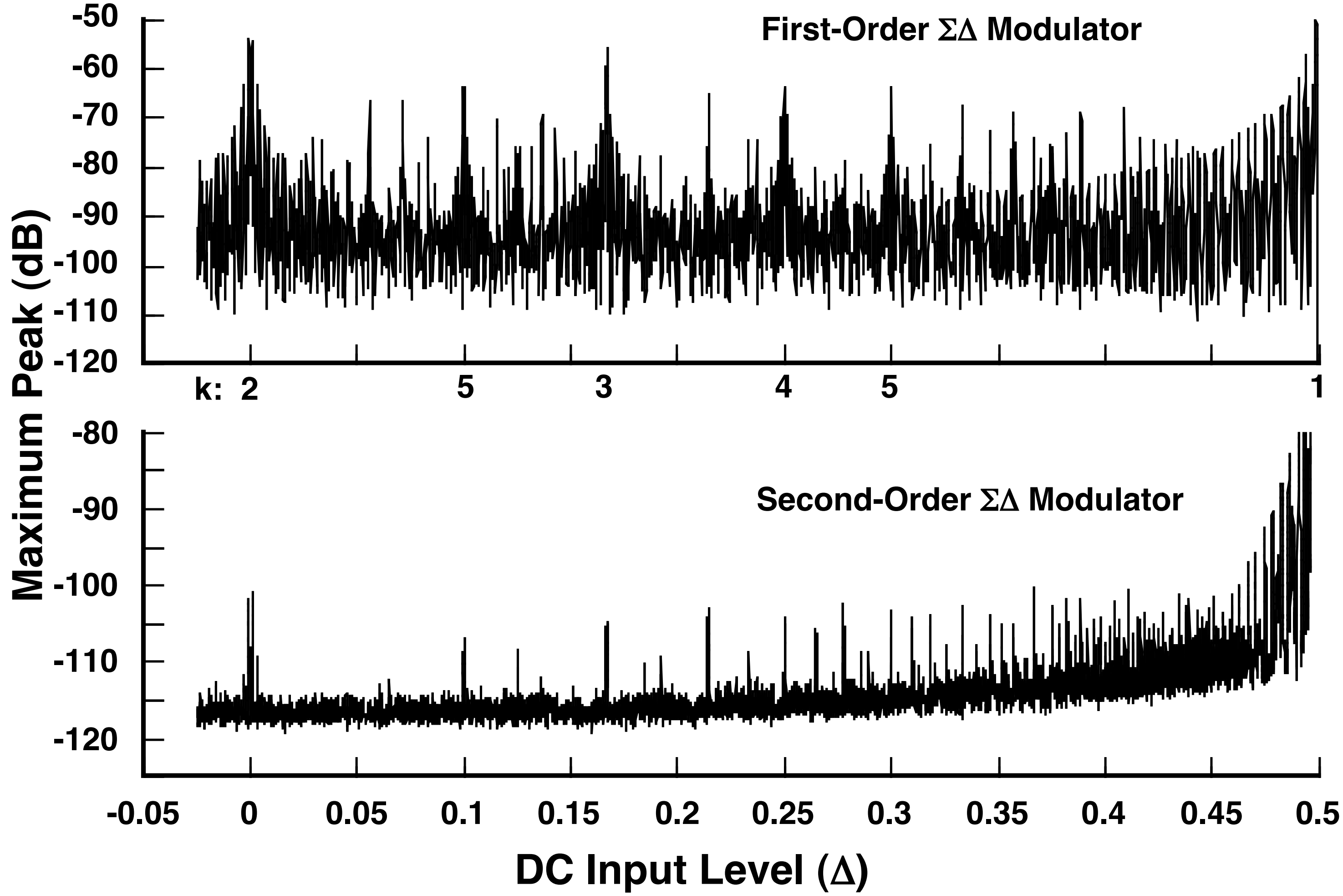
B. Boser and B. Wooley, "Design of a CMOS Second-Order Sigma-Delta Modulator," *ISSCC Dig. Tech. Papers*, Feb. 1988.





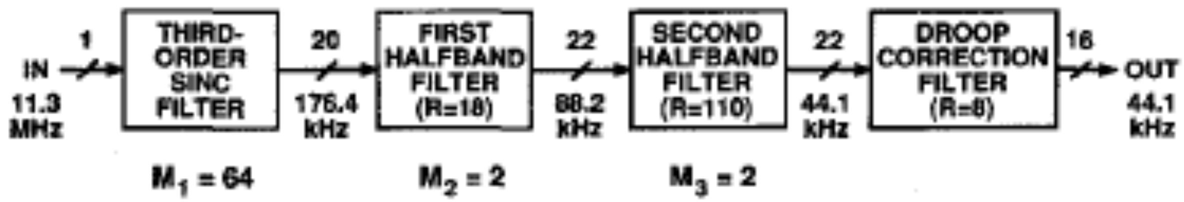


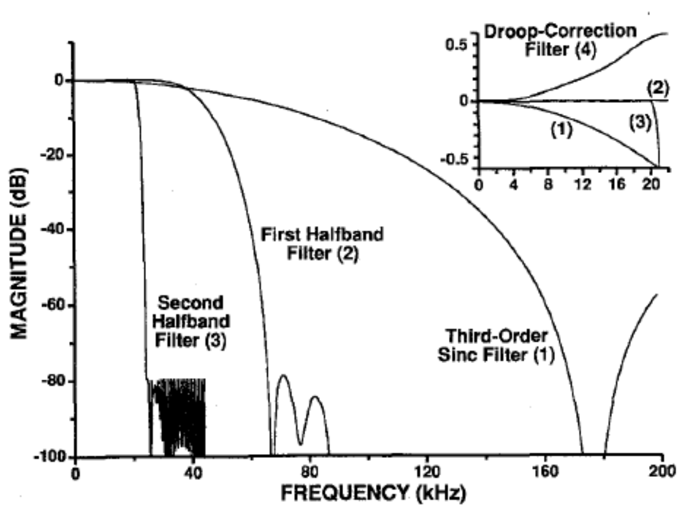
Iwerson Noise in ΣΔ Modulators

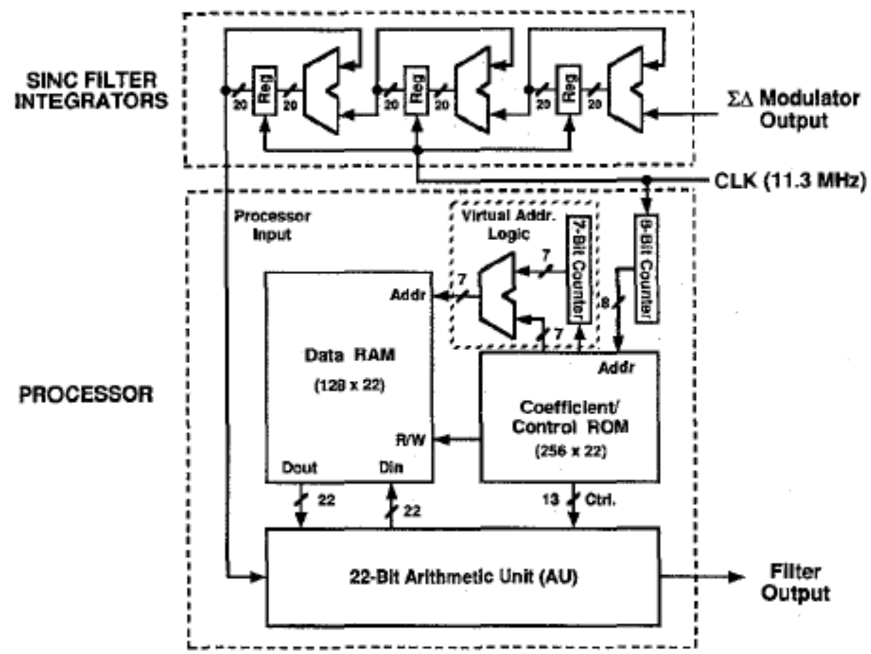


Decimation & Interpolation for Digital Audio

B. Brandt and B. Wooley, "A Low-Power, Area-Efficient Digital Filter for Decimation and Interpolation," *Symp. VLSI Circuits*, May 1993.



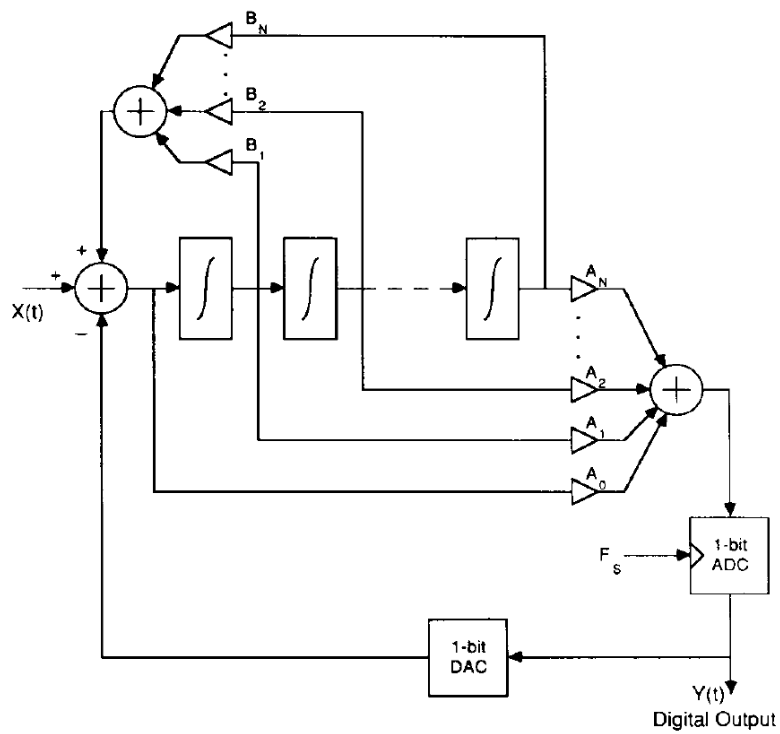




n^{th}-order Single-Quantizer Modulators

- Noise-differencing modulators of order greater than 2 are prone to limit-cycle instability
- Can stabilize higher order, single-quantizer modulators through filter design, non-linear stabilization and/or multi-bit quantization

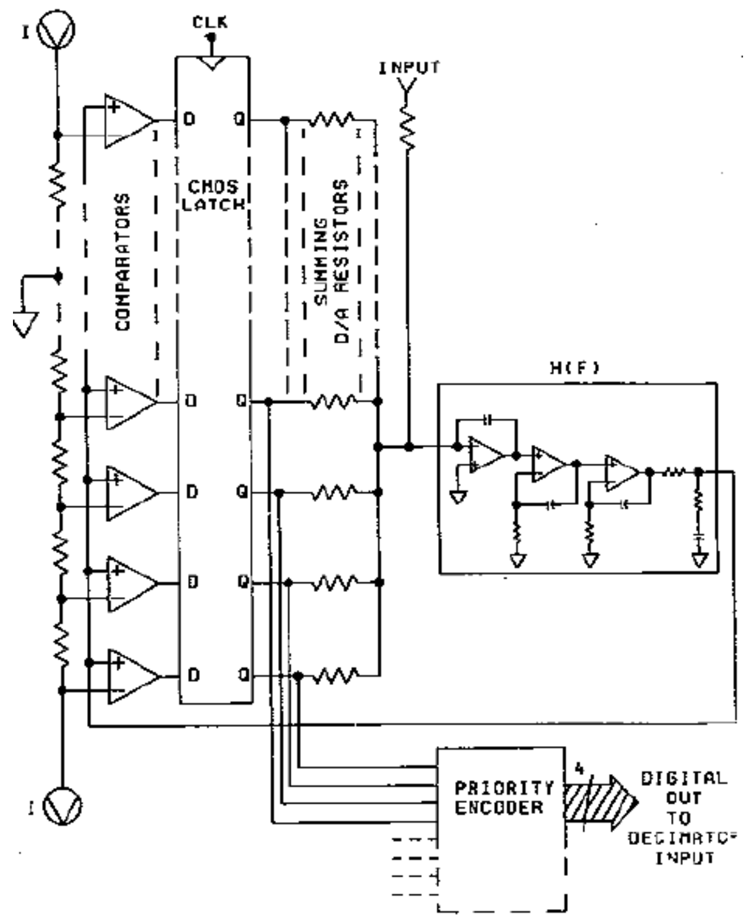
  W. Lee and C. Sodini, "A Topology for Higher Order Interpolative Coders ," *ISCAS Proc.*, May 1987.



ΣΔ Modulation for Digital Audio

Third-order noise shaping with multi-bit quantization:

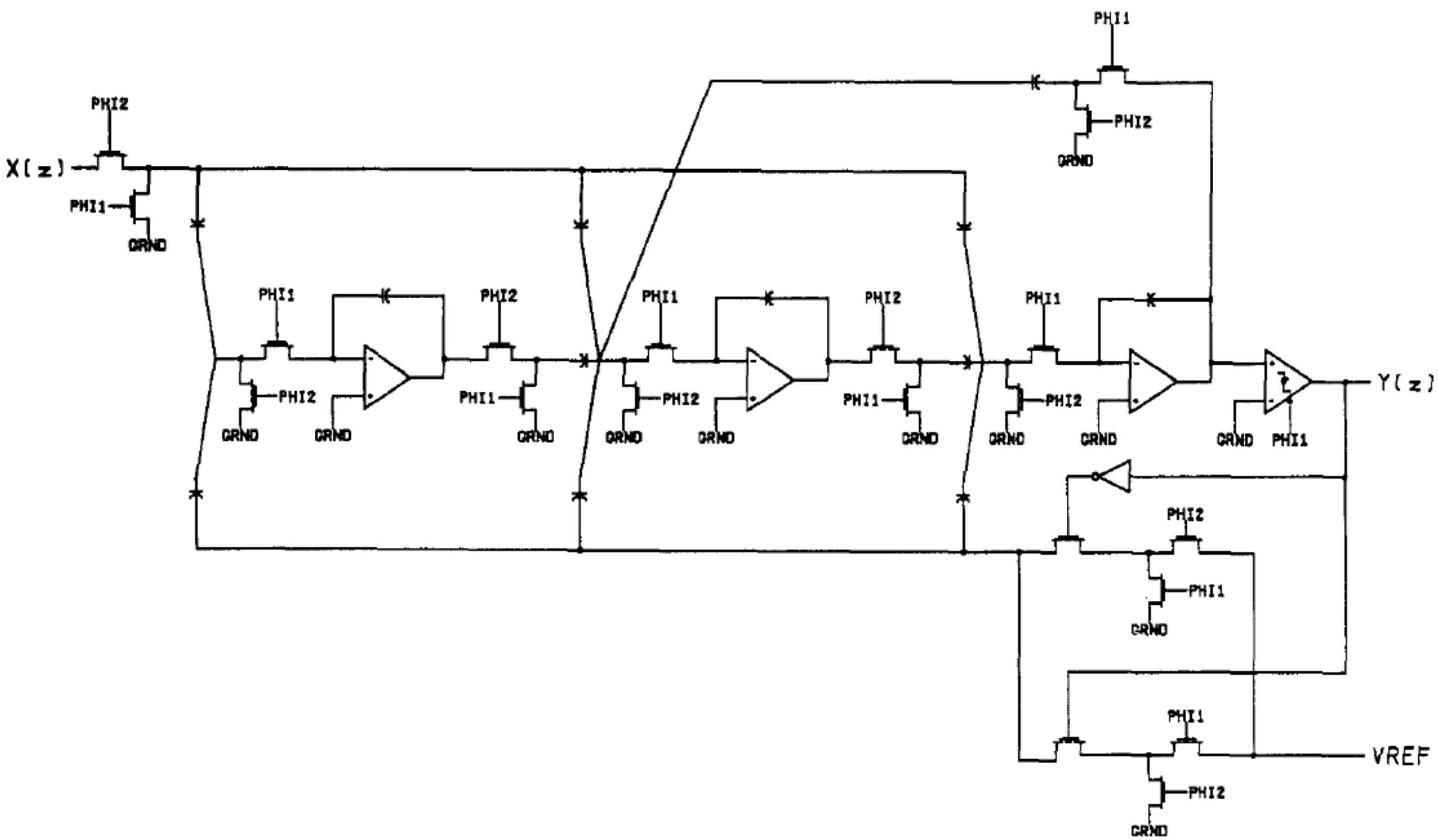
R. Adams, "Design and Implementation of an Audio 18-bit Analog-to-Digital Converter Using Oversampling Techniques," *J. Audio Eng. Soc.*, Mar. 1986.



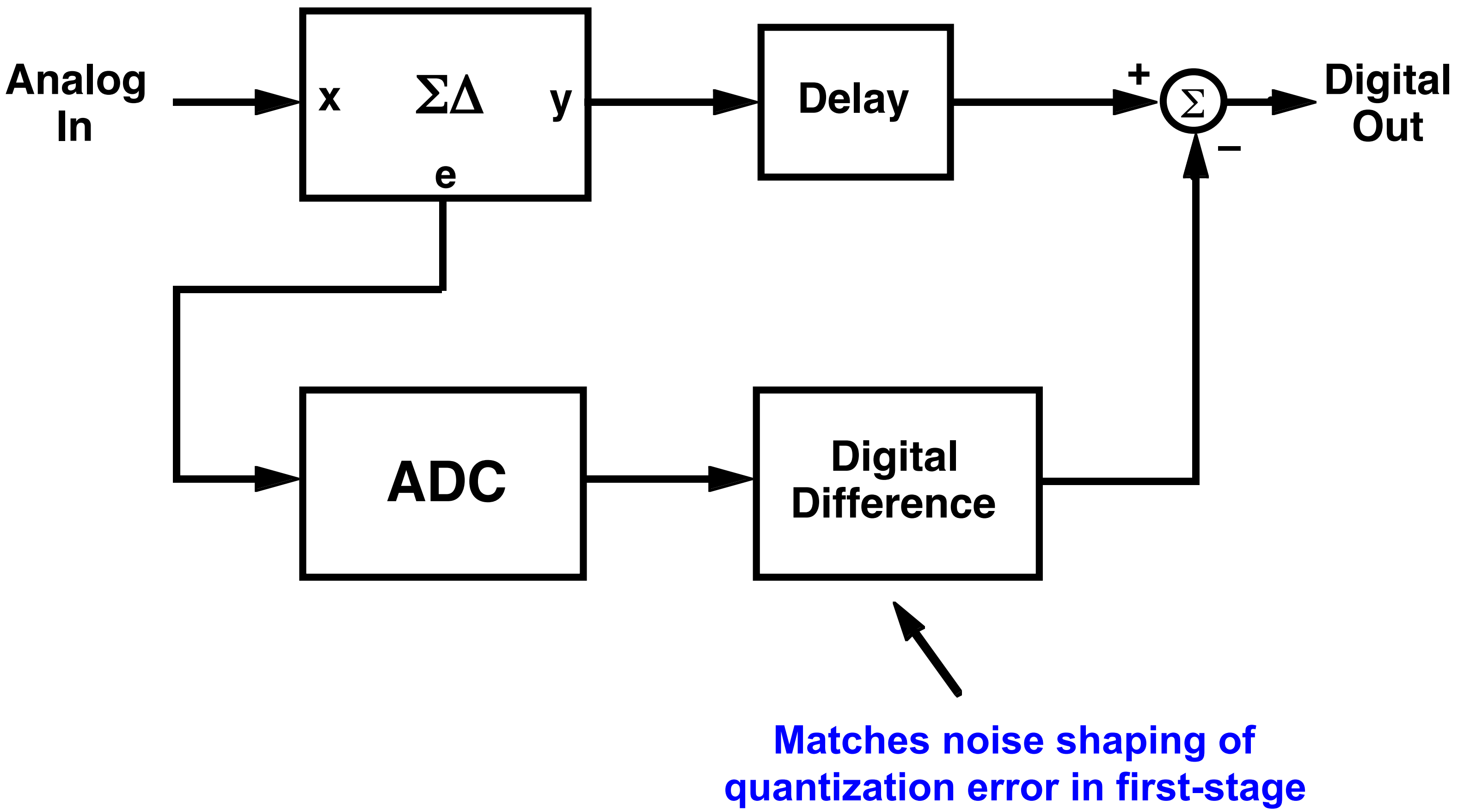
Single Quantizer w/ Distributed Feedback

A high-order, single-bit ΣΔ modulator employing "distributed feedback" and non-linear stabilization:

P. Ferguson, A. Ganesan and R. Adams, "One Bit Higher Order Sigma-Delta A/D Converters," *ISCAS Proc.*, May 1990.



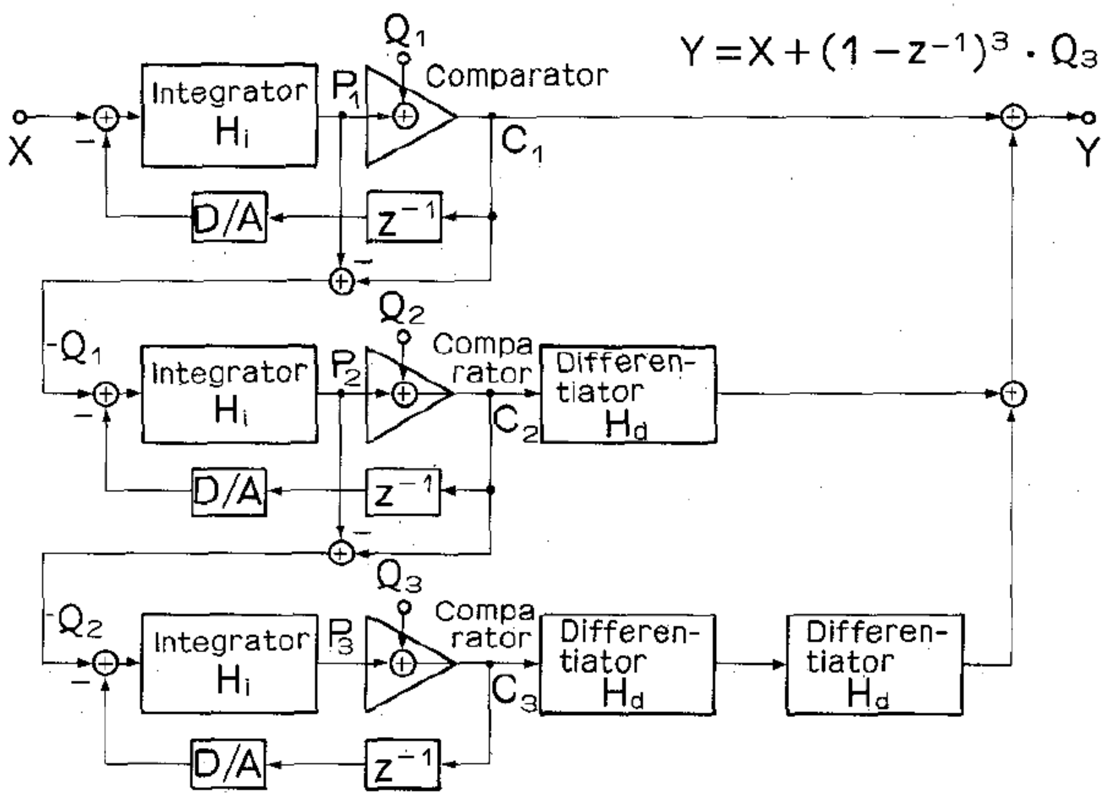
Cascaded (Multi-Stage) Noise-Shaping



Multi-stage Noise Shaping (MASH)

An early paper on multi-stage (**MASH**) modulators for stable high-order noise shaping (for digital audio signals):

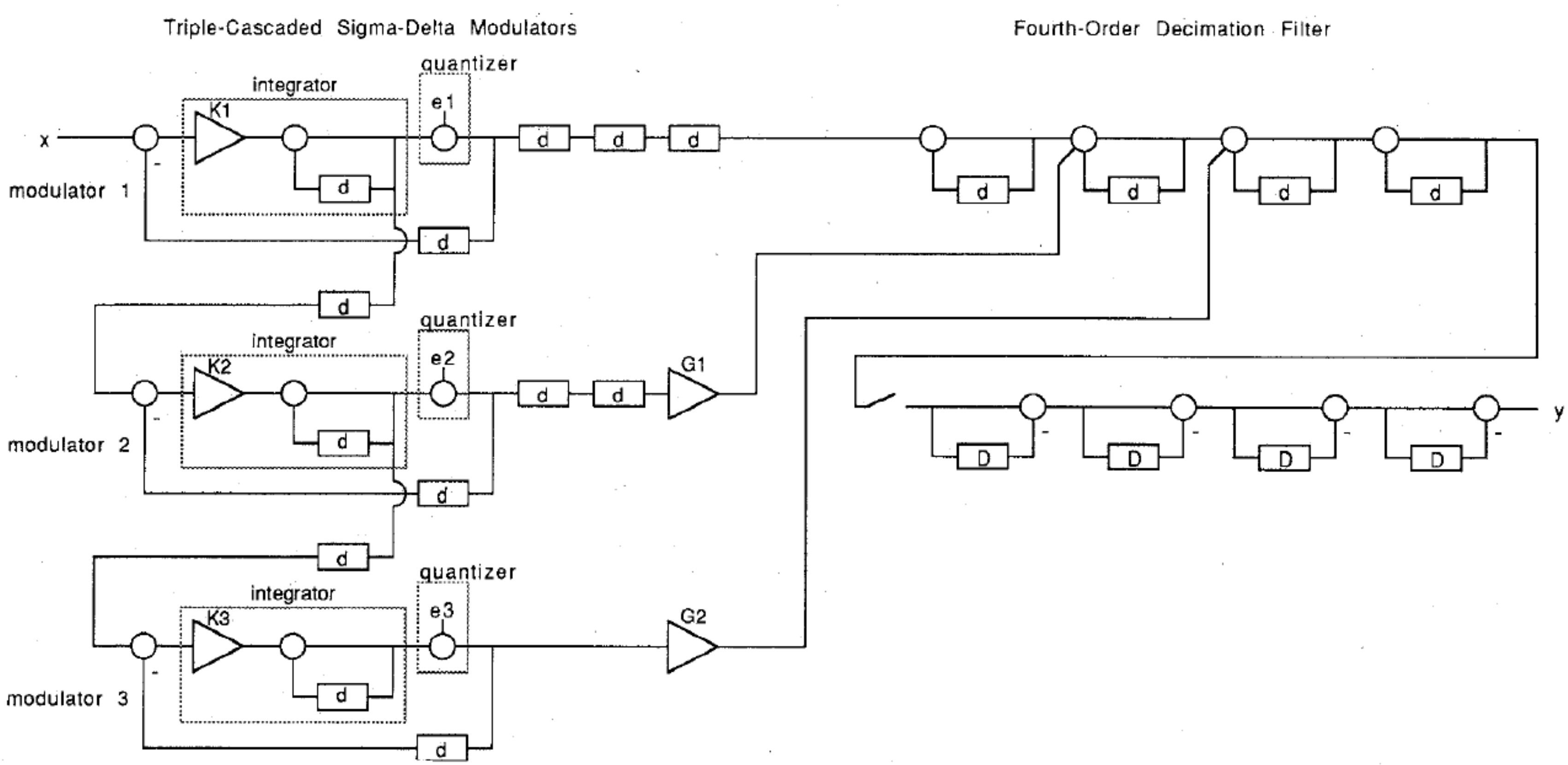
Y. Matsuya, et al., "A 16b Oversampling A/D Conversion Technology using Triple Integration Noise Shaping," *ISSCC Dig. Tech. Papers*, Feb. 1987.



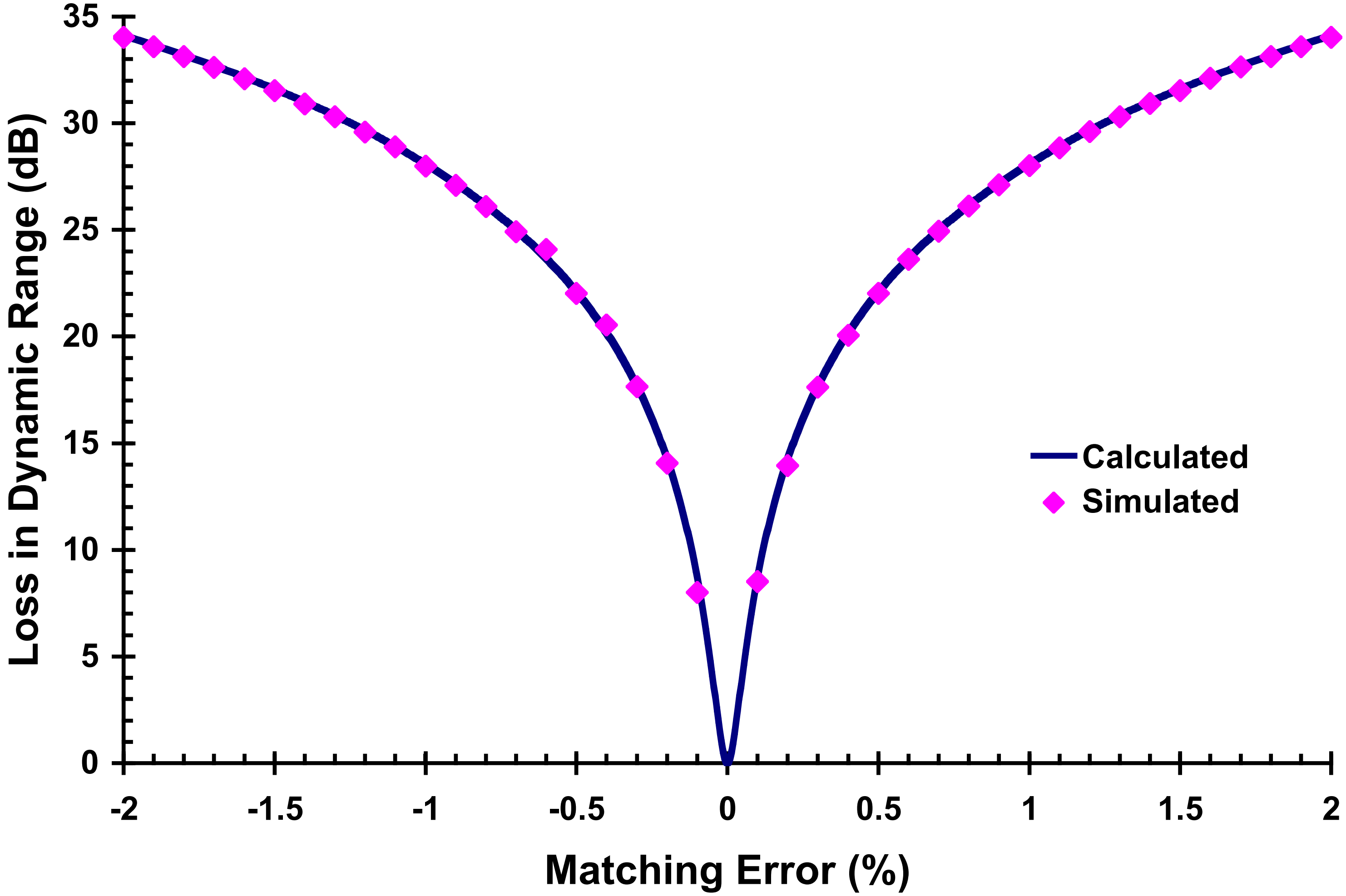
A Cascaded Modulator for ISDN

An early cascade of first-order ΣΔ modulators for ISDN bandwidths:

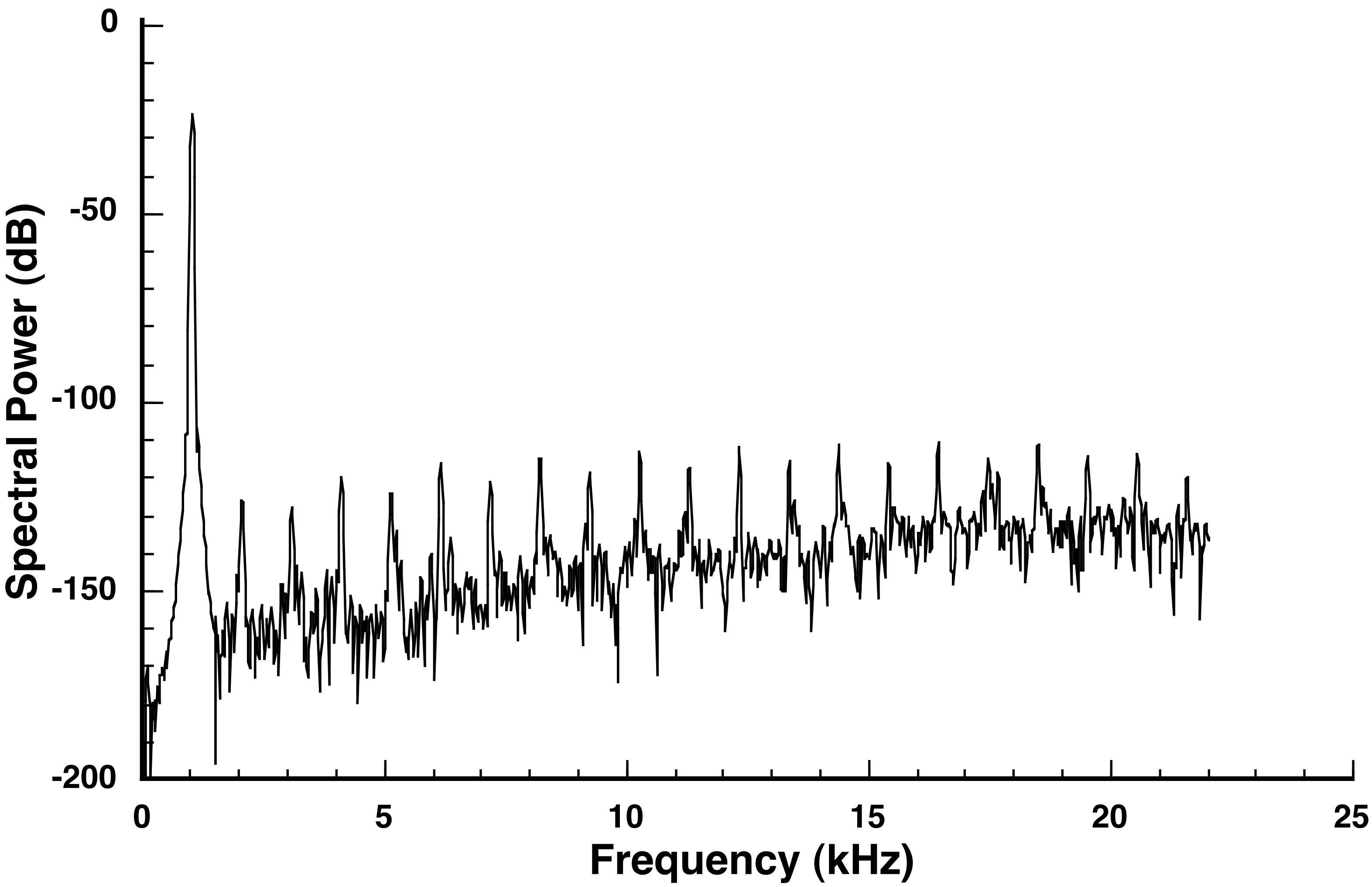
M. Rebeschini, et al., "A 16-Bit 160 kHz CMOS A/D Converter Using Sigma-Delta Modulation," *ISCAS Proc.*, May 1990.



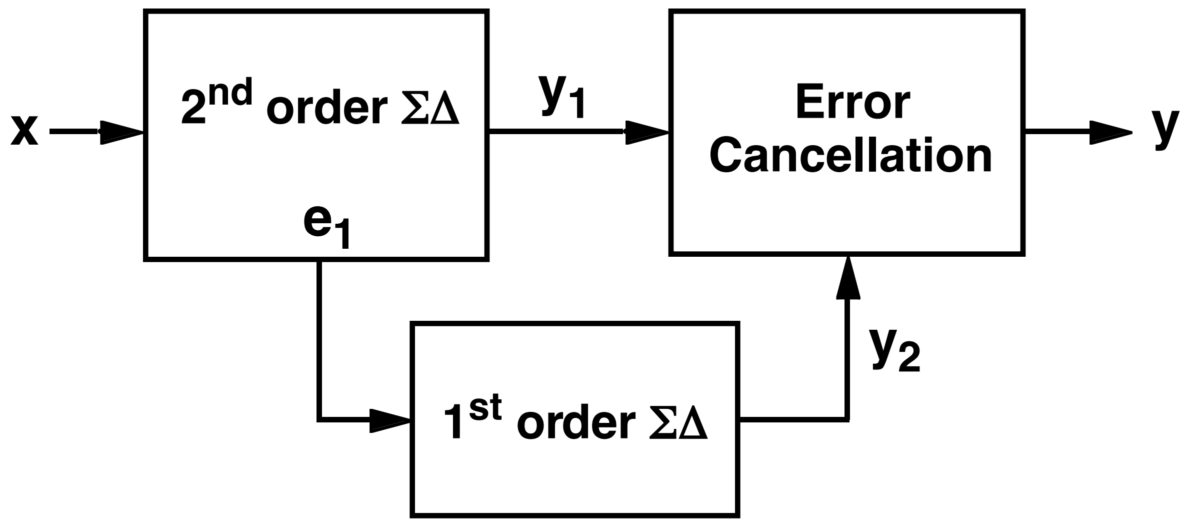
Matching Error in 1-1-1 Cascade



Spectrum of 1-1-1 Cascade w/ Mismatch



Third-Order (2-1) Cascaded Modulator



$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_2(z)$$

2-1 Cascaded ΣΔ Modulator

First description of a two-stage 2-1 cascaded modulator:

L. Longo and M. Copeland, "A 13 bit ISDN-band Oversampled ADC using Two-Stage Third Order Noise Shaping," *Proc. CICC,* Jan. 1988.

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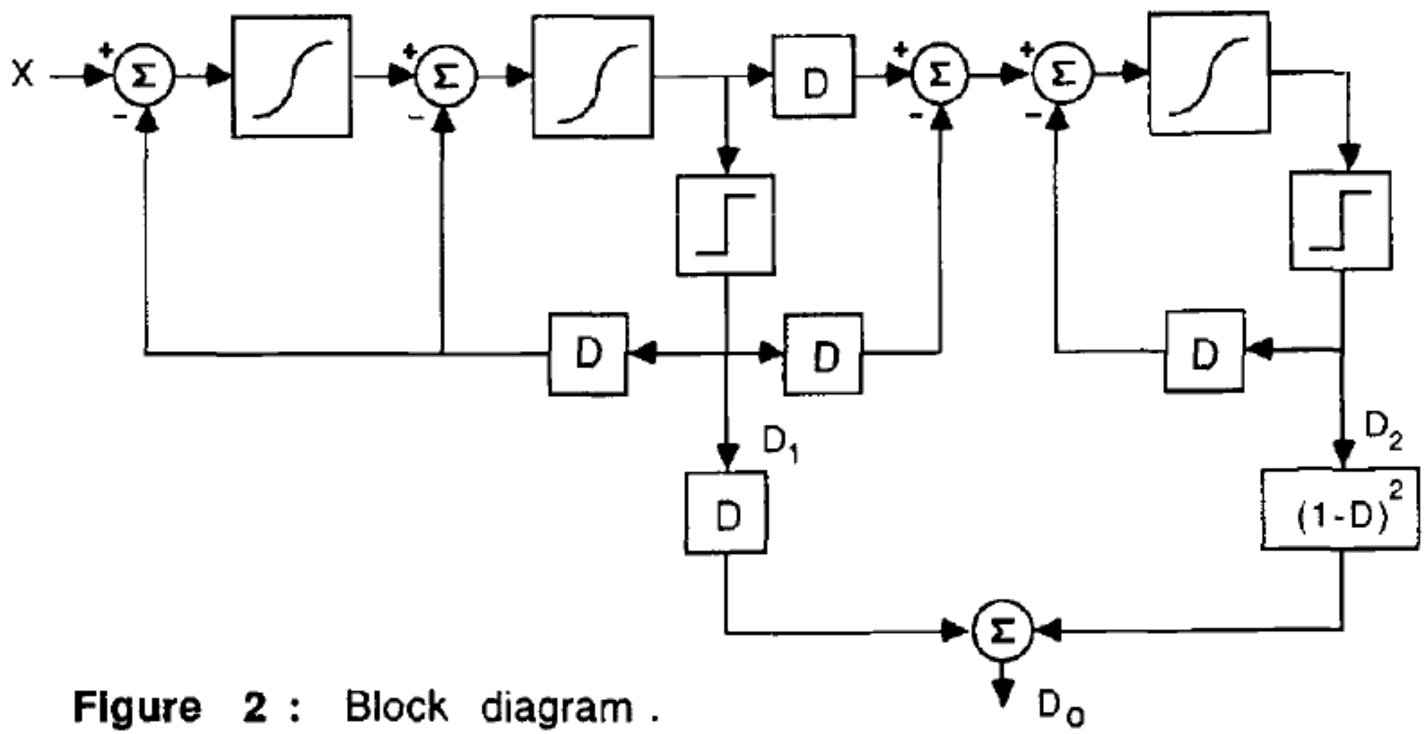
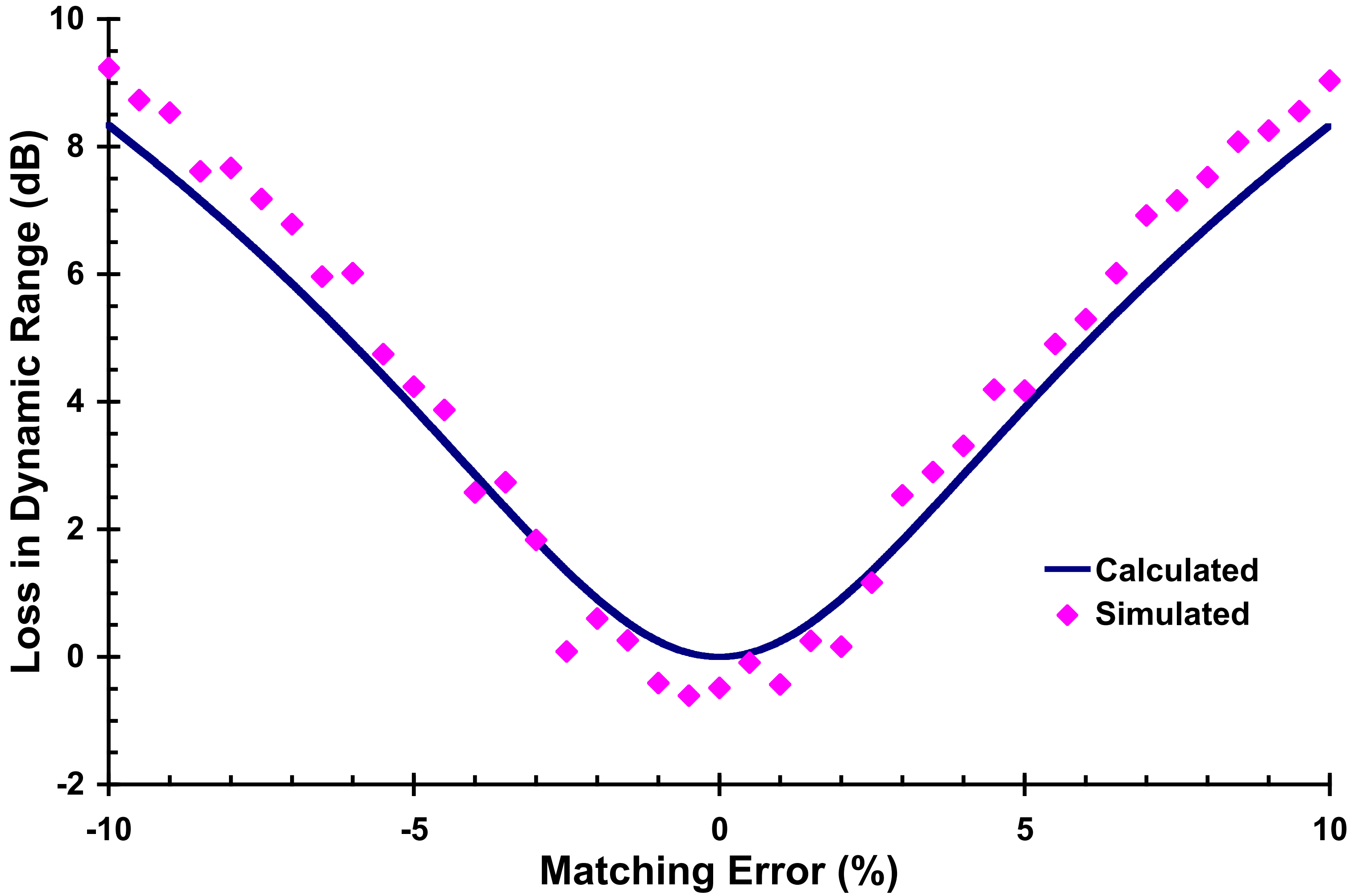
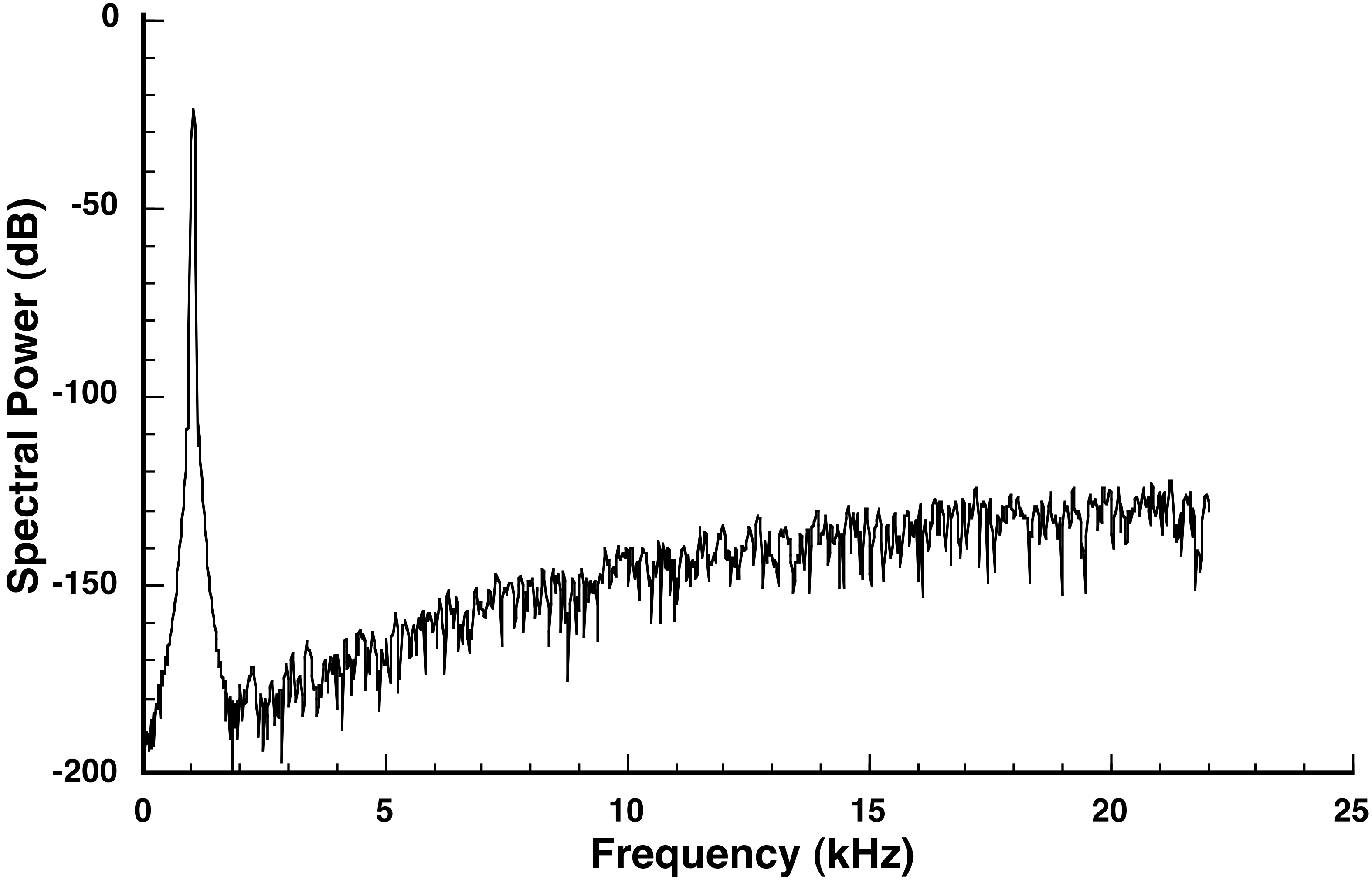


Figure 2 : Block diagram .

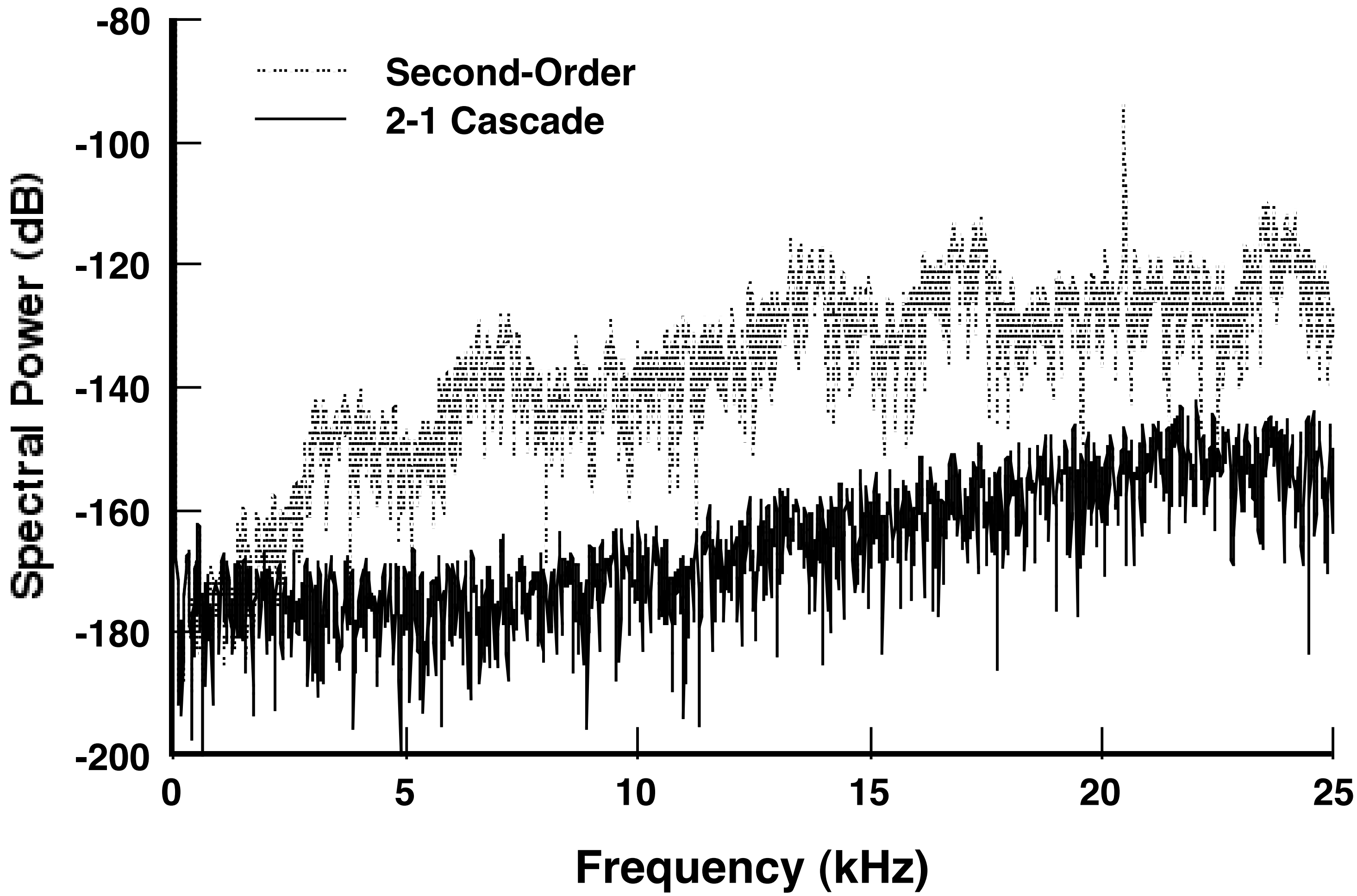
Matching Error in 2-1 Cascade



Spectrum of 2-1 Cascade w/ Mismatch

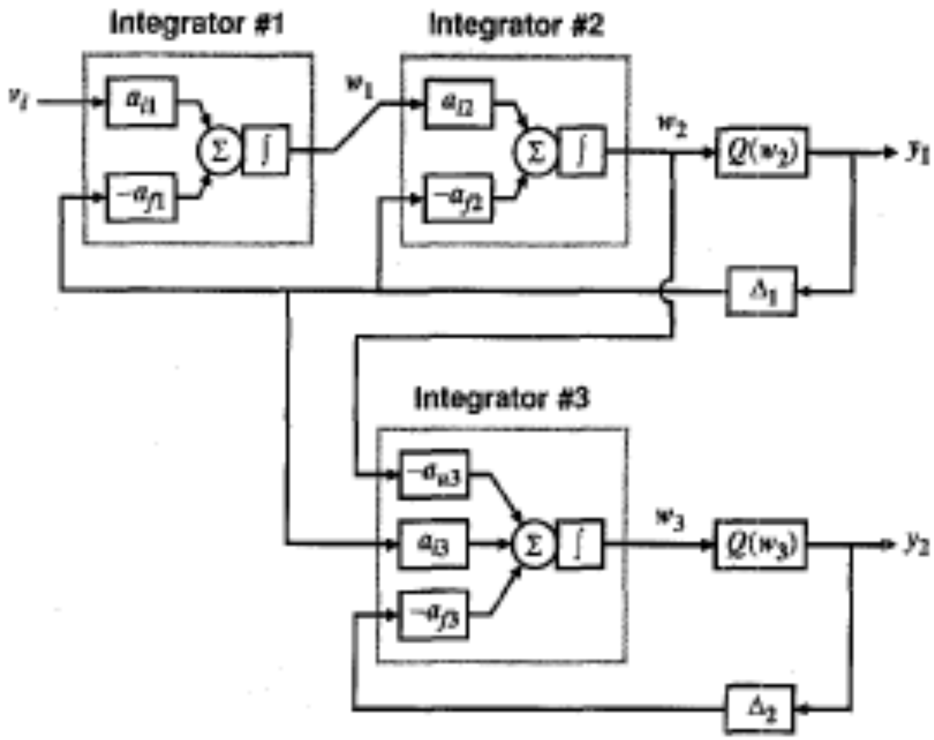


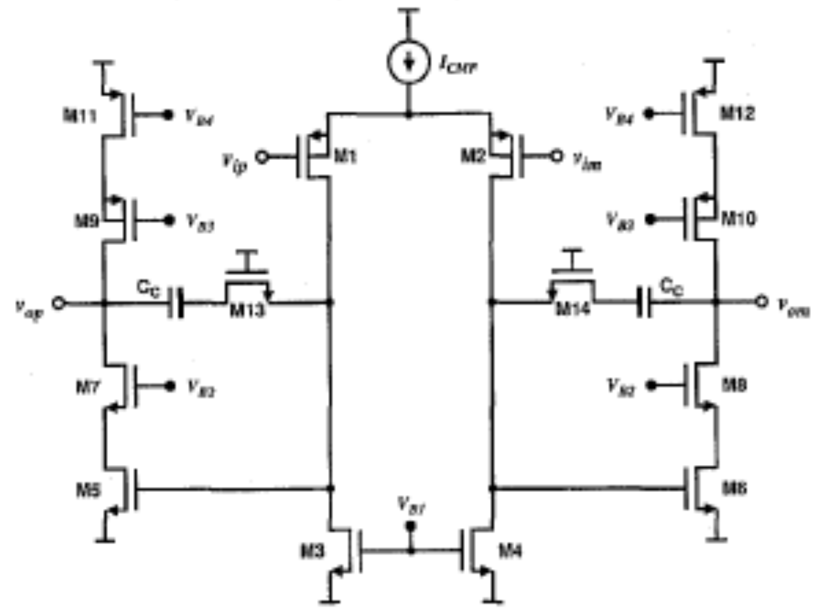
Tone Cancellation in 2-1 Cascade



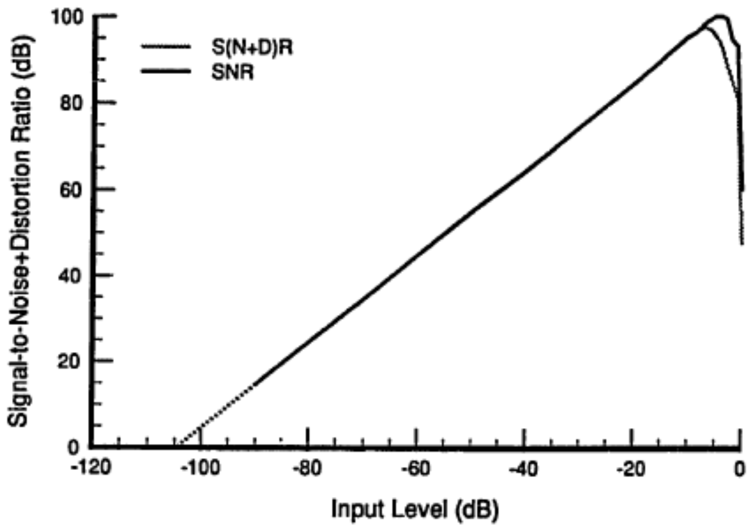
Cascaded ΣΔ Modulator for Digital Audio

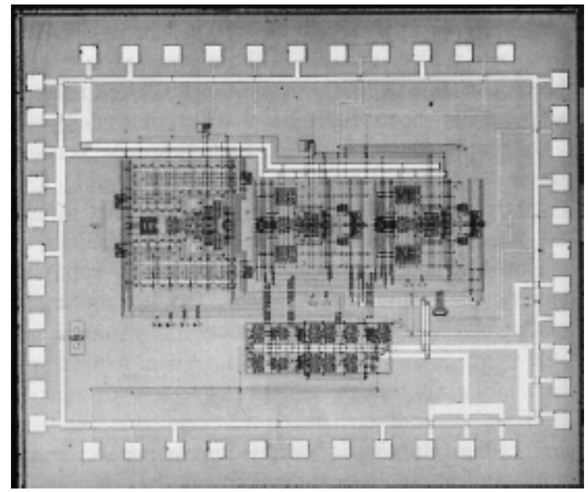
L. Williams and B. Wooley, “A Third-Order Sigma-Delta Modulator with Extended Dynamic Range,” *IEEE J. Solid-State Circuits*, Mar. 1994.

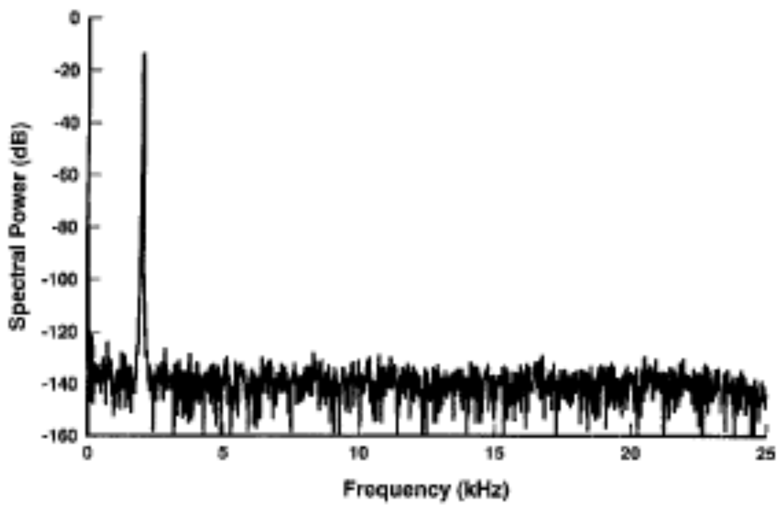




2-1 Cascaded ΣΔM Performance



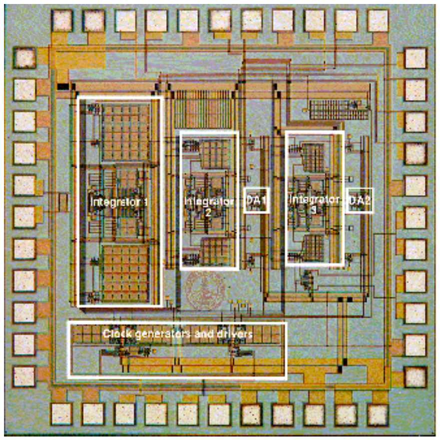


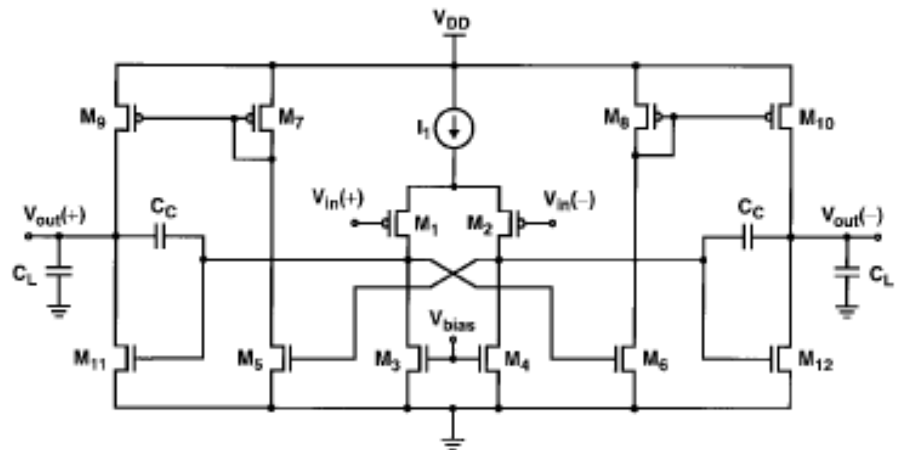


Supply Voltage	5 V
Sampling Rate	6.4 MHz
Signal Bandwidth	25 kHz
Dynamic Range	104 dB
Peak SNDR	98 dB
Power	47.2 mW
Active Area	5.2 mm^2
Technology	1-μm CMOS

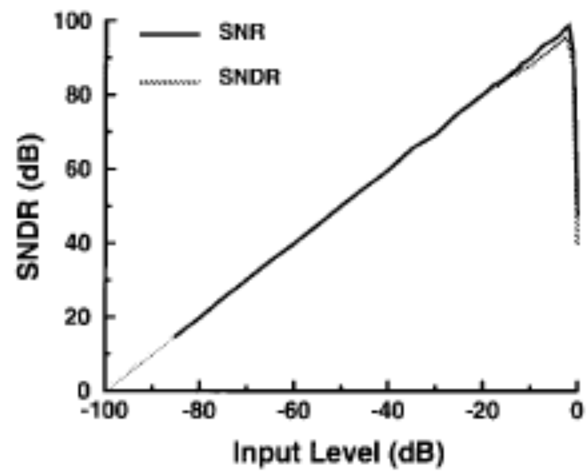
Low-Power 1.8-V ΣΔ Modulator

S. Rabii and B. Wooley, "A 1.8-V Digital Audio Sigma-Delta Modulator in 0.8-μm CMOS," *IEEE J. Solid-State Circuits*, June1997.



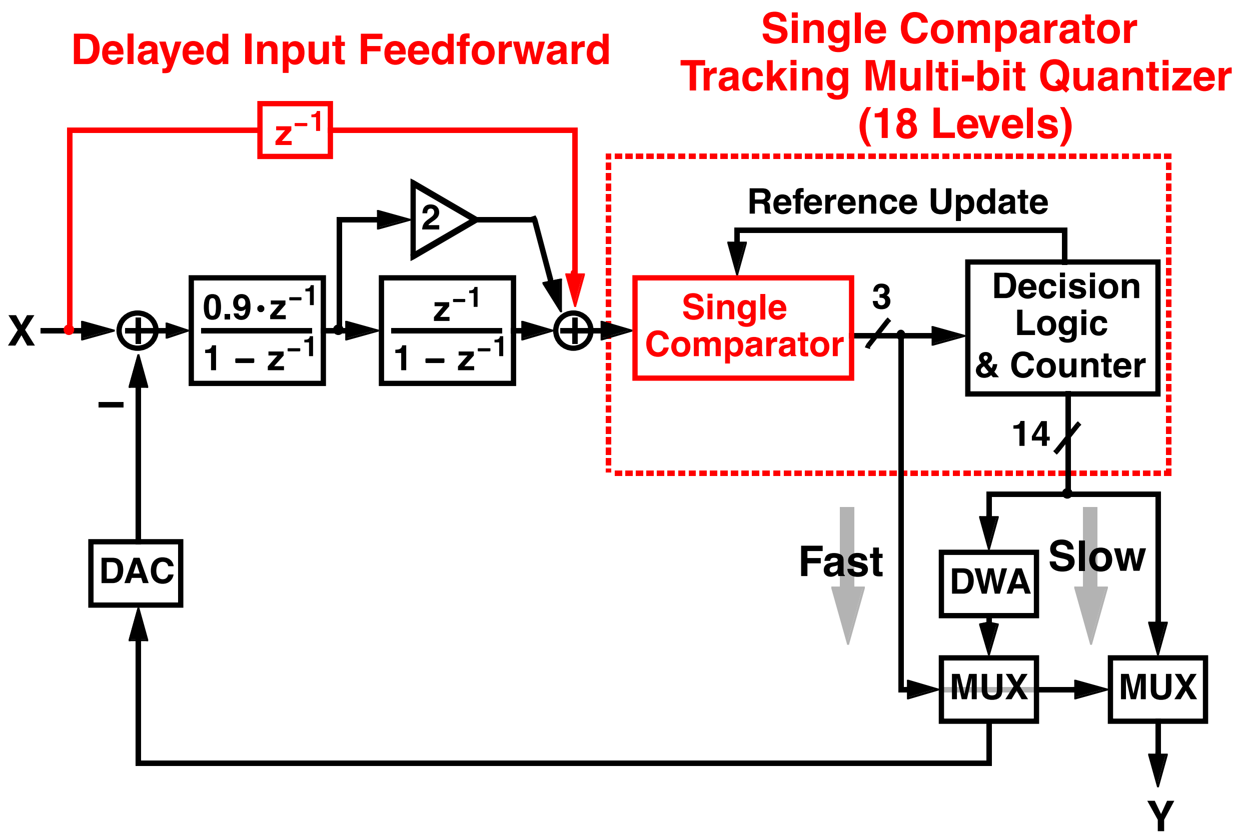


Supply Voltage	**1.8 V**
Sampling Rate	**4 MHz**
Signal Bandwidth	**25 kHz**
Dynamic Range	**99 dB**
Peak SNDR	**95 dB**
Power	**2.5 mW**
Active Area	**1.5 mm^2**
Technology	**0.8-μm CMOS**

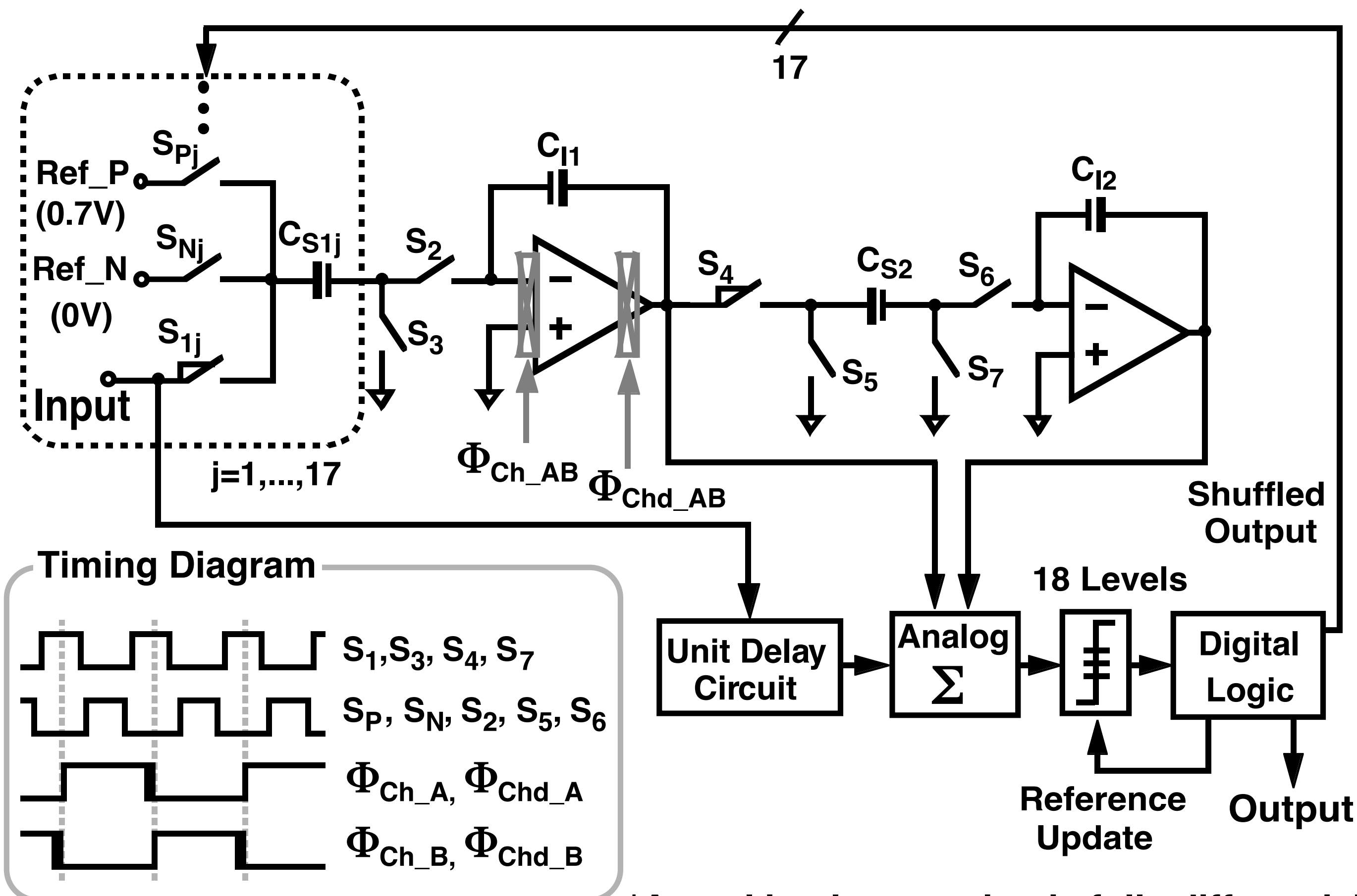


A Low-Voltage Cascaded ΣΔ Modulator

H. Park, et al., "A 0.7-V 870-μW Digital Audio CMOS Sigma-Delta Modulator," *IEEE J. Solid-State Circuits*, Apr. 2009.

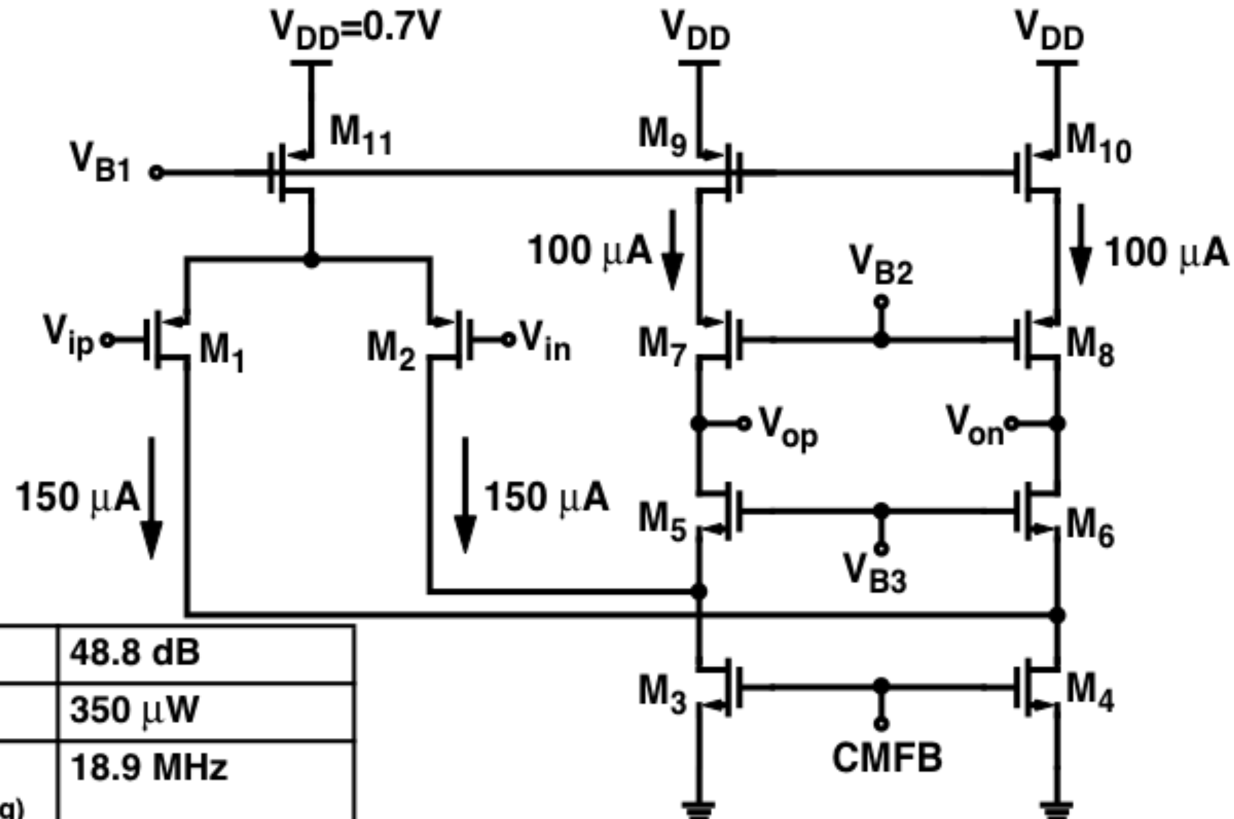


Modulator Implementation



*Actual implementation is fully differential

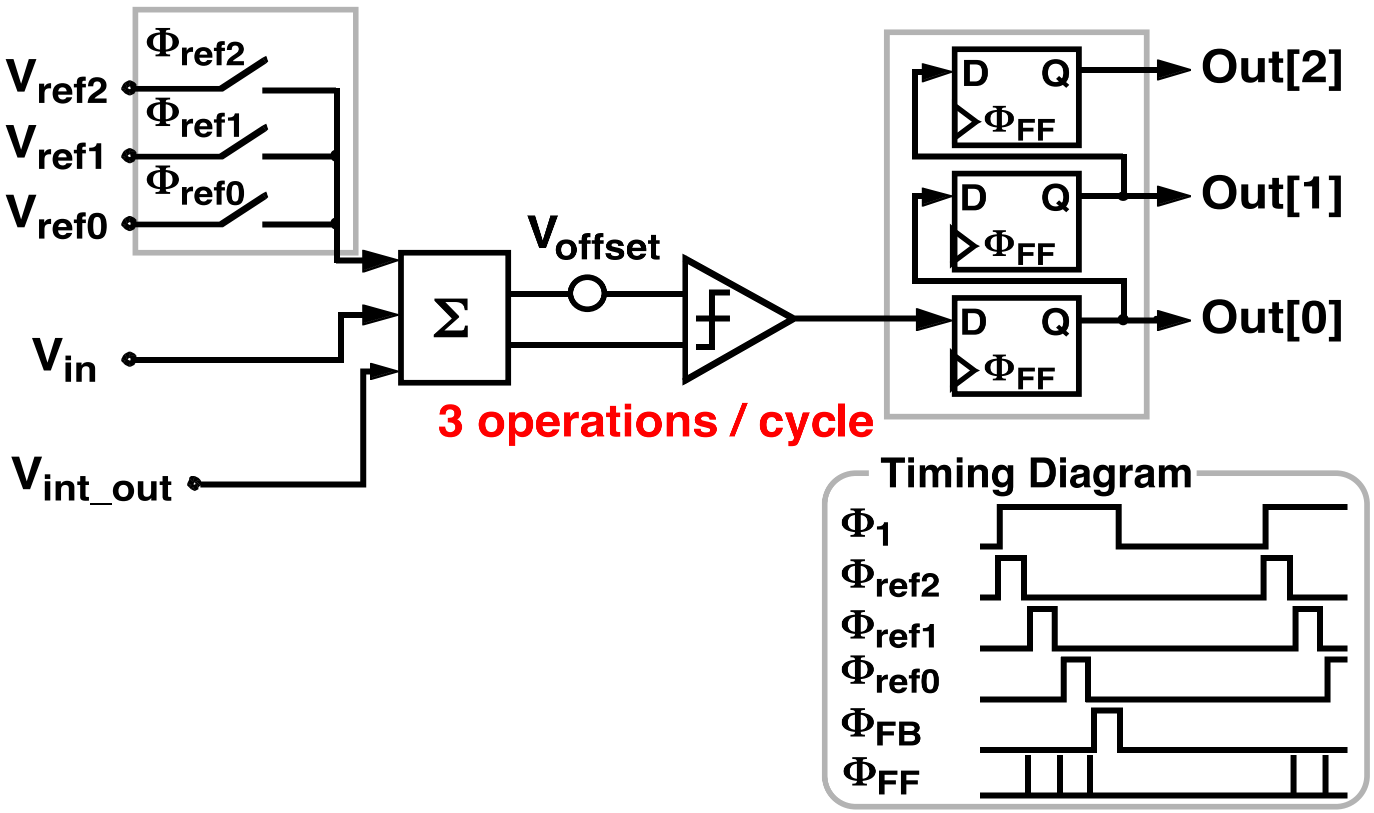
First Integrator Op Amp



DC Gain	48.8 dB
Power	350 µW
BW_u (@ 18pF loading)	18.9 MHz
V_{CM}	0V (Input), 0.35V (Output)

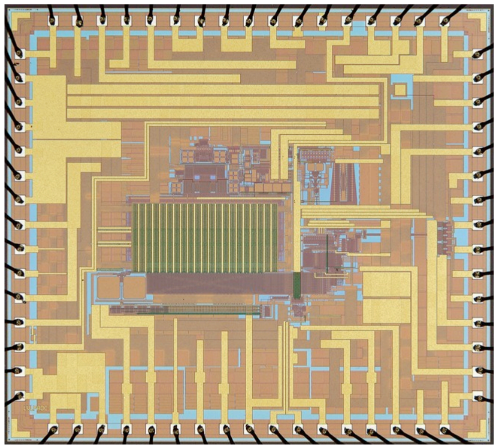
- **Incomplete, but linear, settling in op amp ⇨ low power**

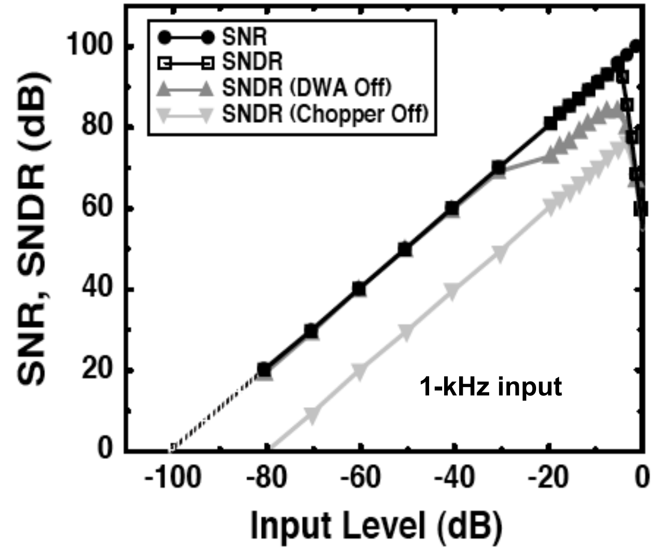
Single Comparator Tracking Quantizer



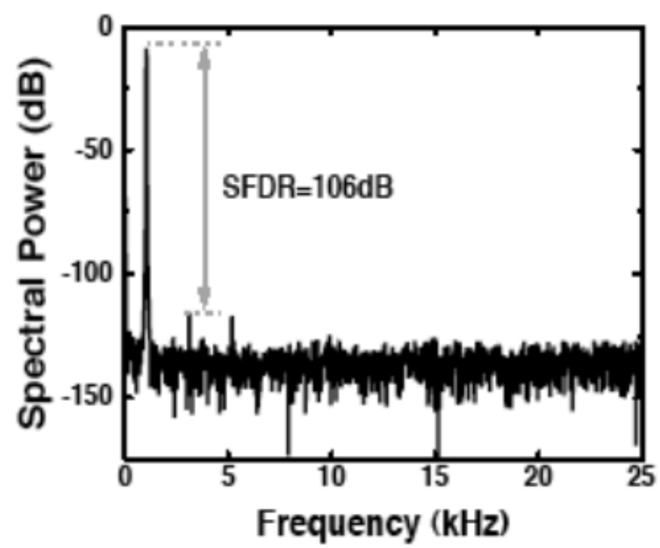
- No comparator offset mismatch problem
- Smaller area and reduced integrator loading
- But timing constraints are difficult when combined with input feedforward

Modulator Performance





Supply Voltage	0.7 V
Sampling Rate	5 MHz
References	0 V, 0.7 V
Signal Bandwidth	25 kHz
Dynamic Range	100 dB
Peak SNR	100 dB
Peak SNDR	95 dB
Power: Analog Digital	680 μW 190 μW
Area (excluding decoupling capacitors, pads & output drivers)	2.16 mm^2
Technology	0.18-μm CMOS



ADC Figure of Merit

$$\text{FoM} = \frac{\text{Power}}{2 * \text{BW} * 2^{2N}}$$

Note the 2N

where N is the peak SNDR in equivalent bits

Williams	0.226 fJ/step
Rabii	0.024 fJ/step
Park	0.0083 fJ/step

Some References

1. W. Kester, *ADC Architectures III: Sigma-Delta ADC Basics,* Analog Devices Tutorial MT-022.
2. W. Kester, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices Tutorial MT-023.
3. S. K. Tewksbury and R. W. Hallock, "Oversampled, Linear Predictive and Noise-Shaping Coders of Order N>1," *IEEE Trans. Circuits and Sys.*, vol. CAS-25, pp. 436-447, July 1978.
4. S. R. Norsworthy, R. Schreier and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, 1997.
5. J. C. Candy and G. C. Temes, *Oversampling Delta-Sigma Converters*, IEEE Press, 1992.

Kester ADI Tutorials

ANALOG DEVICES

MT-022 TUTORIAL

ADC Architectures III: Sigma-Delta ADC Basics

by Walt Kester

INTRODUCTION

The sigma-delta (Σ-Δ) ADC is the converter of choice for modern voiceband, audio, and high-resolution precision industrial measurement applications. The highly digital architecture is ideally suited for modern fine-line CMOS processes, thereby allowing easy addition of digital functionality without significantly increasing the cost. Because of its widespread use, it is important to understand the fundamental principles behind this converter architecture.

Due to the length of the topic, the discussion of Σ-Δ ADCs requires two tutorials, MT-022 and MT-023. This first tutorial (MT-022) first discusses the history of Σ-Δ and the fundamental concepts of oversampling, quantization noise shaping, digital filtering, and decimation. Tutorial MT-023 discusses more advanced topics related to Σ-Δ, including idle tones, multi-bit Σ-Δ ADCs, multistage noise shaping Σ-Δ ADCs (MASH), bandpass Σ-Δ ADCs, as well as some example applications.

HISTORICAL PERSPECTIVE

The Σ-Δ ADC architecture had its origins in the early development phases of pulse code modulation (PCM) systems—specifically, those related to transmission techniques called *delta modulation* and *differential PCM*. (An excellent discussion of both the history and concepts of the Σ-Δ ADC can be found by Max Hauser in Reference 1). Delta modulation was first invented at the ITT Laboratories in France by E. M. Deloraine, S. Van Mierlo, and B. Derjavitch in 1946 (References 2, 3).

The principle was "rediscovered" several years later at the Phillips Laboratories in Holland, whose engineers published the first extensive studies both of the single-bit and multi-bit concepts in 1952 and 1953 (References 4, 5). In 1950, C. C. Cutler of Bell Telephone Labs in the U.S. filed an important patent on differential PCM which covered the same essential concepts (Reference 6).

The driving force behind delta modulation and differential PCM was to achieve higher transmission efficiency by transmitting the *changes* (delta) in value between consecutive samples rather than the actual samples themselves.

In *delta modulation*, the analog signal is quantized by a one-bit ADC (a comparator) as shown in Figure 1A. The comparator output is converted back to an analog signal with a 1-bit DAC, and subtracted from the input after passing through an integrator. The shape of the analog signal is transmitted as follows: a "1" indicates that a positive excursion has occurred since the last sample, and a "0" indicates that a negative excursion has occurred since the last sample.

ANALOG DEVICES

MT-023 TUTORIAL

ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications

by Walt Kester

INTRODUCTION

Tutorial MT-022 discussed the basics of Σ-Δ ADCs. In this tutorial, we will look at some of the more advanced concepts including idle tones, multi-bit Σ-Δ, MASH, bandpass Σ-Δ, as well as some example applications.

IDLE TONE CONSIDERATIONS

In our discussion of Σ-Δ ADCs up to this point, we have made the assumption that the quantization noise produced by the Σ-Δ modulator (see Figure 1) is random and uncorrelated with the input signal. Unfortunately, this is not entirely the case, especially for the first-order modulator. Consider the case where we are averaging 16 samples of the modulator output in a 4-bit Σ-Δ ADC.

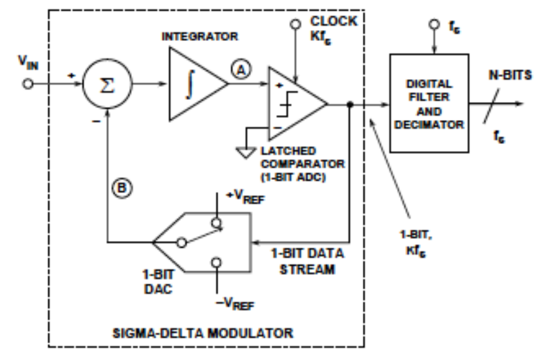


Figure 1: First-Order Sigma-Delta ADC

Figure 2 shows the bit pattern for two input signal conditions: an input signal having the value 8/16, and an input signal having the value 9/16. In the case of the 9/16 signal, the modulator output bit pattern has an extra "1" every 16th output. This will produce energy at $Kf_s/16$, which translates into an unwanted tone. If the oversampling ratio (K) is less than 8, this tone will fall