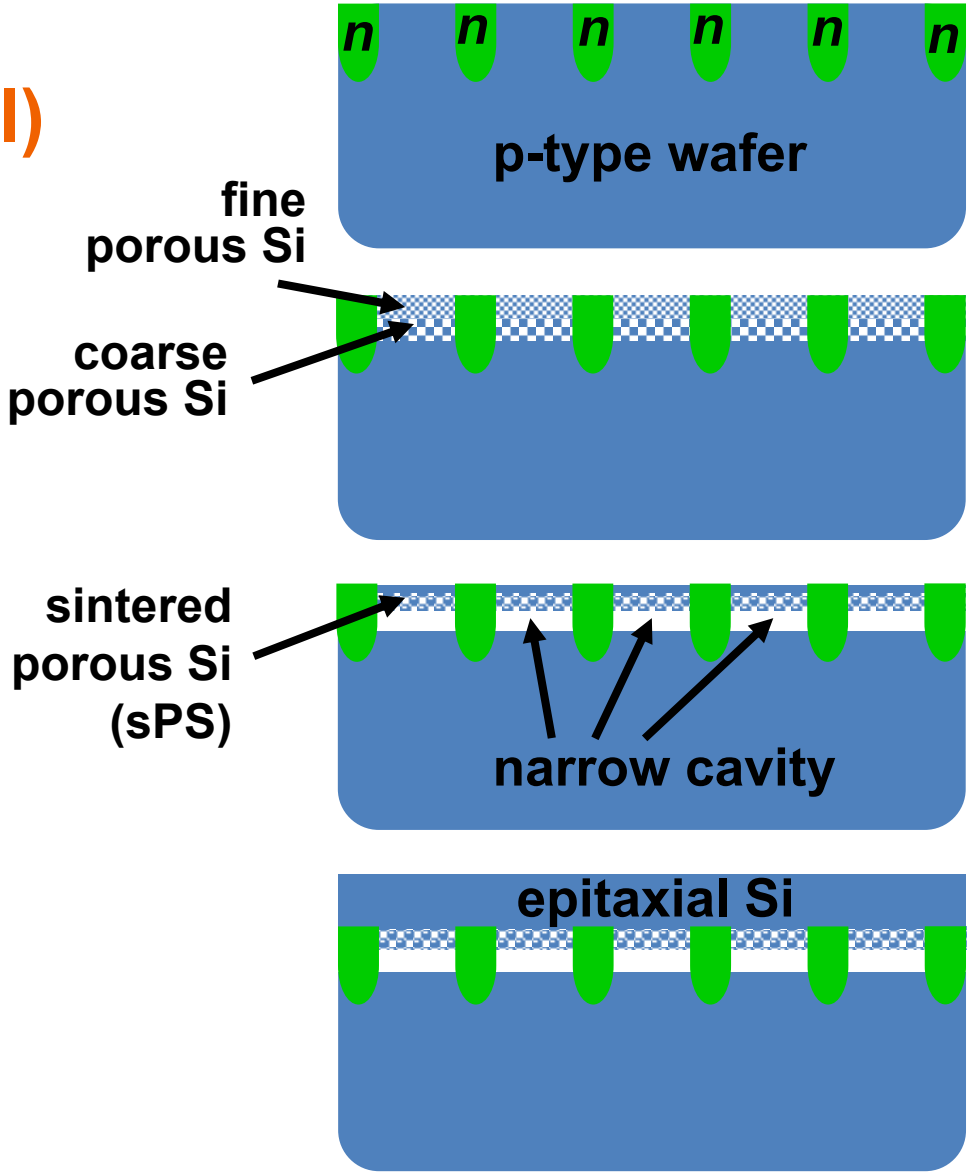
# Chipfilm™-II Technology Process

- **Pre-process module (I)**
  - n-implant
  - anodic etching
  - thermal annealing
  - epitaxial growth
- **Device Integration**
- **Post-process module**
  - Trench etching
  - Chip detachment



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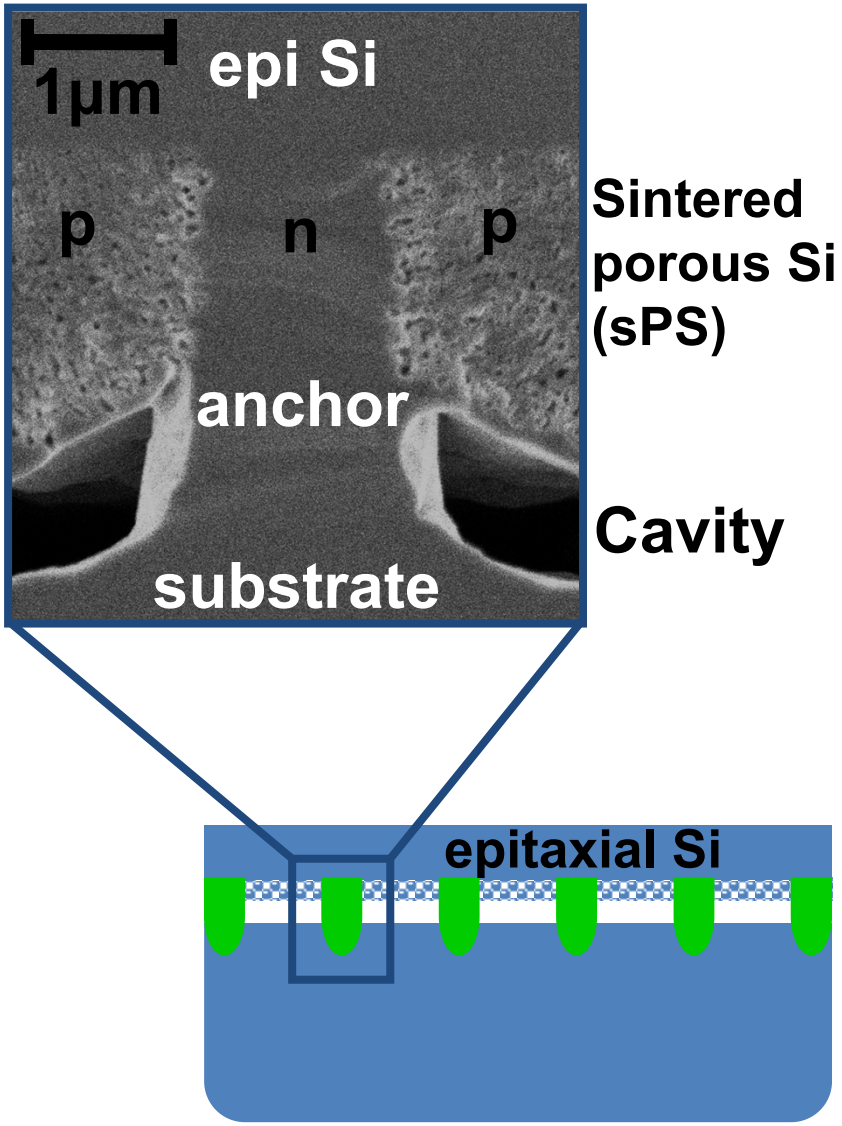

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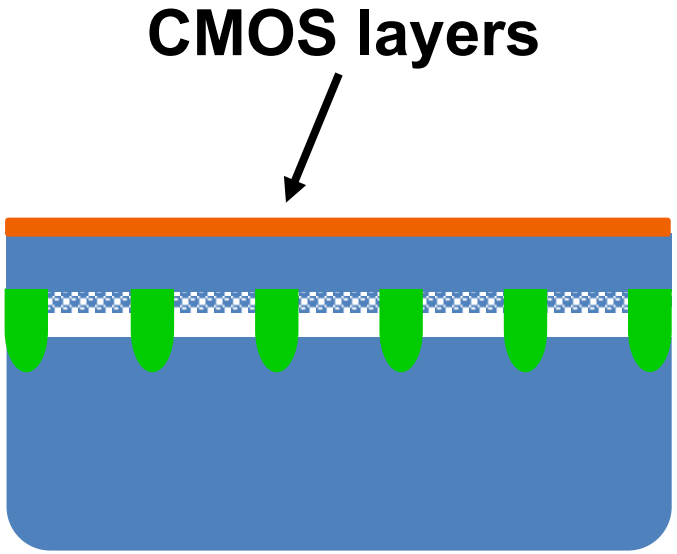

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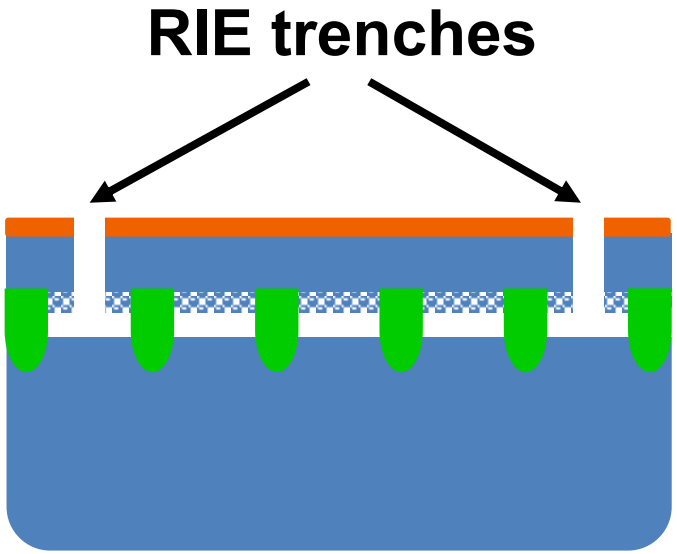

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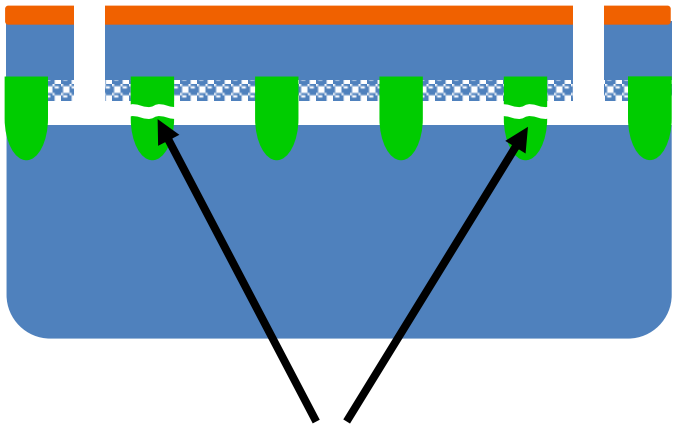

fracture of specific anchors (weak attachment)

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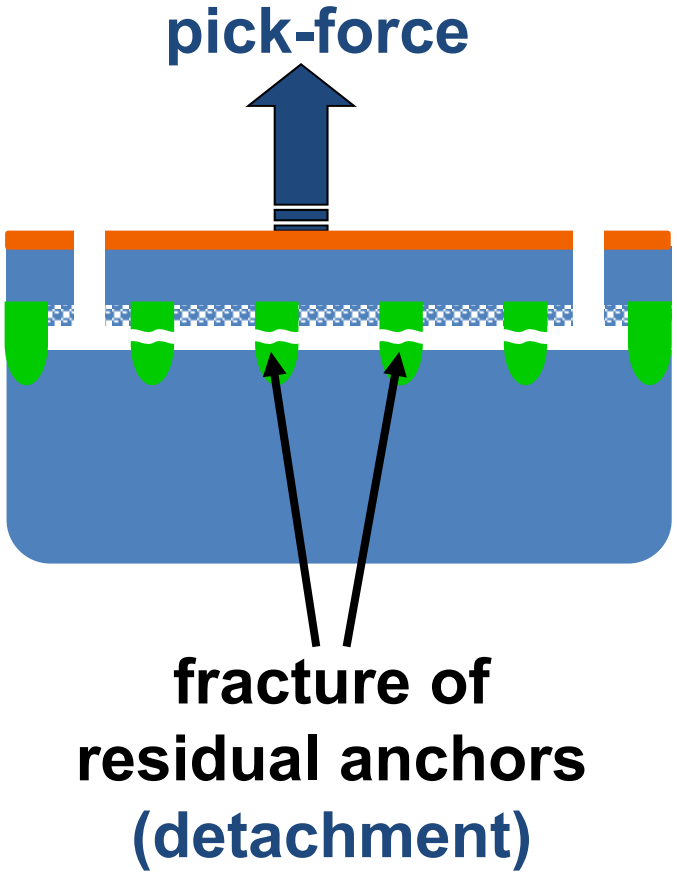

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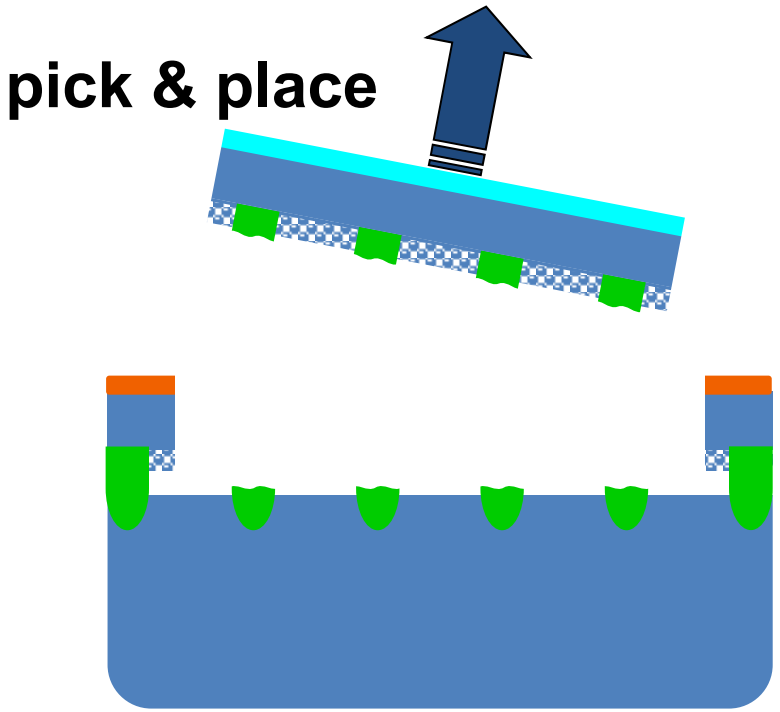

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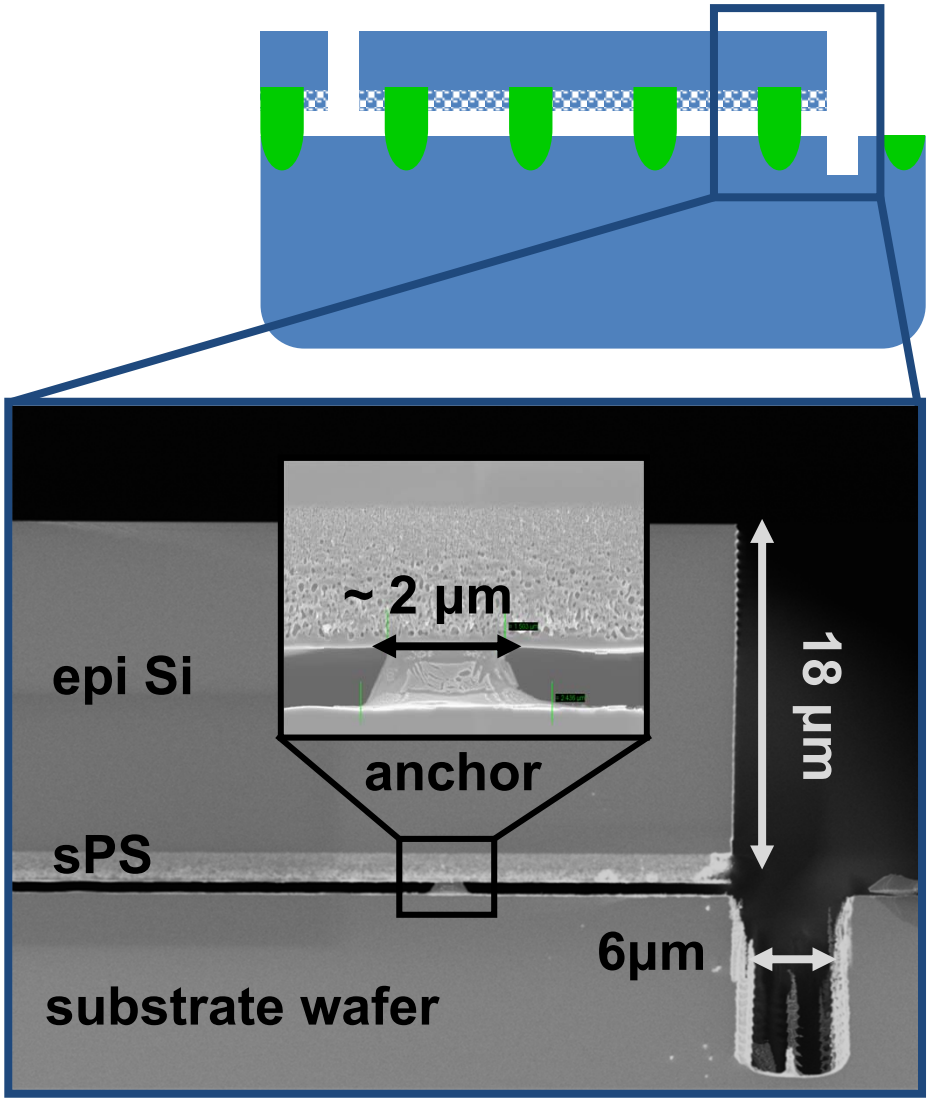
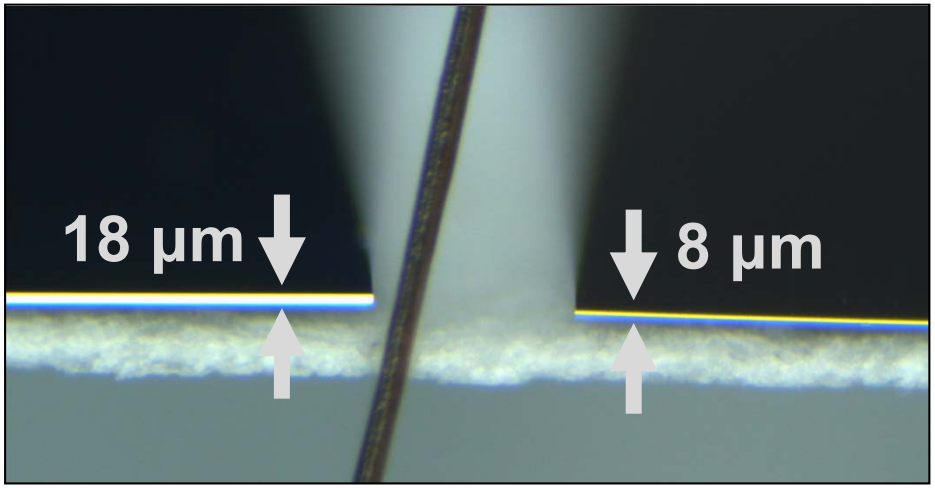
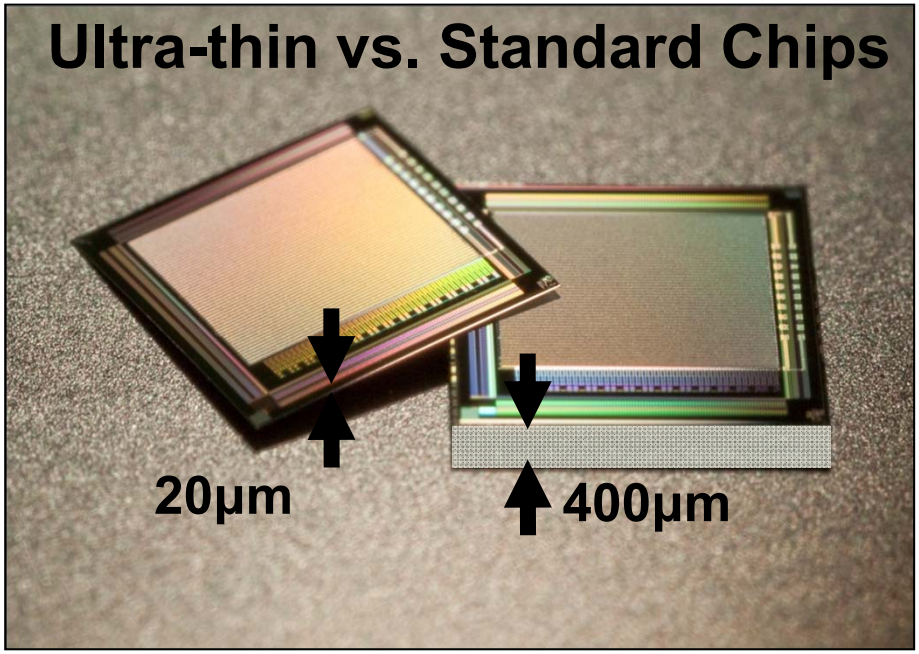


# Fabricated Ultra-Thin Chips

- **Blanket Si wafers**
  - 675 µm
- **Blanket Chipfilm™ dies**
  - 18 µm
  - 8 µm




- **0.8 µm CMOS bulk wafers**
  - 675 µm initial thickness
  - 400 µm after back-grinding
- **Chipfilm™ IC chips**
  - 20 µm

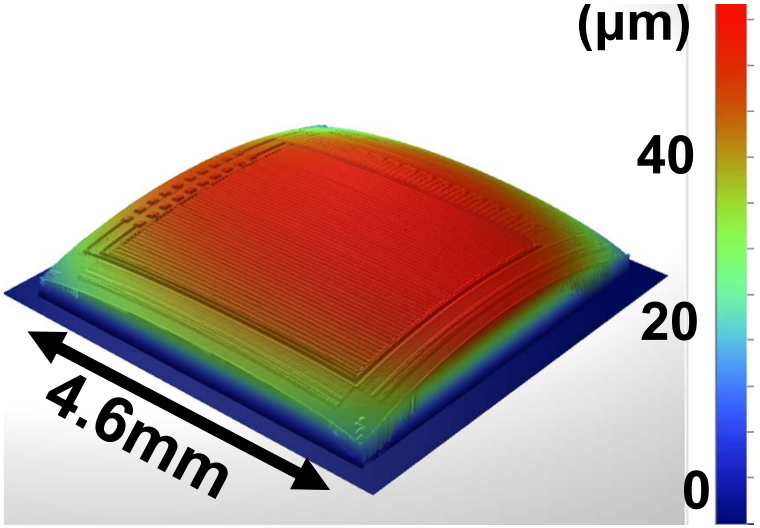
# Process Window (I)

- ✓ Stable anchors during wafer processing
- ✓ Controlled anchor fracture for chip detachment
  - Process Induced Stress (PIS)
  - Externally Induced Stress (EIS)
  - Force from pick & place tool

- **Sources of PIS**
  - Rapid thermal processing
  - Wafer bow
  - Mismatch of CMOS layers

    → thin chip warpage

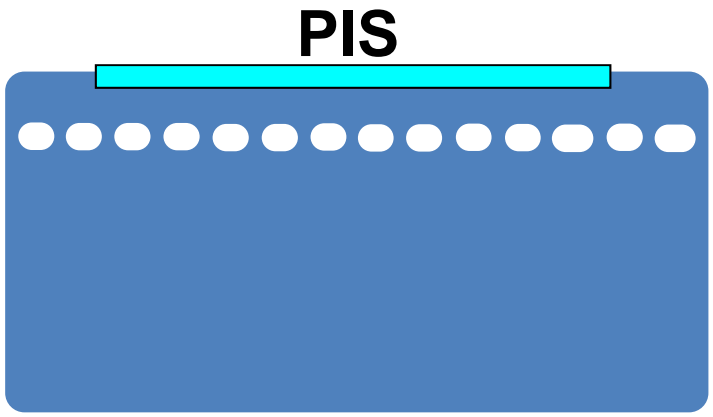
**Warped 20 µm IC chip**



# Process Window (II)

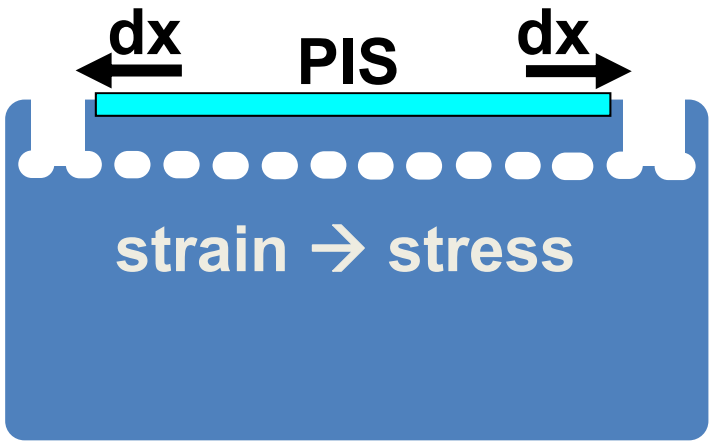
- **Before** etching the separation trenches
  - Anchors are enclosed by substrate and device layers

    → Anchors are shielded from stress

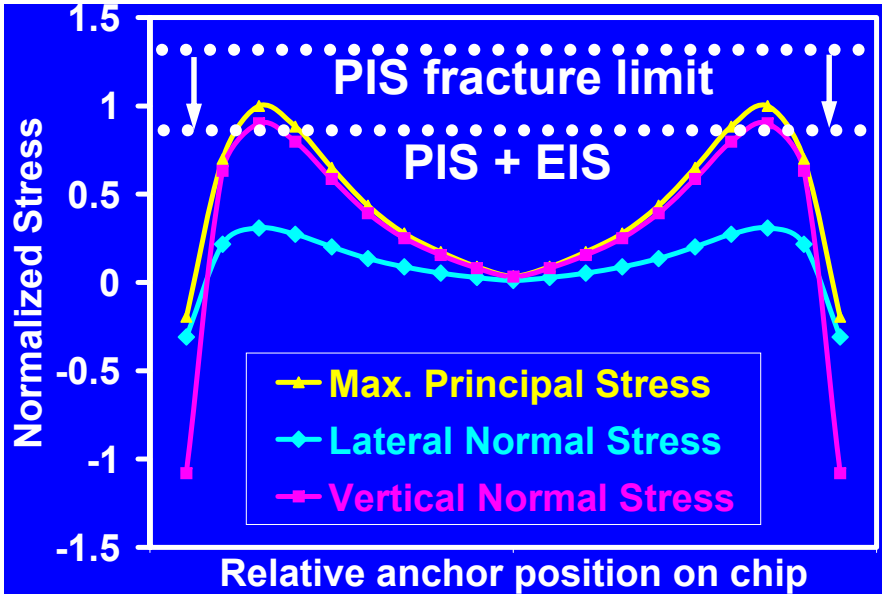


# Process Window (II)

- Before etching the separation trenches
  - Anchors are enclosed by substrate and device layers
    - → Anchors are shielded from stress
- **After etching of separation trenches**
  - **Free lateral space for chip deformation due to PIS**
    - **→ High stress on anchors**

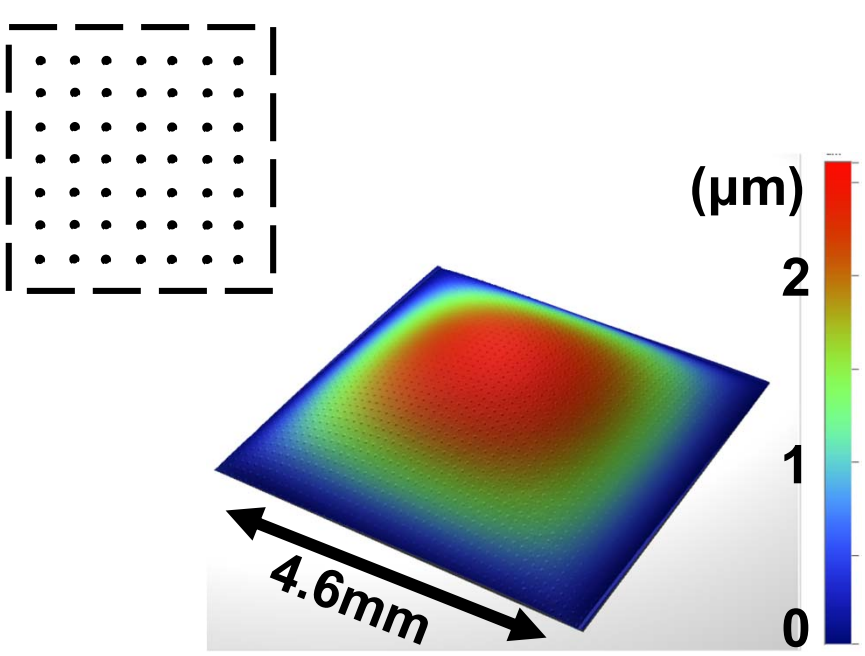


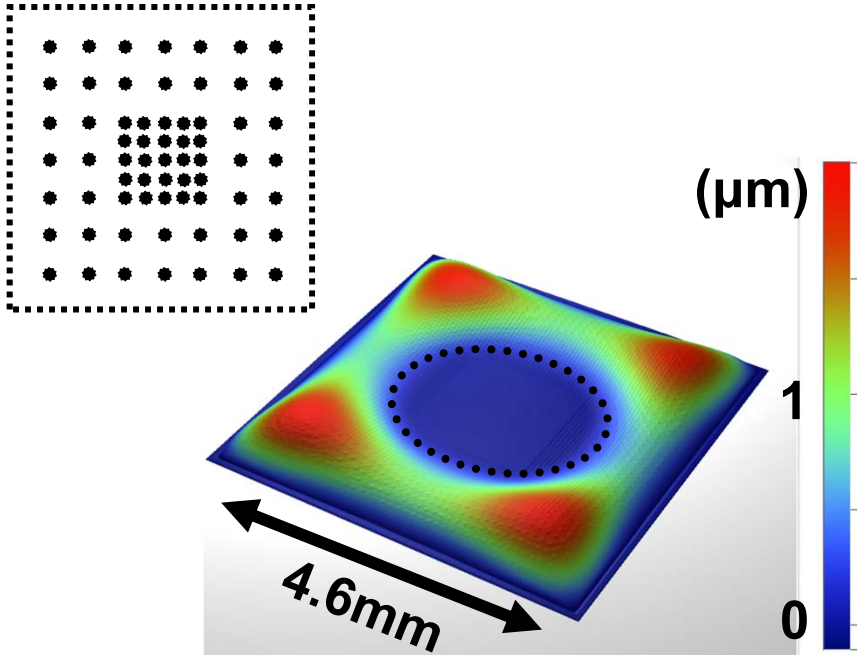

**2D-FEM simulation (ANSYS)**



# Process Window (III)

- **Uniform anchor array**
  - **After EIS remaining:**
    - **Outer ring of anchors**
  - **Used for generic wafers**
- **Non-uniform anchor array**
  - **After EIS remaining:**
    - **Outer ring of anchors**
    - **Inner group of anchors**
  - **Pre-defined chip locations**



# Process Window (IV)

| Diameter (µm) | Pitch (µm) | Trenching chip loss | Pick-yield (before EIS) | Pick-yield (after EIS) |
|---|---|---|---|---|
| | | target: 0% | target: 100% | target: 100% |
| 1.0 | 25 | 0% | 0% | 16% |
| 1.0 | 50 | 0% | 2% | > 99% |
| 1.0 | 100 | ~ 10% | - | - |
| 1.0 | 100/50/25 | 0% | 3% | > 99% |

- **Pick-yield depends on:**
  - Design and pitch of anchor array
  - Anchor dimensions (diameter)
  - PIS (technology, chip thickness, layout)

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- **Pick-yield depends on:**
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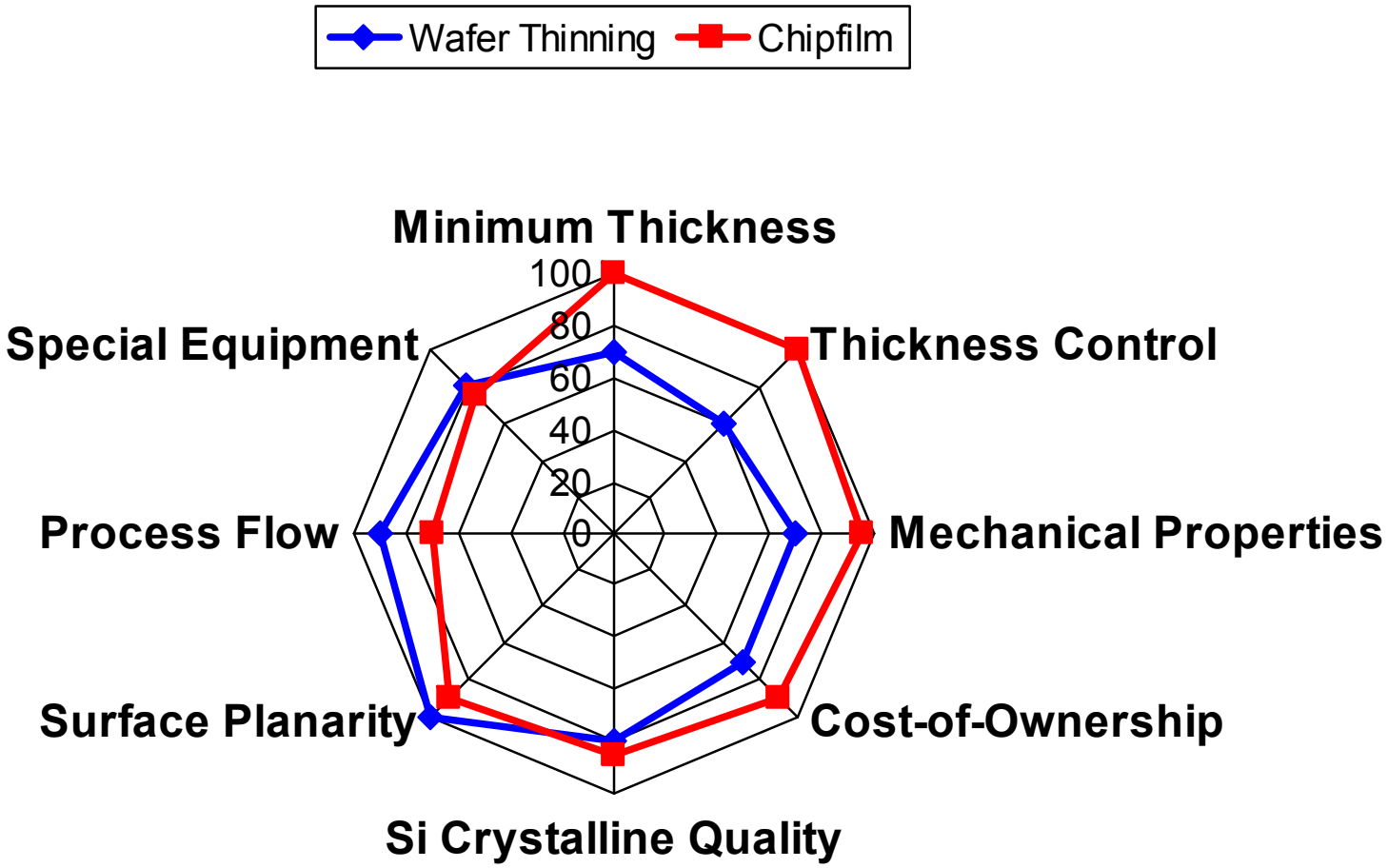
  - PIS (technology, chip thickness, layout)

✓ EIS is essential for maximum pick-yield

# Benchmarking




→ Technologies have different advantages

→ Chipfilm™ will likely be aiming at applications different from wafer thinning

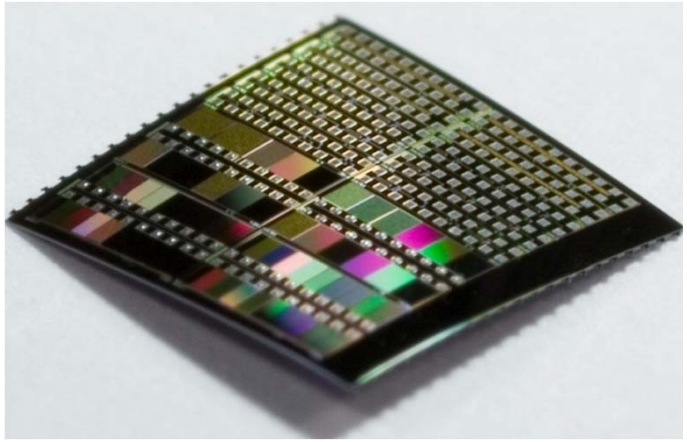
# Outline

- Ultra-thin chips: the paradigm shift
- Applications of ultra-thin chips
  - Traditional, recent and potential future applications
  - 3D ICs: Overcoming a bottleneck in CMOS scaling
  - Systems-in-Foil (SiF): enabler for new applications
- Ultra-thin chip fabrication
  - Post-process wafer thinning
  - Thin chips based on SOI
  - Chipfilm™ technology
- **Characteristics of ultra-thin chips**
  - **Warpage of thin chips**
  - Mechanical stability of thin chips
  - Apparently anomalous piezoresistive effect
- Constraints for circuit design
- Conclusions

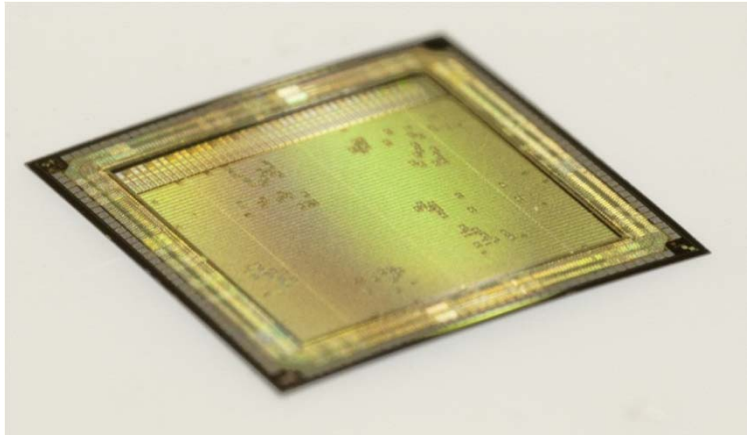
# Thin Chip Warpage (I)

- **Chip warpage becomes substantial if die is extremely thin**
  - Packaging becomes increasingly difficult
  - Piezoresistive offset due to warpage
- **Degree of warpage depends on chip layout**
  - Opportunity to tailor warpage
    - by suitable layout ground rules
    - through layer and structural stress management

*ESTC 2010*

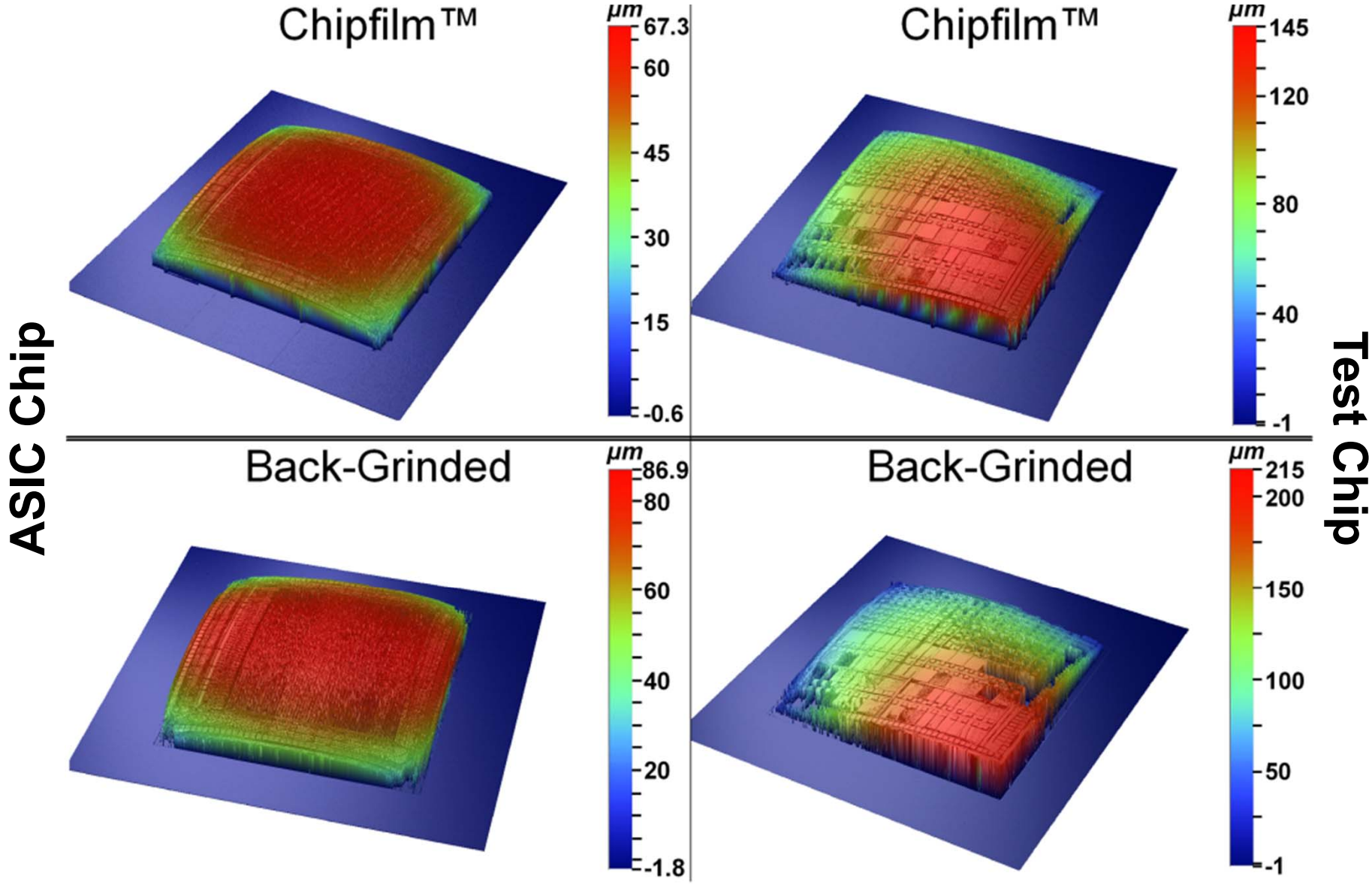


Test Chip



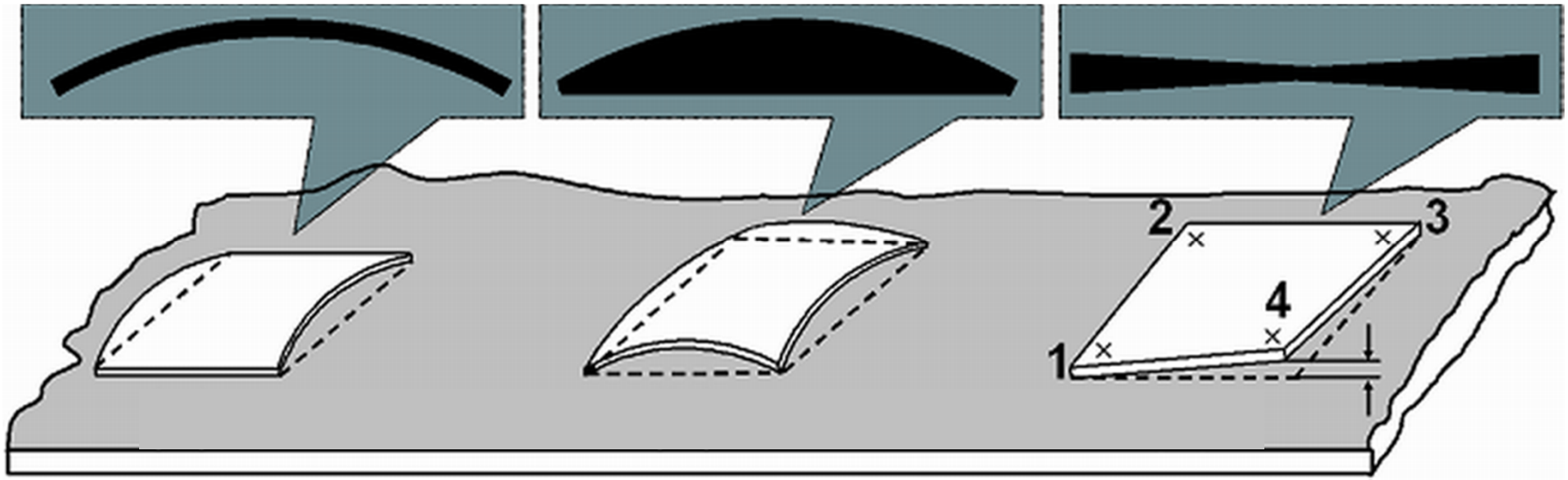
Product Chip

# Thin Chip Warpage (II)



# Thin Chip Warpage (III)

**Cylindrical** **Spherical** **Twist**




| | Product Chip | Test Chip |
|---|---|---|
| Chipfilm™ | Spherical | Twist & Spherical |
| | d ~ 65 µm | d ~ 145 µm |
| Back-Grinded | Spherical & Cylindrical | Twist & Spherical |
| | d ~ 85 µm | d ~ 200 µm |

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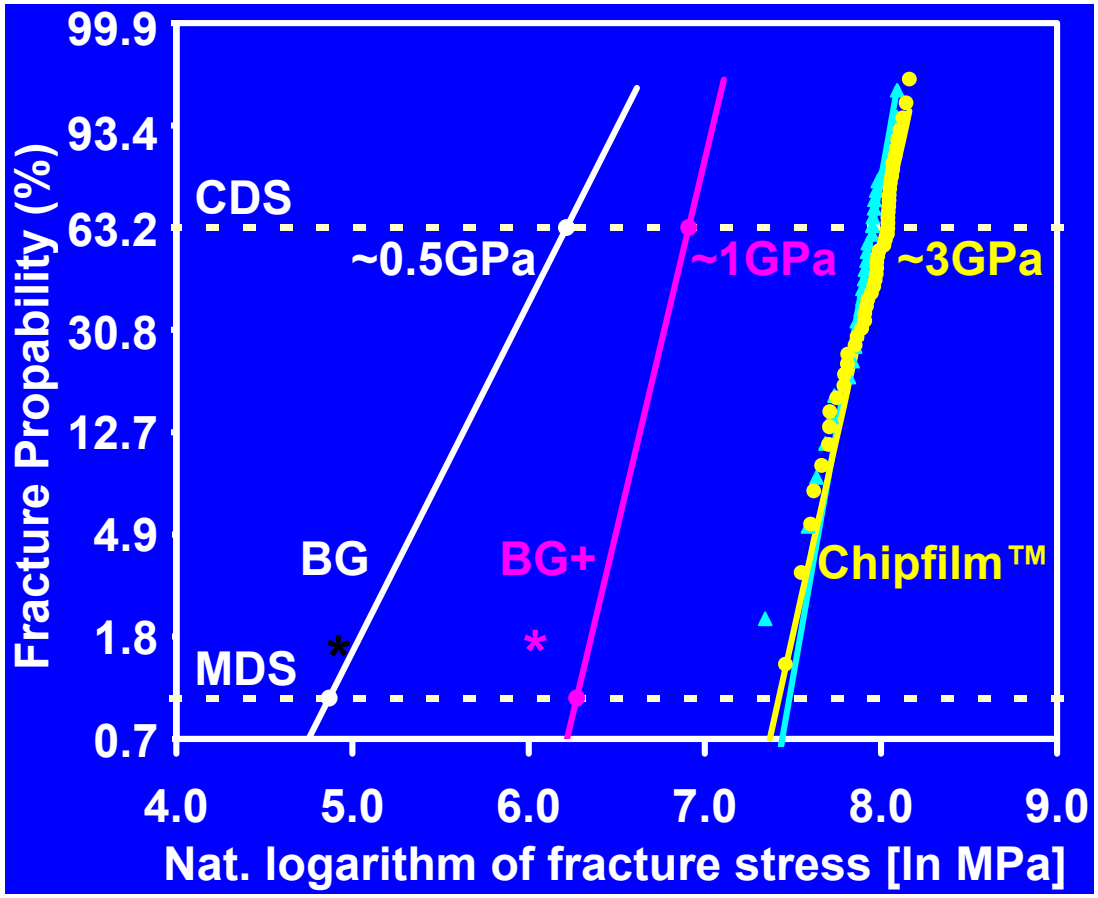
# Mechanical Chip Stability




**50µm back-grinded (BG)***

**50µm back-grinded with plasma etch-relief (BG+)***

**20µm Chipfilm™ IC layer**

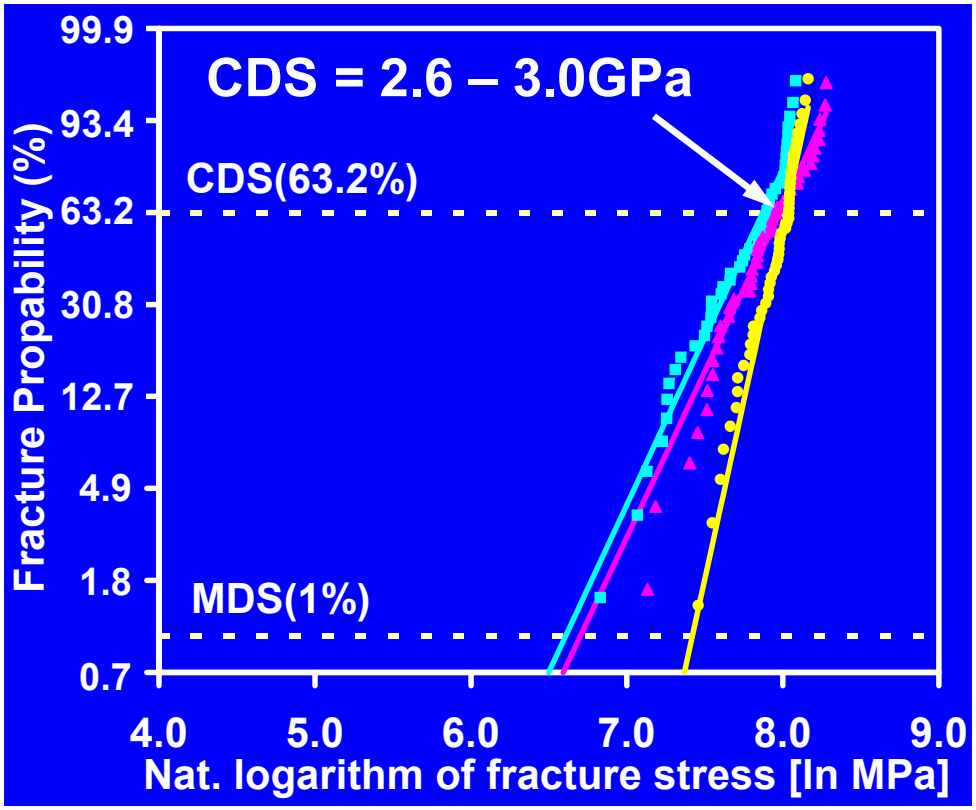
**18µm Chipfilm™ bare Si**

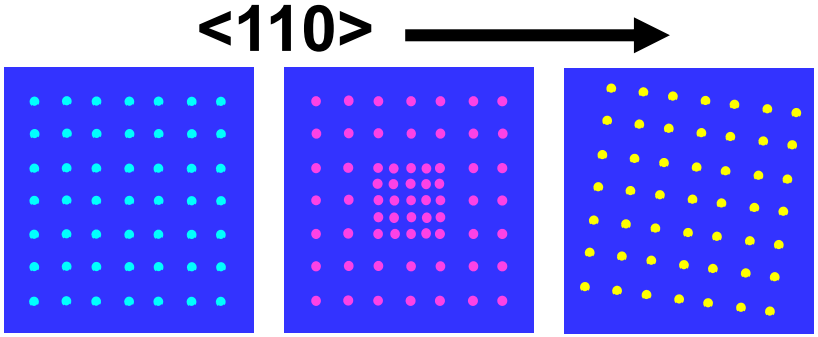
* **P. M. Heinze, Int. Forum *be-flexible*, Munich, 2008 (data trend lines).**

✓ **Chipfilm™ technology offers superior chip stability**

***IEDM 2010***

# Mechanical Chip Stability




pitch = 50µm (rot = 0°)

pitch = 100-50-25µm (rot = 0°)

pitch = 50µm (rot = 3°)

✓ Anchor array design has little effect on chip stability

*IEDM 2010*

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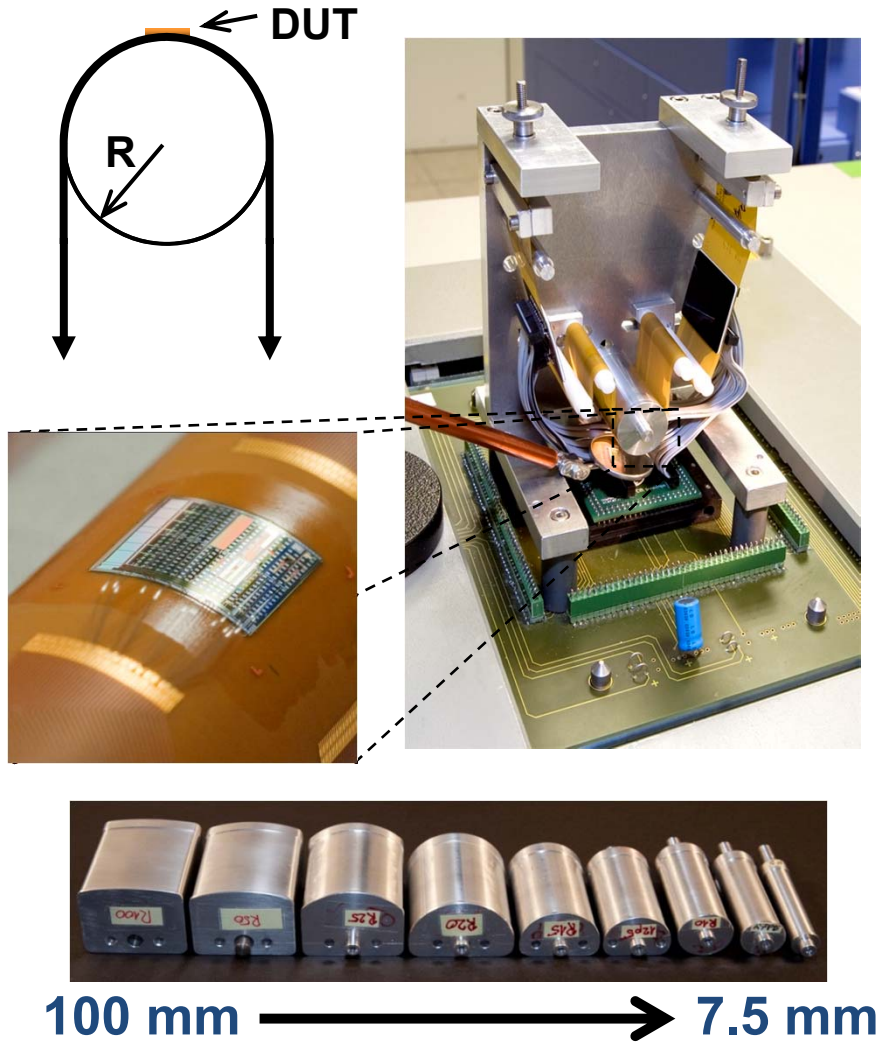
# Piezoresistive Effect (I)

## Issues with thin chip testing:

- 4-point beam bending not applicable
  - Extremely small dimensions
  - Non-linear effects

## Approach:

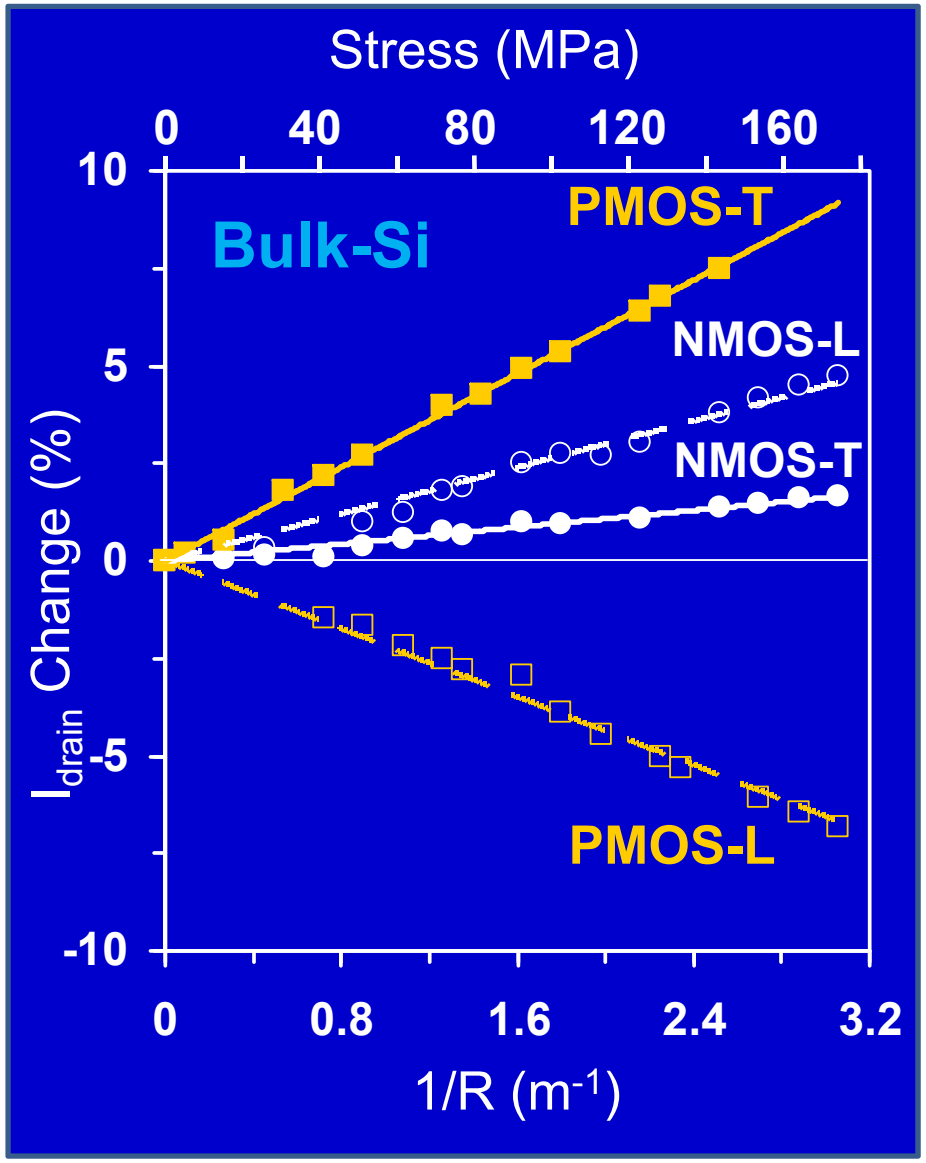
- Chip-tape glue assembly
- DUT bent to radius (R)
- Consistent with application
- Sample-sample variation
- Apparent stress at chip surface unknown

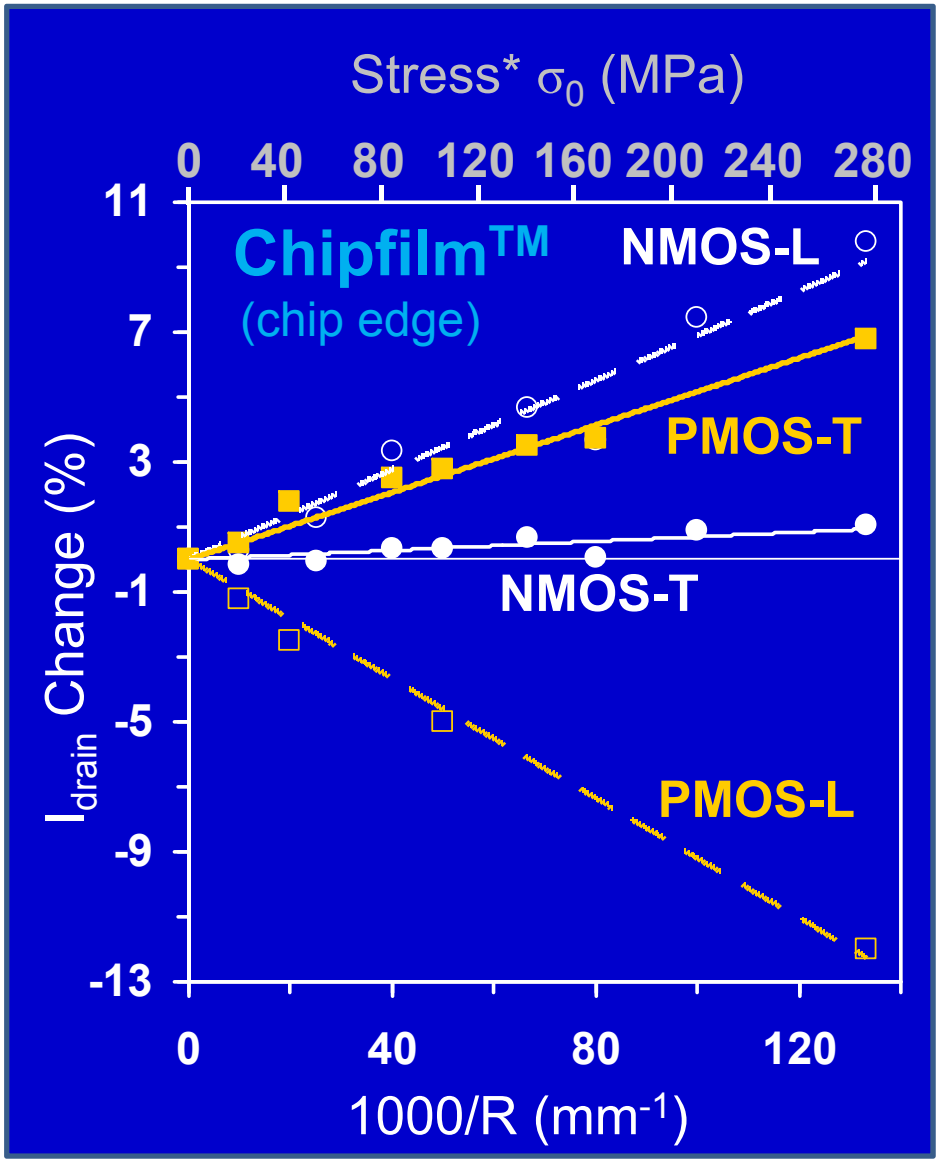



✓ **Apparent piezoresistive effect likely affected by assembly**

*IEDM 2009*

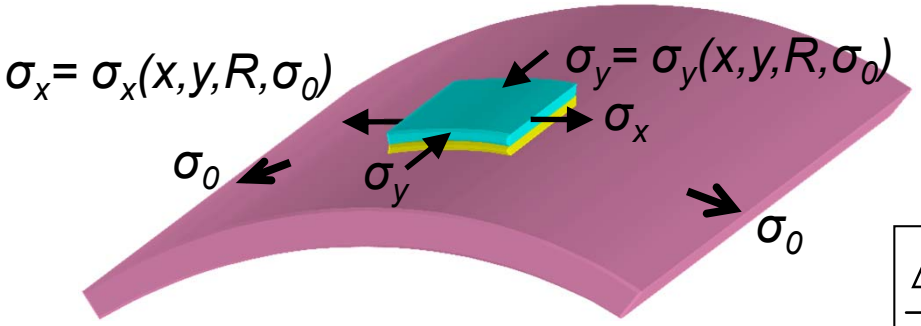
# Piezoresistive Effect (II)



# Piezoresistive Effect (III)

- **Different piezoresistive characteristics for Chipfilm™ vs. Bulk-Si**
  - Apparent superposition of biaxial stress components
  - Viscoelastic glue transforms uniaxial into biaxial stress




$$\frac{\Delta I_D}{I_D} = \Pi \cdot \sigma$$

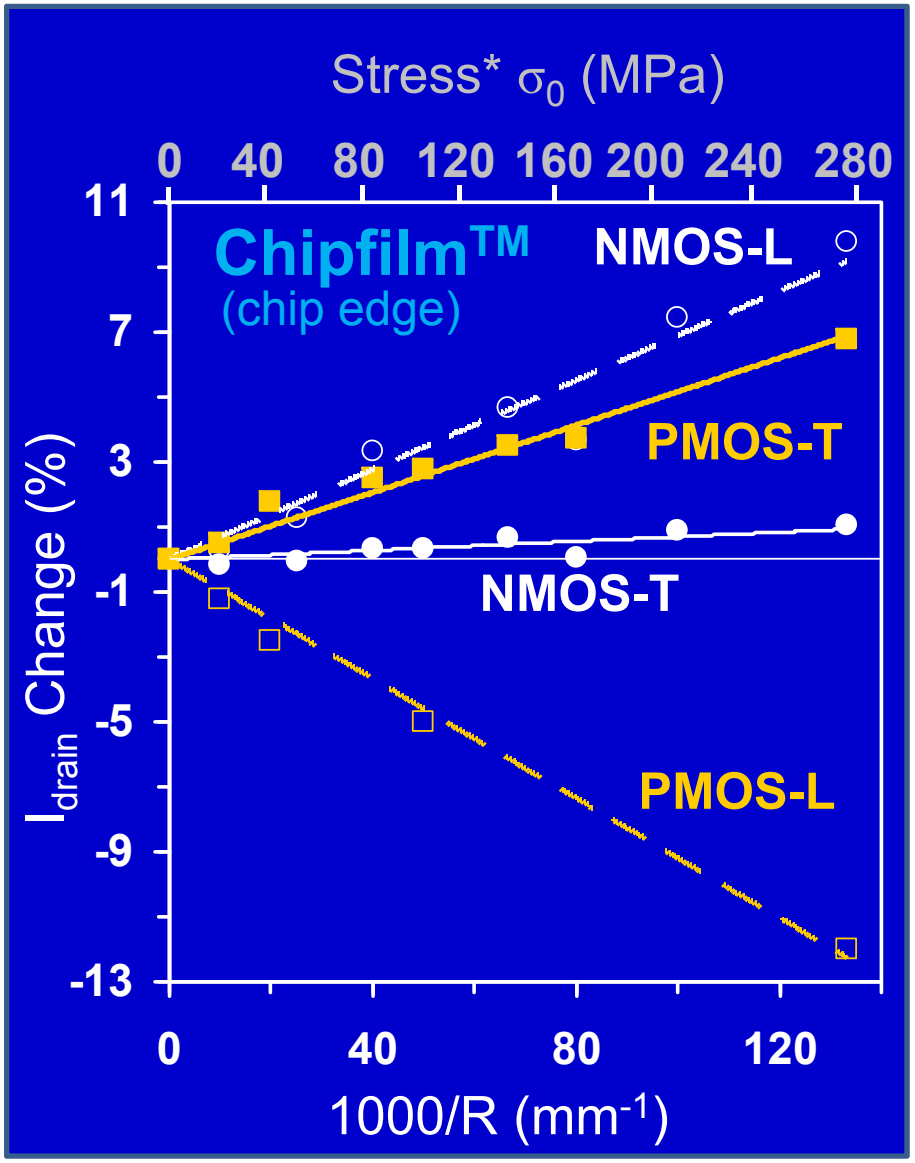
$$\Pi_L^* = \Pi_L - \nu \cdot \Pi_T$$

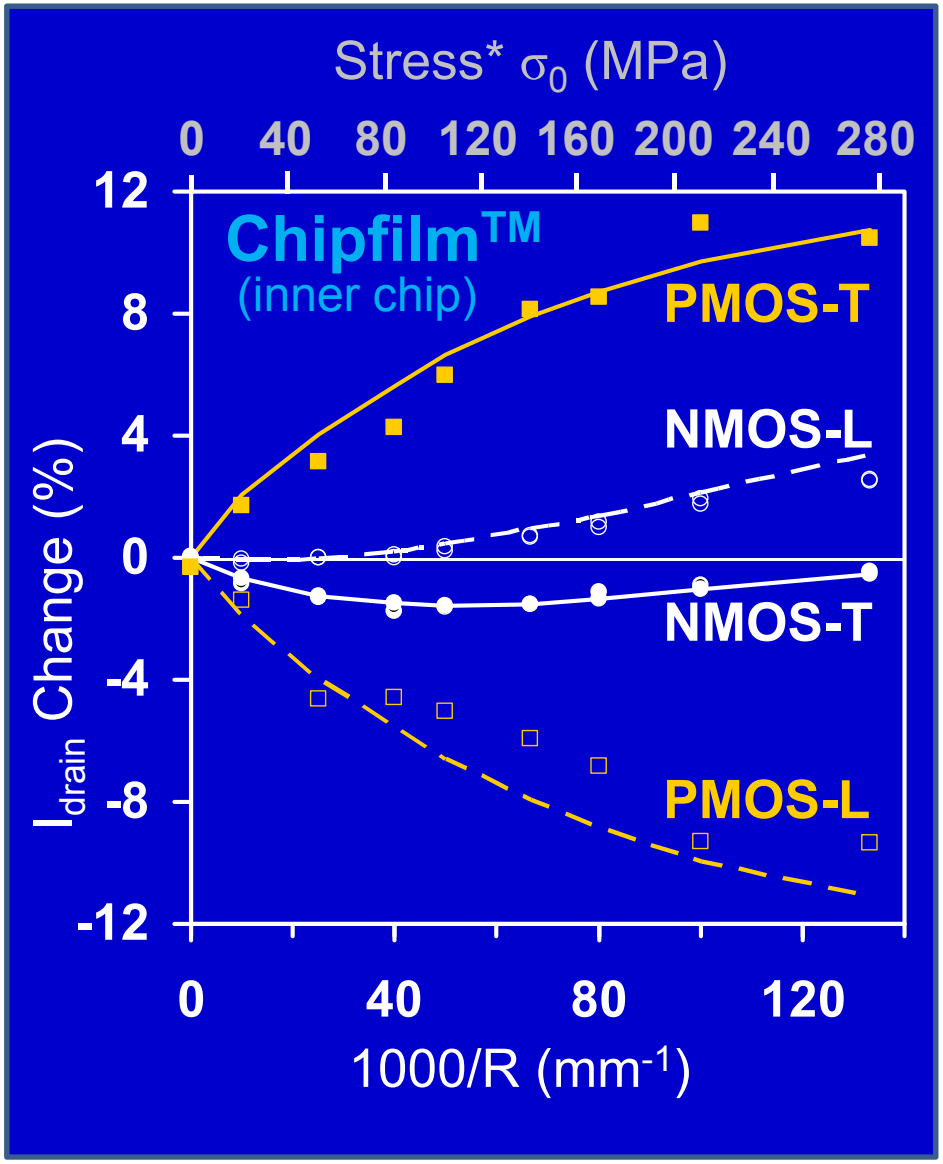
$$\Pi_T^* = \Pi_T - \nu \cdot \Pi_L$$

- **Piezoresistive effect depends on location on chip**
  - Non-linear dependence $\Delta I_D/I_D$ vs. σ, i.e. Π not constant !?
    - Stress offsets $\Delta\sigma_x$ and $\Delta\sigma_y$ from flat assembly of warped chip
    - Offset $\Delta\sigma_x$ changes in test set up while $\Delta\sigma_y$ does not !

*IEDM 2009*

# Piezoresistive Effect (IV)



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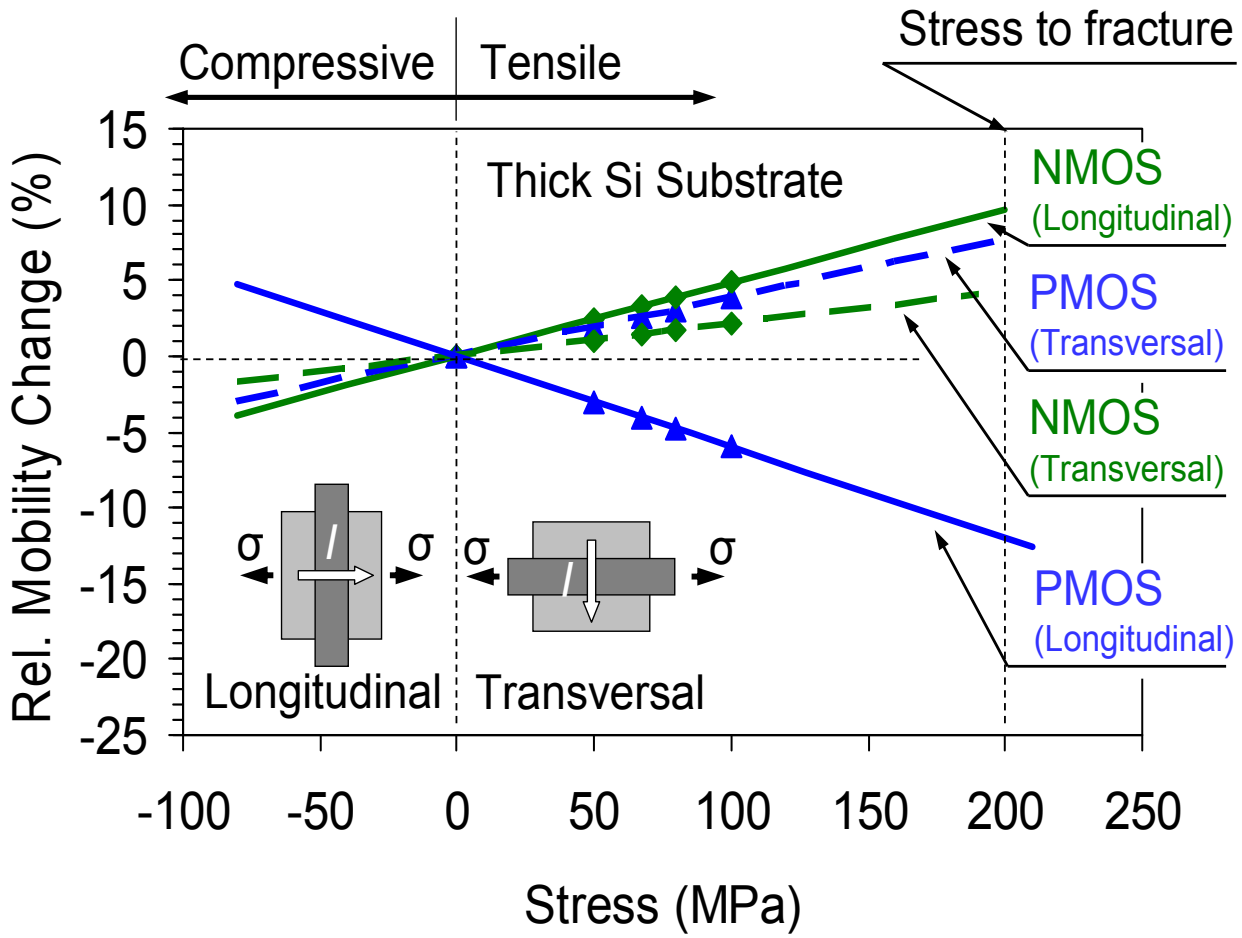
# Constraints on Circuit Design (I)




Strain: $\varepsilon = \frac{h_{Chip}}{2R}$

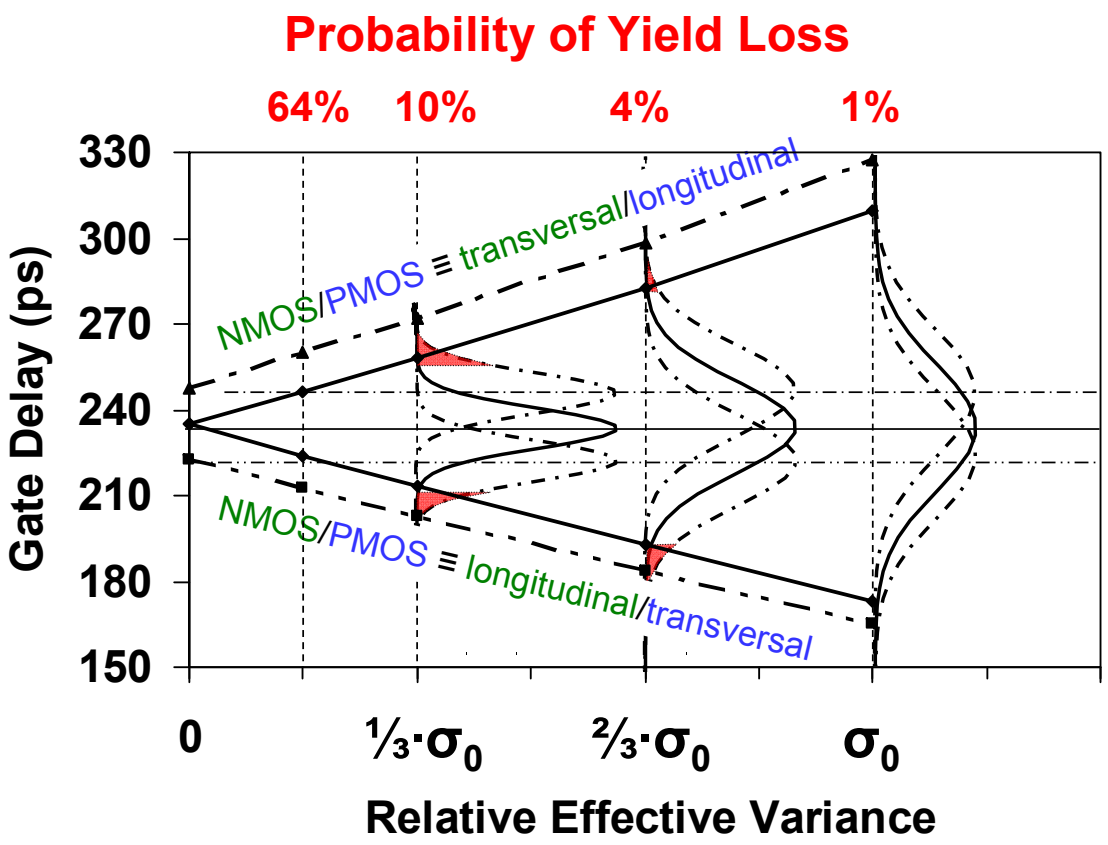
Stress: $\sigma = \varepsilon \cdot E$

$$\sigma = E \cdot \frac{h_{Chip}}{2R}$$

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta \mu}{\mu_0} \cong \Pi_{L,T} \cdot \sigma$$

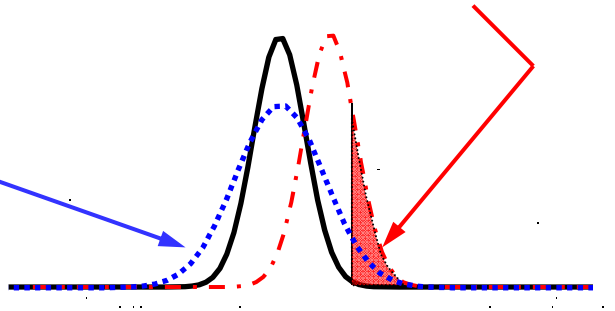
Here: $\prod_L (100)[011]; \prod_T (100)[011]$

# Constraints on Circuit Design (II)




Process-corner based design:

+ Piezoresistive effect:
→ Parameter shift



→ Parametric yield loss

→Eff. process tolerance σ has impact on yield loss !

2. Improvements:

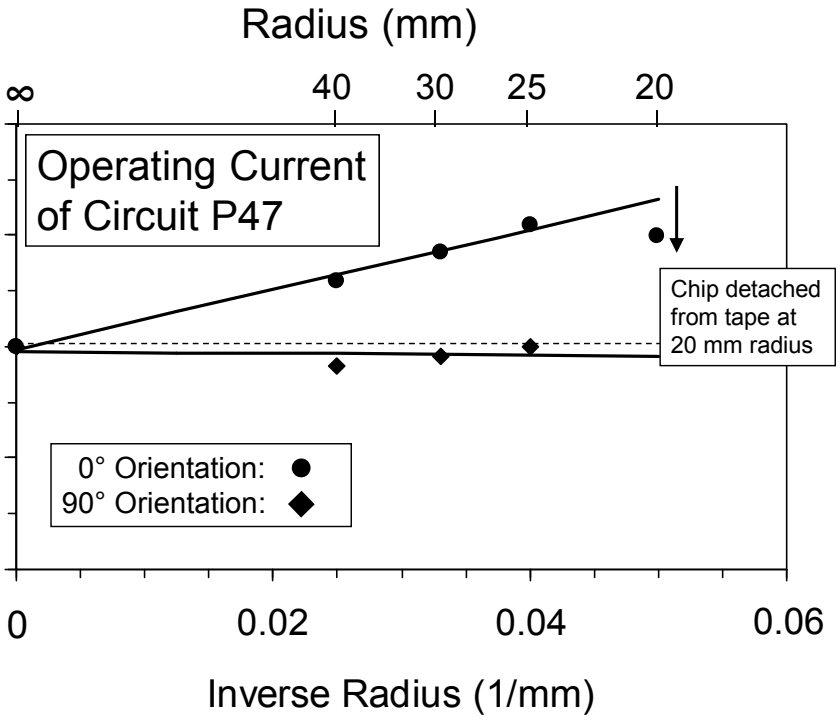
- ✓ Widened process corners
- ✓ Optimum FET layout
- ✓ Compensation by design

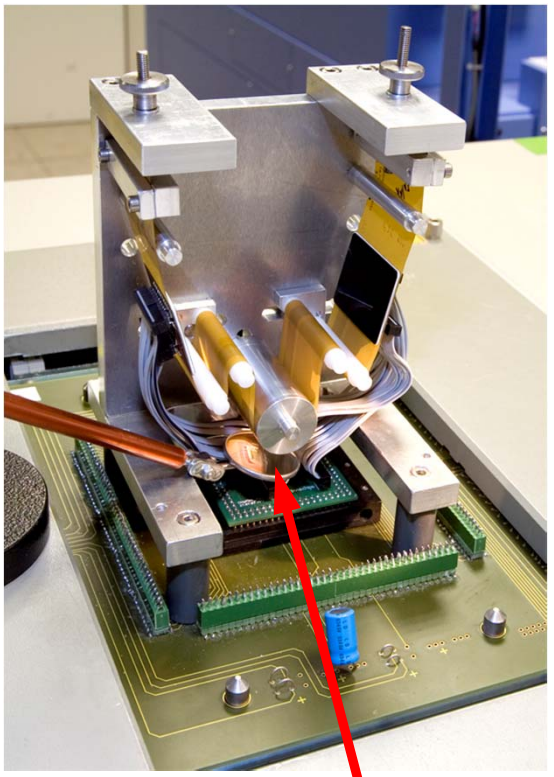
*ISSCC 2008*

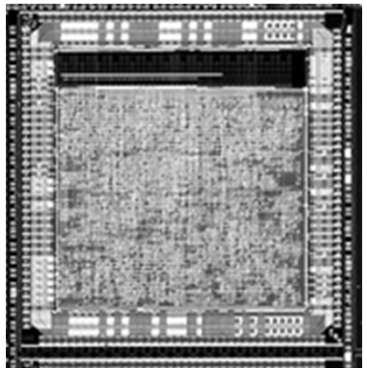
# Constraints on Circuit Design (III)

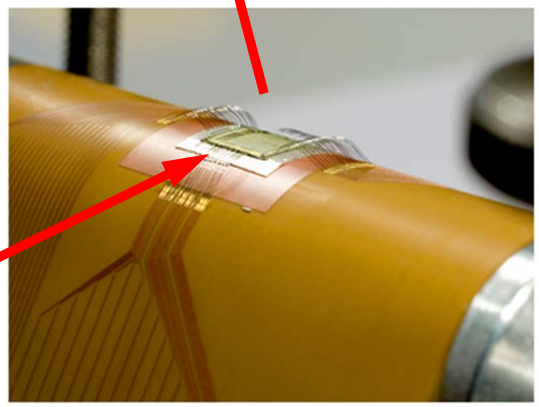
## Mixed-Signal Circuit P47:

- ✓ 38,000 digital FETs (0º)
- ✓ 2,700 analog FETs (90º)
- ✓ Standby current set by current source







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# Outline

- Ultra-thin chips: the paradigm shift
- Applications of ultra-thin chips
  - Traditional, recent and potential future applications
  - 3D ICs: Overcoming a bottleneck in CMOS scaling
  - Systems-in-Foil (SiF): enabler for new applications
- Ultra-thin chip fabrication
  - Post-process wafer thinning
  - Thin chips based on SOI
  - Chipfilm™ technology
- Characteristics of ultra-thin chips
  - Warpage of thin chips
  - Mechanical stability of thin chips
  - Apparently anomalous piezoresistive effect
- Constraints for circuit design
- **Conclusions**

# Conclusions

- Ultra-thin chips will help to overcome various bottlenecks and be the basis for new applications in silicon technologies.
- **But:** Ultra-thin chips and wafers call for new techniques in wafer and chip processing and handling.
- **But:** Ultra-thin chips have properties that are partly different from those of thick silicon chips.
- **But:** The differences in chip properties may call for their appropriate consideration in circuit design.
- **Therefore:** Ultra-thin chip technology represents a paradigm shift in silicon technology.

# Our Publications on Ultra-Thin Chips

- **Invited Reviews and Tutorials**
  - ESSDERC-ESSCIRC 2009 (Athens, Greece)
  - BCTM 2009 (Capri, Italy)
- **Conferences**
  - IEDM 2006 (San Francisco, USA)
  - ISSCC 2008 (San Francisco, USA)
  - IEDM 2009 (Baltimore, USA)
  - ICICDT 2009 (Austin, USA)
  - ESTC 2010 (Berlin, Germany)
  - IEDM 2010 (San Francisco, USA)
  - Transducers 2011 (Beijing, China)
  - etc.
- **Journals**
  - IEEE Trans. El. Dev., 2009
  - Sol. St. Electronics, 2011


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