Ultra-Thin Chips

- A New Paradigm in Si Technology -

Joachim N. Burghartz

INSTITUT FÜR MIKROELEKTRONIK STUTTGART

Innovationsallianz Baden-Württemberg

Outline

- Ultra-thin chips: the paradigm shift
- Applications of ultra-thin chips
  - Traditional, recent and potential future applications
  - 3D ICs: Overcoming a bottleneck in CMOS scaling
  - Systems-in-Foil (SiF): enabler for new applications
- Ultra-thin chip fabrication
  - Post-process wafer thinning
  - Thin chips based on SOI
  - Chipfilm™ technology
- Characteristics of ultra-thin chips
  - Warpage of thin chips
  - Mechanical stability of thin chips
  - Apparently anomalous piezoresistive effect
- Constraints for circuit design
- Conclusions

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Ultra-Thin vs. Thin Chips: the paradigm shift

- **Thick chips and wafers (conventional)**
  - **300 µm – 1000 µm:**
    - Mechanically stiff and stable

- **Thin chips and wafers (conventional)**
  - **100 µm – 300 µm:**
    - Mechanically stiff with limited stability
    - Reduced thermal resistance

- **Ultra-thin chips and wafers**
  - **50 µm – 100 µm:**
    - Limited stiffness and limited stability

  - **10 µm – 50 µm:**
    - Flexibile with good stability

  - **< 10 µm:**
    - Flexible with good stability
    - Optically transparent

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Properties of Ultra-Thin Chips and Wafers

- **Mechanical**
  - **Warpage, curl-up**
  - **Young's modulus may deviate from bulk-Si value!**
    - Rough edges, e.g. from dicing
    - Rough backside, e.g. from polishing
    - Topographic frontside from layer depositions
- **Electrical**
  - **Piezoresistive effect**
  - **Backgate effects**
- **Optical**
  - **Absorption spectrum limited**
  - **Back-surface effects**
- **Thermal**
  - **Bi-material displacement**

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Processing Issues for Ultra-Thin Wafers/Chips

- **Front-end processes**
  - Handle/carrier substrates needed
  - Overheating effects (high-dose implant, RTP)
- **Back-end processes**
  - Excessive warpage from stress in interconnect layer stack
- **Packaging and assembly**
  - Edge chipping in dicing processes
  - Chip detachment from tape and transfer in assembly
  - Chip attachment to package
  - Mechanical pressure in wire bonding processes

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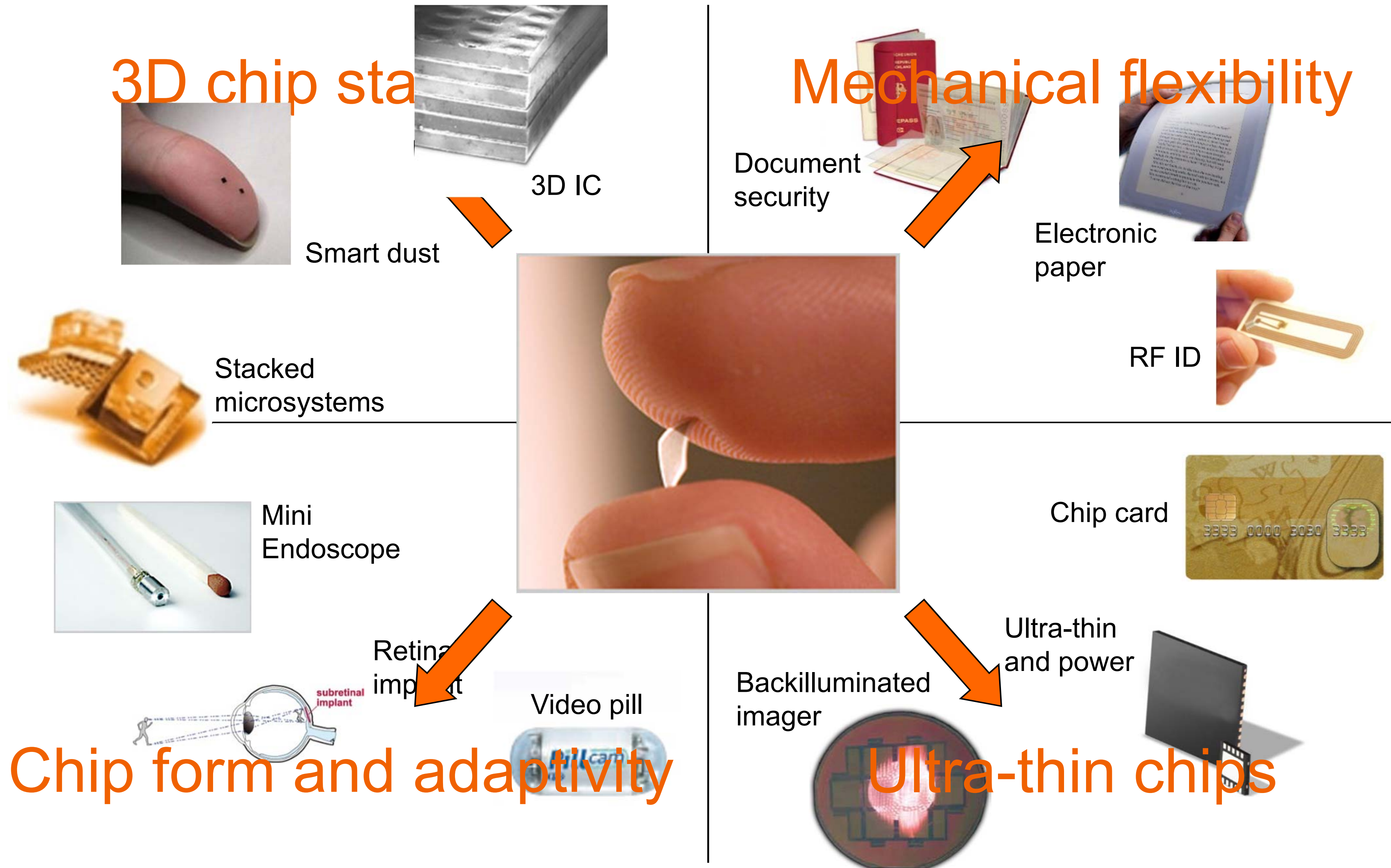
Applications of Ultra-Thin Chips



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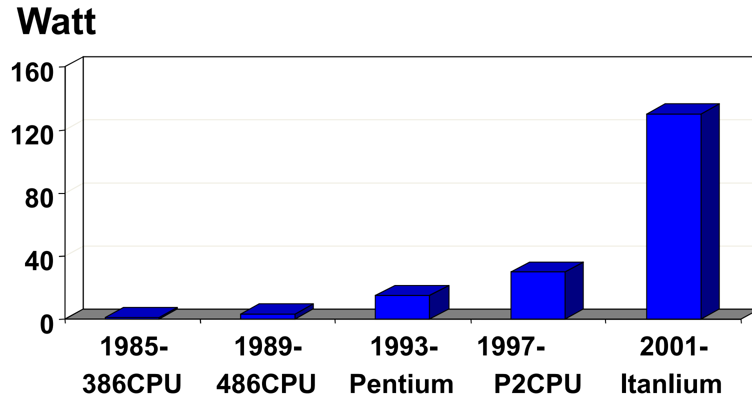
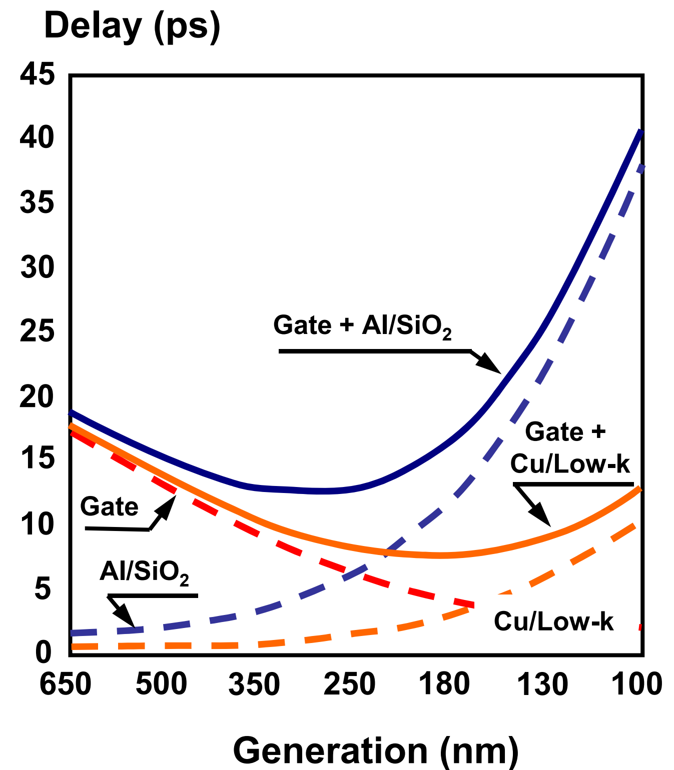
Bottlenecks in CMOS Scaling

Chip power



Interconnect Delay

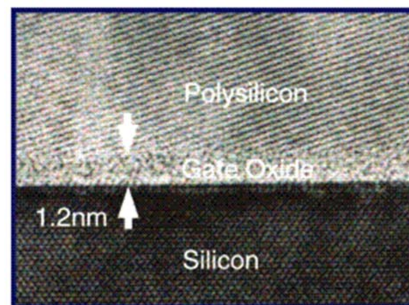


3D chip stacking:

- Shorter interconnects
- Relaxed device dimensions
- Power-delay tradeoff (?)

Transistor

- Subthreshold slope
- Gate oxide thickness
- Shallow junctions
- # dopants in channel
- …………



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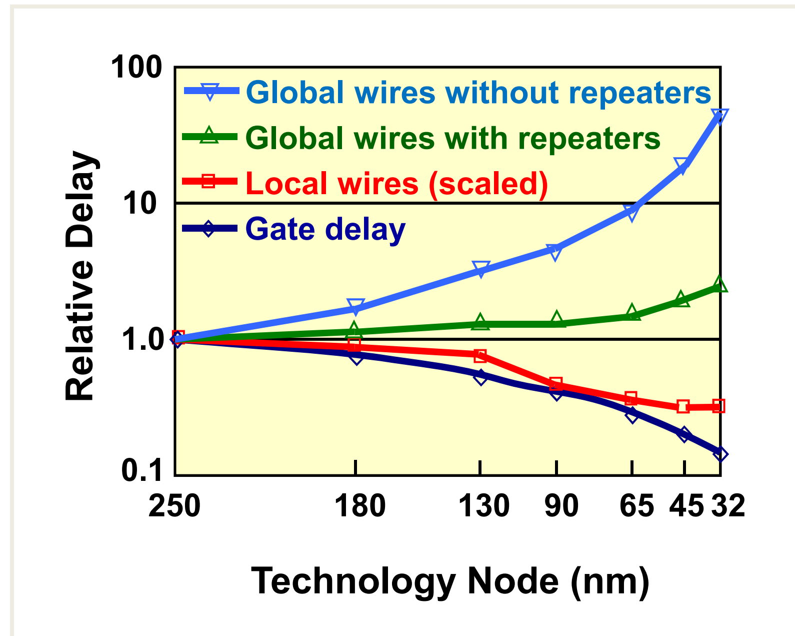
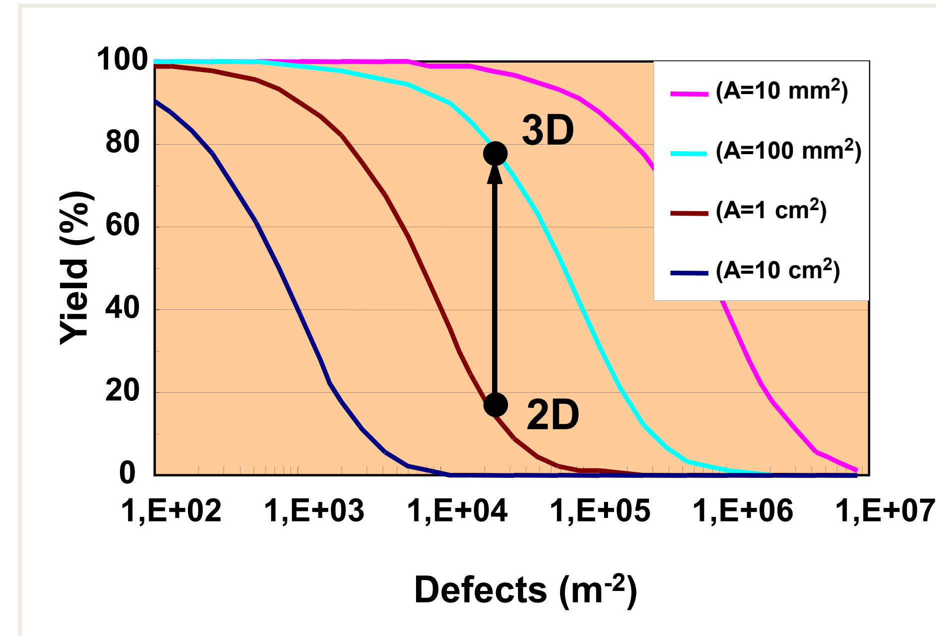
Interconnect Delay and Yield





- Smaller interconnect *RC* delays through shorter wires !
- Higher process yield through smaller chip area !

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3D-IC Integration Concepts

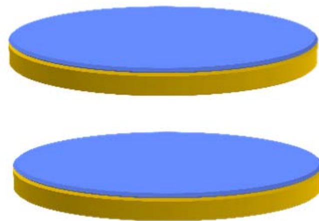
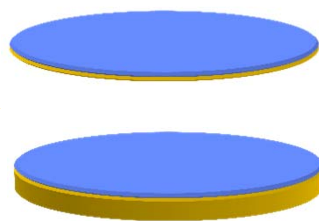
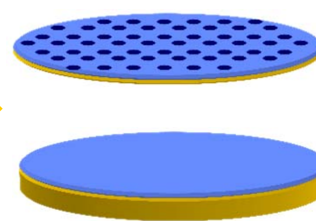
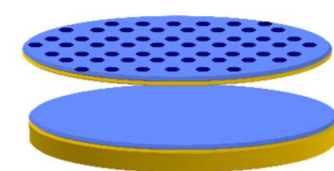
Wafer-to-wafer

1. CMOS integration

2. Wafer thinning
→ Minimum thickness?

3. Through-chip vias
→ Via diameter?

4. Wafer attachment
→ Process yield?

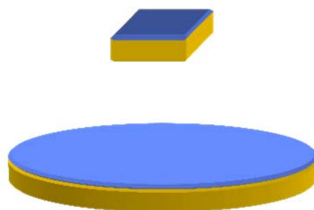
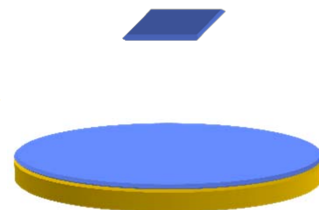
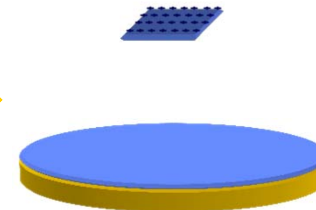
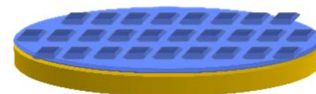
Chip-to-wafer and Chip-to-Chip

1. CMOS chip

2. Chip thinning
→ Throughput?

3. Through-chip vias

4. Chip attachment
→ Throughput?
→ Process yield!

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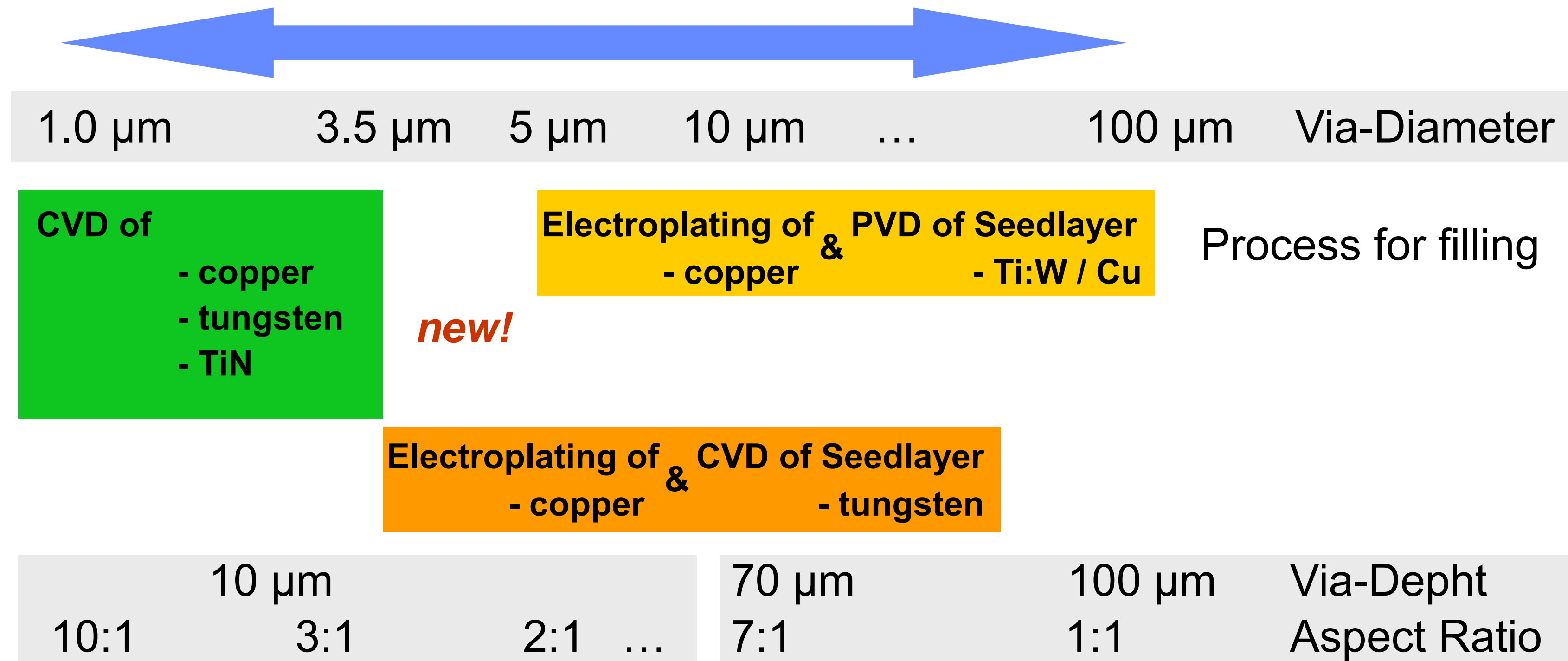
Through-Chip-Via Process

Via Formation for VSI – *Via Metal Filling*



***Source:* FhG-IZM**

- **More than 10:1 aspect ratio is difficult to achieve !**
- **Need for ultra-thin chips postulated on ITRS Roadmap**

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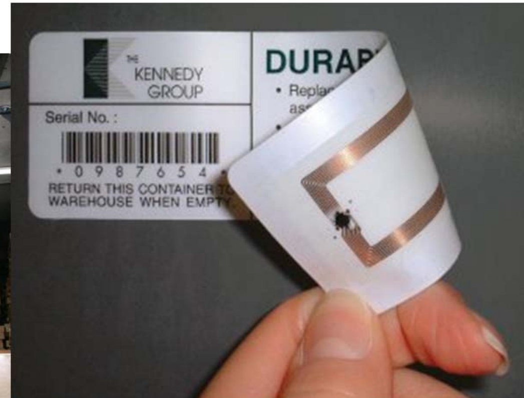
RF ID Tag

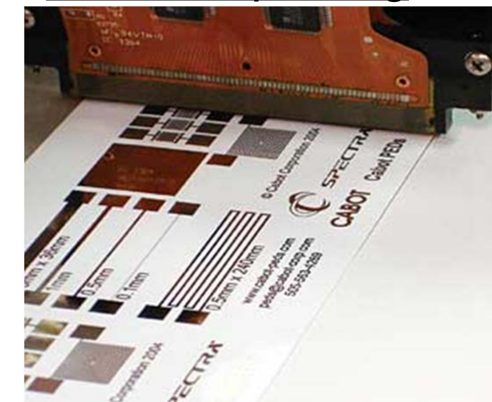
Warehouse storage



Roll-to-roll assembly

Department store sales

Low-cost printing



Source: **Metro**

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Source: **Unidym**

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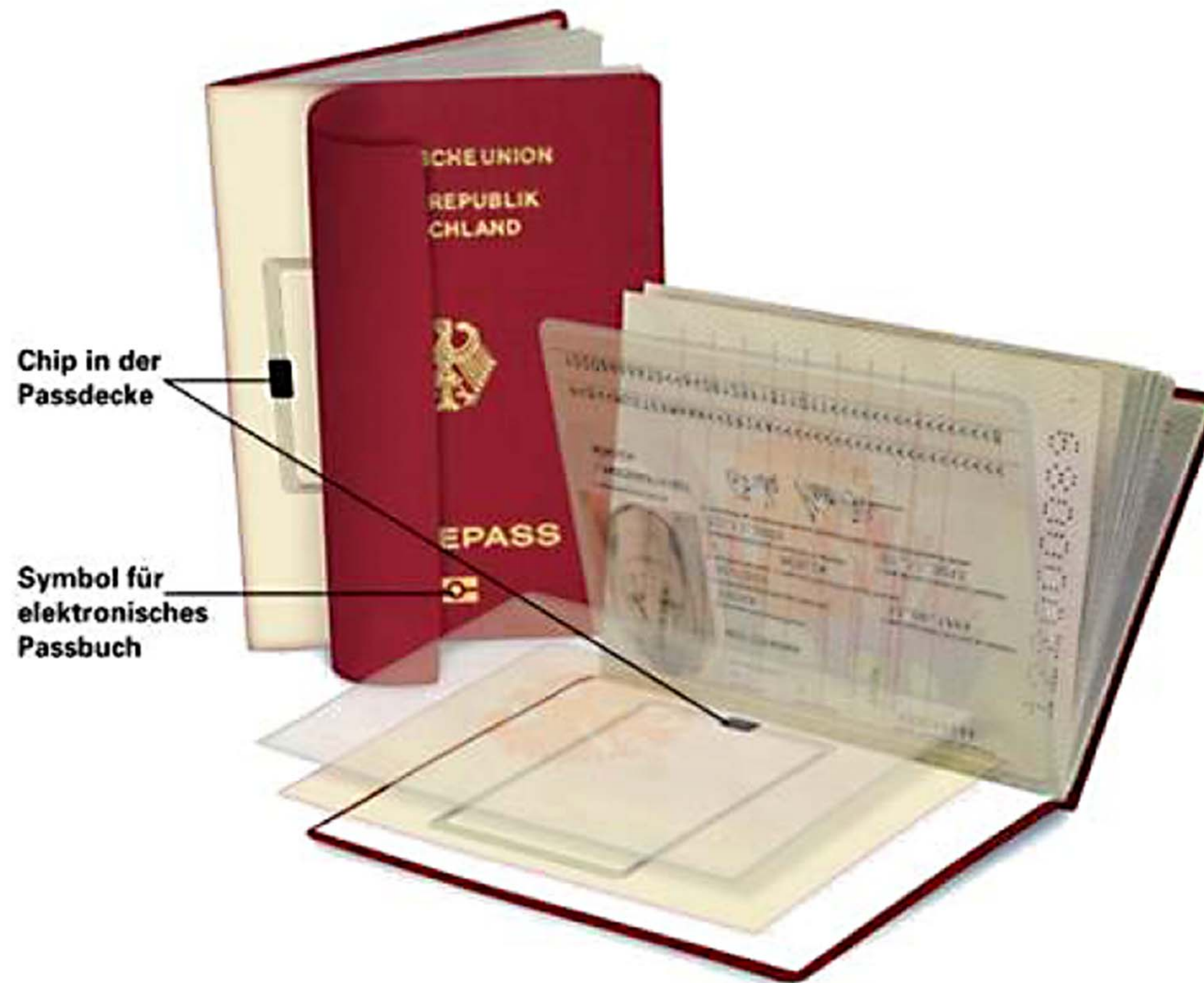

Source: NXP

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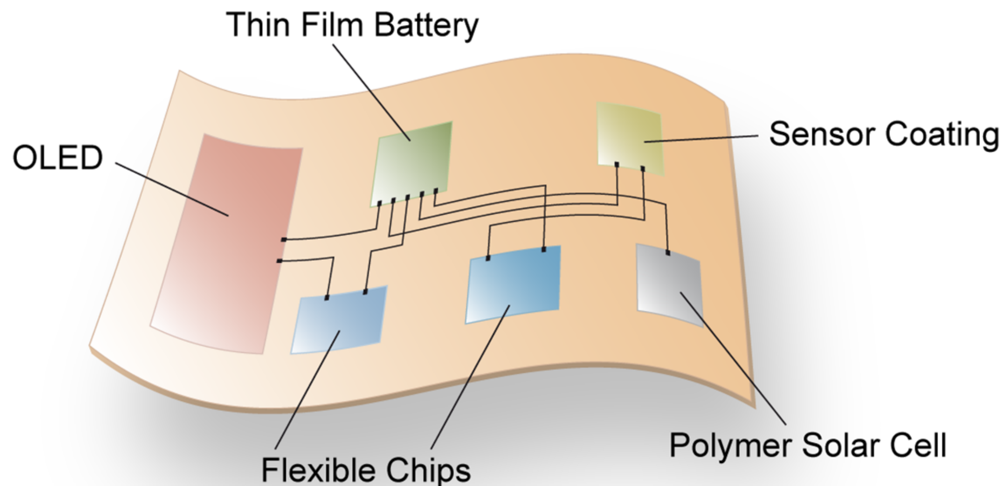
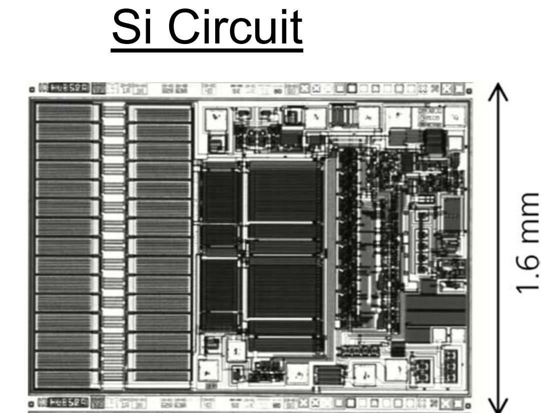
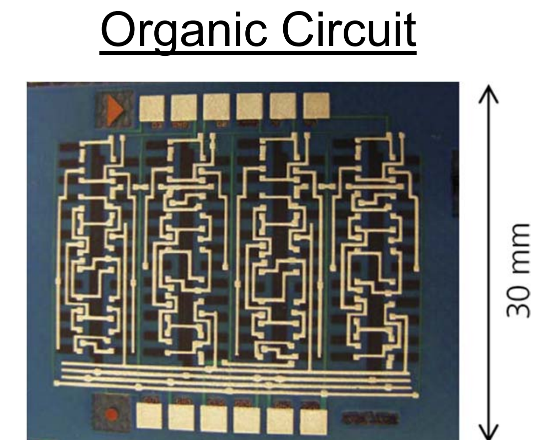
Hybrid Systems-in-Foil



Si Circuit



Organic Circuit



***Source:* FhG-IZM**

Thin Film Electronics **Si Integration**

- **Pro:** devices widely spaced
- **Con:** low integration density
- **Pro:** flexibility

\+

- **Con:** devices on chip
- **Pro:** high integration
- **Con:** thick Si chips

↓

- **Pro:** thin, flexible chips !

→ **Hybrid systems-in-foil = combining technologies with complementary merits!**

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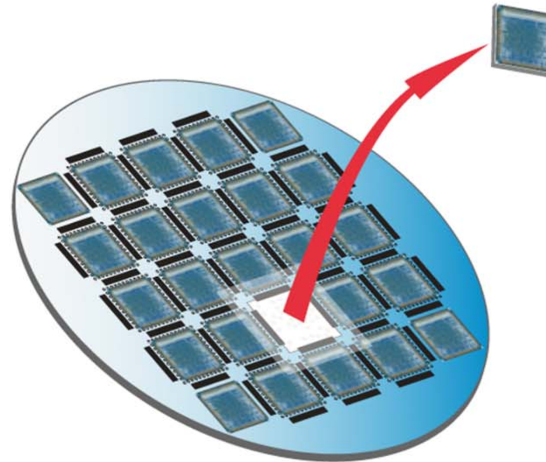
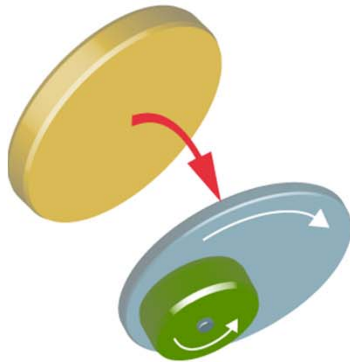
Process Technologies for Ultra-Thin Chips

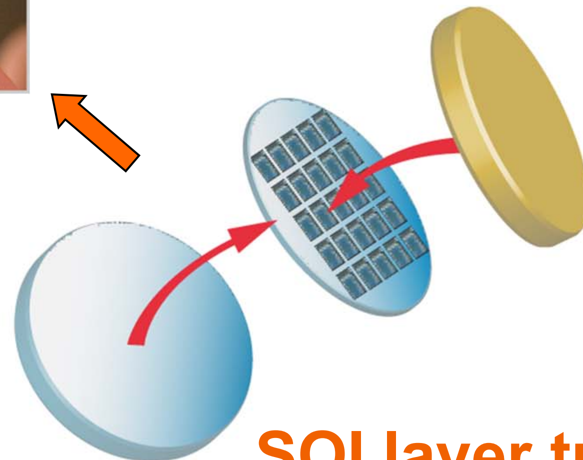
Chipfilm™



Additive process

Subtractive processes





Wafer back thinning

SOI layer transfer

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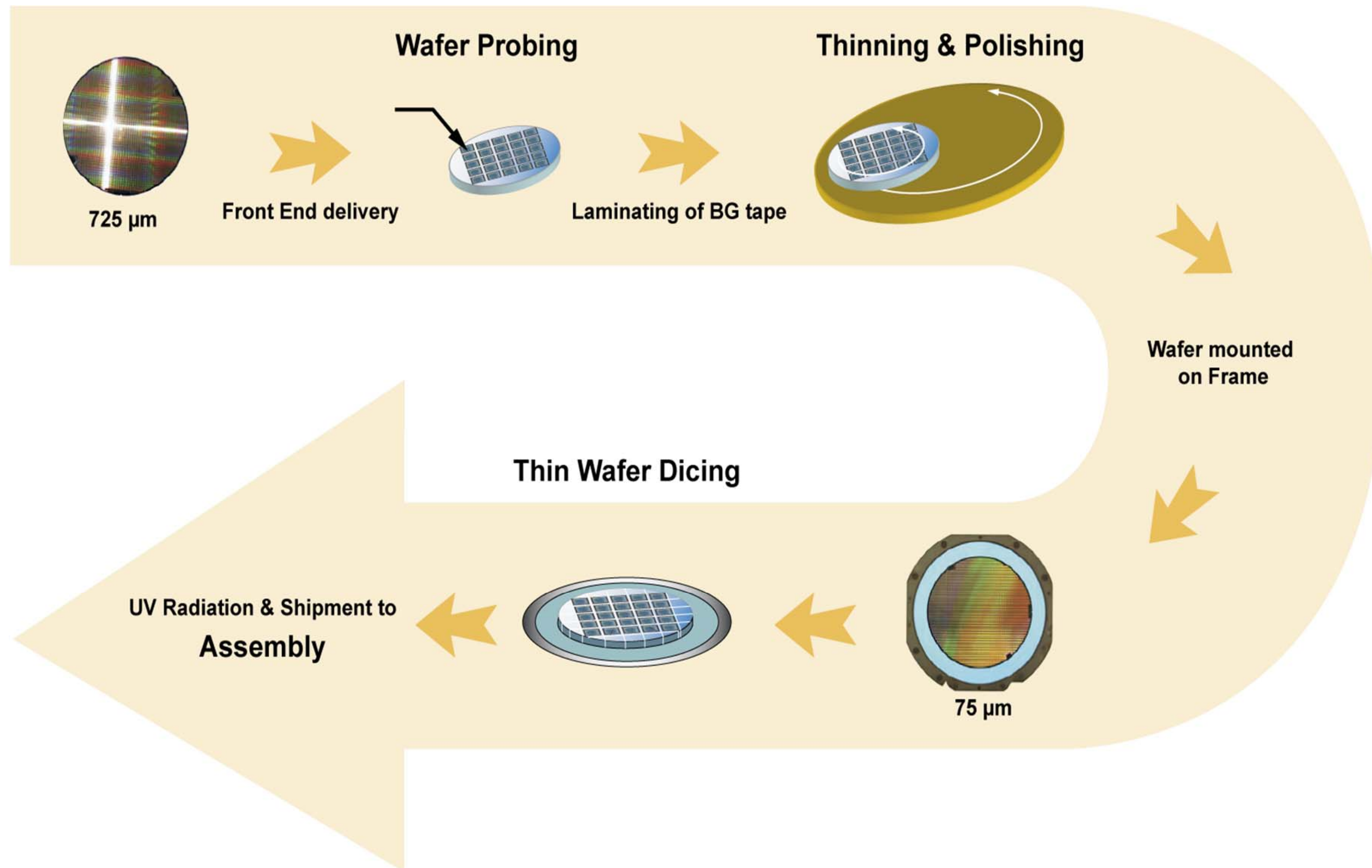
Wafer Back-Thinning: Process Sequence



→ **Economically practical wafer thickness >50 µm ! (NXP)**

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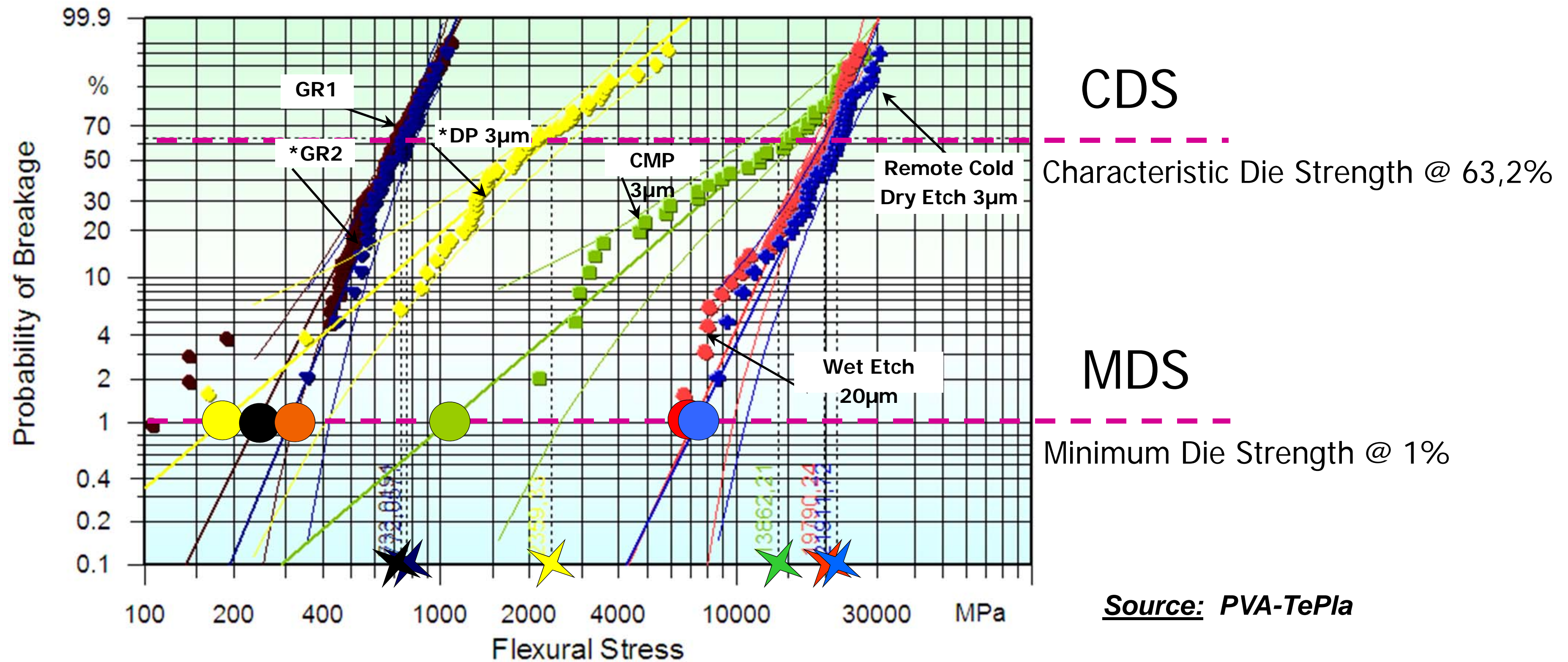
Wafer Back-Thinning: Mechanical Stability

Die Strength (Ball Ring Method), 75 µm 10x10 mm²



→ **Fast grinding processes introduce more defects than slow etch processes**

→ **Combination of fast grinding followed by defect removal steps**

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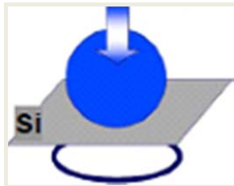
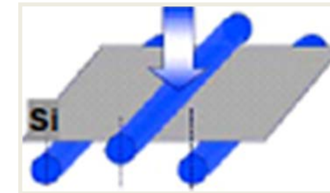
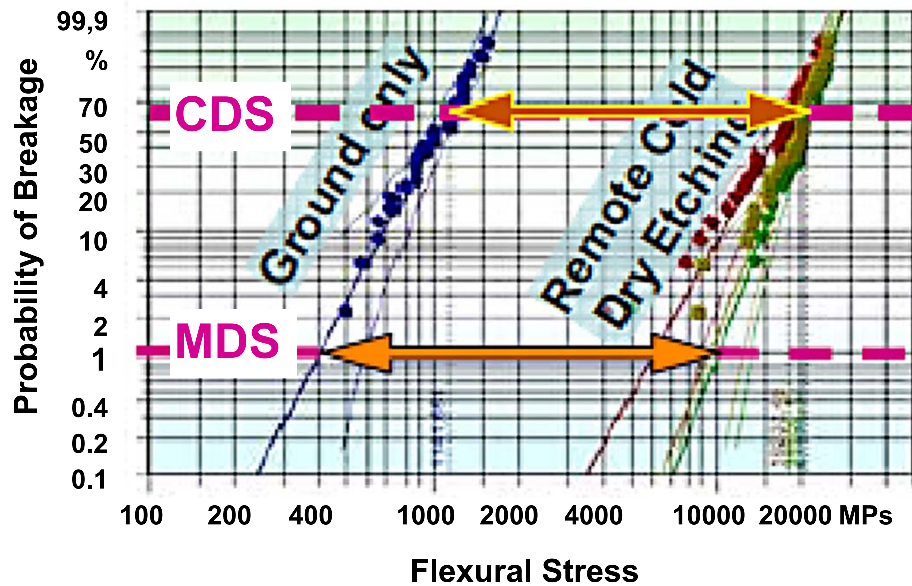
Process Effects on Mechanical Stability

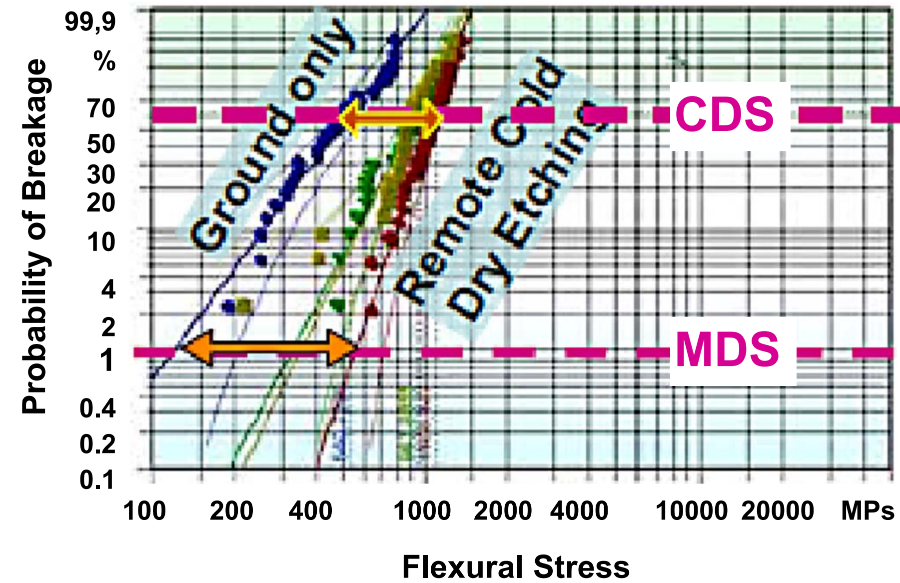


Ball-Ring-Method
75 µm 10x10 mm^2



3-Point-Method
75 µm 10x10 mm^2





Source: ***PVA-TePla***

→ Surface and edge quality of thin chips affect mechanical stability

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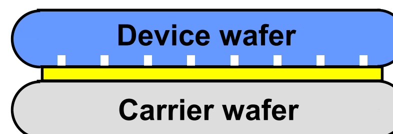
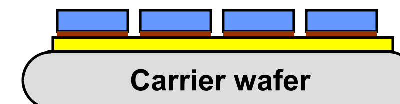
Dicing-by-Thinning concept DbyT“

Manufacture and transfer of 20 µm thin chips

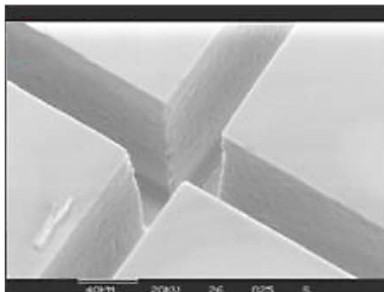
Prepare front side groves by etching or sawing



Reversible bonding onto carrier and wafer thinning



Chip separation by wafer thinning, transfer of thin dies



Wafer thinning: Grinding, etching, polishing

→ Improved edge quality and thus mechanical stability

Source: FhG-IZM

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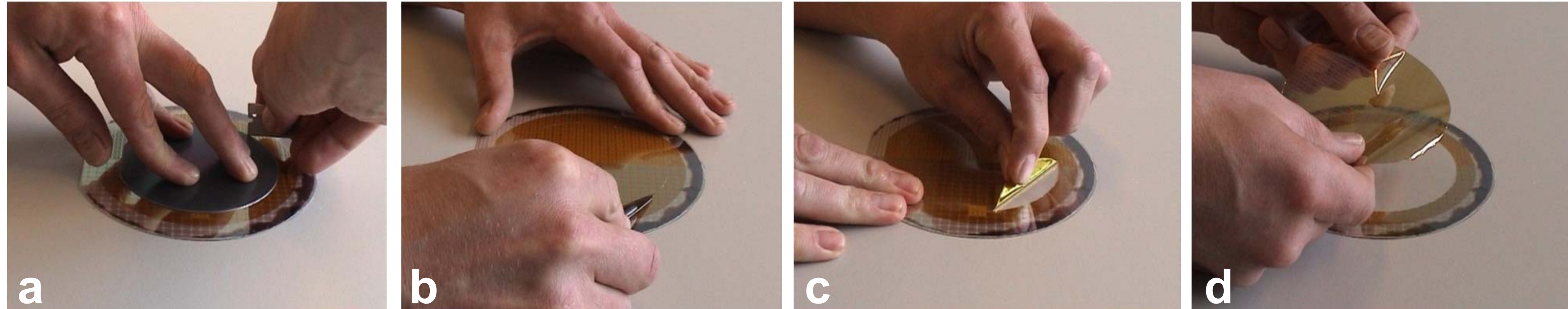
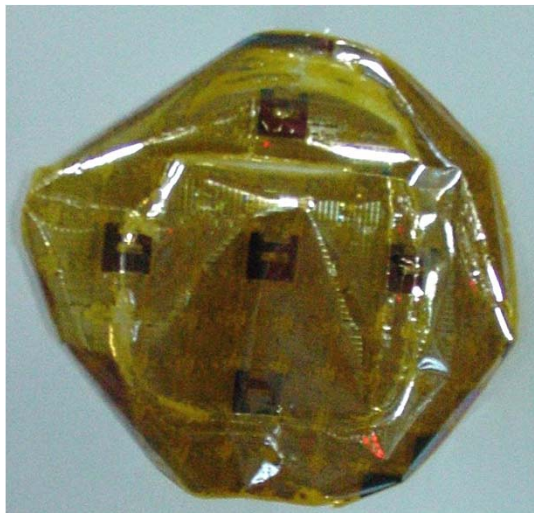
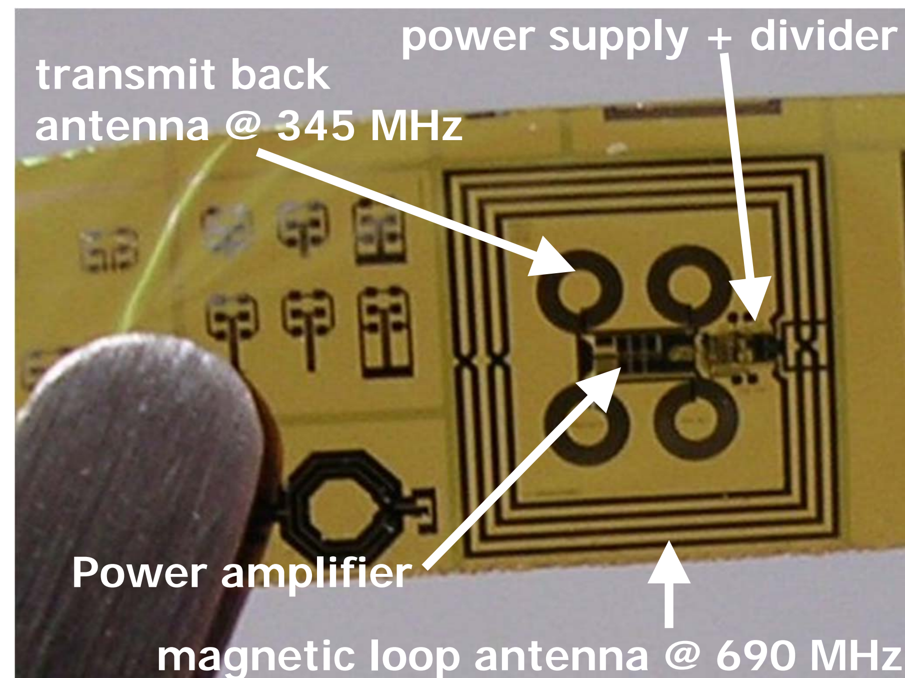
Philips's Circonflex Technology



Accidental detachment of Si-on-Glass Lead to Philips's Circonflex technology





***Source:* R. Dekker, Philips**

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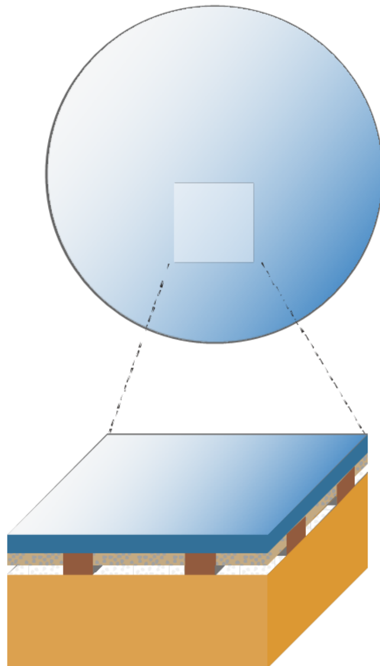
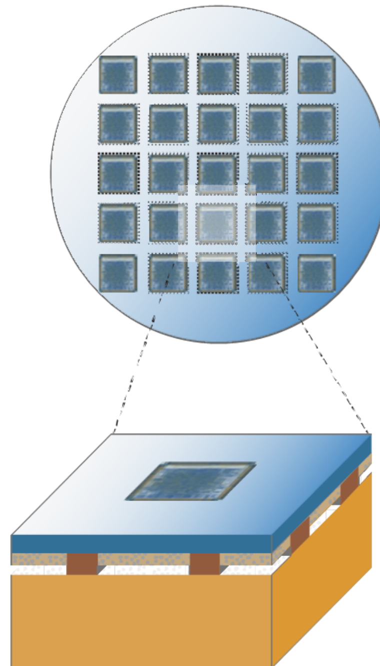
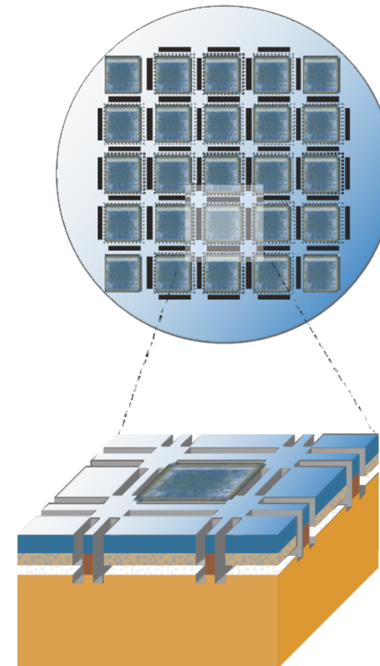
Chipfilm™ Technology

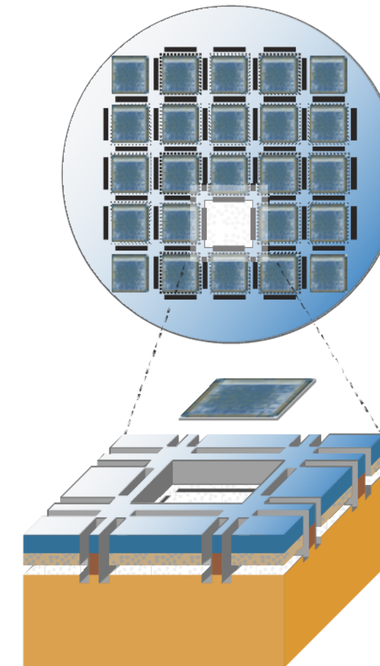
Chipfilm™ Wafer	CMOS Process	Trench & Test	Pick, Crack & Place™
Buried cavities	Device integration	Anchor structures	Chip singulation

- lateral (Chipfilm™-I)
- vertical (Chipfilm™-II)









IEDM 2006 Late News: Introduction of Chipfilm™-I

IEDM 2010: Introduction of Chipfilm™-II

Since July 2008: Joint development with Robert Bosch GmbH

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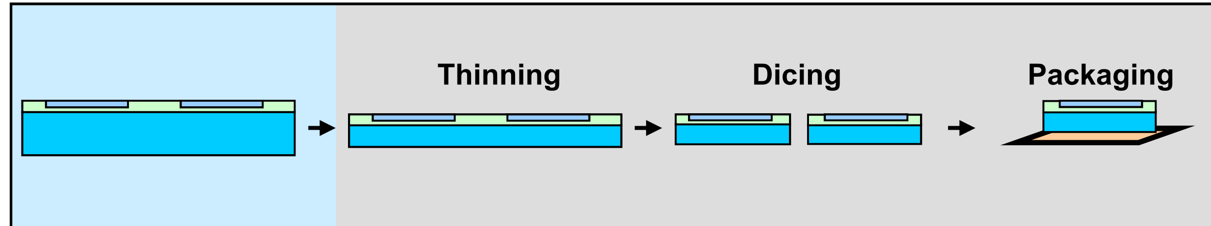
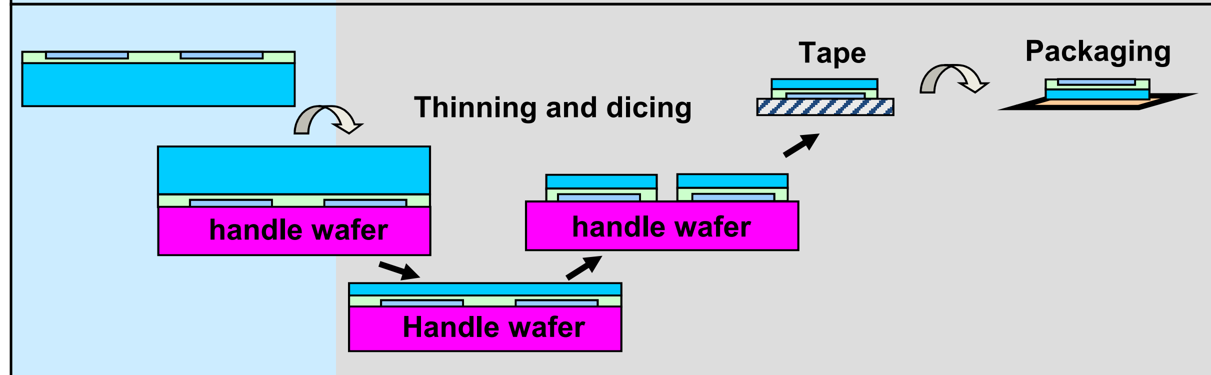
Chipfilm™ vs. Back-Thinning

Pre-Process CMOS Assembly

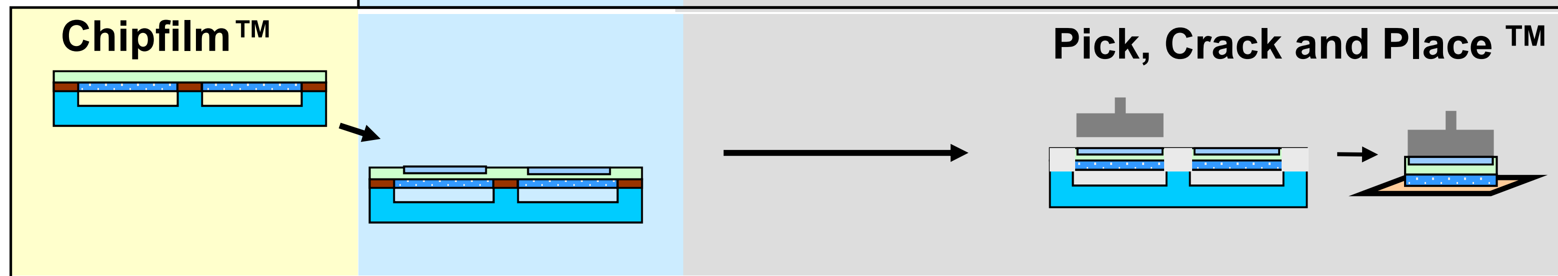
Standard wafer thinning



Wafer thinning for very thin chips



Chipfilm™ Technology



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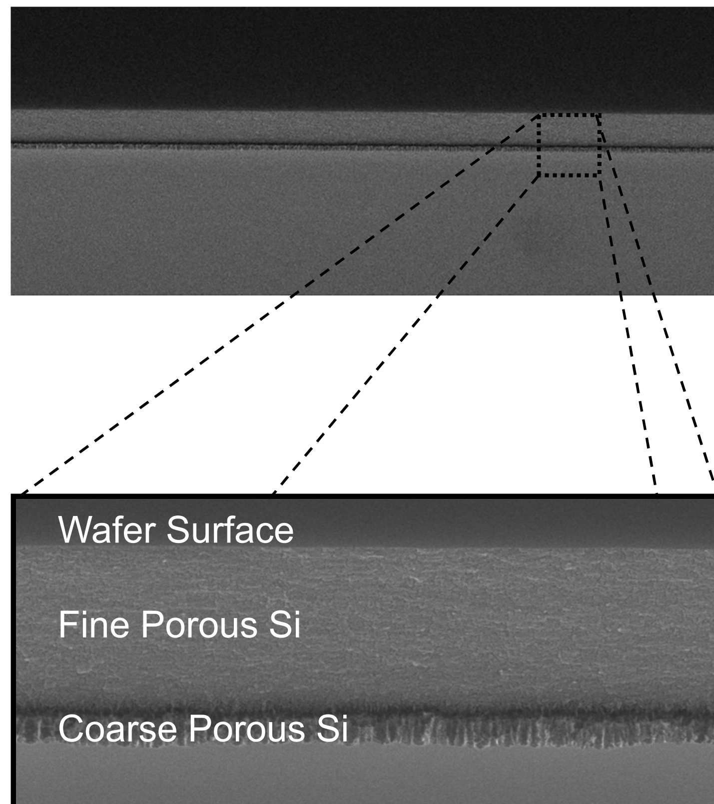
The Chipfilm^{TM} Pre-Process

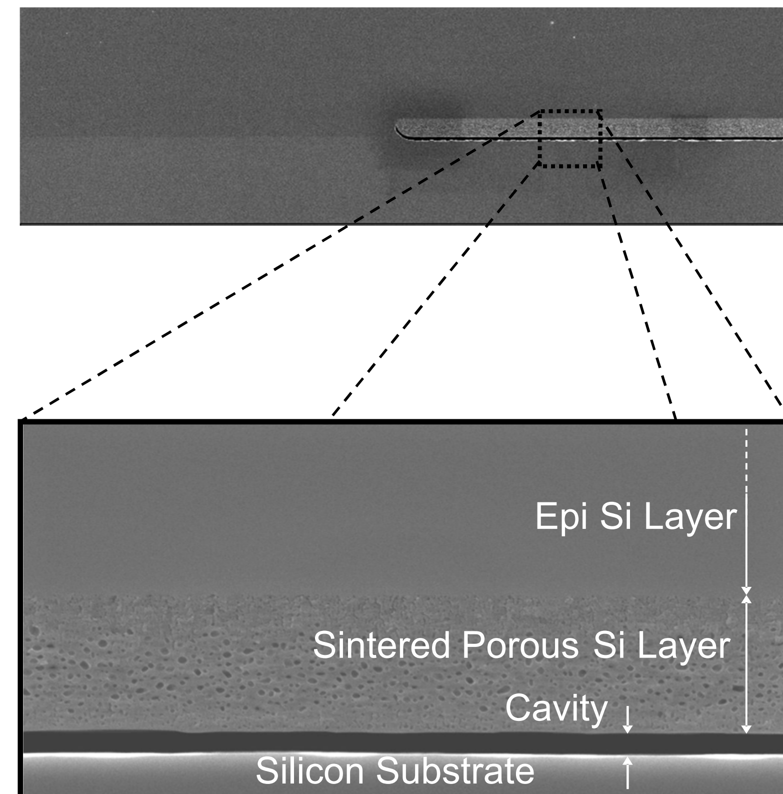
Step1:

- **Anodic etching of a Si wafer**
  - Dual porous Si formation
  - Masking through n^+ doping



Step2:

- **Sintering in oxygen-free ambient**
  - Silicon reflow
  - Fine porous Si → Nano grains
  - Coarse porous Si → Buried cavity



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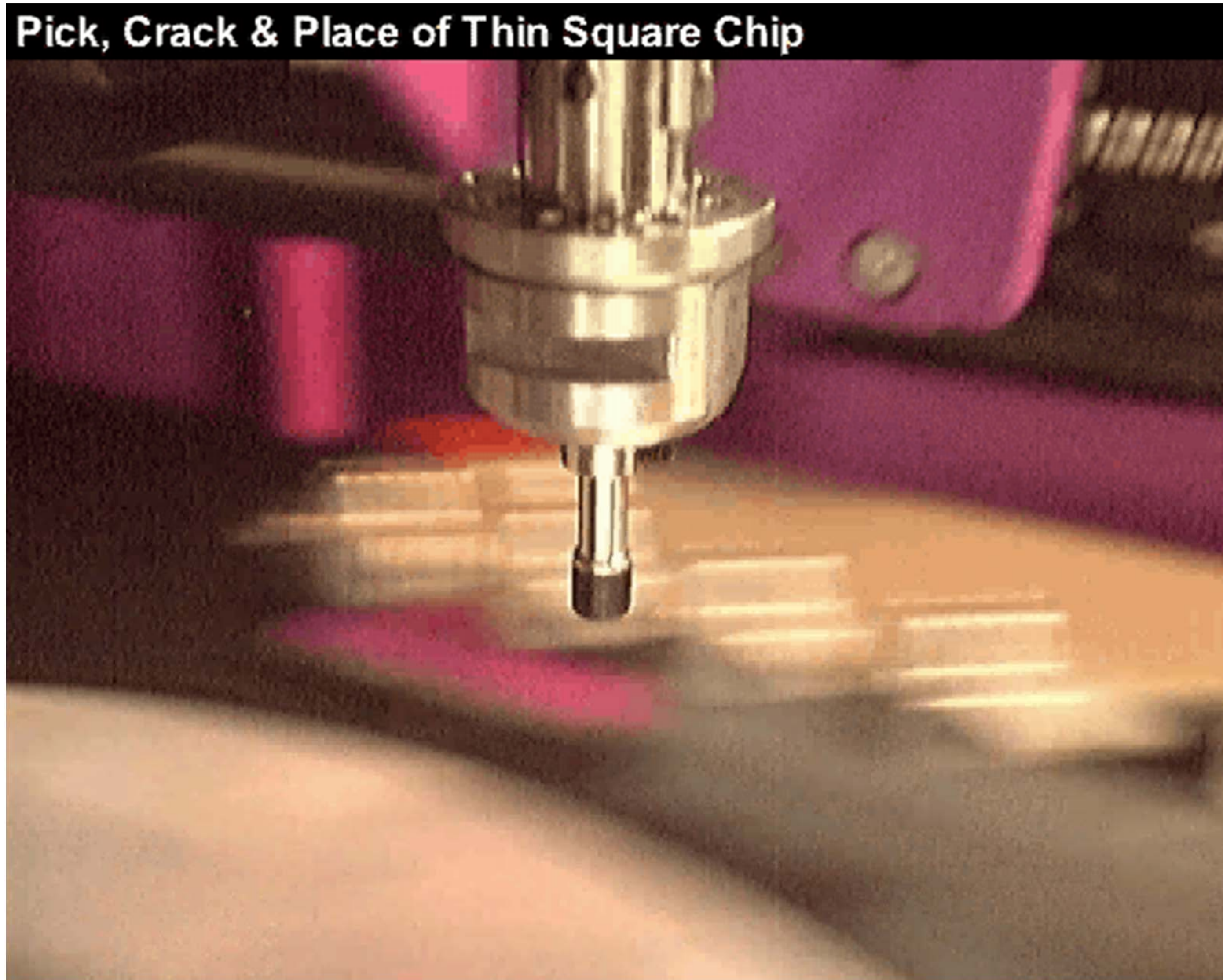
The Paick, Crack & Place™ Post-Process



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Technology Comparison

- **Chipfilm™-I** *IEDM 2006*
  - Continuous cavity
  - Lateral anchors

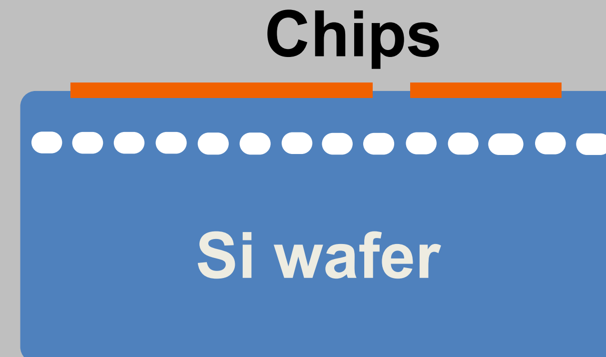
Pros:

+ Thickness limit < 20µm

Cons:

- Surface steps (~ 200nm)
- Predefined chip size

- **Chipfilm™-II** *IEDM 2010*
  - Discontinuous cavity
  - Vertical anchors



Pros:

+ Thickness limit < 20µm
+ High planarity (r_{avg}~ 7nm)
+ Generic wafer substrate

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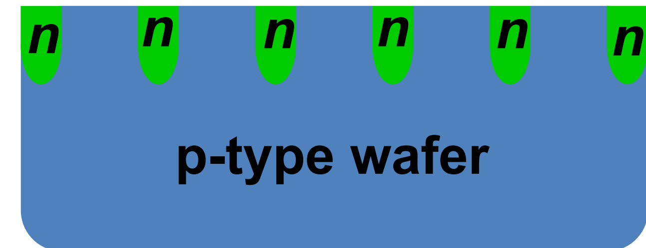
Chipfilm™-II Technology Process

- **Pre-process module (I)**
  - n-implant
  - anodic etching
  - thermal annealing
  - epitaxial growth

- **Device Integration**

- **Post-process module**
  - Trench etching
  - Chip detachment



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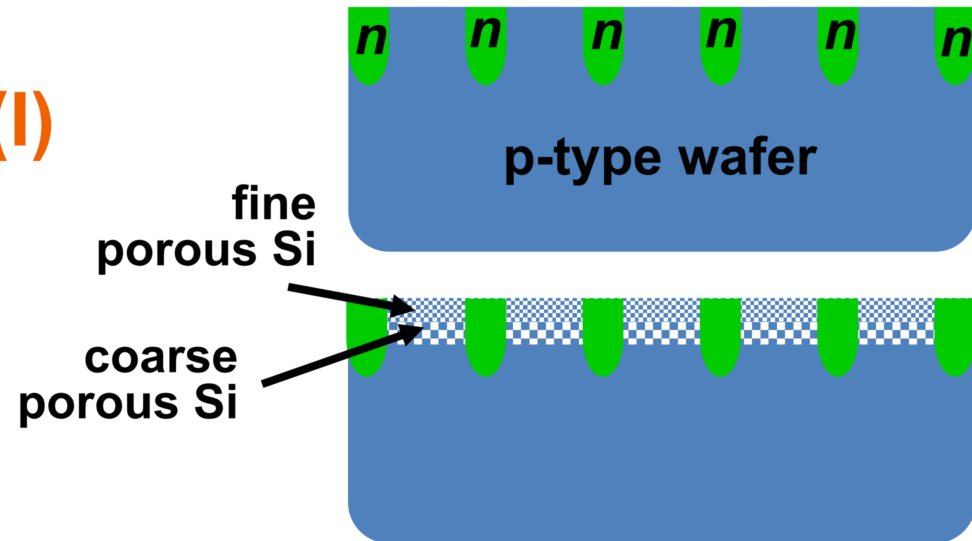

- **Device Integration**

- **Post-process module**
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IMS CHIPS

Chipfilm™-II Technology Process

- **Pre-process module (I)**
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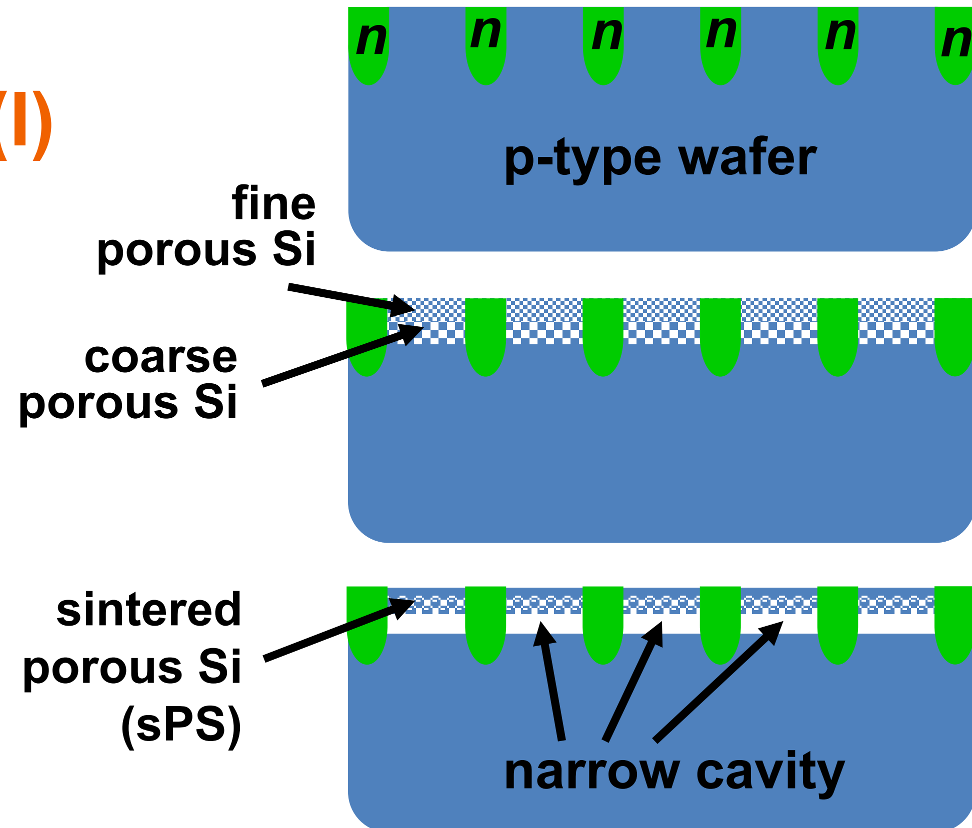

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