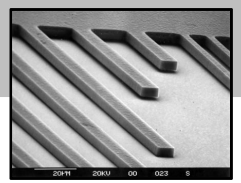
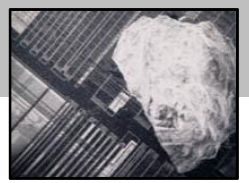
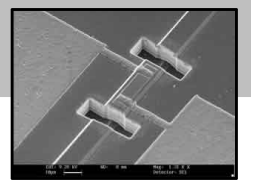
University of Pavia
Integrated Microsystems Laboratory

Power Efficient Data Convertes

Franco Maloberti

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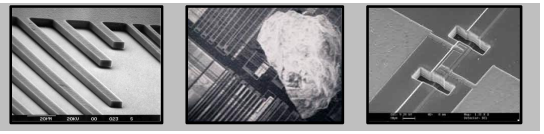
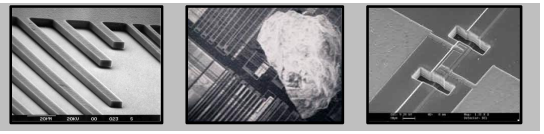


OUTLINE

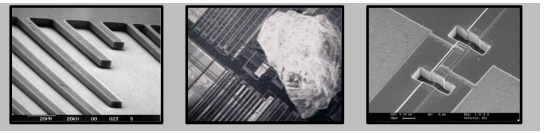
- Introduction
- Managing the noise power budget
- Challenges of State-of-the-art Technologies
- Analog Power-aware Design
- Design examples
- Digital Assisted Analog
- Conclusions

Introduction



RATIONALE

- In the fast growing electronic world, analog integrated circuits continue playing an important role for sensing and networking, security and safety, healthcare medical and life science, entertainments and education, and many other applications.
- Two important and essential features of many modern systems are connectivity and portability.
- Low power, or better micro-power design is very important because having a long battery life or even ensuring battery-less operation are essential features. The reduction of the supply voltage is not imposed by just an evolving IC technology but also by the need of minimum power consumption.
- Therefore, low-voltage analog and A/D design is an important research topic.



Research for future needs

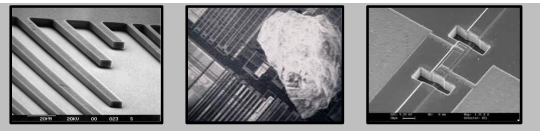
Technology advancements and the electronics market evolution more and more favor applications with nomadic features:

- Limited power refueling;
- Autonomous operation (no power specifically provided with capability to acquire the power that needs and modulate its activity depending on the available power budget).

Nomadic electronics impose an optimum trade-off between power and performance $\Rightarrow$ Minimum power and its aware use.

Hot Topics

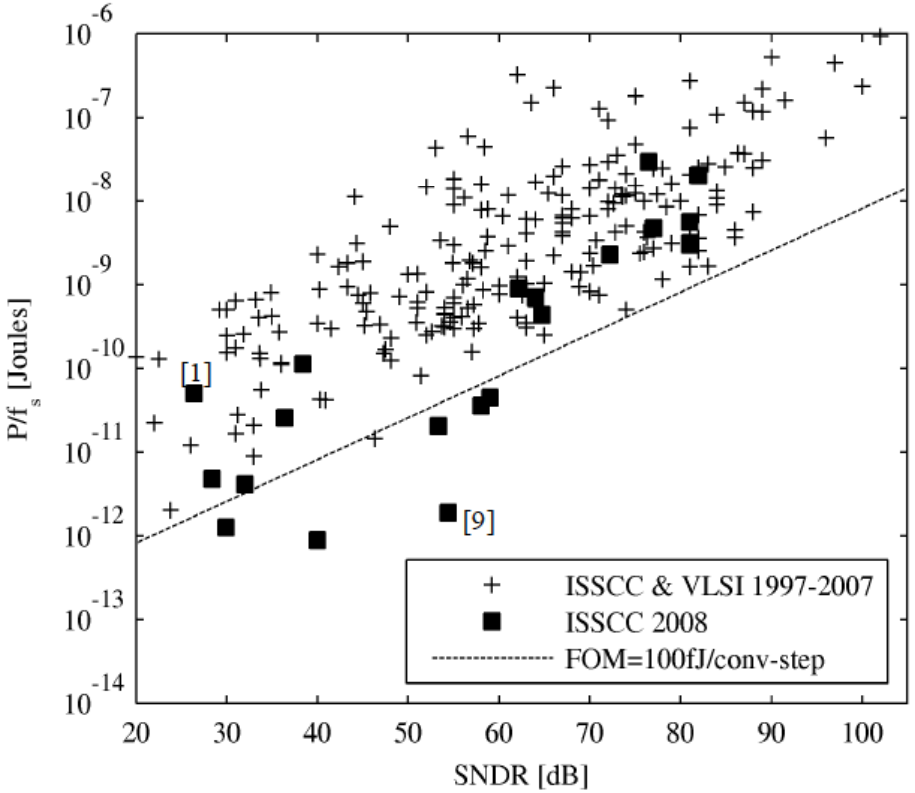
- Ultra-low power analog conditioning;
- Ultra-low power data conversion;
- Power aware digital design;
- Re-design of basic digital cells and power optimization of algorithms.
- Portable Power Management.

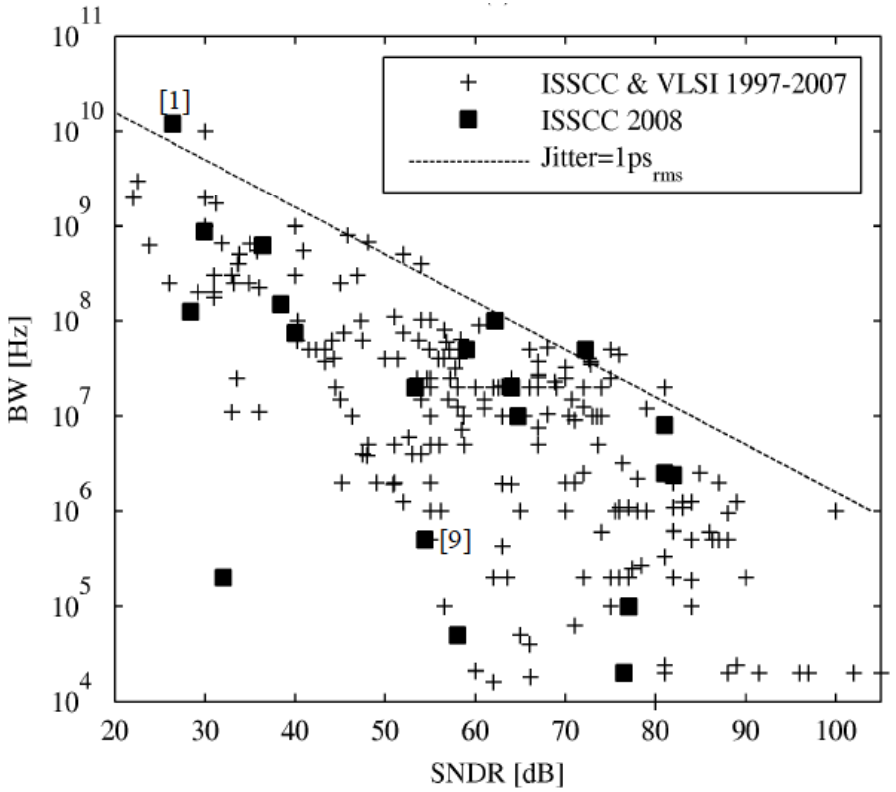


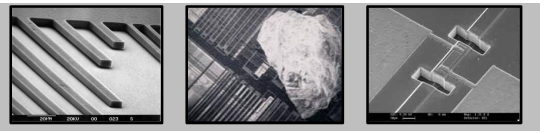
HOW TO MEASURE THE POWER EFFECTIVENESS?

$$FOM = \frac{P}{f_s \cdot 2^{ENOB}}$$

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02}$$







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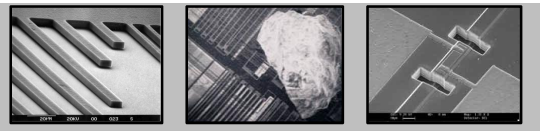
Managing the Noise Budget



THE RESOLUTION OF A DATA CONVERTER IS NOT MEANINGFUL

The bits just represent the accuracy of an ideal conversion system

- The true parameter is the ENoB (effective number of bit)
- Or the SNR

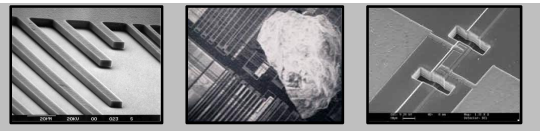
$$SNR = 6.02 \cdot ENoB + 1.76$$

- That, for a given V_{DD} define V_{FS} and estimate the allowed noise power

$$V_{noise,Tot}^2 = \frac{V_{FS}^2}{8 \cdot 10^{SNR/10}}$$

- The noise power gives the available noise budget for the various noise sources.

Noise Budget



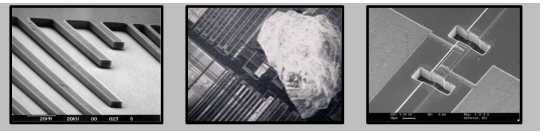
The key issue is to properly assign the available noise budget to the various noise sources

- Quantization noise
- Sampling noise
- Speed related noise
- Interference (power of tones)
- Board-level noise

Quantization

$$V_Q^2 = \int_{f_1}^{f_1+f_B} v_Q^2 \left| NTF(f) \right|^2 df \qquad f_1 < f_{in} < f_1 + f_B$$

Noise sources



- Sampling noise

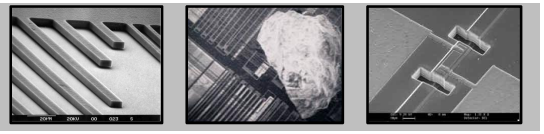
$$V_{Samp}^2 = \alpha \frac{kT}{C_S} \frac{1}{OSR} \qquad f_1 < f_{in} < f_1 + f_B$$

  - Assumes that the sampling noise is not shaped
  - $\alpha > 2$ depends on the noise contributed by the op-amp or due to multiple sampling

- Speed related noise
  - Clock jitter

$$V_{ji}^2 = \frac{V_{FS}^2}{8} 2\pi (f_1 + f_B)^2 \delta_{ji}^2 \frac{1}{OSR} \qquad f_1 < f_{in} < f_1 + f_B$$

Noise sources



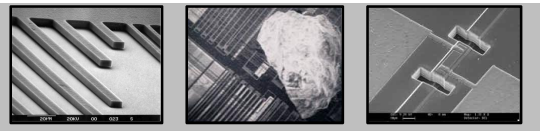
- Speed related noise
  - Sub-harmonic tones

$$V_{harm}^2 = \sum_i V_{tone,i}^2$$

- Interference/substrate noise V_{sub}^2
  - White noise floor X f_B
  - Tones

- Board level noise V_{board}^2
  - Give a small part of the budget to this term

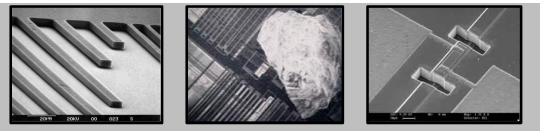
How to allocate the noise budget?

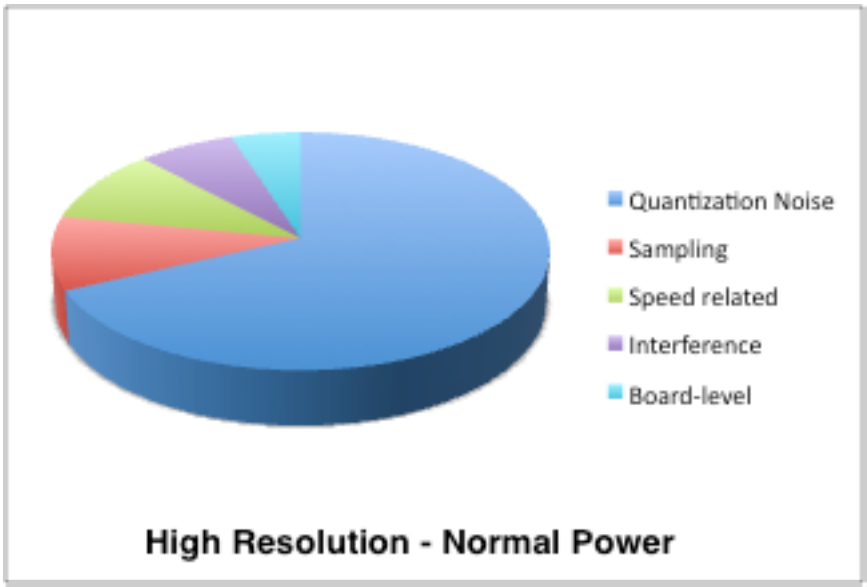


$$V_{noise,Tot}^2 = V_Q^2 + V_{Samp}^2 + V_{ji}^2 + V_{harm}^2 + V_{sub}^2 + V_{board}^2$$

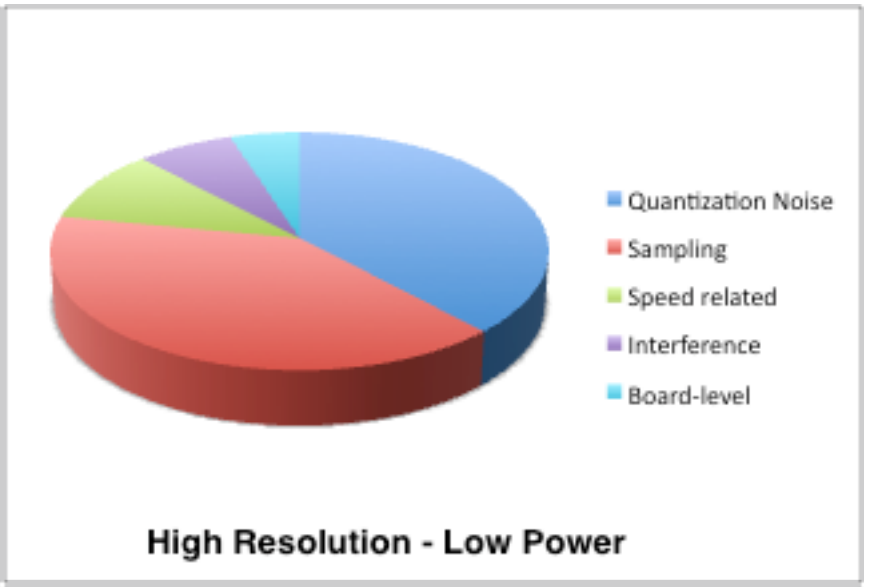
- Estimate the last three terms (to be kept to the minimum with a careful execution)
- Calculate the residual noise available and assign it …
  - At low frequency V_{ji}^2 is negligible (unless CT-ΣΔ)
  - Little budget to V_{Samp}^2 means increasing power
  - Little budget to V_Q^2 means more bit or higher noise shaping.

How to allocate the noise budget?

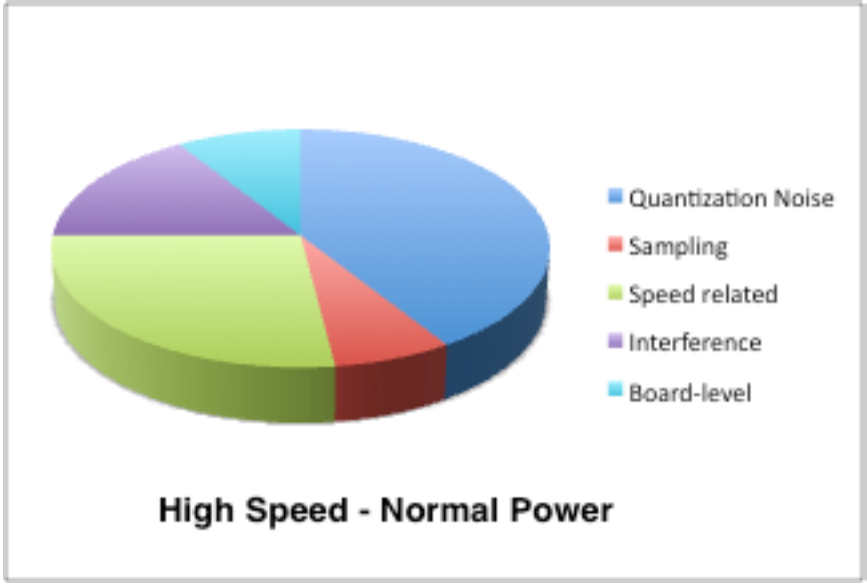




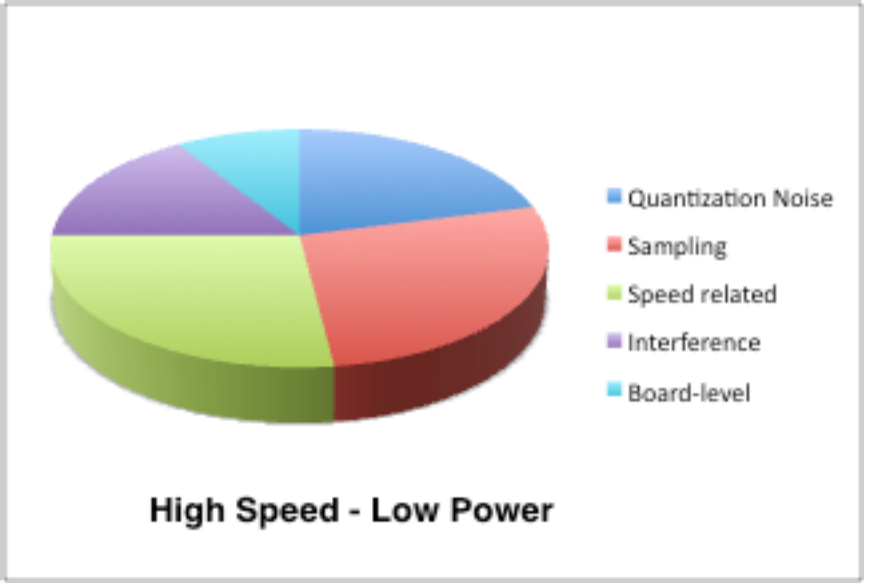
High Resolution - Normal Power



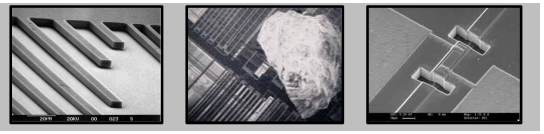
High Resolution - Low Power



High Speed - Normal Power



High Speed - Low Power



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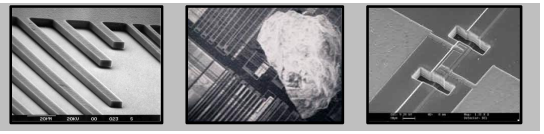
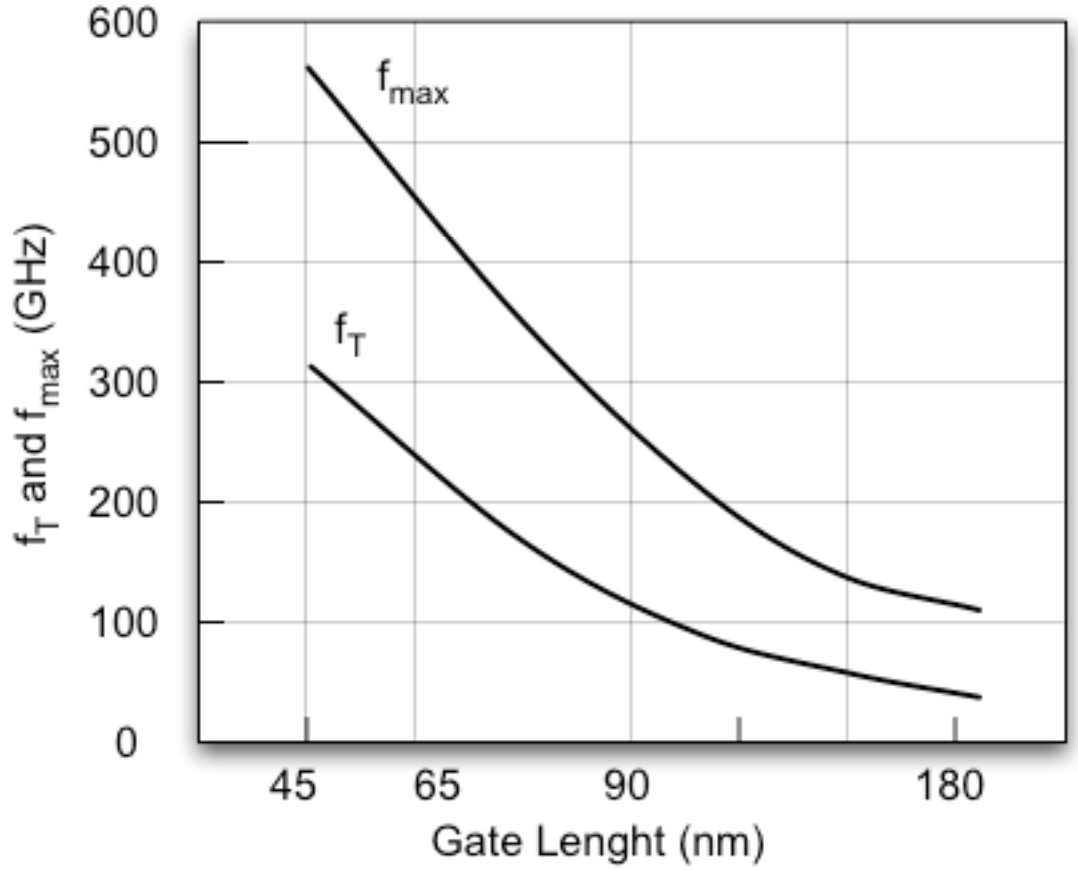
Good and Bad of Technology

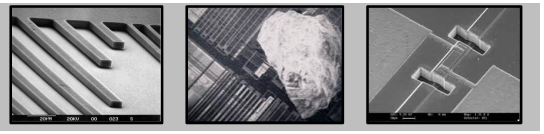


- Increase of speed ☞ process f_T of CMOS

$$f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \sim \frac{1}{L_g^2}.$$



Parameters of DSM Transistors

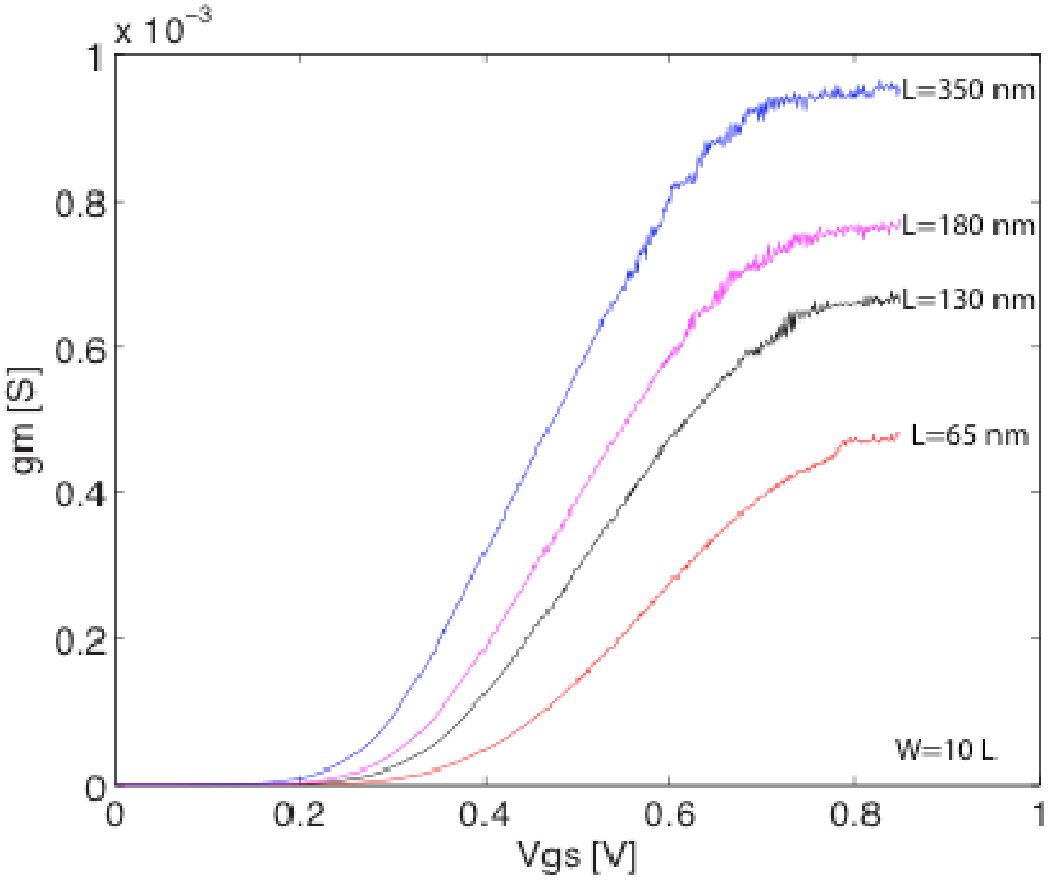


- Transconductance at saturated carrier velocity

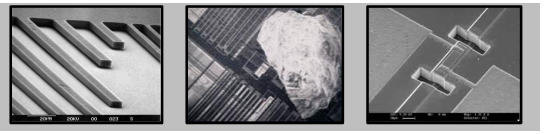
$$I_D = (\alpha W C_{ox} V_{ov}) v_{sat} \qquad g_m = \alpha W C_{ox} v_{sat}$$

Increase the width and/or enlarge the transistor

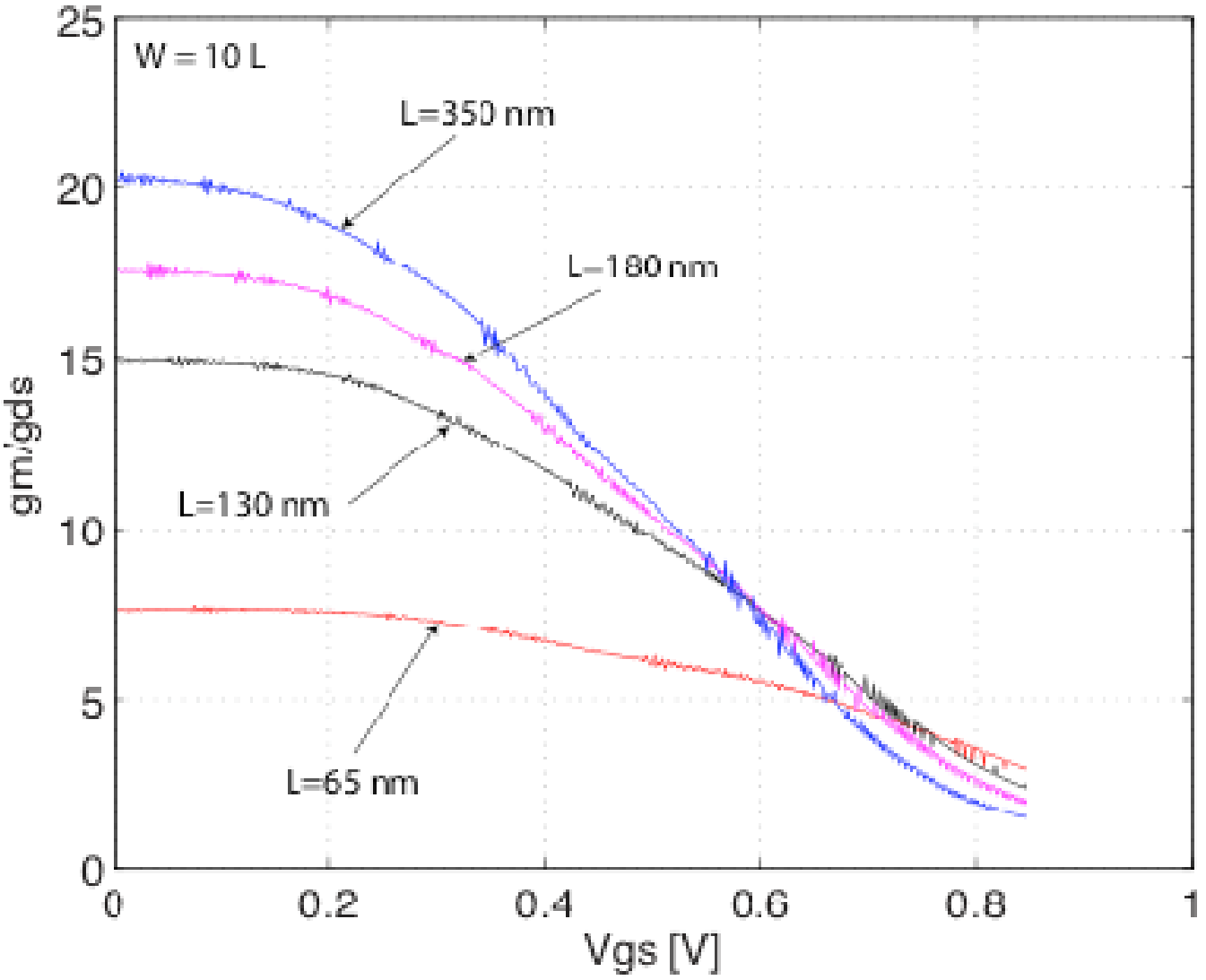
With a 65 nm technology



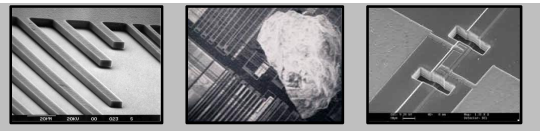
Parameters of DSM Transistors



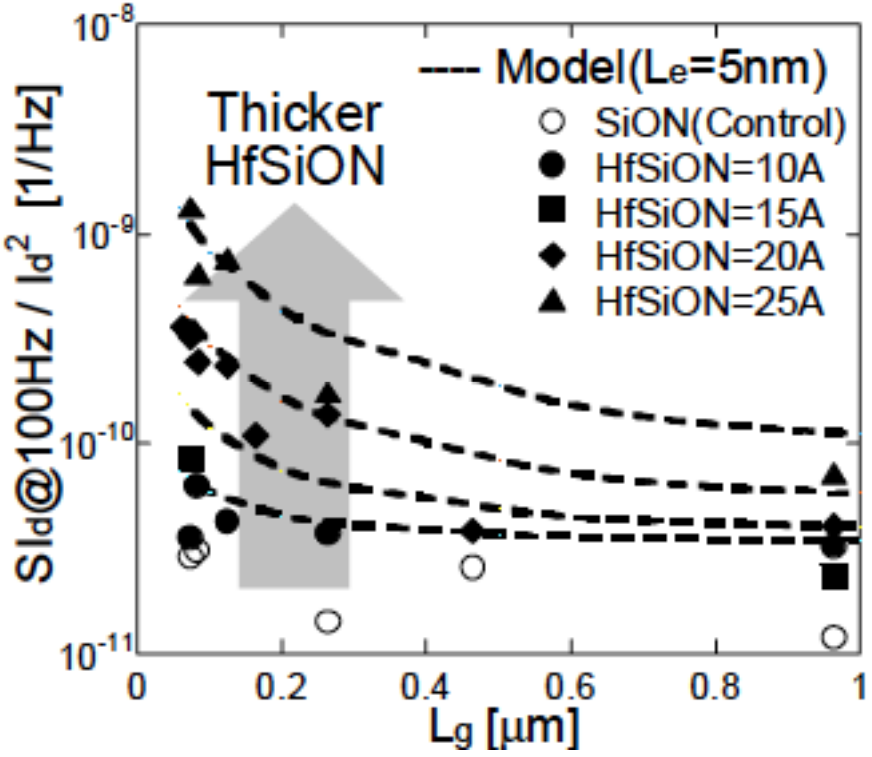
- Intrinsic gain

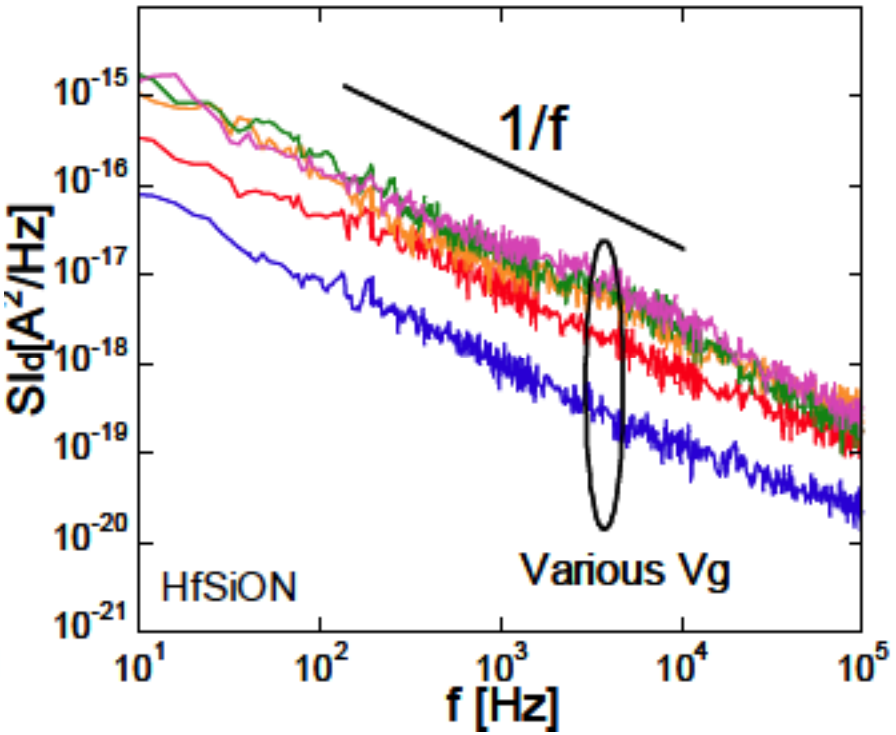


Parameters of DSM Transistors



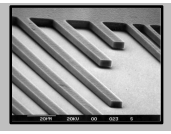
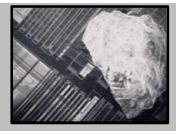
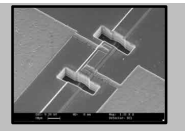
- Use of high-k oxides causes much more 1/f





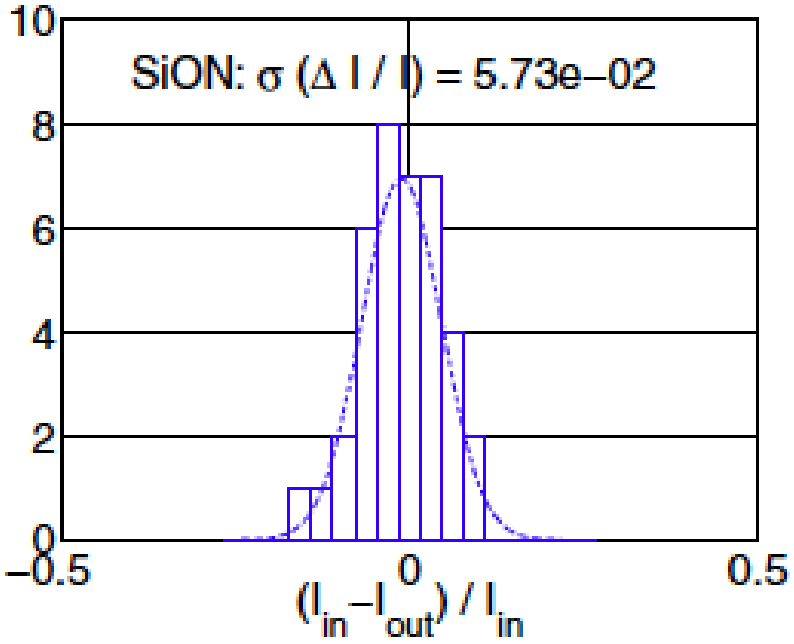
Yuri Yasuda et al.
2006 Symposium on VLSI Technology

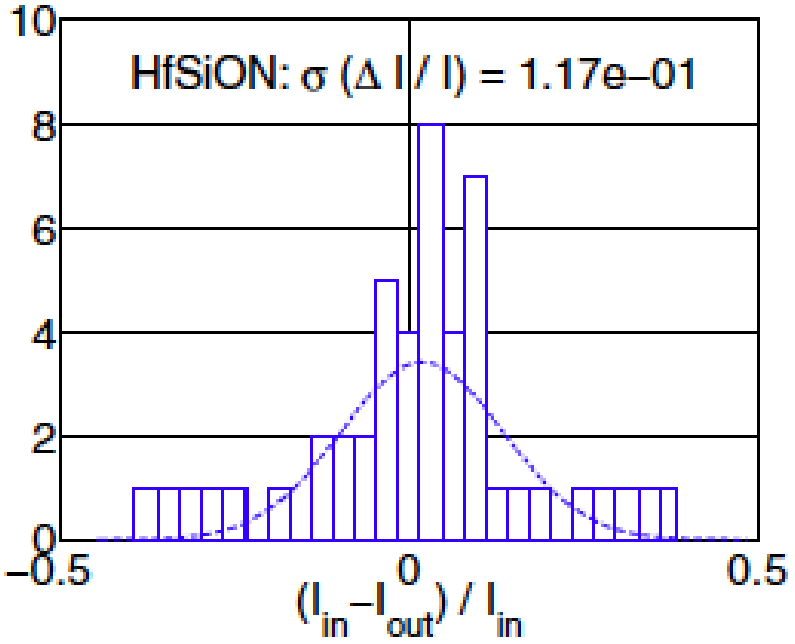
Parameters of DSM Transistors

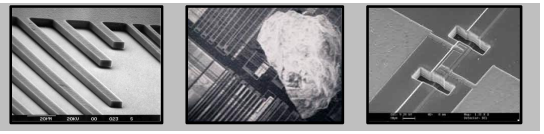
- Matching

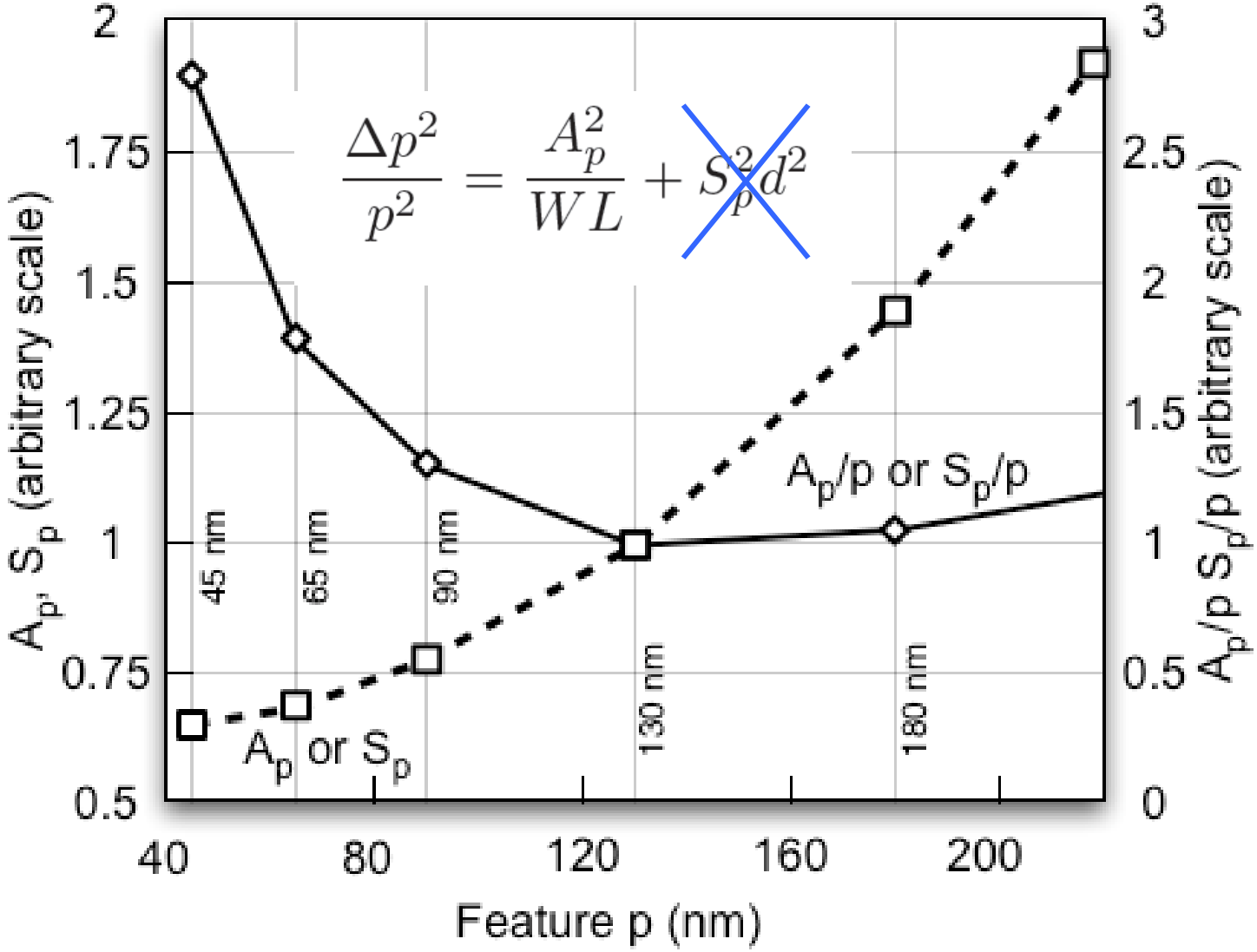
$$\frac{\Delta p^2}{p^2} = \frac{A_p^2}{WL} + S_p^2 d^2$$

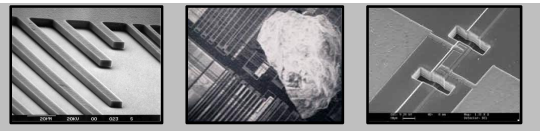




Matching Parameter and Matching







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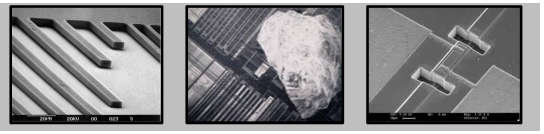
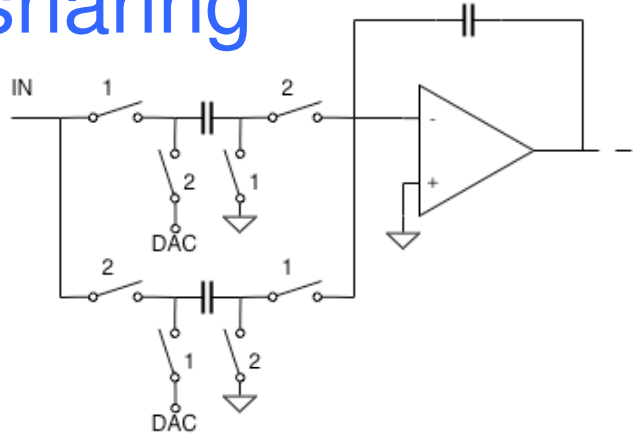
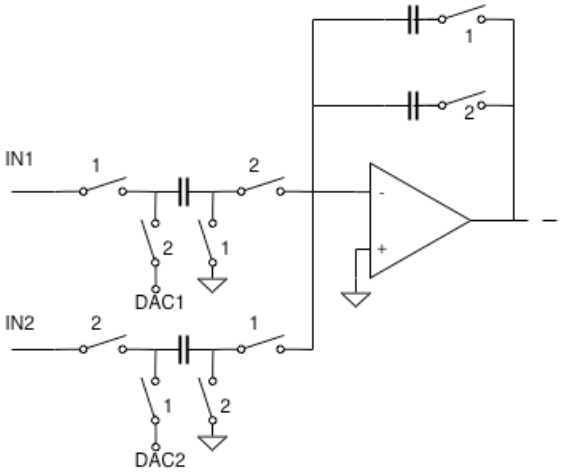


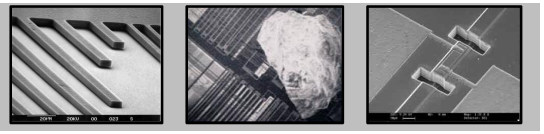
DESIGN STRATEGIES

Double sampling or Op-amp sharing

- Bandwidth of the Op-amp must be a bit higher
- No time for the virtual ground settling
- Feedback factor can be time variant
- Power saving is about 0.3 $P_{op\text{-}amp}$

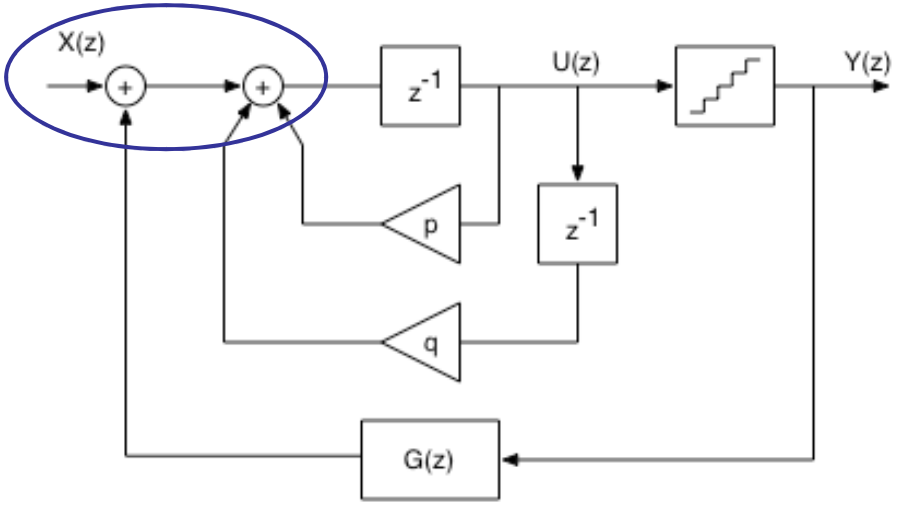






Use less Op-amp than the order ΣΔ

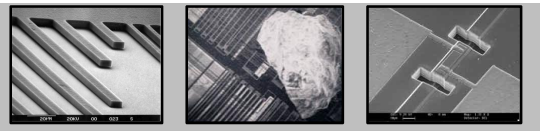
More details and
Experimental results
J.Ko et al.
@ ISSCC 05



p = 2
q = -1
G= $2-z^{-1}$

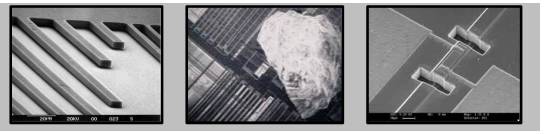
Patent by
J.Koh @ TI

- The adding node requires using one op-amp
- The integration block is $1/(1-2z^{-1}+z^{-2})=1/(1-z^{-1})^2$
- The NTF is $(1-z^{-1})^2$
- Mismatch in capacitances moves the NTF zeros
- Solution suitable for medium resolution and low OSR



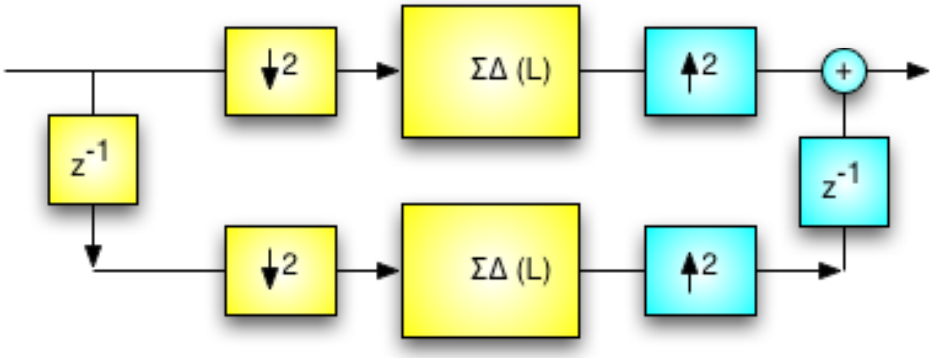
More bit or higher OSR in ΣΔ architectures

- Multi-bit helps in reducing the power consumption:
  - Second order -> double the clock to get 2.5 extra bit
    - Doubling the clock means more than doubling the power
    - 2.5 bit means $2^{2.5}$x = 5.6x the number of levels used in the ADC and DAC (5.6x comparators)
- Consider a second order ΣΔ with a 2-bit DAC
    - $P_{op\text{-}amp}$=1 mW; P_{comp}= 30 μW
    - $P_{\Sigma\Delta}=2\cdot P_{op\text{-}amp} + (2^2-1)\cdot P_{comp} + P_{dig} \approx 2 + 0.09 + 0.1 = 2.2$ mW
  - Doubling the clock frequency
    - $P_{op\text{-}amp}$=2 mW; P_{comp}= 40 μW; $P_{\Sigma\Delta}$= 4.25 mW
  - Using 5.6x comparators (4.5-bit) (and a bit more digital)
    - $P_{\Sigma\Delta}=2\cdot P_{op\text{-}amp} + 22\cdot P_{comp} + P_{dig} \approx 2 + 0.66 + 0.15 =$ 2.8 mW



N-path and NTF Synthesis

- The motivation of this approach is
  - Reduction of power consumption
  - Obtain convenient NTF
- Basic structure is a set of ΣΔ modulators running at f_{ck}/N that are used in an N-path arrangement

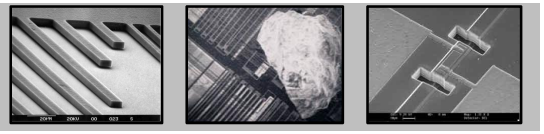


$$z^{-1} \rightarrow z^{-2}$$

$$NTF = (1 - z^{-1})^L$$

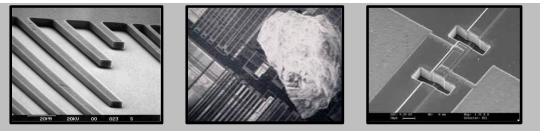
$$NTF' = (1 - z^{-2})^L$$

- The op-amps run at half clock frequency; we have two op-amps
  - The NTF can be modified adding new terms



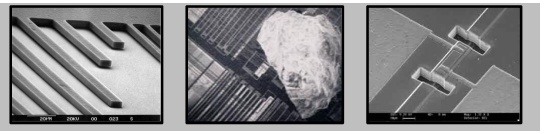
Design of suitable building blocks

- The use of well established scheme can be non-optimal
  - Op-amps linearity and gain really necessary?
  - Existing comparator architecture are optimal?
  - Can we trade speed with accuracy even at the block level?
- Look at the reference generator power needs
- Use of digital methods to relax the block specs



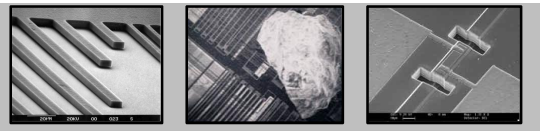
OUTLINE

- Introduction
- Managing the power budget
- Challenges of State-of-the-art Technologies
- Analog Power-aware Design
- Design examples
- Digital Assisted Analog
- Conclusions



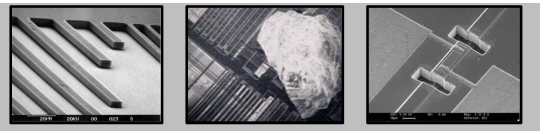
Examples

- Band-pass Sigma Delta
- Sigma-Delta for DVB-H
- Low-power SAR Design



Band-pass Sigma-Delta

- Use of N-path and NTF synthesis



How to obtain band-pass response

- The goal is to have NTF= $(1+z^{-1}+z^{-2})^2$

$$NTF = (1+z^{-1}+z^{-2})^2 = (1+2z^{-1}+3z^{-2}+2z^{-3}+z^{-4})$$

$$= \left[(1+2z^{-2}+z^{-4})+z^{-2}\right]+\left[2z^{-1}+2z^{-3}\right]=$$

$$= \left[(1+z^{-2})^2+z^{-2}\right]+\left[2z^{-1}(1+z^{-2})\right]$$

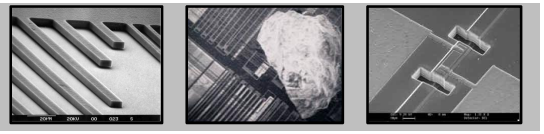
Second order NTF=$(1+z^{-1})^2$ $z \rightarrow z^2$

Extra term

Delay

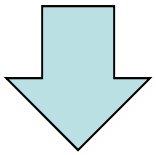
First order $(1+z^{-1})$ $z \rightarrow z^2$

I. Galdi, E. Bonizzoni, P. Malcovati, G. Manganaro, F. Maloberti: "40 MHz IF 1 MHz Bandwidth Two-Path Bandpass ΣΔ Modulator with 72 dB DR Consuming 16 mW" IEEE Journal of Solid-State Circuits, July 2008, pp. 1648-1656.



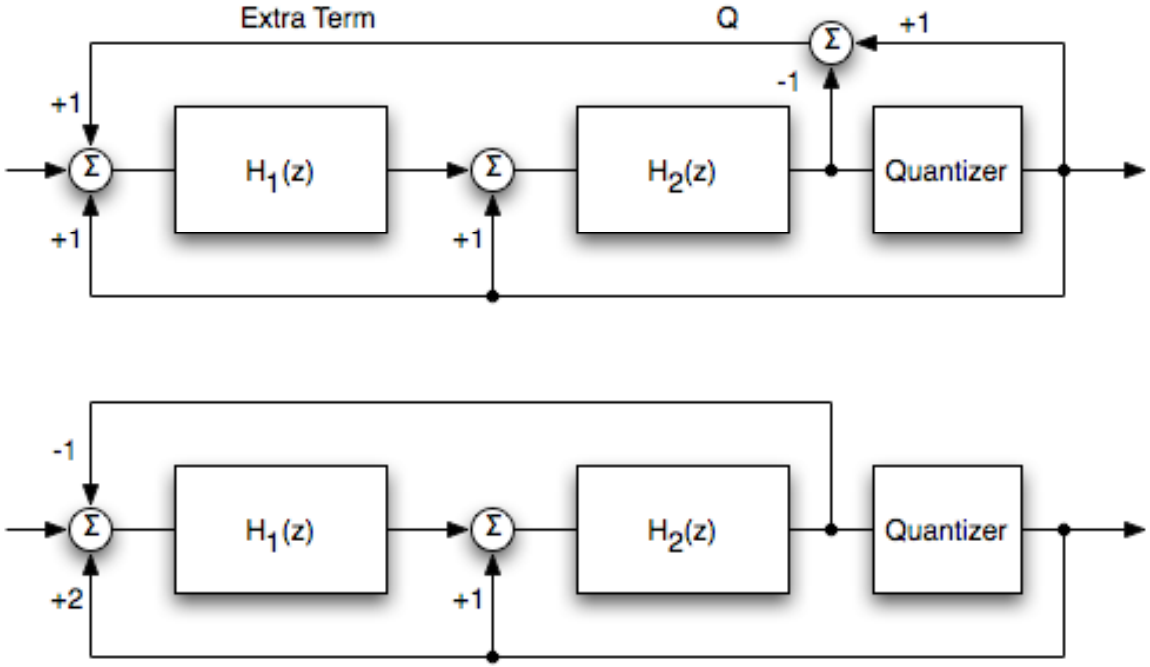
- Path structure
  - Second-order ΣΔ and extra term

$$H(z) = \frac{1}{1 - z^{-1}}$$

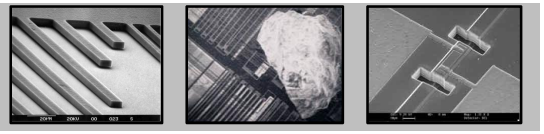


$$H_1(z) = \frac{1}{1 + z^{-1}}$$

$$H_2(z) = \frac{z^{-1}}{1 + z^{-1}}$$



Band-pass Sigma Delta



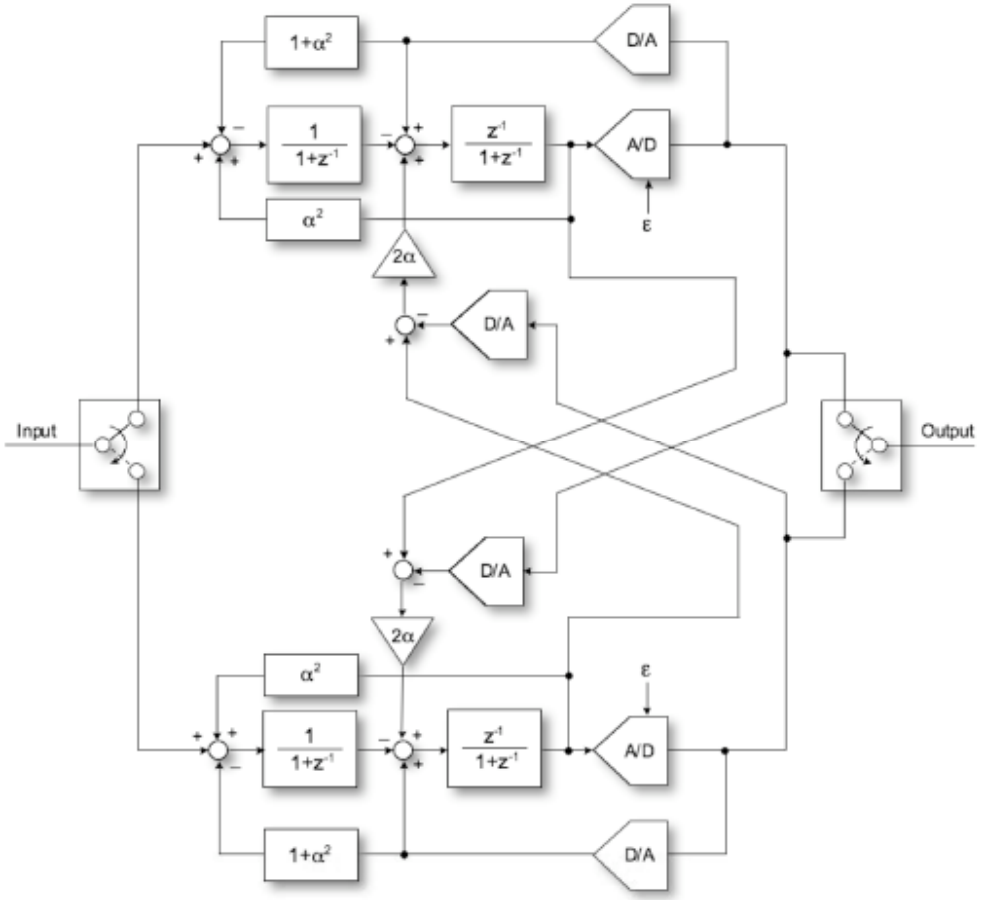
- Modified 2-nd order ΣΔ

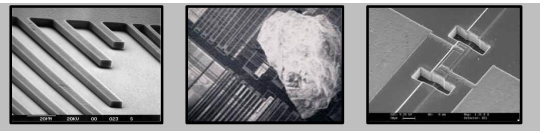
$$H_1(z) = \frac{1}{1+z^{-1}}\,;\; H_2(z) = \frac{z^{-1}}{1+z^{-1}}$$

- Cross coupling
  - Realize the missing terms

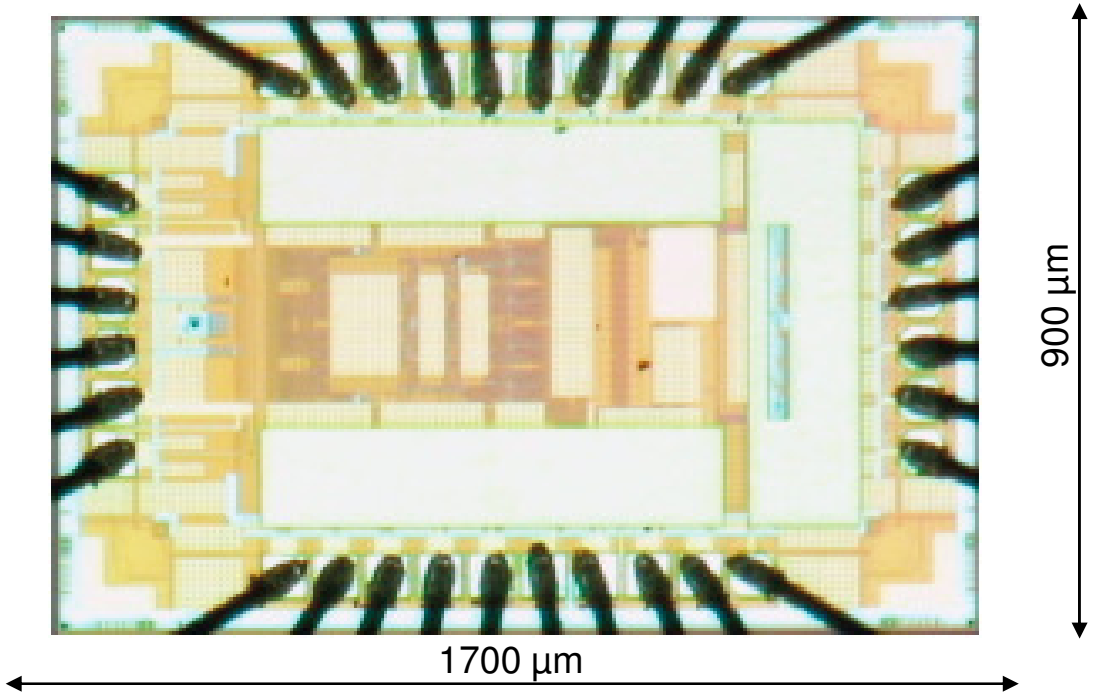
$$\left[2z^{-1}(1+z^{-2})\right]$$

- Op-amp sharing
  - First integrator
  - Second integrator
- Obtain split zeros
  - With suitable coefficients
  - Reduced gains

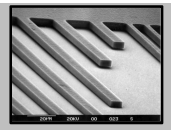
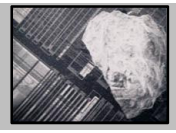
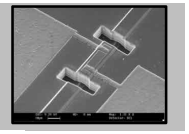




- Implementation technology:
  - 0.18-µm single-poly 5-metal CMOS technology

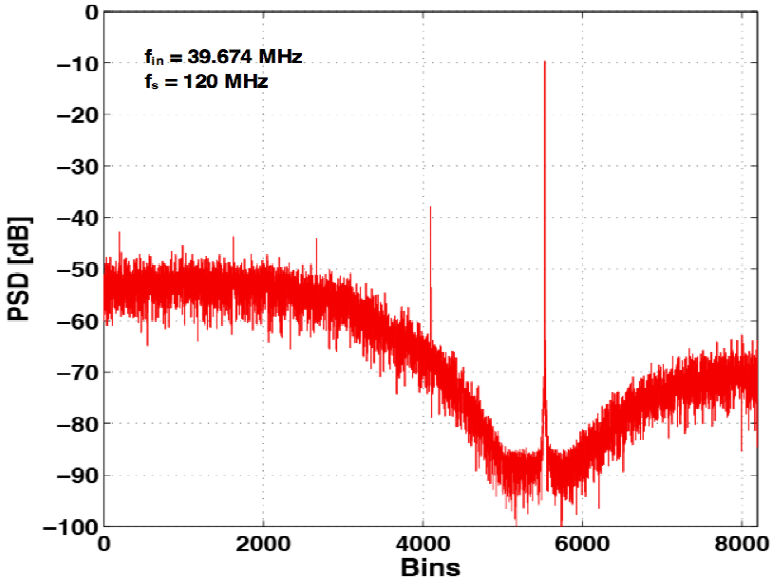


Band-pass Sigma Delta

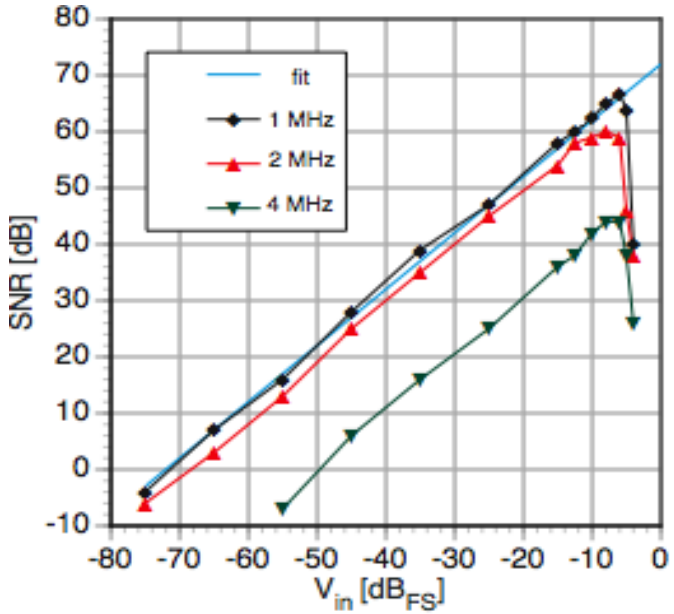




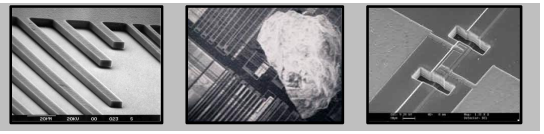
Experimental Results

- SNR = 65.1 dB
- DR = 72 dB
- BW = 1MHz
- F_s= 120 MHz
- IF = 40 MHz



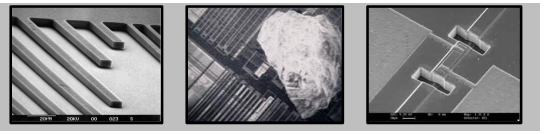
- BW = 1 MHz
  - DR = 72 dB
- BW = 2 MHz
  - DR = 69 dB
- BW = 4 MHz
  - DR = 50 dB





Obtained Experimental Results

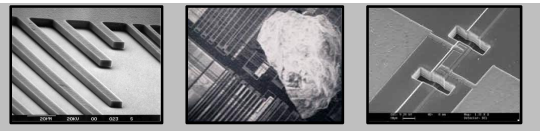
F_s	60 MHz (x 2)
IF	40 MHz
Voltage References	± 0.5 V
Signal Bandwidth	up to 4 MHz
Peak SNR	65.1 dB @ 1 MHz Band
Active Area	0.44 mm^2
Supply Voltage	1.8 V
Power Consumption	16 mW
IMD	68 dB_c
DR	72 dB @ 1 MHz Band



Sigma-Delta for DVB-H

- Scaling (to satisfy the power need) of the architecture

Sigma Delta for DVB-H



ΣΔ

- Minimum Requests of Analog Accuracy.
- Medium-High Resolutions.
- Low OSR.
- Good FoM.

CHALLENGE

Digital Video Broadcasting-Handheld (DVB-H) [1]

Bandwidth	Power Consum.
4-8MHz	<10mW

DVB-H Environment

Cellular-Radio Environment

COMPARABLE

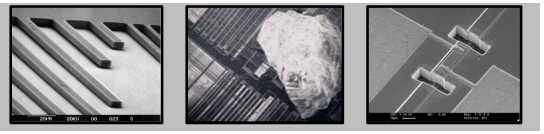
- Personal Digital Assistant (PDA).
- Cellular Phones.
- Pocket PC Equip.

HANDHELD

- Small Size.
- Light Weight.
- Long Battery Life.

COMMON

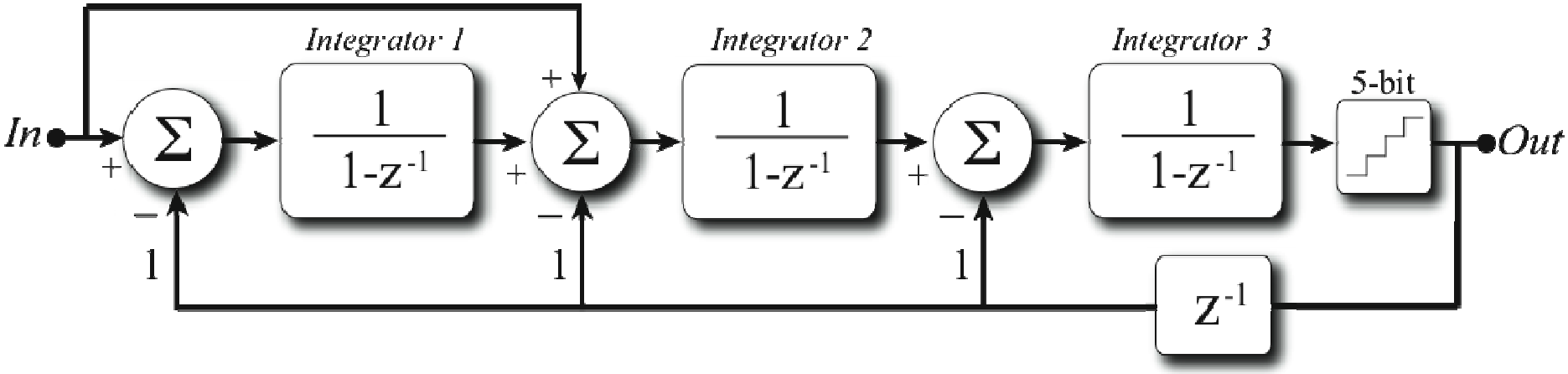
E. Bonizzoni, A. Pena Perez, F. Maloberti, M. Garcia-Andrade: "Third-Order ΣΔ Modulator with 61-dB SNR and 6-MHz Bandwidth Consuming 6 mW"; ESSCIRC 2008, pp. 218-221.

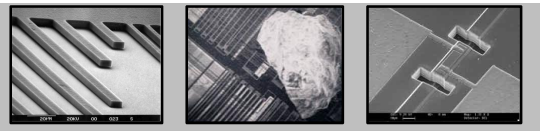


A. REDUCTION OF THE NUMBERS OF OP-AMPS

Basic 3rd Order ΣΔ Modulator, OSR=8:

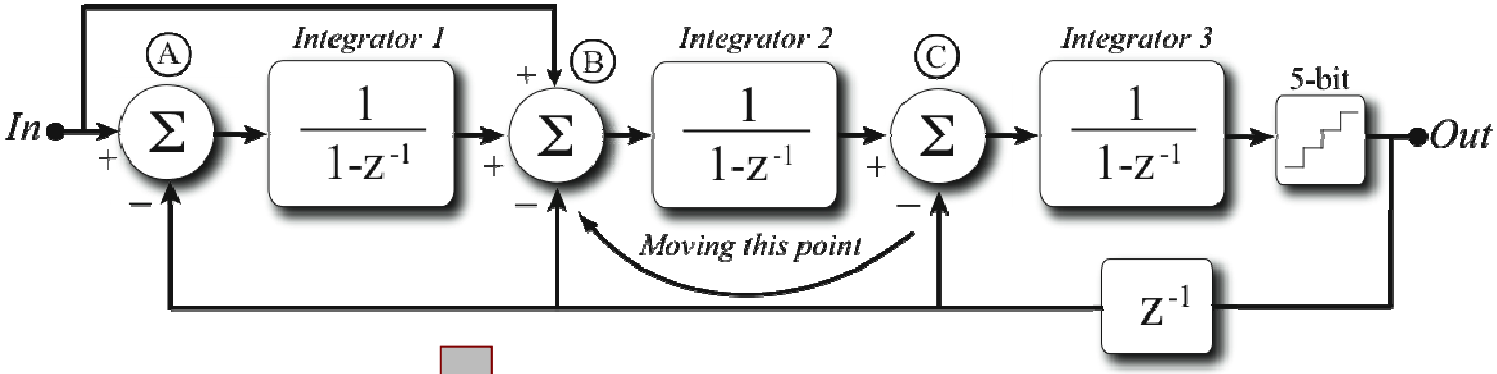
- 3 Integrators without delay.
- NTF = $(1-z^{-1})^3$.
- Feed-forward path *(Limit 1st Op-amp Swing)*.
- 5-bit Quantizer.

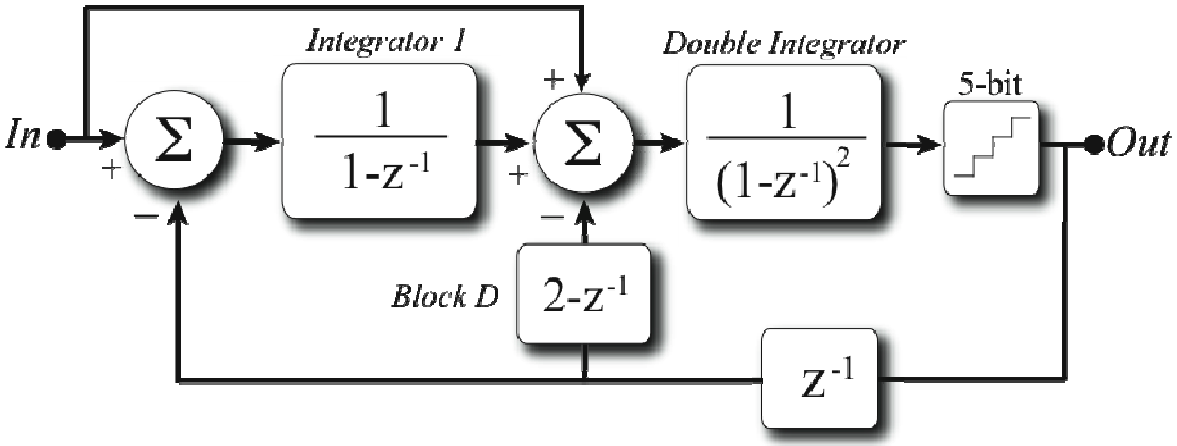




1st STEP

Feedback input 3rd Op-amp is moved at the input 2nd Op-amp.

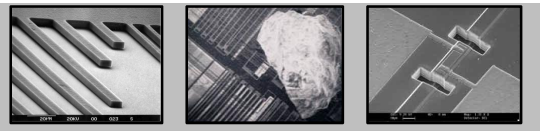




Operation:

$$-1-(1-z^{-1}) = -(2-z^{-1})$$

- ✓ One op-amp is **eliminated**.
- ✓ A **third-order** modulator with only **two integrators** is made.

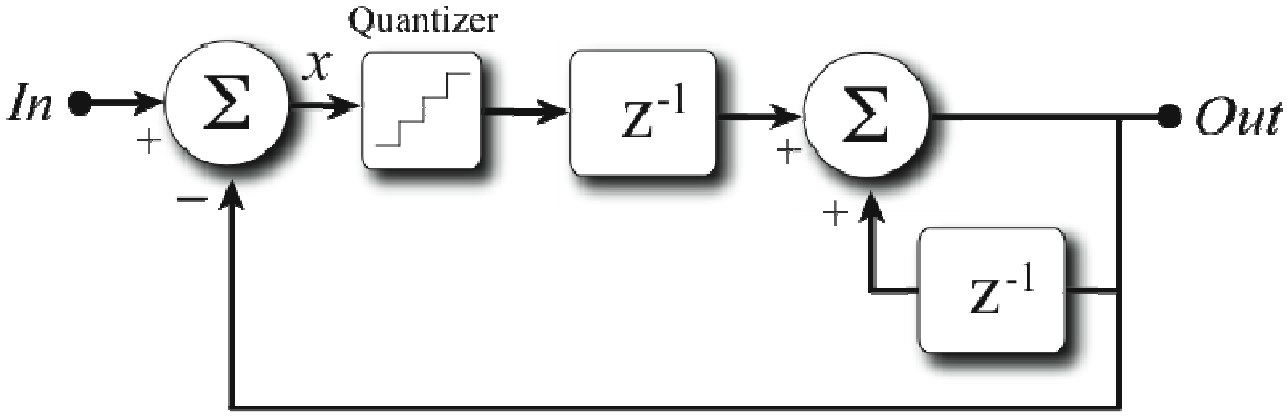


B. REDUCTION OF THE NUMBERS OF COMPARATORS

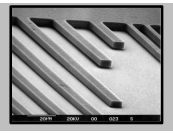
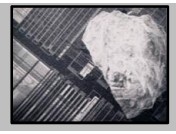
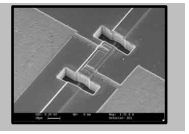
2nd STEP | Use a 5-bit quantizer with reduced input range.

Is more convenient to quantize

$V_O(n) - V_{O,Q}(n-1)$ | Previous quantization



✓ Considering a 5-bit quantizer the number of comparators decreases from 31 to 18.

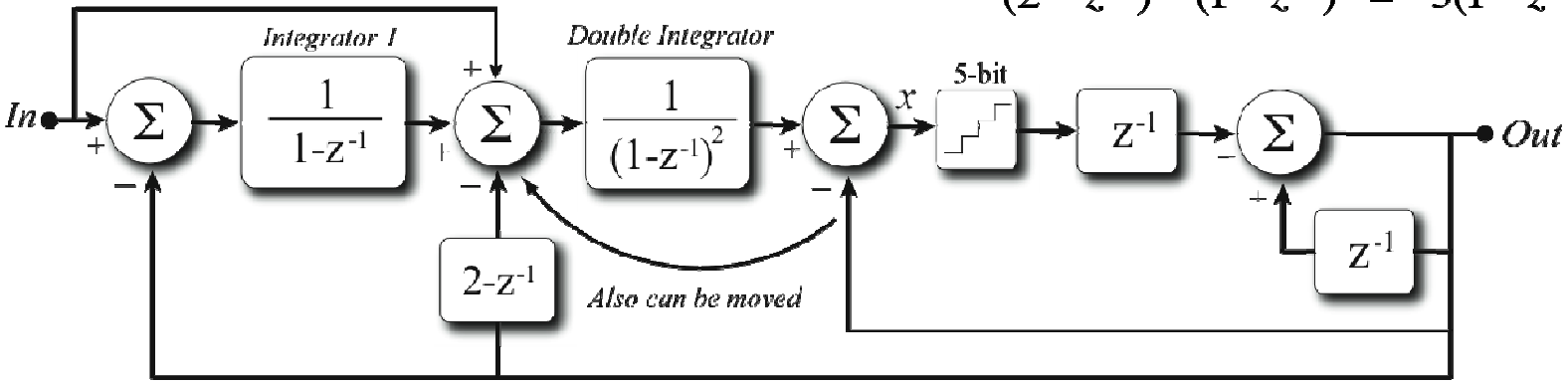
B. REDUCTION OF THE NUMBERS OF COMPARATORS

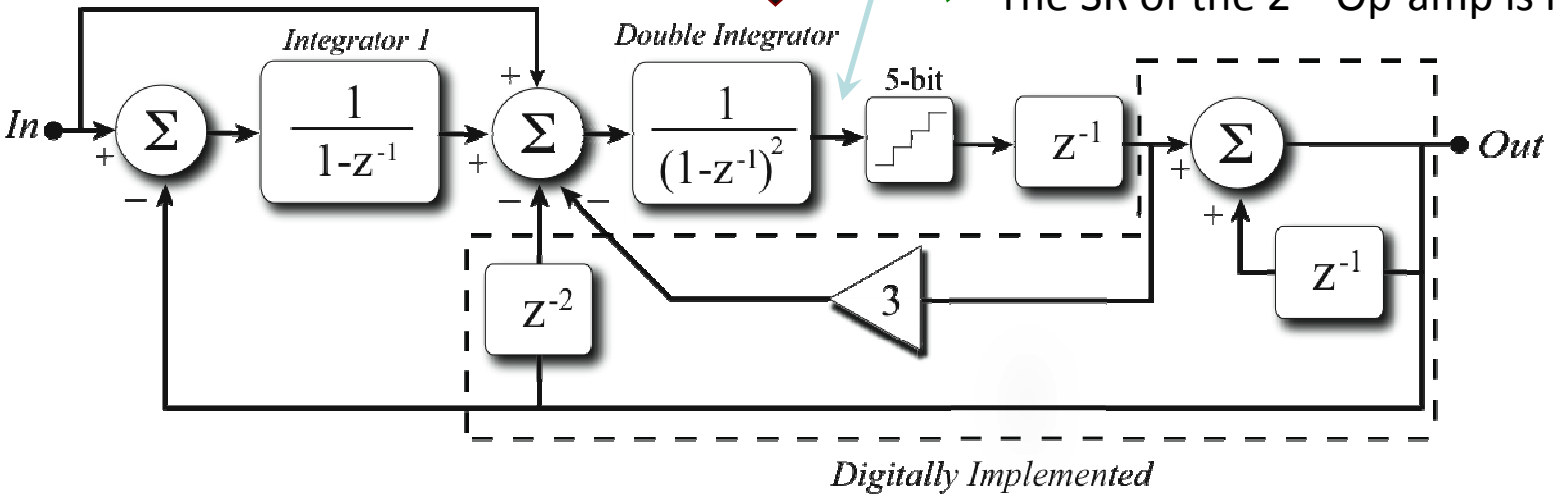
3rd STEP

Feedback input Quantizer is moved at the input Double Integrator.

Operation:

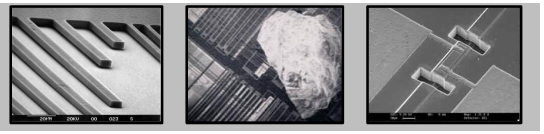
$$-(2-z^{-1})-(1-z^{-1})^2=-3(1-z^{-1})-z^{-2}$$





✓ The SR of the 2nd Op-amp is relaxed.

Sigma Delta for DVB-H



TWO OP-AMPS

SCHEME	Fully-Differential Folded Cascode
CMFB	Switched-Capacitor

INTEGRATORS

1st STAGE	Input Capacitor C_i = 80 fF
2nd STAGE (Double Int.)	Feedback Capacitors C_f = 40 fF

Input of the Double Integrator uses two DACs:

‼ Avoid interferences.

‼ Reduce the Digital Processing.

✗ Additional Power: 15% of the total.

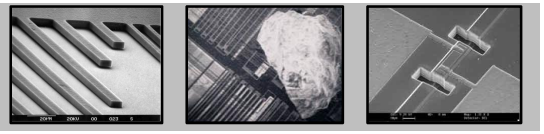
5-bit DAC

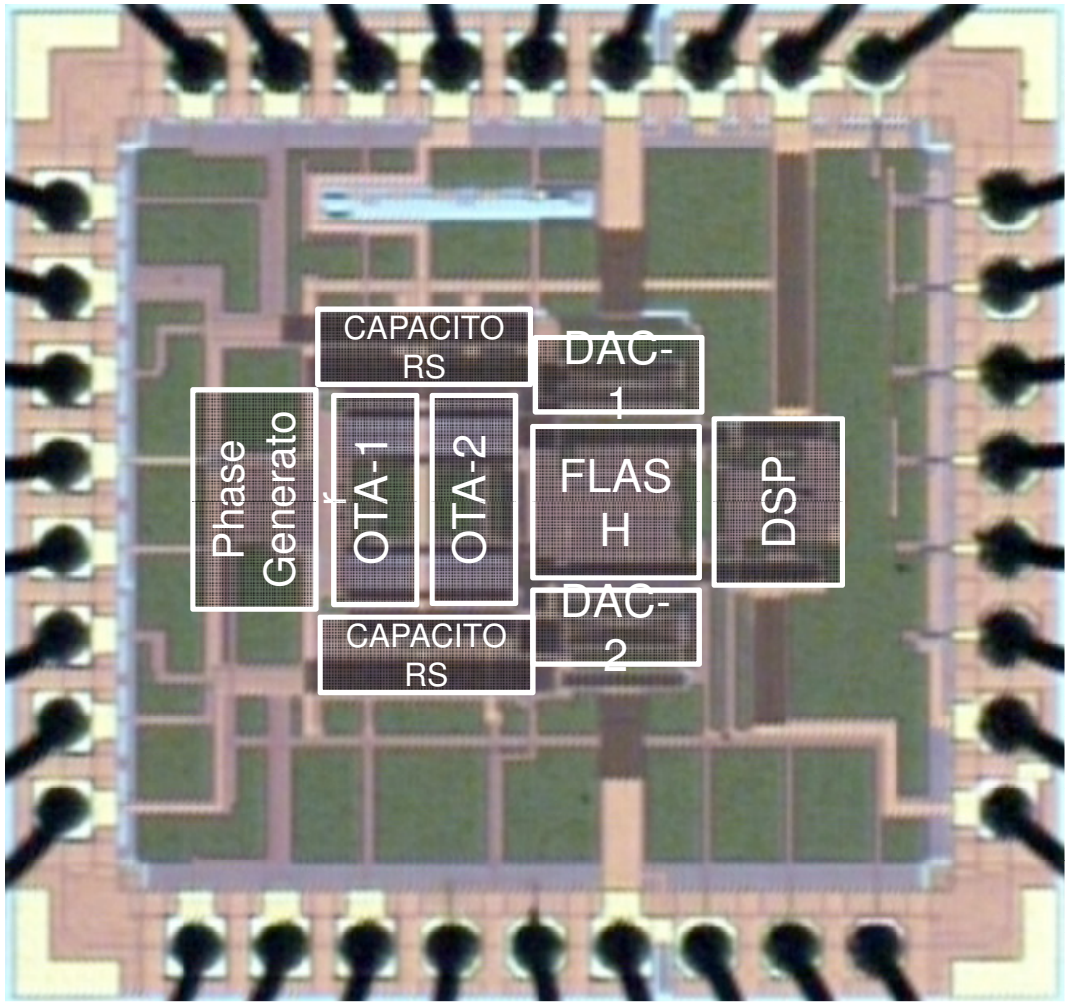
SCHEME	Resistive Divider 32 x R=200 Ω

TABLE I. OP-AMPS PERFORMANCE

Feature	First Integrator	Double Integrator
Supply Voltage	1.8-V	1.8-V
Bandwidth	580-MHz	890-MHz
Slew-Rate	300-V/µs	400-V/µs
Gain	51-dB	48-dB
Power Consumption	1.9-mW	2.4-mW

Sigma Delta for DVB-H



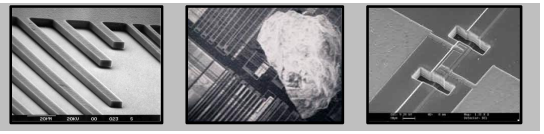


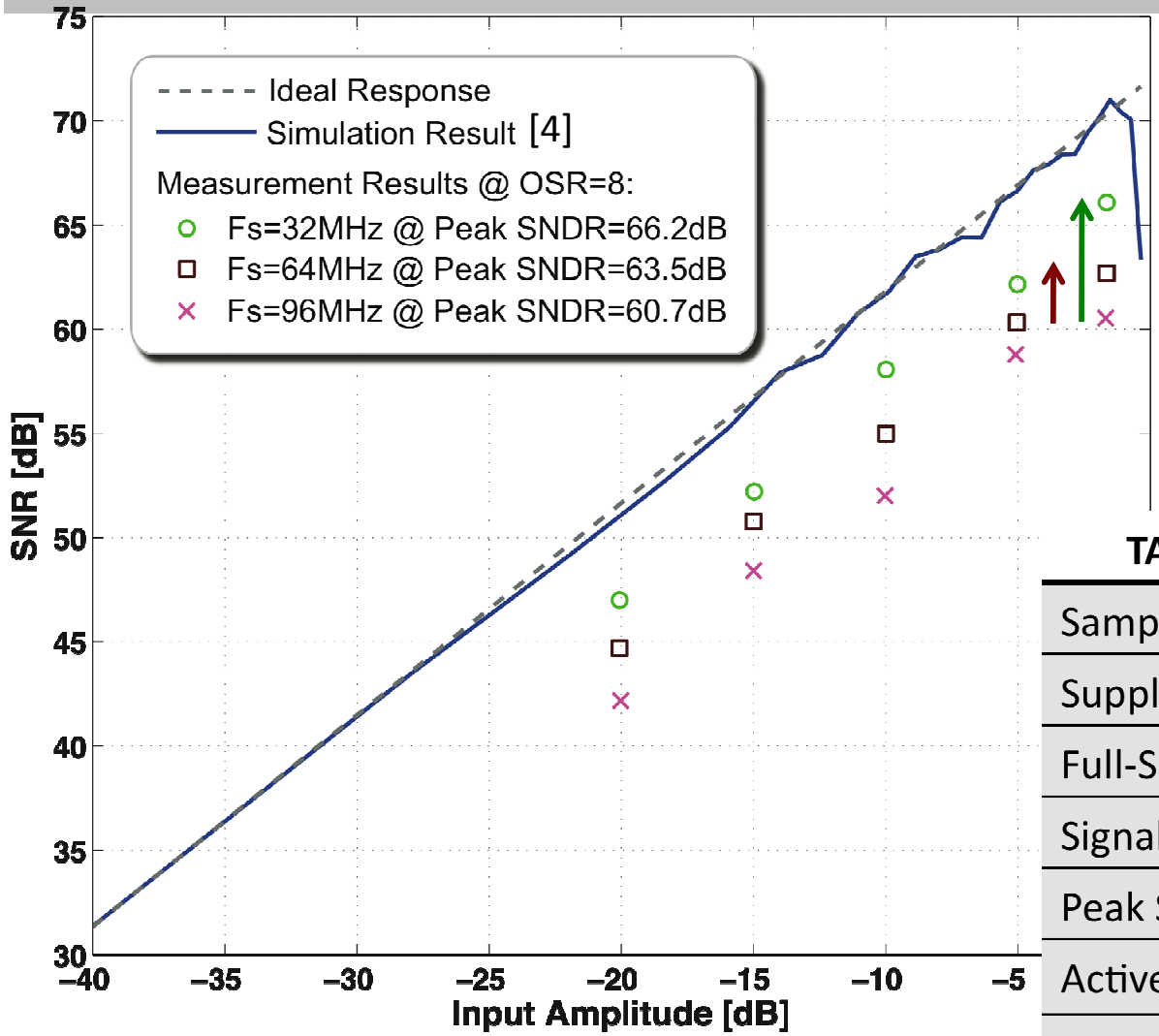
CHIP MICROPHOTOGRAPH

Third-Order ΣΔ Modulator

Technology:	0.18-µm CMOS Double poly
Metal Levels:	5
Active Area:	0.32 µm²
Package:	40-pins LLP
Power Supply:	1.8V

Sigma Delta for DVB-H

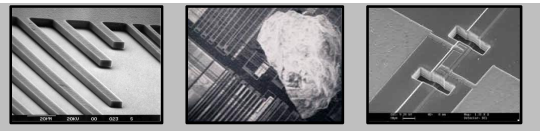




[4] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, **"Behavioral Modeling of Switched-Capacitor Sigma-Delta Modulators"**, IEEE Trans. on Circuits and Systems – I: Funamental Theory and Applications, vol. 50, no. 3, pp. 352-364, March 2003.

TABLE II. PERFORMANCE SUMMARY

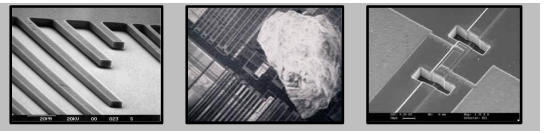
Sampling Frequency	96 MHz
Supply Voltage	1.8 V
Full-Scale Input Signal	600 mV p.p
Signal Bandwidth	6 MHz
Peak SNDR	60.7 dB
Active Area	0.32 μm^2
Power Consumption	6.18 mW
FoM	0.59 pJ/Conversion



Low-power SAR Design

- Use of time-domain comparator

Low-Power SAR



LOW power is the most relevant design concern for battery-powered mobile applications.

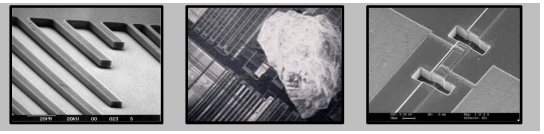
Since the ADCs operate at 10s of MS/s with 10b to 12b, the pipeline ADC is the commonly used architecture because of its power efficiency.

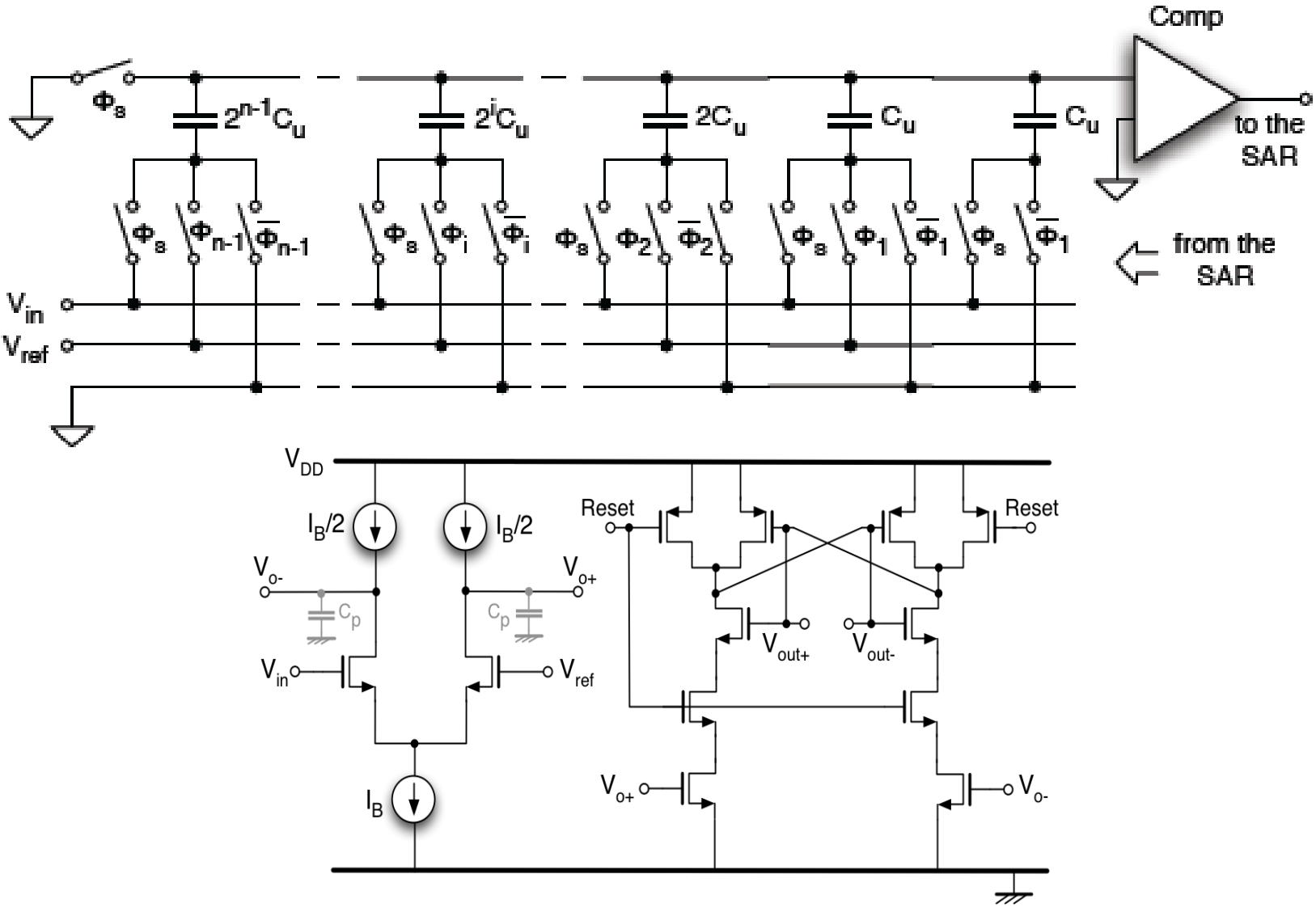
Recently, the successive approximation resistor (SAR) architecture has re-emerged as a valuable alternative to the pipelined solution.

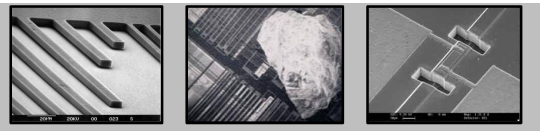
The techniques used for low speed can be re-used for high speed.

This example is a state-of-the-art FOM low speed.

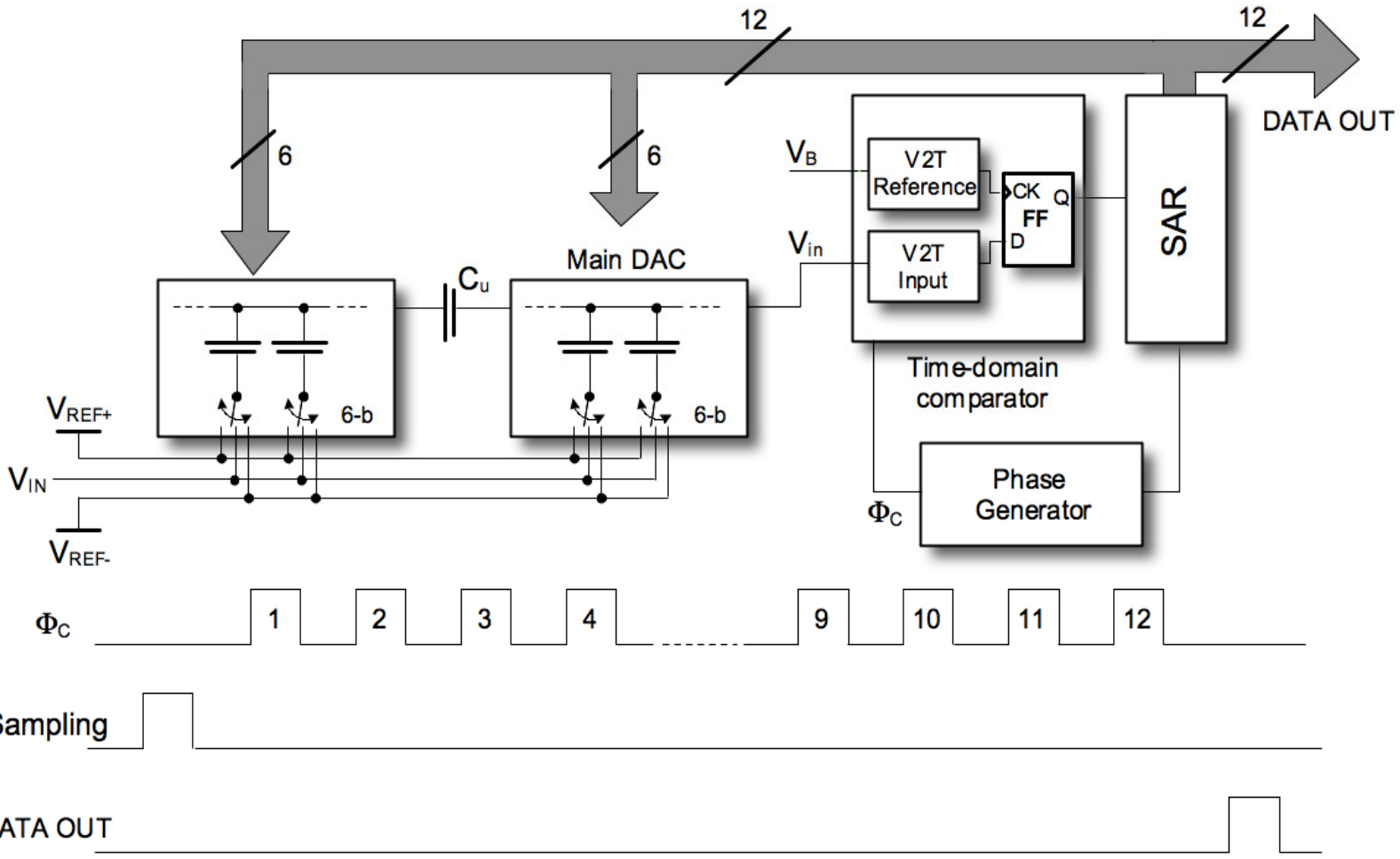
Low Power SAR



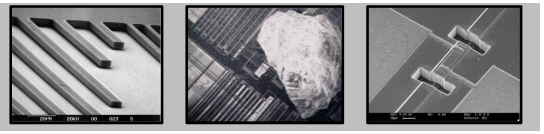




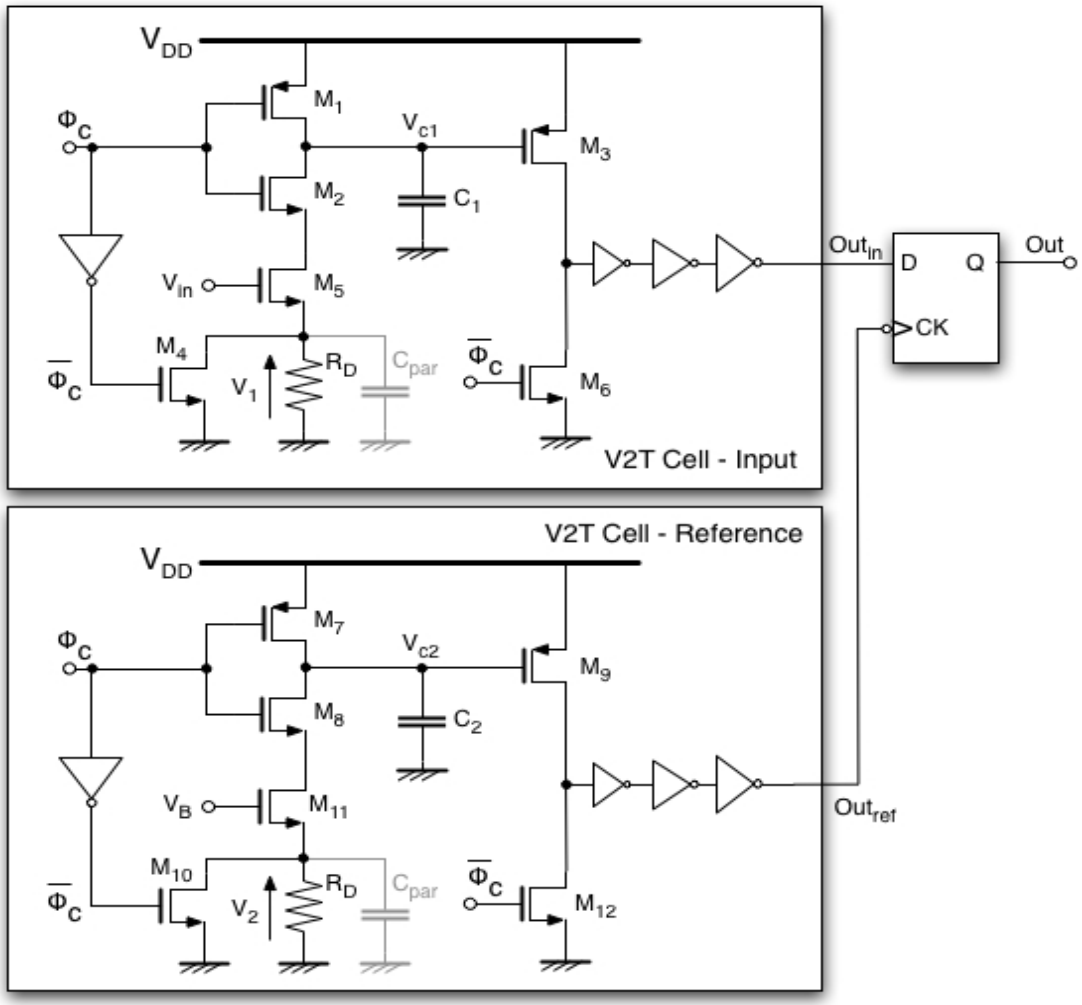
Use of unity attenuation capacitor and V2T comparator

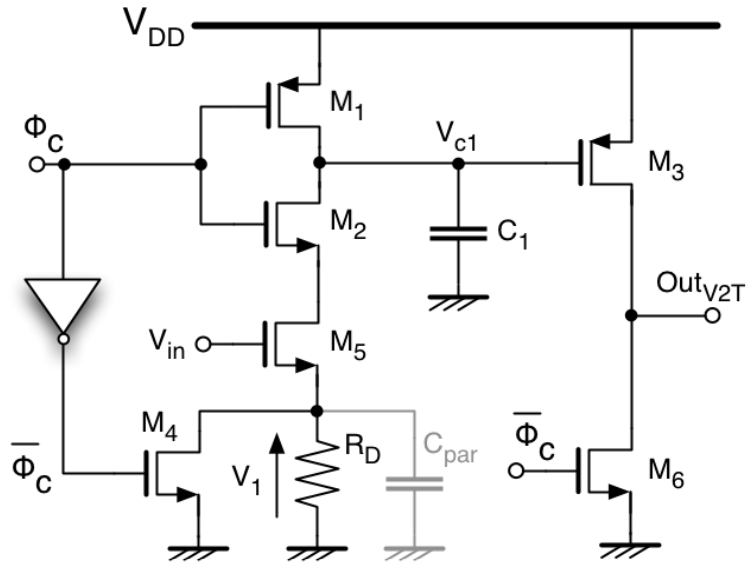


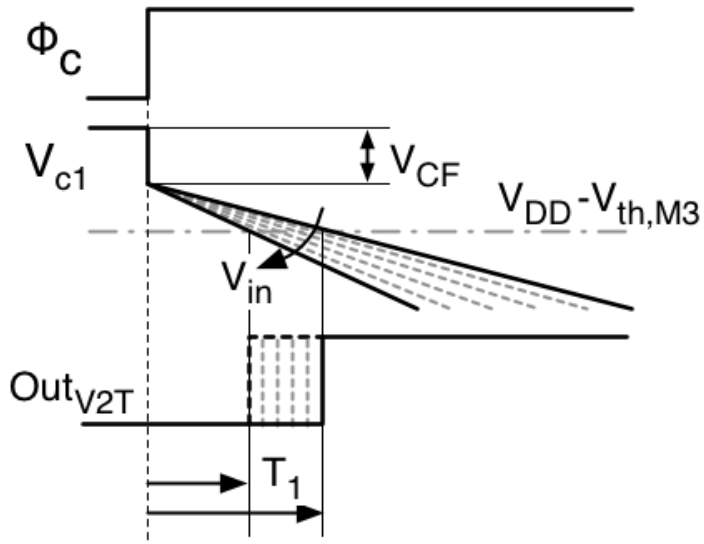
A.Agnes, E. Bonizzoni, P. Malcovati, F. Maloberti: "A 9.4-ENOB 1V 3.8µW 100kS/s SAR ADC with Time-Domain Comparator"; ISSCC 2008, pp. 246-247.



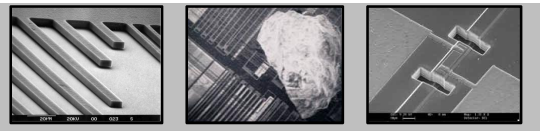
The time-domain Comparator



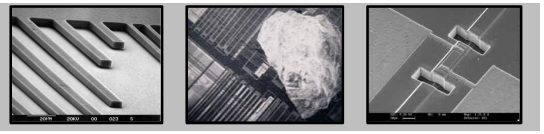




Low-Power SAR



	[3]	[4]	[5]	[6]	[7]	This Work
Technology	0.18 µm	90 nm	0.18 µm	90 nm	0.18 µm	0.18 µm
Supply Voltage	1 V	1 V	0.83 V	1 V	0.6 V	1 V
Sampling Rate	100 kS/s	20 MS/s	111 kS/s	40 MS/s	100 kS/s	100 kS/s
ENoB	10.55	7.8	7.46	8.56	8.7	9.4
ower Consumtion	25 µW	290 µW	1.16 µW	820 µW	1.3 µW	3.8 µW
FoM	167 fJ/c.-l.	65 fJ/c.-l.	60 fJ/c.-l.	54 fJ/c.-l.	31 fJ/c.-l.	56 fJ/c.-l.



OUTLINE

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- Managing the power budget
- Challenges of State-of-the-art Technologies
- Analog Power-aware Design
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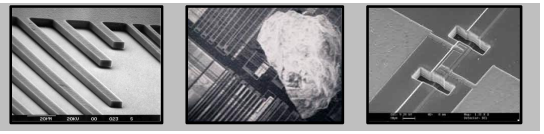
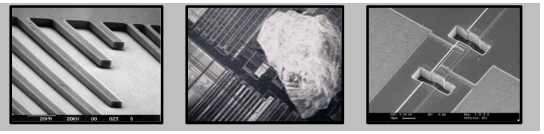
Digital Calibration

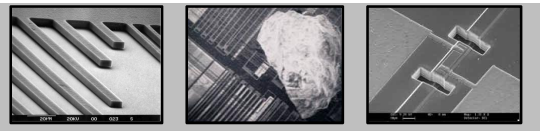


- The real advantage of thin line-width technologies is the huge number of transistors available with which we can perform complex digital functions and dynamically store huge data
- Foreground (or offline) calibration, that uses specific time-slots for calibration, and background calibration (or online), that performs the circuit calibration during the normal operation of the circuit
  - Background calibration is more complex than foreground because it requires to ensure normal operation together with calibration.
  - There are two main approaches: the use of circuit redundancy or the use of test terms added to the signal.



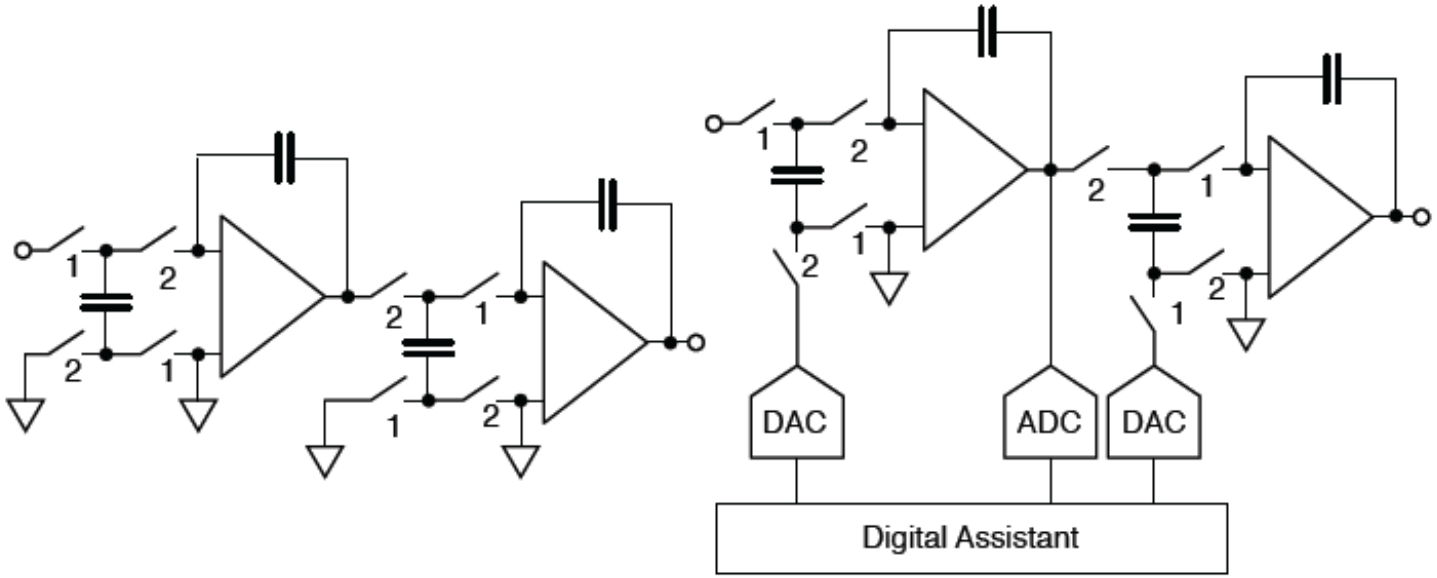
ADC Energy versus Digital Energy

- Interesting metric to look at
  - How many digital gates can you toggle for the energy needed in one A/D conversion?
- Example
  - Standard digital gates (NAND2) in 0.13mm CMOS consume about 6nW/Gate/MHz
    - Energy/Gate = 6fJ
  - State-of-the-art 10-bit ADC consumes 0.1mW/MSps
    - Energy/Conversion = 0.1nJ
  - Energy equivalent number of gates
    - 16.7K

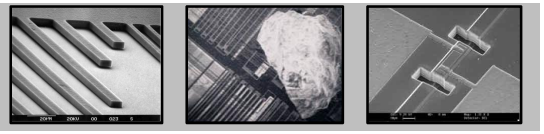


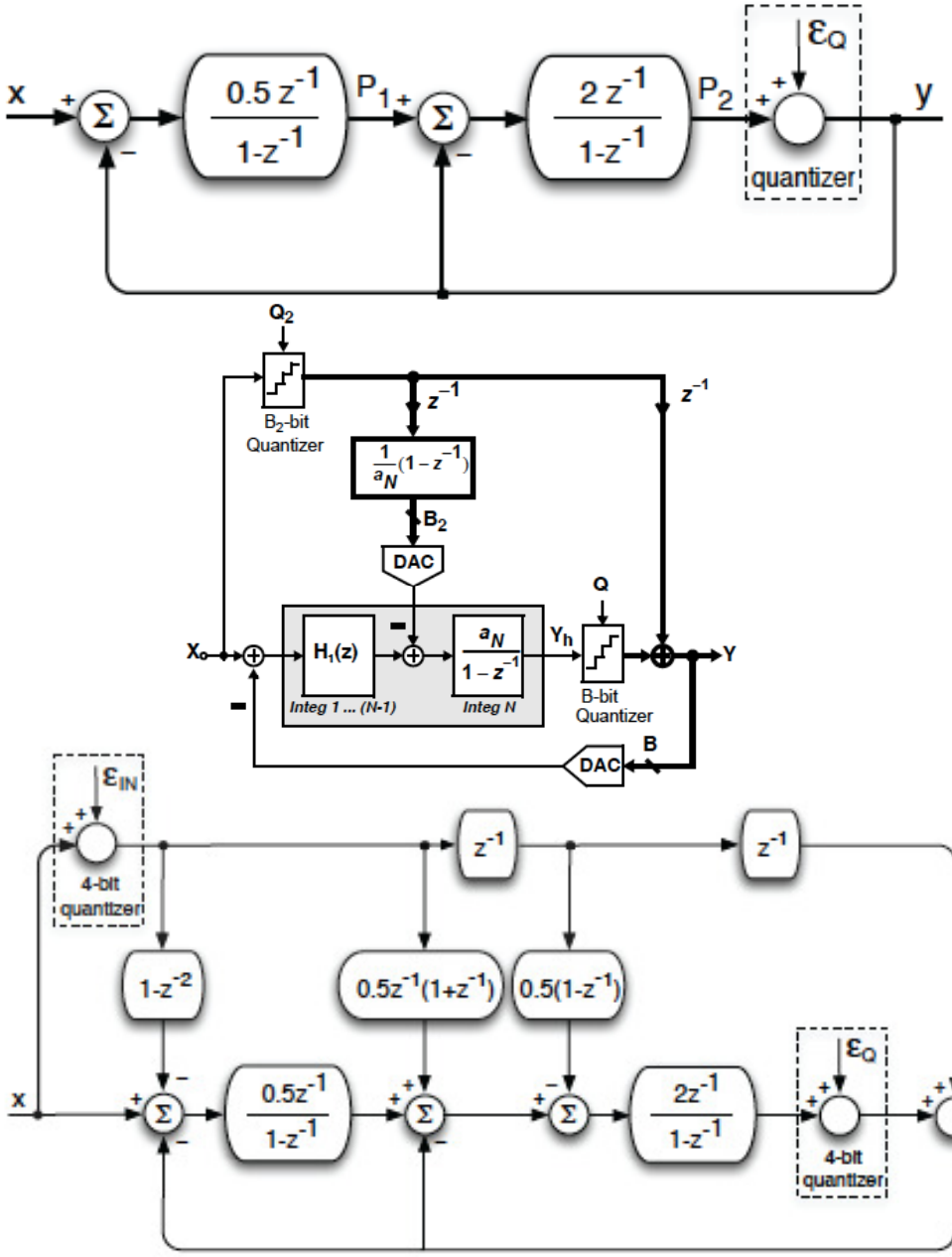
Digitally Assistant Analog

- The digital assistant analog techniques are now in an infancy phase.
- It is expected that the method will significant grow for helping, in addition to digital calibration, the analog designer in facing the limits of DSM technologies

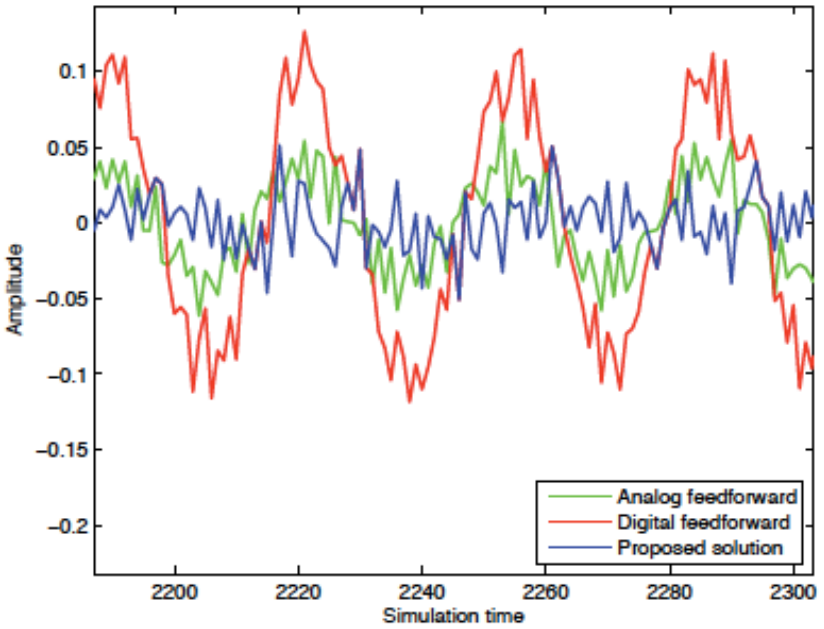


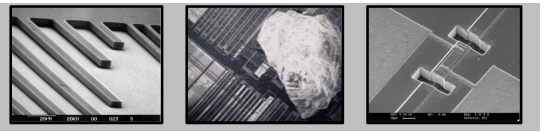
Digital Control of Analog Circuits





Use of digital representations of signals to improve analog performances of sigma-delta modulators





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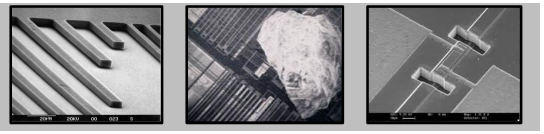

- Portable and autonomous applications need power efficient data converters
- Solutions involve architecture optimization, trade-off and, it may be, choice of the optimal technology
- Remember that the optimum can require extra-bit in the quantizer to compensate for power and speed needs
- Examples are just examples and not an indication of a unique path to find the optimum
- Consider more and more the advantages offered by the digital processing at zero cost.


Thank you!!!