Methodology for Energy-Efficient Design of Digital Circuits

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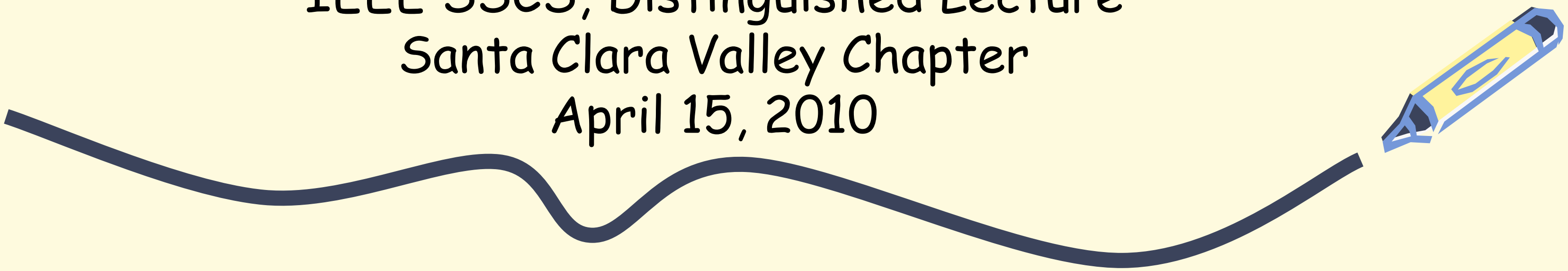


*with acknolwedgment to contributions of my former students:
Dr. Hoan Dao, AMD, Austin, TX and
Dr. Bart Zeydel, Plato Networks

Summary of the Presentation

Energy Efficiency of Digital CMOS Circuits

- Problems
- Energy-Delay Relationship
- Minimizing Energy for a given delay
- Methodology
- Determining the best structures for high-performance system
- Implications on the architecture

Challenges in High-Performance Design

- ❑ Optimizing for **power** – *not speed*! (or maximizing speed under the power budget)

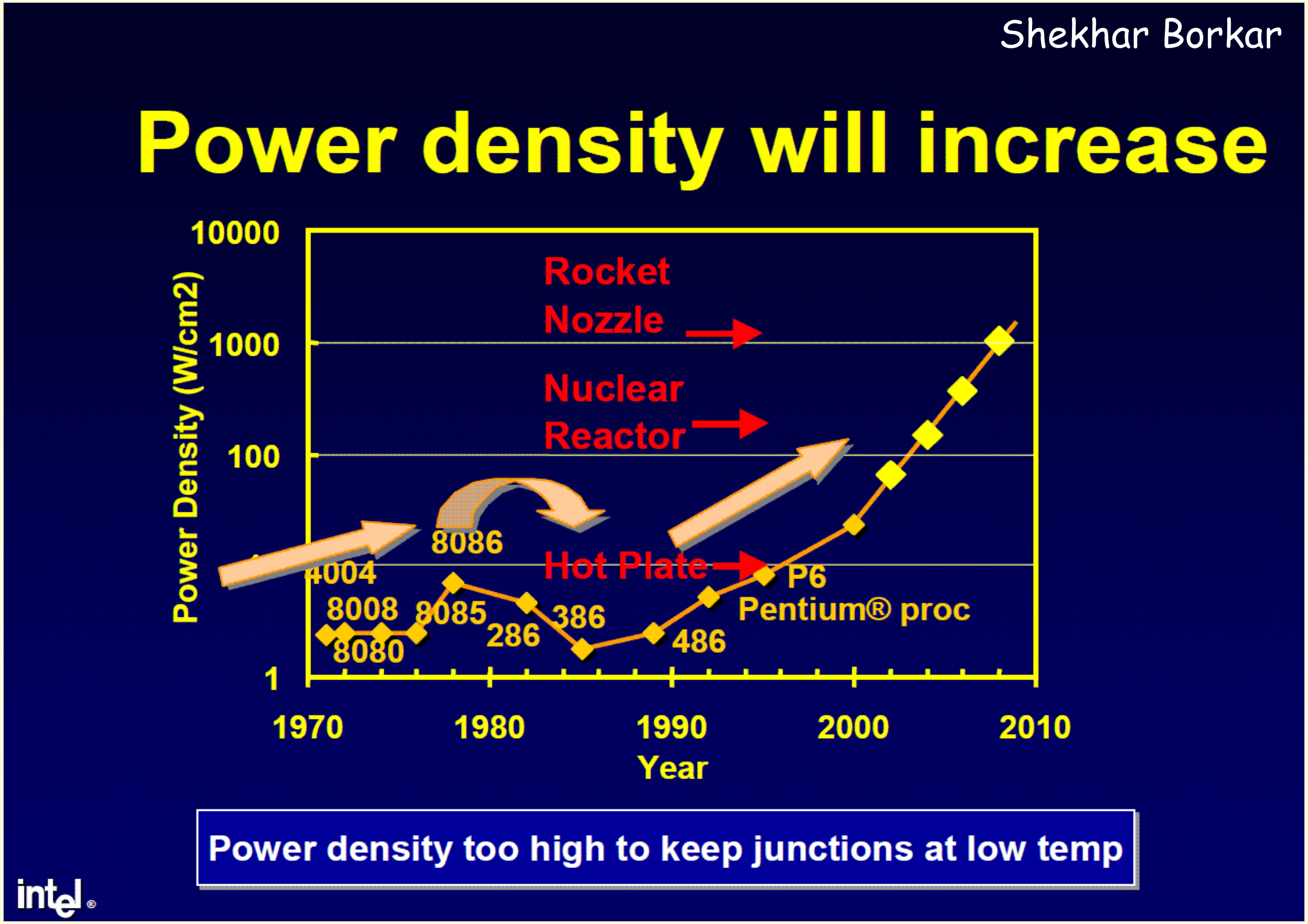
- ❑ Logical Effort (LE) optimizes for speed, regardless of power i.e. brings us in the worse energy spot.

- ❑ Our method optimizes for:

  power @ given speed or ***speed @ given power***

- ❑ We are developing new approaches for power efficiency (overlooked by delay optimization) applicable to:
  - Circuit structures
  - Design techniques
  - Energy-Delay Space
  - Creation of optimal Standard cell (ASIC) libraries

Motivation for Energy Efficient Design



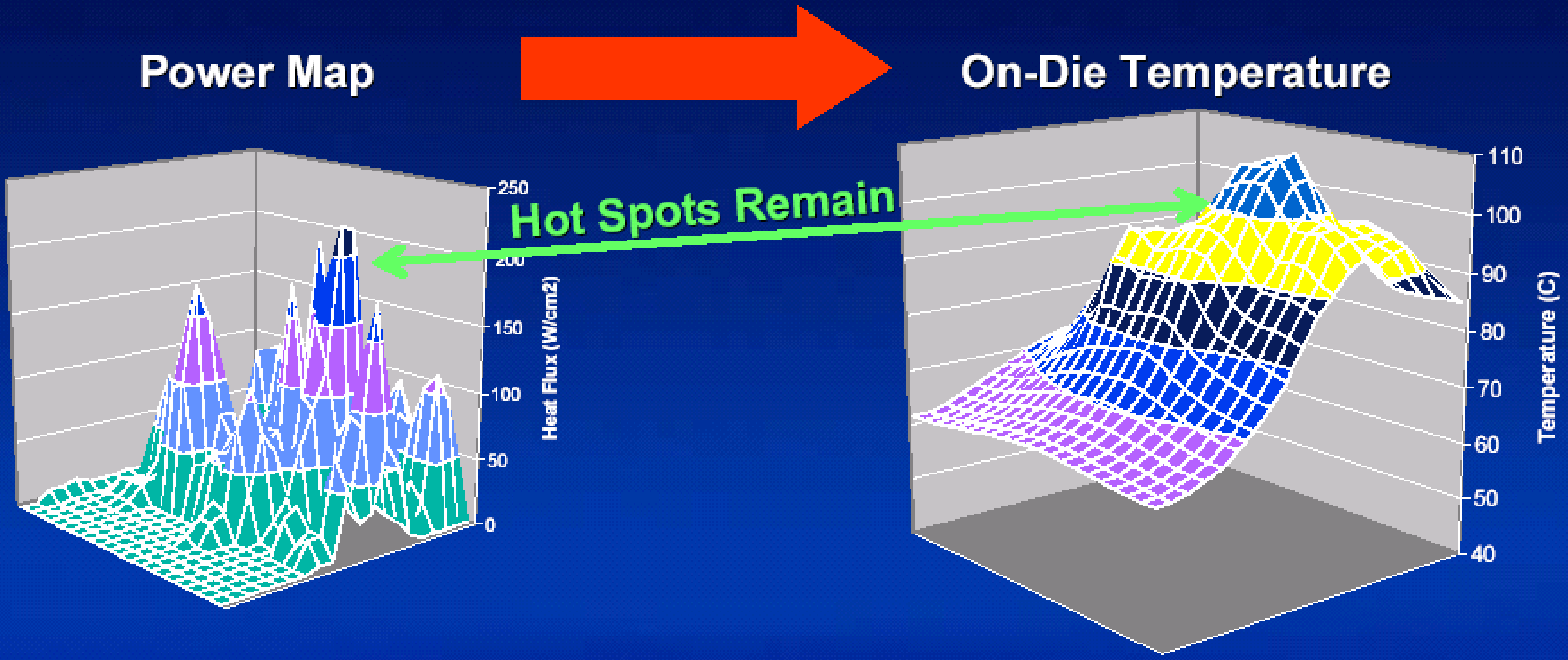
Shekhar Borkar

Power density will increase

Power density too high to keep junctions at low temp

- Power density passed the level found in the Nuclear Reactor !
- Power density degrades the reliability and speed.

Power Density: The Future



Power Map

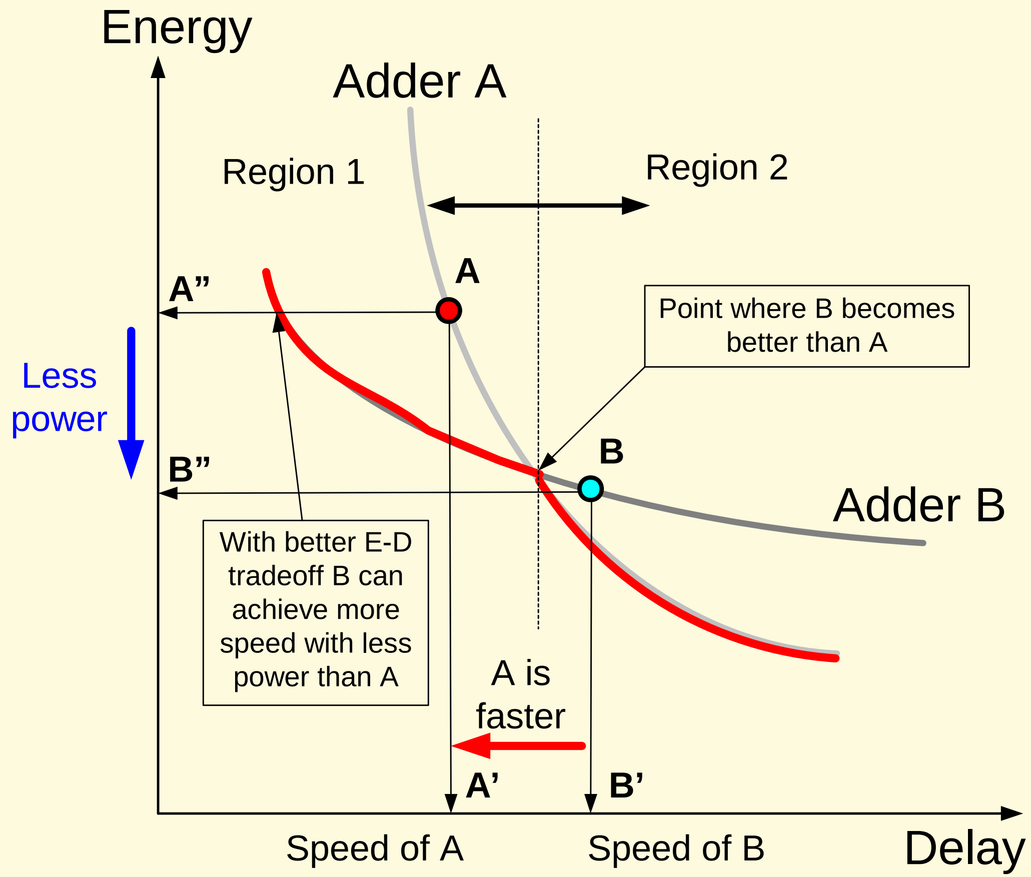
On-Die Temperature

Hot Spots Remain

- With high power density, cannot assume uniformity
  - As die temperature increases, CMOS logic slows down
  - At high die temp., long-term reliability can be compromised

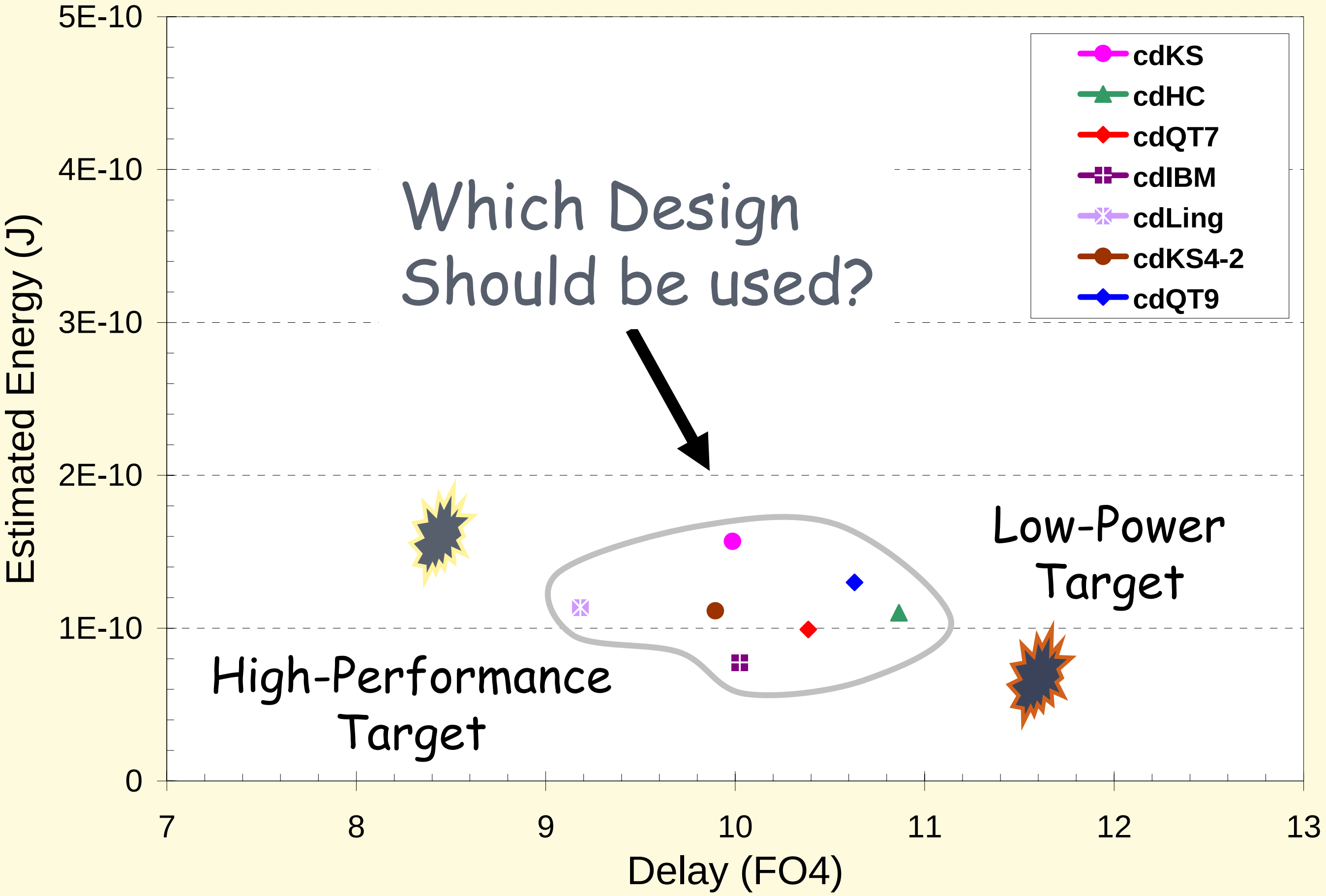
Energy-Delay Relationship

Energy-Delay Space View


Energy
Adder A
Region 1
Region 2
A
A"
Point where B becomes better than A
Less power
B
B"
Adder B
With better E-D tradeoff B can achieve more speed with less power than A
A is faster
A'
B'
Speed of A
Speed of B
Delay

- Must look at Energy-Delay Space of designs

Energy-Delay Space View

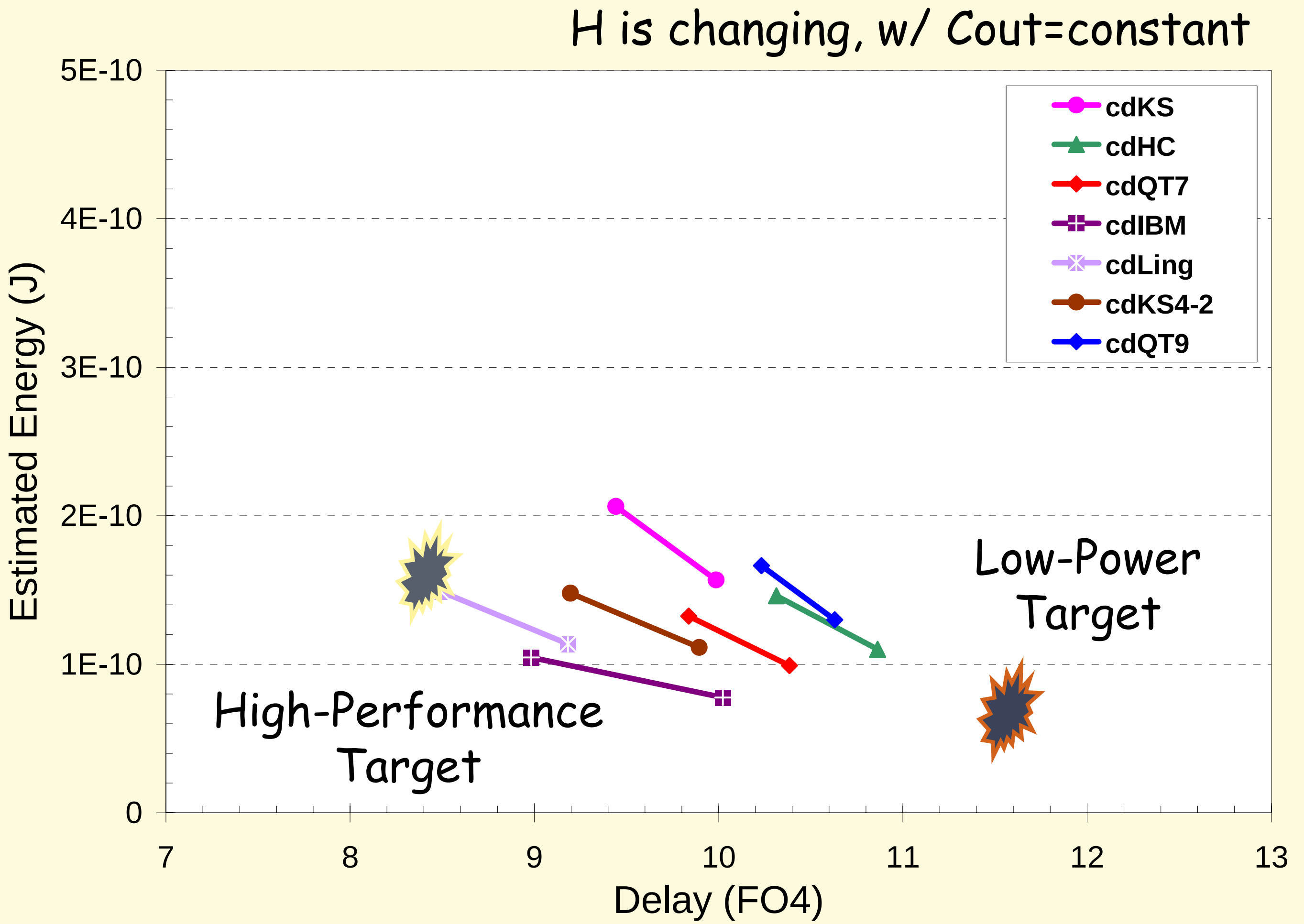


Which Design Should be used?

Low-Power Target

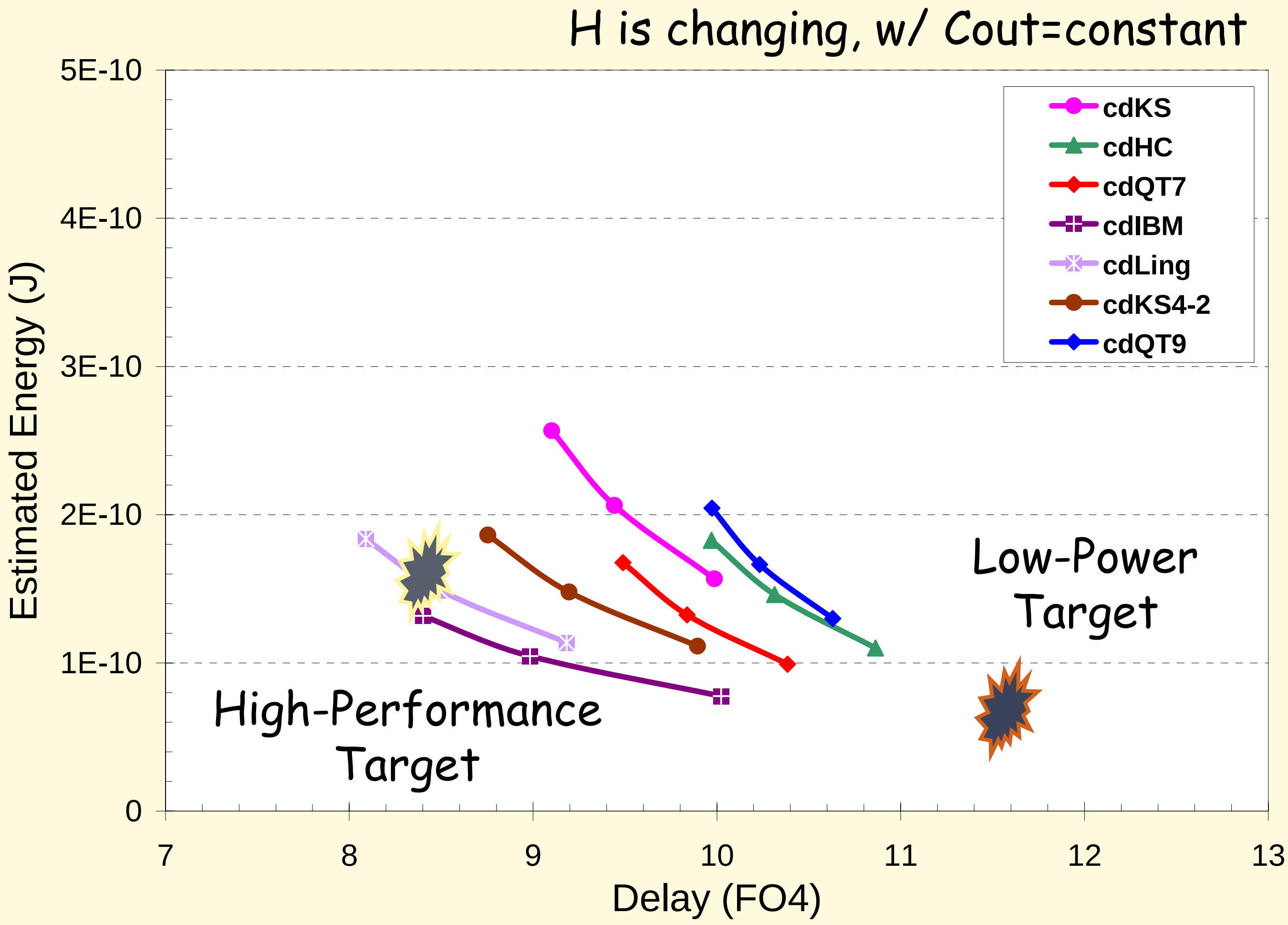
High-Performance Target

Energy-Delay Space View



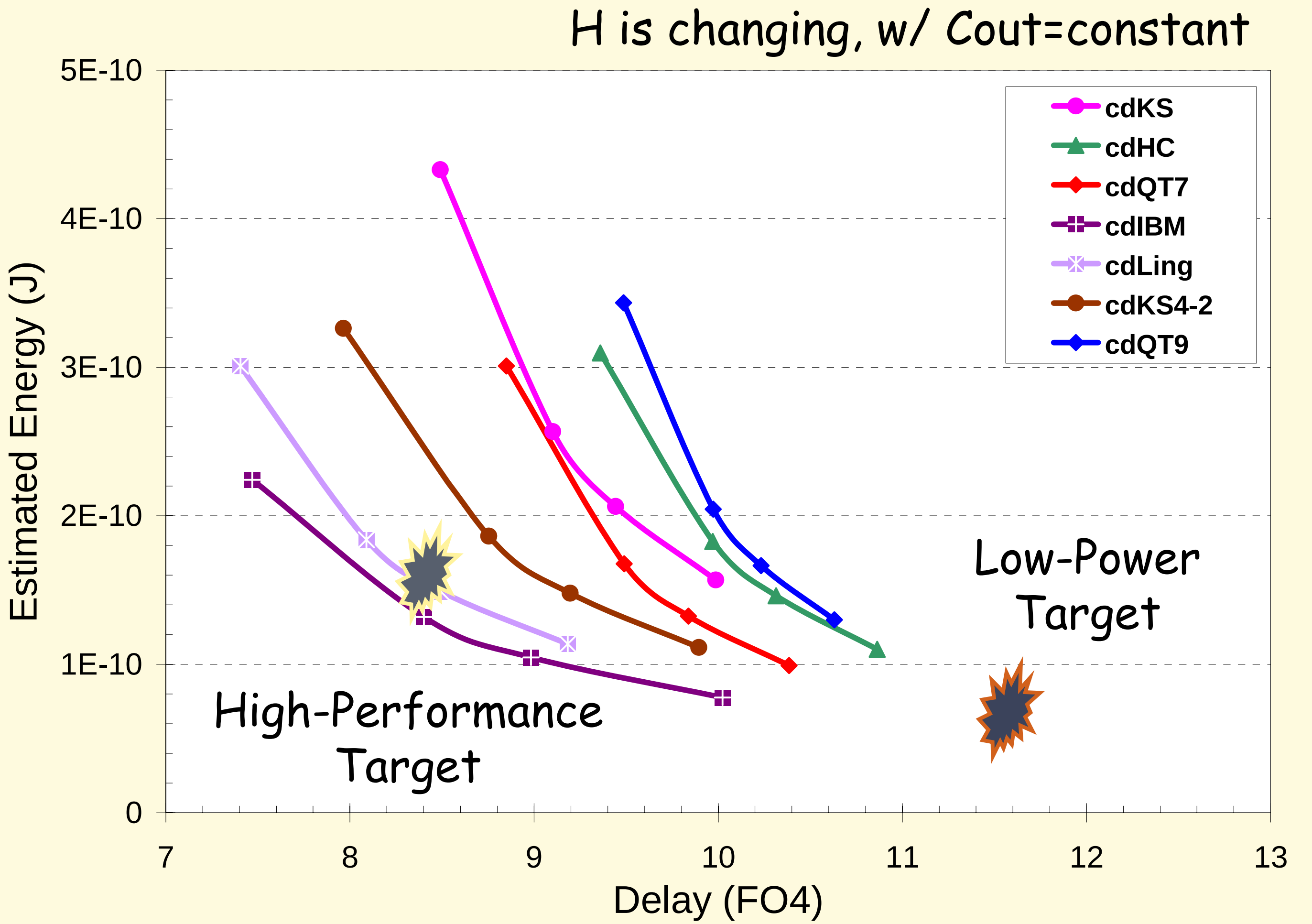
- Begin to see characteristics of designs

Energy-Delay Space View



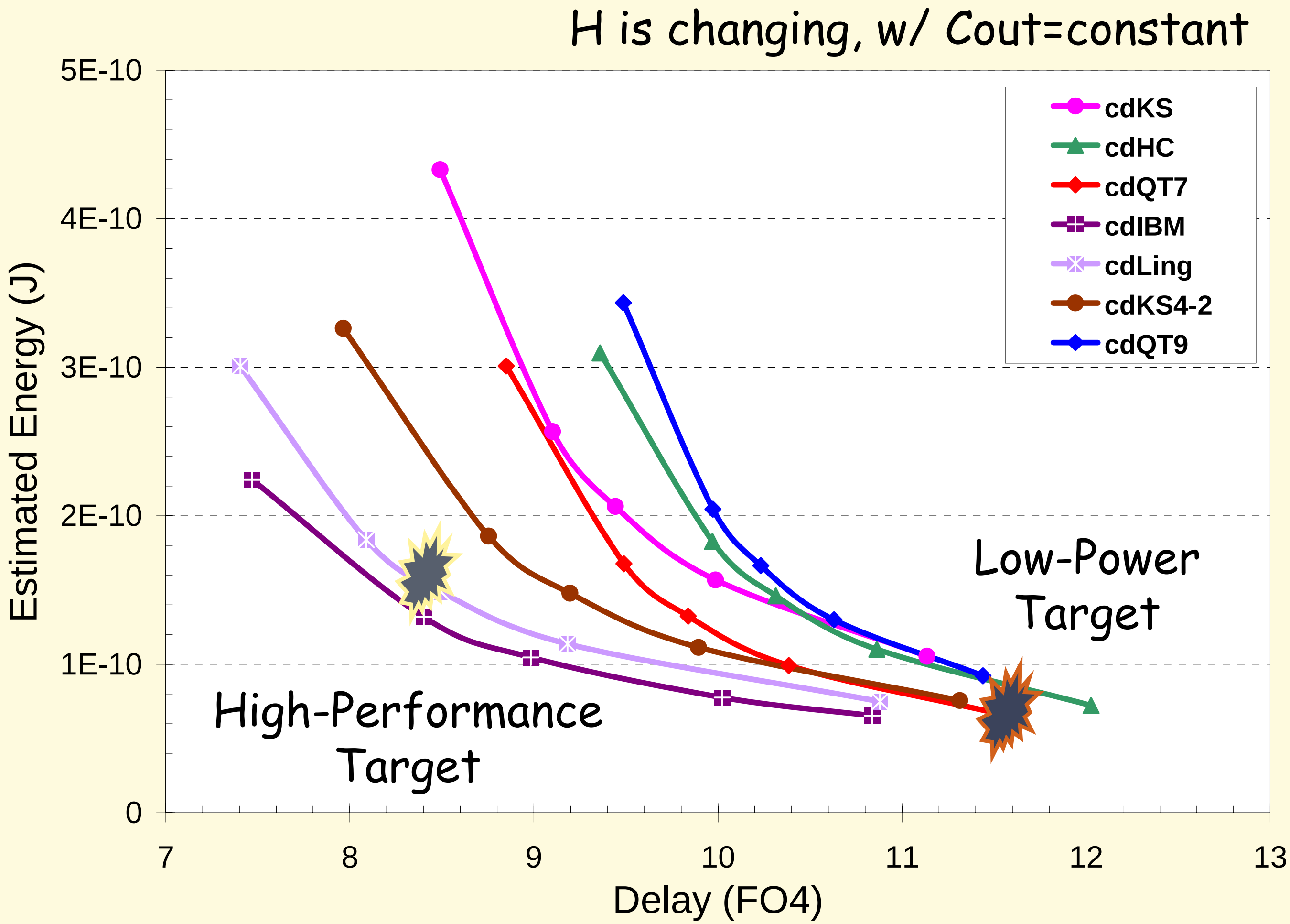
- Begin to see characteristics of designs

Energy-Delay Space View



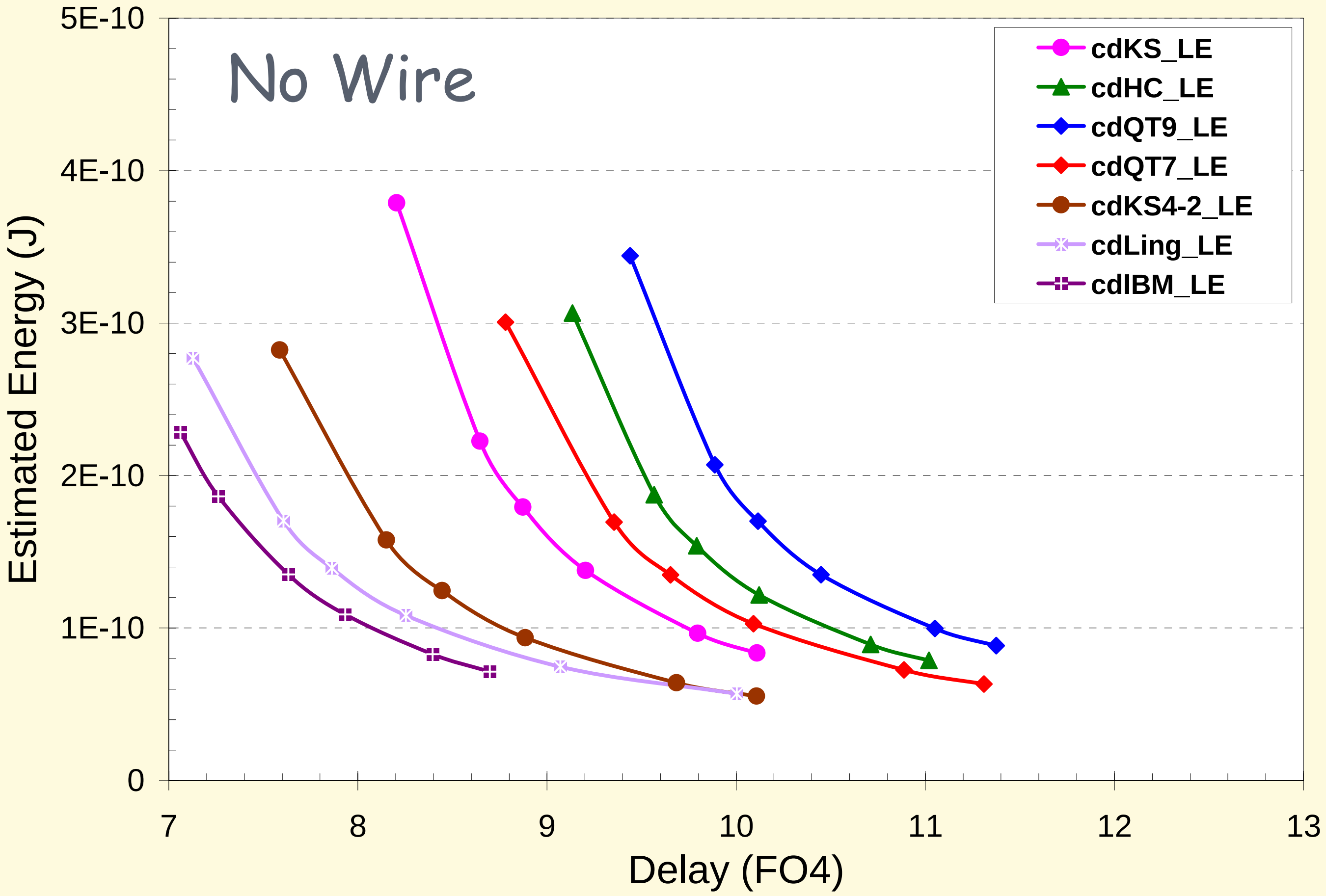
- Best High-Performance designs are clearly seen
- Different than what would be chosen from single point

Energy-Delay Space View



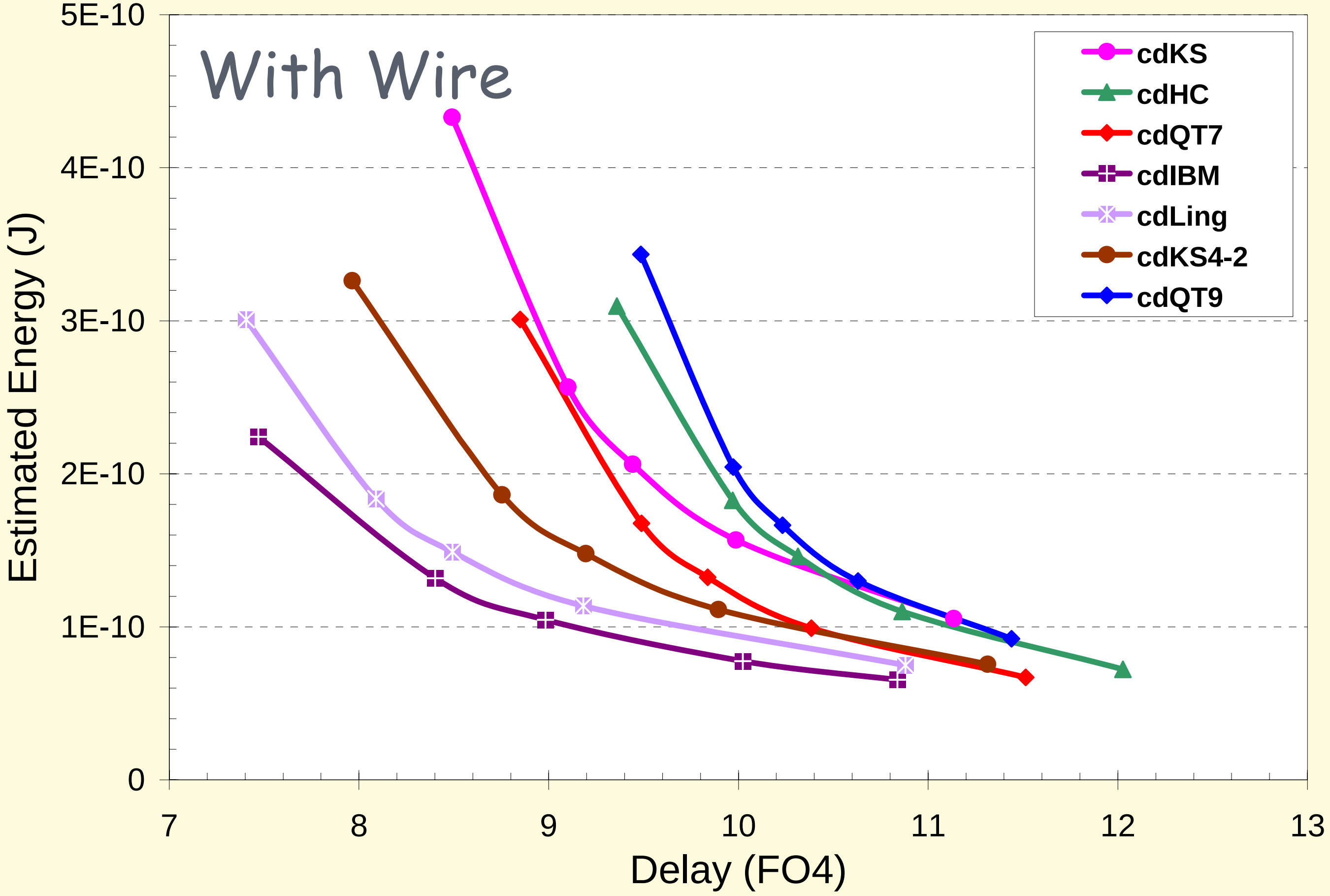
- Also determines best design for Low-Power Target

Contribution of Wire to Delay and Energy should be examined too



- Without wire, differences appear large

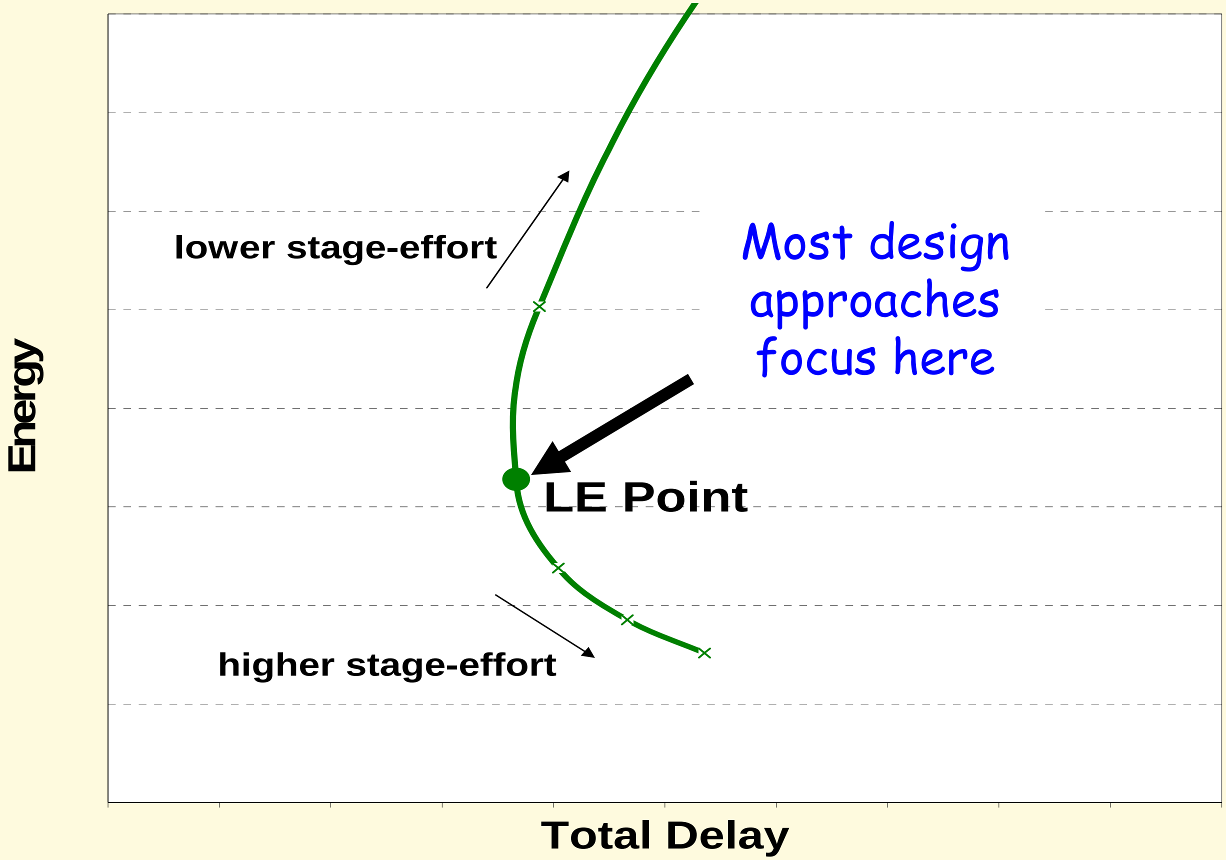
Contribution of Wire to Delay and Energy should be examined too



- Wire strongly impacts selection of "best adders"

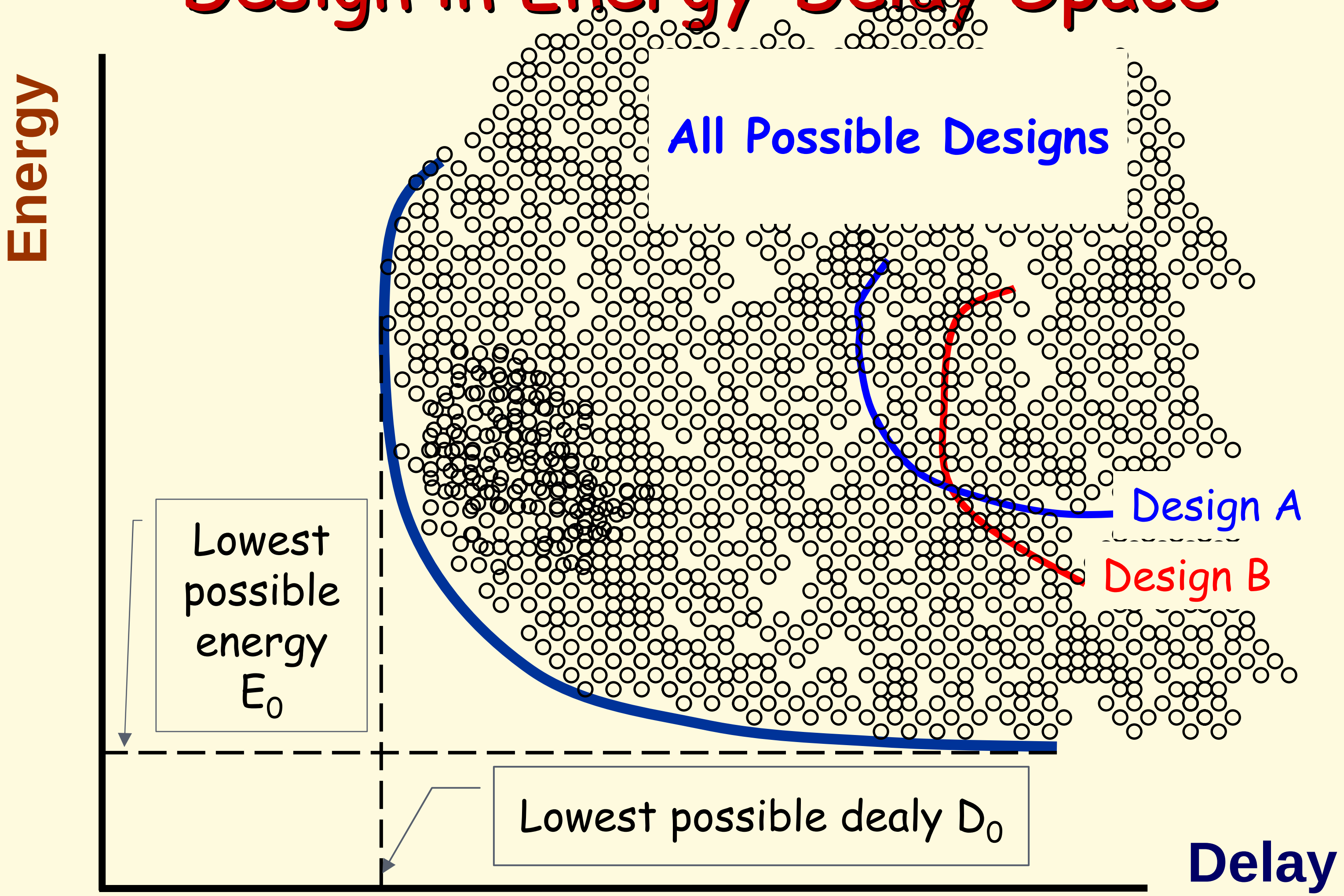
Energy

Where does Logical Effort lead us?



- It is possible to lower energy by trading delay? or …

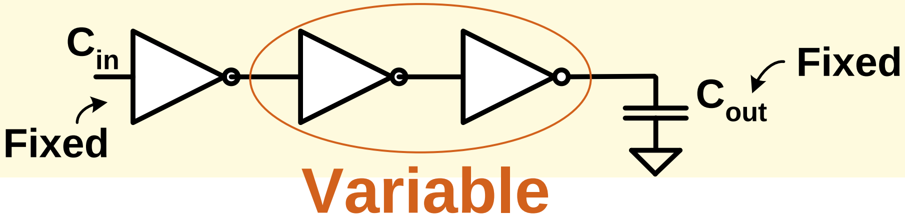
Design in Energy-Delay Space

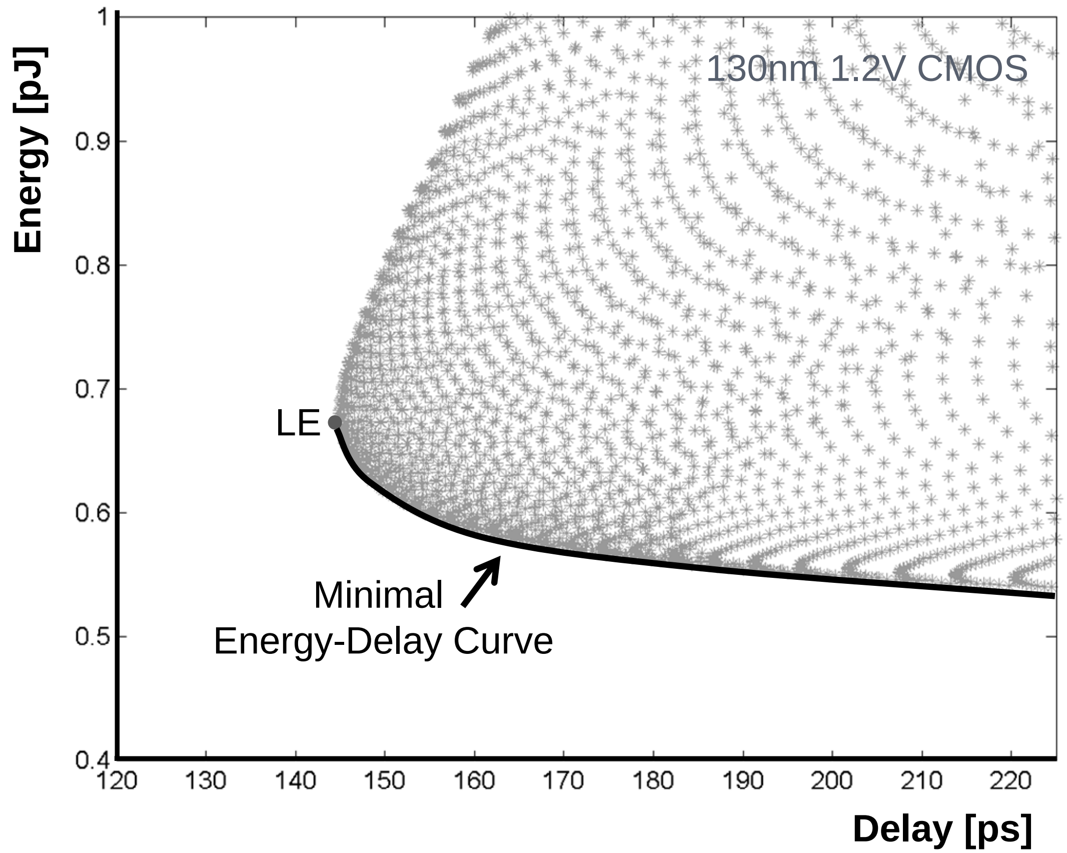


$$(E-E_0)(D-D_0)=0.2xE_0D_0$$

**P. Penzes, Caltech, PhD 2002, V. Zyuban, ISLPED 2002*

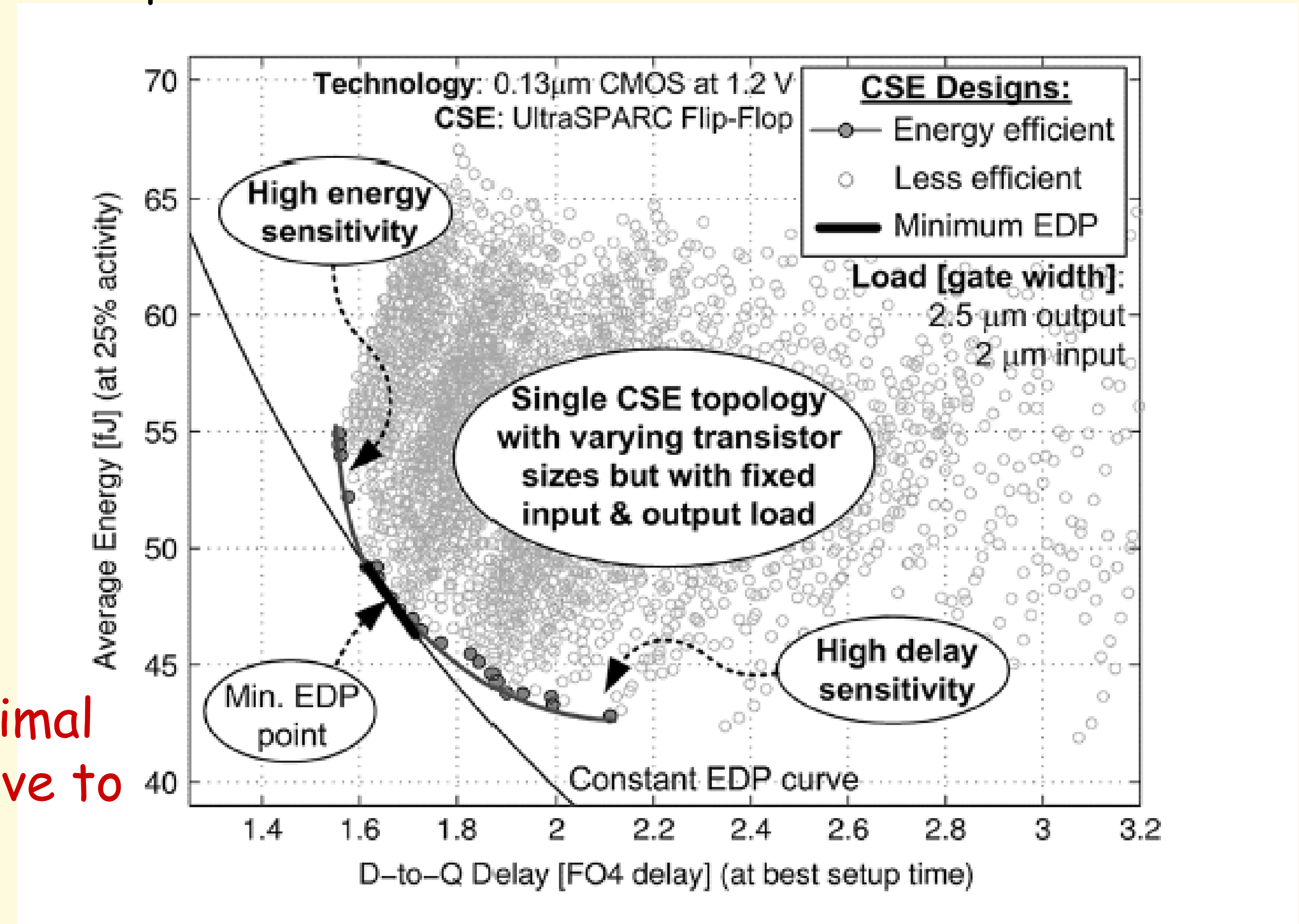
Energy-Delay Space of a Circuit
(Fixed Input Size and Output Load)





Exhaustive search

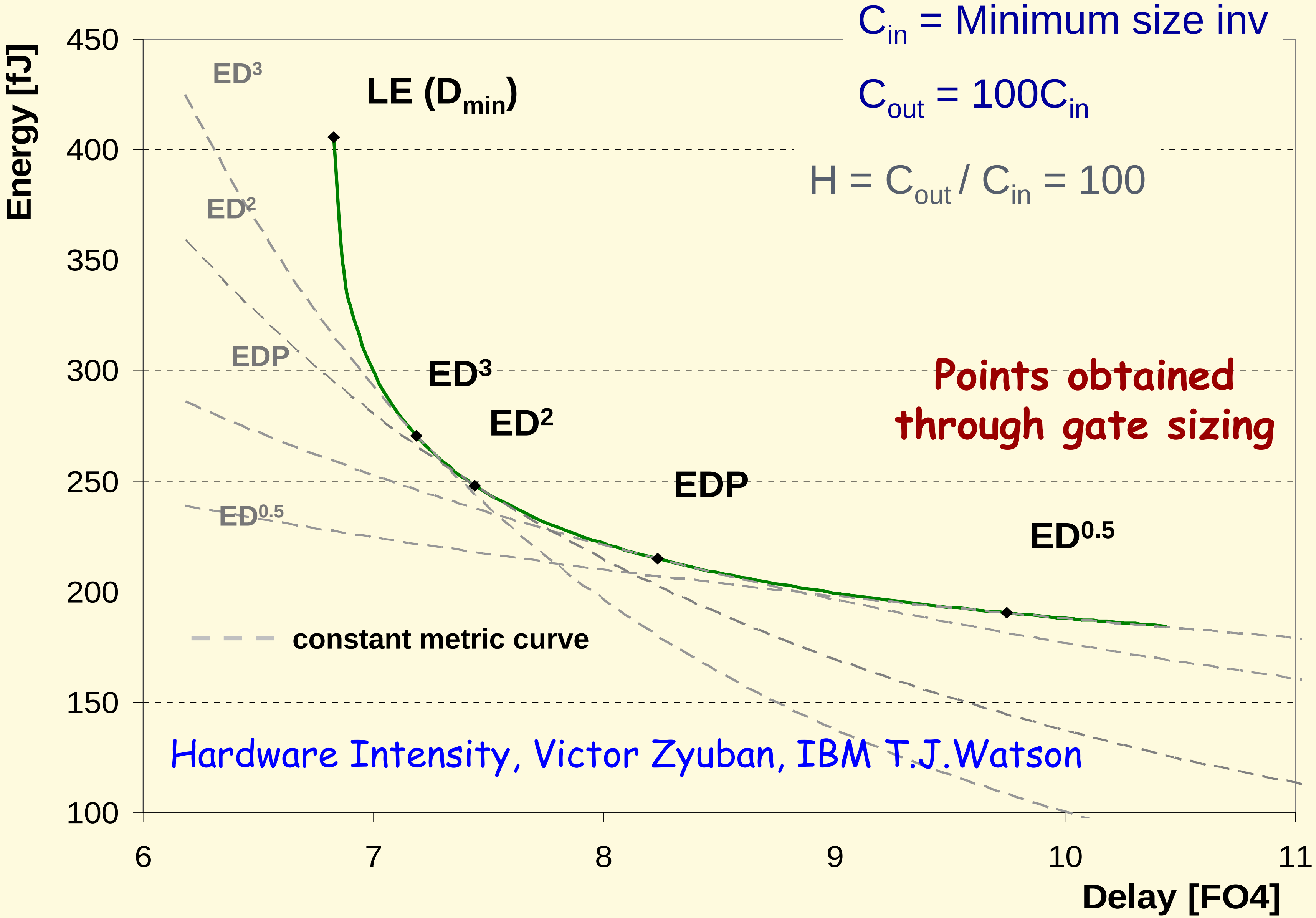
A circuit with **10** transistors and **10** possible size for each transistor requires to check **10^{10}** possible solutions!



To obtain the minimal E-D curve do I have to check all possible solutions?

C. Giacomotto, N. Nedovic, and V. G. Oklobdzija, "*The Effect of the System Specification on the Optimal Selection of Clocked Storage Elements*", IEEE JoSSC, vol. 42, no. 6, June 2007.

Hardware Intensity: V. Zyuban, IBM



C_{in} = Minimum size inv

$C_{out} = 100C_{in}$

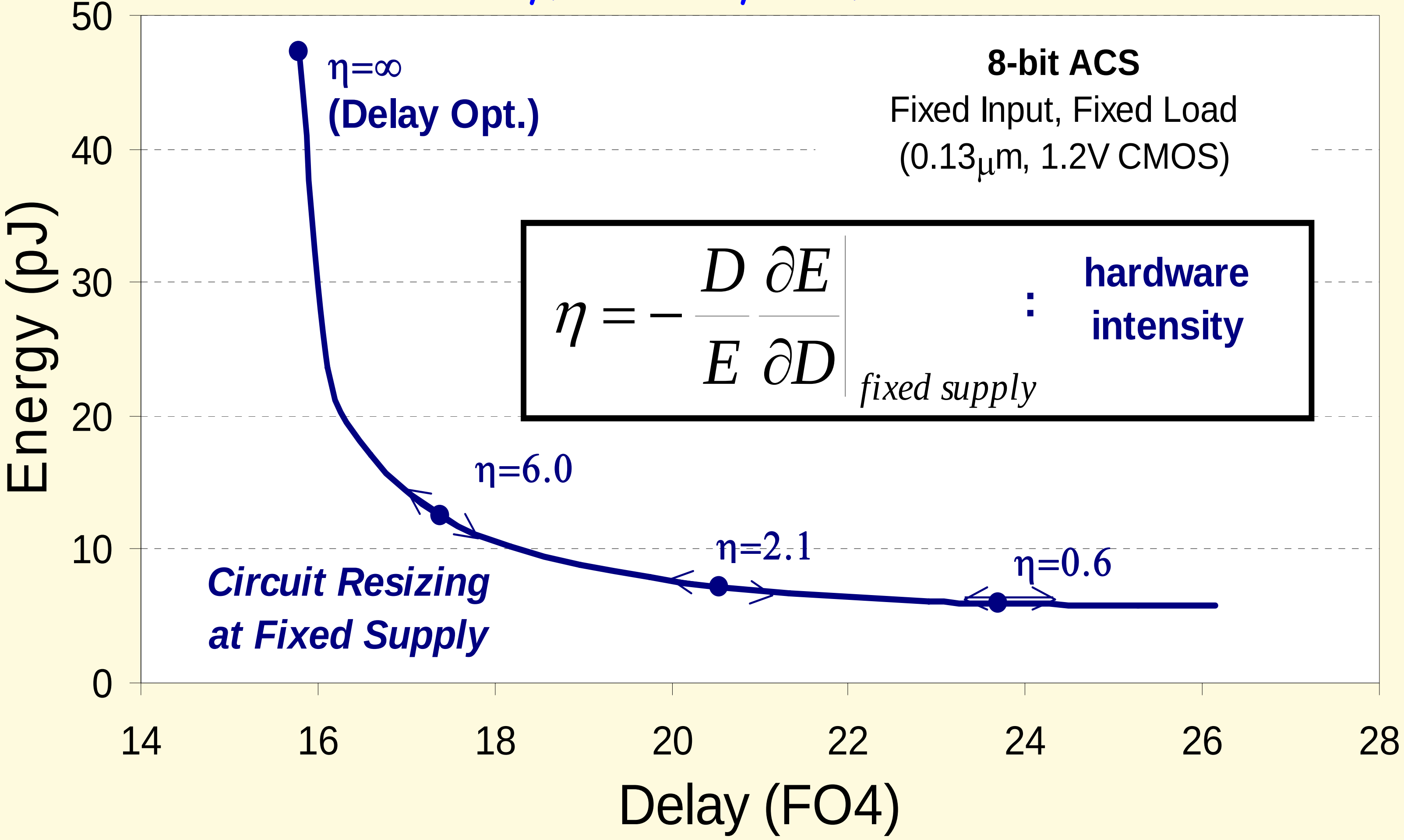
$H = C_{out} / C_{in} = 100$

Points obtained through gate sizing

Hardware Intensity, Victor Zyuban, IBM T.J.Watson

Design Objective at Nomial V_{DD}

Hardware Intensity, Victor Zyuban, IBM T.J.Watson



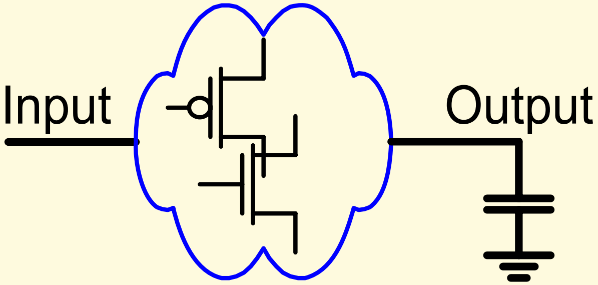
$$\eta = -\frac{D}{E}\frac{\partial E}{\partial D}\bigg|_{\text{fixed supply}}$$

: **hardware intensity**

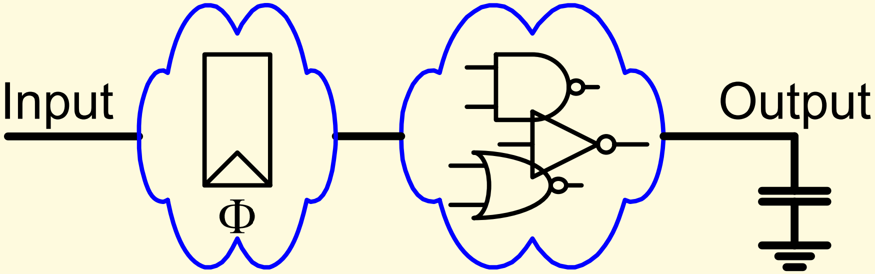
- Design choice depends on (E,D) requirements

Prior Work on Design Optimization

- **Transistor-based** [TILOS]
  - Sizing individual transistors
  - Growing complexity
  - Applicable to small blocks only



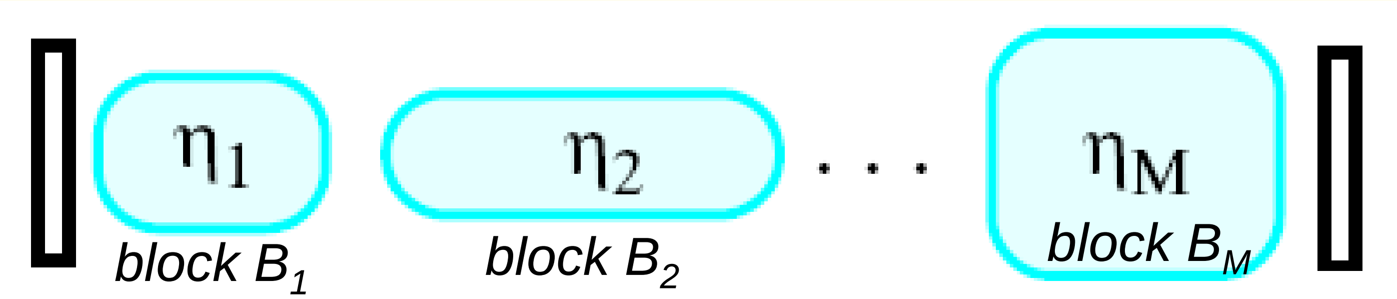
- **Block-based** [Zuyban & Strenski]
  - Blocks: latch & logic
  - Trading {energy,delay} of blocks
  - CAD tools
  - Fixed interface



Transistor-Based Approach

- Optimization problem: (i=1..M)
  - Minimize: $\text{Area}(W_1,\ldots,W_M) \approx \Sigma W_i$
  - Constraint: $D_{\text{worst}}(W_1,\ldots,W_M) = T$
- Delay modeling
  - Linear (RC-like): TILOS
  - Look-up table: AMPS (Synopsys)
- A convex problem $\Rightarrow$ minimal solution exists
  - Different polynomial algorithms developed
  - May have issues with convergence
  - Long run time with increasing design complexity

Block-Based: Zyuban (IBM)

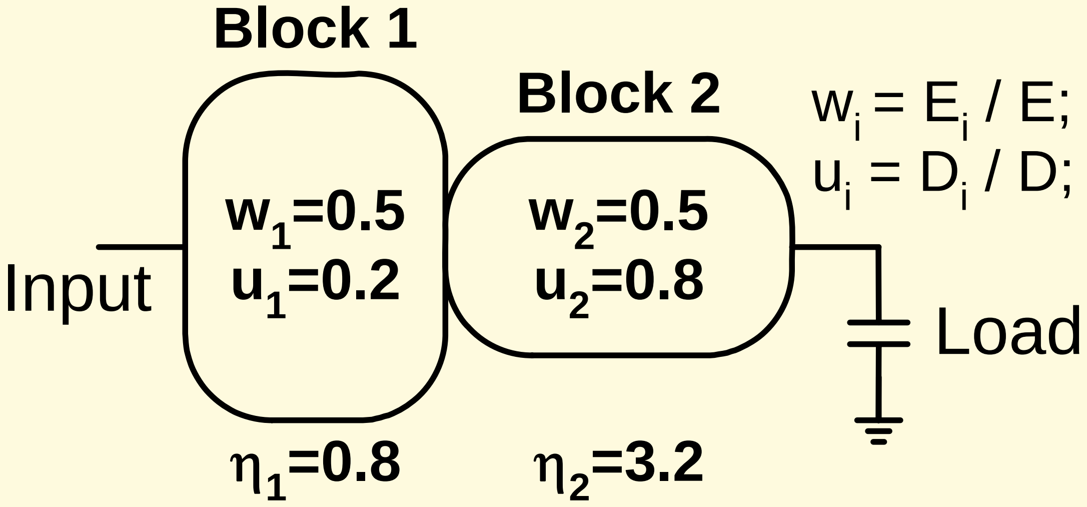


[Zyuban, IBM T.J. Watson Research]

- Optimization problem for a pipelined stage:
  - Minimize energy: $E(B_1,\ldots,B_M) = \Sigma E_{Bi}$
  - Delay constraint: $D(B_1,\ldots,B_M) = \Sigma D_{Bi} = T$
- Optimal criteria:
  - $\boxed{(w_i / u_i) \cdot \eta_i = (w_k / u_k) \cdot \eta_k}$ for any (i,k)

  with $w_x = E_{Bx}/E$, $u_x = D_{Bx}/T$, $\eta_x = (\partial E_{Bx}/E_{Bx})/(\partial D_{Bx}/D_{Bx})$
- Similar criteria for a simple pipelined system

Application: Solution Verification



Block 1

$w_1=0.5$
$u_1=0.2$

$\eta_1=0.8$

Block 2

$w_2=0.5$
$u_2=0.8$

$\eta_2=3.2$

Input

Load

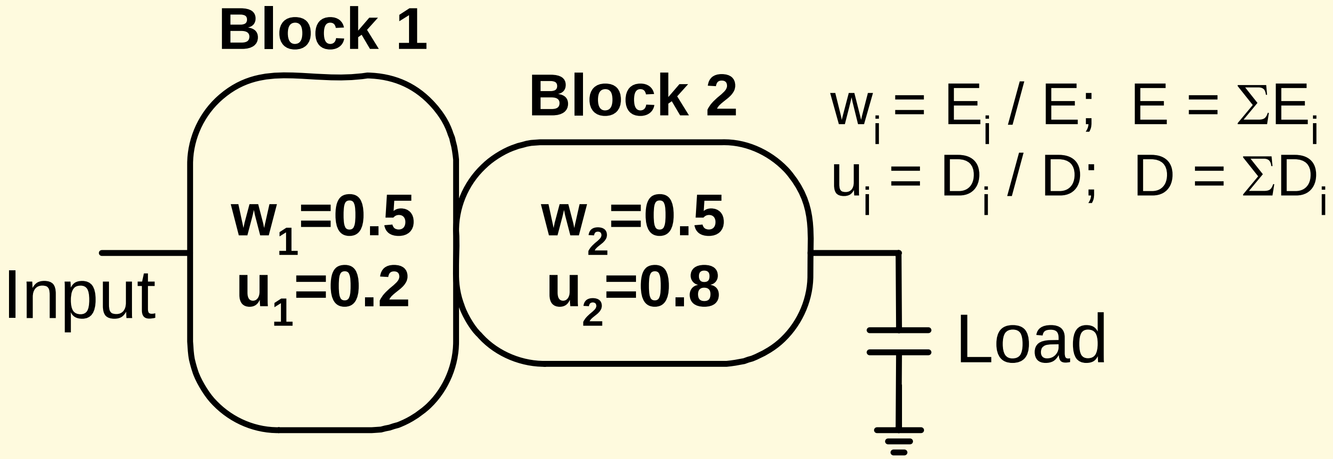
$w_i = E_i / E; \;\; E = \Sigma E_i$
$u_i = D_i / D; \;\; D = \Sigma D_i$

[Zyuban, IBM T.J. Watson Research]

- Verify optimality of solution:
  - Block 1: $(w_1/u_1)\cdot\eta_1 = 2.0$
  - Block 2: $(w_2/u_2)\cdot\eta_2 = 2.0$

$\Big\}$ *Equal ⇒ optimal!*

Application: Solution Verification



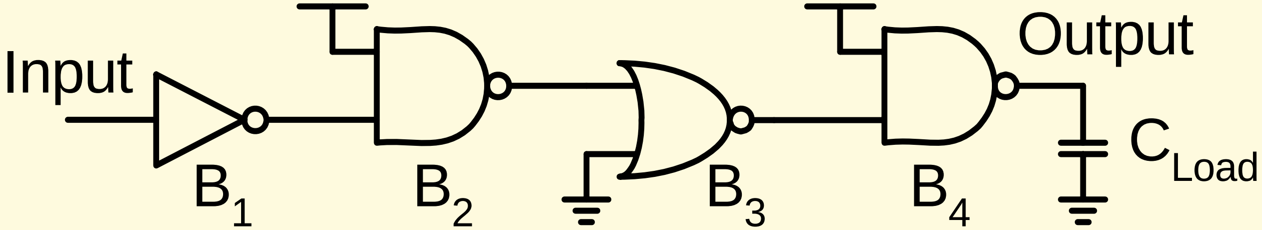
$w_i = E_i / E$; $E = \Sigma E_i$

$u_i = D_i / D$; $D = \Sigma D_i$

- If $\eta_1 = 3.2$ and $\eta_2 = 0.8$
  - Block 1: $(w_1/u_1)\cdot\eta_1 = 8.0$
  - Block 2: $(w_2/u_2)\cdot\eta_2 = 0.5$

  } *Unequal ⇒ not optimal*
  - Better solution? Relax η_1 and increase η_2

Major Limitation



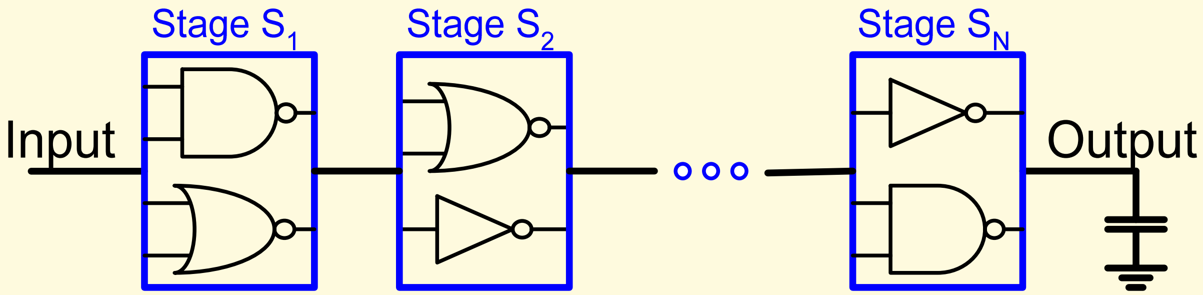
- Zyuban's assumption:
  - Delay & energy independence of each block B_i
- Single path: block ≡ gate

$$\begin{cases} Delay\ T_d \propto \{ C_{out}, C_{in} \} \\ Energy\ E \propto \{ C_{out}, C_{in} \} \\ C_{in}\ :\ current\ gate\ cap \\ C_{out}\ :\ next\ gate\ cap \end{cases}$$

: energy, delay dependency of adjacent gates

- Similar dependency between blocks and pipelines
- No analytical solution if accounting dependency

Proposed Stage-Based Approach



- Stage ≈ logic depth
- Gates → stage
  - Based on maximal distances to input and output
  - Stage delay: $d_{stage} = max\{d_{gate}\}$
  - Stage energy: $E_{stage} = \Sigma E_{gate}$
  - Estimated from gate energy & delay models

Delay and Energy Modeling of Gates

- Logical Effort delay model:

reference delay τ

(technology dependent)

$$T_{d,gate} = \left[\frac{\kappa R_{gate} C_{gate}}{\kappa R_{inv} C_{inv}} \circ \frac{C_{out}}{C_{gate}} + \frac{\kappa R_{gate} C_{par}}{\kappa R_{inv} C_{inv}} \right] \left(\kappa R_{inv} C_{inv} \right) = \left(gh + p \right) \tau$$

logical effort ***g***

(gate dependent)

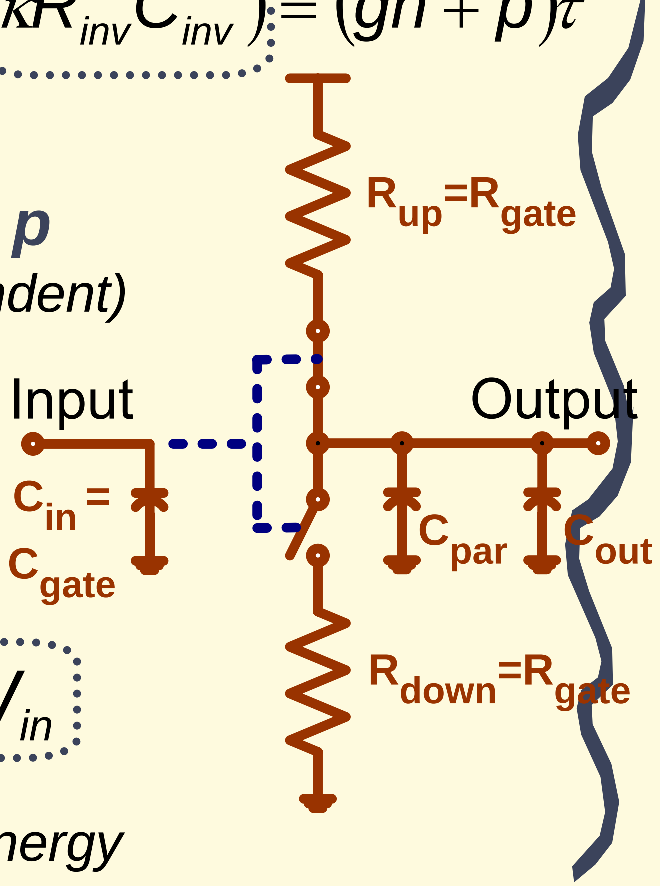
electrical effort ***h***

(load dependent)

parasitic ***p***

(gate dependent)

stage effort ***f*** = *g•h*



- Energy model:

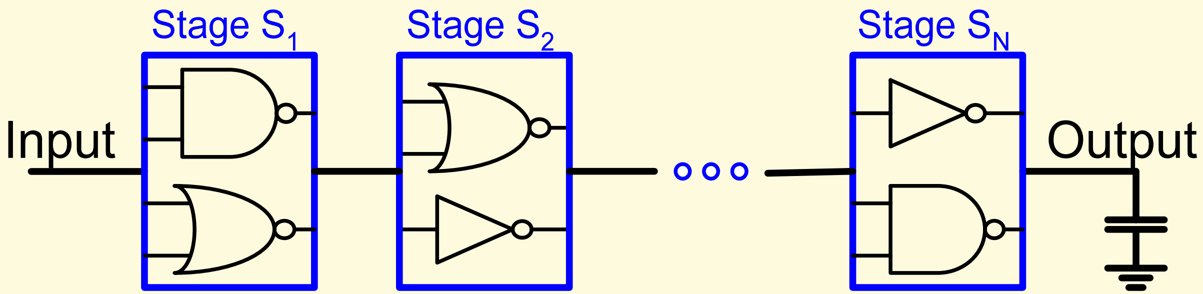
$$E_{gate}(W) = E_g W_{out} + E_p W_{in} + P_l T_{CK} W_{in}$$

Active Energy

Leakage Energy

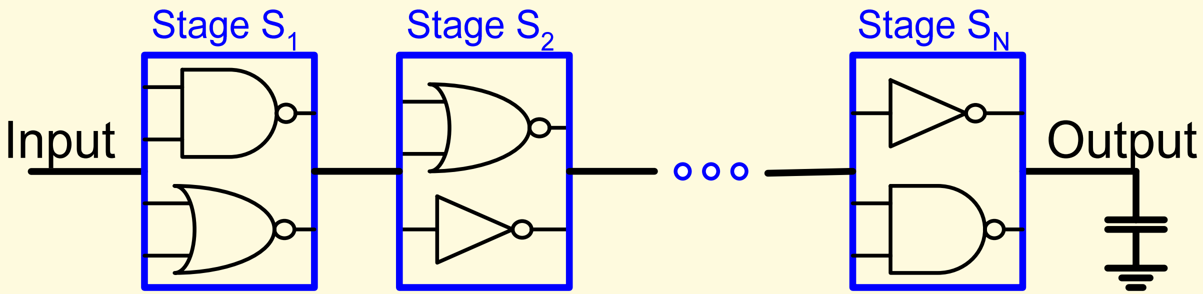
Pipelined Stage Optimization

Stage-Based Optimization



- Optimization functions
  - Delay: $D = \Sigma D_{Stage(i)}$
  - Energy: $E = \Sigma E_{Stage(i)}$
- Possible design constraints
  - Delay target, D
  - Input size, W_{input}
  - Output load, C_{load}
- Posynomial Problems
  - Solvable with polynomial algorithms

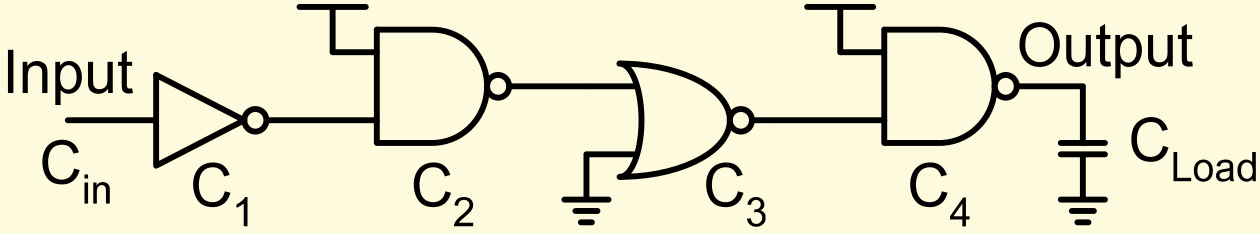
Problem A: Delay Optimization



- Optimization problem
  - Minimize: $D = \Sigma D_{Si}$
  - Constraint: {Input, Load} = const.

- Objectives
  - Obtain minimally achievable delay, D_{min}
  - Wanted in performance-critical designs
  - Disregard energy consumption (*actually*, $\partial E_i / \partial D_i = \infty$)

Single Path: Logical Effort



$$D = \sum_{i=1}^{N} \left(g_i \frac{C_{i+1}}{C_i} + p_i \right)$$

C_i = input cap of gate i
C_{in} = C_1 : fixed
C_{N+1} = C_{Load} : fixed

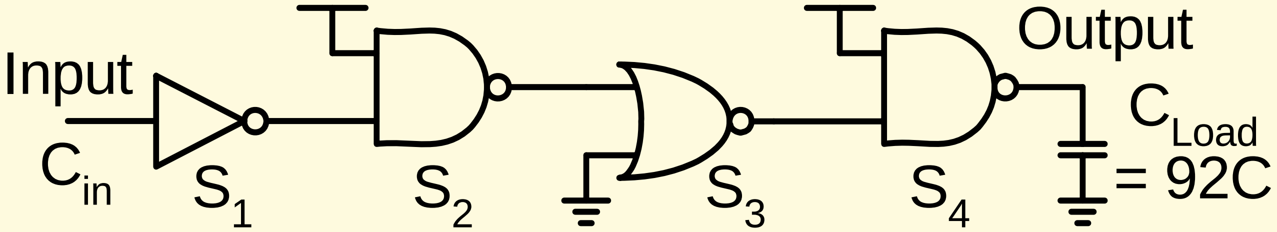
$dD/dC_i = 0\ (\forall i = 1..N)$: $$f_i = f_{opt} = \left[\left(\prod_{i=1}^{N} g_i \right) \left(\frac{C_{Load}}{C_{in}} \right) \right]^{1/N}$$

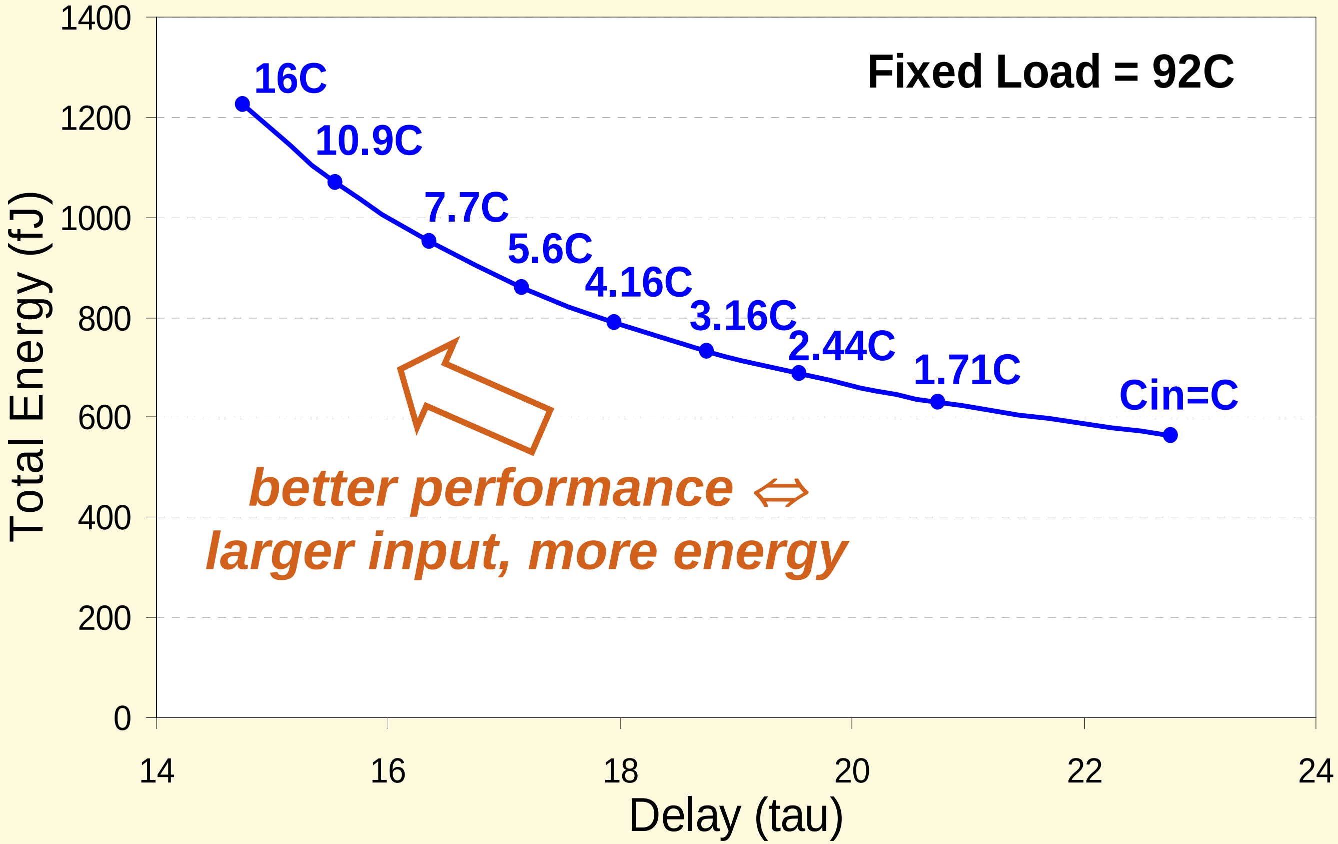
$$\boxed{D_{min} = N\ f_{opt} + \sum_{i=1}^{N} p_i}$$

⇧ *Path Gain, H*

- Solution = equal stage effort f (i.e. fan-out)

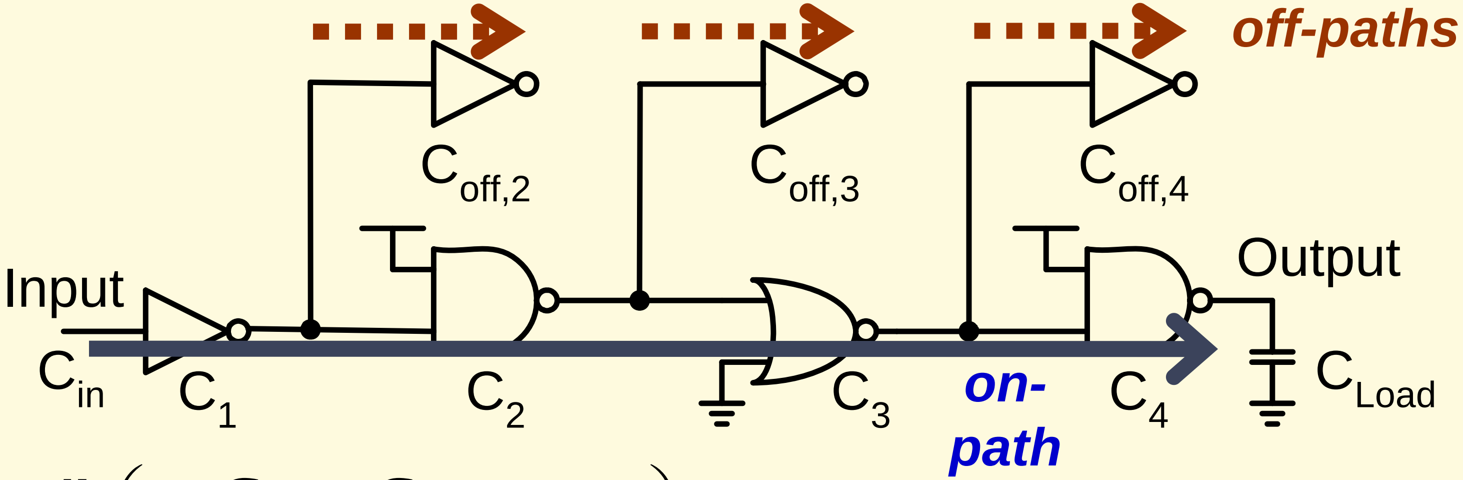
Energy Cost vs. Total Delay





better performance ⇔ larger input, more energy

Multi-Path Circuits



$$D = \sum_{i=1}^{N} \left(g_i \frac{C_{i+1} + C_{off\,,i+1}}{C_i} + p_i \right)$$

$$= \sum_{i=1}^{N} \left(g_i \underbrace{\frac{C_{i+1} + C_{off\,,i+1}}{C_{i+1}}}_{b_{i+1}} \frac{C_{i+1}}{C_i} + p_i \right)$$

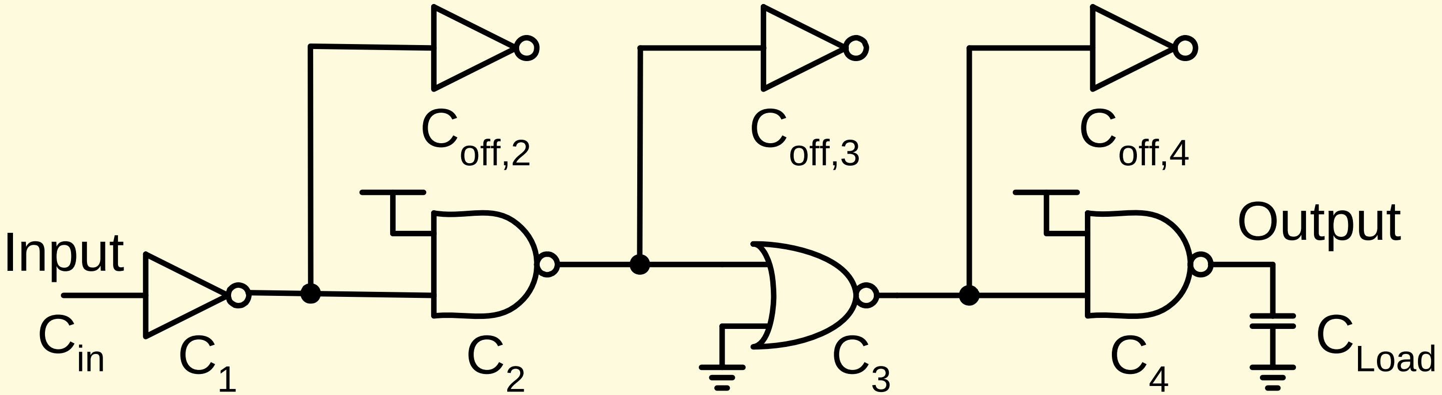
C_i = input cap of gate i

$C_{off,i}$ = input cap of i th off-path gate

b_{i+1} = branching factor at (i+1)th-gate input

- Optimal delay depends on off-path load

Linear Branching



- Linear branching: $\boldsymbol{C_{off,i} / C_i = const.}$

$$dD/dC_i = 0\ (\forall i = 1..N):\quad f_i = f_{opt} = \left[\left(\prod_{i=1}^{N} g_i\right)\left(\prod_{i=1}^{N} b_i\right)\left(\frac{C_{Load}}{C_{in}}\right)\right]^{1/N}$$

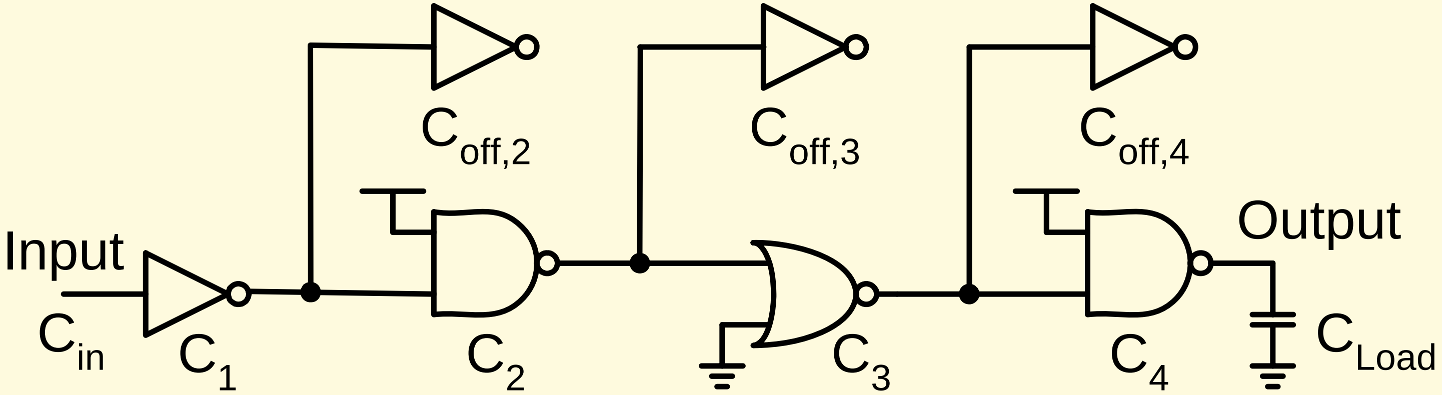
$$\boxed{D_{min} = N\ f_{opt} + \sum_{i=1}^{N} p_i}$$

⇧

Branching Factor, B

- Similar analytical form for solution

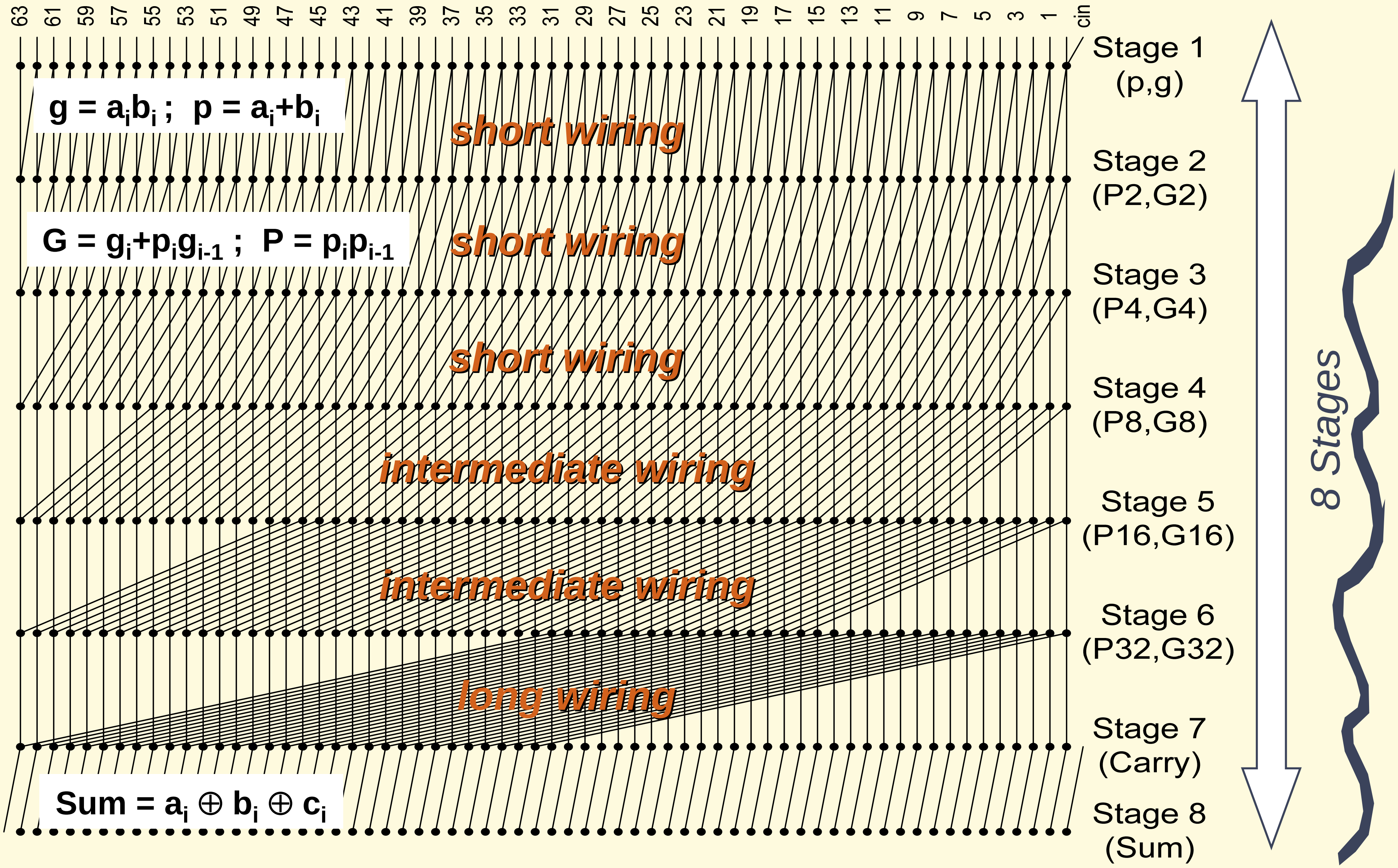
Non-Linear Branching



- Nonlinearity due to:
  - Constant off-path load (wire cap, min-size gates)
  - Unequal path lengths
  - Parasitic delay difference of gates

- ***No analytical form***
  - Recursive solving
  - Solution: unequal stage efforts

64-bit Static Kogge-Stone Adder

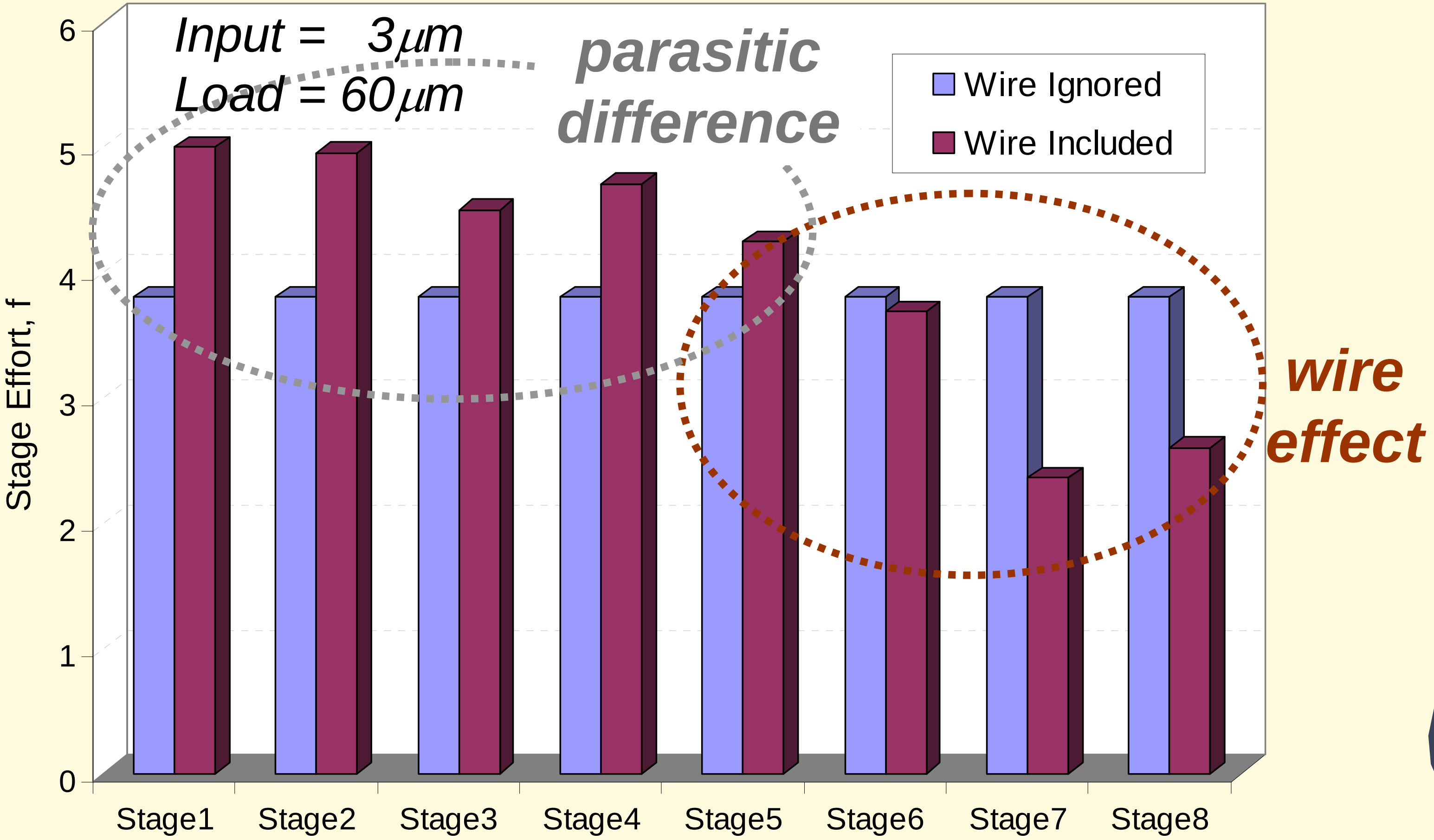


$g = a_i b_i$; $p = a_i + b_i$

$G = g_i + p_i g_{i-1}$; $P = p_i p_{i-1}$

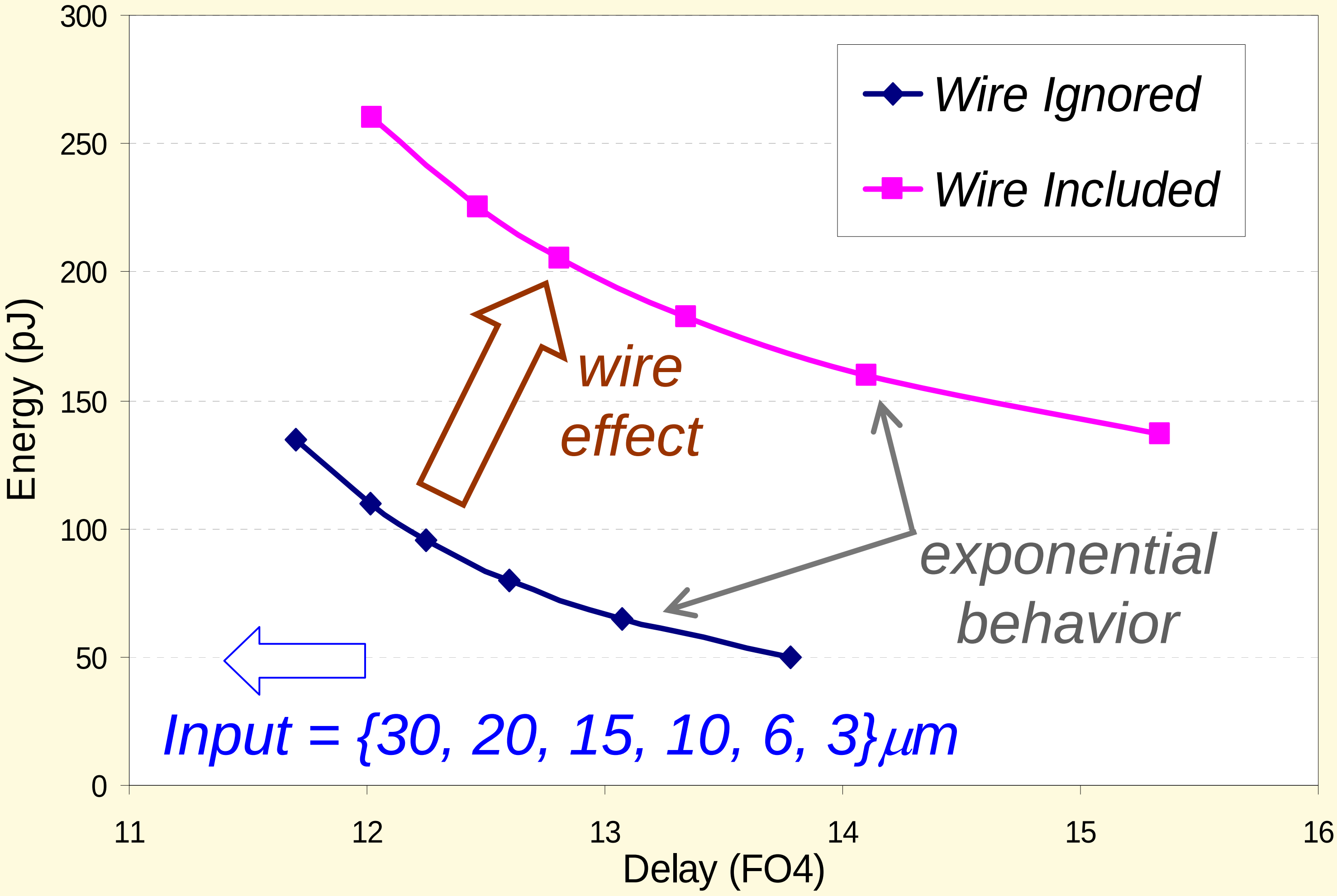
$Sum = a_i \oplus b_i \oplus c_i$

64-b KS: Stage Effort Distribution



- Nonlinearity causes unequal stage efforts
  - Nonlinear factors: wire load, parasitic delay diff.

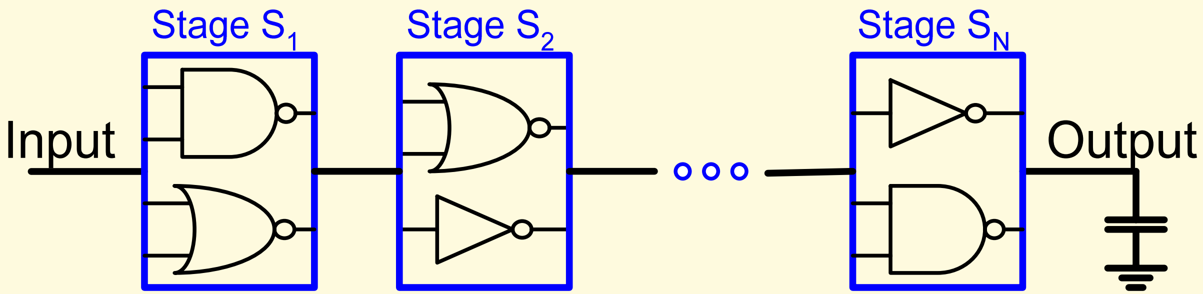
64-b KS: Energy versus Delay



Input = {30, 20, 15, 10, 6, 3}µm

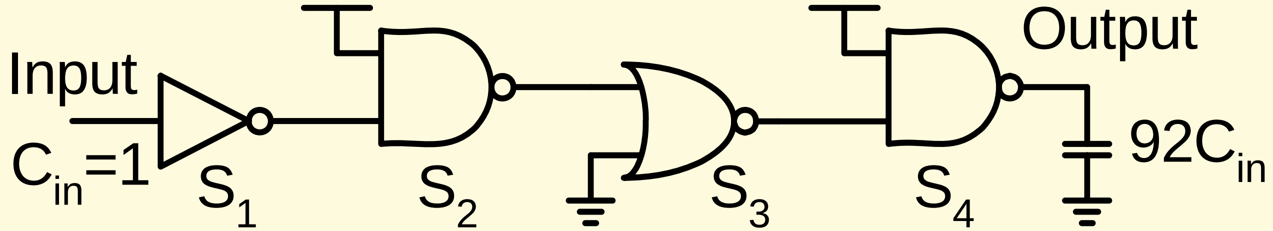
- Significant wire effect on delay & energy

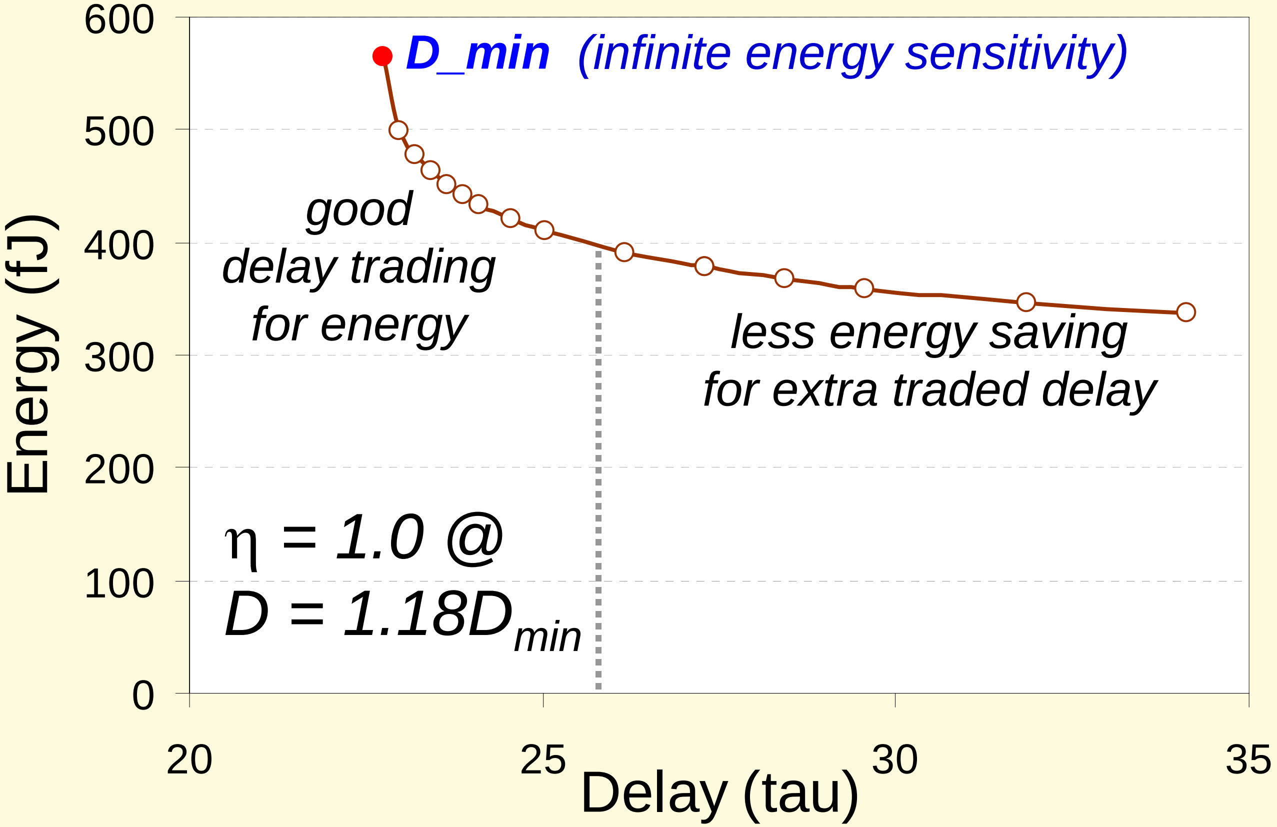
Problem B: Energy-Delay Tradeoff



- Optimization Problem
  - Minimize: $E = \Sigma E_{Stage(i)}$
  - *Constraint:* *{Input, Load} = const.*
    $\Sigma D_{Stage(i)} = D_{min} + \Delta D$
- Objectives
  - Avoid infinite energy sensitivity at D_{min}
  - Equalize energy-delay sens.: $(\partial E/\partial D)_{Si} = (\partial E/\partial D)_{Sk}$
  - Trade delay for energy (*traditional approach*)

E-D Trade-off: Single Path





D_min *(infinite energy sensitivity)*

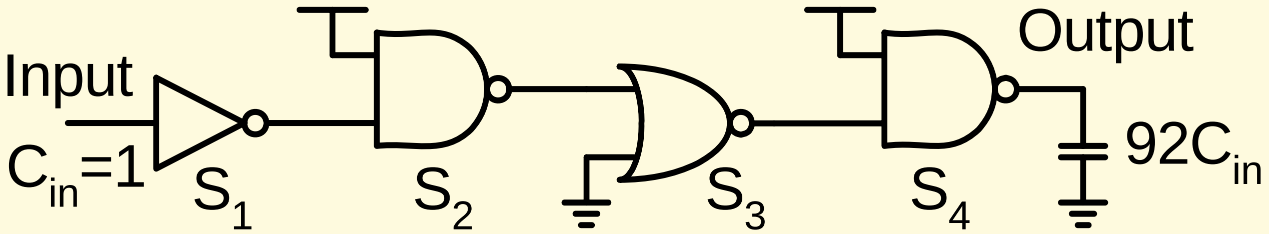
good delay trading for energy

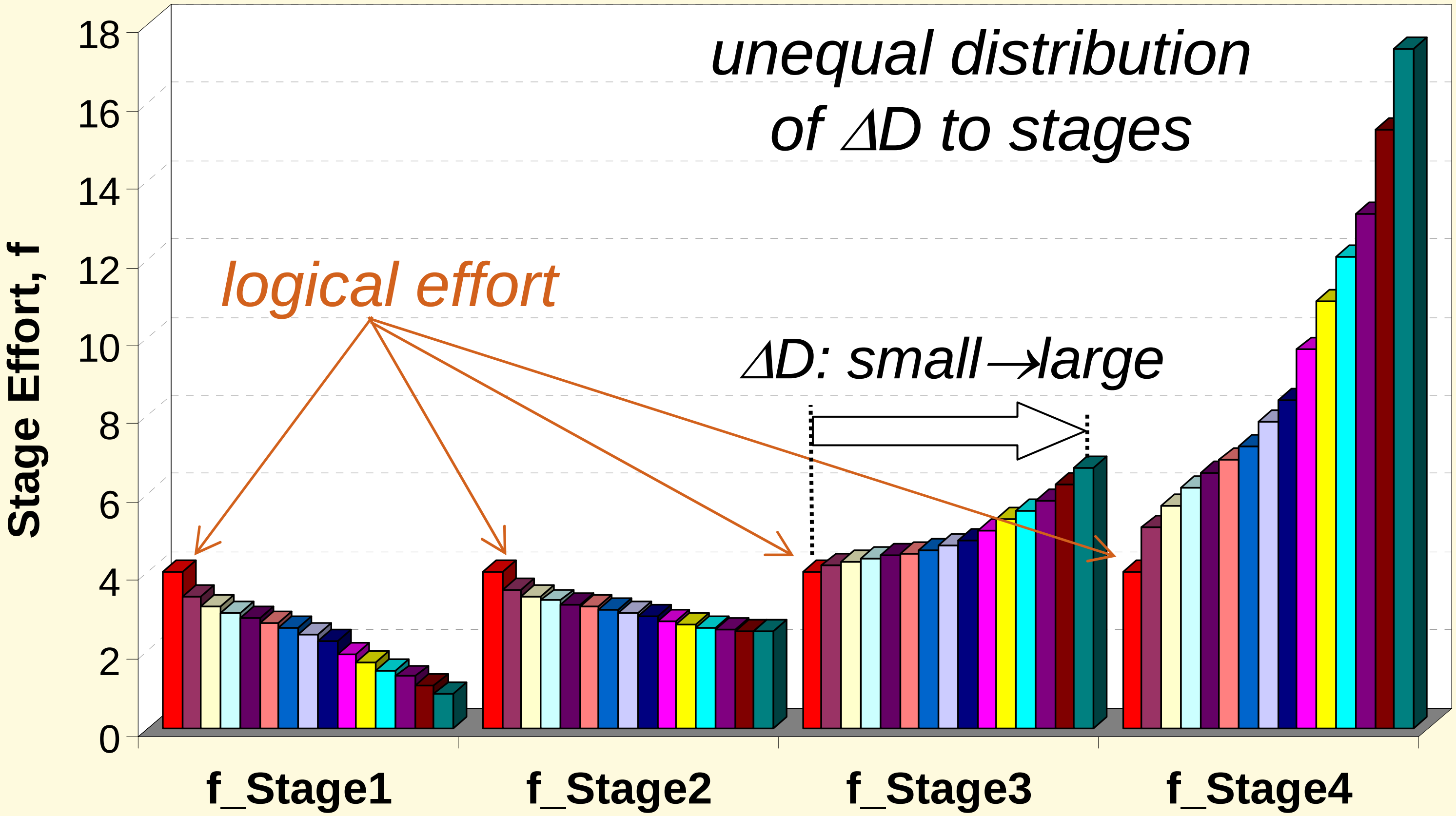
less energy saving for extra traded delay

η = *1.0 @*

$D = 1.18D_{min}$

E-D Trade-off: Stage Effort Distrib.

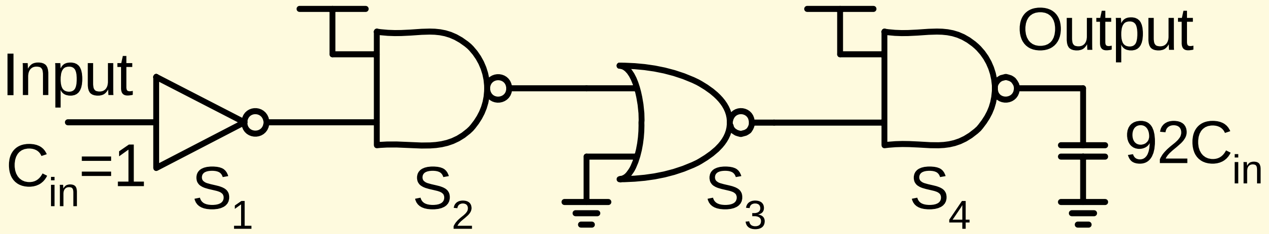


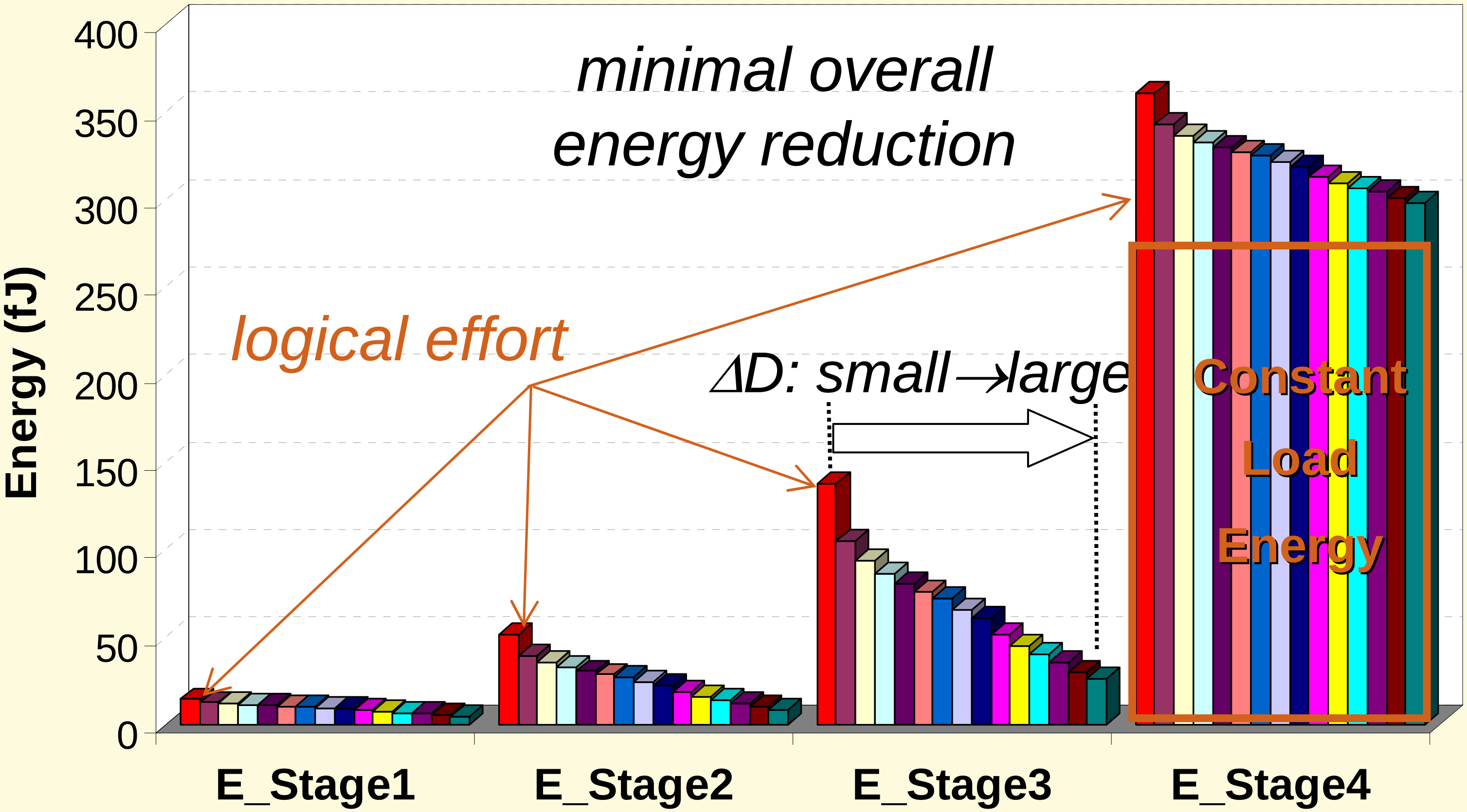

unequal distribution of ΔD to stages

logical effort

ΔD: small→large

E-D Trade-off: Energy Distrib.





minimal overall energy reduction

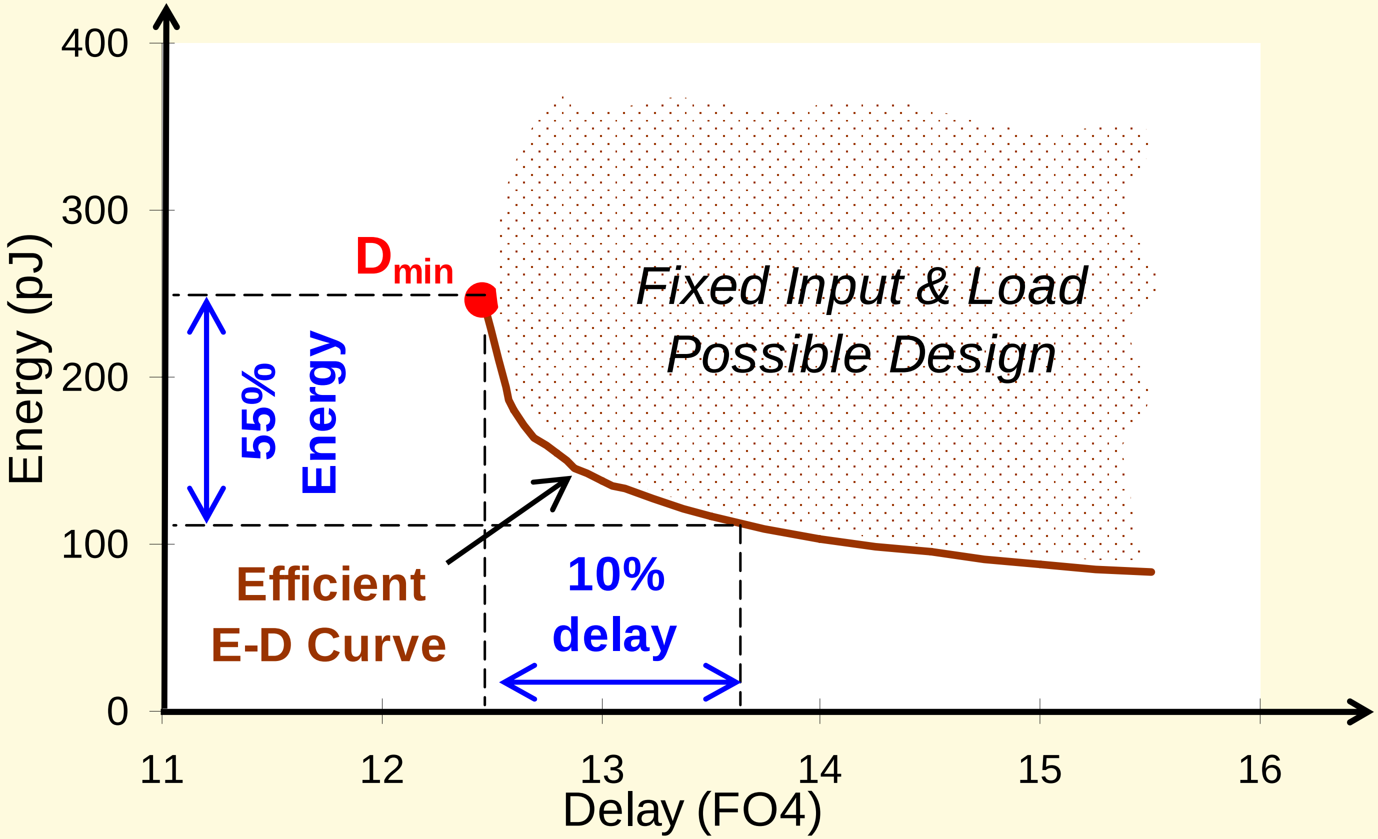
logical effort

ΔD: small→large

Constant Load Energy

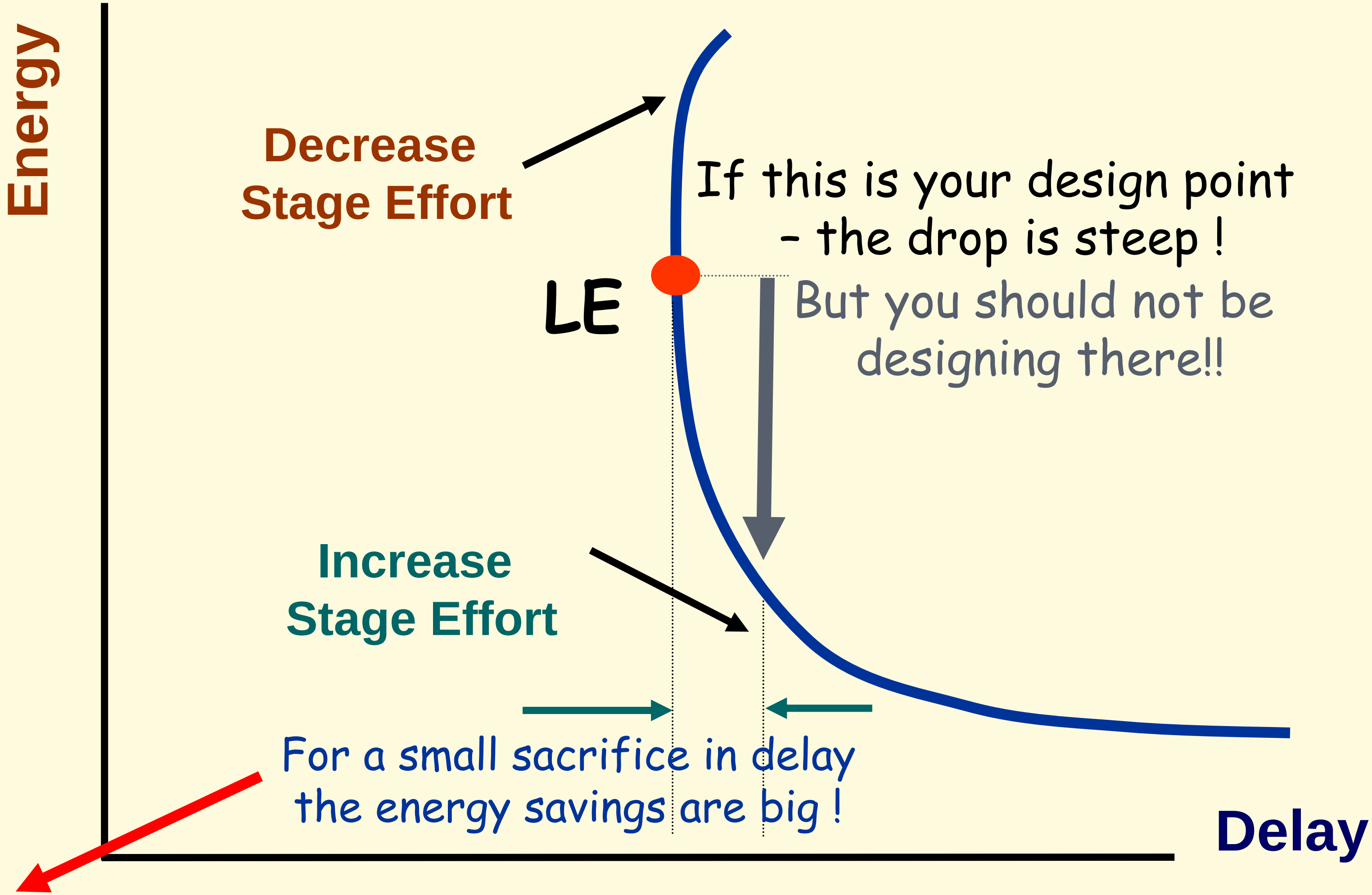
(*) Including constant output load

64-b KS: Energy Delay Tradeoff



- D_{min} solution is very inefficient in energy
- 55% energy saving with 10% delay traded
- Solution = equal stage energy-delay sensitivity

Design in Energy-Delay Space



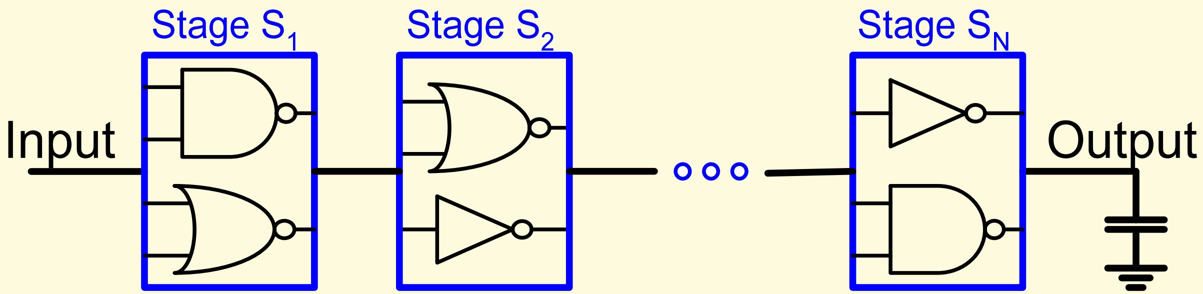
If this is your design point – the drop is steep !

But you should not be designing there!!

For a small sacrifice in delay the energy savings are big !

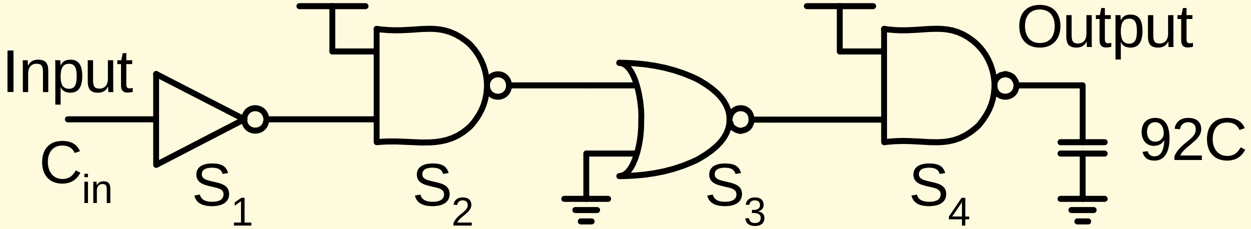
From:
R.W. Brodersen, M.A. Horowitz, D. Markovic, B. Nikolic, V. Stojanovic, "Methods for True Power Minimization," International Conference on Computer-Aided Design, ICCAD-2002, Digest of Technical Papers, San Jose, CA, November 10-14, 2002, pp. 35-42.

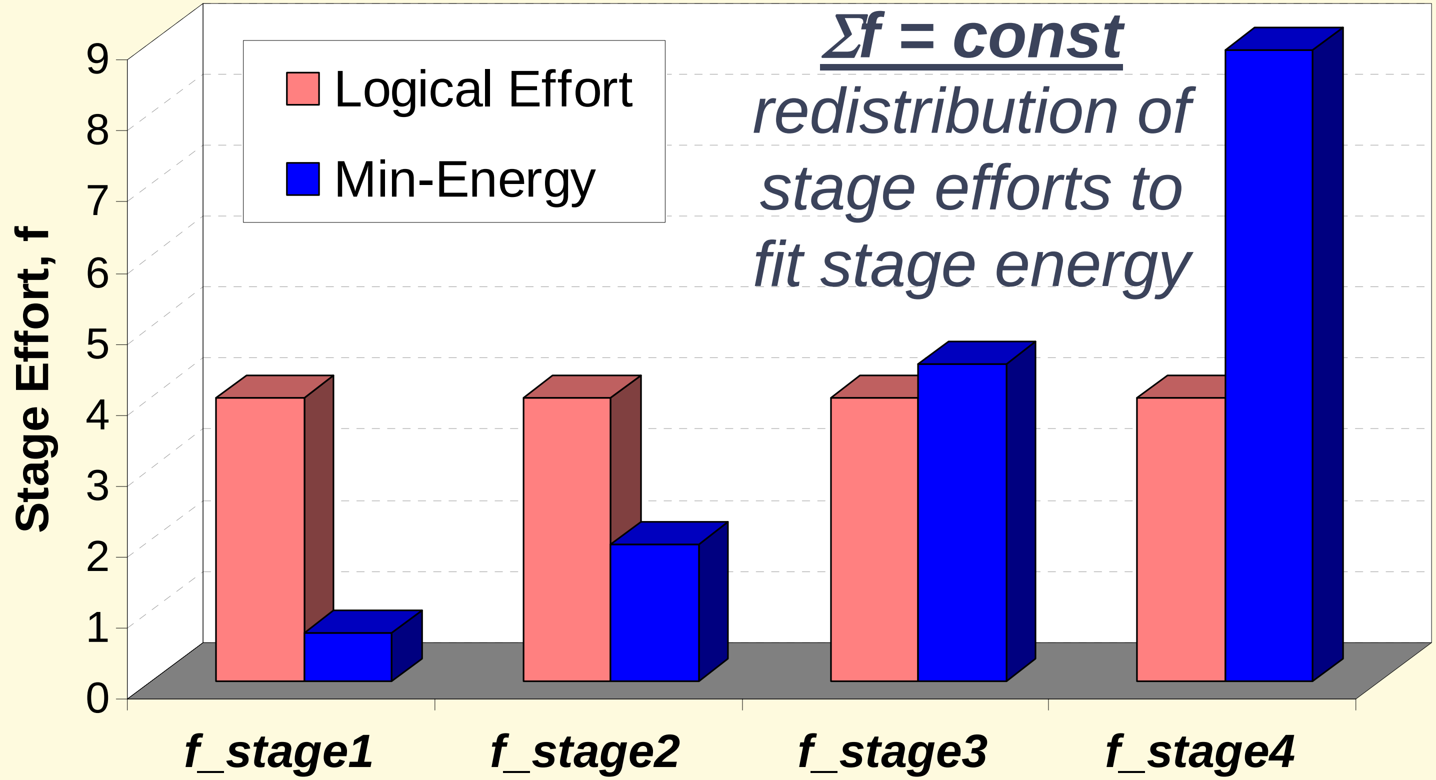
Problem C: Energy Minimization



- Problem:
  - Minimize: $E = \Sigma E_{Si}$
  - *Constraint:* $D = \Sigma D_{Si} = const.$
    Load = const.
- Objective:
  - Obtain absolute minimal energy @ given delay
  - Equalize energy-delay sens.: $(\partial E/\partial D)_{Si} = (\partial E/\partial D)_{Sk}$
  - Trade input size such that $(\partial E / \partial Input)_D = 0$

Single Path: Stage Effort Redistrib.

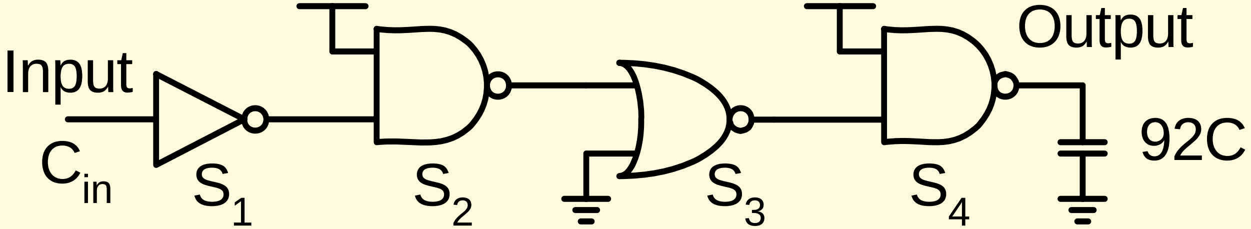


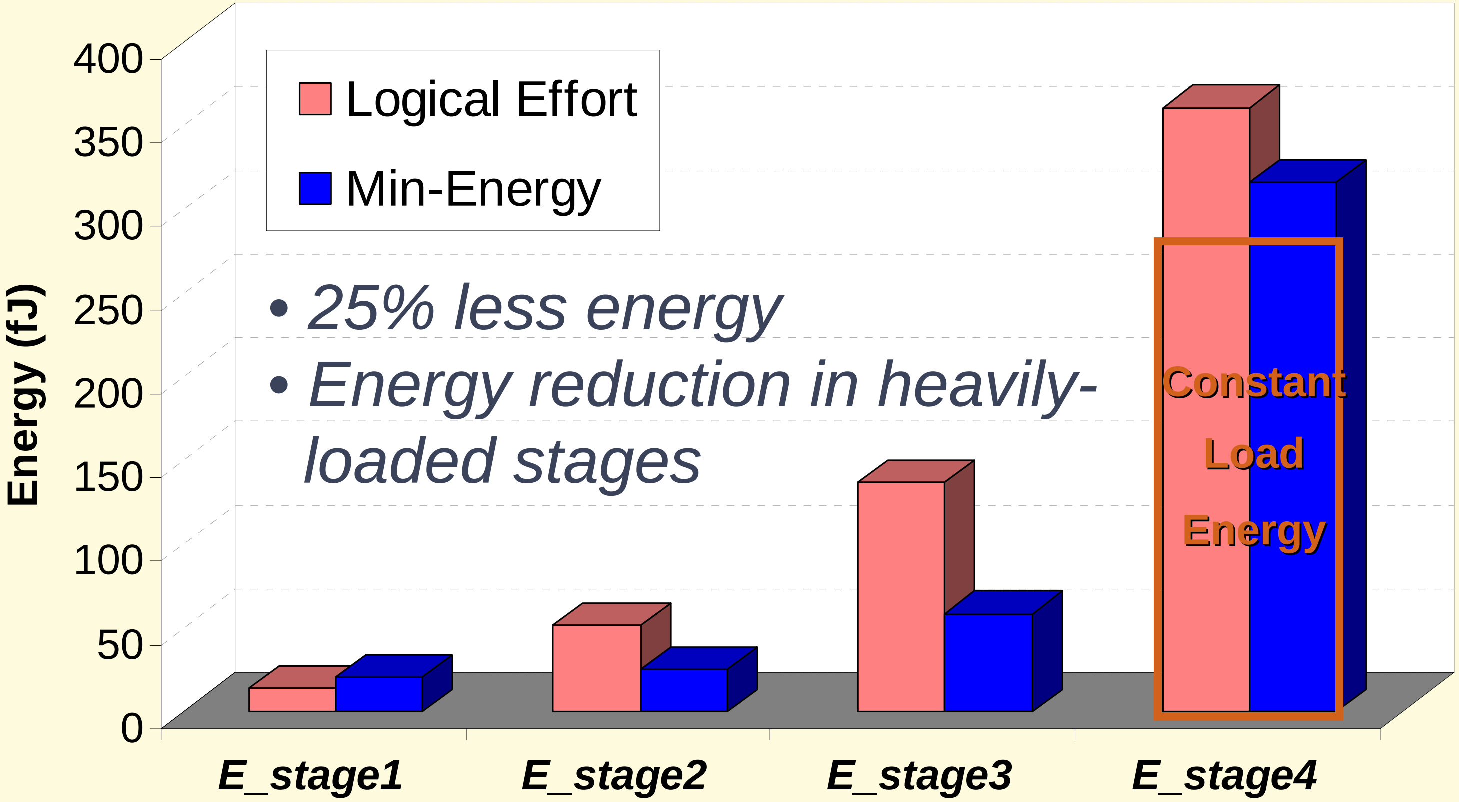


Σf = const

redistribution of stage efforts to fit stage energy

Single Path: Energy Distribution





- *25% less energy*
- *Energy reduction in heavily-loaded stages*

$^{(*)}$ *Including energy consumed on output load*

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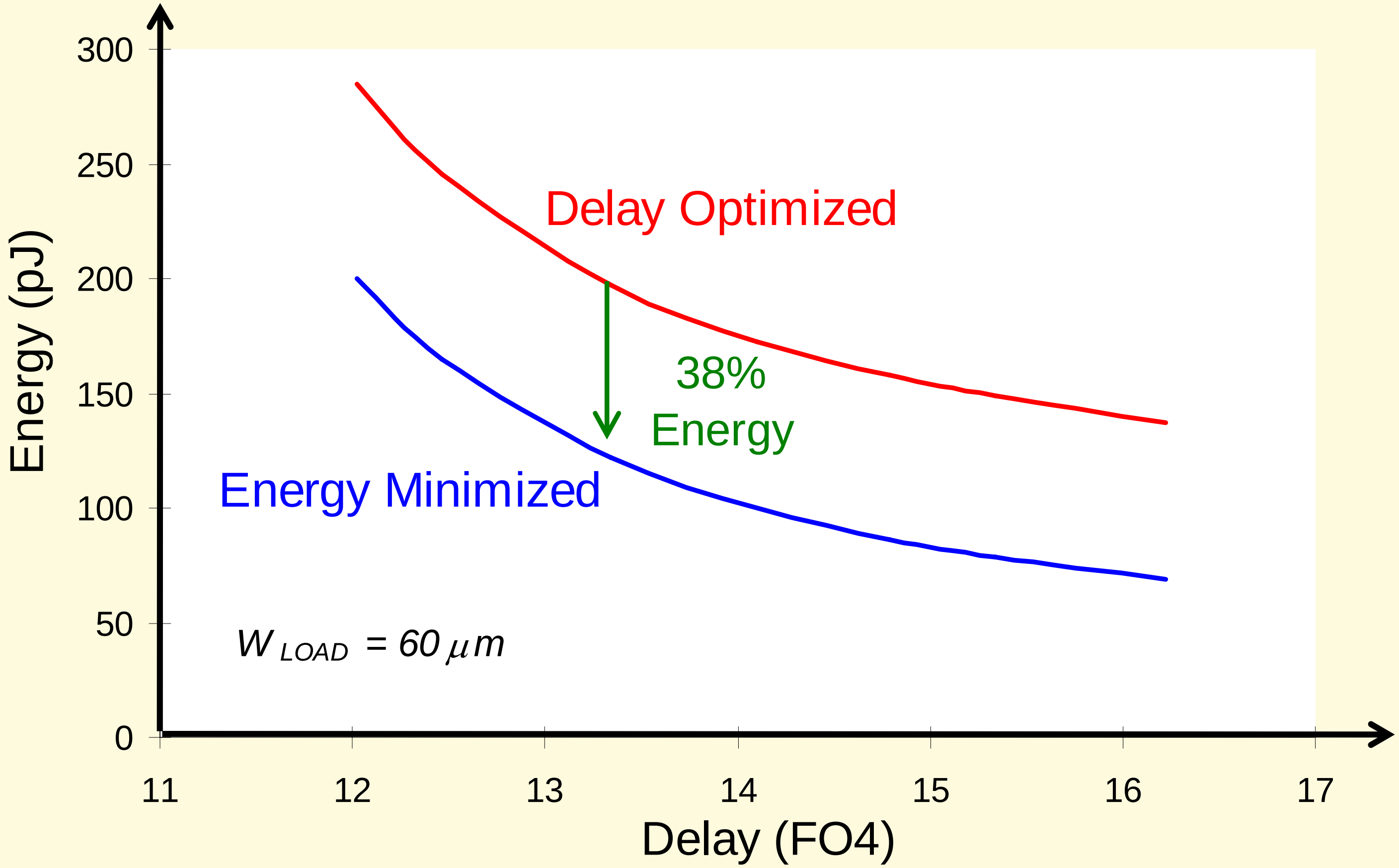
64-b KS: Minimal Energy vs. Delay



- 30 - 50% energy saving @ same performance
- 1.6 - 3.6X input size

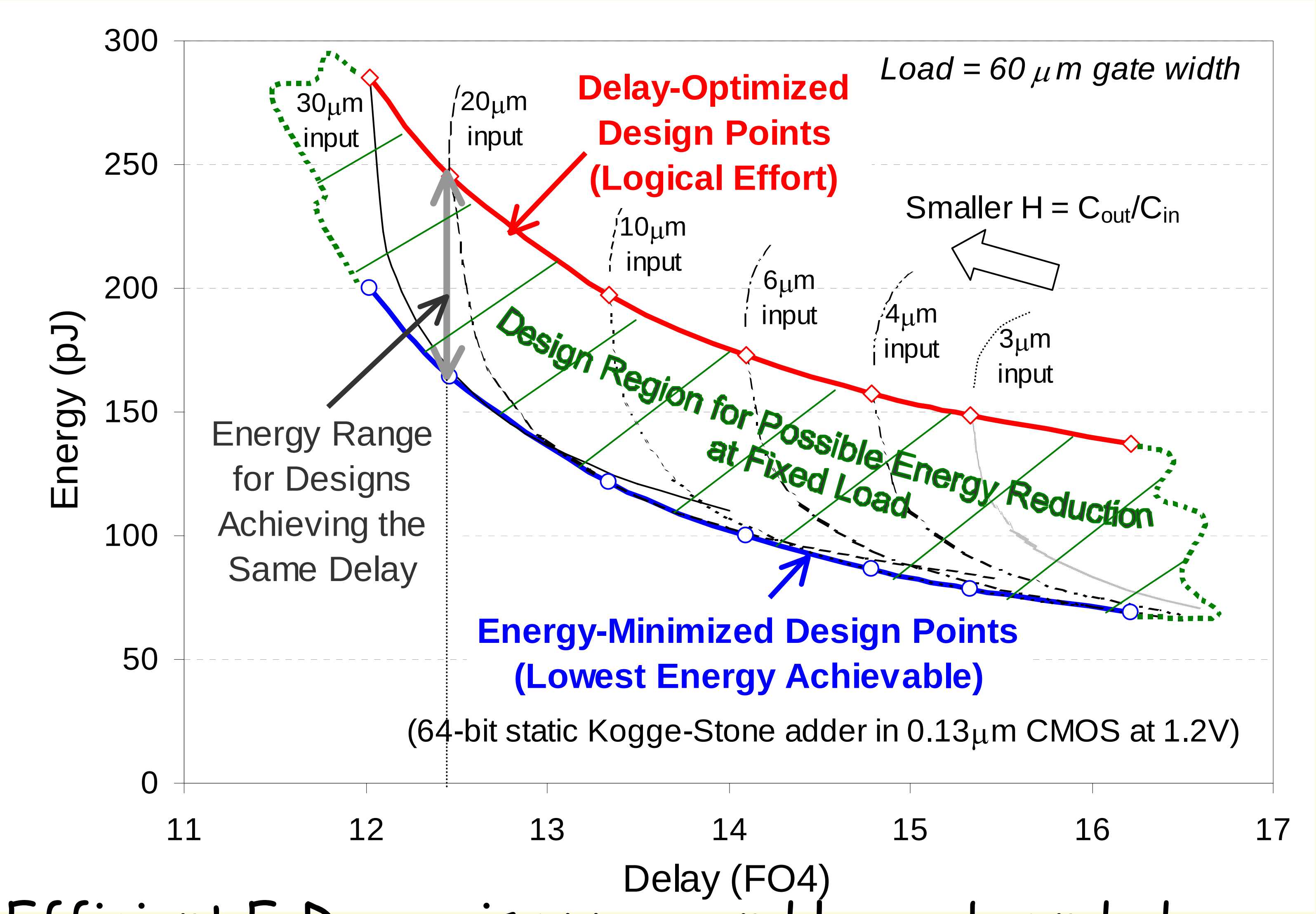
Pipelined System Optimization

Pipelined System Optimization

- Design constraints
  - Delay target
  - External I/O constraint

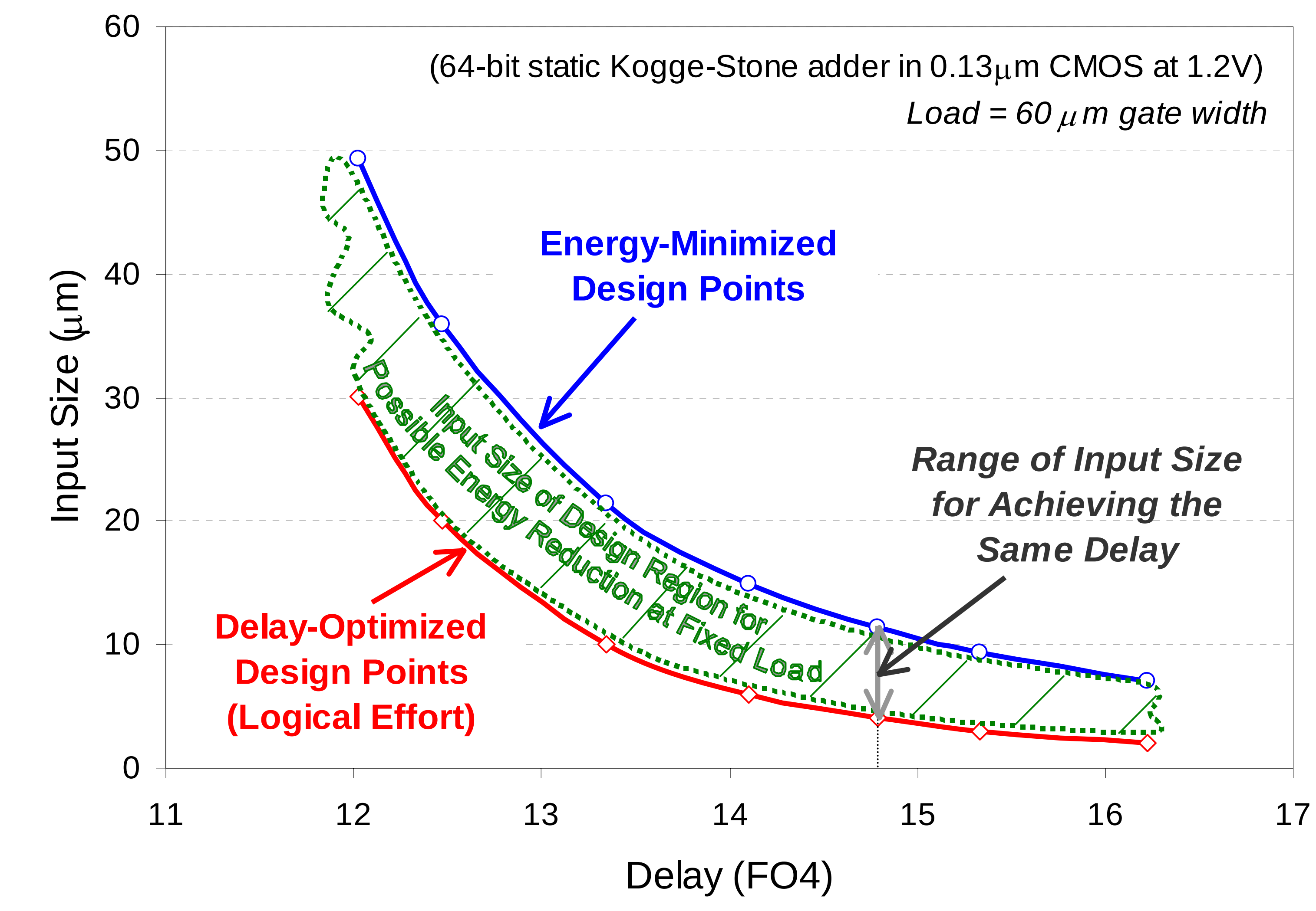
- How to obtain minimal-energy solution?
  - Pipelined stages
    - Minimized for energy
    - Sensitive to input and load variations
  - System level
    - Balancing energy sensitivities at pipelined boundaries
  - Recursive process

Pipelined Stage: Efficient E-D Area



- Efficient E-D area is upper- and lower-bounded

Efficient Input-Delay Area



- Larger/smaller input ⬄ less/more energy

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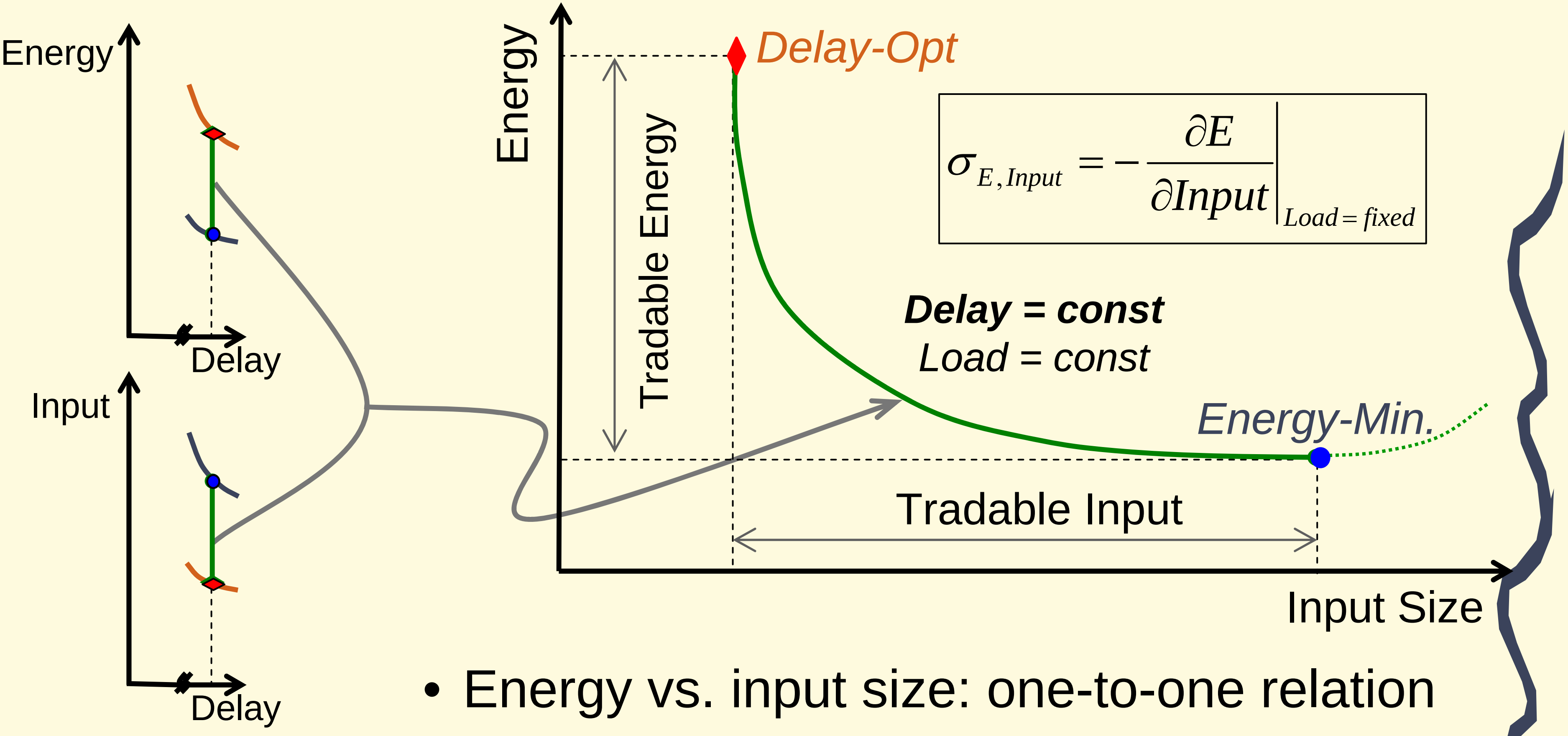
Efficient Energy-Input @ D = const.

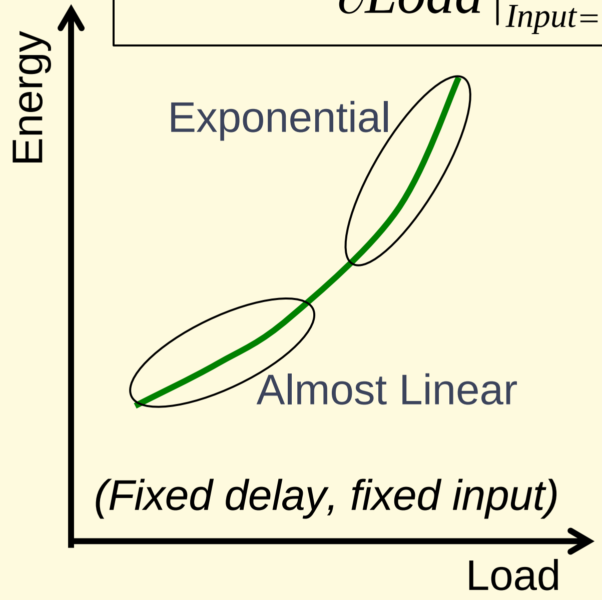


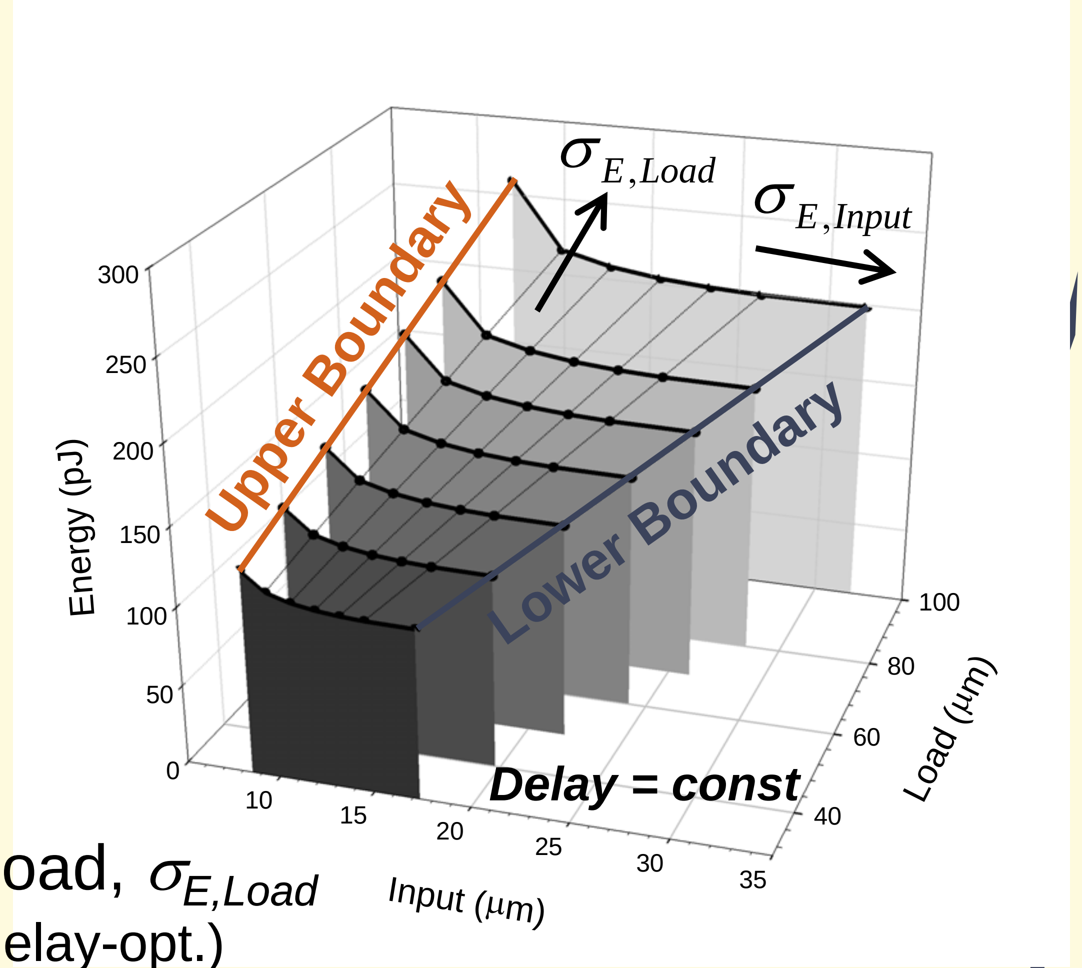
$$\sigma_{E,Input} = -\left.\frac{\partial E}{\partial Input}\right|_{Load = fixed}$$

- Energy vs. input size: one-to-one relation
  - – Energy sensitivity to input, $\sigma_{E,Input}$
- Flat energy in upper half of input range

Sensitivity to Load @ D = const.

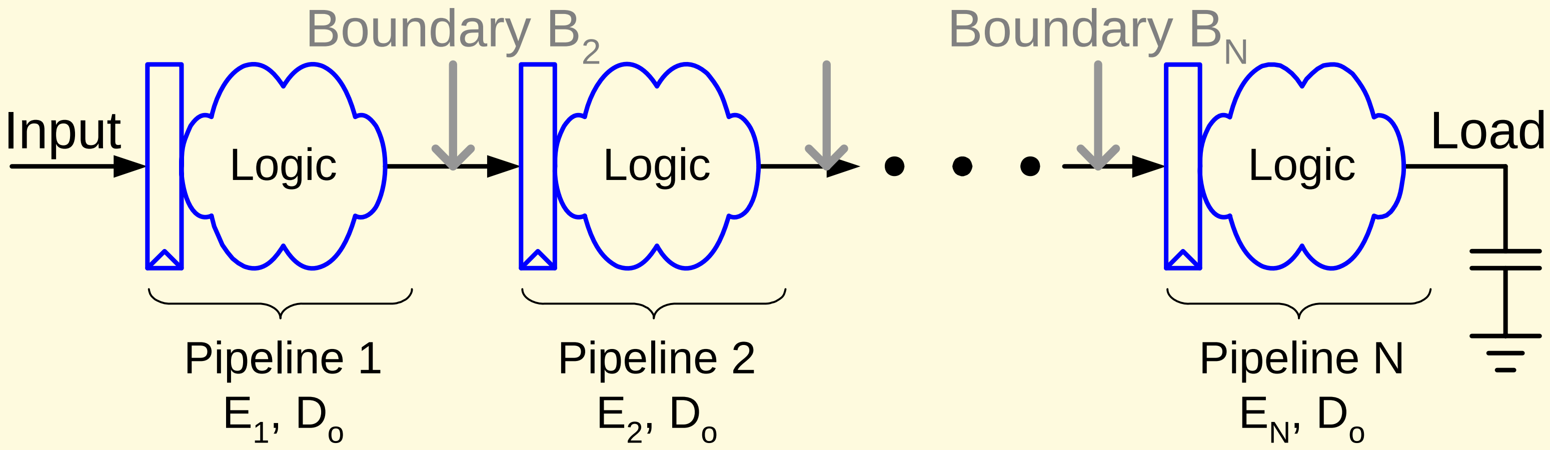
$$\sigma_{E,Load} = \left.\frac{\partial E}{\partial Load}\right|_{Input=fixed}$$





- Energy sens. to output load, $\sigma_{E,Load}$
  - More @ upper bound (delay-opt.)
  - Less @ lower bound (energy-min.)
- Energy components = energy + its sensitivities

System Energy Optimization



- Energy minimization
  - – Pipeline: minimize energy @ given input & load
  - – System: balance energy sensitivities @ boundaries

- Trading elements: input size, output load

- Optimal criteria:

$$\begin{cases} E_{Stage\,A_i} = minimal \\ \sigma_{E,Input\,A_i} = \sigma_{E,Load\,A_{i-1}} \end{cases}$$

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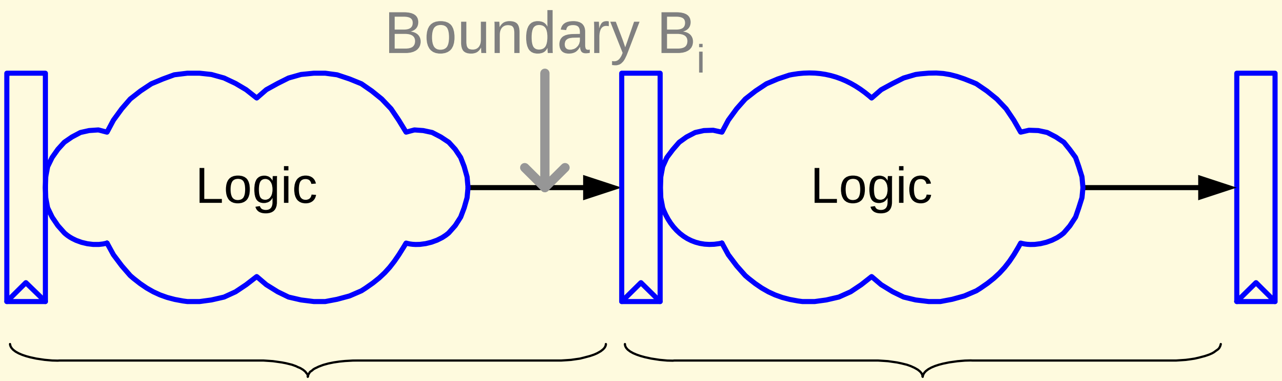
How to Achieve Less Total Energy



Boundary B_i

Logic

Logic

$(i\ -1)^{th}$ Pipeline: $\{E, D, \sigma_{E,Input}, \sigma_{E,Load}\}$

$i^{\ th}$ Pipeline: $\{E, D, \sigma_{E,Input}, \sigma_{E,Load}\}$

Case A:

□ $\sigma_{E,Input\ (i)} > \sigma_{E,Load\ (i-1)}$

- *Increase $i^{\ th}$ input*

  $\Rightarrow$ less E_{Total}

Case B:

▪ $\sigma_{E,Input\ (i)} < \sigma_{E,Load\ (i-1)}$

▪ *Reduce $i^{\ th}$ input*

  $\Rightarrow$ less E_{Total}

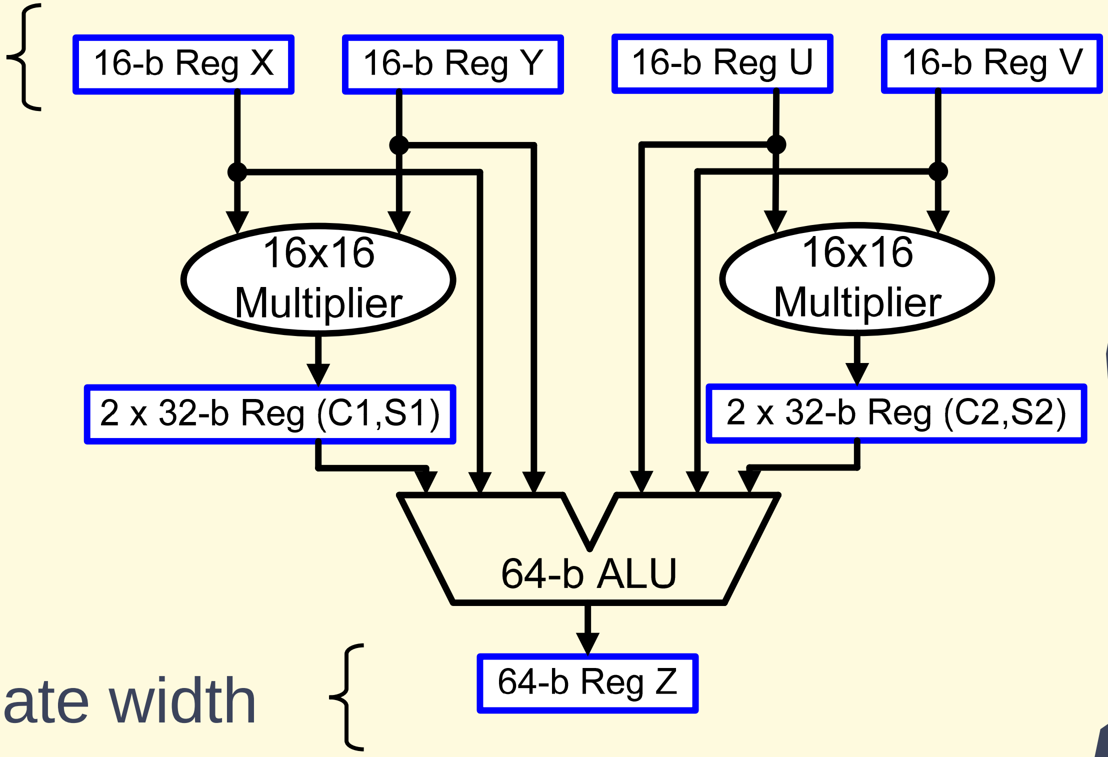
$$\boxed{E_{i-1} + E_i = min \;\Leftrightarrow\; \sigma_{E,Input(i)} = \sigma_{E,Load(i-1)}}$$

Case Study: Media Datapath

Maximal Input = 30μm

Target Delay = 17FO_4

Output Load = 60μm gate width



- What is the minimal energy solution?

Case Study: Optimal Criteria

$\mathrm{MAX}\{X,Y,U,V\} = 30\mu m$

$\{Z\} = 60\mu m$

$\mathrm{Delay} = 17\mathrm{FO}_4$

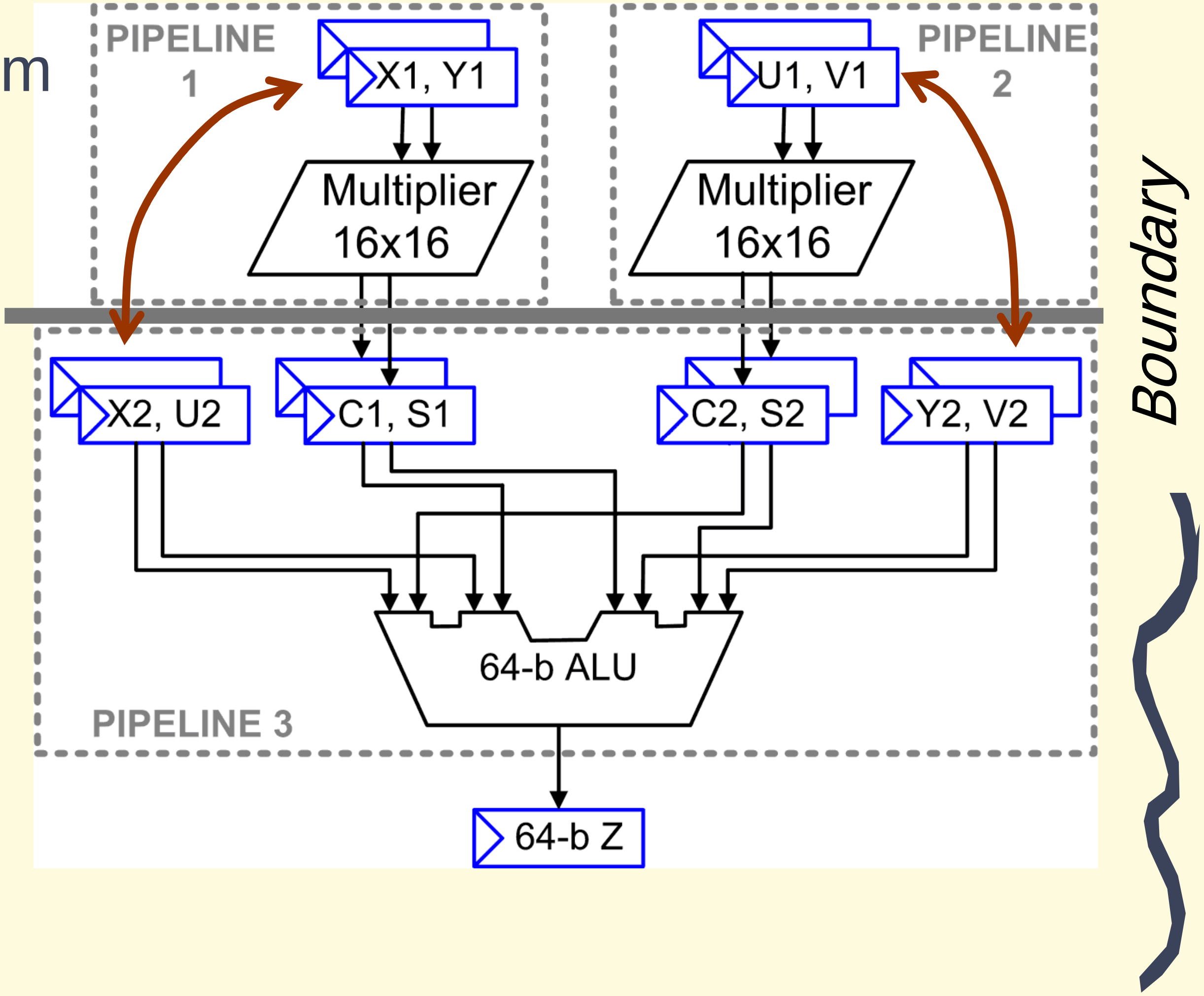
$E\{P1\} = \mathrm{min.}$

$E\{P2\} = \mathrm{min.}$

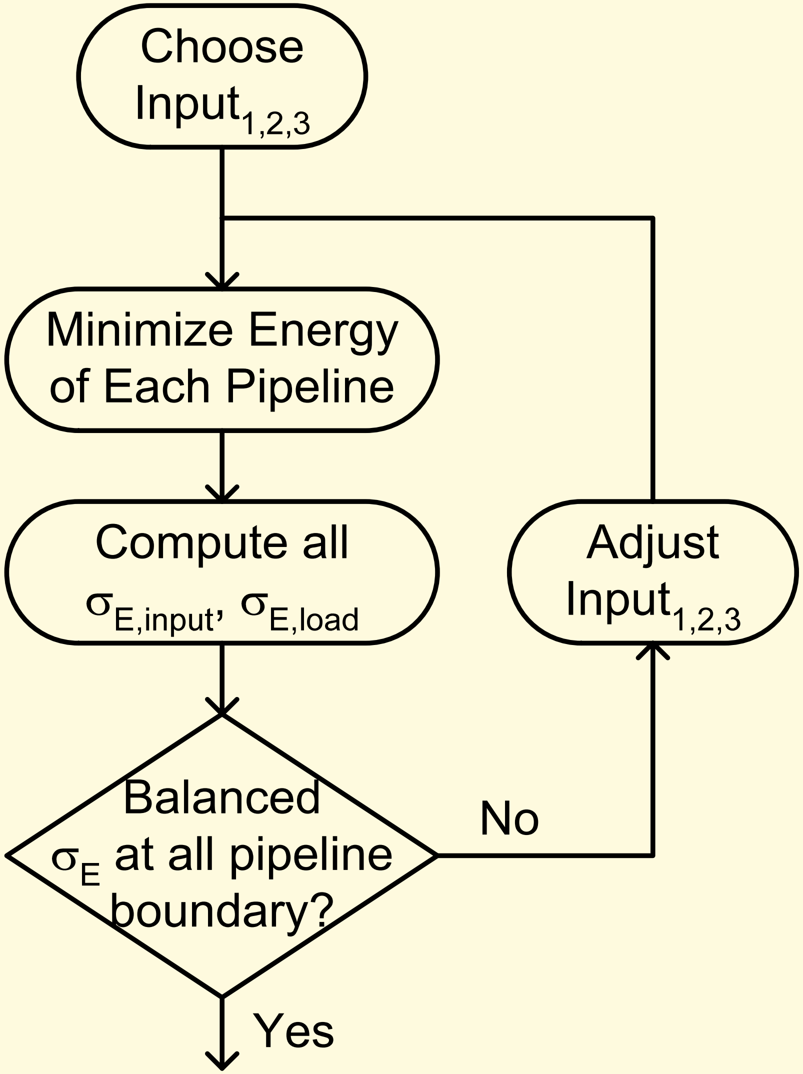
$E\{P3\} = \mathrm{min.}$

$$\sigma_{E,\mathrm{Load\ P1}} + \sigma_{E,\mathrm{Load\ P2}} = \sigma_{E,\mathrm{Input\ P3}}$$

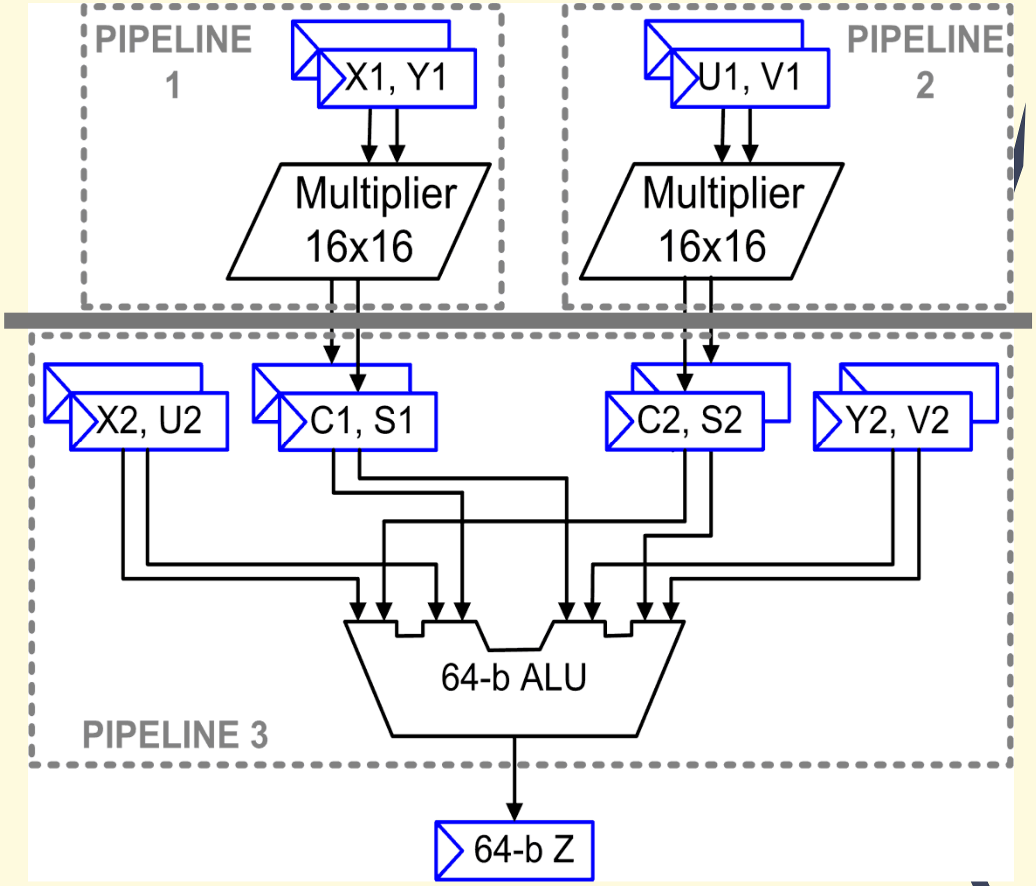
Simplified Datapath



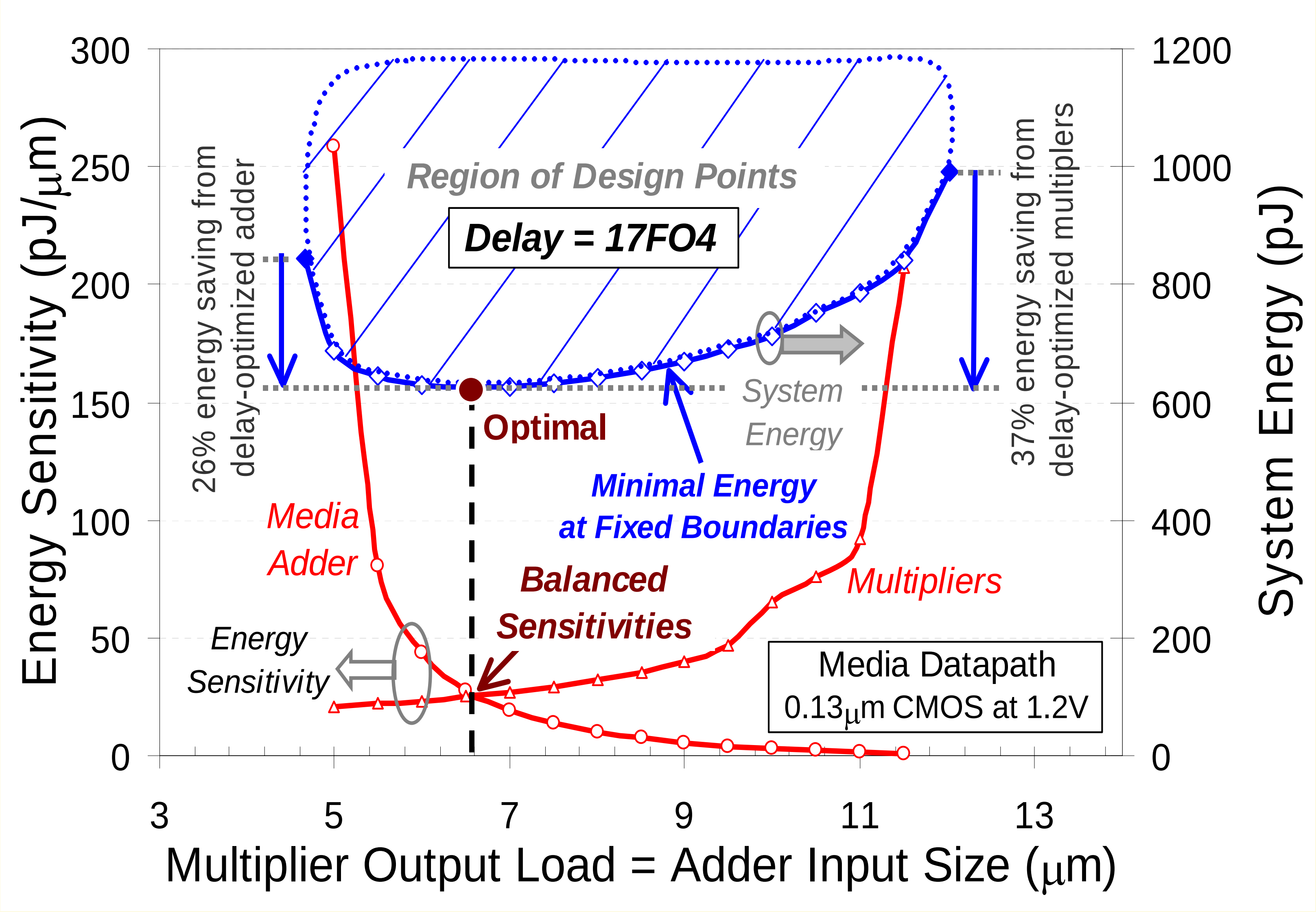
Case Study: Optimal Algorithm


Choose Input$_{1,2,3}$
Minimize Energy of Each Pipeline
Compute all $\sigma_{E,input}$, $\sigma_{E,load}$
Balanced σ_E at all pipeline boundary?
No
Adjust Input$_{1,2,3}$
Yes

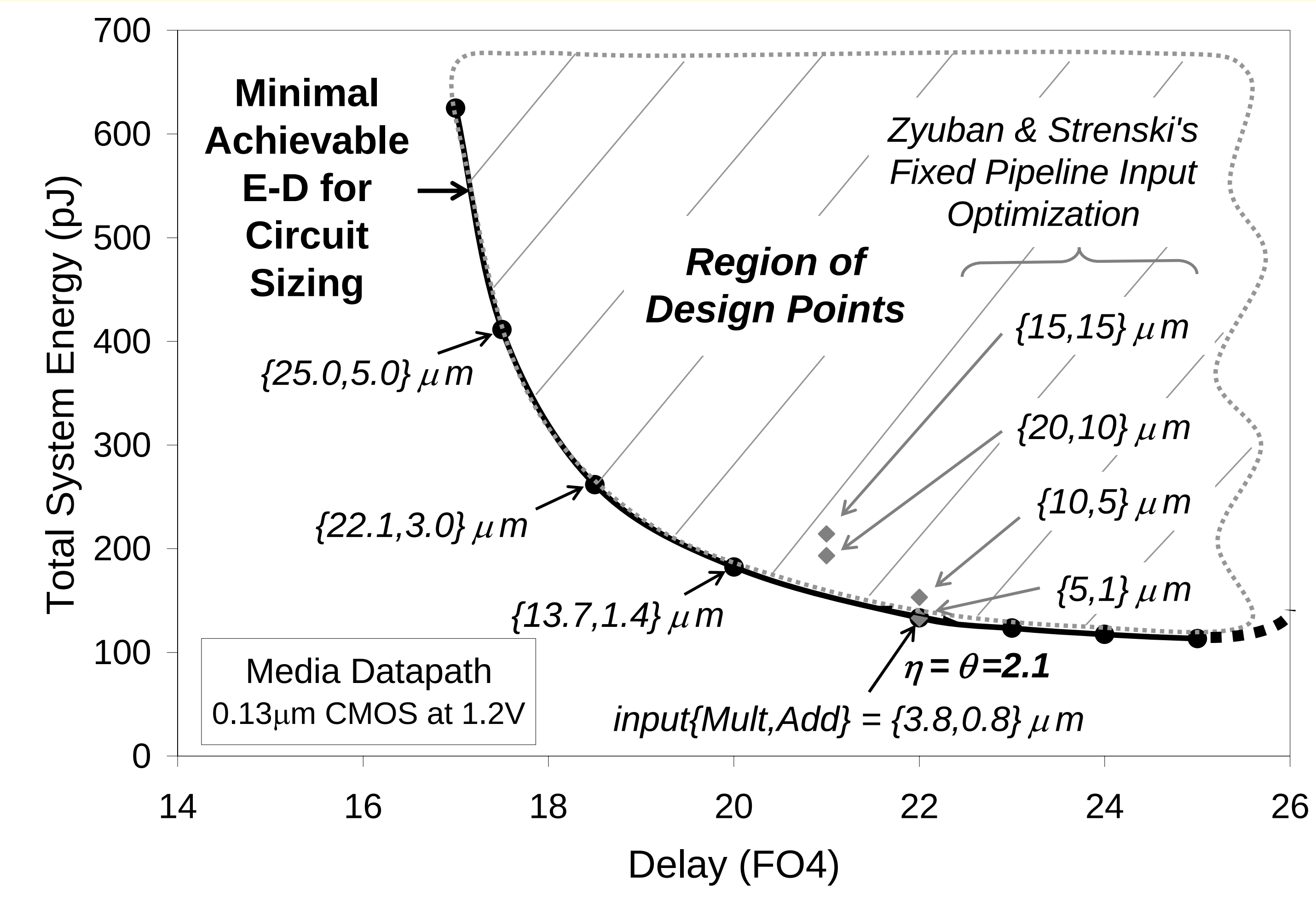
Simplified Datapath



Case Study: Media Datapath Solution

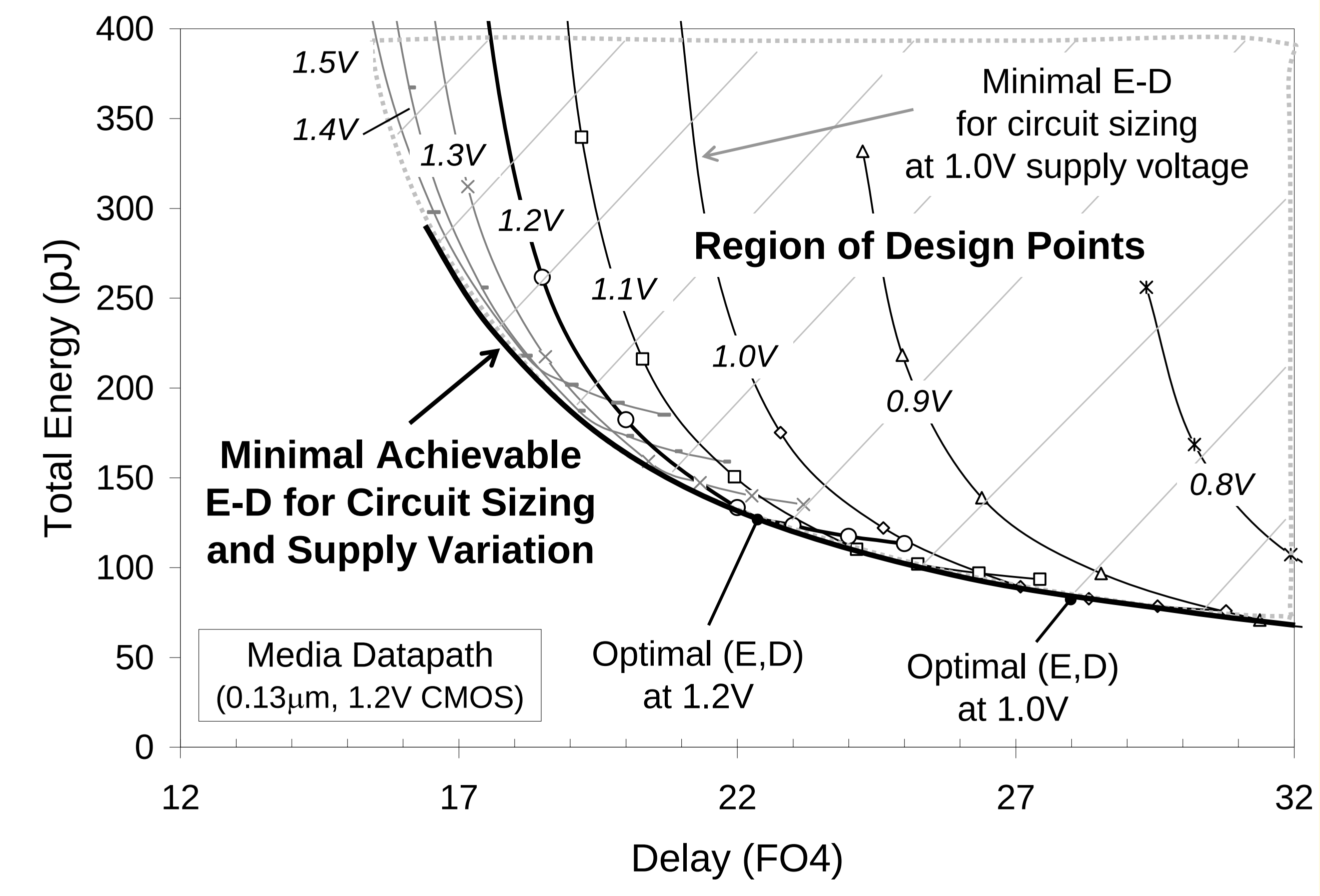


System Energy-Delay @ V_{DD}=const.



- Similar E-D characteristics as single stages
- Possibly less input size @ lower delay

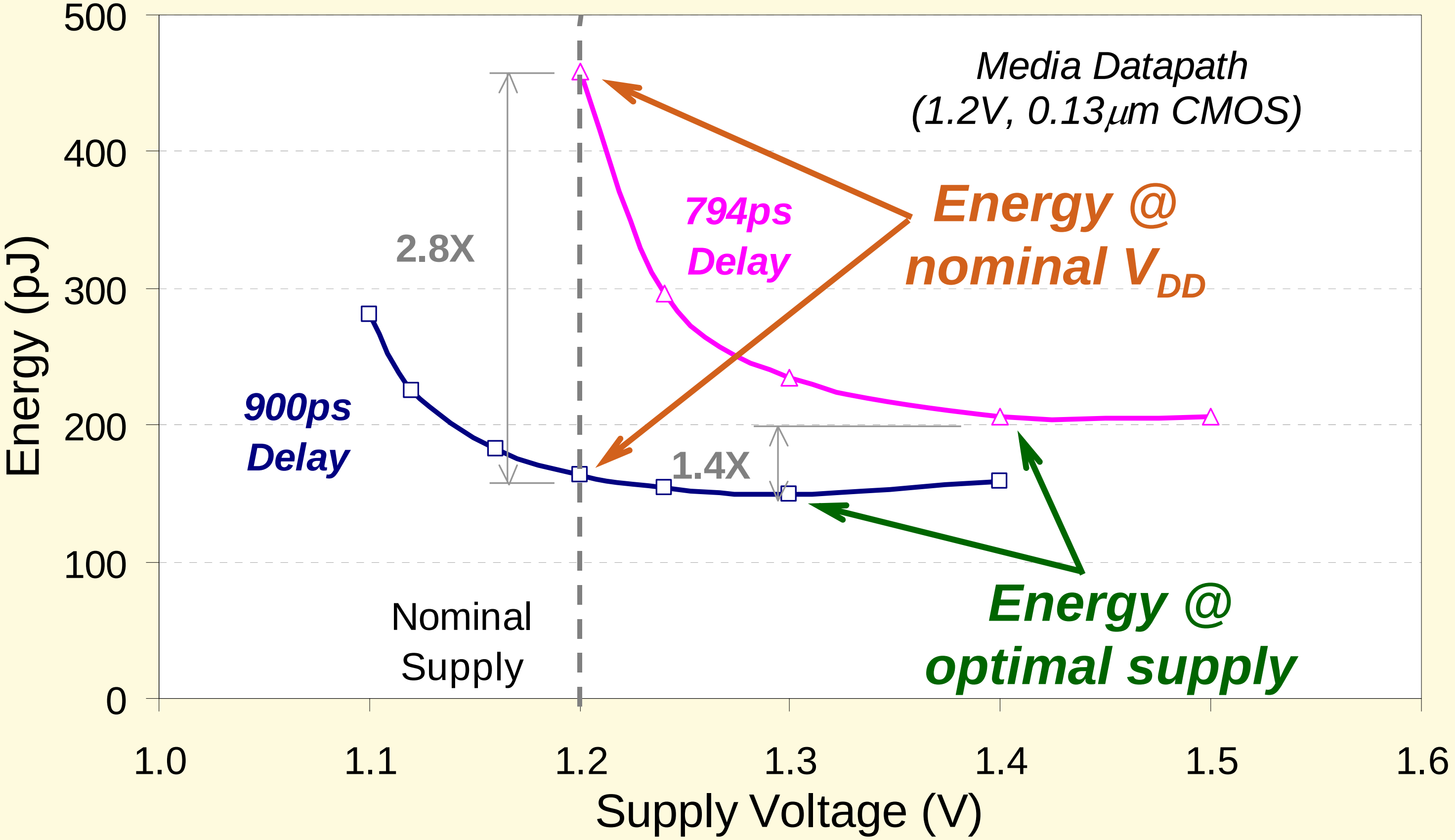
Effect of Supply Scaling



- Efficient {E, D, V_{DD}} are dependent
- Optimal criterion:

$$\boxed{\left.\frac{D}{E}\frac{\partial E}{\partial D}\right|_{sizing} = \left.\frac{D}{E}\frac{\partial E}{\partial D}\right|_{supply} \quad or \quad \eta_{system} = \theta}$$

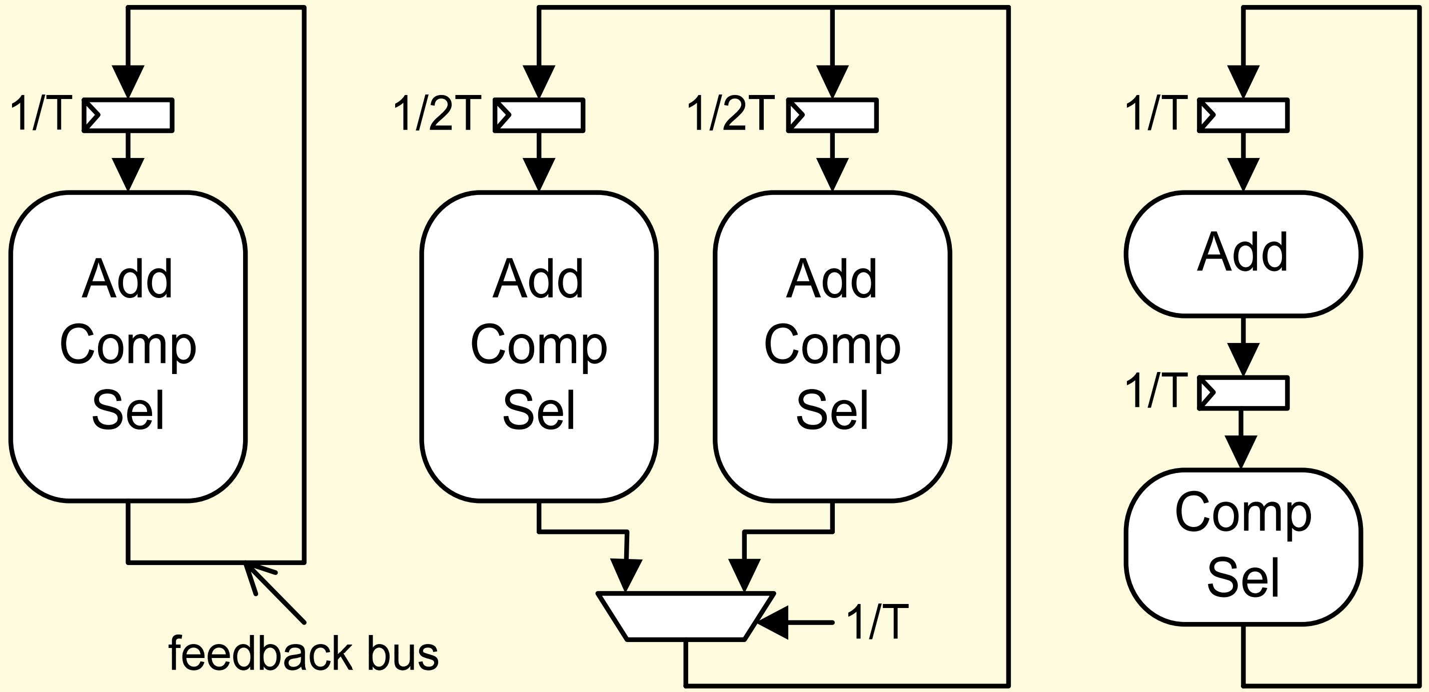
Potential Saving of System Energy



- Significant energy saving with correct supply or delay selection

Energy-Delay Improvement of Pipelined Stages

Architectural Advantages



(a) Reference

(b) Parallelism

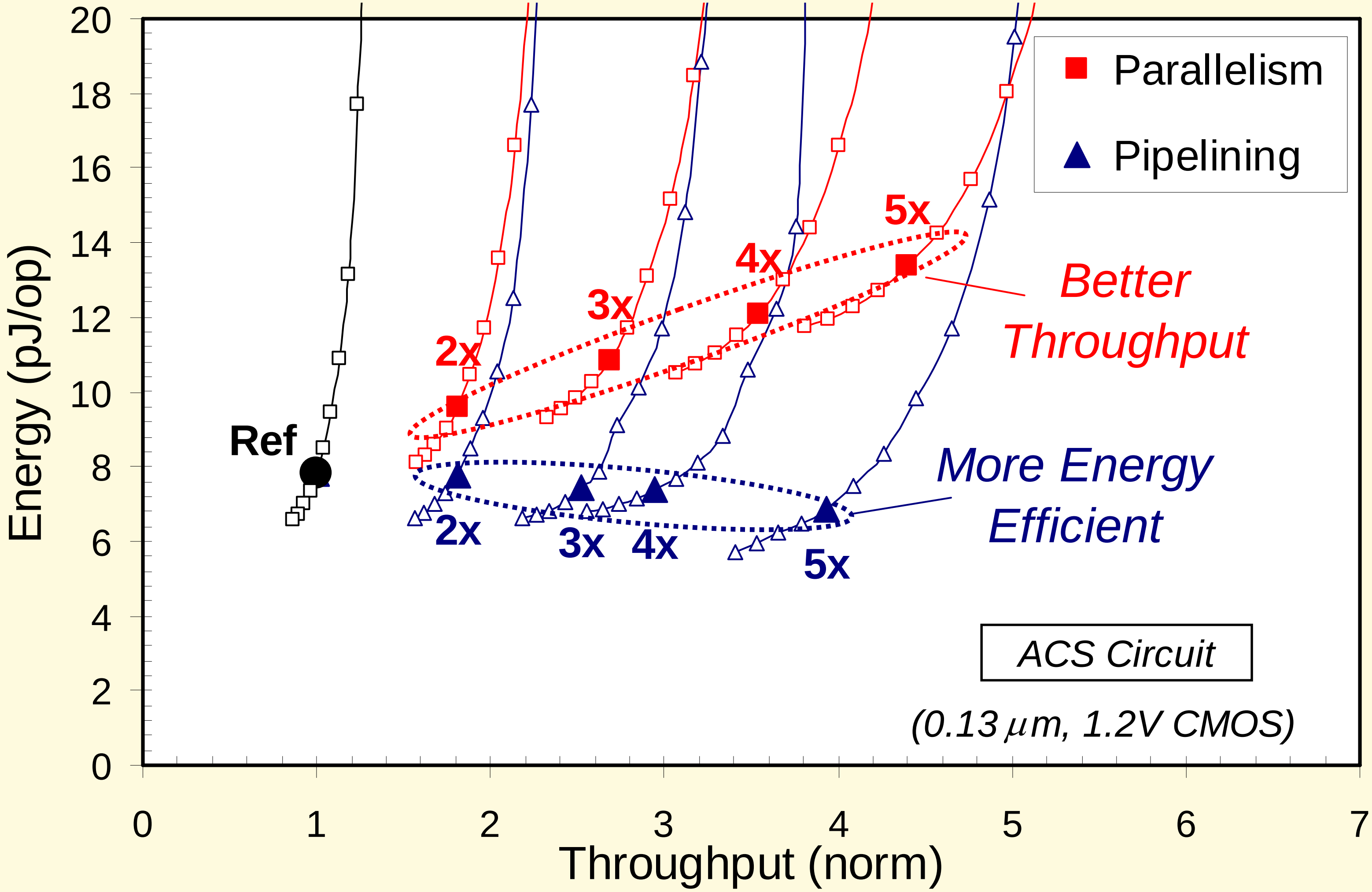
(c) Pipelining

- Feedback bus is typical
- Length = 128μm

- ≅ N • area
- ≅ N • bus length
- 1/N clock rate

- ≅ area
- ≅ bus length
- Same clock rate

Energy-Throughput Comparison



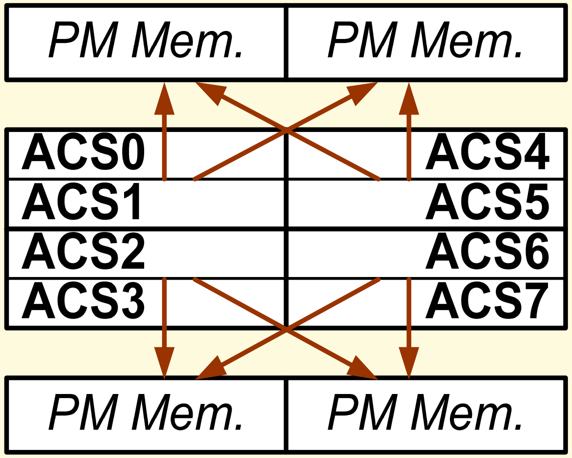
- Pipelining is mostly more efficient in E-D domain!

ACS Unit Implementation

Application:

64-state rate-$\frac{1}{2}$

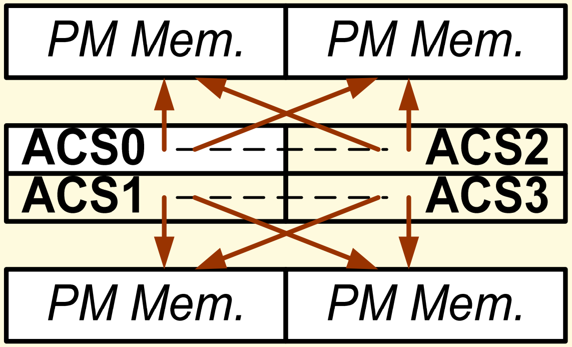
Viterbi decoder



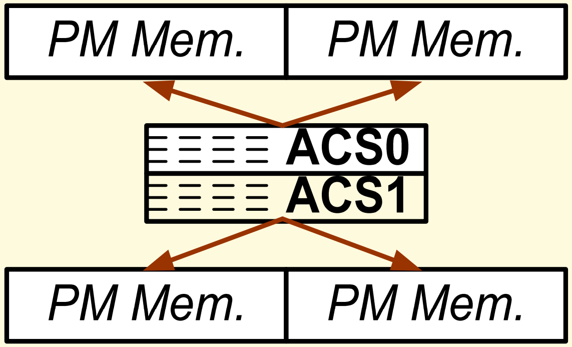
(a) Non-Pipelined

- Not pipelined
- 8 ACS circuits
- Largest area
- *Least PM entries per ACS*

- Pipelined-2
- 4 ACS circuits
- Midway area
- *More PM entries / ACS*



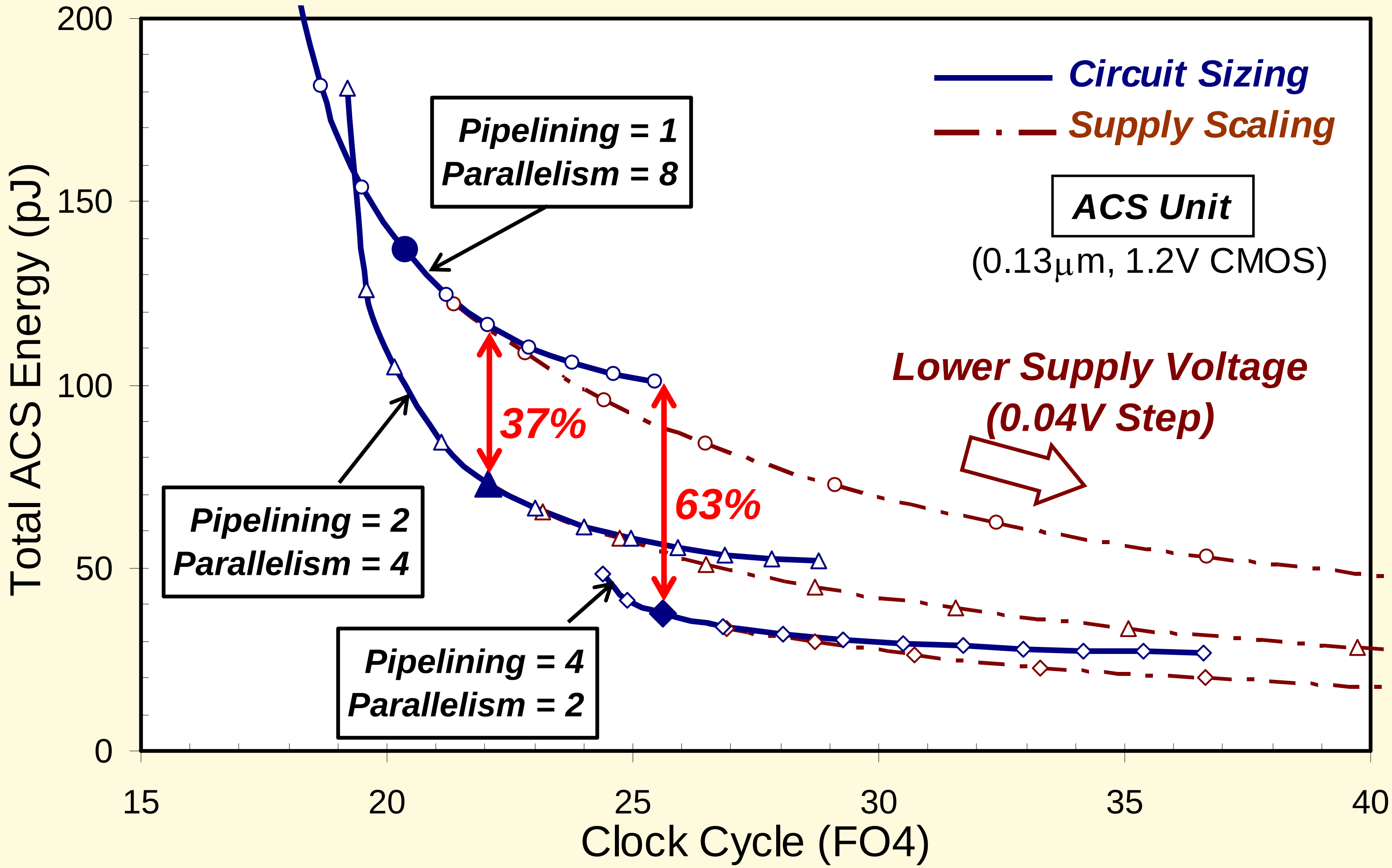
(b) Pipelined-2



(c) Pipelined-4

- Pipelined-4
- 2 ACS circuits
- Small area
- *Most PM entries / ACS*

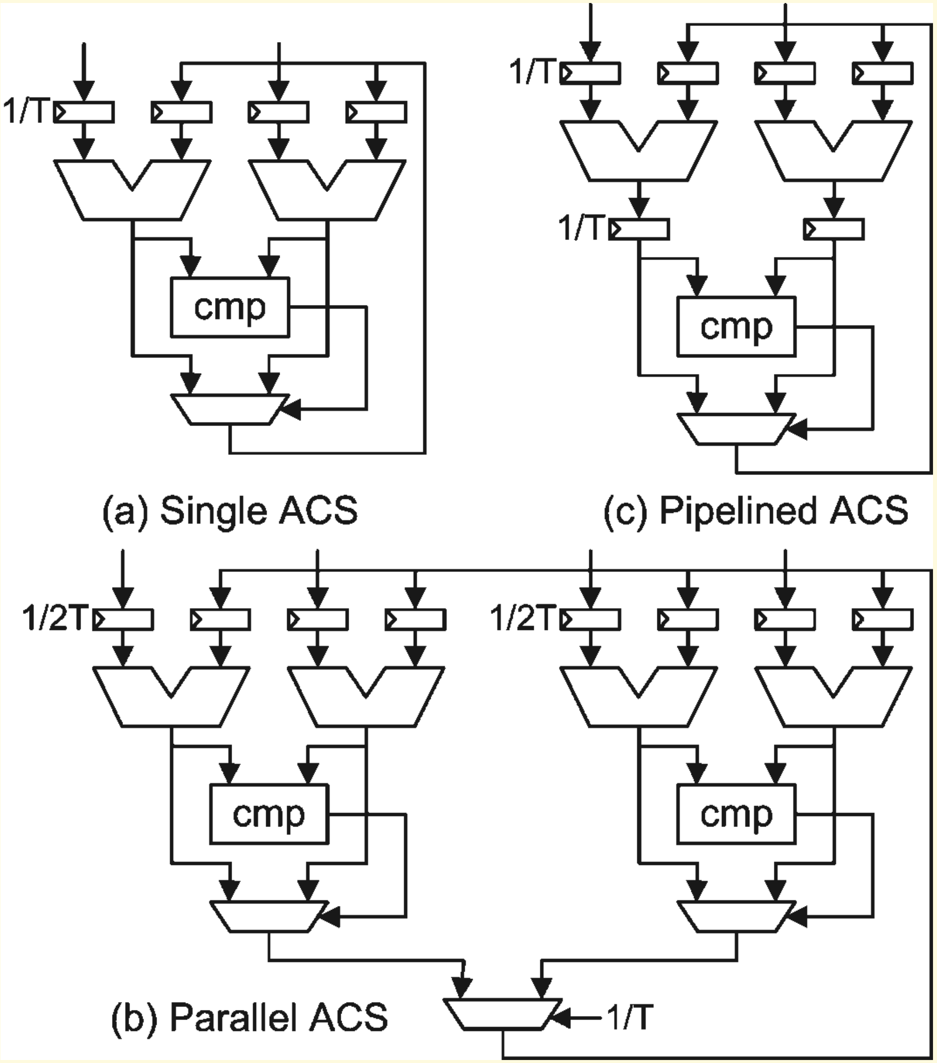
Energy-Throughput Comparison



- Less energy for deeper pipeline at given throughput

Designing a System for a Fixed Performance in the Energy-Delay Space

Pipelining and Parallelism for an ACS Circuit



(a) Single ACS

(c) Pipelined ACS

(b) Parallel ACS

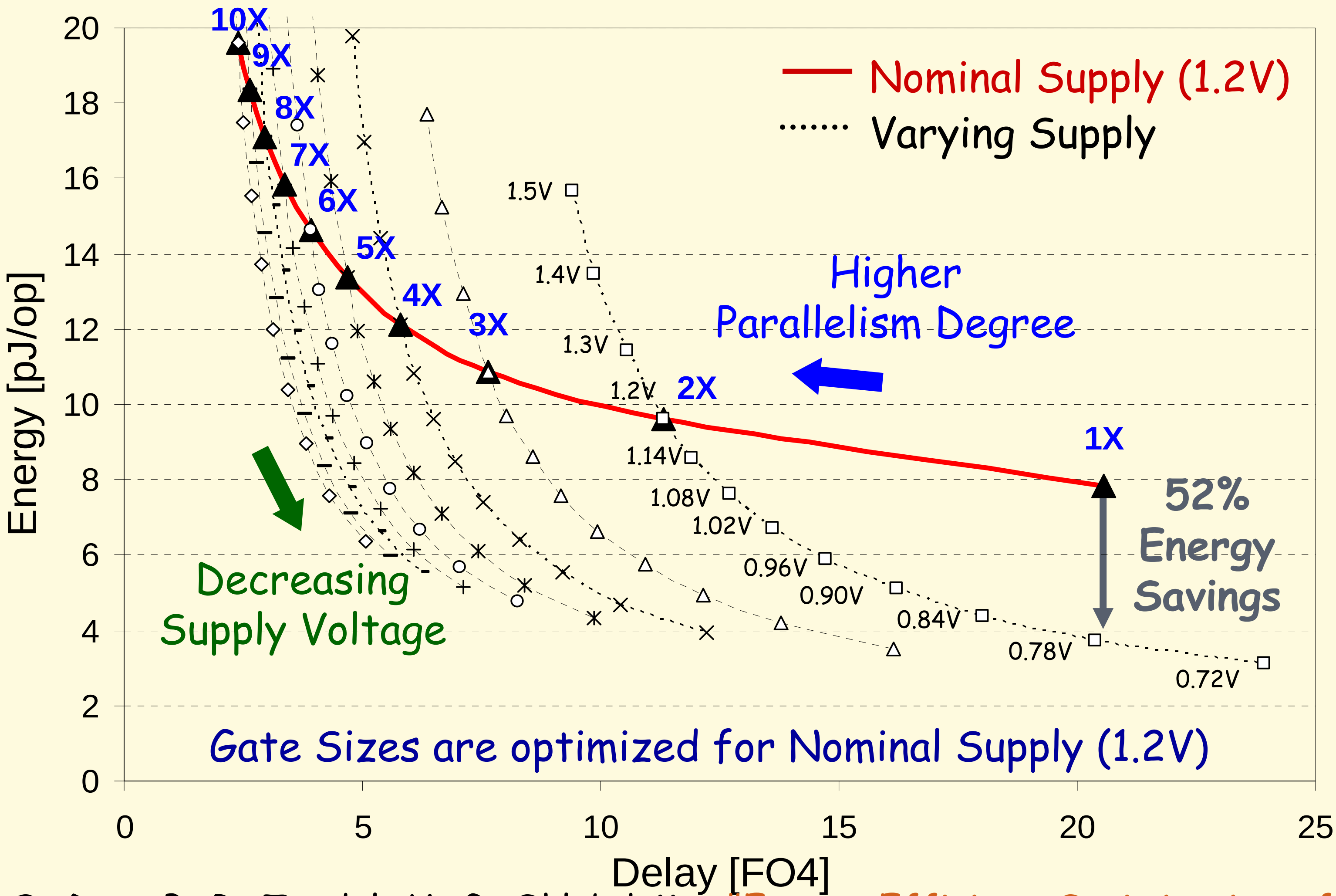
Ideal Degree-N Parallelism

- N-time throughput
- (Area, routing) overhead

Ideal Depth-N Pipelining

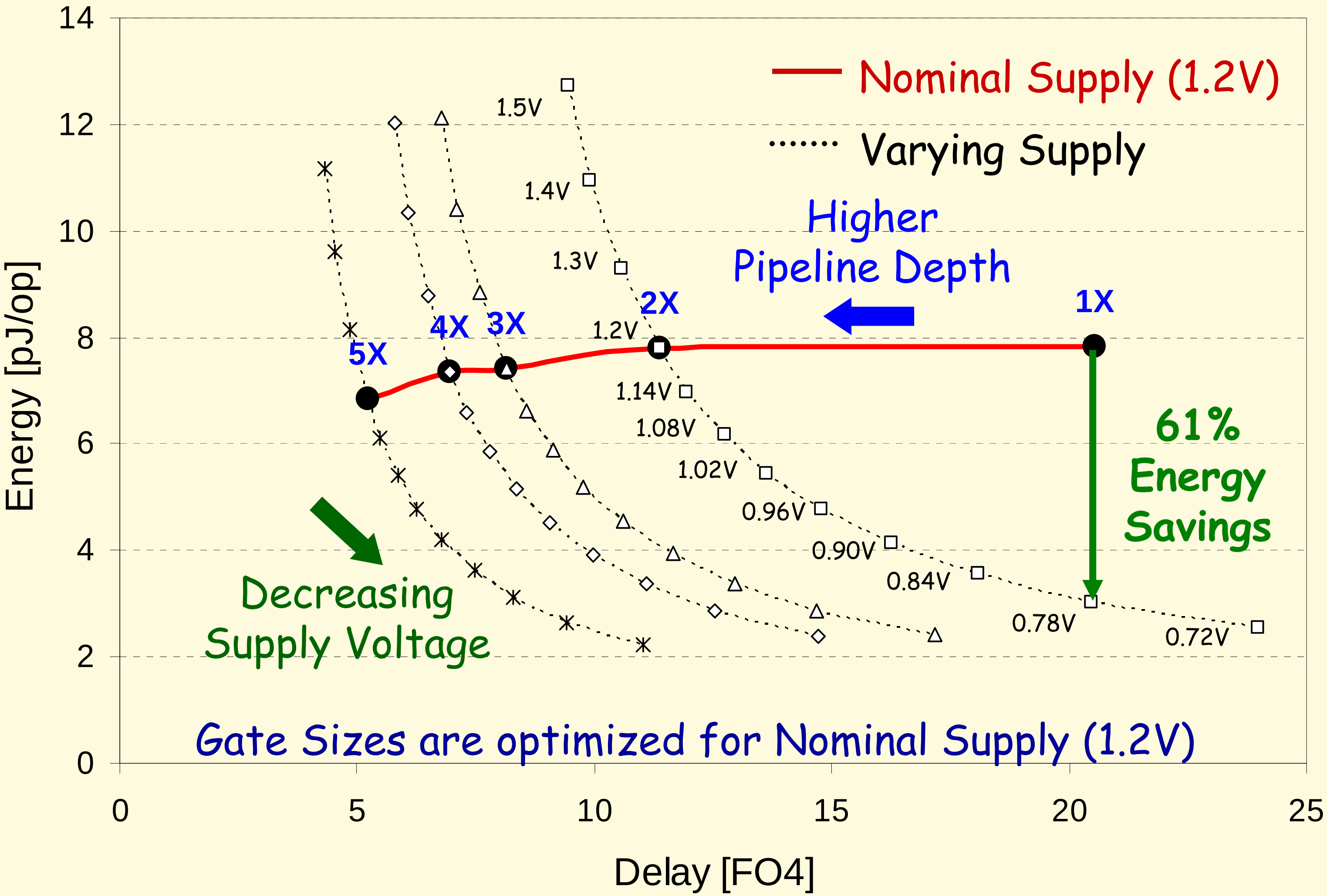
- N-time throughput
- CSE overhead

Energy-Delay Results for Parallelism



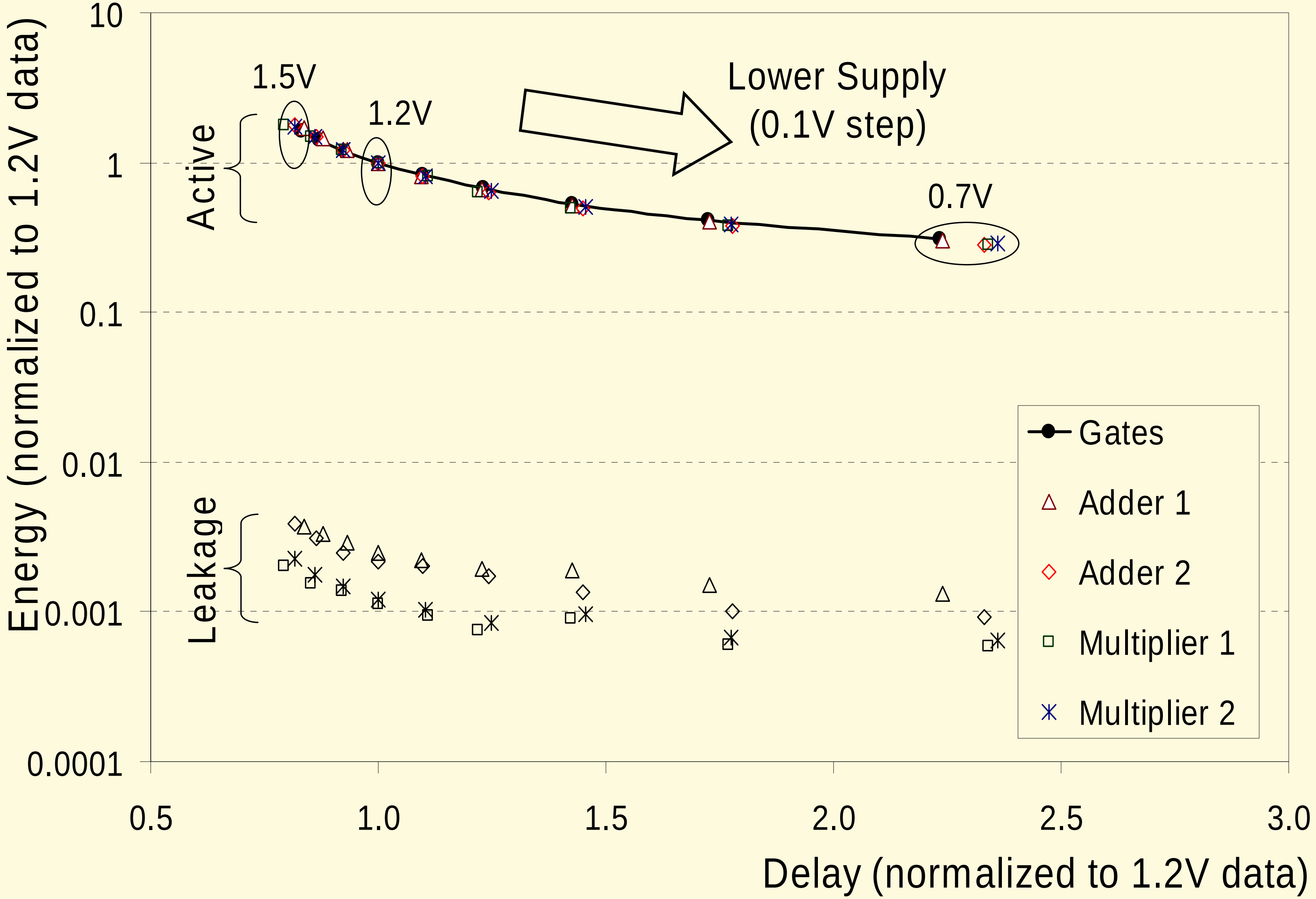
H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, "Energy-Efficient Optimization of the Viterbi ACS Unit Architecture", Proceedings of the Asian Solid-State Circuit Conference, A-SSCC 2005, Hsinchu, Taiwan, November 1-3, 2005.

Energy-Delay Results for Pipelining

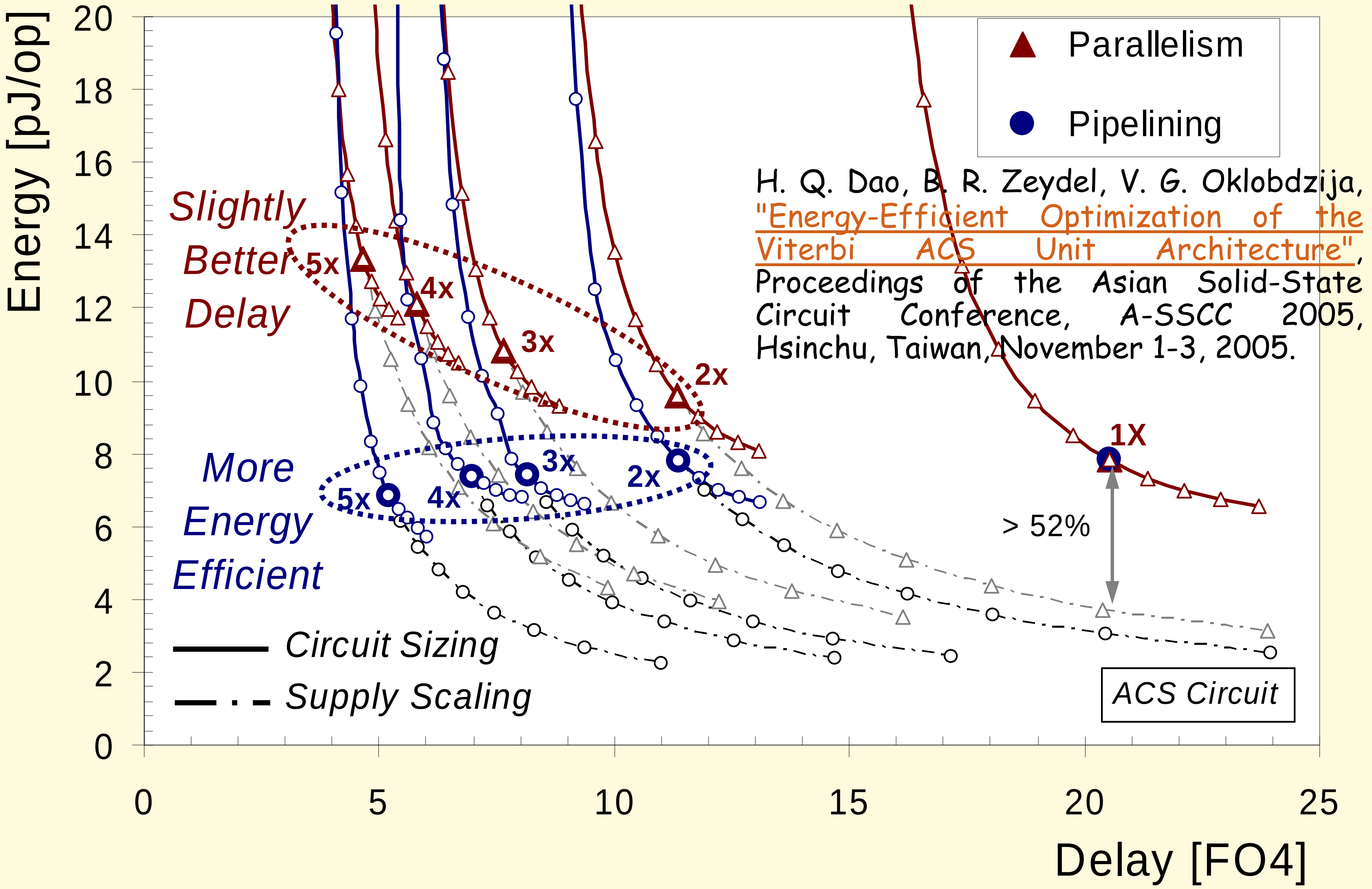


H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, "Energy-Efficient Optimization of the Viterbi ACS Unit Architecture", Proceedings of the Asian Solid-State Circuit Conference, A-SSCC 2005, Hsinchu, Taiwan, November 1-3, 2005.

Energy-Delay Estimation Matches Complex Circuit Simulation

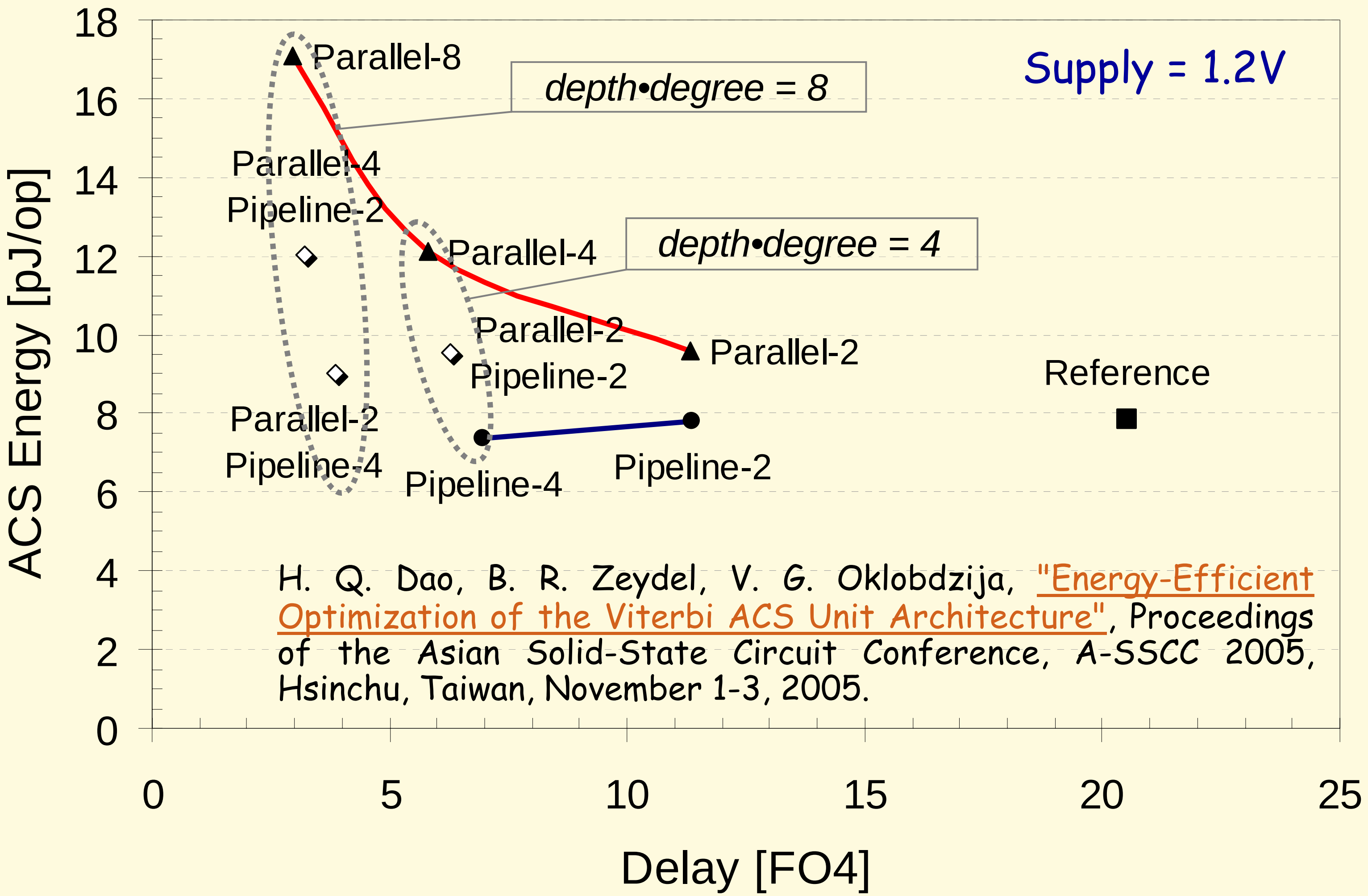


Energy Efficiency of Architectural Choices (including supply scaling and circuit sizing)



H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, "Energy-Efficient Optimization of the Viterbi ACS Unit Architecture", Proceedings of the Asian Solid-State Circuit Conference, A-SSCC 2005, Hsinchu, Taiwan, November 1-3, 2005.

Eergy-Delay Results for Parallelism and Pipelining



Supply = 1.2V

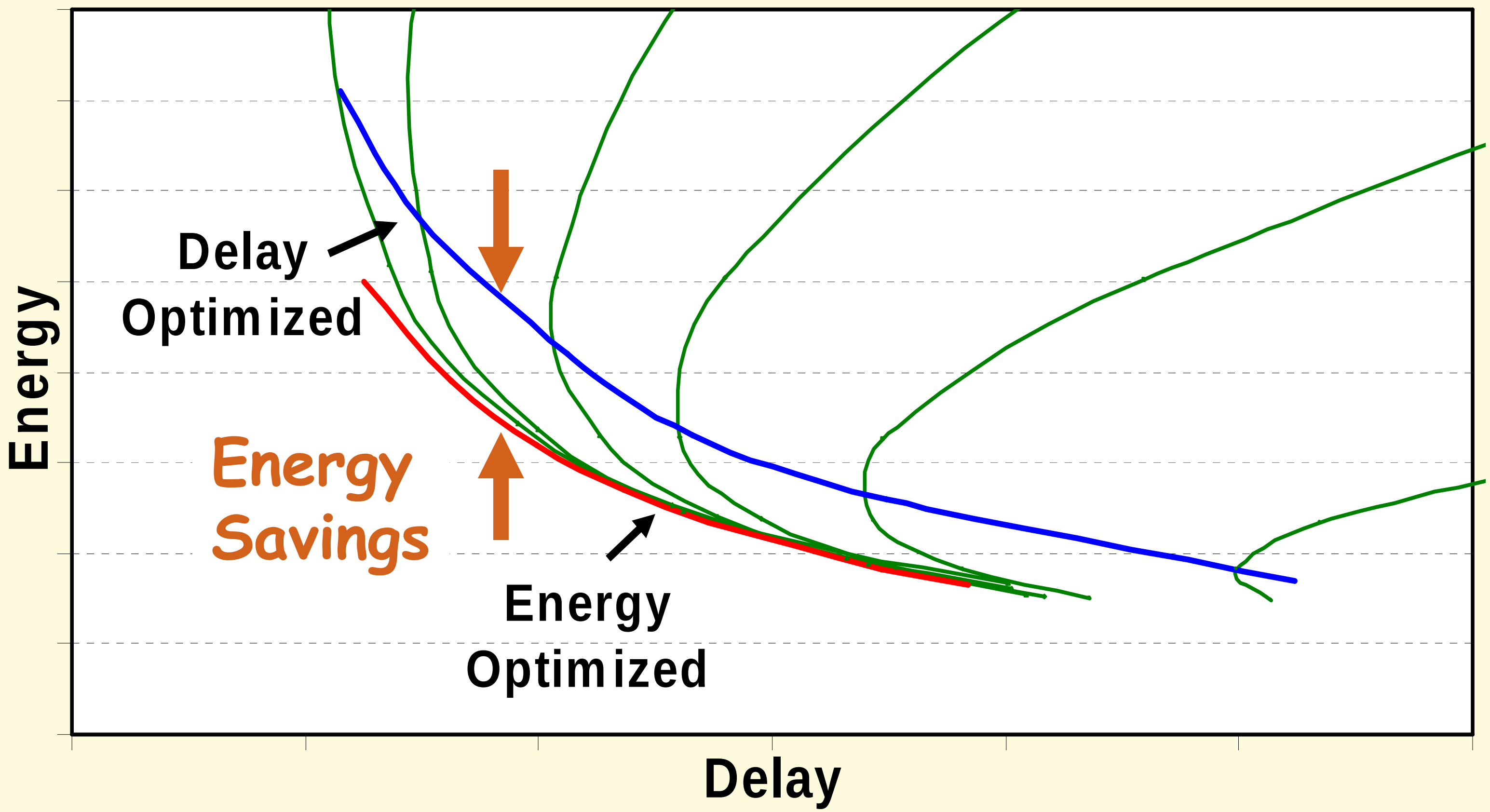
depth•degree = 8

depth•degree = 4

H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, "Energy-Efficient Optimization of the Viterbi ACS Unit Architecture", Proceedings of the Asian Solid-State Circuit Conference, A-SSCC 2005, Hsinchu, Taiwan, November 1-3, 2005.

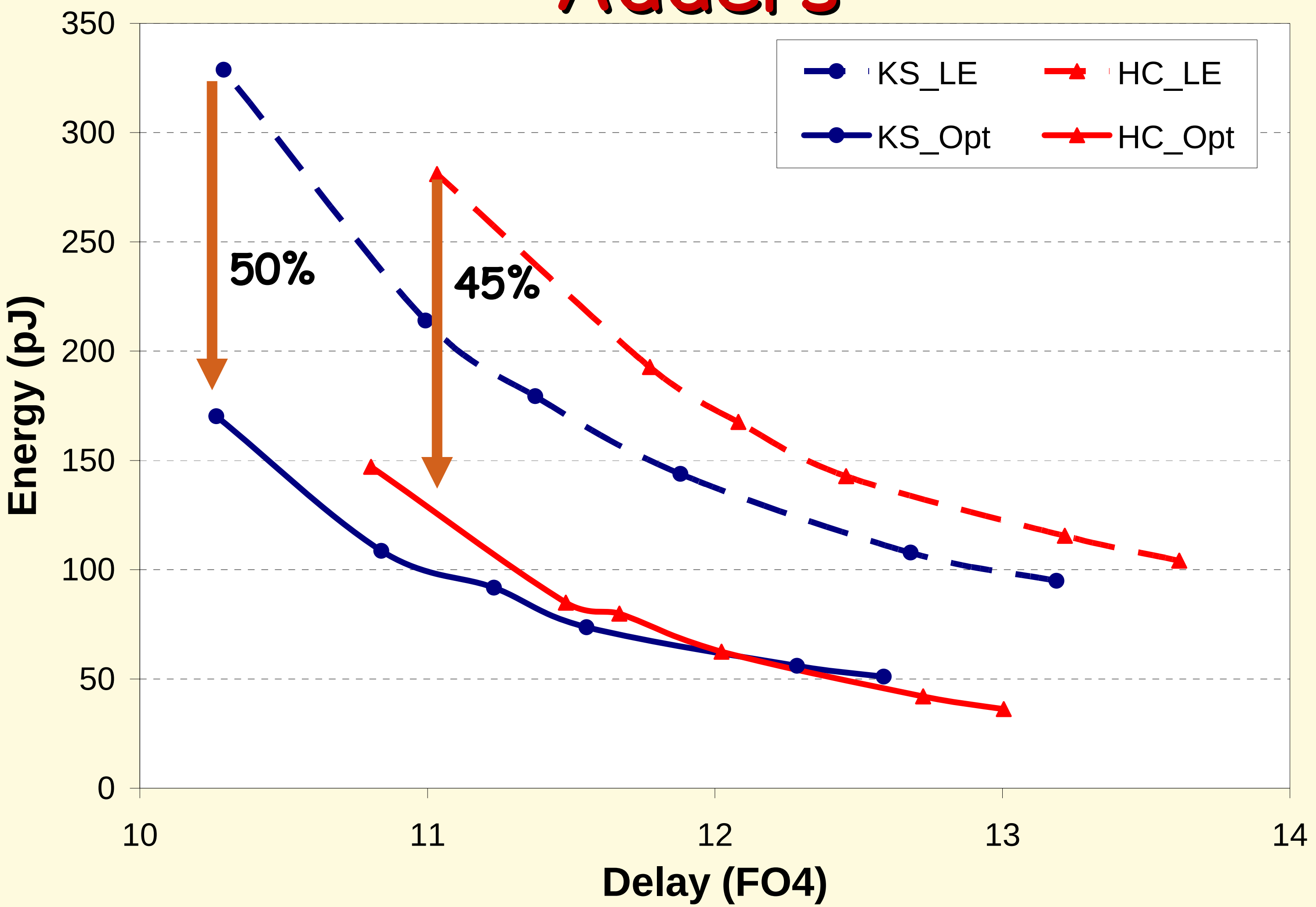
Pipelining has the Best Energy-Delay Tradeoff

Is it possible to lower the Energy ?



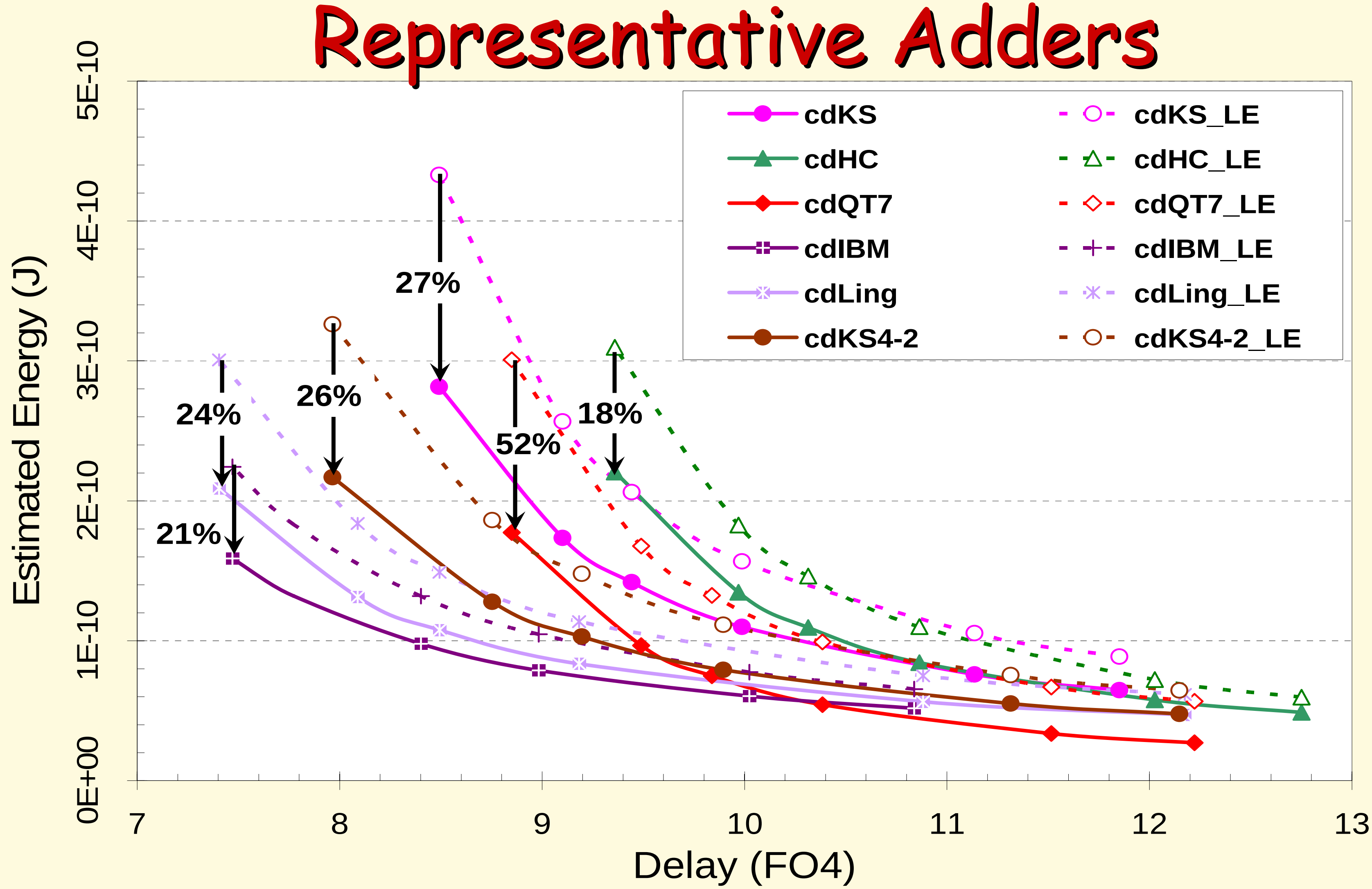
- Reduce Energy for same Delay!
- Improve Delay for same Energy!

Achieved Energy Savings in KS and HC Adders



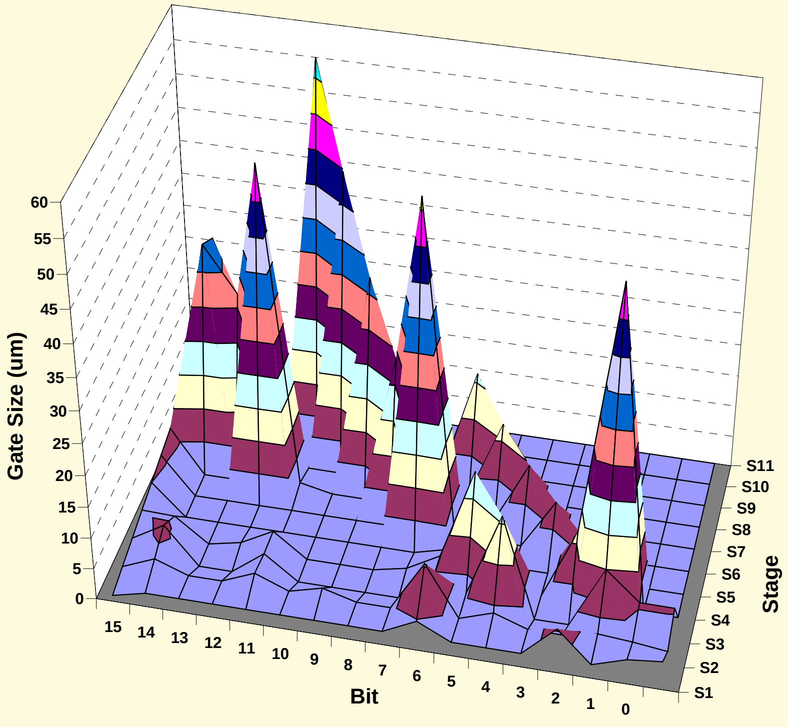
- Simulation of 64-bit static adders confirms saving!

Achieved Energy Savings in Representative Adders

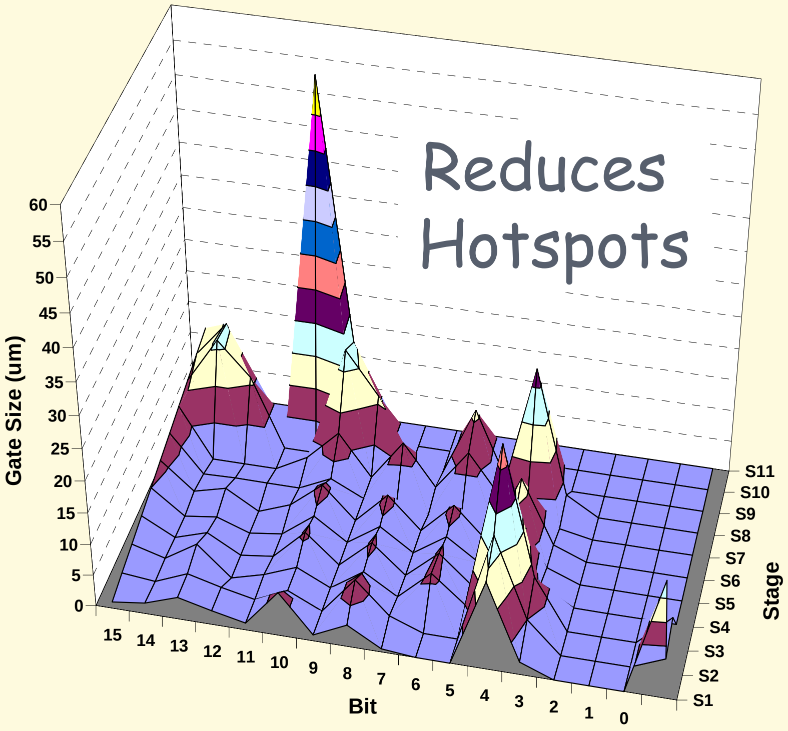


- Comparison of high-performance 64-bit adders
  - Delay and Energy Optimized

Reduction of Hot-Spots



Delay Optimized

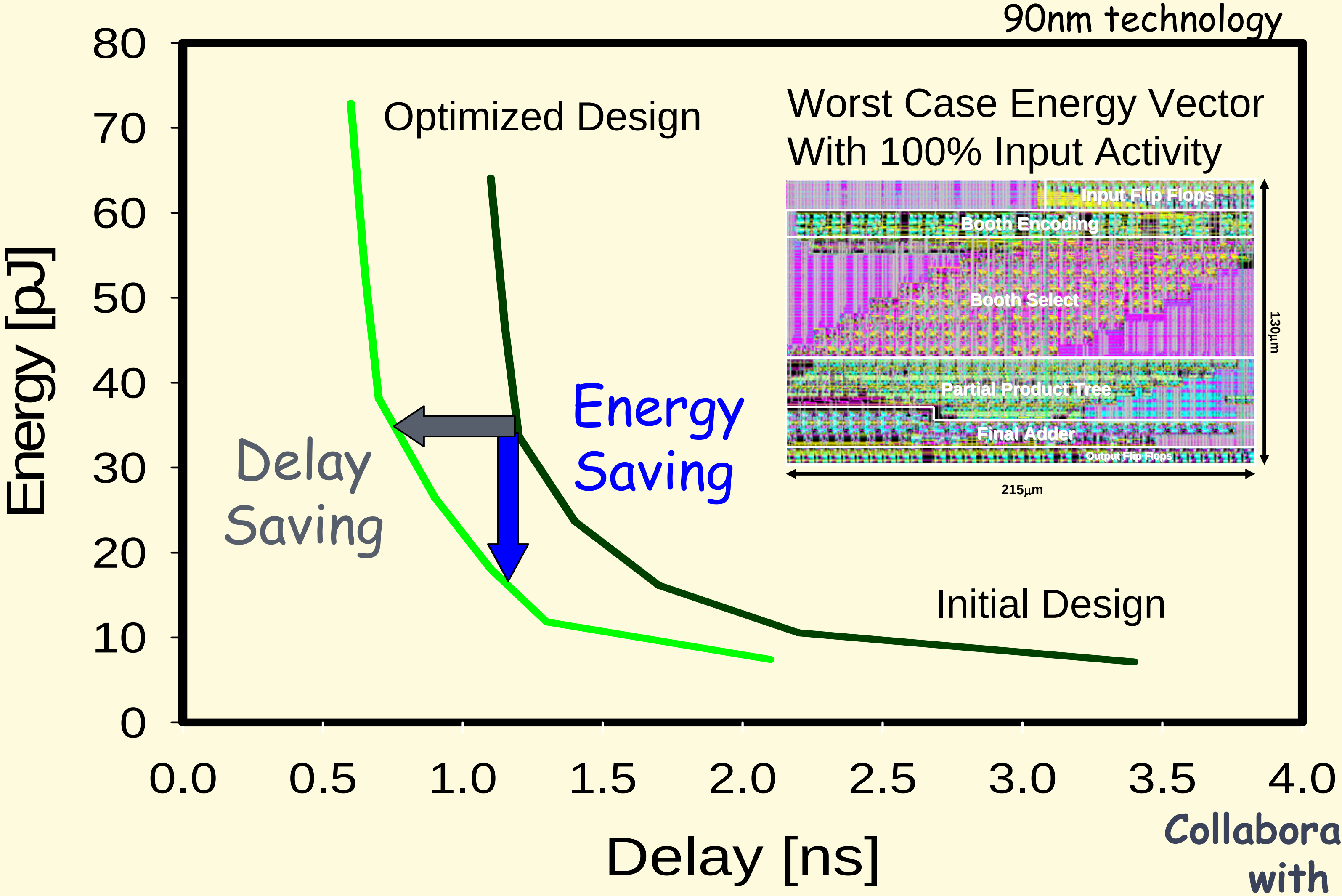


Reduces Hotspots

Energy Optimized

- Energy minimization improves hotspots!

Accomplishments
(June 30, 2003 to June 30, 2004)



Collaboration with Intel AMR

Summary

- Energy-Efficient Design requires:
  - Early structure comparison in energy-delay space
  - Early Layout/Floorplanning
  - Optimization using energy minimization objective function
- LE does not guarantee a good design
- Our method of **energy-minimization** focuses on reducing power
- The same principles hold for other logic functions

Future Work

- Methodology improvement
  - General design rules
  - Algorithms with fast convergence
  - Guidelines for close-to-optimal solutions
- CAD tool
  - Custom vs. standard cell library
- Improve gate modeling & characterization
  - Worst-case vs. single-switching,… or between?
  - Process variation

Publications on Energy-Delay:

- Vojin G. Oklobdzija, Bart R. Zeydel, Hoang Dao, Sanu Mathew, Ram Krishnamurthy, “*Energy-Delay Estimation Technique for High-Performance Microprocessor VLSI Adders*", Proceedings of the International Symposium on Computer Arithmetic, ARITH-16, Santiago de Compostela, SPAIN, June 15-18, 2003.
- Hoang Q. Dao, Bart R. Zeydel, Vojin G. Oklobdzija, “*Energy Minimization Method for Optimal Energy-Delay Extraction*", Proceedings of the European Solid-State Circuits Conference, ESSCIRC 2003, Estoril, PORTUGAL, September 16-18, 2003.
- V. G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, R. Krishnamurthy, "Comparison of High-Performance VLSI Adders in Energy-Delay Space", *IEEE Transaction on VLSI Systems*, Volume 13, Issue 6, pp. 754-758, June 2005.
- Hoang Q. Dao, Bart R. Zeydel, Victor Zyuban, and Vojin G. Oklobdzija, “On Energy Optimization of Digital Systems”, The fourth annual IBM Austin Conference on Energy-Efficient Design, ACEED 2005, Austin, Texas, March 1-3, 2005.
- H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, "Energy-Efficient Optimization of the Viterbi ACS Unit Architecture", *Proceedings of the Asian Solid-State Circuit Conference, A-SSCC 2005, Hsinchu, Taiwan, November 1-3, 2005.*
- H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, "Energy Optimization of Pipelined Digital Systems Using Circuit Sizing and Supply Scaling", *IEEE Transaction on VLSI Systems,*Vol. 14, Issue 2, Feb. 2006 pp. 122-134.
- S. K. Hsu, S. K. Mathew, M. A. Anders, B. R. Zeydel, V. G. Oklobdzija, R. K. Krishnamurthy, S. Y. Borkar, *“A 110 GOPS/W 16-bit Multiplier and Reconfigurable PLA Loop in 90-nm CMOS”*, IEEE Journal of Solid-State Circuits, Vol.41, No.1, January 2006.
- B. R. Zeydel, D. Baran, V. G. Oklobdzija, *“Energy Efficient Design of High-Performance VLSI Adders”*, IEEE Journal of Solid-State Circuits, June 2010.