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Solid State Circuits Society
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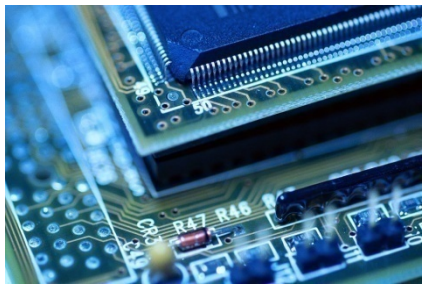
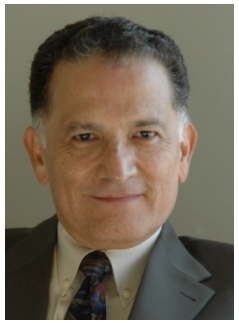


Low Drop-Out (LDO) Linear Regulators: Design Considerations and Trends for High Power-Supply Rejection (PSR)



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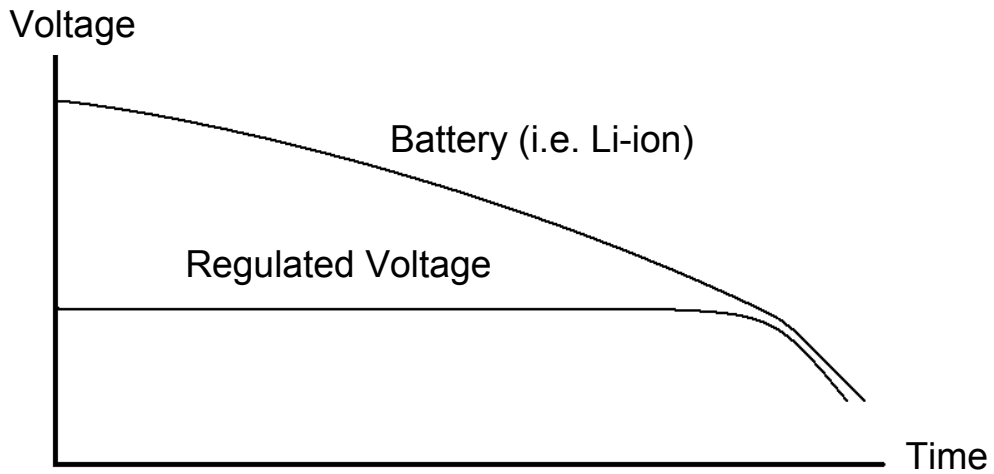
Power Management

- Why do we need power management?
  - Batteries discharge “almost” linearly with time.
  - To optimize the charging of batteries to be safe and extend their life.
  - Circuits with reduced power supply that are time dependent operate poorly. Optimal circuit performance can not be obtained.
  - Mobile applications impose saving power as much as possible. Thus, the sleep-mode and full-power mode must be carefully controlled.
  - **Objective of a power converter is to provide a regulated output voltage**



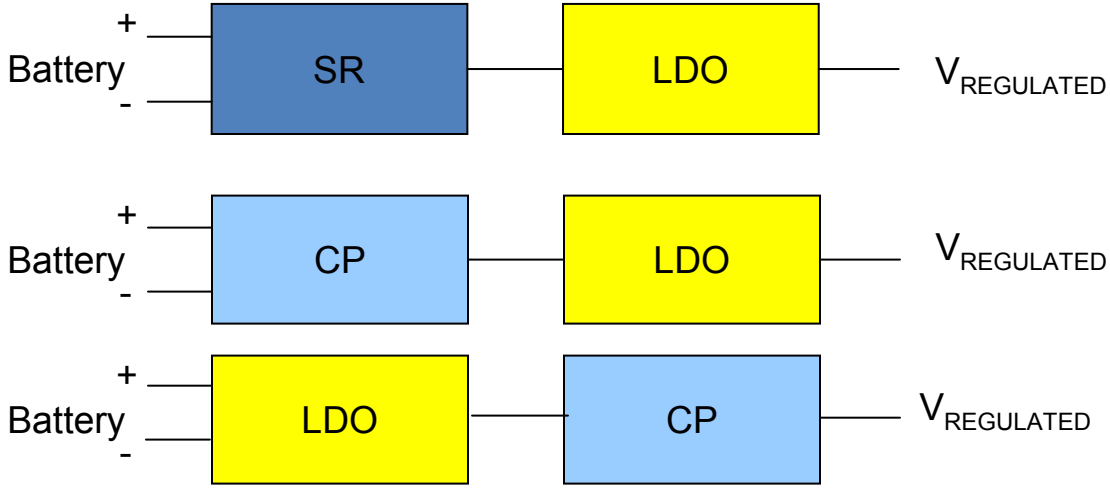
What are the conventional power converters?

- Low drop-out linear regulator (LDO)
- Switch-inductor regulator (switching regulators)
- Switch-capacitor regulator (charge pump)

Why do we need different Power Converters Types?

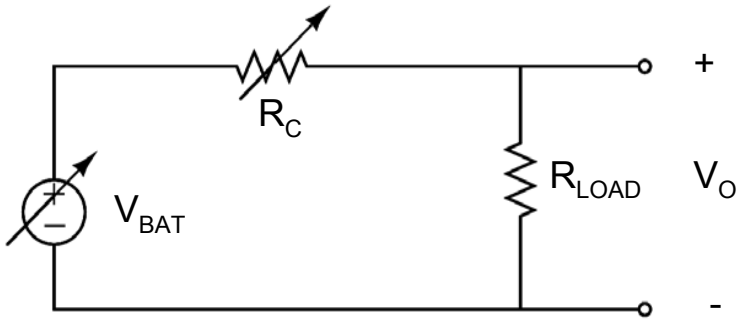
- Different applications
- Desired efficiency and output ripple

Can we combine them?



What is the purpose of combining several converters?

Linear Regulator: Basic Idea



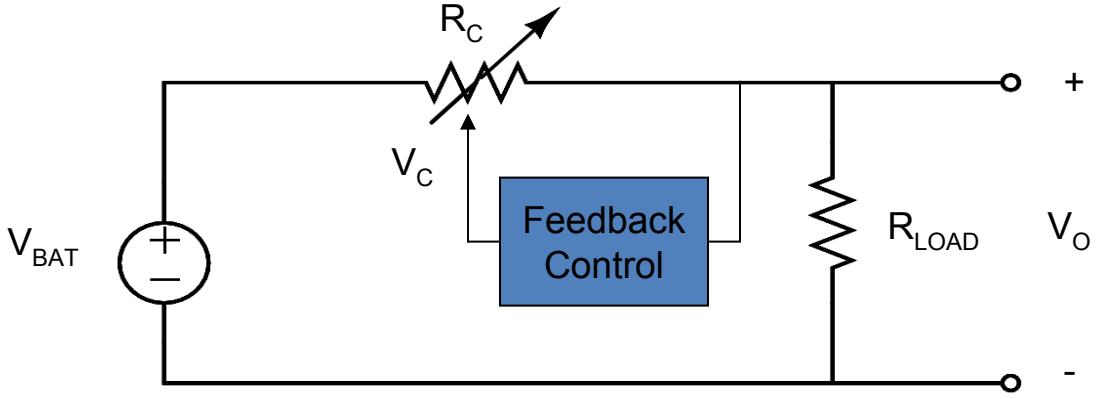
- V_o must be constant and $R_C << R_{LOAD}$
- V_{BAT} is changing as a function of time

$$V_O = \frac{R_{LOAD}}{R_{LOAD} + R_C} V_{BAT}$$

Thus in order to keep constant V_o, the value of the controlling resistor R_C yields:

$$R_C = R_{LOAD} \cdot \left(\frac{V_{BAT}}{V_O} - 1 \right) = R_{LOAD} \cdot \left(\frac{V_{BAT} - V_O}{V_O} \right) = R_{LOAD} \cdot \left(\frac{V_{LDO}}{V_O} \right)$$

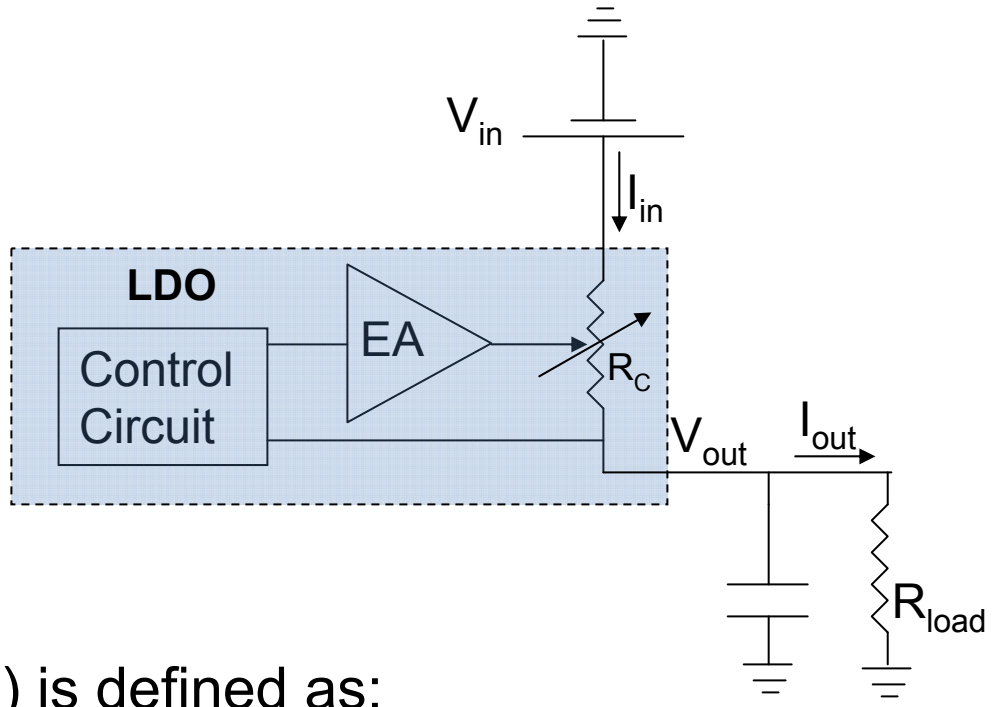
So R_C should be controlled such that $V_o = V_{desired,\ reg\text{-}voltage}$



Low Dropout Voltage Regulator (LDO)

- The LDO act as a variable resistor that is placed between input power source and the load in order to drop and control the voltage applied to the load.

- Compared to DC-DC switching regulators, LDOs are:
  - Of continuous operation
  - Easier to use
  - Cheaper solution
  - But of Lower efficiency



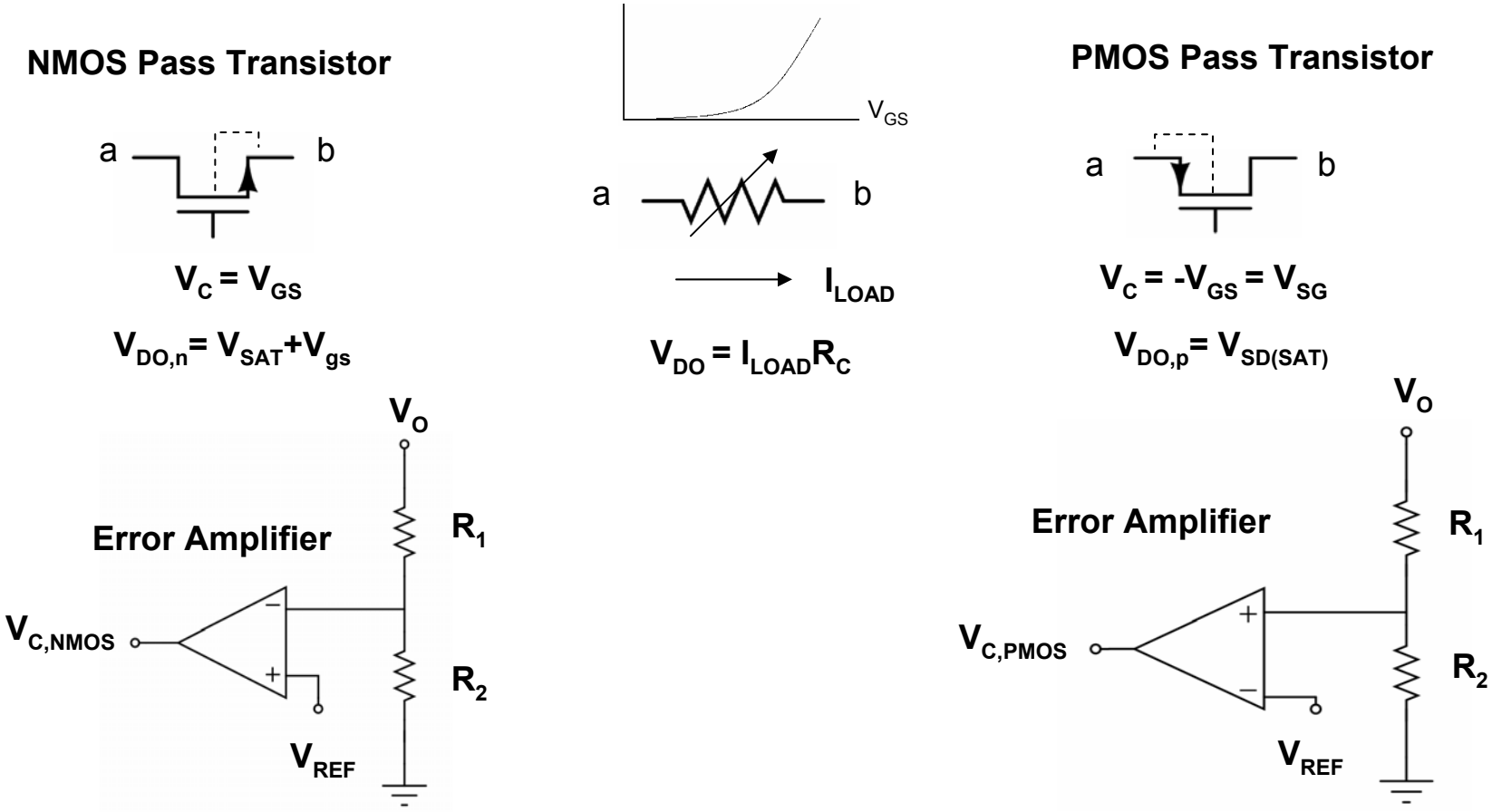
$$\eta \equiv \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{LOAD}}{V_{IN} I_{IN}} < \frac{V_{OUT}}{V_{IN}} = \frac{V_{IN} - V_{LDO}}{V_{IN}}$$

$$\rightarrow \quad \eta \approx 1 - \frac{V_{LDO}}{V_{BAT}}$$

- The output error voltage (EVO) is defined as:

$$E_{VO} \equiv \frac{R_C}{R_C + R_{LOAD}} \cdot 100\% \quad \text{OR} \quad E_{VO} = \frac{V_{OUT-MAX} - V_{OUT-LOAD}}{V_{OUT-MAX}} \cdot 100\%$$

Implementing R_C and the Feedback Control



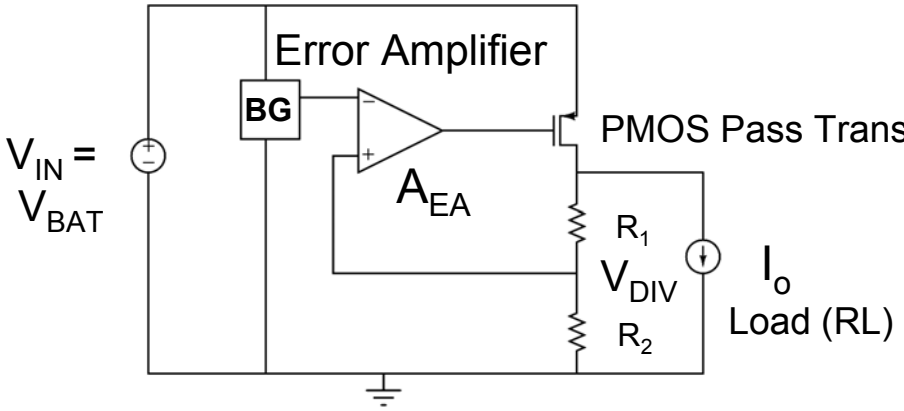
- For an ideal op amp gain, the differential input is zero, i.e.

$$V_O \frac{R_2}{R_1 + R_2} - V_{REF} \cong 0 \qquad \textbf{OR} \qquad V_{OUT} = V_{REG} = V_O = \left(1 + \frac{R_1}{R_2}\right) V_{REF}$$

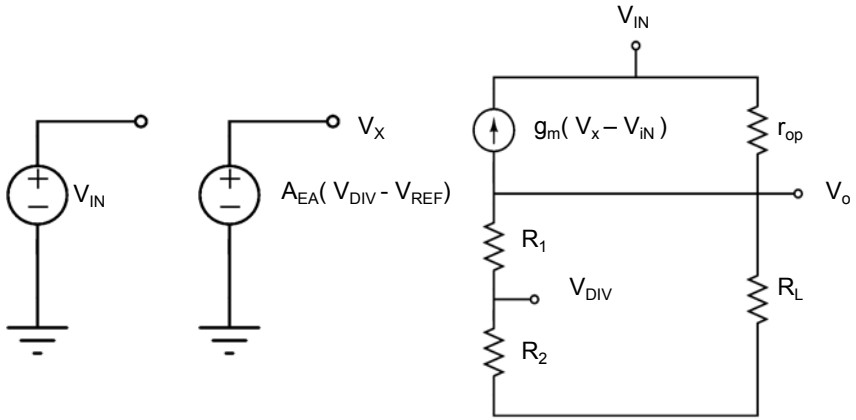
- VREF is a Bandgap voltage which is also supplied by $V_{BAT}=V_{IN}$.

LDO Analysis

- Let us analyze the basic LDO architecture. First, we will consider ideal components, then the non-idealities are introduced together with the accompanied design challenges to tackle. BG is the band gap reference voltage.



Basic LDO Topology



Small Signal Representation

$$V_O\left(\frac{1}{r_{op}}+\frac{1}{R_L}+\frac{1}{R_1}\right)-V_{IN}\left(\frac{1}{r_{op}}+g_m\right)-V_{DIV}\left(\frac{1}{R_1}+g_m A_{EA}\right)=g_m A_{EA} V_{REF} \qquad (1)$$

$$V_{DIV}\left(\frac{1}{R_1}+\frac{1}{R_2}\right)-\frac{V_O}{R_1}=0 \qquad (2)$$

Solving the (1) and (2), Vo becomes:

$$V_o = \frac{V_{in}(1+A_{PT})\beta + V_{REF}A_{PT}A_{EA}\beta}{\beta[1+\beta A_{PT}A_{EA} + \frac{r_{op}}{R_L}]}$$

Where: $A_{PT} = g_m r_{op}$, $\beta = R_2/(R_1+R_2)$, and $(R_1+R_2) >> R_L$

Thus V_o can be expressed as:

$$V_o = \frac{V_{in}A_{PT}\beta}{\beta(1+\beta A_{PT}A_{EA})} + \frac{V_{REF}A_{PT}A_{EA}\beta}{\beta(1+\beta A_{PT}A_{EA})}$$

If $T = A_{PT}A_{EA}\beta$ V_o yields: $V_o \cong \frac{V_{in}T/A_{EA}}{\beta(1+T)} + \frac{V_{REF}T}{\beta(1+T)}$

T is the open loop gain. Furthermore for T >>1

$$\boxed{V_o \cong \frac{V_{in}}{A_{EA}\beta} + \frac{V_{REF}}{\beta}}$$

Observe that *Vin* is attenuated by A_{EA} and V_{ref} is not.

Line Regulation

The line regulation is a steady-state specification. It can be defined as:

$$L_R = \frac{\Delta V_o}{\Delta V_{in}} = \frac{\beta A_{PT}}{\beta(1+\beta A_{PT} A_{EA})} = \frac{A_{PT}}{1+\beta A_{PT} A_{EA}}$$

$$\boxed{L_R = \frac{\Delta V_o}{\Delta V_{in}} \cong \frac{1}{\beta A_{EA}}}$$

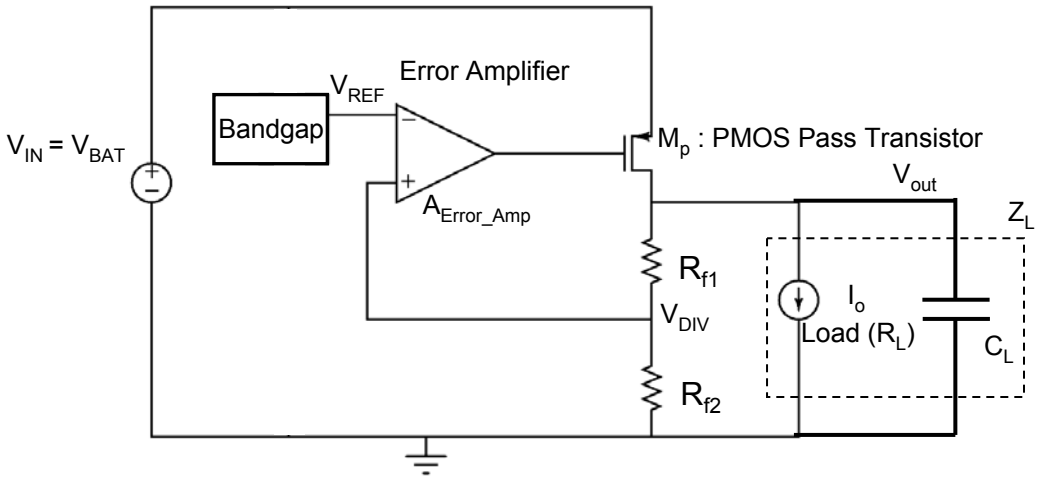
For a practical case with non-idealities such as offset Op-Amp voltage ΔV_{os} and reference voltage error i.e. ΔV_{ref} ; the line regulator becomes:

$$\frac{\Delta V_o}{\Delta V_{in}} = \frac{1}{\beta A_{EA}} + \left(1+\frac{R_1}{R_2}\right)\left(\frac{\Delta V_{REF} + \Delta V_{os}}{\Delta V_{in}}\right)$$

Observe that designers should also minimize: ΔV_{os}

and provide V_{ref} to be independent of V_{BAT} and temperature and process variations.

Issues of Concern in LDO Design



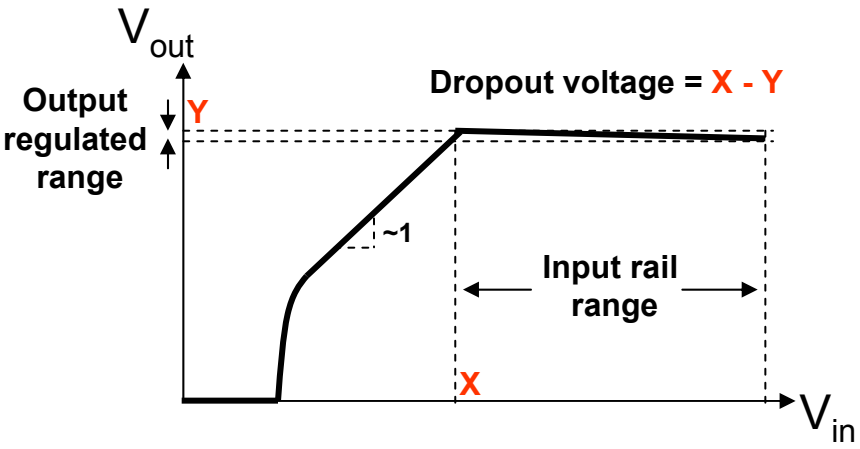
- Pass transistor
  - ➔ load current will determine its size and thus layout
- Error amplifier
  - ➔ The accuracy required by the LDO, determines the magnitude of the open loop gain.
  - ➔ Single pole architectures are recommended for better and easier stability.
  - ➔ The amp transient requirement is dependent on the stability i.e. gain and phase margins. There is a trade-off in making the PM high and speed of amp. This is also true for the Gain.
  - ➔ Should have high PSRR
- Bandgap voltage reference
  - ➔ Should have high PSR
- Stability and speed of the feedback loop
  - ➔ Should be assured under all load conditions
- Choice of the capacitors and feedback resistors (R_{f1} and R_{f2})

NMOS vs. PMOS Pass Transistor

- NMOS pass FET is easier to compensate at low loads and dropout, due to the higher output impedance of PMOS.
- NMOS pass FET are smaller due to weaker drive of PMOS.
- NMOS pass FET LDO requires the VDD rail to be higher than Vin, while a PMOS does not. To do this, a charge pump is usually required with accompanying disadvantages of higher quiescent current and extra charge pump noise.
- Power Supply Rejection (PSR) is better with PMOS

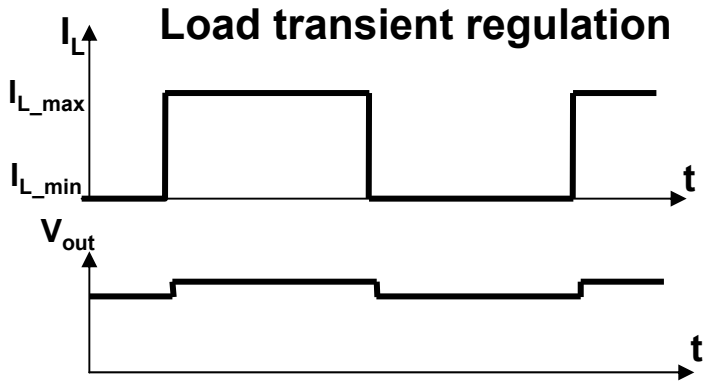
LDO Significant Parameters 1

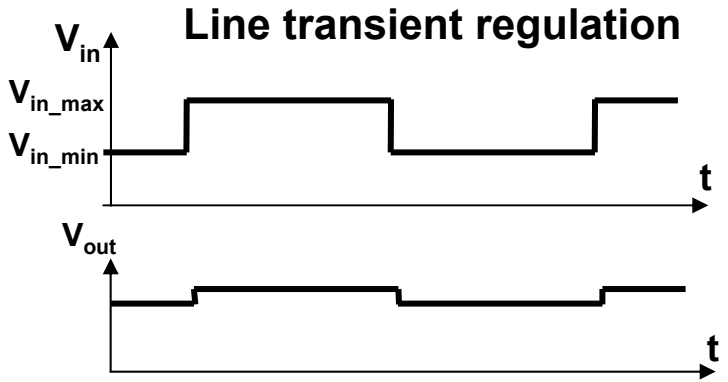
- **Dropout voltage (Vdo):** This is the difference between the minimum voltage the input DC supply can attain and the regulated output voltage.
- **Input rail range:** This is the input supply voltage range that can be regulated. Lower limit is dependent on the dropout voltage and upper limit depends on the process capability.
- **Output regulated voltage range:** This is the output voltage variation the regulator guarantees. When output voltage is in this range, it is said to be in regulation.



LDO Significant Parameters 1

- **Output current range:** This is the output current handling capability of the regulated output voltage.
  - Minimum current limit is mainly dependent on the stability requirements
  - Maximum current limit is dependent on Safe Operating Area (SOA) of pass FET and also maintaining output voltage in regulation.
- **Load regulation:** This is the variation in output voltage as current moves from min. to max.
- **Line regulation:** This is the variation in output voltage as supply voltage is varied from min. to max..
- **Load/Line transient regulation:** This is a measure of the response speed of the regulator when subjected to a fast load/Vsupply change.





LDO Significant Parameters 2

- **PSR:** Power Supply Rejection (or ripple rejection) is a measure of the ac coupling between the input supply voltage on the output voltage.

- **Power Efficiency;** This is the ratio of the output load power consumption to input supply power. Linear regulators are not really efficient especially at high input supply voltages.

- **Output capacitor range:** This is the specified output capacitance the regulator is expected to accommodate without going unstable for a given load current range.

- **Short circuit current limit:** This is the current drawn when the output voltage is short circuited to ground. The lower limit is determined by the maximum regulated load current and the upper limit is mainly determined by the SOA and specified requirements.

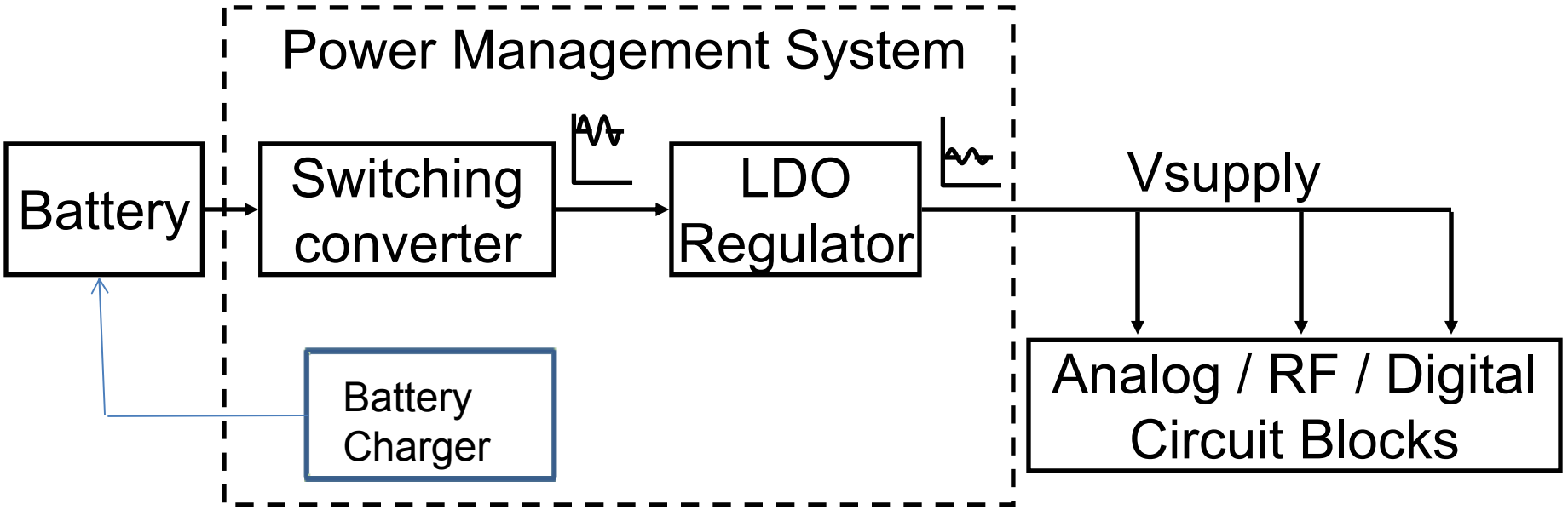
- **Overshoot;** It is important to minimized high transient voltages at start-up and during load and line transients.

High PSR using Feed-Forward Ripple Cancellation Technique

References.

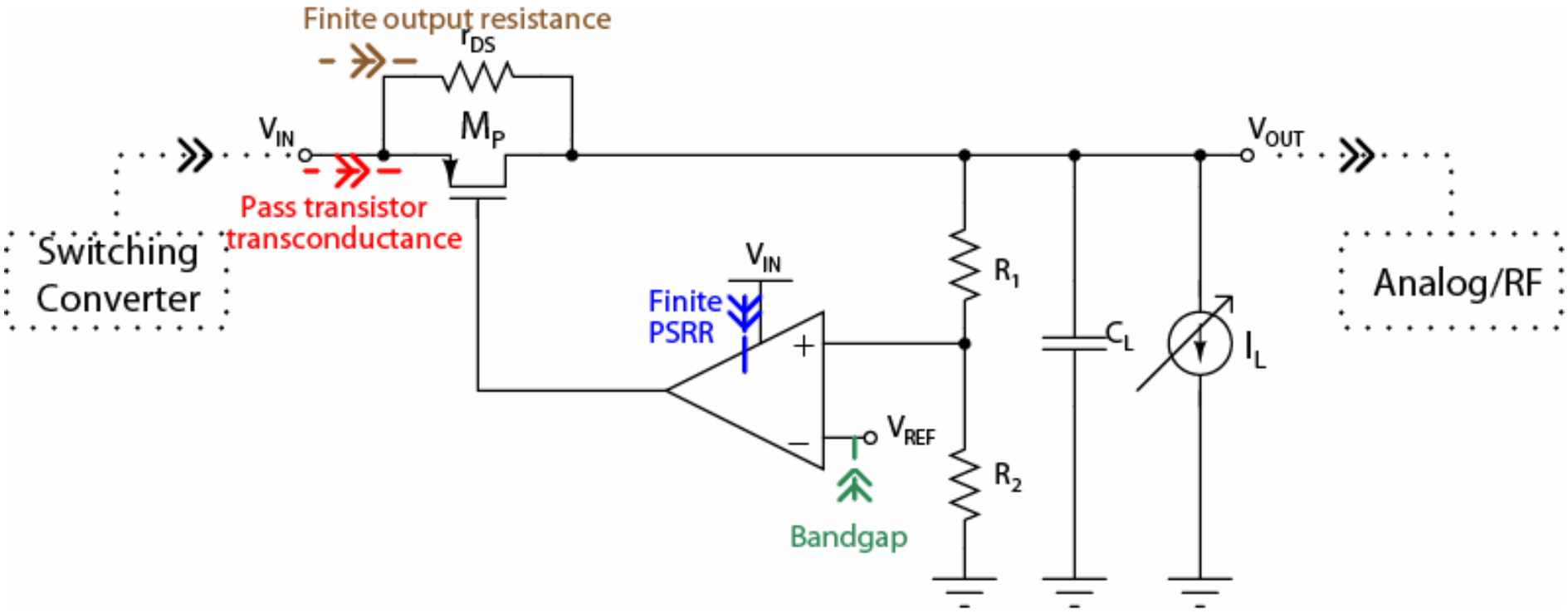
- M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sánchez-Sinencio, "A 25mA 0.13µm CMOS LDO Regulator with Power Supply Rejection better than -56dB up to 10MHz using Feed-Forward Ripple Rejection Technique," *in Proceeding of IEEE International Solid State Circuits Conference,* Feb. 2009.
- M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sánchez-Sinencio, "LDO with Feed forward Ripple Cancellation Technique for High Power Supply Rejection," *to appear in J. of Solid State Circuits*, Mar. 2010.

Motivation



- **Problem:**
  - Supply ripples affect Analog/RF blocks
  - Switching converter ripple frequencies are increasing
- **Solution:** LDO with good PSR at higher operating frequencies
- **Challenges:** Low drop-out voltage, low quiescent current, small area, high PSR across a wide frequency range

Introduction

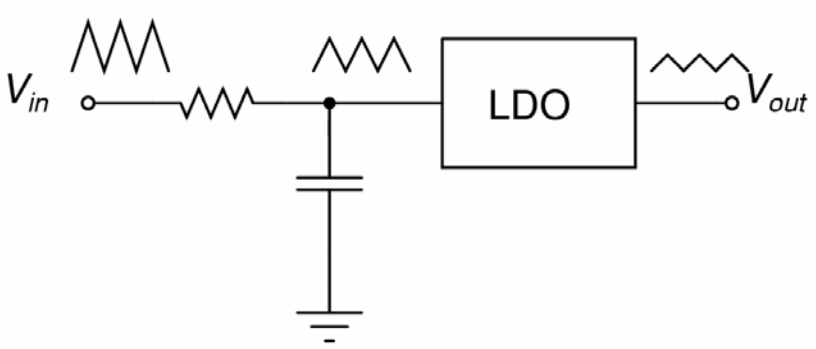


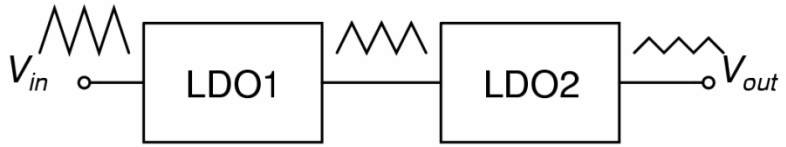
Conventional LDO

- **Input-Output Ripples Paths**
  - Low frequency: Bandgap (V_{REF}) and Error Amplifier
  - High frequency: Pass transistor and loop GBW

Prior Work

- Existing Techniques:
  - RC filtering
  - Cascading LDOs
  - Combined RC and cascading
  - Increasing Loop Bandwidth



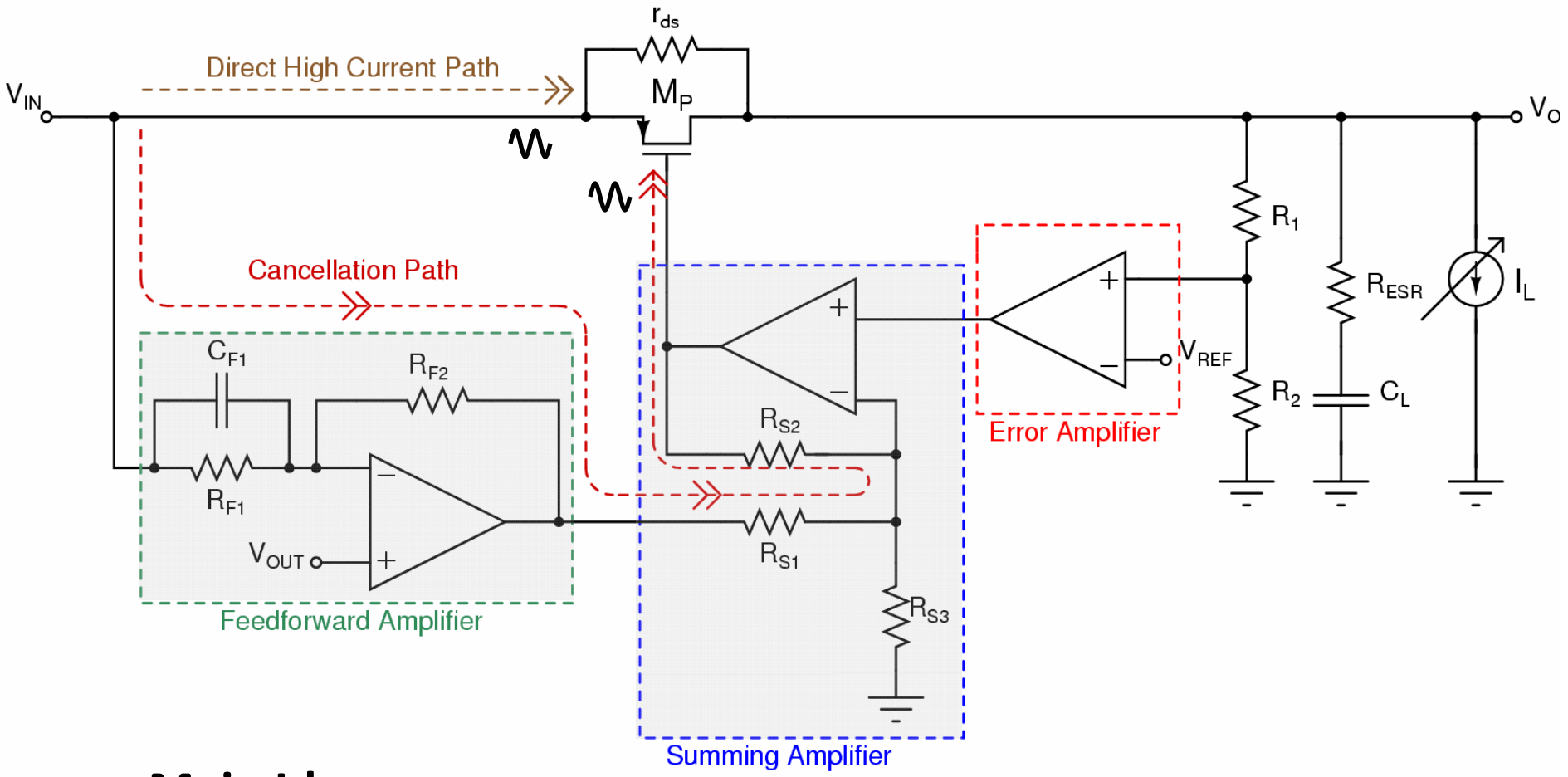


- Drawbacks:
  - Large area consumption
  - Large dropout voltage
  - High power consumption

☞ **All these techniques do not provide sufficient PSR at frequencies up to required ripple frequencies**

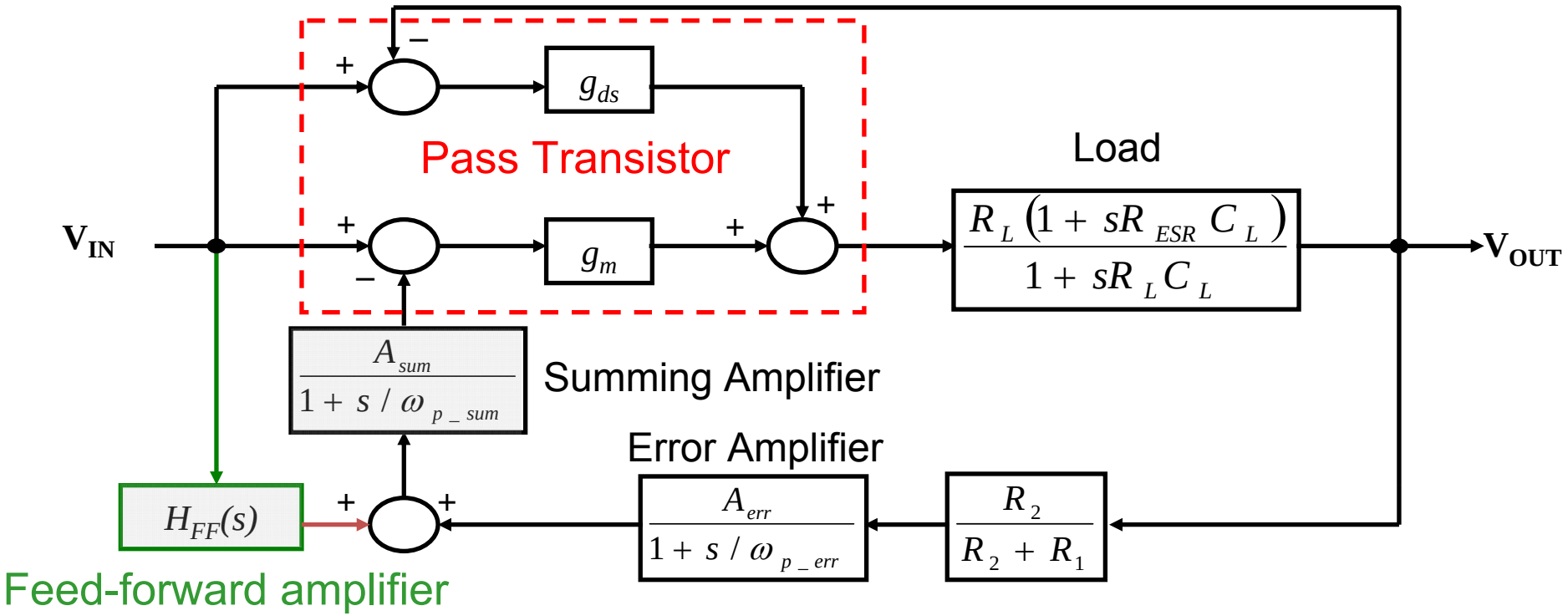
Proposed Architecture:

Feed-**F**orward **R**ipple **C**ancellation (FFRC) LDO



- **Main Idea:**
  - Cancellation path replicates the ripples at gate of pass transistor
  - Gate-source overdrive voltage is free of ripples

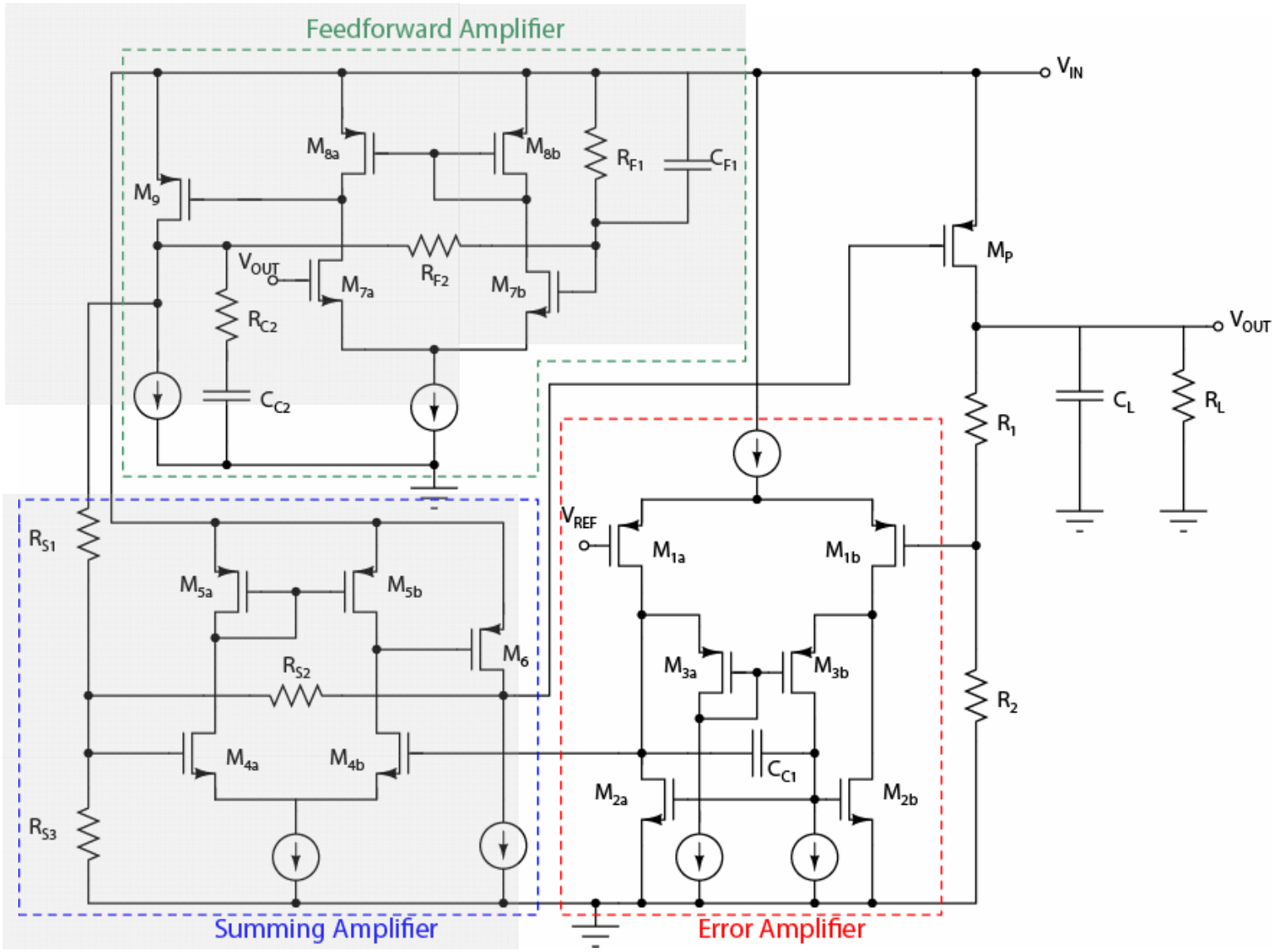
Mathematical Model of FFRC-LDO



Optimum $H_{FF}(s)$ *for a zero transfer gain:*

$$H_{FF}(s)\cdot\frac{A_{sum}}{1+s/\omega_{p\_sum}}\cdot\frac{g_m}{g_m+g_{ds}}=1$$

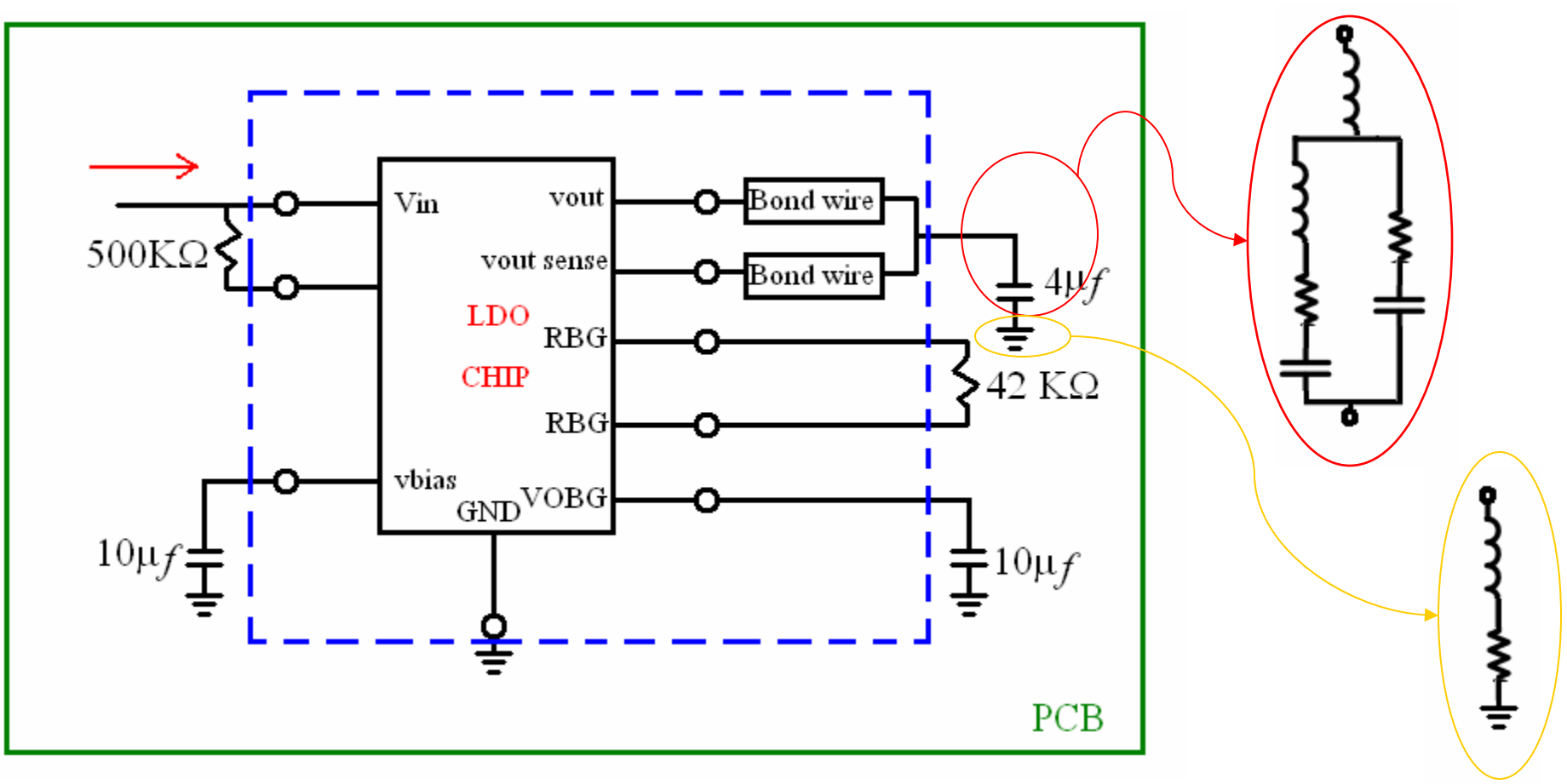
Circuit Implementation



Main Features

- **High Power Supply Rejection**
- **Low Drop-out Voltage:** same as conventional LDOs
- **Loop Dynamics:** same as conventional LDOs
- **Error Amplifier:** specifications are relaxed compared to conventional LDOs
- **Low power consumption**
- **Low sensitivity to process Variation:** ratio of resistors

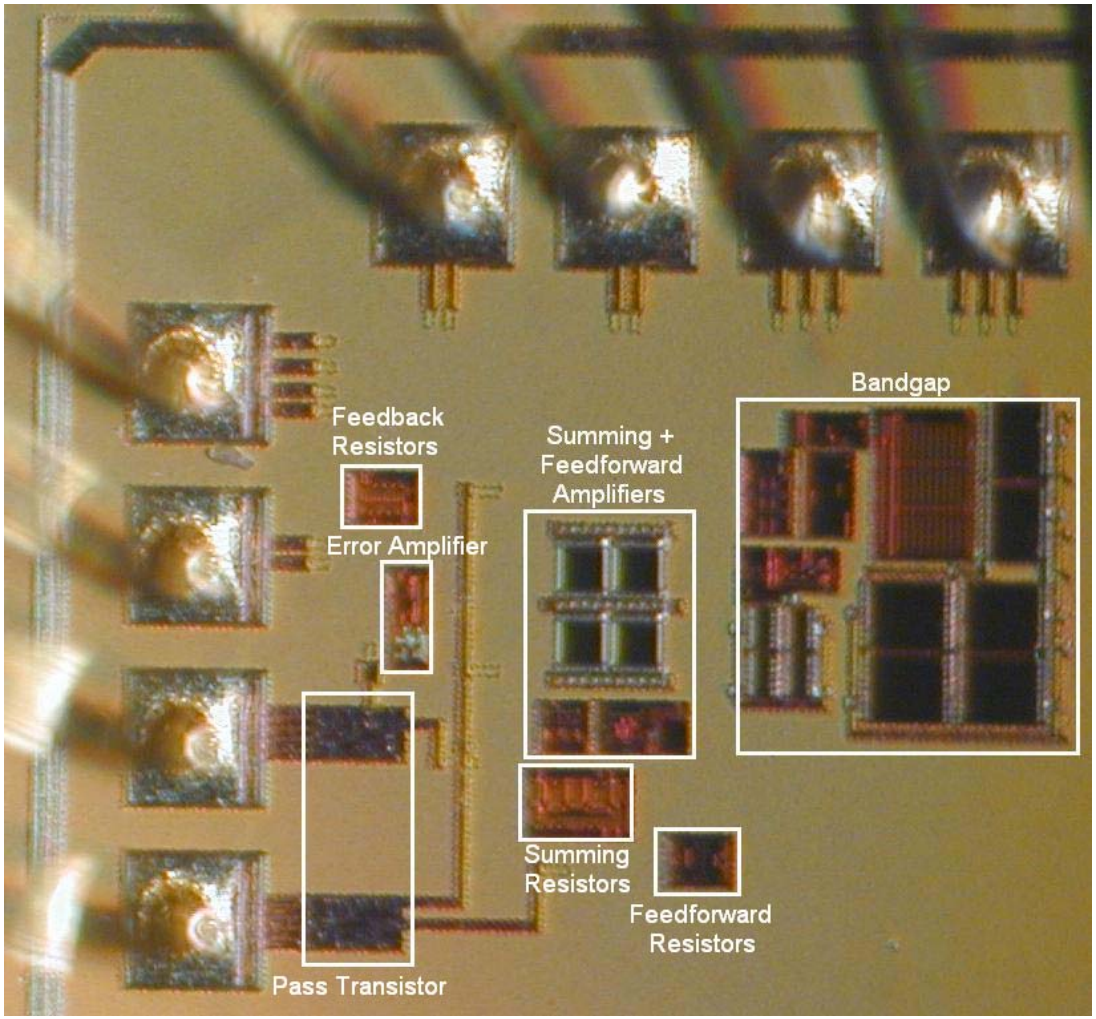
PCB View of the LDO



→Capacitor ESL and the trace inductance limit the performance at higher frequencies

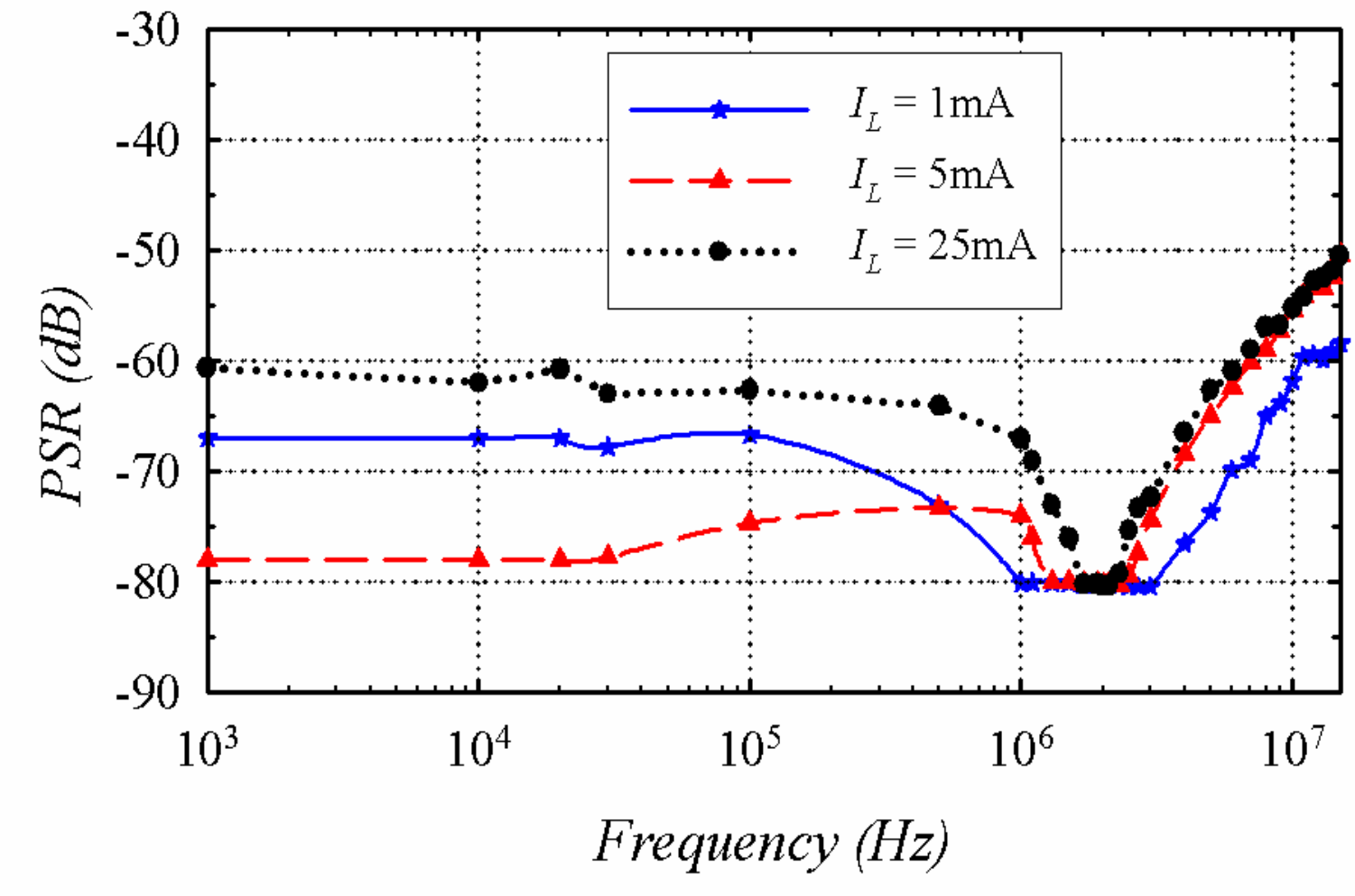
→The traces and the bonding wires should be modeled during the simulations

Chip Die-Photo



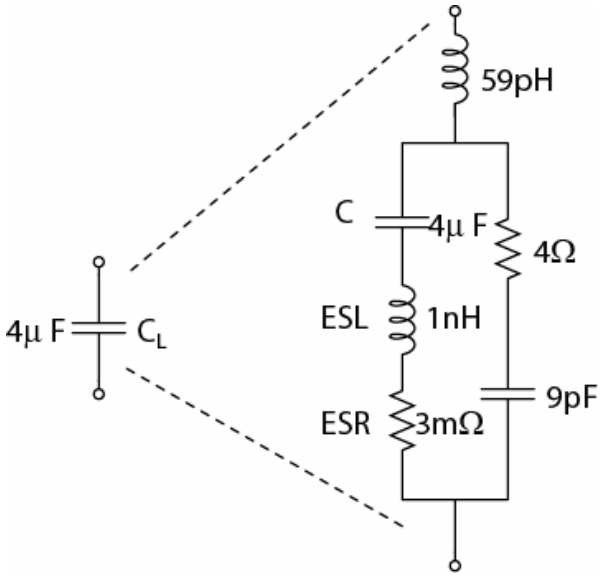
Technology: UMC 0.13µm CMOS

PSR Measurement Results



PSR Degradation

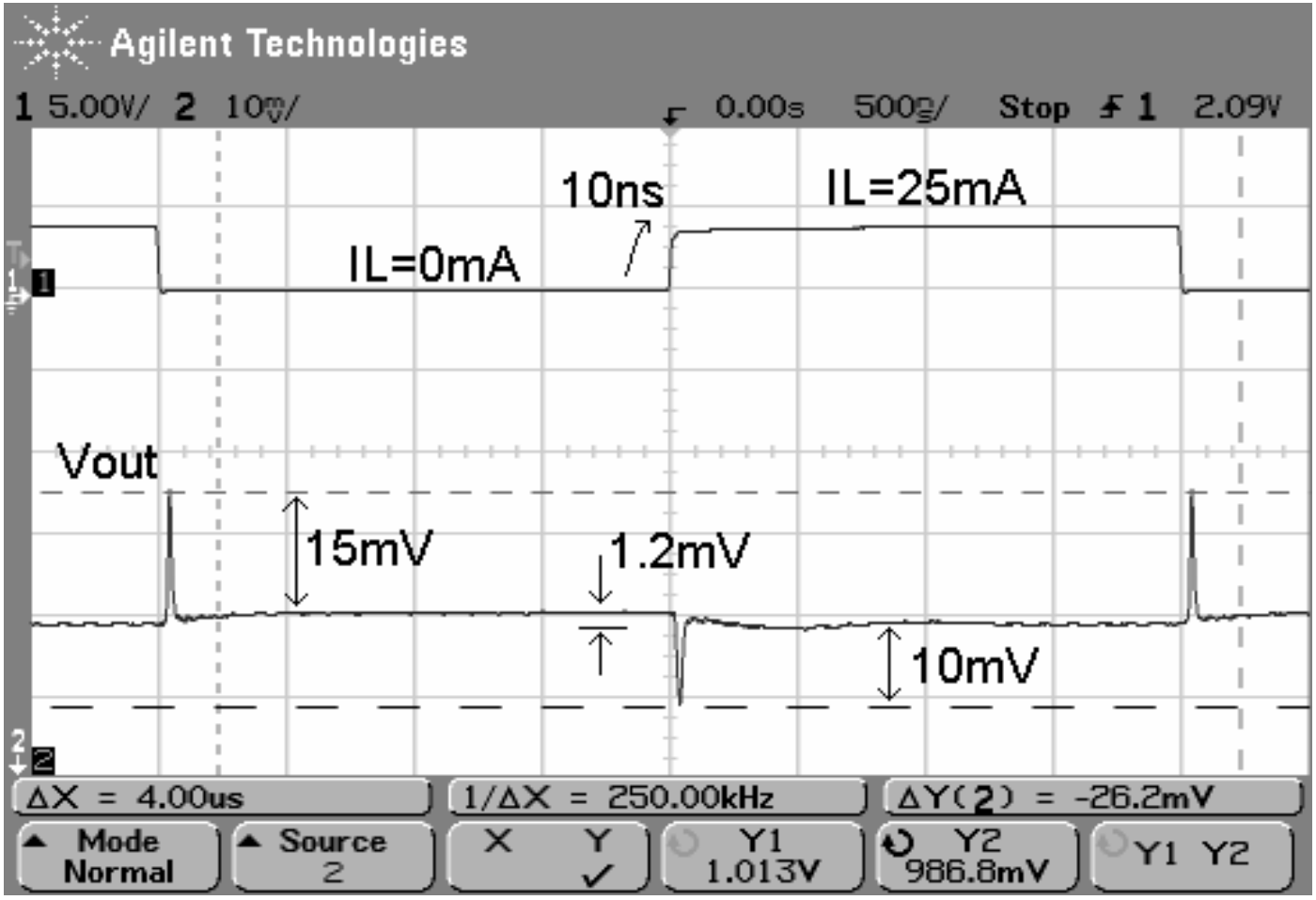
- PSR degrades at higher frequencies due to:
  - Finite GBW of feed-forward amplifier (cancellation path)
  - Finite closed loop bandwidth
  - Finite self inductance (ESL) of off-chip capacitor



Transient Response

ILoad

Vout



Performance Summary

	ISSCC 07	ISSCC 08	This work
Technology (CMOS)	0.6	0.35	0.13
Active Area (mm^2)	N.A.	0.053*	0.049*
V_{in} (V)	> 1.8	> 1.05	> 1.15
V_{out} (V)	1.2	0.9	1
Dropout Voltage (mV)	> 0.6	> 0.15	> 0.15
Maximum Load (mA)	5	50	25
I_Q (μA)	70**	80@25mA* 160@50mA*	50***
PSR (dB)	-40@1MHz -27@10MHz	-50@1MHz N.A.@10MHz	-67@1MHz -56@10MHz
Load Regulation (mV/mA)	34.2	0.0614	0.048
$\Delta V_{out}/V_{out}$ (mV/V)	766/1.2	6.6/0.9	26/1

* Without the bandgap circuit, ** Error amplifier and voltage reference only

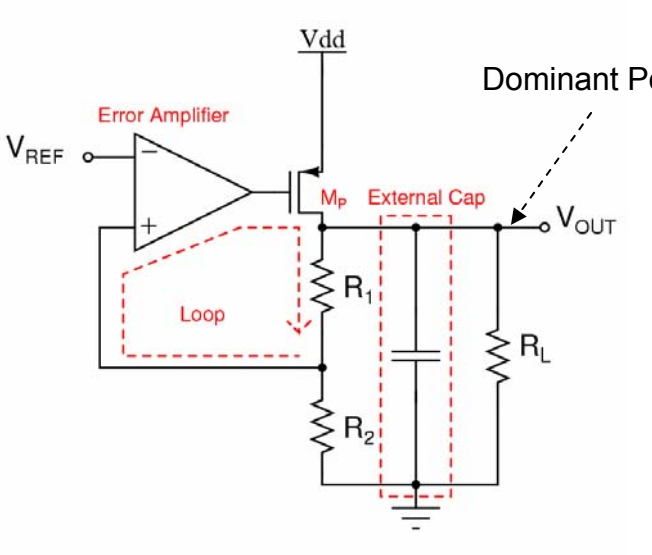
*** Overall quiescent current, including amplifiers and voltage reference

Capacitor-Less Low Drop-Out Voltage Regulators

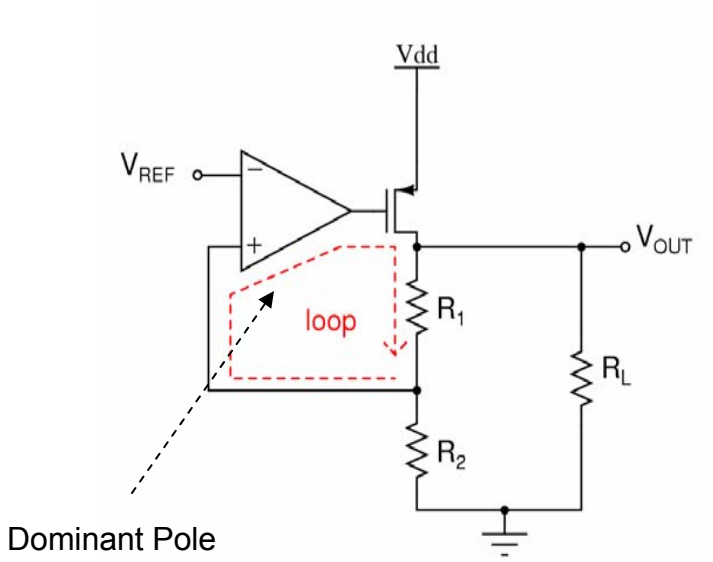
A Comparative Study

Introduction

- Conventional LDOs are typically implemented with at least one feedback loop which is stabilized using a huge external capacitor
- Present research in LDOs is focused on removing this external capacitor while maintaining stability, good transient response and high power supply rejection performance



Conventional LDO



Capacitor-Less LDO

Design Considerations in Capacitorless LDOs

- Stability (light loads)
- Load Transient Response
- Power Supply Rejection

Case 1: Stability of Two Gain Stages

- Consider that poles are located at the output of error amplifier (EA) and the output of LDO
- EA pole is the dominant pole, thus the output pole need to be placed beyond unity gain frequency (UGF) to achieve stability
- Note that poles are function of load current (I_L)

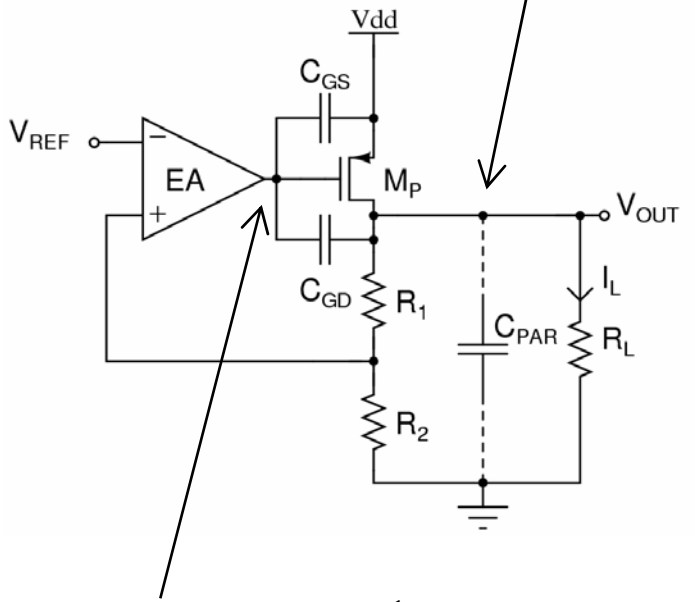
$$\omega_{EA} \propto \sqrt{I_L}$$

$$\omega_{OUT} \propto I_L$$

$$\omega_{OUT} >> \omega_{EA} \quad \text{For Capacitorless}$$

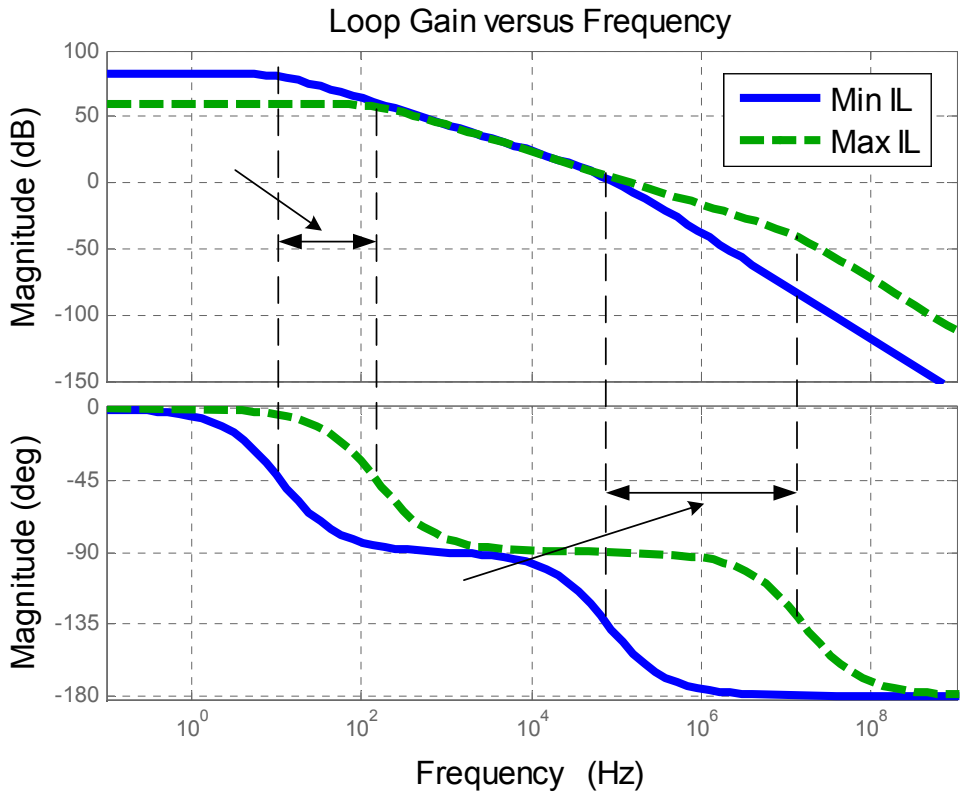
$$\omega_{OUT} << \omega_{EA} \quad \text{For External } (C_L) \text{ Capacitor}$$

$$\omega_{OUT} = \frac{1}{C_{PAR}(R_{ds} \parallel (R_1 + R_2) \parallel R_L)}$$



$$\omega_{EA} = \frac{1}{R_{O,EA}\left(C_{GS} + (1 + g_{m,MP}(R_{ds} \parallel (R_1 + R_2) \parallel R_L))C_{GD}\right)}$$

Poles Movement (ω_{EA} & ω_{OUT})



- Phase margin at light loads (Min I_L) is reduced.
- Observe that output pole frequency reduces at a much faster rate than the EA pole frequency with reducing load current.
- Stability is a concern for light load conditions.

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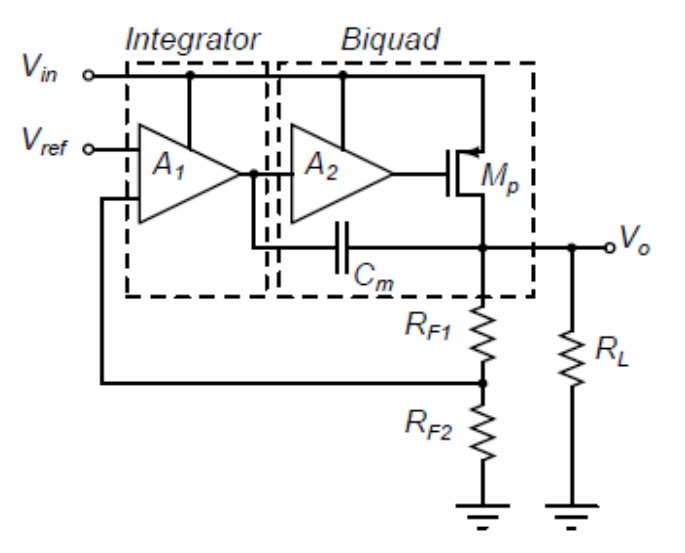
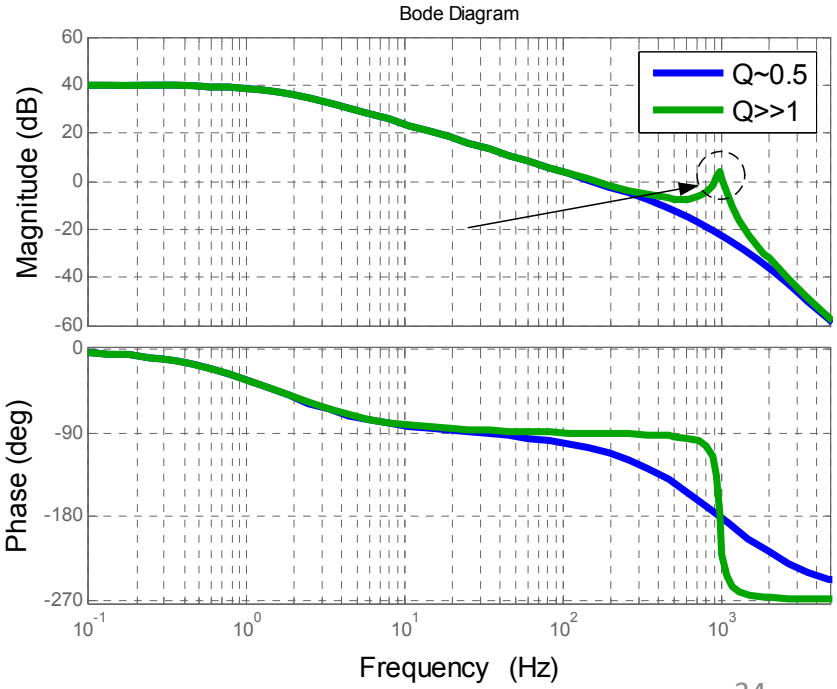
Case 2: Stability of Three Gain Stages



$$\frac{V_{out}}{V_{in}} = \frac{A_{dc}}{(1+s/\omega_{\text{int}})(s^2/\omega_o^2 + s/(\omega_o Q)+1)}$$

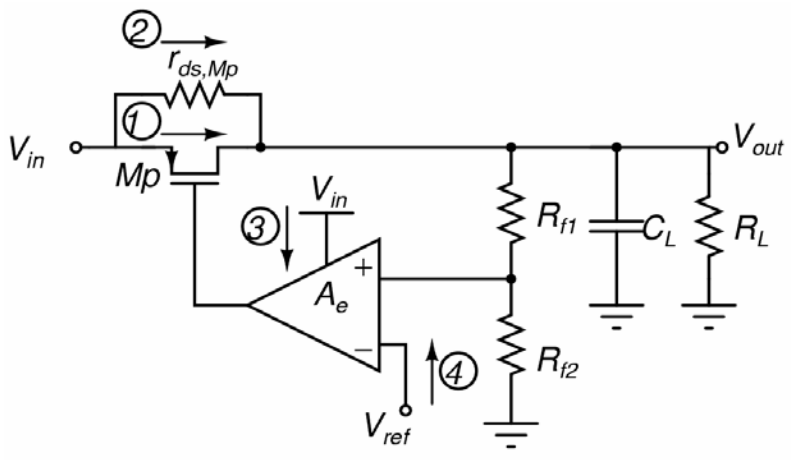
- LDOs with three stages can be seen as a cascade of a first and second-order filters
- Dominant pole is formed by integrator whereas non-dominant poles arise from the biquad

- At light loads (large R_L), the non-dominant poles become complex and peaking occurs in the magnitude response due to the high Q of the biquad. If this peaking crosses the 0-dB axis the LDO loop becomes unstable



LDO Power Supply Rejection [El-Nozahi10]

- Supply noise is propagated to the output through multiple paths that are shown in the adjacent figure



- **$g_{m,Mp}$: transconductance of pass transistor**
- **$r_{ds,Mp}$: channel resistance o pass transistor**
- **Z_L : total load impedance (w/o R_{f1} &R_{f2})**
- **A_{eo} : DC gain of error amplifier**
- **ω_e : dominant pole of error amplifier**

$$\frac{V_{out}}{V_{in}}(s)\Big|_{1,2} = \frac{1+g_{m,MP}r_{ds,MP}}{1+\frac{r_{ds,MP}}{Z_L(s)}+\frac{r_{ds,MP}}{R_{f1}+R_{f2}}+\frac{g_{m.MP}r_{ds,MP}A_{eo}R_{f2}}{(1+s/\omega_e)(R_{f1}+R_{f1})}}$$

(PSR due to paths 1 & 2)

- From the equation it is observed that PSR largely depends on the feedback gain $\frac{A_{eo}}{(1+s/\omega_e)}\frac{R_{f2}}{R_{f1}+R_{f2}}$
- At low frequency, the feedback gain is large and consequently low frequency supply rejection is good. However, beyond the frequency of the error amplifier pole feedback gain reduces and supply noise rejection degrades likewise.
- ω_e is low frequency (10s of Hz) in capacitor-less LDOs implying that high frequency ripple rejection is very bad.

Capacitor-less LDO Topologies

Capacitor-less LDOs can be roughly divided into two main groups based on the number of active loops.

- Single Loop LDOs
  - Have at least three gain stages to increase the loop gain

- Multiple Active Loop LDOs
  - Have two or more loops to enhance slew rate at the gate of the pass transistor

Next we discuss first single loop LDOs!

Miller Compensation Architecture [Leung03]

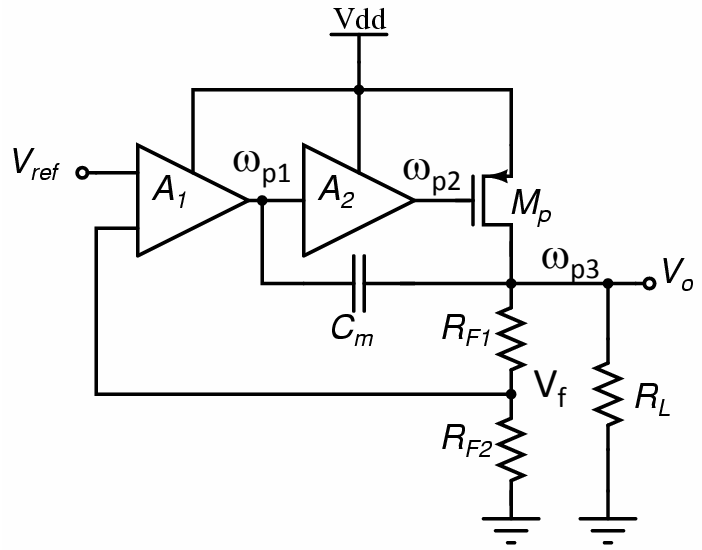
(A single loop LDO architecture)

Main Features:

- Basic architecture to provide regulation

Principle of Operation:

- Amplifier A_1 is used to provide the necessary regulation
- Amplifier A_2 servers for:
  - Providing the necessary current to drive the pass transistor
  - Amplifying the miller capacitance (C_m) form the dominate pole at the output of A_1
- Dominate pole is determined through the miller capacitor

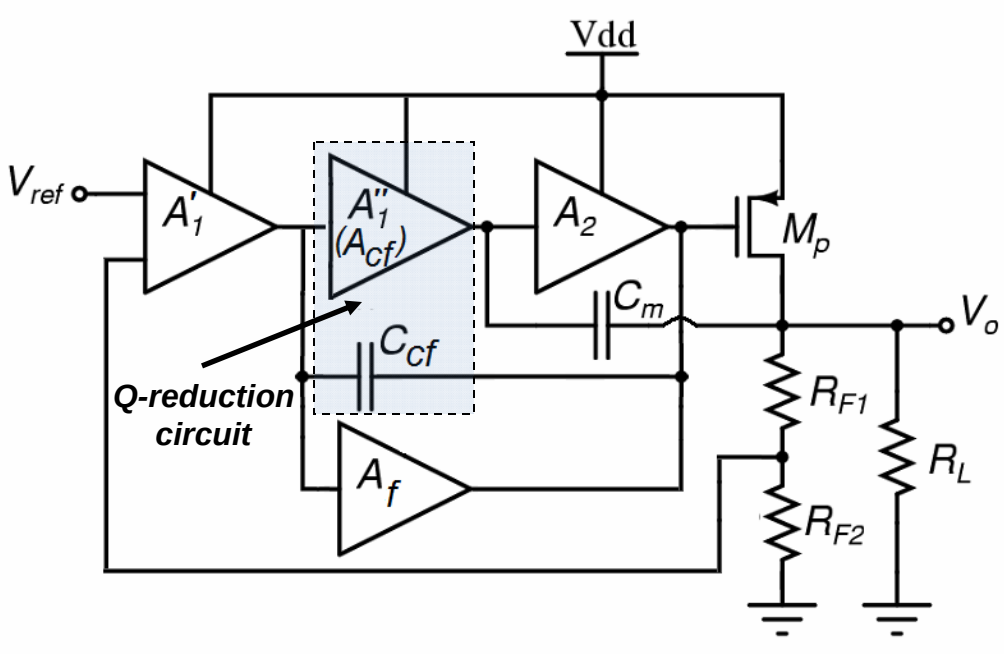


$\omega_{p1} << \omega_{p2}, \omega_{p3}$

Q-Reduction Architecture [Lau07]

Main Features:

- This topology focuses on minimizing the on-chip capacitance and minimum output-current requirement down to 100μA through controlling the non-dominant complex poles.



Principle of Operation:

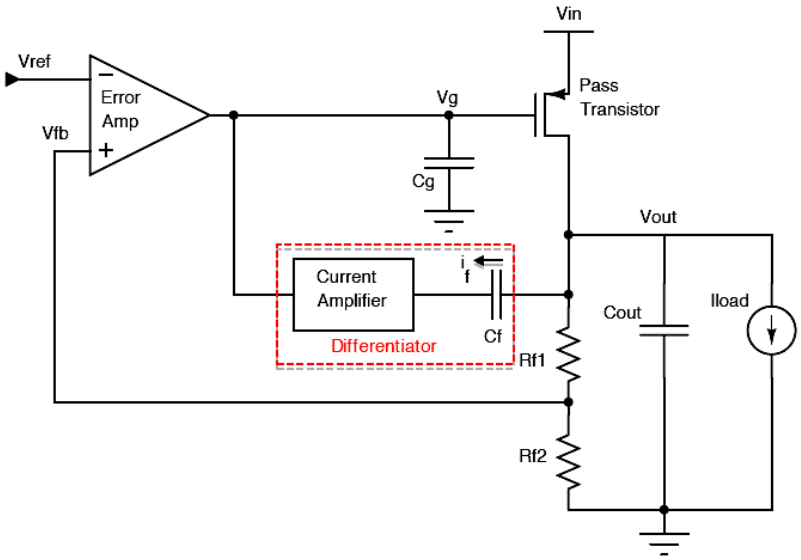
- The Q-reduction circuit is formed by C_{cf} and a current buffer A_{cf} of transconductance g_{mcf}, *where Q is decreased by a larger* C_{cf} *and a smaller* g_{mcf}.
- A feed-forward transconductance stage A_{cf} is used to generate a LHP zero to improve LDO stability and slewing at the PFET gate.

Multiple Loop Architectures

Differentiator Architecture [Milliken07]

Main Features:

- This topology enhances the load transient response by reducing the undershoots and overshoots
- The on-chip Miller Capacitor is reduced a lot because of the amplifier in the Differentiator path and thus saving area without sacrificing chip area



Principle of Operation:

- The capacitance C_f reacts to the changes in output voltages happening for load current transients by generating a equivalent transient current .
- The auxiliary loop includes a current amplifier which amplifies current and injects it into the pass transistor's gate capacitance.
- At the same time, splitting occurs because of the Miller Effect making the Error Amplifier's output to be the dominant pole.

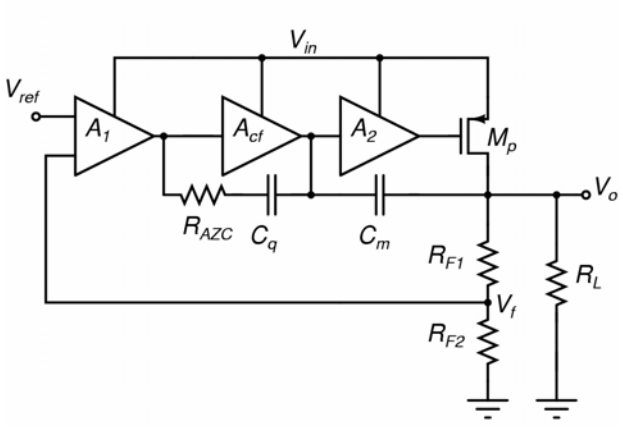
Minimized-Q & Adaptive Zero Compensation (MQ&AZC) [H.C. Yang08]

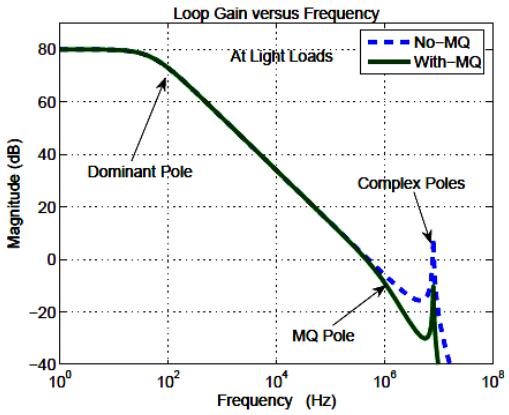
Main Features:

- This topology has the advantage of being stable at very light loads (50μA)
- Phase margin of 60° is maintained over the entire range of load currents thus enhancing the transient performance of this LDO

Principle of Operation:

- A non-dominant pole Is introduced between the UGF of the loop and the complex poles generated by the biquad
- Thus, the loop gain is attenuated at the complex pole frequency and as result the LDO can tolerate higher Q or peaking





- A phase margin of ≅60° is maintained over the entire current load range by combining the MQ pole with an adaptive zero.

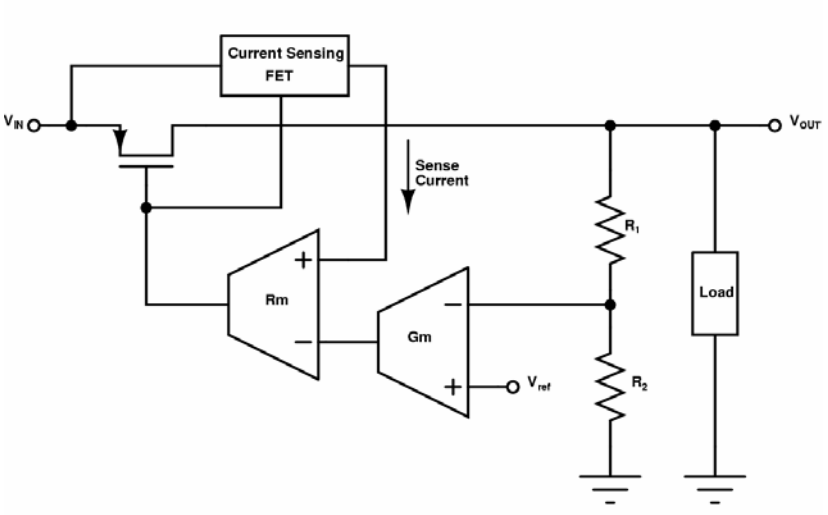
Transimpedance LDO [J.J. Chen07]

Main Features:

- This topology has the advantage of very fast response to load & line transients

Principle of Operation:

- Current variation at the output is detected by a sense FET which generates a current proportional to the load current
- Sense current is fed back through a transimpedance stage to the gate of the pass transistor
- Slew rate of error amplifier is boosted by this additional feedback current



- The secondary loop (through the transimpedance) has a much smaller response time than the main voltage LDO loop

Common Design Specifications For Comparison Study

- All the previously discussed capacitor-less LDO architectures have been designed using different technology processes or with different design specifications.

- As a result, it is very difficult to compare them

- To fairly compare them the following common design specifications are used:

Parameter	Specification
V_{ref}	1.4V
V_{in}	3.0V
V_{out}	2.8V
Pass Transistor Dimensions	M=2000, W=18µm and L=0.6µm
GBW (open loop)	500KHz
R_{F1}/R_{F2}	100KΩ/100KΩ
Technology	ON Semi 0.5µm

Experimental Results

Technology: 0.5μm ON Semi CMOS

Performance Summary

Topologies	Load Transient ΔV_{out} (V)*	Load Transient Settling (μs)	Load Range (mA)	Line Transient (mV)	Quiescent Current (μA)	PSR (dB)	Load Regulation (mV/mA)	Line Regulation (mV/V)	Total Compensation Capacitance (pF)
Miller [Leung03]	1.026/0.168	1.20/3.09	0.10-50	144/271	**63 @ 100μA 60 @ 50 mA**	**-52@ 1 kHz -50@ 10 kHz -27@ 100 kHz**	**0.160**	0.018	8
Q-Reduction [Lau07]	1.134/0.325	4.23/1.54	0.10-50	264/241	**64@ 100μA 60 @ 50mA**	-63@ 1 kHz -45@ 10 kHz -20@ 100 kHz	0.721	** **0.000**	7
MQ & AZC [H.C. Yang08]	1.207/0.345	1.73/1.56	0.05-50	**76/93**	80 @ 100μA 100 @ 50 mA	-48@ 1 kHz -47@ 10 kHz -26@ 100 kHz	0.842	0.002	2.8
Differentiator [Milliken07]	1.207/0.281	**0.8/1.34**	**0.00-50**	428/209	78 @ 100μA 80 @ 50 mA	-53@ 1 kHz -36@ 10 kHz -16 @ 100 kHz	0.902	0.003	**1.2**
Trans-impedance [J.J. Chen07]	**0.962/0.289**	1.04/3.56	0.10-50	419/496	46@ 100μA 170 @ 50 mA	-46@ 1 kHz -26@ 10 kHz -7@ 100 kHz	0.862	** **0.000**	2.7

*PSR results are for I_L = 50mA

**Value extremely low to be measured

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