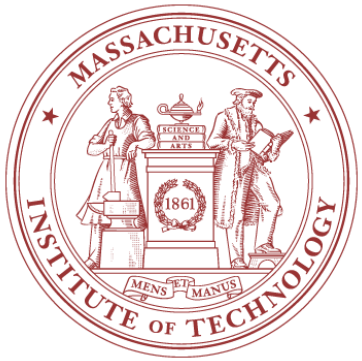
Integrated Circuit Design with Nano-Electro-Mechanical Switches

Elad Alon[1], Tsu-Jae King Liu[1], Vladimir Stojanovic[2], Dejan Markovic[3]

[1]University of California, Berkeley

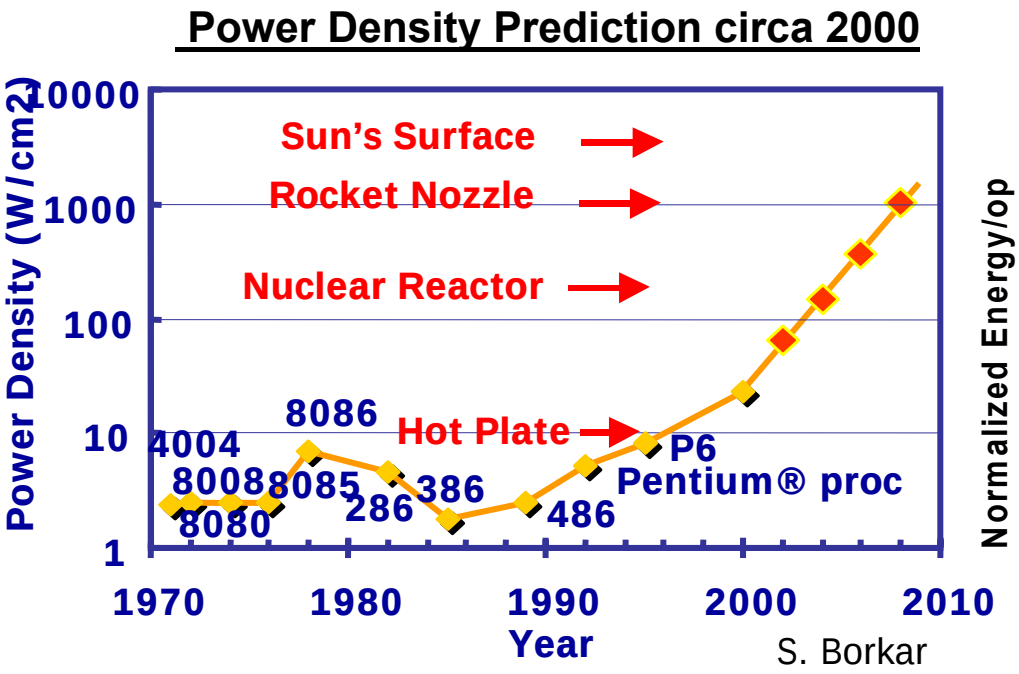
[2]Massachusetts Institute of Technology

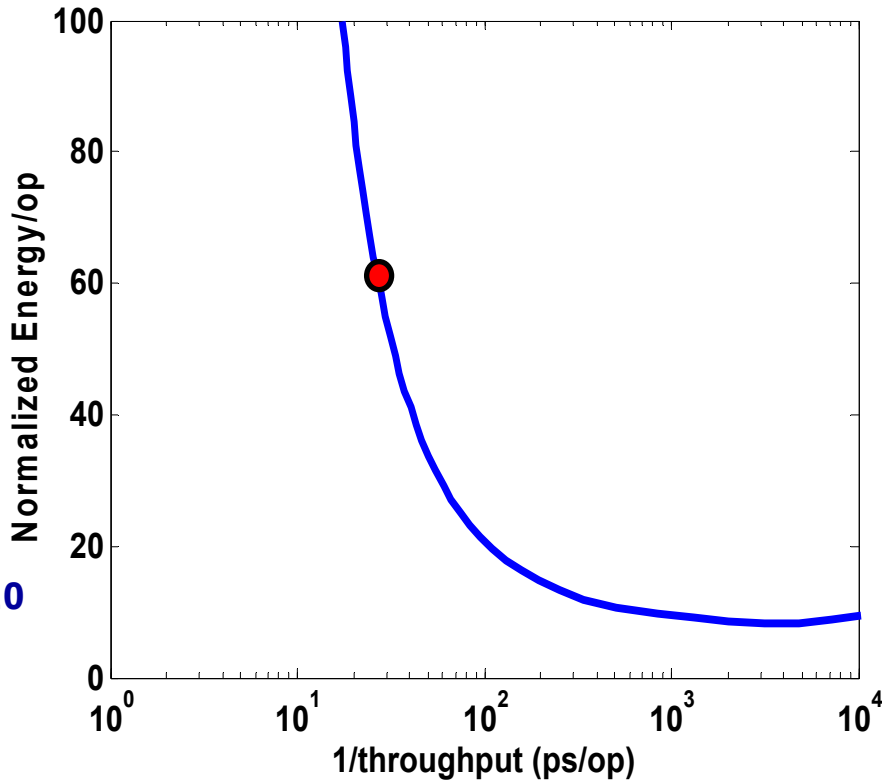
[3]University of California, Los Angeles



UCLA

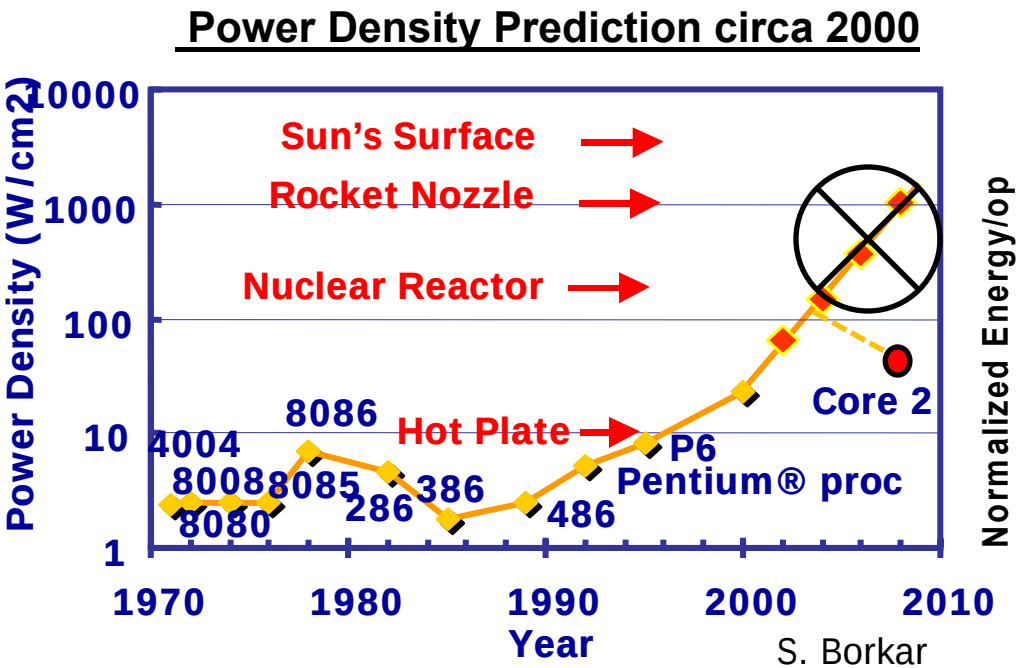
CMOS is Scaling, Power Density is Not

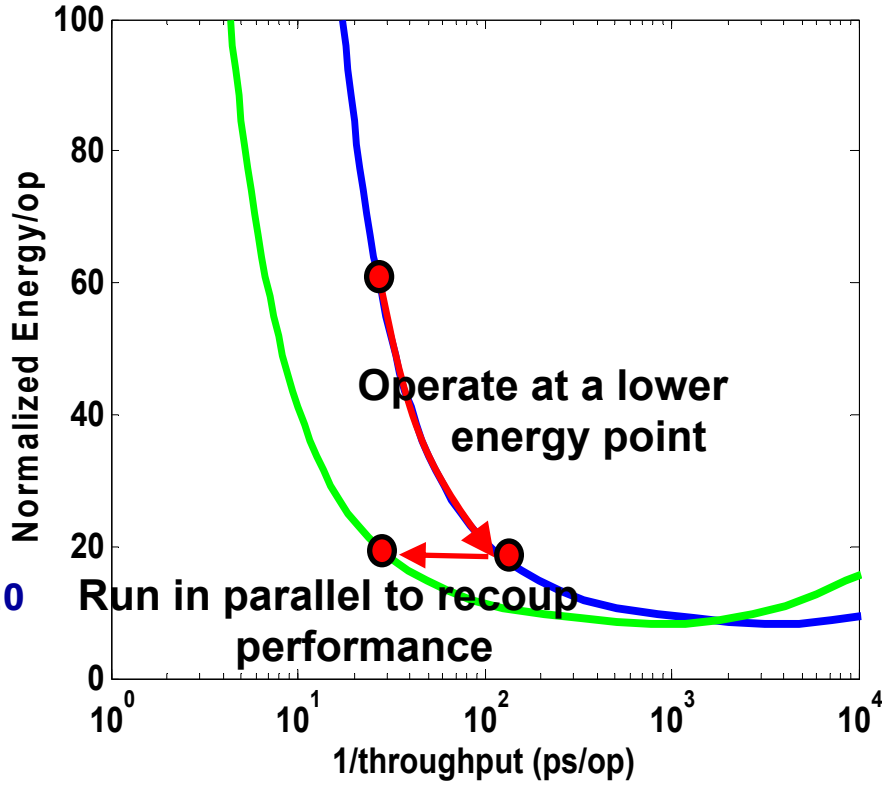




- V_{dd} and V_t not scaling well → power/area not scaling

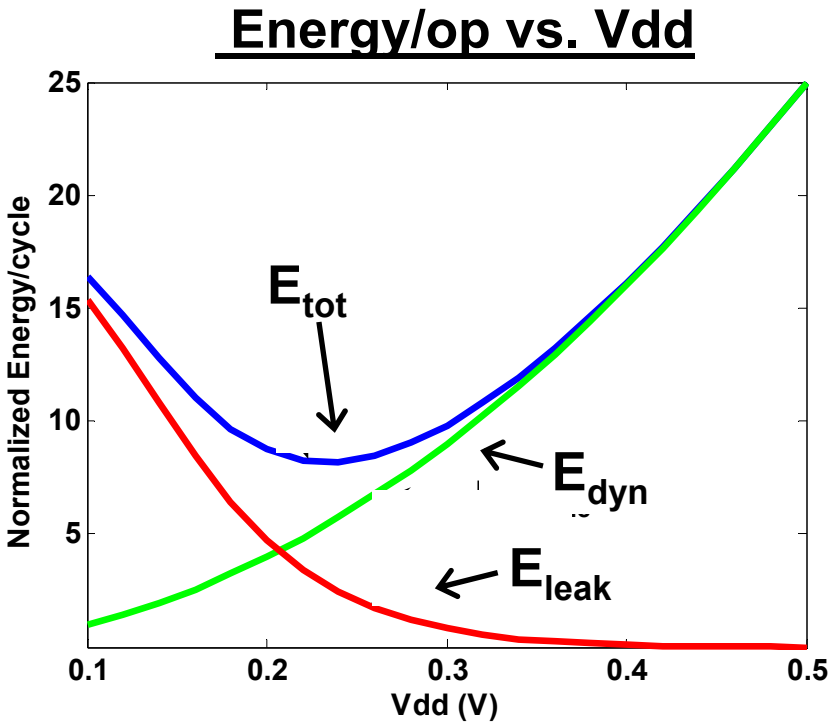
CMOS is Scaling, Power Density is Not

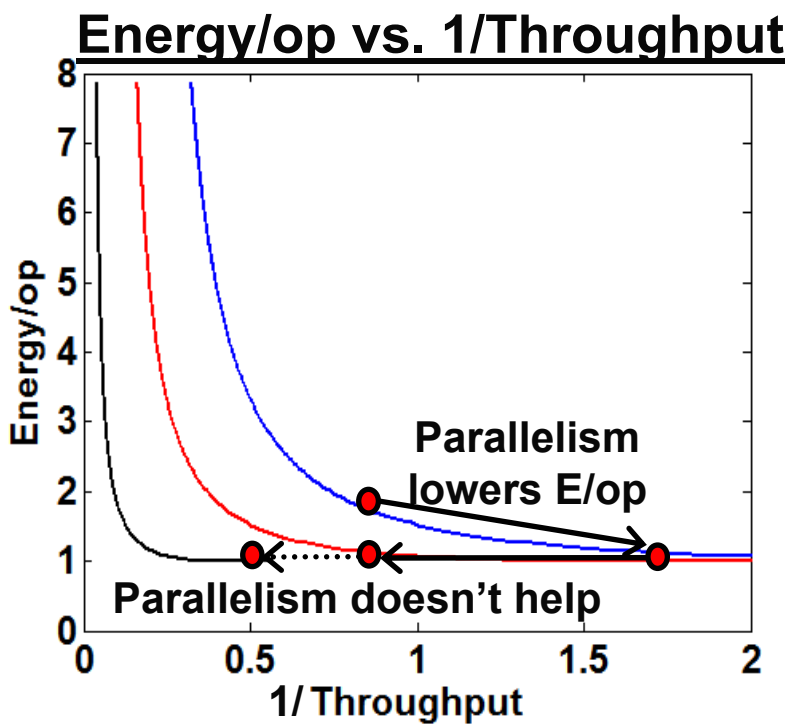




- V_{dd} and V_t not scaling well → power/area not scaling
- Parallelism to improve throughput within power budget

Where Parallelism Doesn't Help

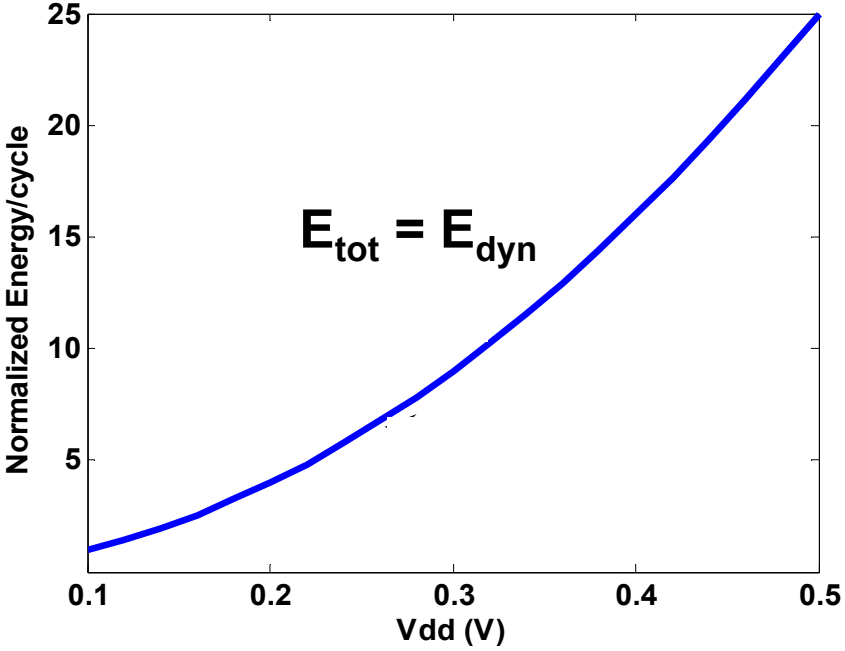




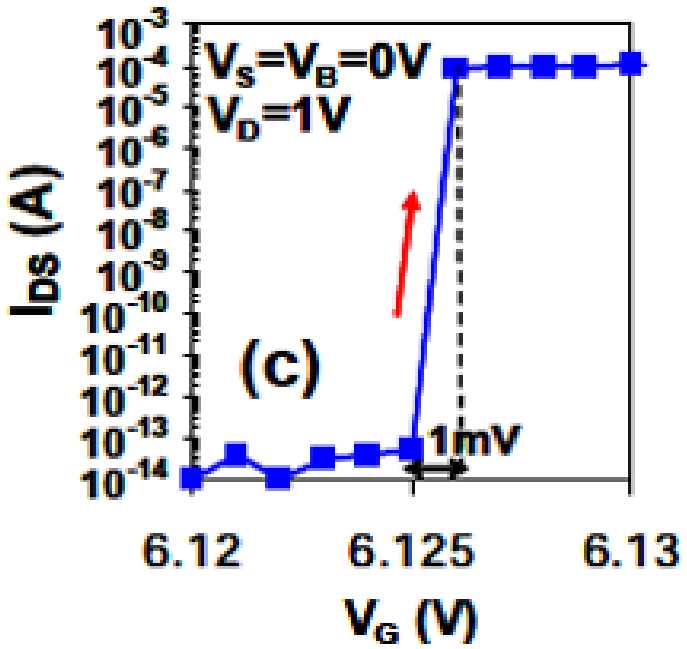
- CMOS circuits have well-defined minimum energy
  - Caused by leakage and finite sub-threshold swing
  - Need to balance leakage and active energy
- Limits energy-efficiency, no matter how slowly the circuit runs

What if There Was No Leakage?

Energy/op vs. Vdd



Measured MEM Switch IV*



- Vdd decreases → energy decreases
- Mechanical switch offers near infinite sub-threshold slope and no leakage current

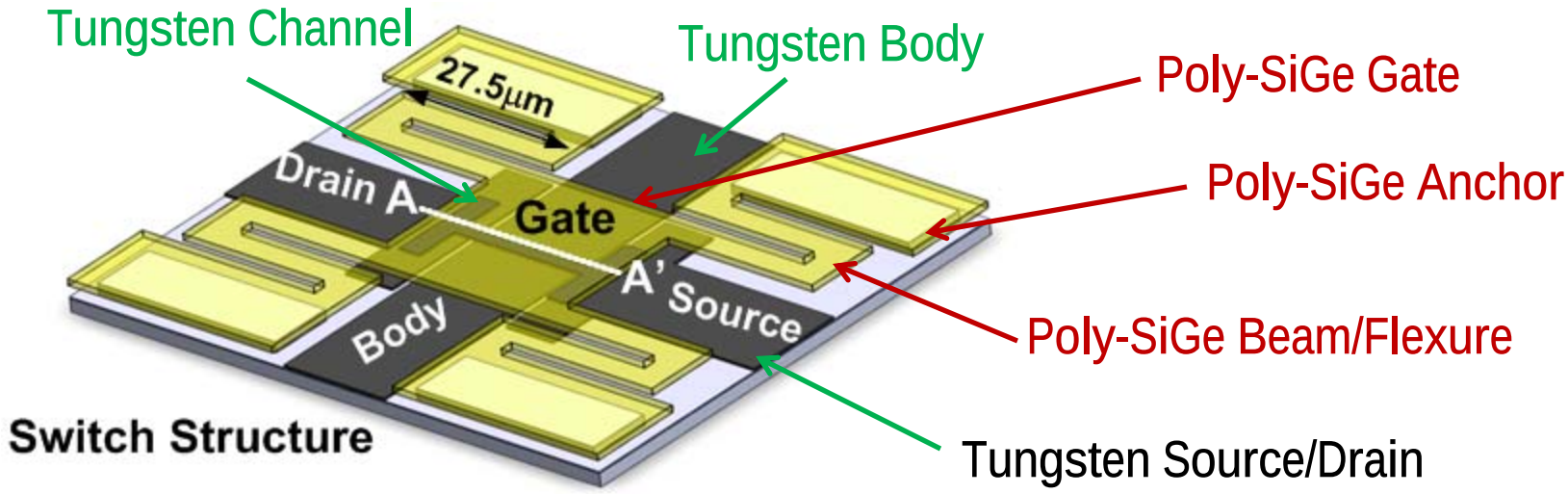
*R. Nathanael *et al*., "4-Terminal Relay Technology for Complementary Logic," *IEDM 2009*

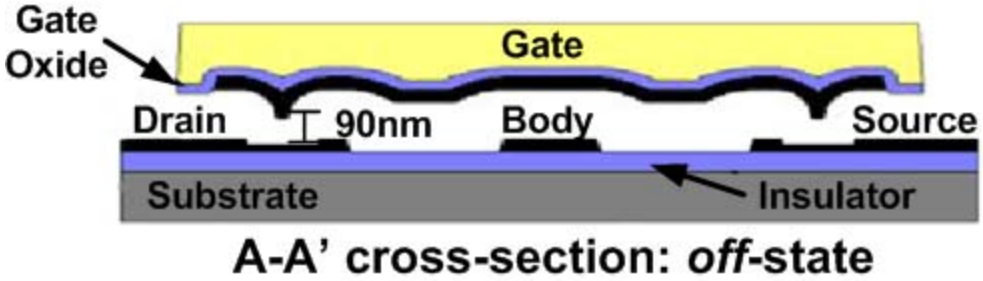
Outline

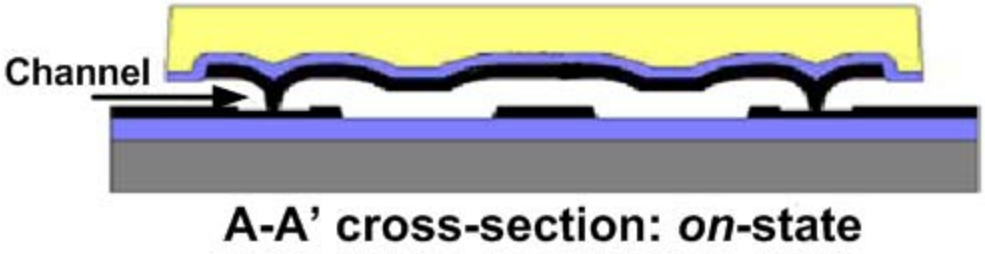
- Digital Circuit Design with NEM Relays
  - Relay device/circuit basics
  - Comparisons to CMOS
  - Device implications
- Analog/Mixed-Signal Design with Relays
- Looking Forward and Conclusions

F. Chen *et al*., "Integrated Circuit Design with NEM Relays," *ICCAD 2008*

Switch Structure & Operation







Open Switch ("OFF"):

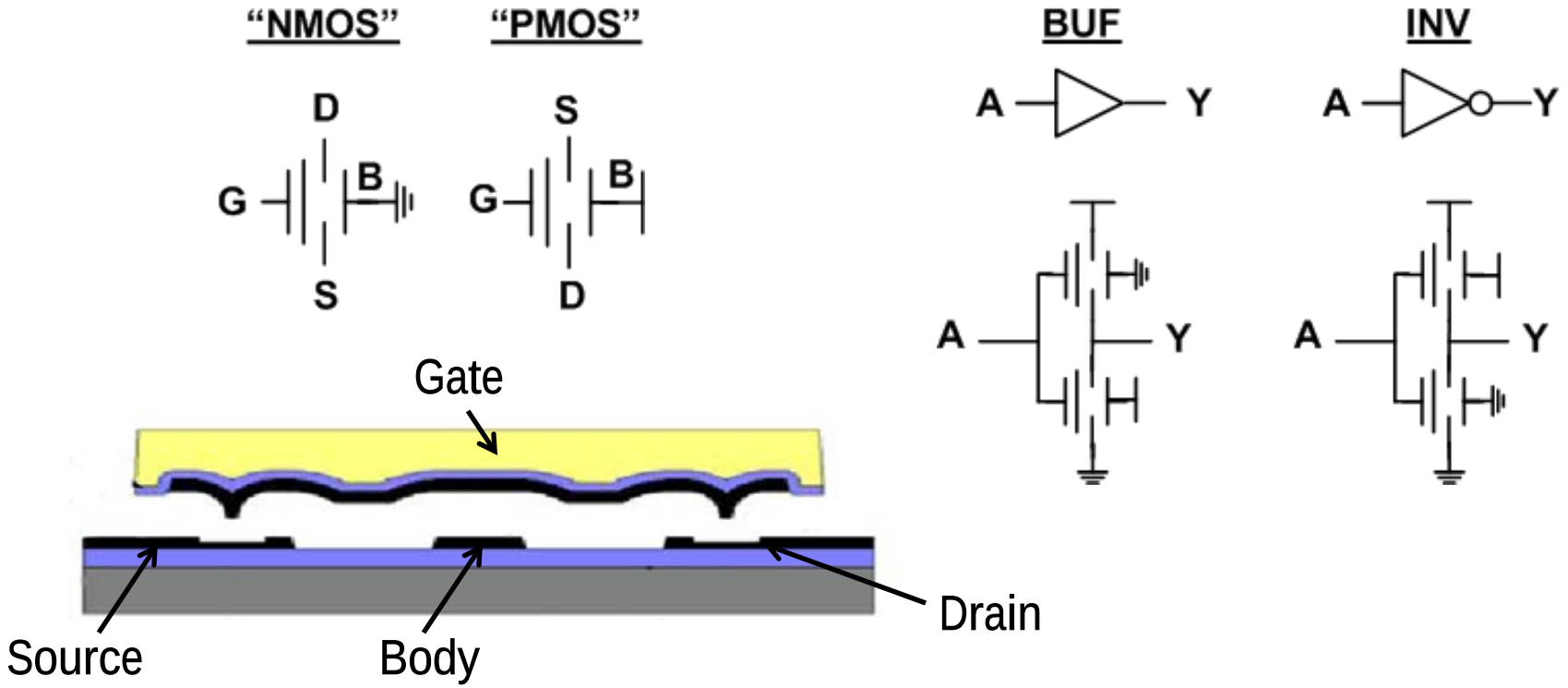
$|V_{gb}| < V_{po}$ (pull-out voltage)

Closed Switch ("ON"):

$|V_{gb}| > V_{pi}$ (pull-in voltage)

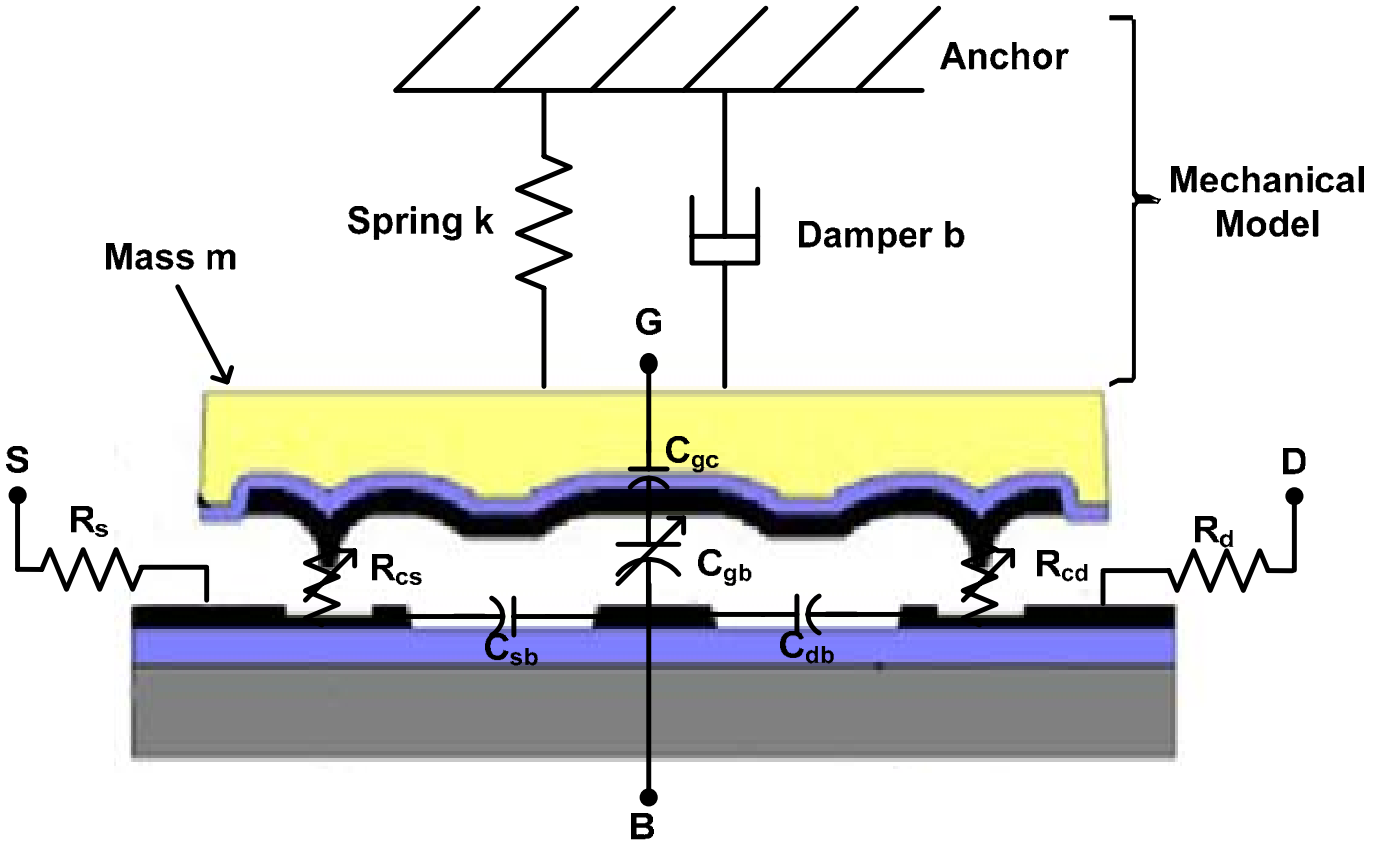
R. Nathanael *et al*., "4-Terminal Relay Technology for Complementary Logic," *IEDM 2009*

NEM Relay as a Logic Element



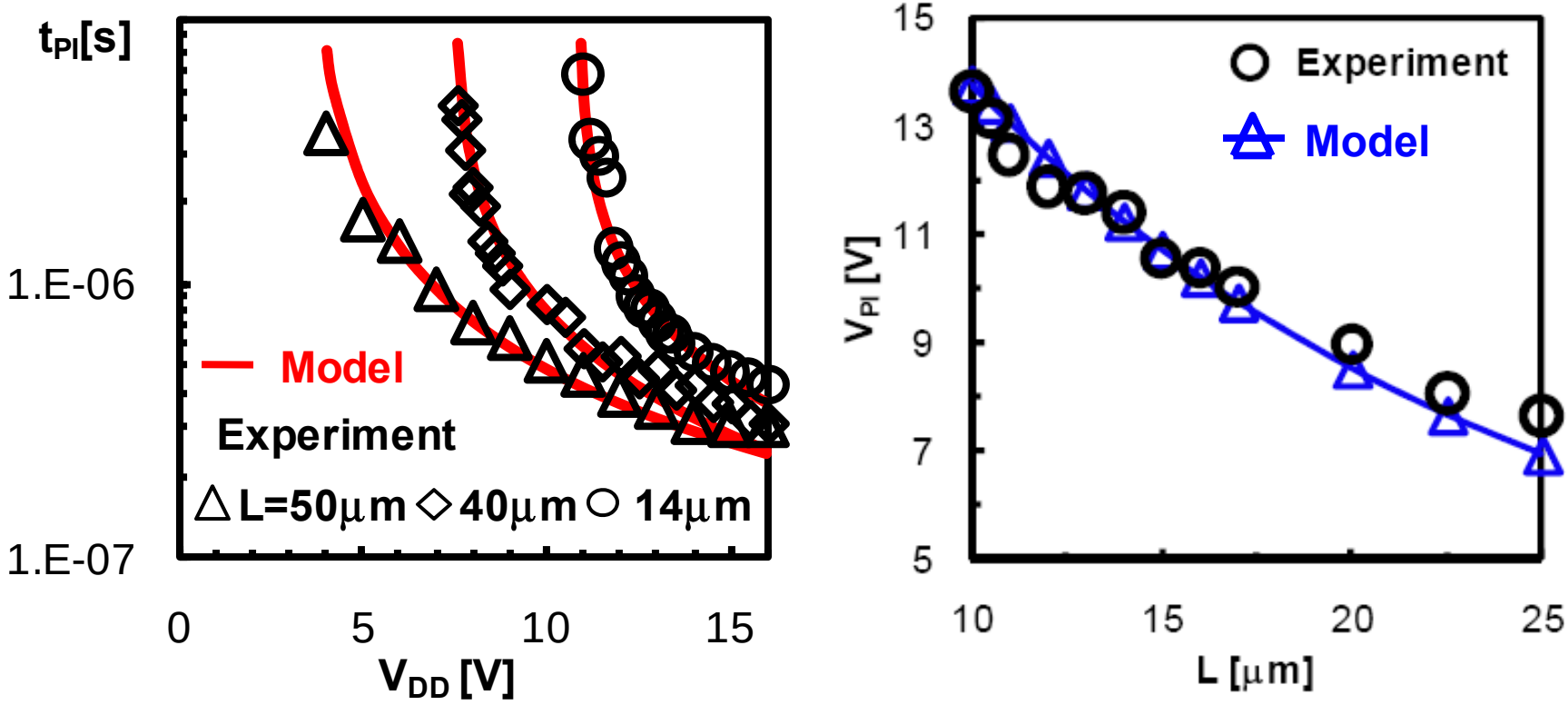
- **4-terminal design mimics MOSFET operation**
  - **Electrostatic actuation is ambipolar**
- **Non-inverting logic is possible**
  - **Actuation independent of source/drain voltages**

NEM Relay Model



- **Lumped Verilog-A model for circuit sims:**
  - **Mechanical dynamics: spring (k), damper (b), mass (m)**
  - **Electrical parasitics: non-linear gate-body (C_{gb}), gate-channel (C_{gc}), and source/drain-body cap ($C_{s,db}$), contact ($\underline{R_{cs,d}}$)**

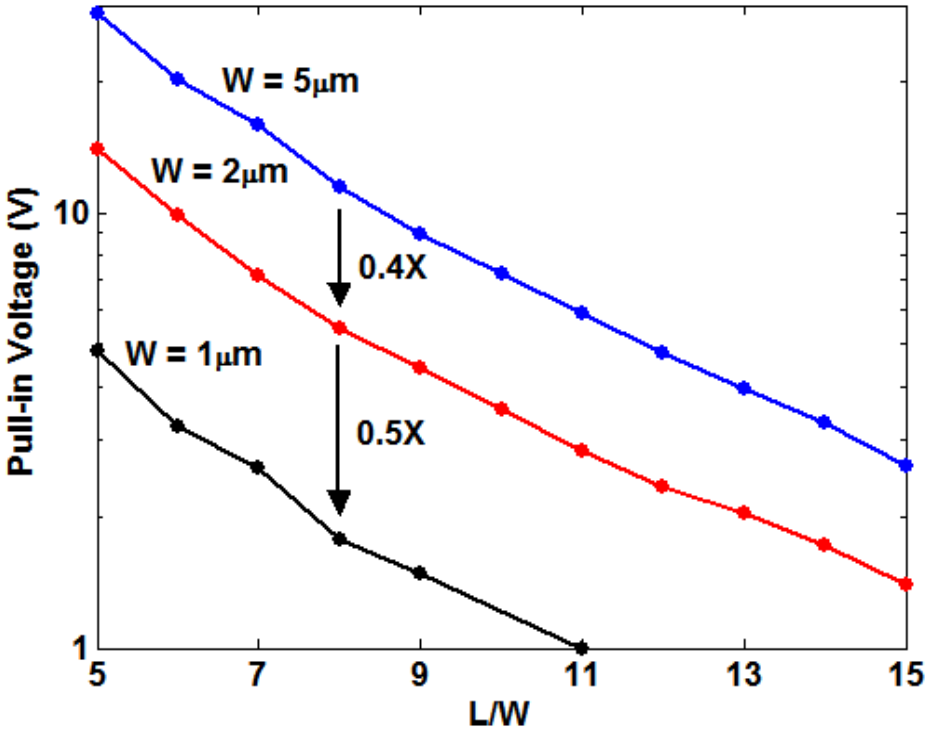
Relay Characteristics



- Lumped model matches measurements
- Use calibrated models for circuit design

Relay Scaling

- **Constant E-field: mechanical delay and V_{PI} scale linearly***
  - **Assuming surface forces scale – more later**

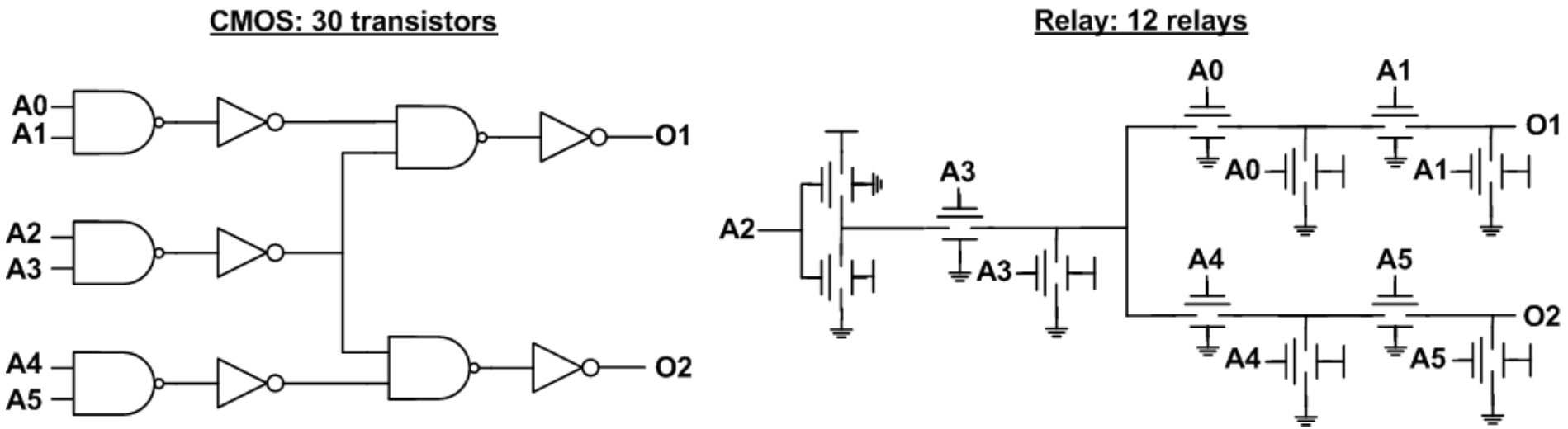


- **For a 90nm device: V_{PI} ~200mV, t_{PI} ~10ns @ V_{dd} = 1V**
  - **(cantilever beam with W = 90nm, H = 90nm, t_{gap} = 10nm, L = 2.3um)**

- **Seems "large" and "slow" *vs.* CMOS, but…**

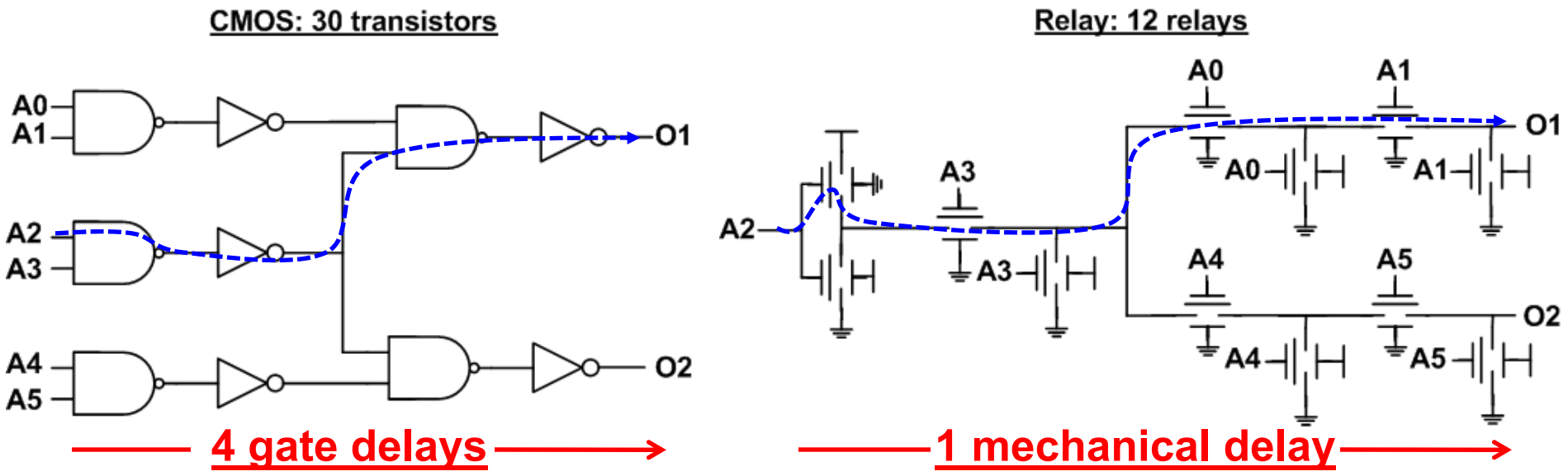
*H. Kam *et al*., "Design and Reliability of a Micro-Relay Technology…," *IEDM 2009*

Digital Circuit Design with Relays



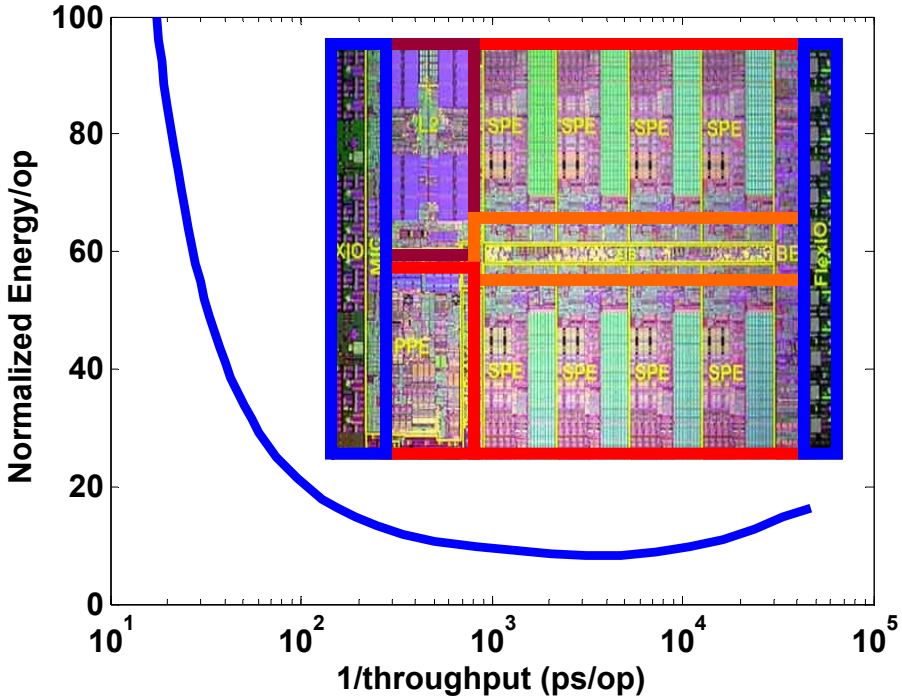
- **CMOS: delay set by electrical time constant**
  - **Quadratic delay penalty for stacking devices**
  - **Buffer & distribute logical/electrical effort over many stages**
- **Relays: delay dominated by mechanical movement**
  - **Can stack ~100-200 devices before $t_{d,elec} \approx t_{d,mech}$**
  - **So, want all relays to switch simultaneously**
  - **→ Implement logic as a single complex gate**

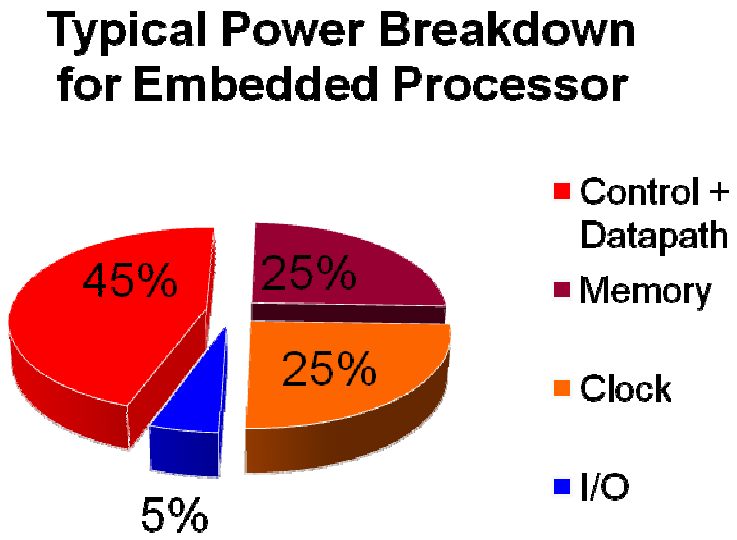
Digital Circuit Design with Relays



- **Delay Comparison vs. CMOS**
  - Single mechanical delay vs. several electrical gate delays
  - For reasonable load, relay delay unaffected by fan-out/fan-in
- **Area Comparison vs. CMOS**
  - Larger individual devices
  - Fewer devices needed to implement the same logic function

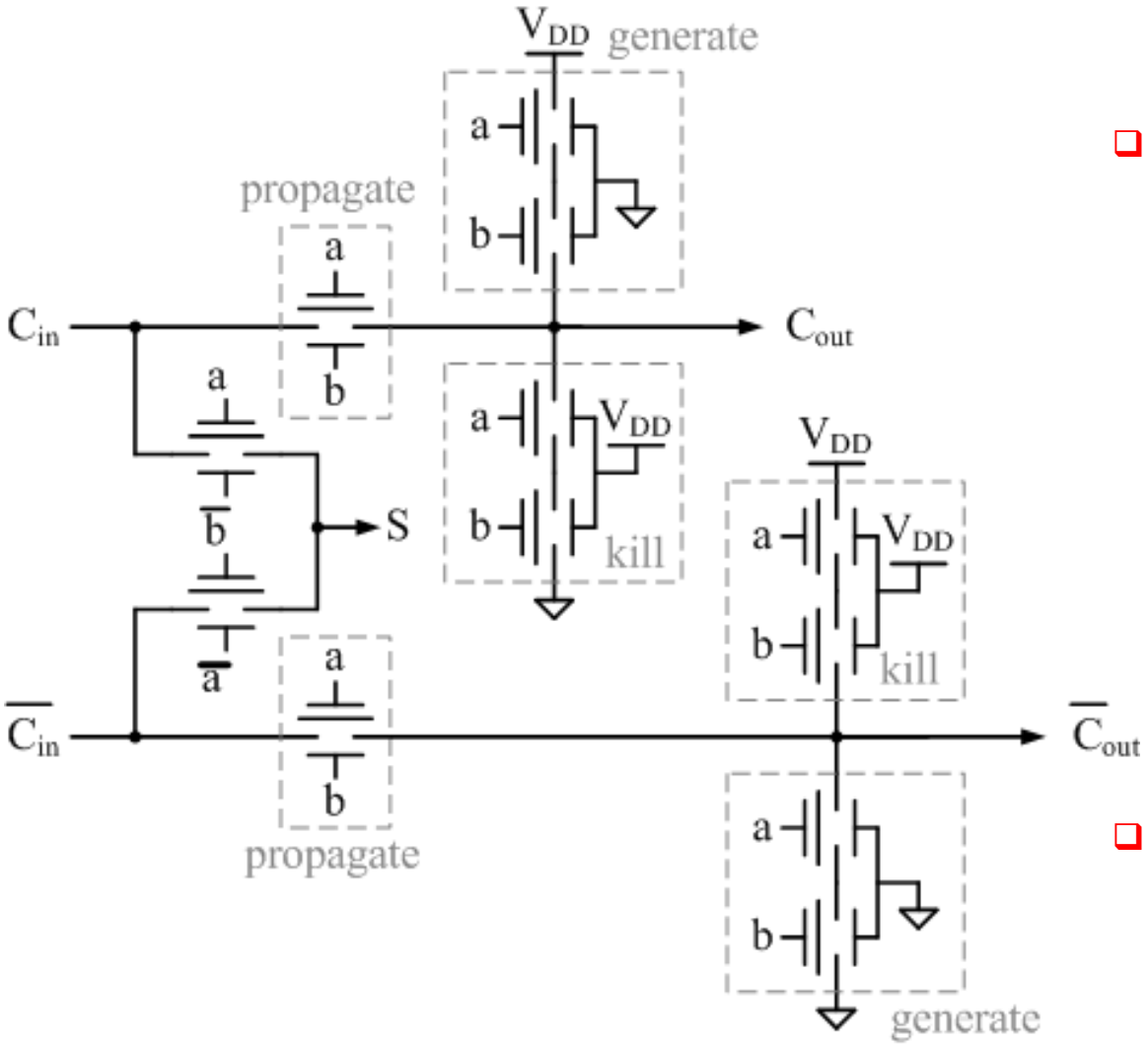
CMOS vs. Relays: Digital Logic





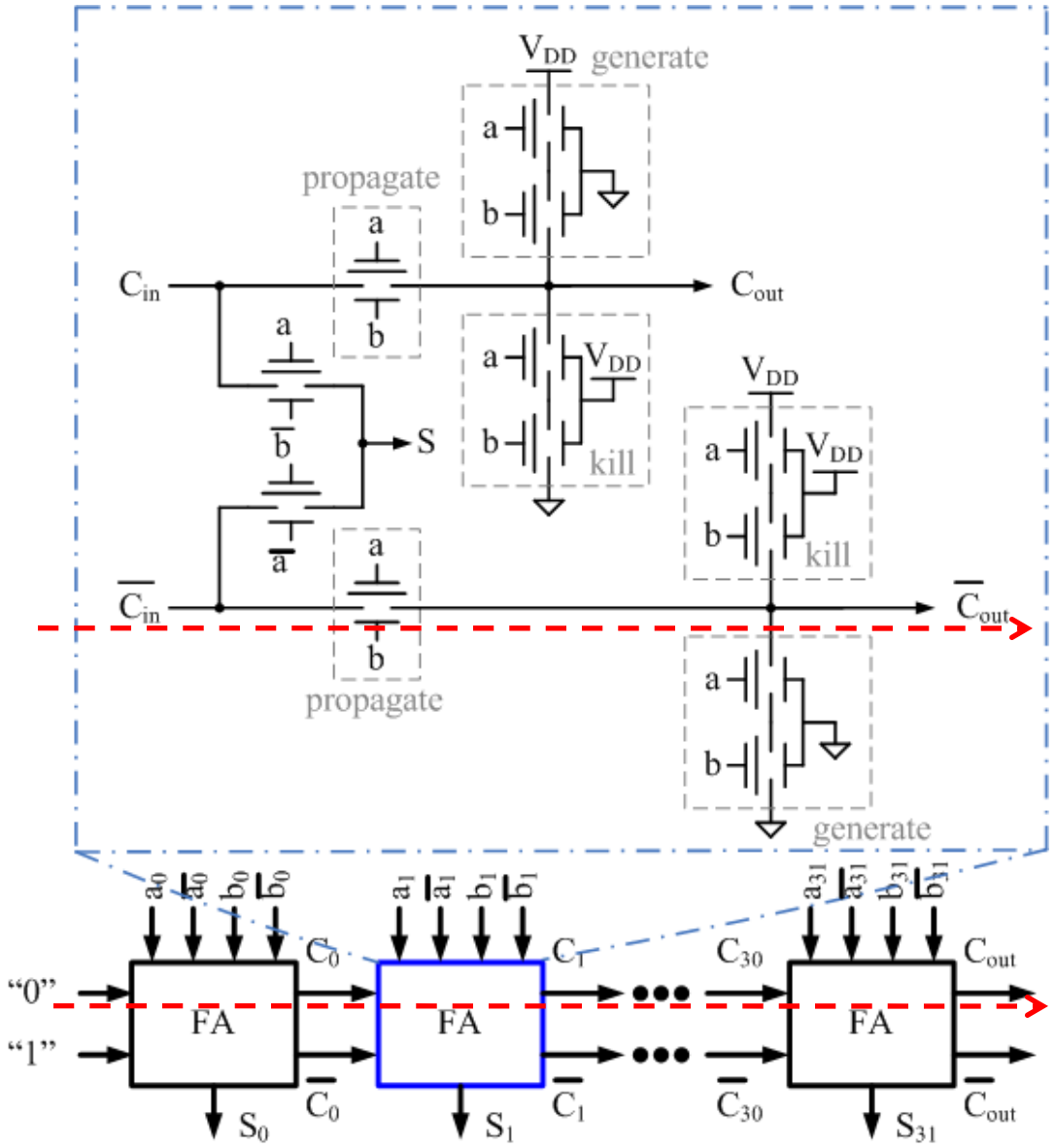
- Most processor components exhibit the energy vs. performance tradeoff of static CMOS
  - Control, Datapath, Clock
- Adder energy performance tradeoff is representative

Relay-Based Adder



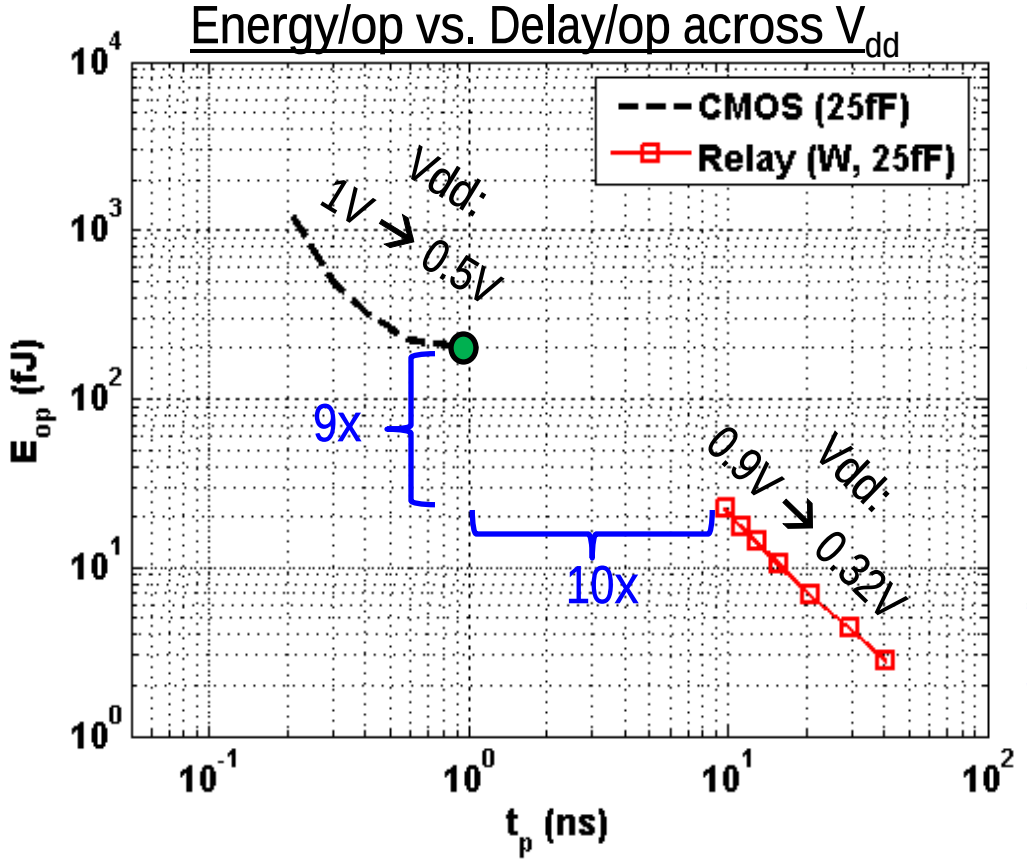
- **Full adder cell:**
  - **12 relays vs. 24 transistors**
  - **XOR "free"**
  - **Complementary signals avoid extra mechanical delay (to invert)**
- **Relays all sized minimally**

N-bit Relay-Based Adder



- Ripple carry configuration
- Cascade full adder cells to create larger complex gate
- Stack of N relays, but still single mechanical delay

Simulated Energy-Delay vs. CMOS

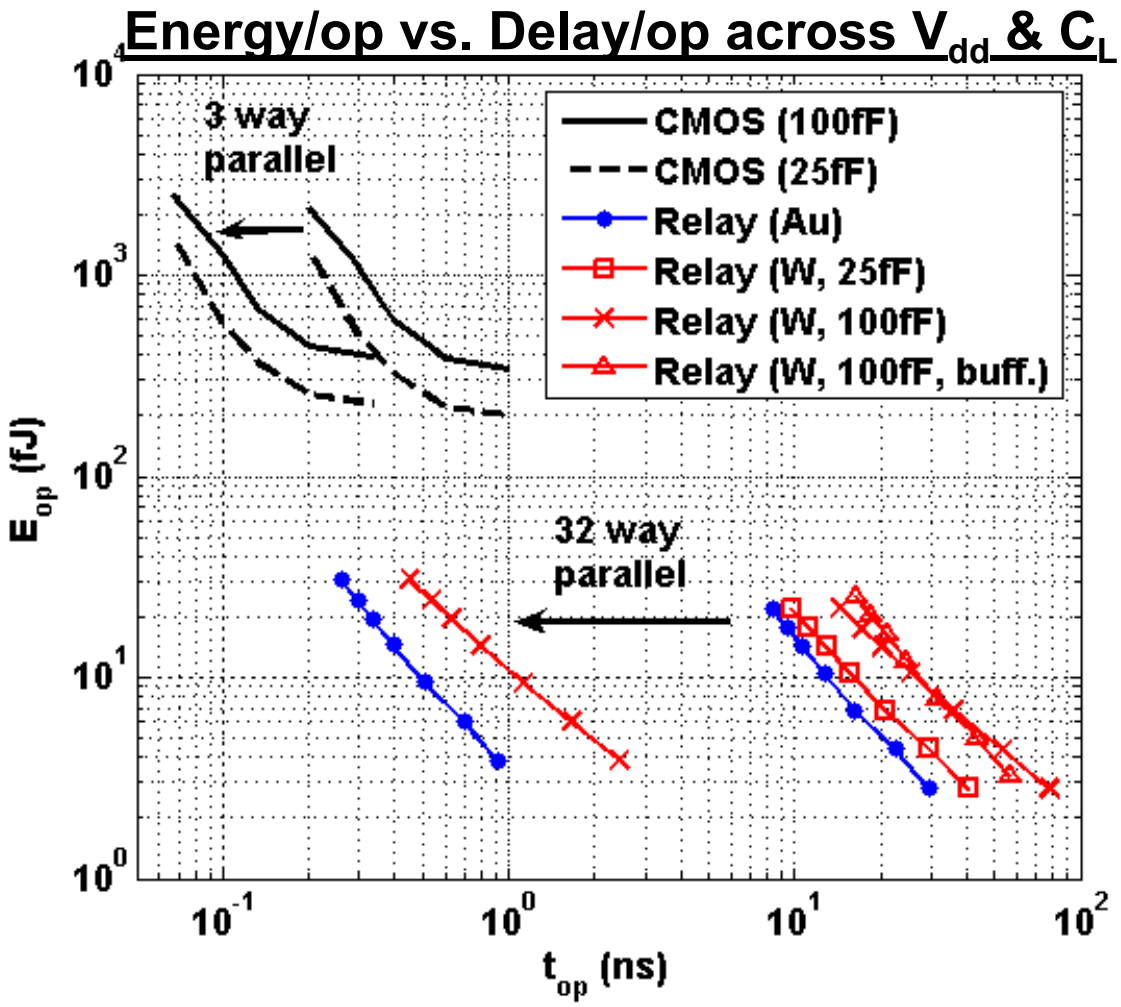


- Compare *vs.* Sklansky CMOS adder*
- 30x less capacitance
  - Lower device C_g, C_d
  - Fewer devices
- 2.4x lower V_{dd}
  - No leakage energy

- For similar area: >9x lower E/op, >10x greater delay

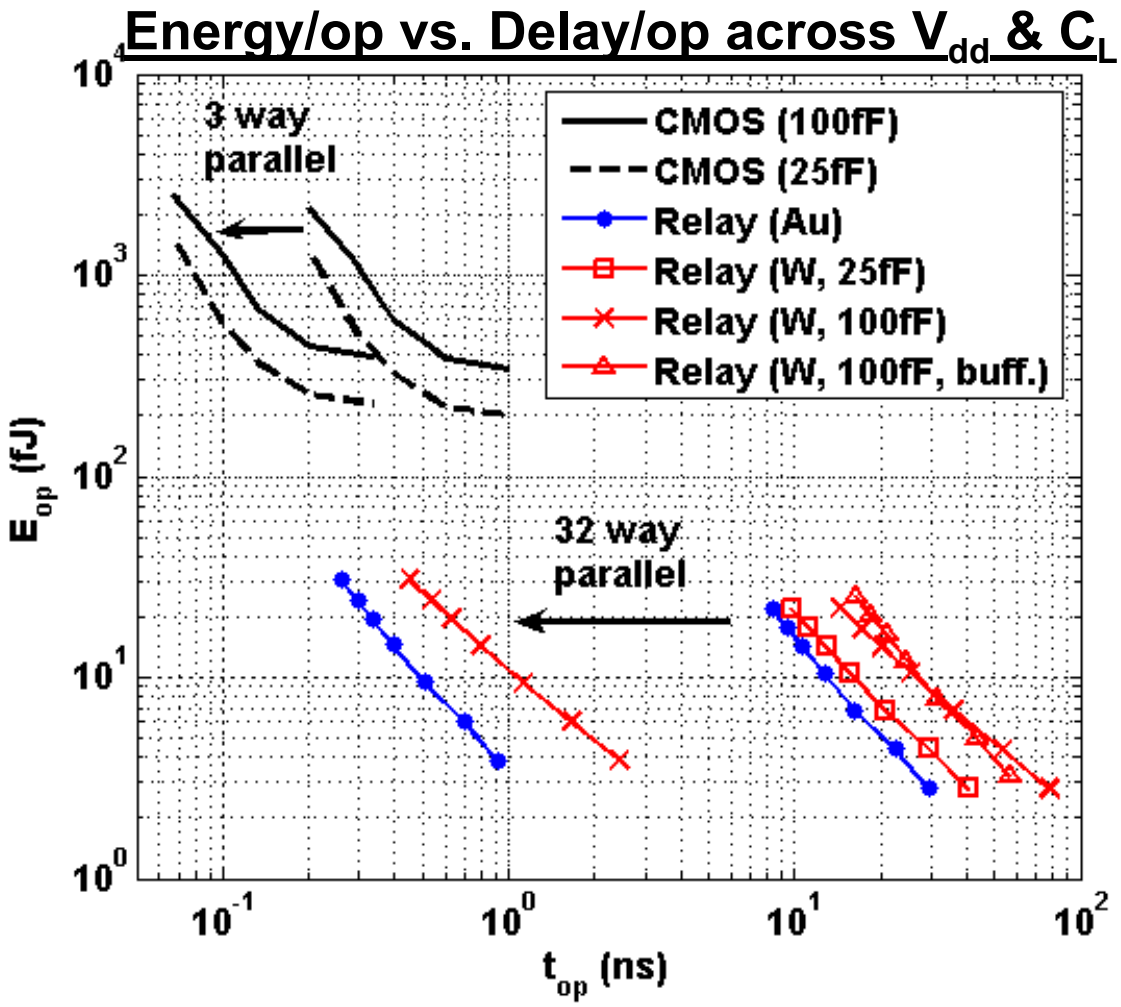
*D. Patil et. al., "Robust Energy-Efficient Adder Topologies," in Proc. 18th IEEE Symp. on Computer Arithmetic (ARITH'07).

Parallelism



- Can extend energy benefit up to GOP/s throughput
  - As long as parallelism is available
- Area overhead bounded
  - Need to parallelize CMOS at some point too

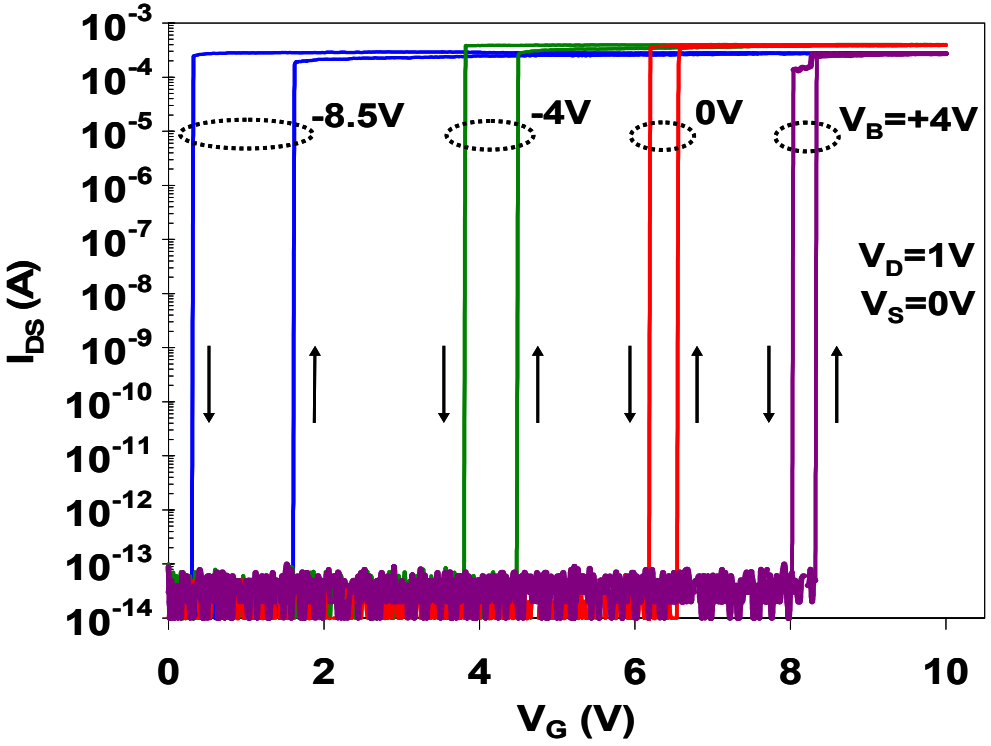
Contact Resistance

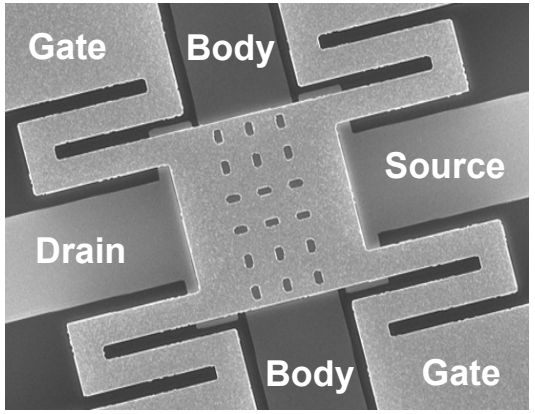


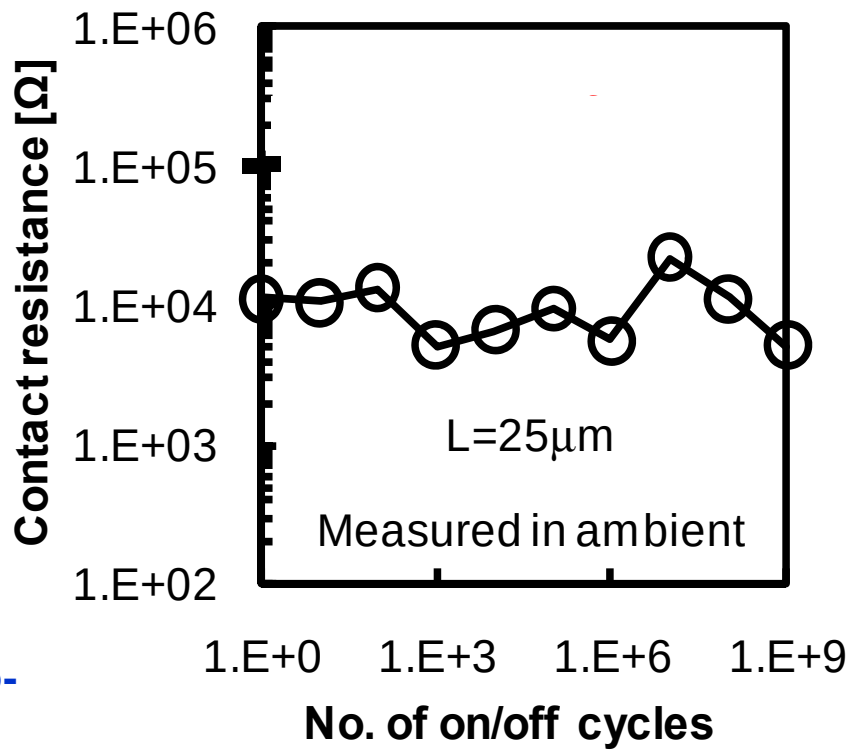
- **Low contact R not critical**
  - **Enables low force, hard contact material**
- **Good news for reliability…**

Fabricated Device Revisited

- **Improve reliability: intentionally increase contact R**
  - **Coat W electrodes with TiO_2**



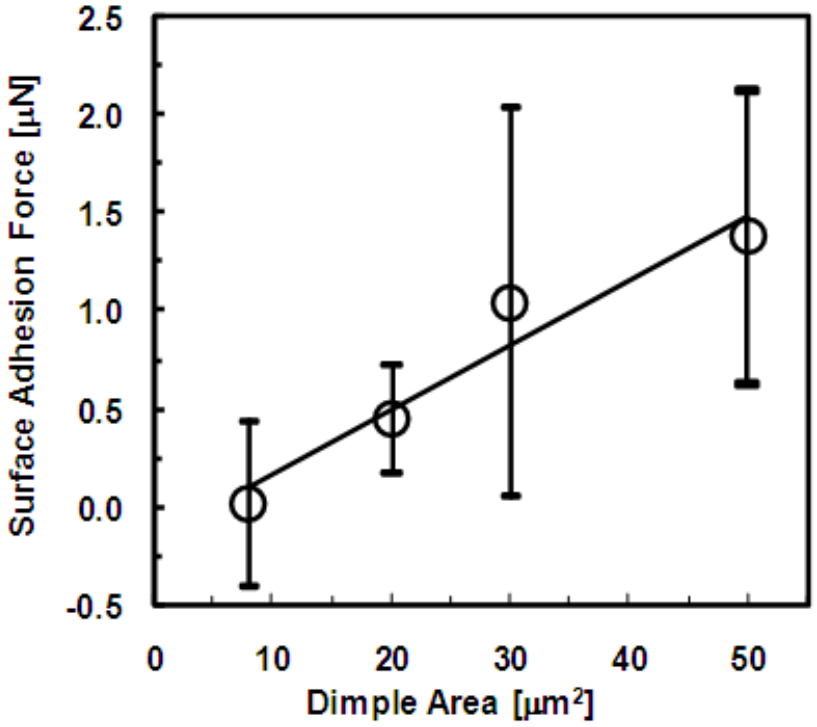




*H. Kam *et al*., "Design and Reliability of a Micro-Relay Technology…," *IEDM 2009*

Relay Energy Limit

- Spring force must be able to overcome surface adhesion force F_A
- For large contacts, F_A scales with area:



- Extracted surface energy ~5μJ/m²
- Relay energy limit set by required R_{on}

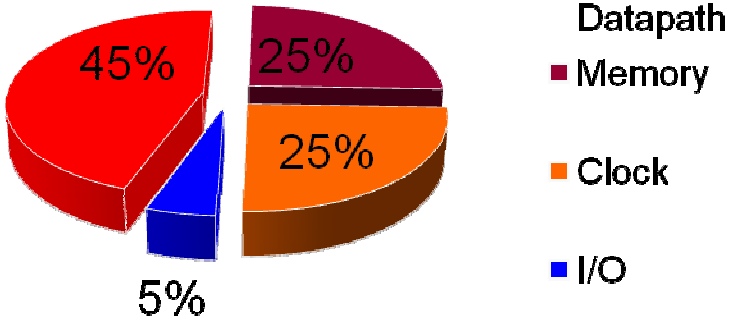
*H. Kam *et al*., "Design and Reliability of a Micro-Relay Technology…," *IEDM 2009*

Outline

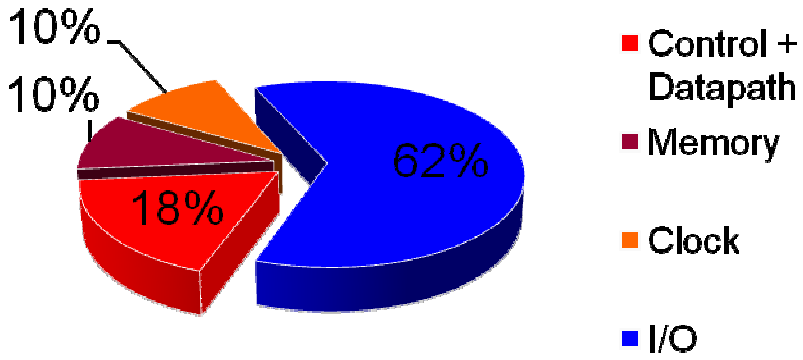
- Digital Circuit Design with NEM Relays
  - Relay device/circuit basics
  - Comparisons to CMOS
- **Analog/Mixed-Signal Design with Relays**
- Looking Forward and Conclusions

CMOS vs. Relays: Mixed Signal

Typical Power Breakdown for Embedded Processor



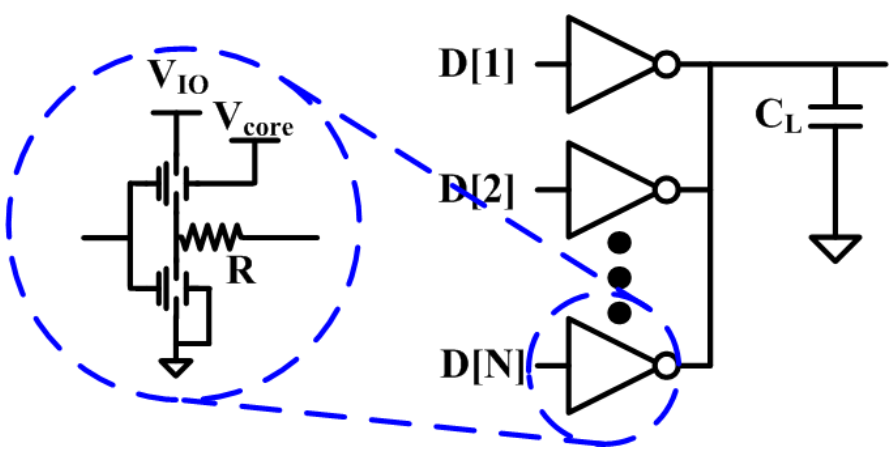
Power Breakdown: core implemented in relays



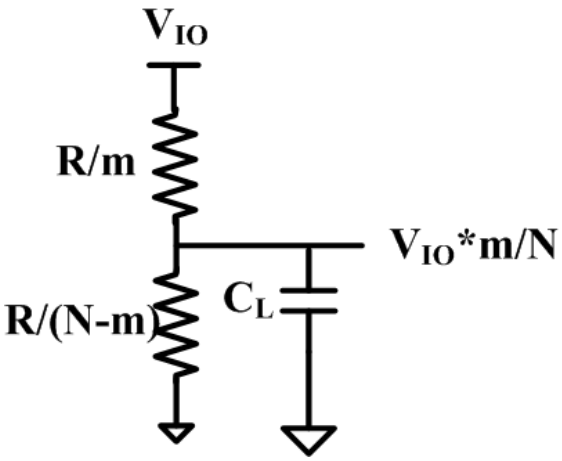
- **I/O energy dominant if core is ~30x more efficient**
  - **See if I/O circuits can benefit as well**
  - **Representative examples: DAC & ADC**
- **How to process/generate analog signals?**
  - **No or limited "linear gain" in relays – rely on switching**

NEM Relay Based DAC

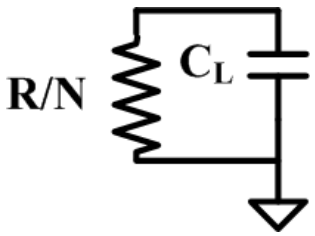
DAC Architecture



Voltage Output



AC Impedance

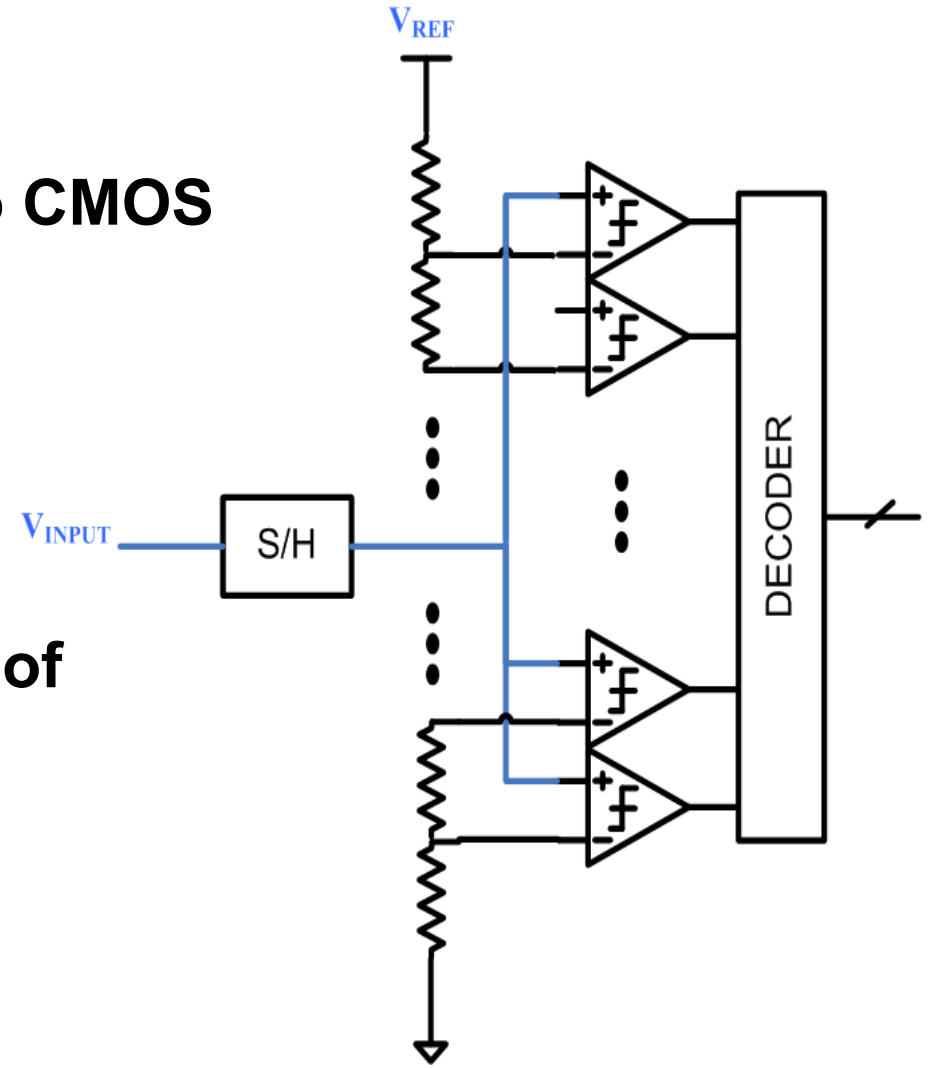


$$E_{BIT} = \frac{\pi}{2} V_{IO}^2 C_L$$

- **Same topology as CMOS, except:**
  - **Add passive R to set impedance**
  - **Relays' gate voltage independent of I/O voltage**
- **Energy dominated by actual I/O energy:**
  - **@V_{IO}=200mV, C_L=1pF: 62.8fJ/bit vs. ~780fJ/bit for CMOS**

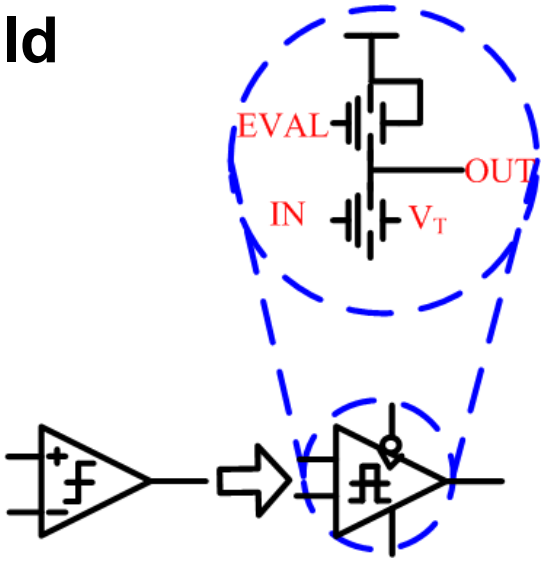
NEM Relay Based Flash ADC

- Topologically identical to CMOS
  - Sample/Hold input
  - Flash Converter – bank of comparators
- Key difference: behavior of "comparators"

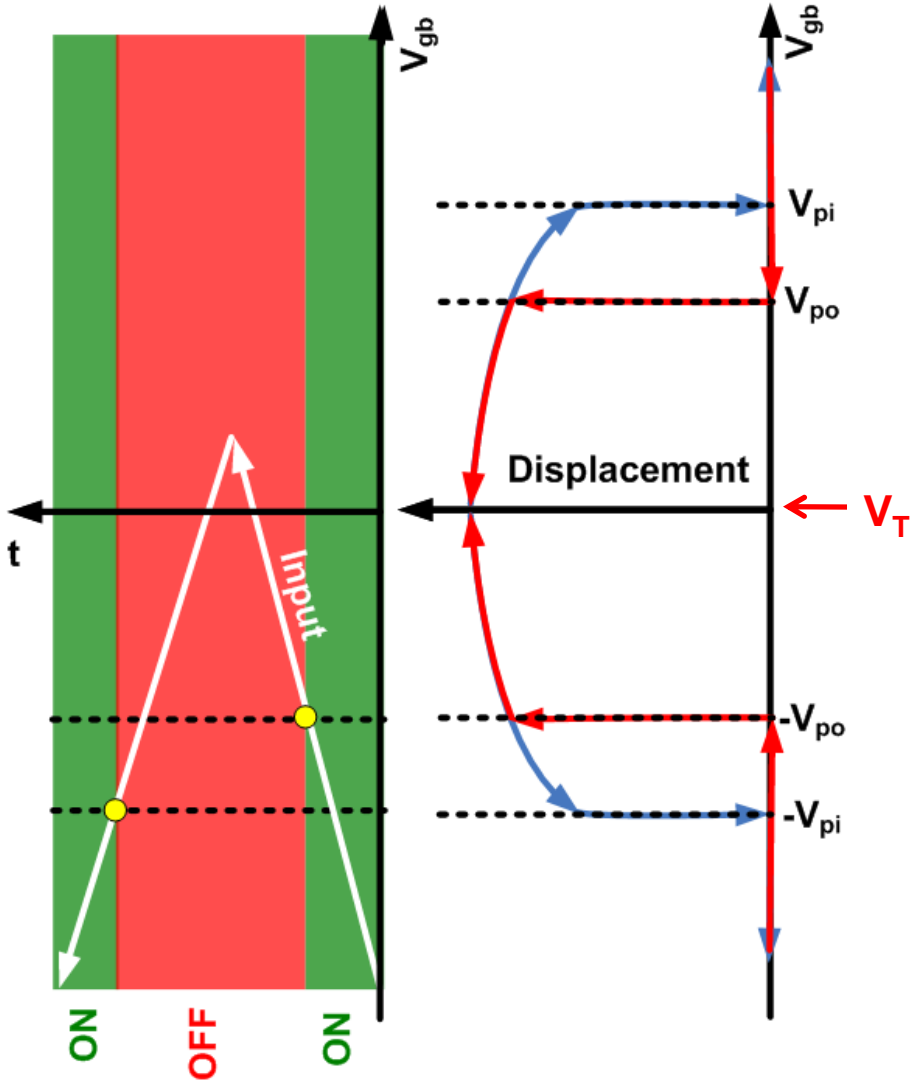


Relay Based Comparators

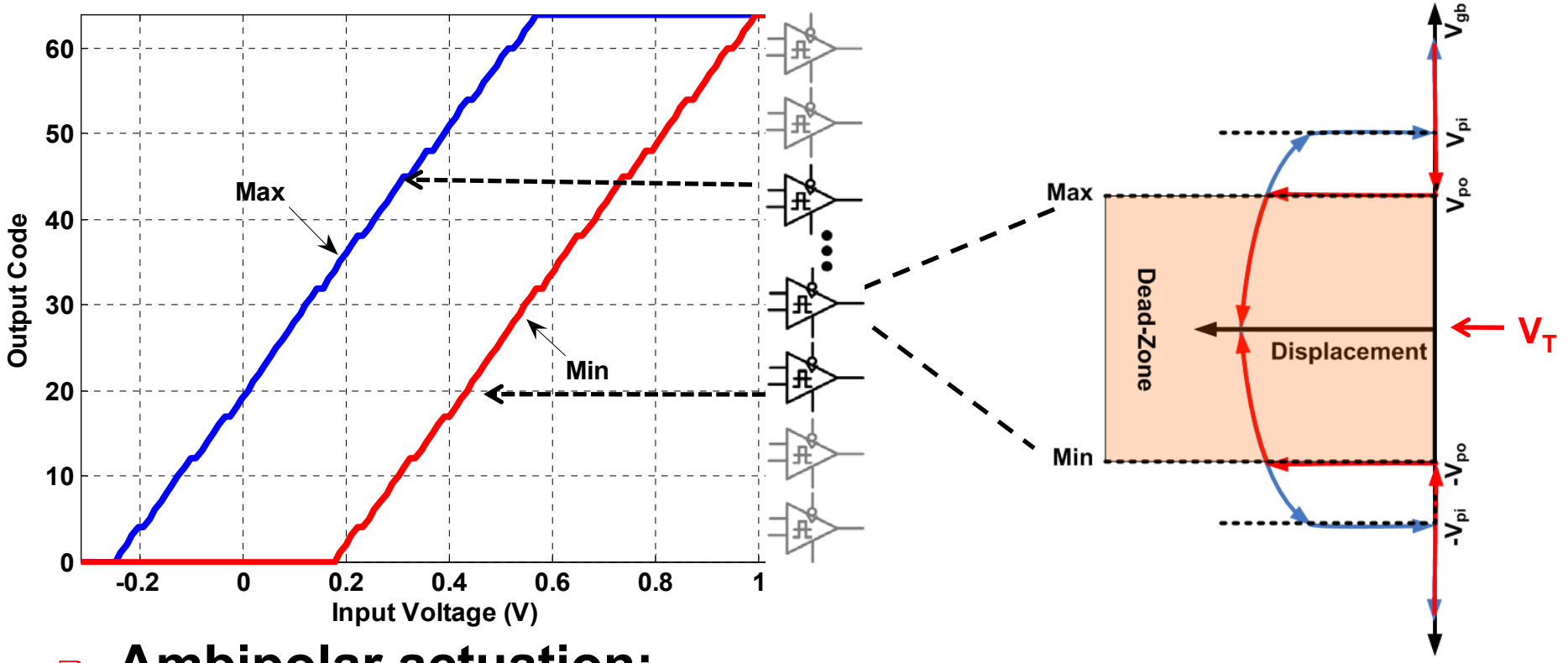
- **Body terminal used to set threshold**



- **Hysteretic switching:**
  - **Comparator threshold varies with previous state**
  - **Need to reset all comparators to the same initial state**



Relay Based Comparators



- **Ambipolar actuation:**
  - Comparators above & below input will evaluate
  - Use a different decoder
- **Each comparator has a "dead-zone" where it stays off**
  - Can use "Max" or "Min" of this range to determine code

ADC Results

V_{core} = 0.3V

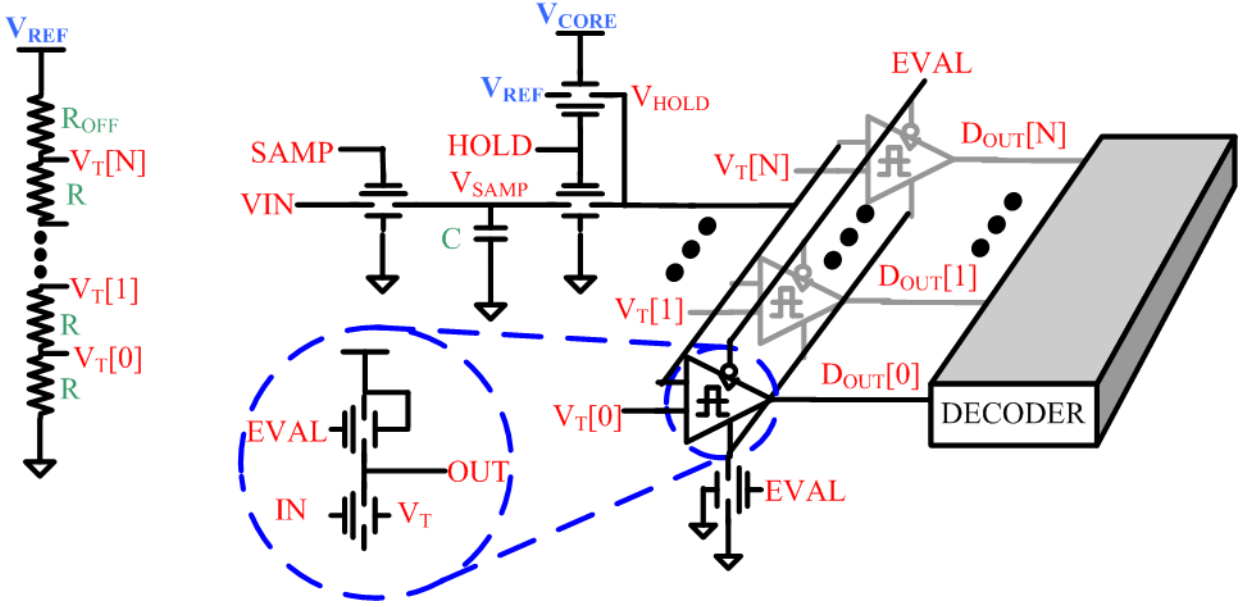
C = 500fF

R = 4kΩ

V_{REF} = 1V

f_{samp} = 10 MS/s

6-bit res: 5.5fJ/conv



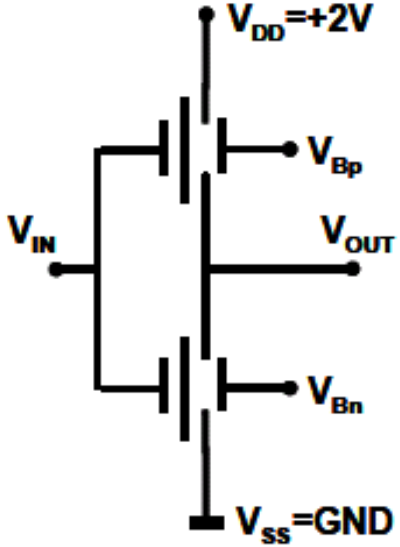
- Energy dominated by resistor string (320fJ out of 350fJ)
  - Power set by input dynamic range (V_{REF}), not core voltage
  - FOM improves with more resolution (up to thermal noise limit)
- Advantages stem from $R_{on}C_g$ product

Outline

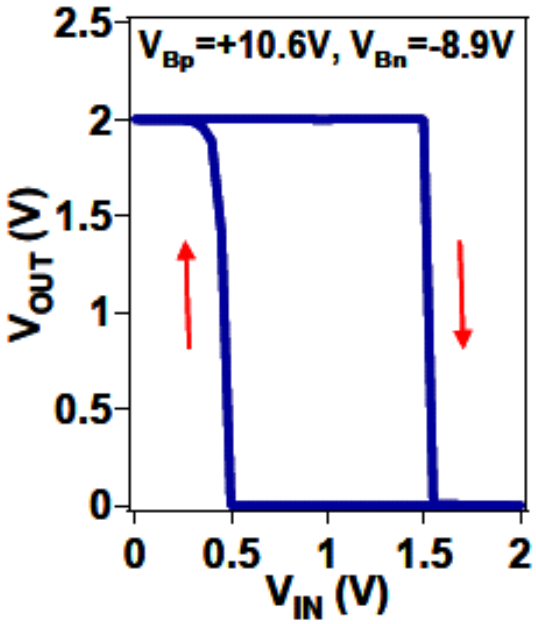
- Digital Circuit Design with NEM Relays
  - Relay device/circuit basics
  - Comparisons to CMOS
- Analog/Mixed-Signal Design with Relays
- **Looking Forward and Conclusions**

Experimental Relay Circuits: Inverter

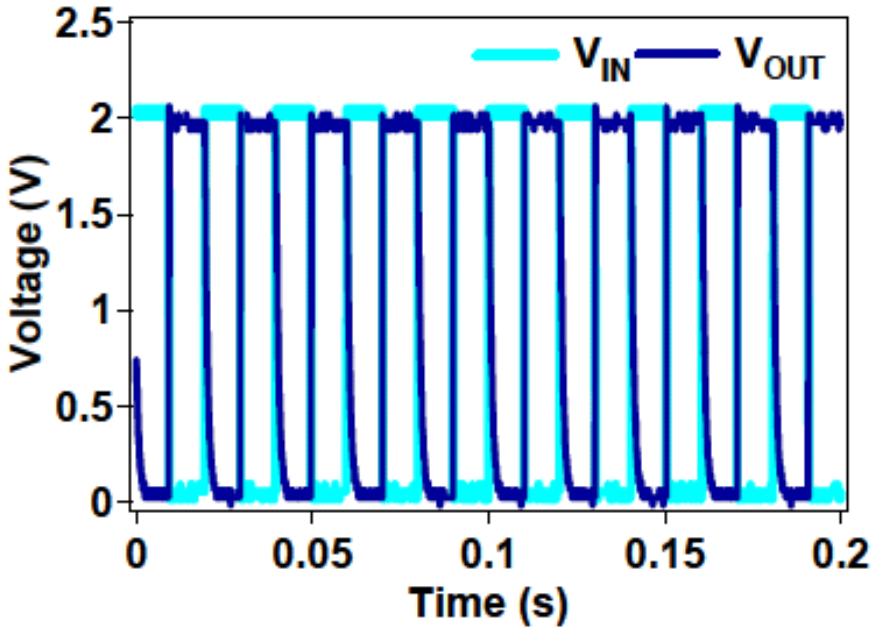
Circuit Diagram



Voltage Transfer Char.

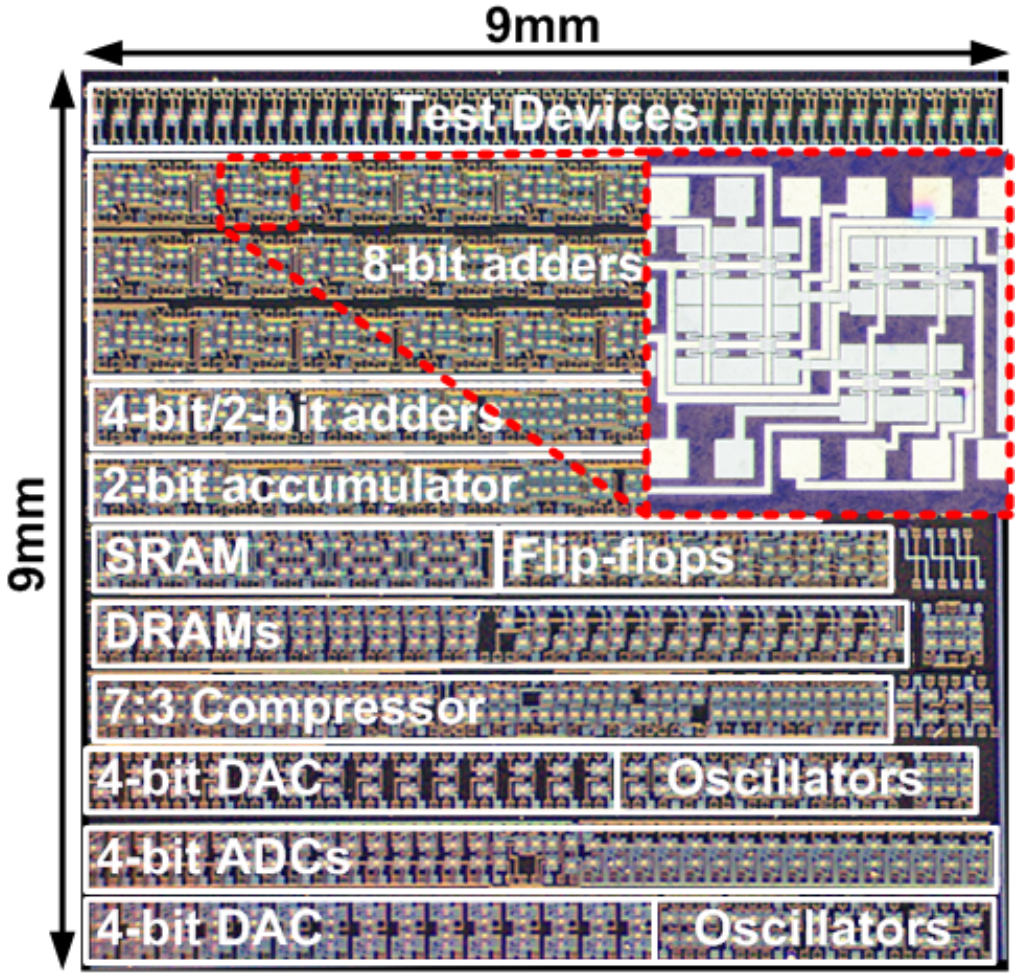


Voltage Waveforms



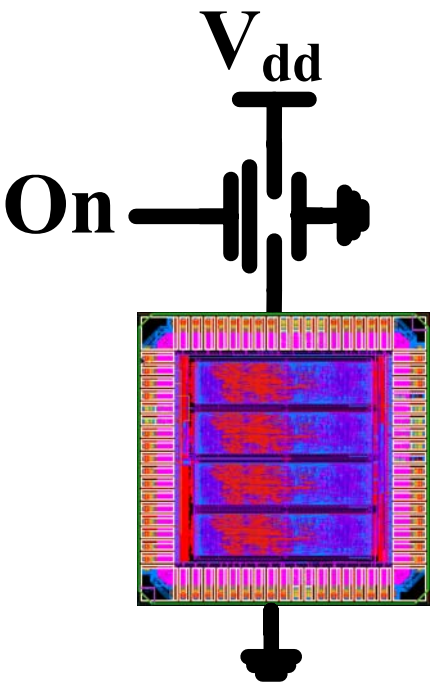
Circuit Demonstration Test-Chip

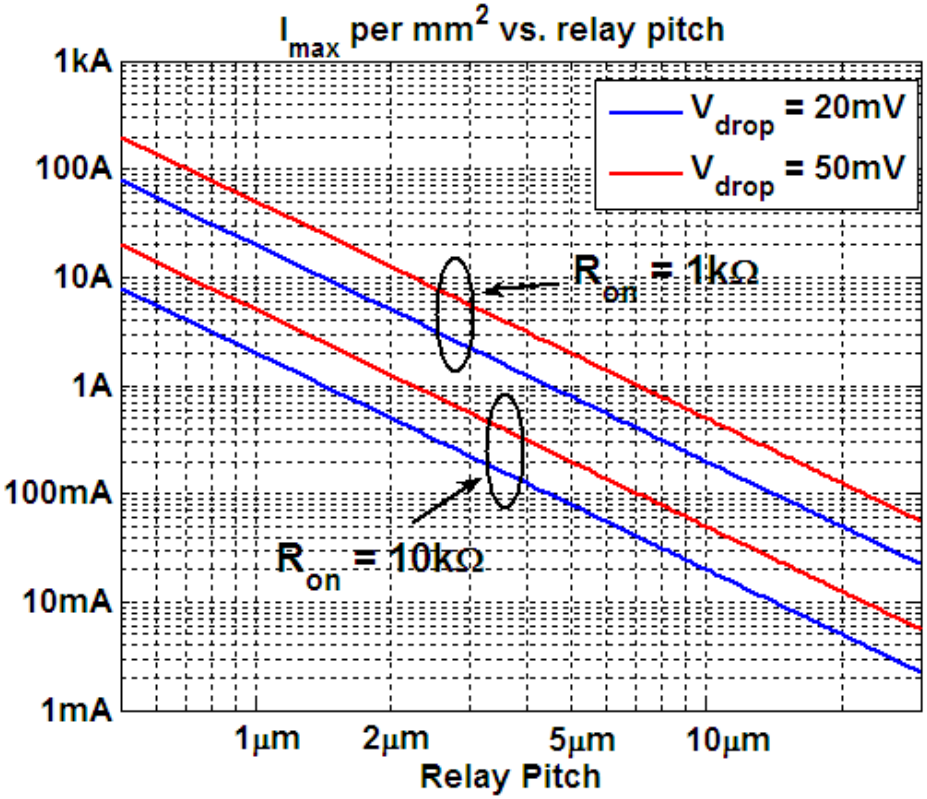
- Test devices
- Adders
- Flip-flops/Latches
- 7:3 Compressor
- SRAM, DRAM
- DAC
- ADC
- Oscillators



F. Chen *et al*., "Demonstration of Integrated Micro-Electro-Mechanical Switch Circuits for VLSI Applications," to be presented at *ISSCC 2010*.

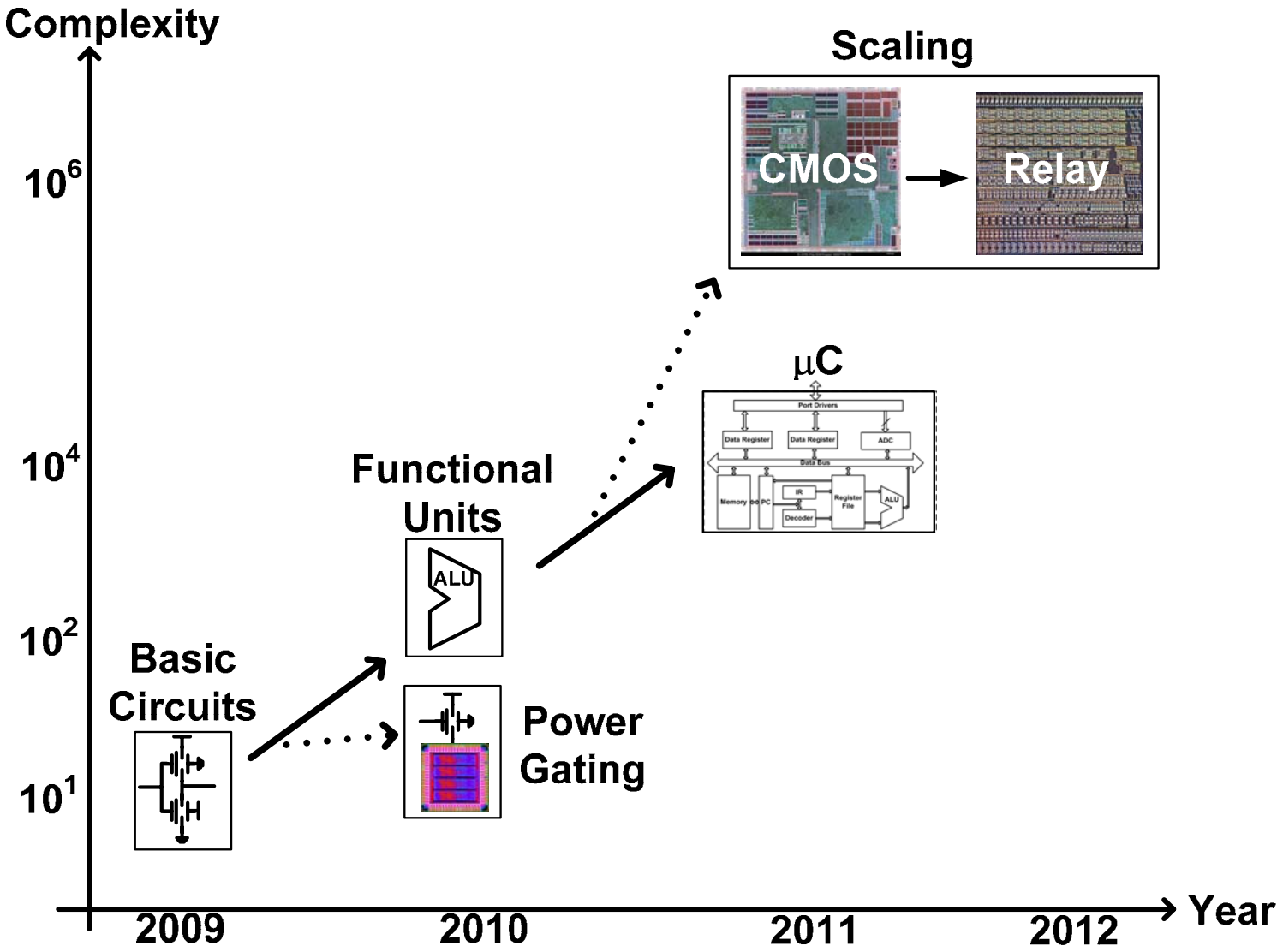
Near-Term Driver: Power Gating





- Pitch scaling enables high current density
  - Even with high individual device R_{on}
- TI micro-mirror pitch (~7.5µm): Imax ~ 100mA/mm^2

Roadmap


Complexity
10^6
10^4
10^2
10^1
Scaling
CMOS
Relay
µC
Port Drivers
Data Register
Data Register
ADC
Data Bus
Memory
PC
IR
Decoder
Register File
ALU
Functional Units
ALU
Basic Circuits
Power Gating
2009
2010
2011
2012
Year

Conclusions

- **NEM relays offer unique characteristics**
  - **Nearly ideal I_{on}/I_{off}**
  - **Significantly lower C_g than CMOS**
  - **Switching delay largely independent of electrical τ**
- **Relay circuits show potential for order of magnitude better energy efficiency**
- **Key challenges are scaling & reliability**
  - **Circuit-level insights have proven critical (contact R)**

Acknowledgements

- Students: Fred Chen, Hossein Fariborzi, Abhinav Gupta, Jaeseok Jeon, Hei Kam, Rhesa Nathanael, Vincent Pott, Matthew Spencer, Cheng Wang

- DARPA NEMS program
- FCRP (C2S2, MSD)
- Berkeley Wireless Research Center
- NSF