Blocker Tolerant Software Defined Receivers

Hooman Darabi

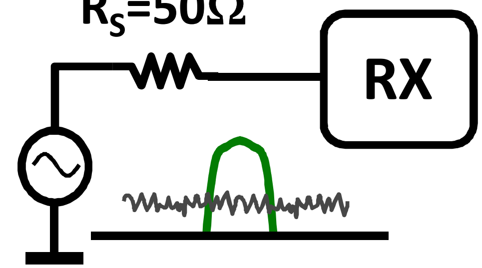
7/25/13

Receiver Noise and Linearity

- Receiver NF sets the sensitivity, range:

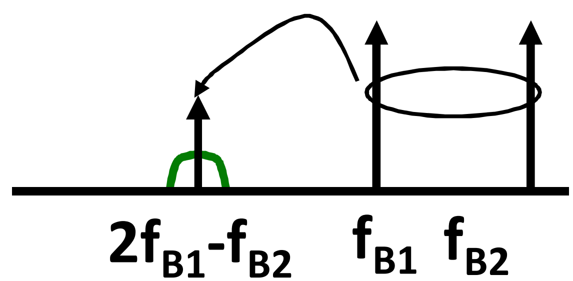
Sensitivity = -174 + NF + 10Log(BW) +SNR

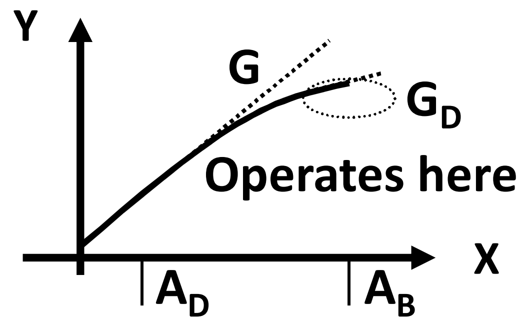
10Log(KT), dBm/Hz — Set by the standard



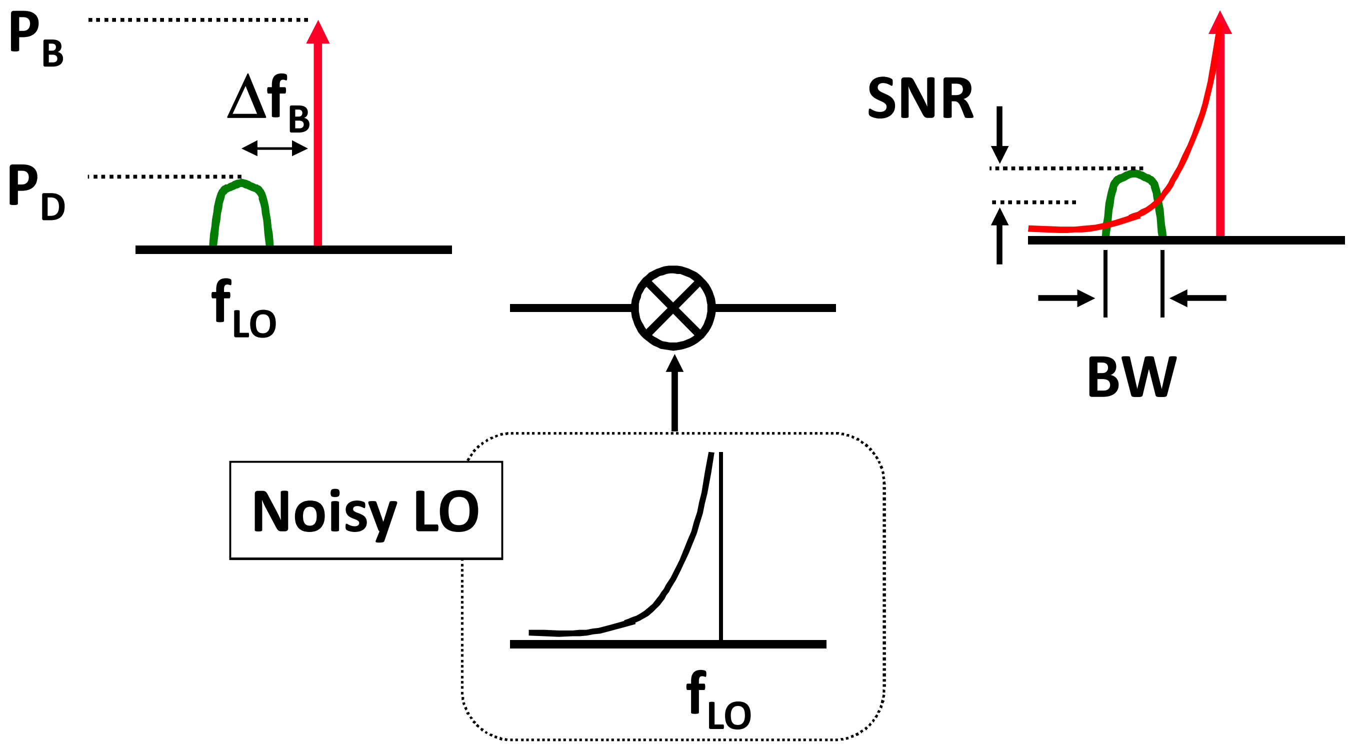
Blockers: In/Out-Band

- Small signal linearity:
  - IIP_2, IIP_3
- Large signal linearity:
  - Gain compression
- Reciprocal mixing
- Harmonic mixing



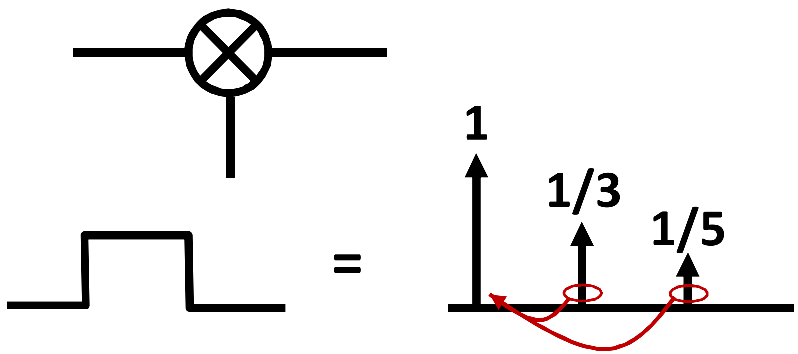


Reciprocal Mixing

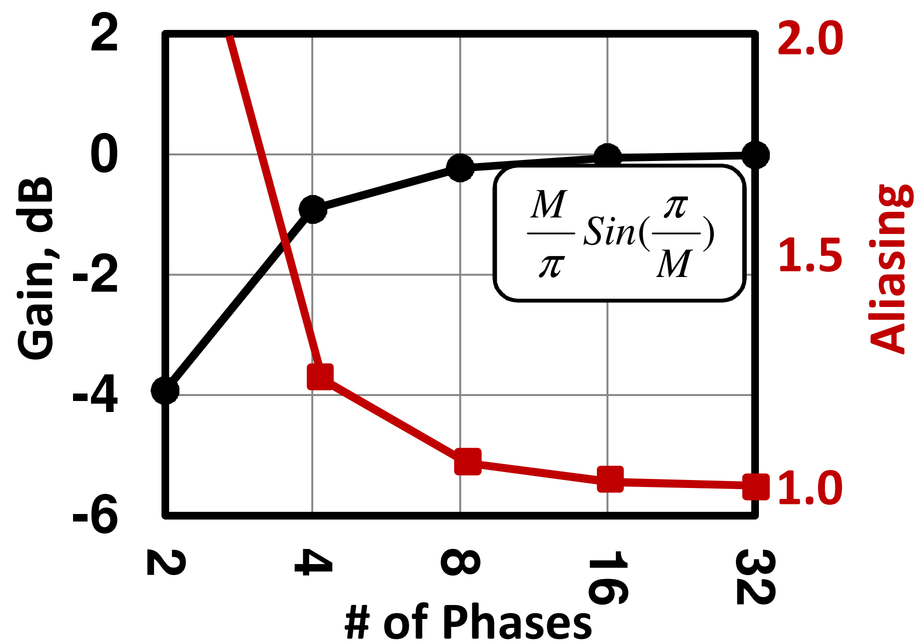


- $P_B + PN(\Delta_B) + 10 \times LOG(BW) = P_D - SNR$
- $BNF = 174 + PB + PN$

Harmonic Rejection & Aliasing in Mixers



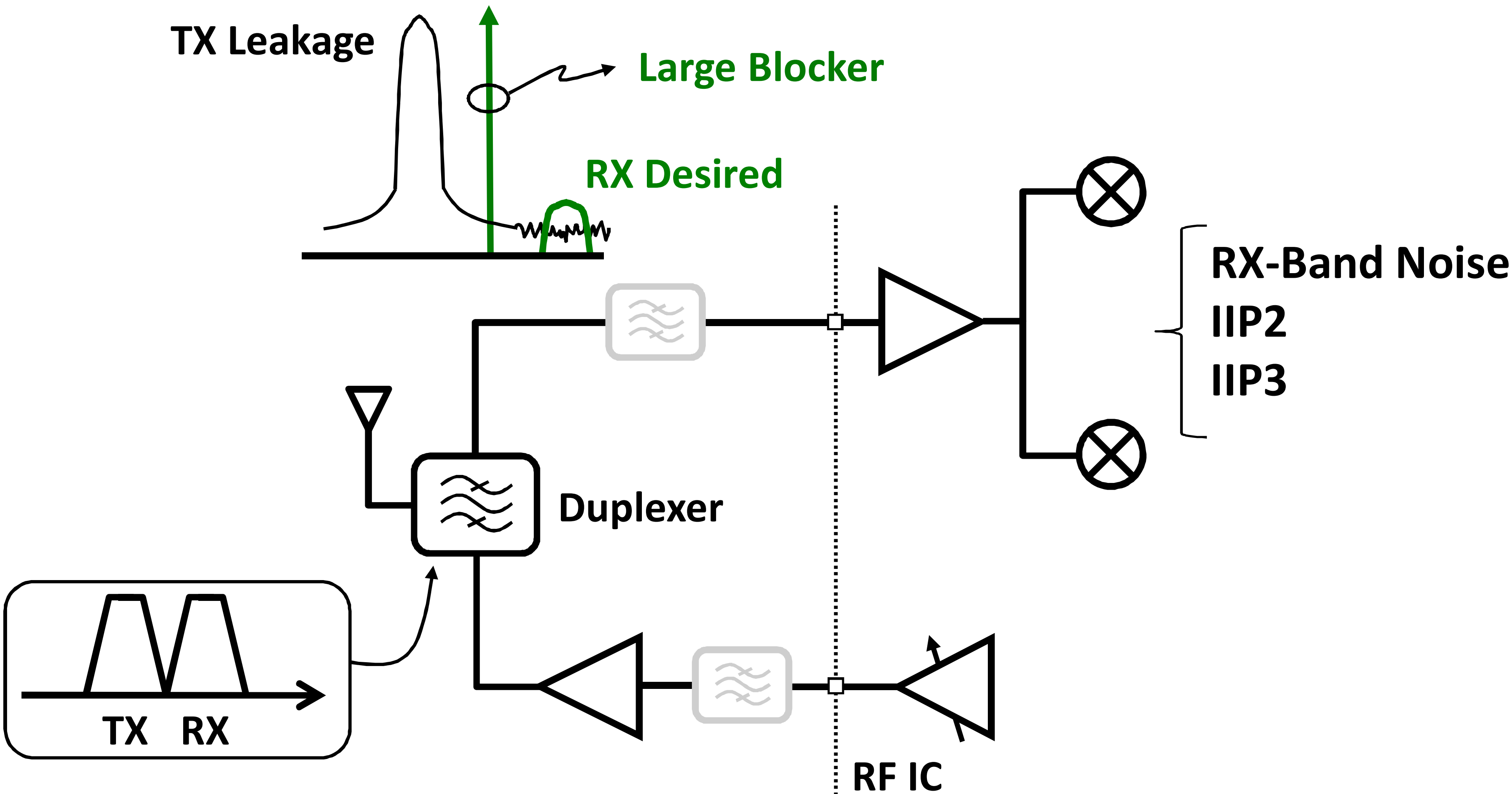
Aliasing = $1+1/3^2+1/5^2+\ldots = \pi^2/2$



- **Square-wave LO harmonically rich**
- **More phases alleviates the issue**
- **More energy in main, less in higher harmonics**

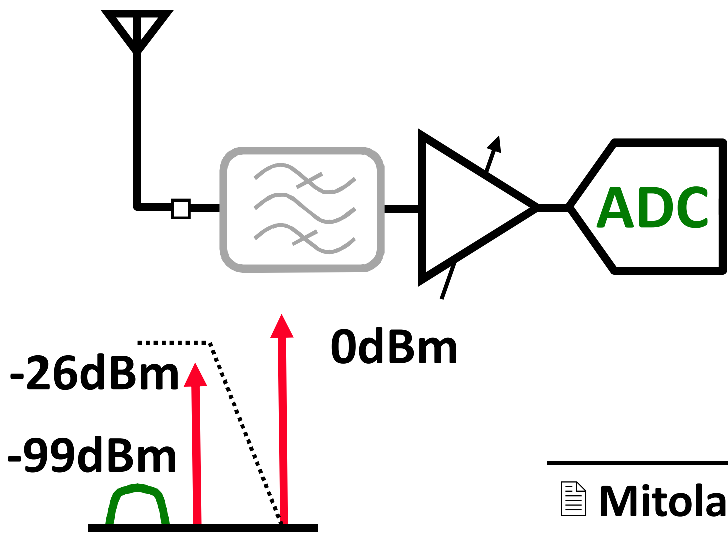
Weldon, JSSC 2001

3/4G Full-Duplex Problem

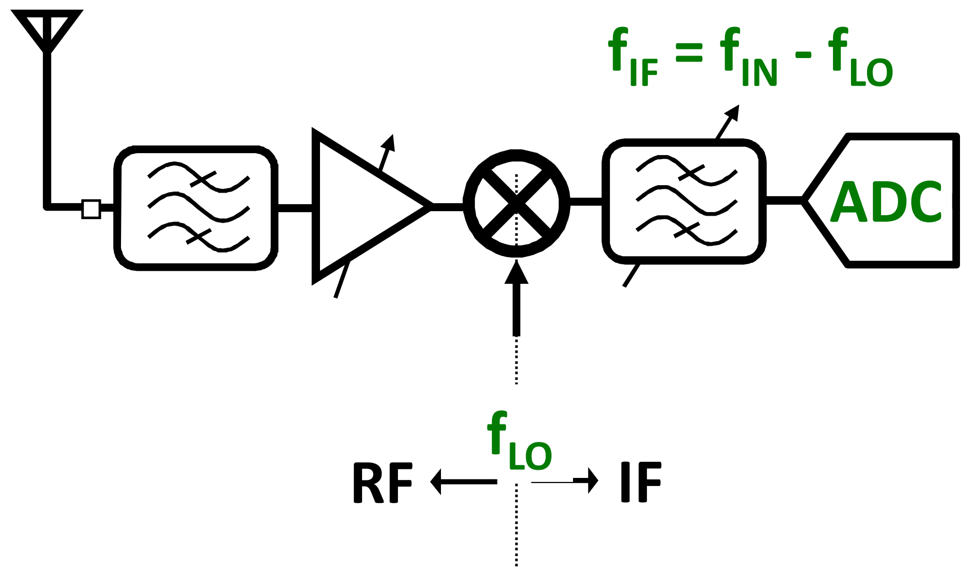


- Duplexer is a dual-band filter
- Similar issue due to co-existence

Ideal Receiver



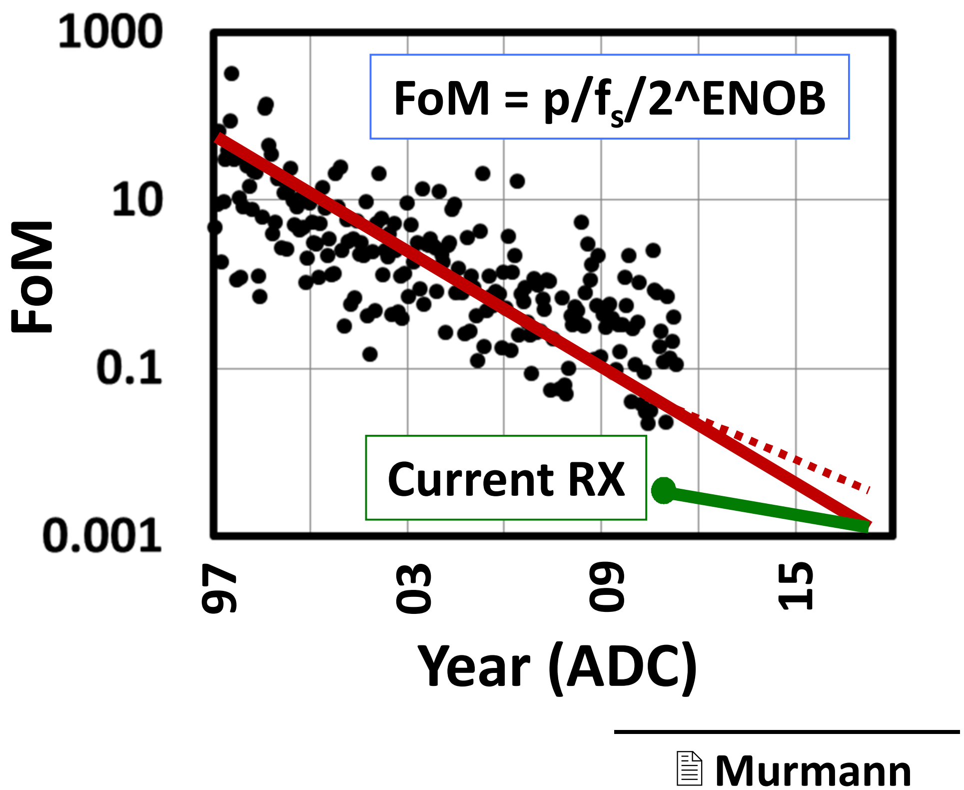
Mitola 1995

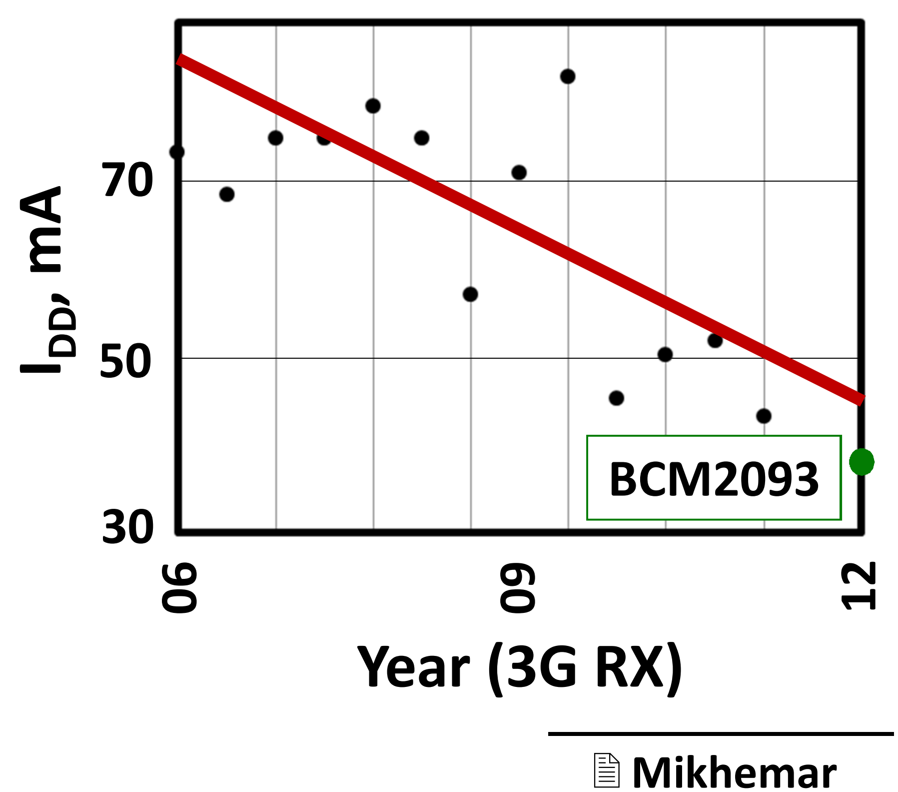


- **Filter only rejects out-of-band blockers**
- **In-band blockers require a high-resolution ADC**
- **Power hungry**

- **Invented by Armstrong in 1918**
- ***Down-conversion* relaxes IF signal processing**
- **Lower power**

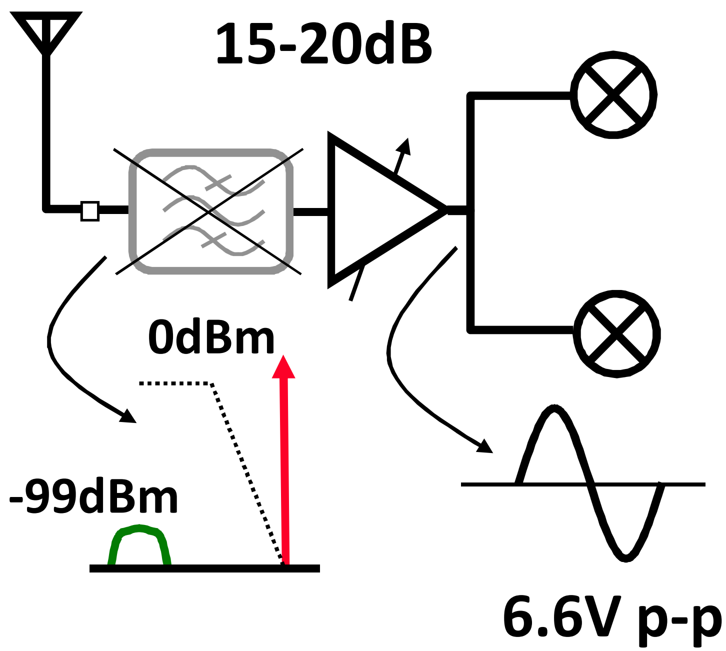
Ideal Receiver – Challenges

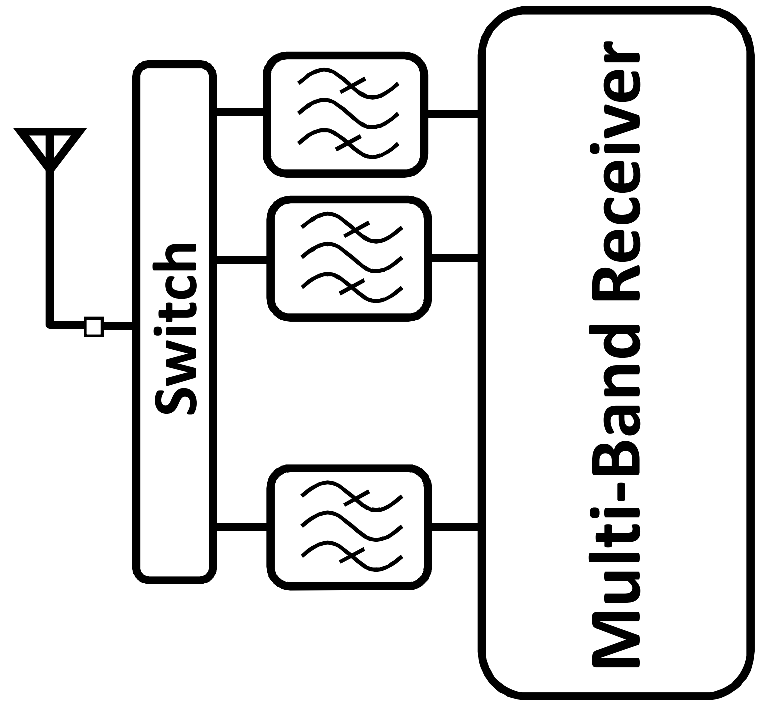




- Scalable
- Broad-band: Low-noise, Blocker tolerant
- Low-power

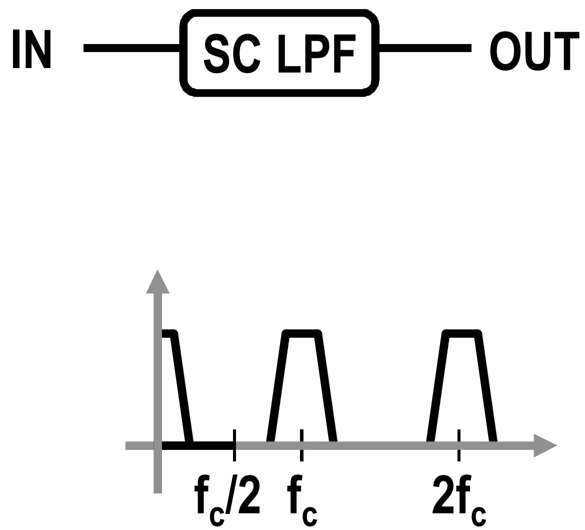
Narrow-Band Filtering Concerns

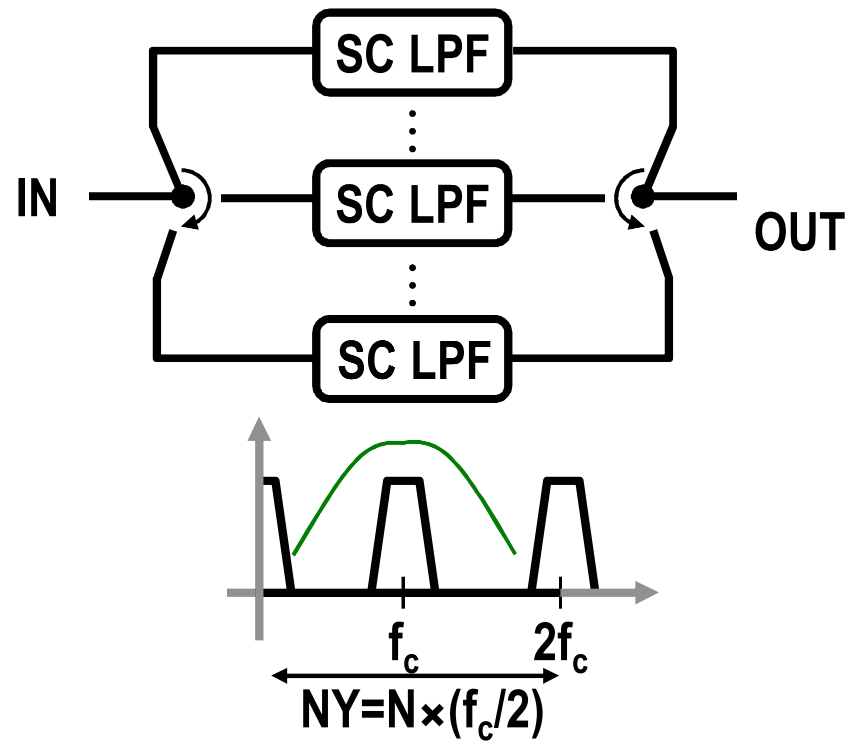




- Large blockers compress the receiver
- External filtering is narrow-band and costly

N-Path Filtering Concept



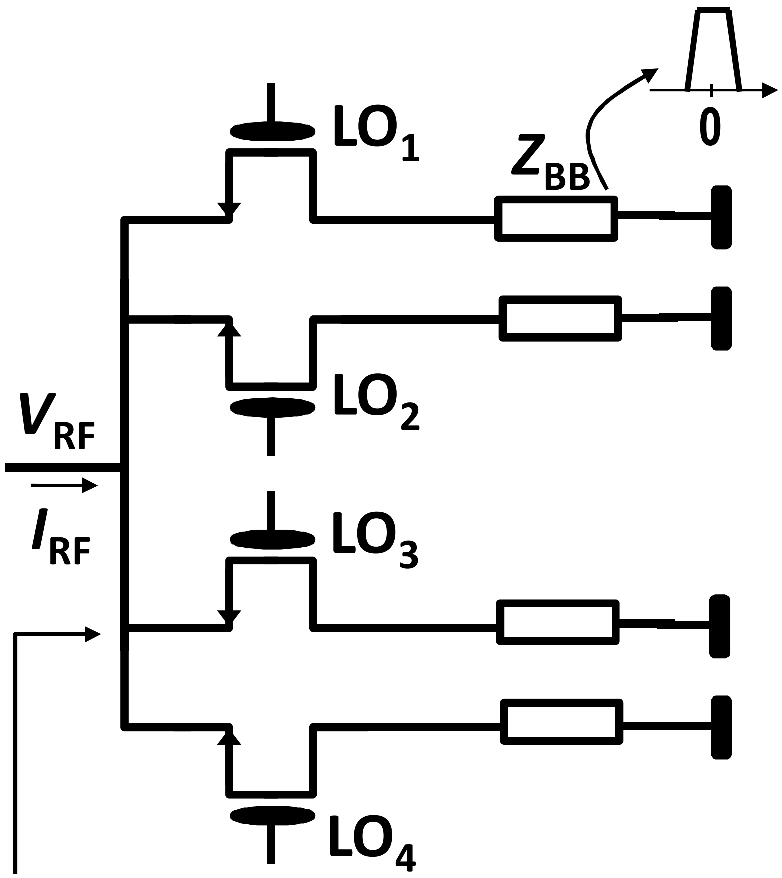


- Very high-Q passives needed
- *N-path filtering* extends Nyquist rate[1]

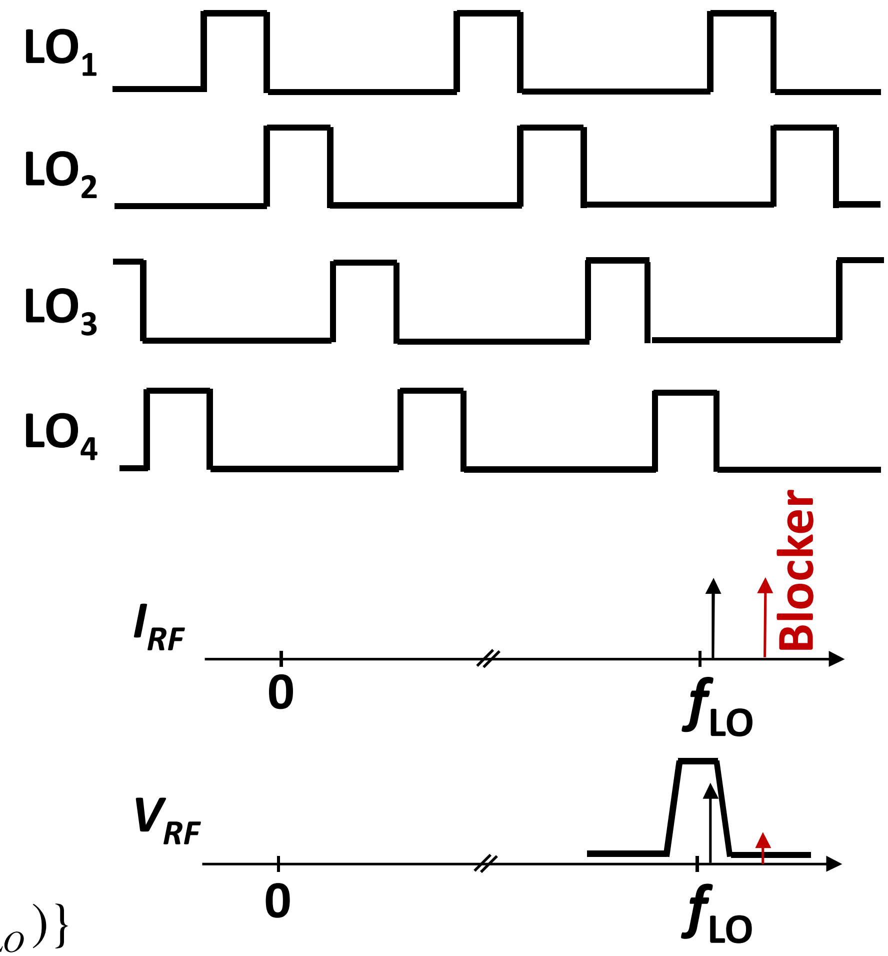
---

1. L. Franks, Bell Syst. Tech. J., 1960

Passive Mixers as High-Q Filters



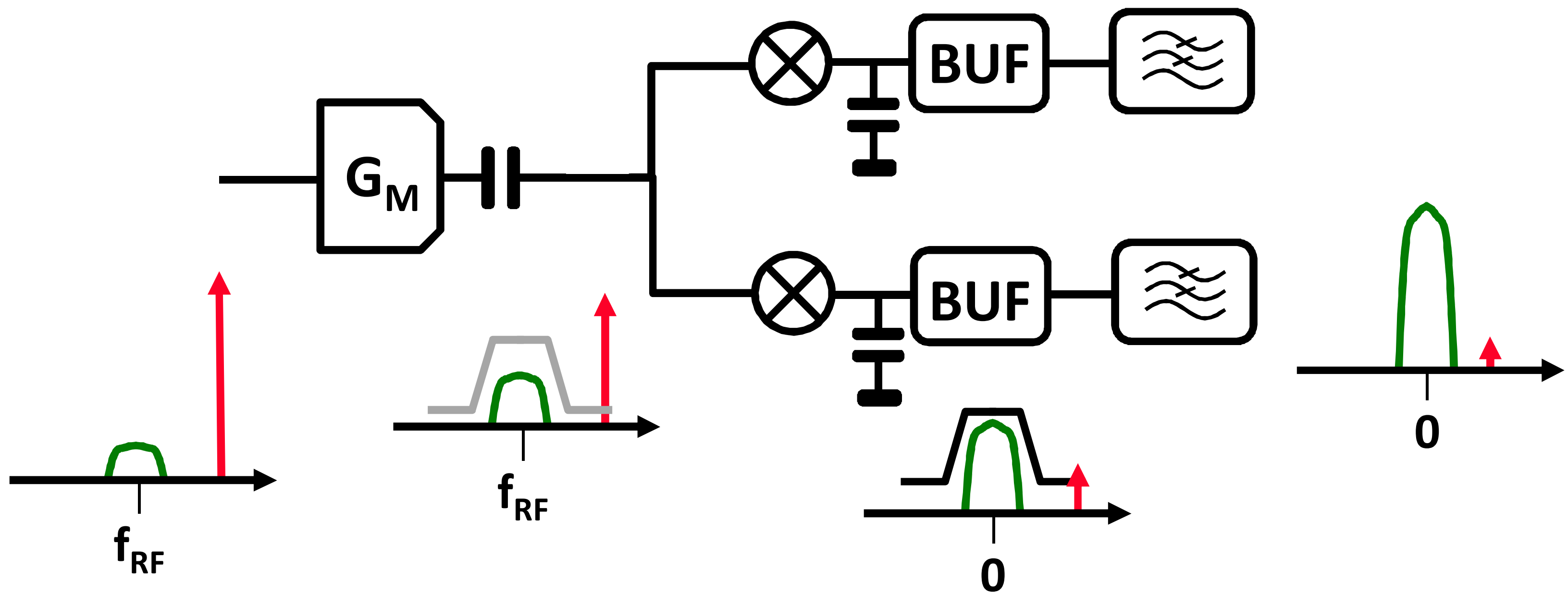
$$Z_{in}(s) \approx R_{SW} + \frac{2}{\pi^2}\{Z_{BB}(s - j\omega_{LO}) + Z_{BB}(s + j\omega_{LO})\}$$



High-Q BPF from low-Q LPF

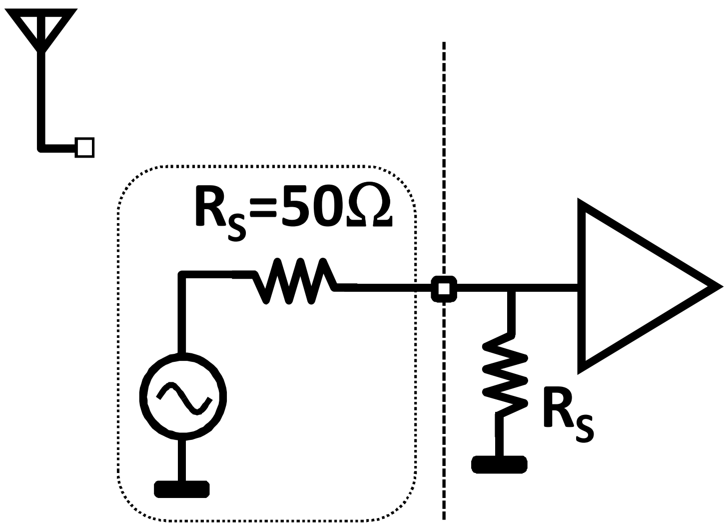
Mirzaei, TCAS 2010

Current-Mode Receivers

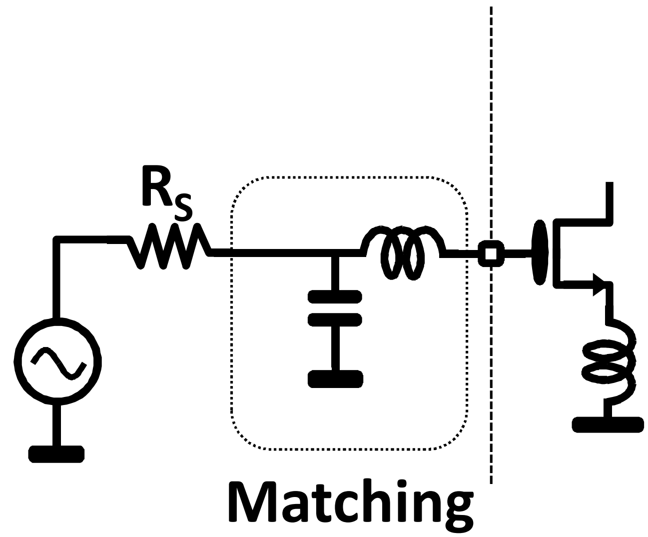


- Passive mixers to achieve high-Q filtering
- Current mode LNA: LNTA
- Enhance the blocker tolerance

Front-End Matching Concerns



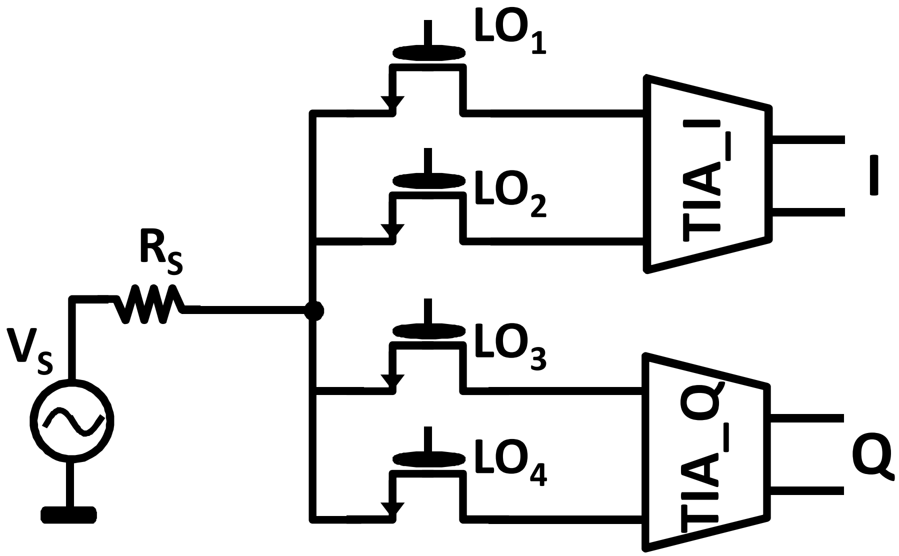
NF > 3dB

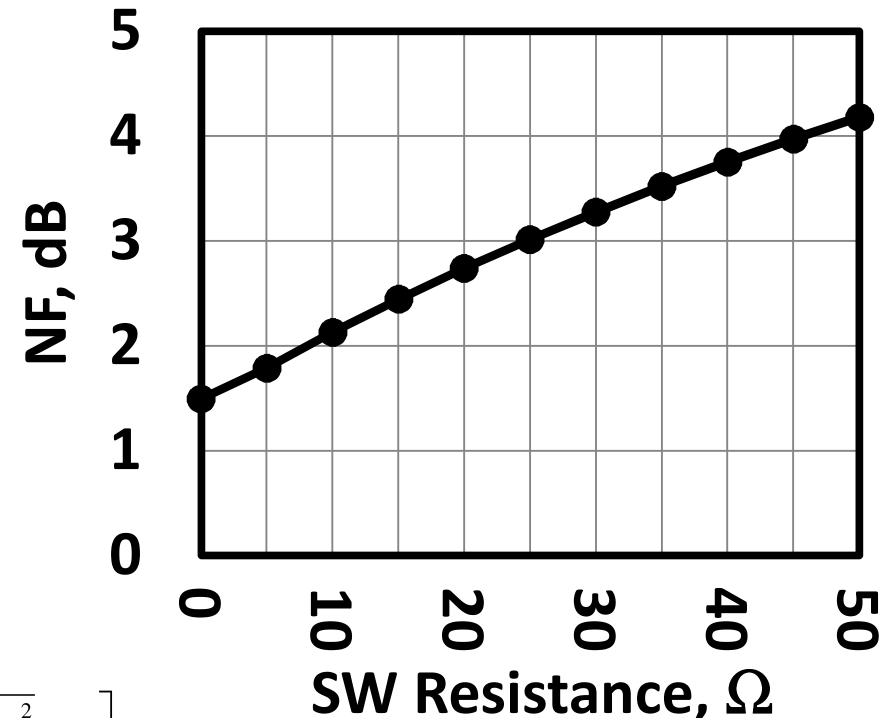


- Wide-band matching
- Good linearity
- NF suffers

- Narrow-band matching
- Good NF
- Modest linearity

Mixer-First Receivers

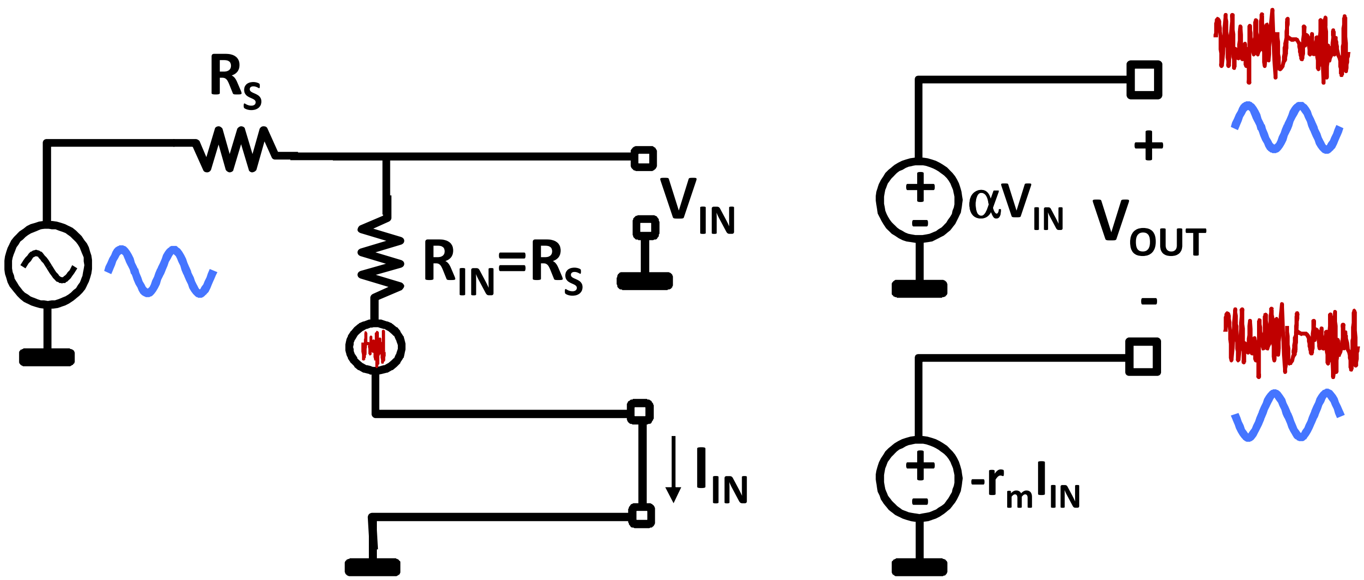




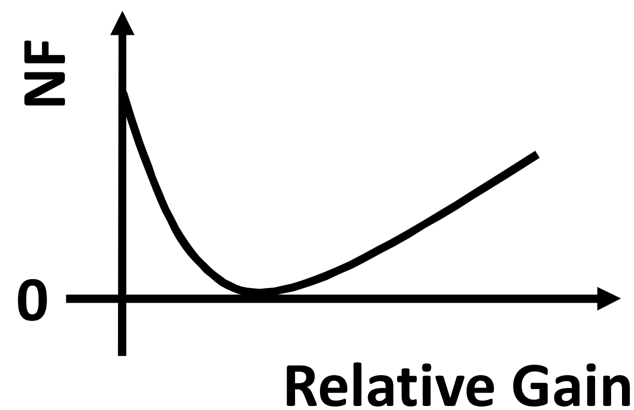
- **For M phases:** $$F = \left[1 + \frac{r_{DS}(ON)}{R_S} + \frac{\overline{v_{bb}^2}}{M(4KTR_S)}\right] \times N_{Aliasing}$$
- **N = 1 / (sinc (π/M))^2 > 1**
- **NF > 3dB in practice at GHz frequencies**

Andrews, JSSC 2010

Noise Cancelling Concept



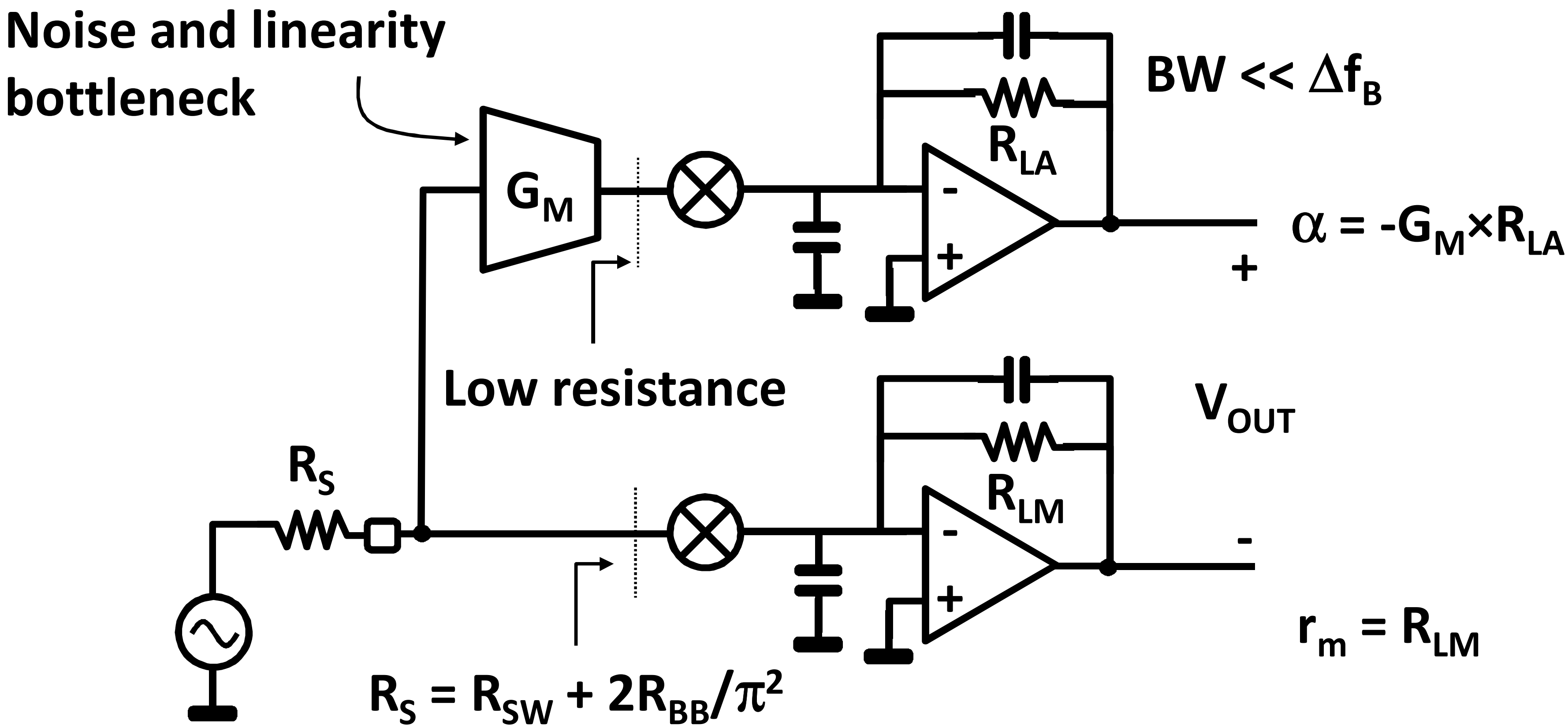
$$\underline{r_m = \alpha \times R_S}$$



- Used in broad-band LNA's
- Poor linearity

Bruccoleri, ISSCC 2002

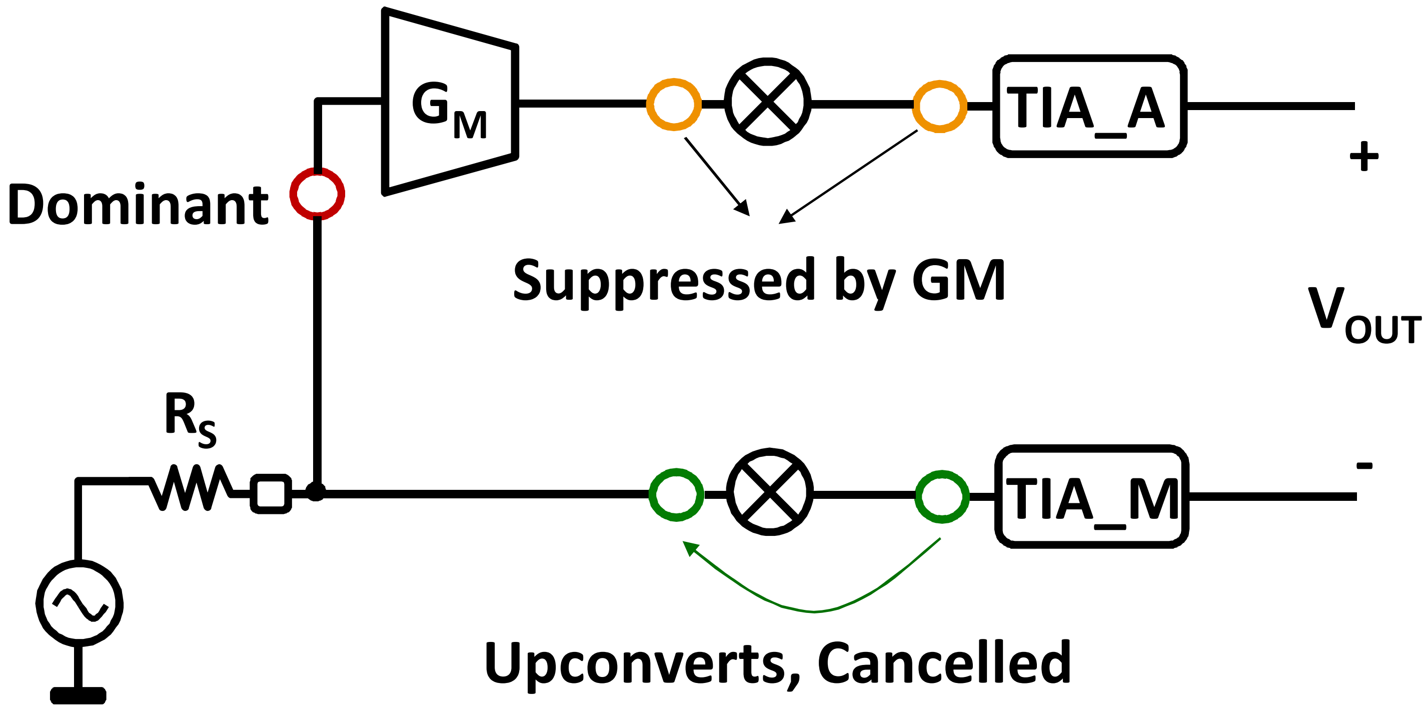
Noise Cancelling RX Architecture



- Low noise and linear
- No Balun required

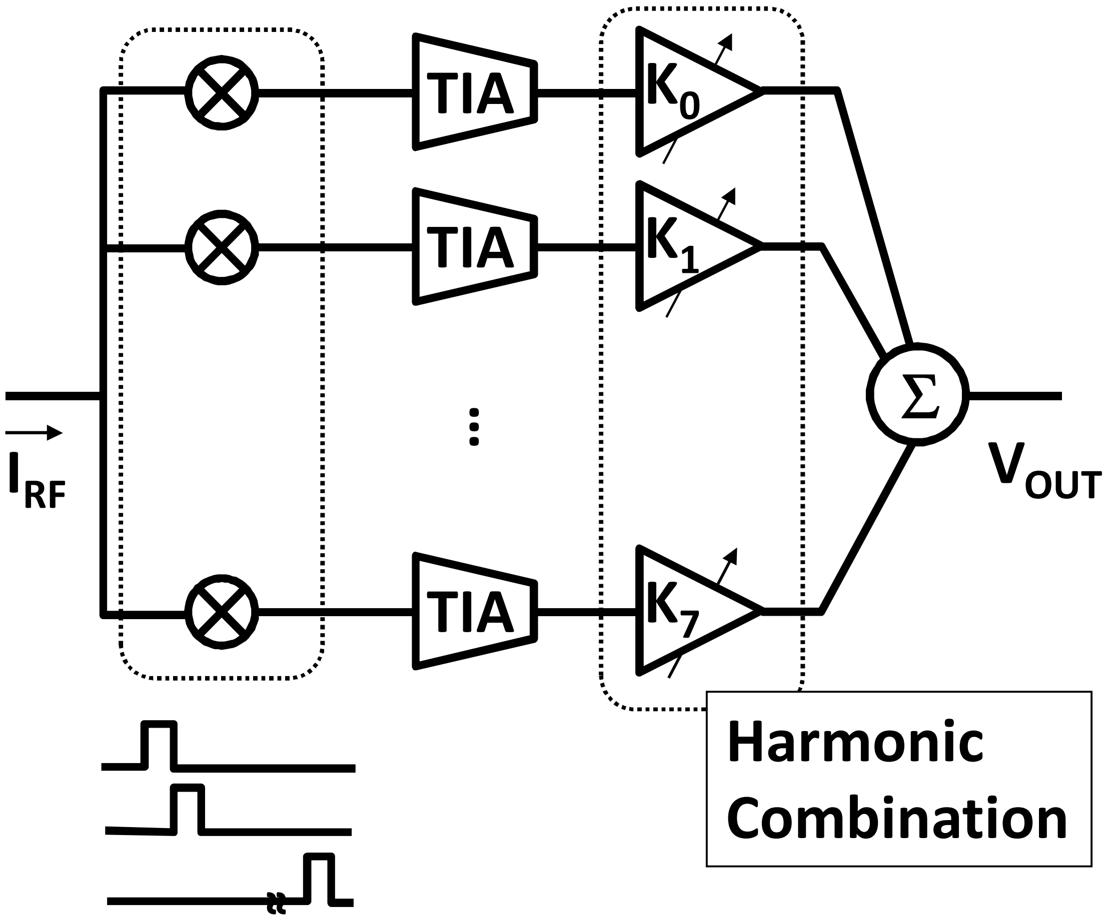
Murphy, ISSCC 2012

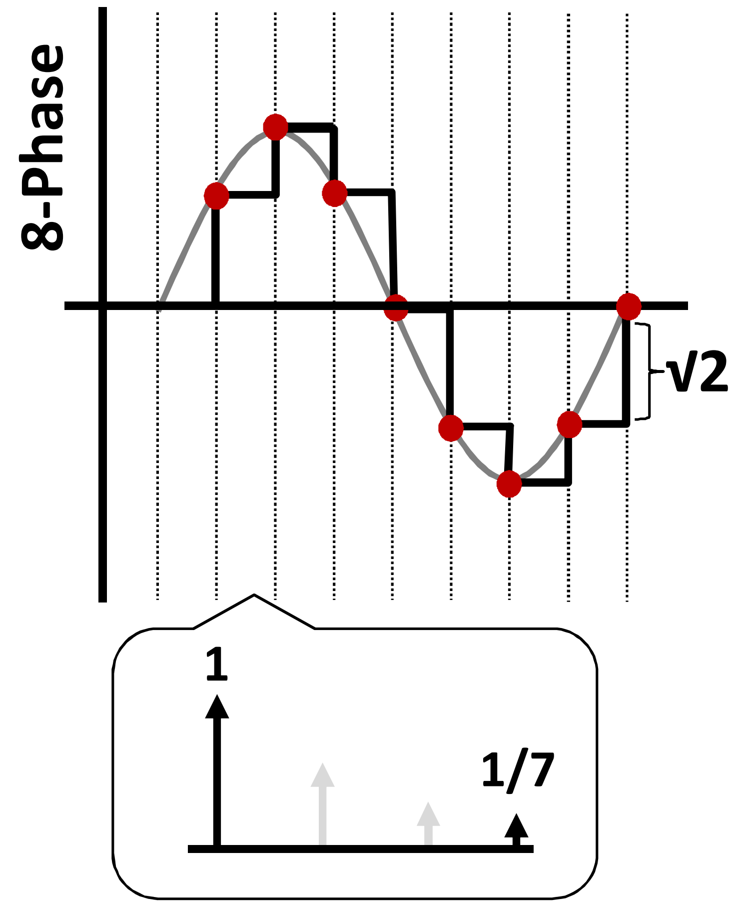
Noise & Linearity Performance of NC RX



- G_M noise dominant, no need to provide matching
  - $F \cong (1+v_{GM}^2/4KTR_S)\times N$
- Similarly main path distortion cancelled:
  - $IIP_3 \cong (1+R_S/R_{IN})^{3/2} \times IIP_{3\_AUX}$

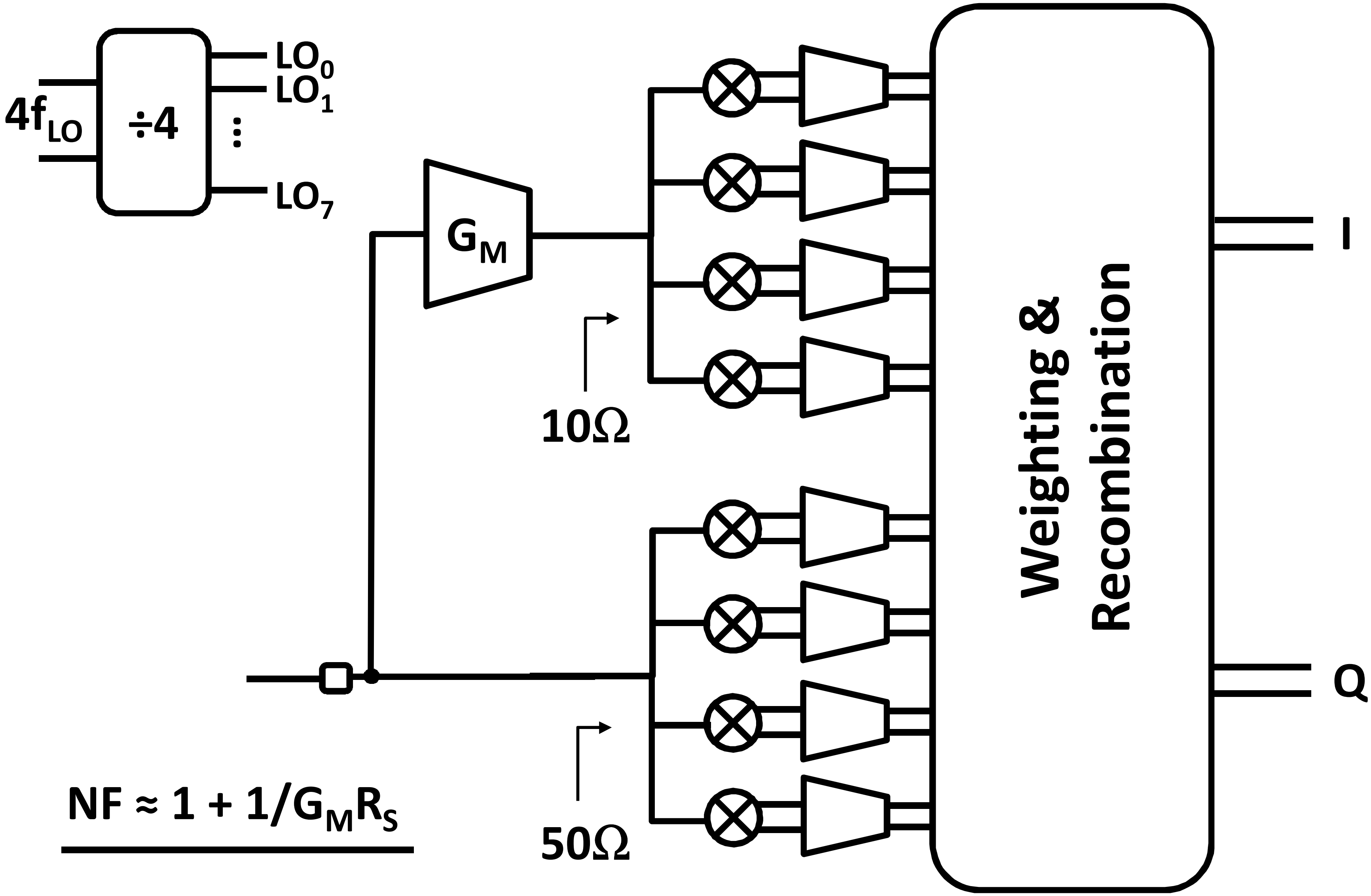
Over-Sampling Mixer Architecture





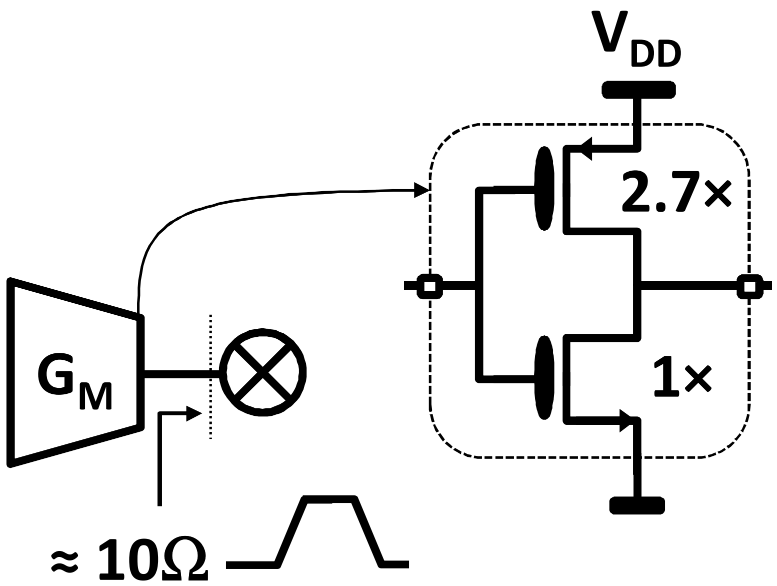
- **Synthesizes arbitrary 8-phase LO:** $V_{OUT} = i_{RF}(t)\sum_{x=0}^{7} K_x sw(t - \frac{x}{8T})$

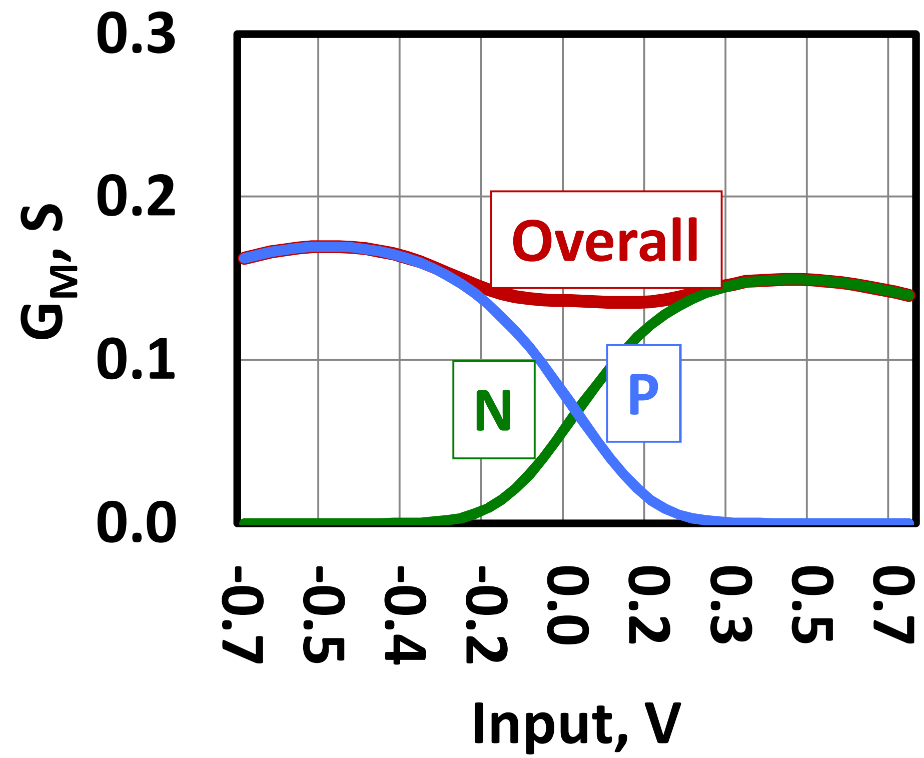
Complete NC Receiver Architecture



$NF \approx 1 + 1/G_M R_S$

RF G_M Cell

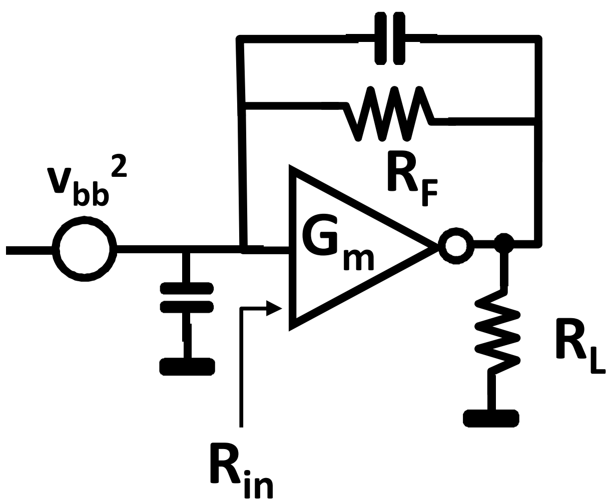


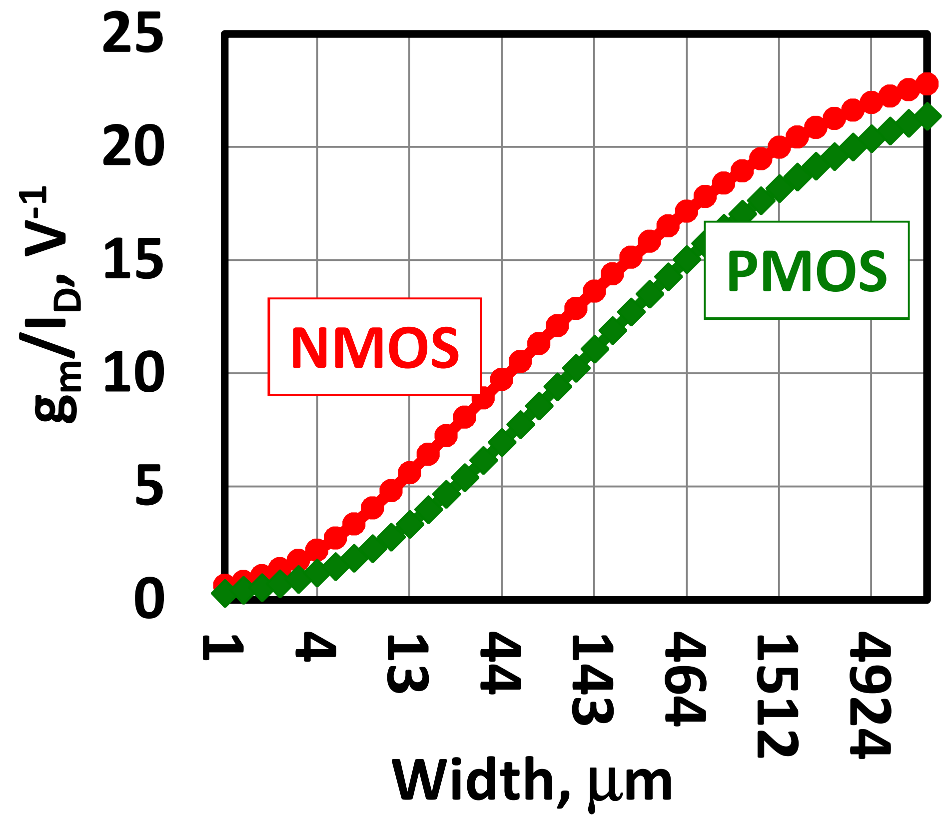


- Class AB transconductance
- Scalable
- Linear due to class AB and low-impedance loading

Baseband TIA

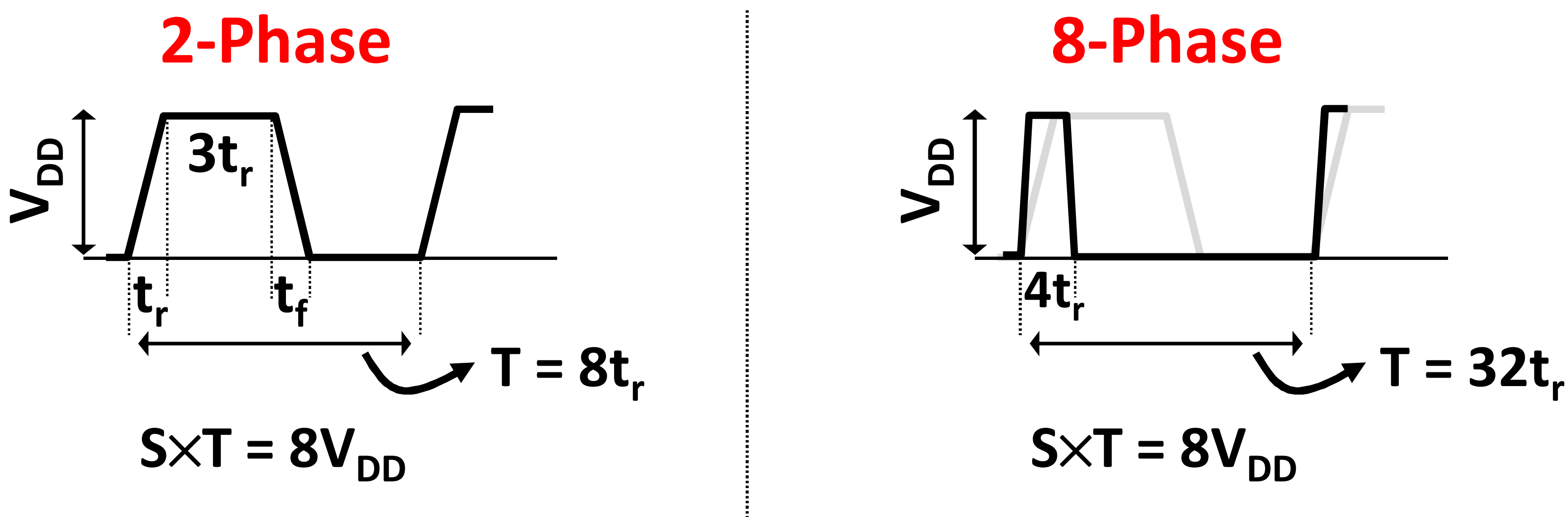
$G_m = g_{mn} + g_{mp} \approx 40 \times I_D$





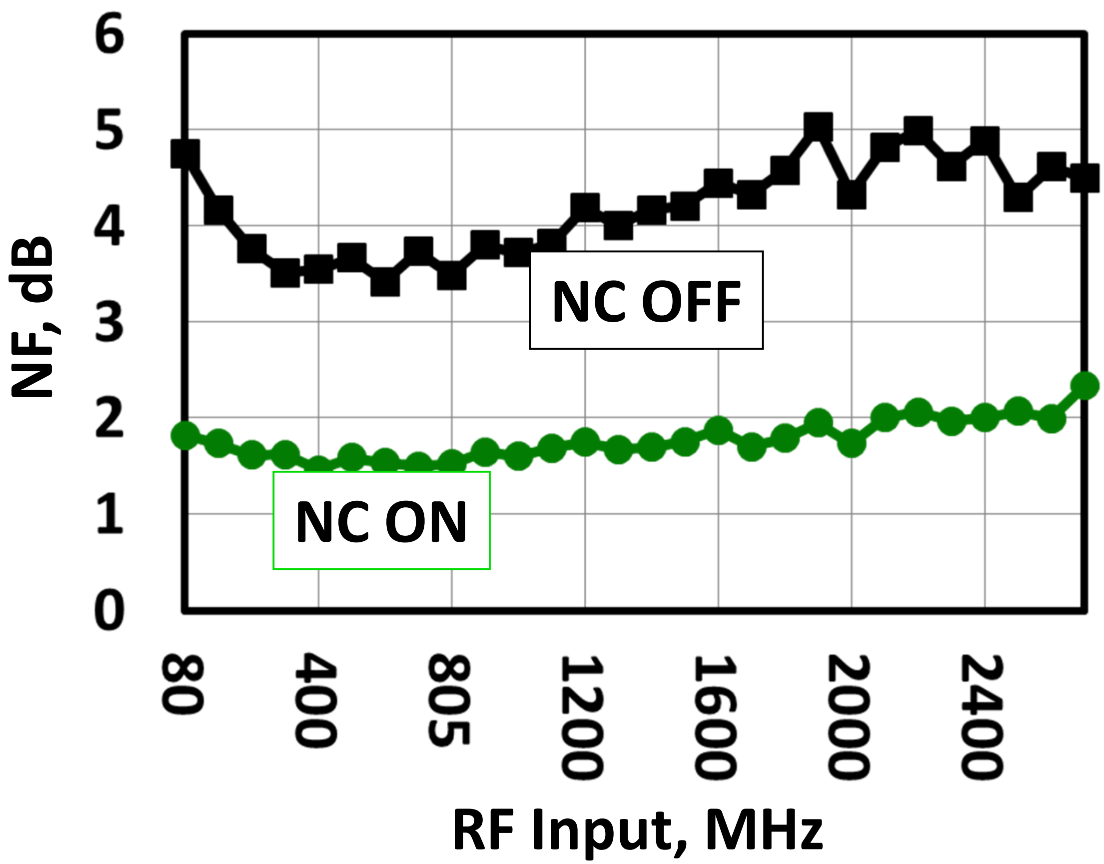
- Most power efficient
- Noise: $v_{bb}^2 \approx 4KT\gamma/G_m \approx 4KT/40I_D$
- Input resistance: $R_{in} \approx R_F / A_{OPEN} \approx R_F / (G_m(R_F \| R_L))$

Receiver Scalability



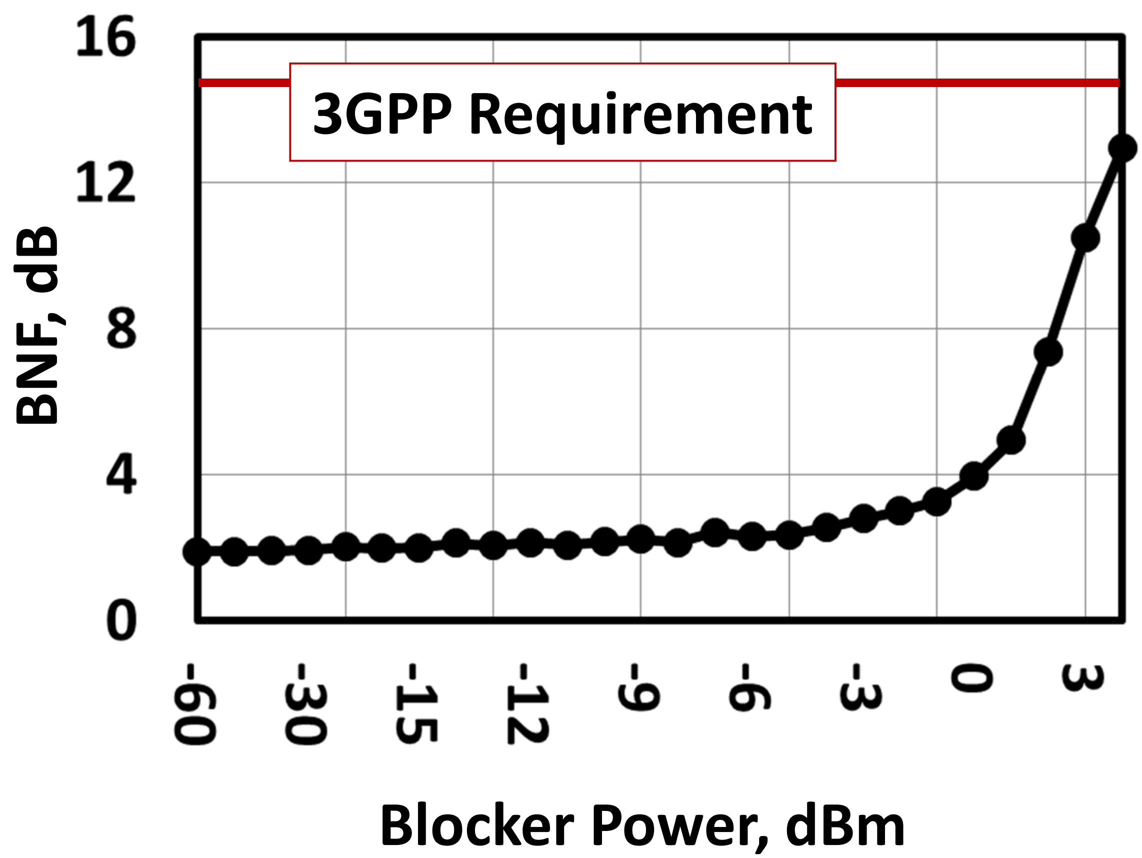
- Inherently relies on high-speed logic, switches
- In 40nm, $t_r \approx 10pS$:
  - 12.5GHz for 2-phase (overlapping)
  - 3.12GHz for 8-phase
- Scales w/ technology

Noise Figure



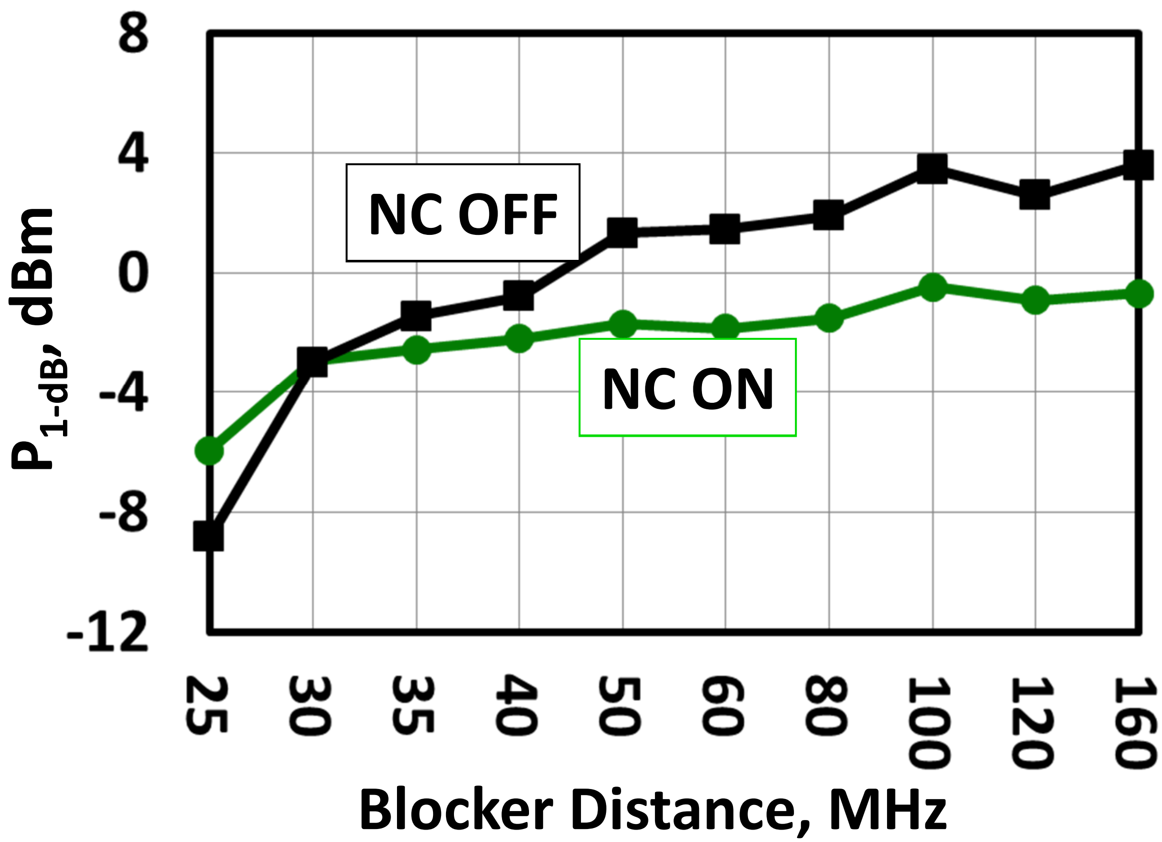
- 1/f corner reduces from 100kHz to less than 10kHz
- Corresponds to <-113dBm GSM sensitivity

Blocker Noise Figure



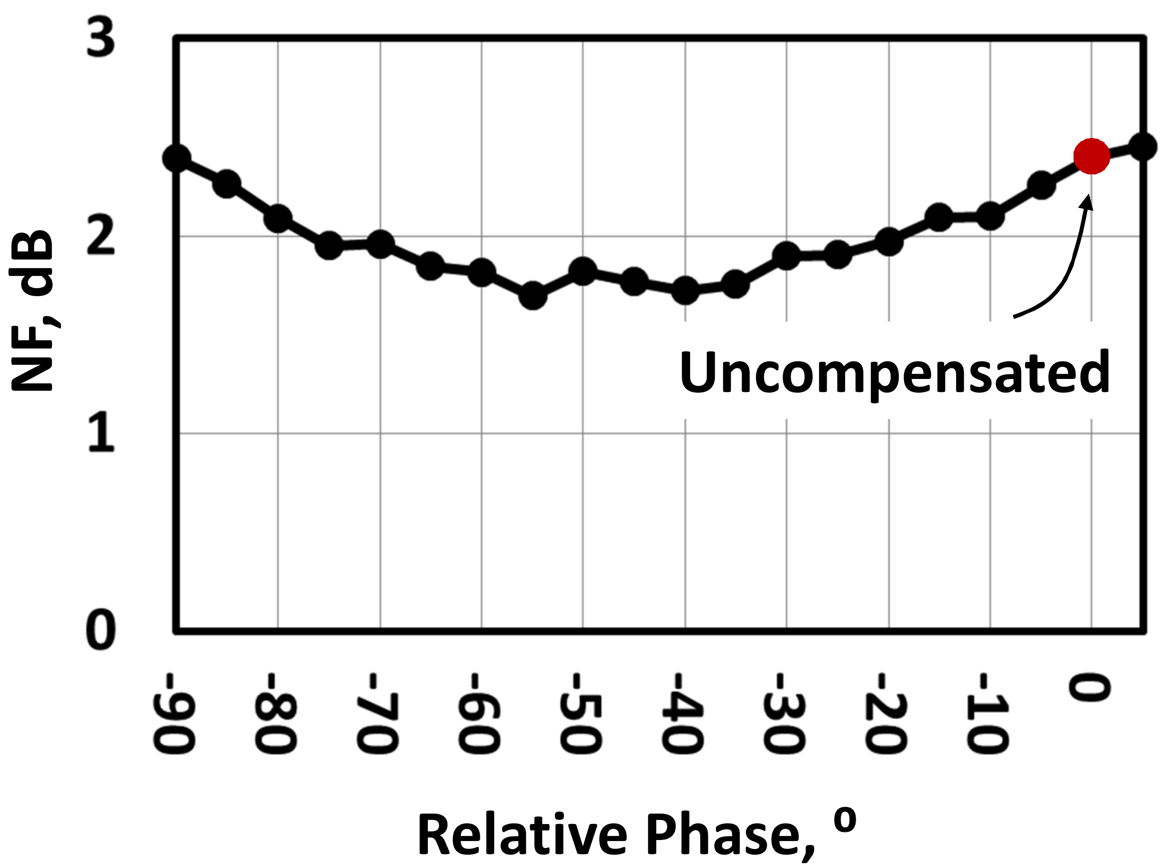
- 4.1dB 0dBm BNF, mostly limited by reciprocal mixing

Linearity



- **Close to 0dBm 1dB compression at maximum gain**

NF vs. Relative Phase Correction

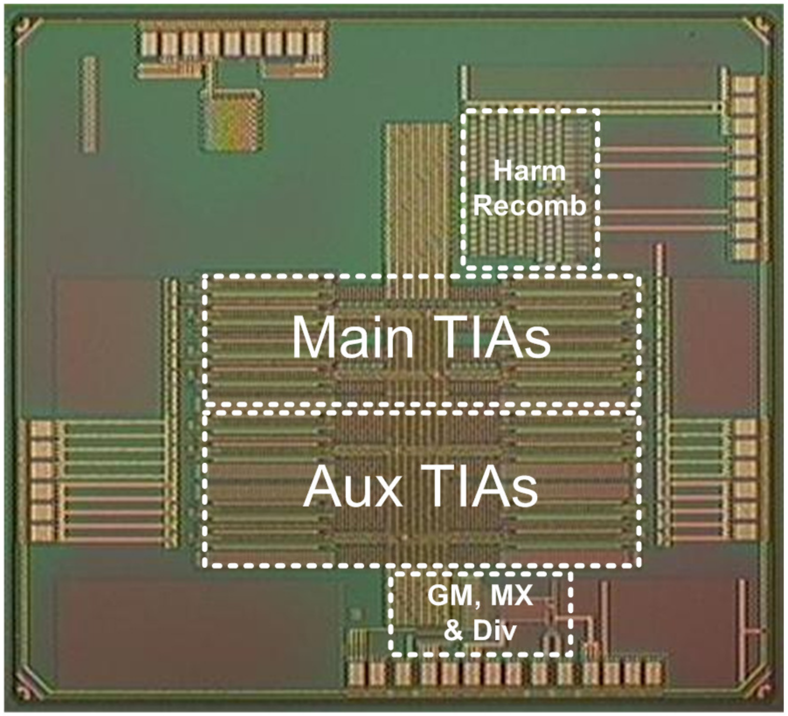


- **Robust at optimum point**

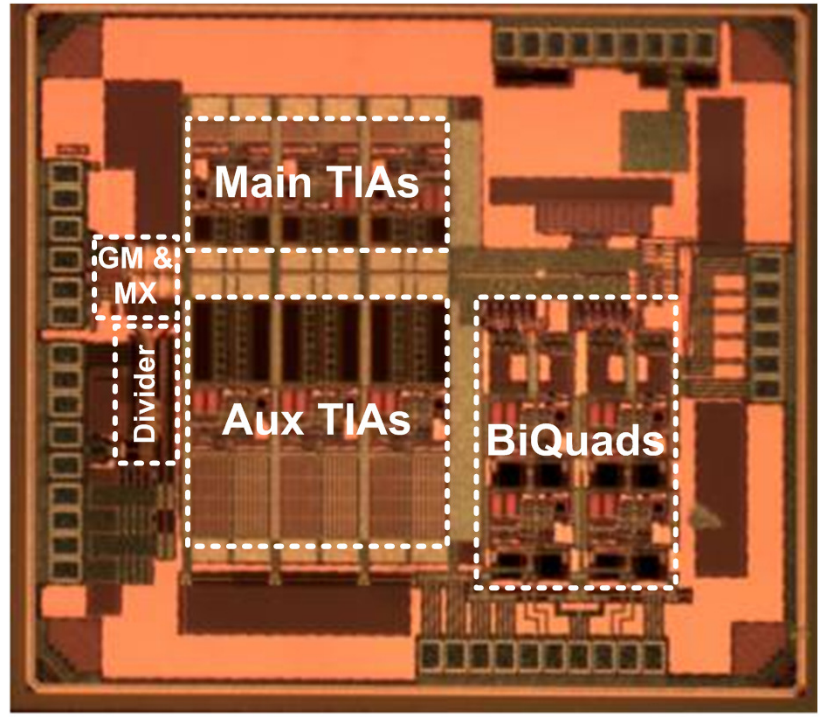
Summary of Performance

Architecture	Mixer first	NC LNA	NB SAW-Less	NC RX
RF Range	0.1-2.4GHz	0.4-6GHz	900/1800	0.1-2.7GHz
Input	SE	Differential	Differential	SE
NF at 2GHz	7dB	4.4dB	4.1dB	1.8dB
0dBm BNF	NA	13dB	7dB	4.1dB
$3^{rd}/5^{th}$ HR	35/43dB	None	None	42/45dB
OB IIP3	25dBm	10dBm	NA	14dBm
RX Current	12mA	12mA	37mA	12mA
Area	$2mm^2$	$2mm^2$	$1.4mm^2$	$1.2mm^2$
Technology	65nm	40nm	65nm	40nm

NC RX Die Photo



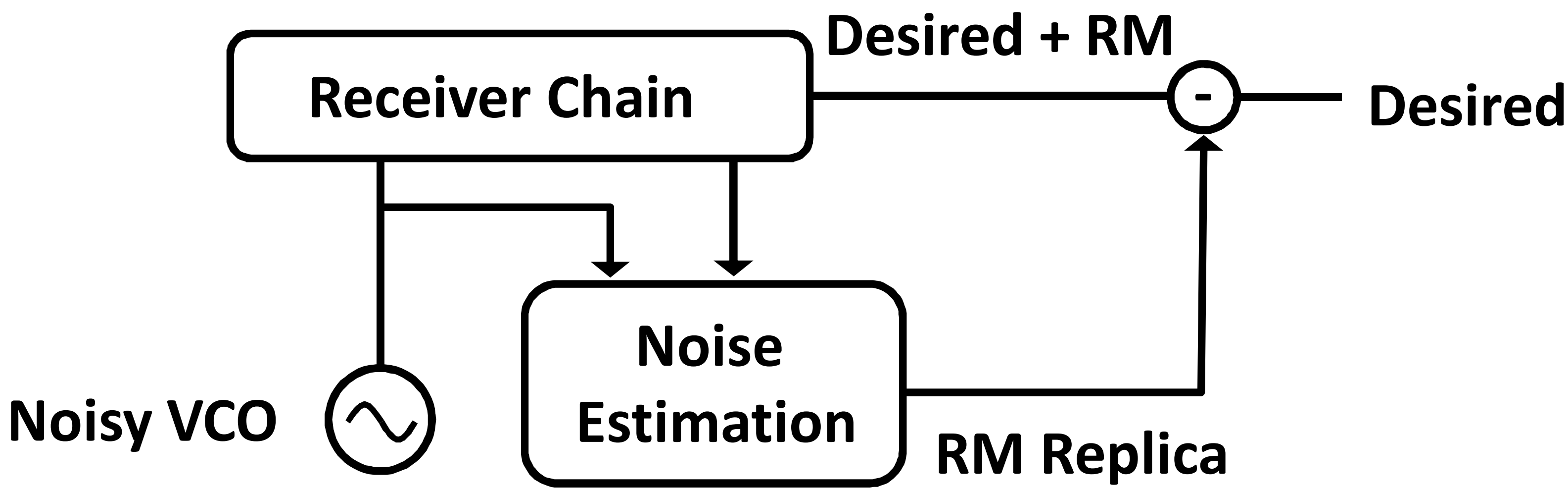
Differential



Single-Ended

- **Die area: 1.2mm^2**
- **Inductor-less**

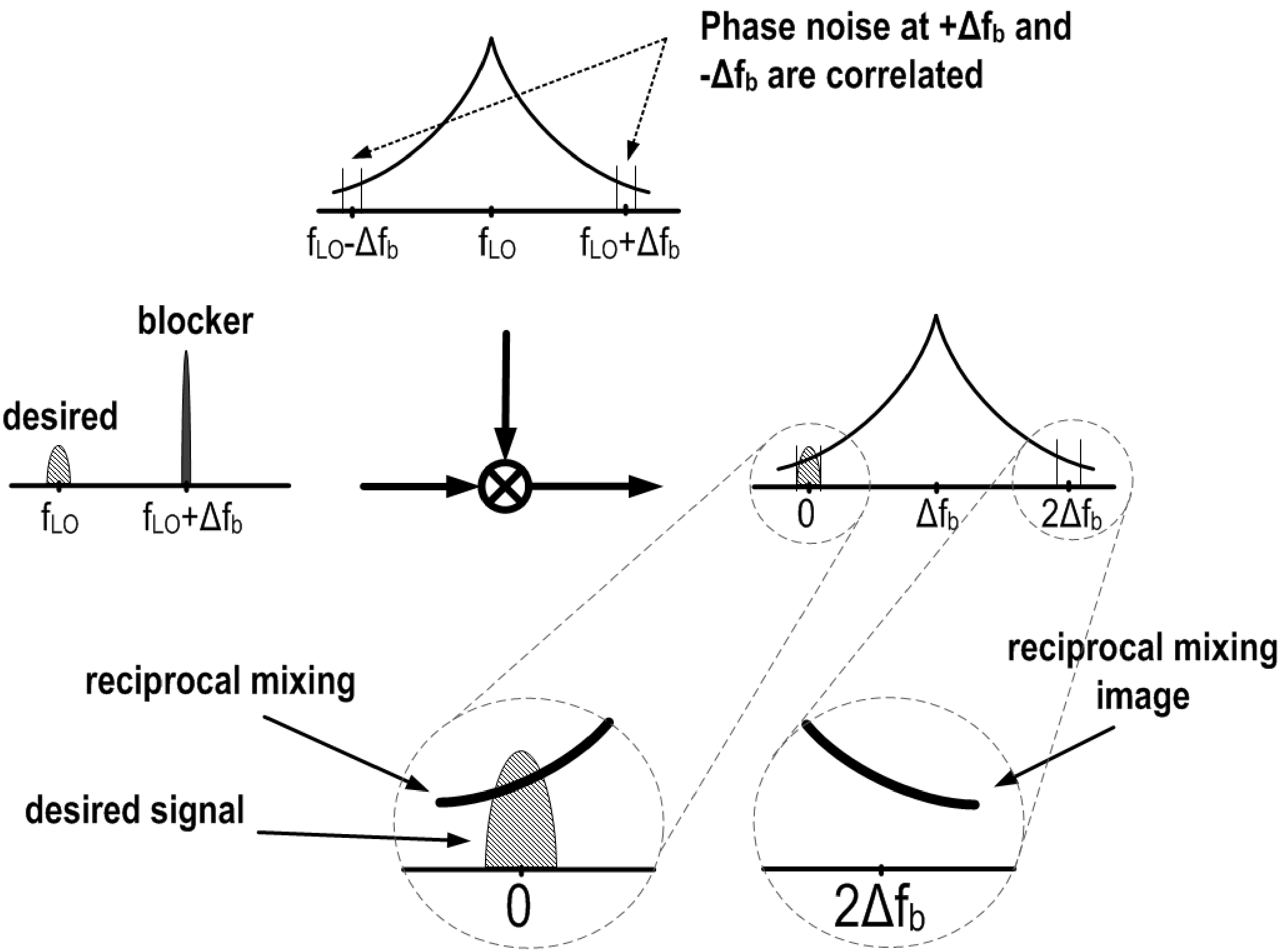
Reciprocal Mixing Issue – System Approach



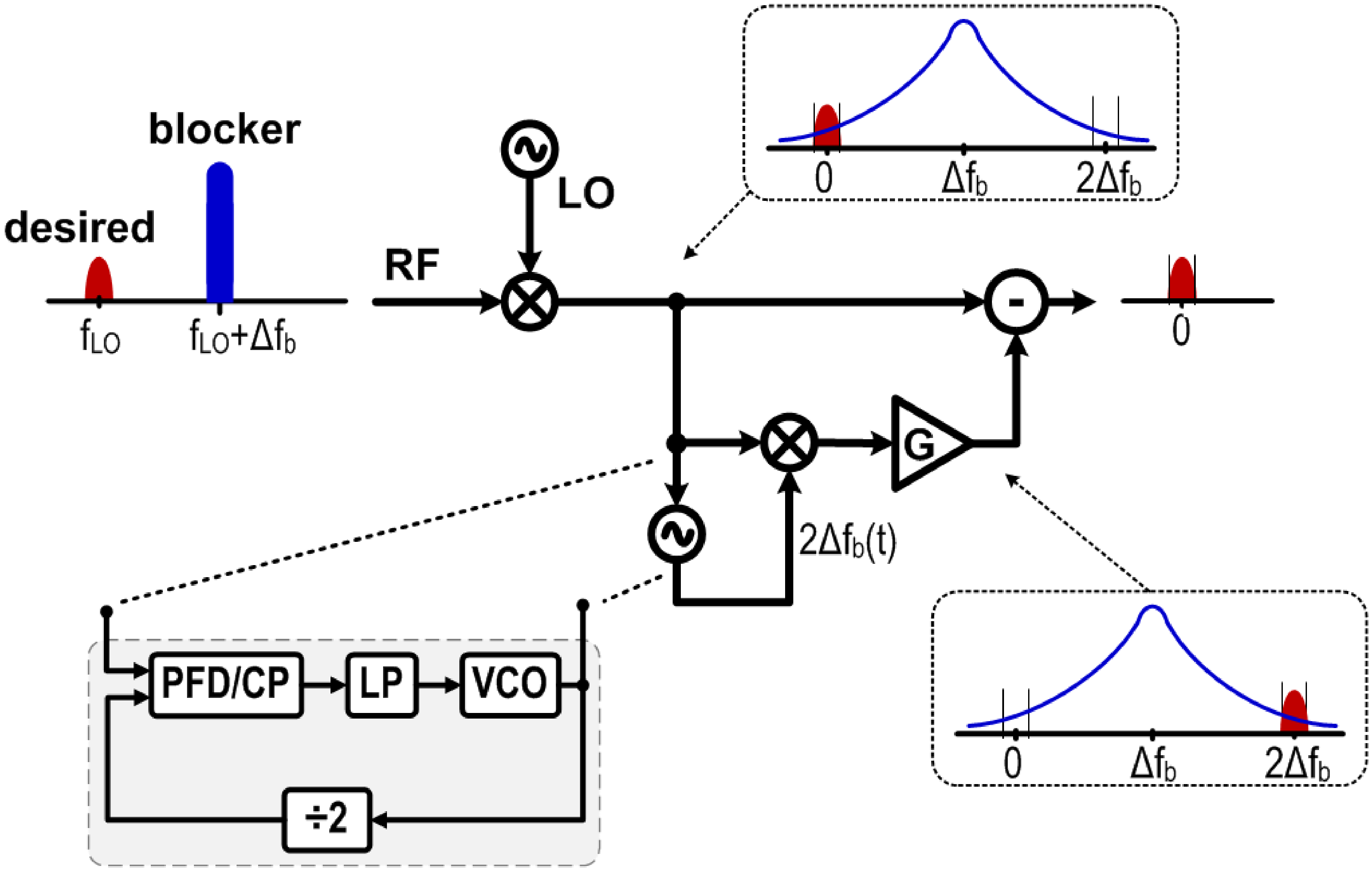
Reciprocal mixing NF = 174 – P_B -PN

- Start w/ a low-power/cost VCO
- Deal with its consequences in system level
- Proper phase noise estimation is key

Symmetry of Reciprocal Mixing



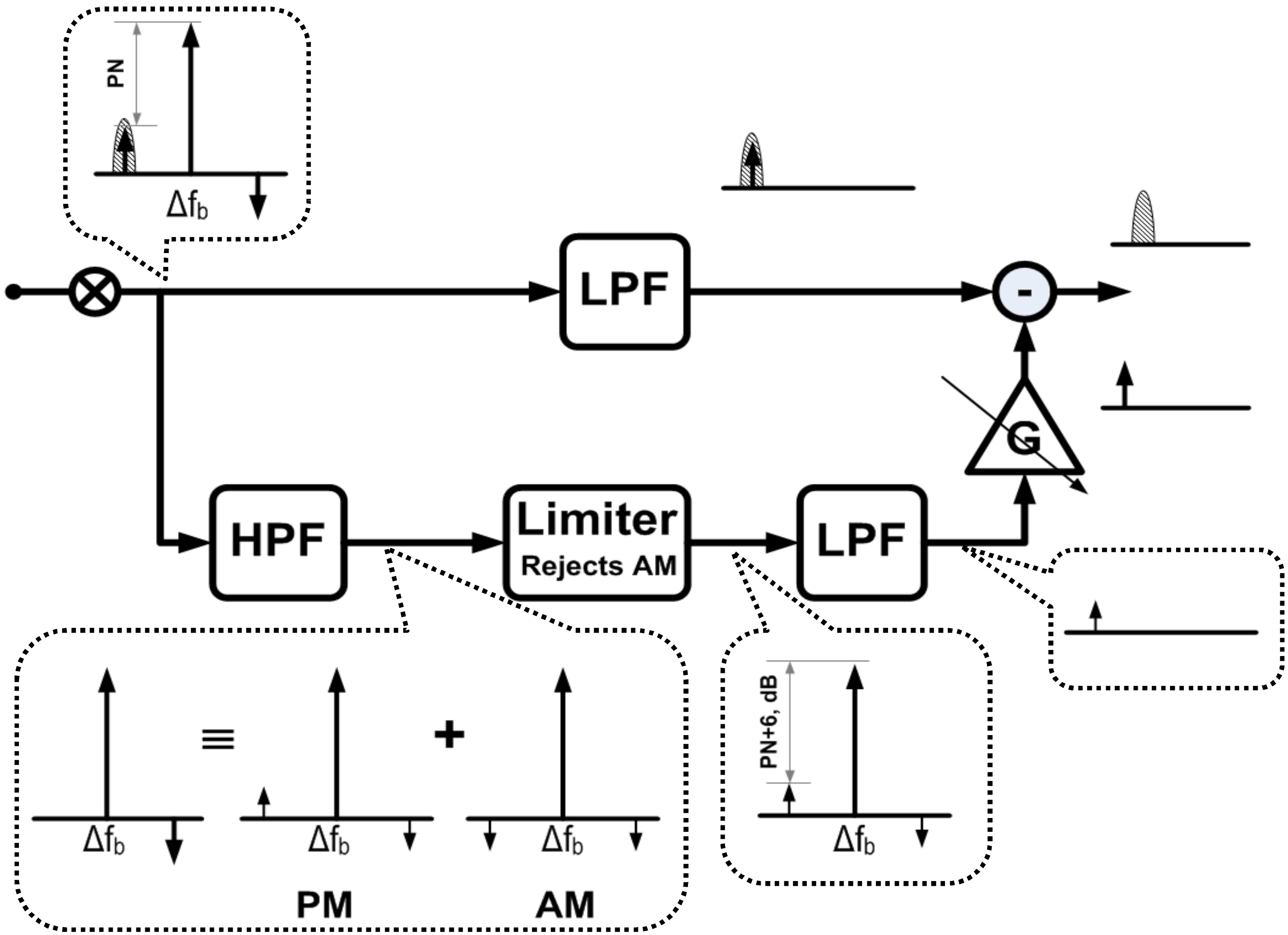
RM Cancellation Architecture



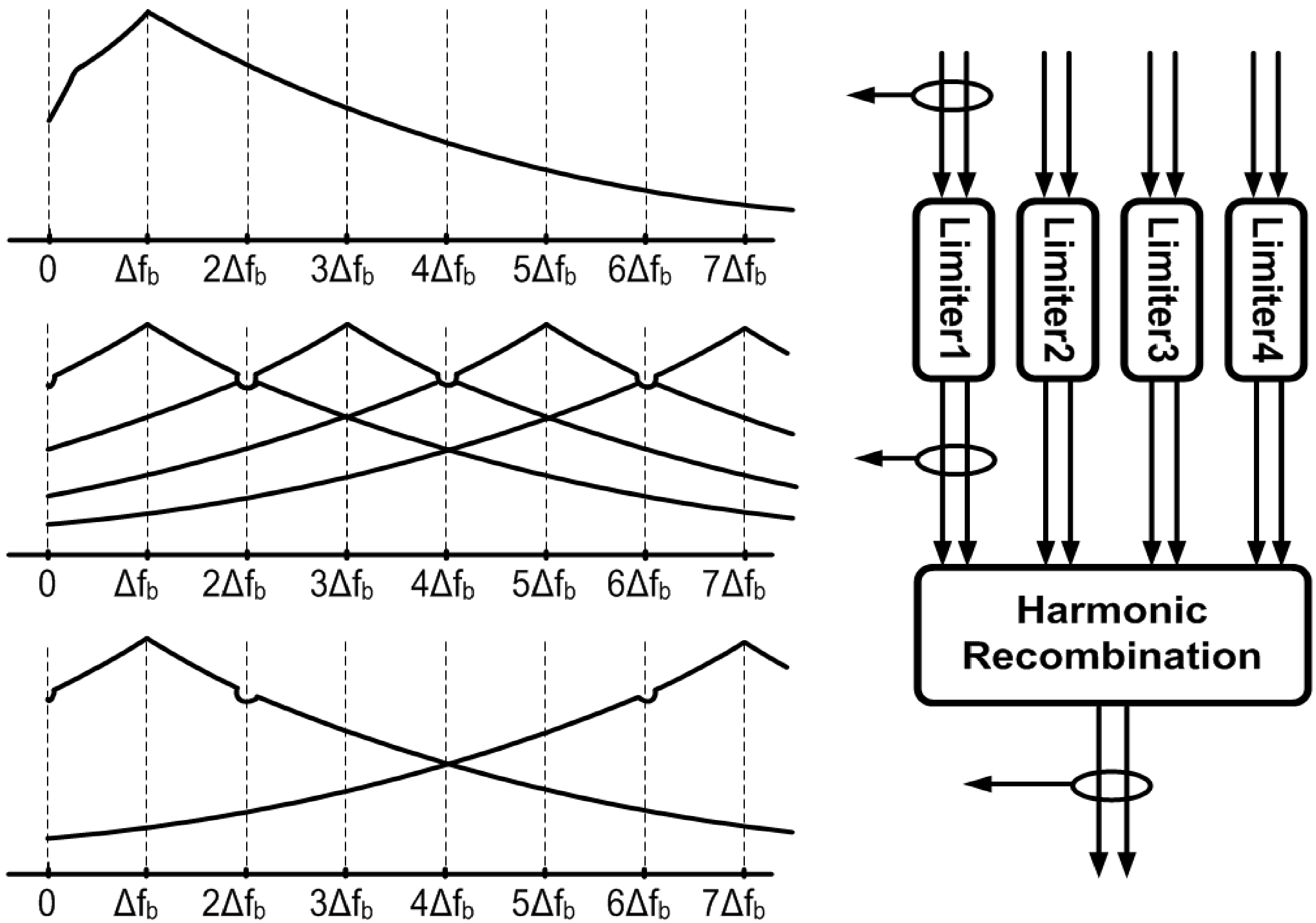
Wideband PLL

(Low Frequency & Low Power, >20dB spec relaxation)

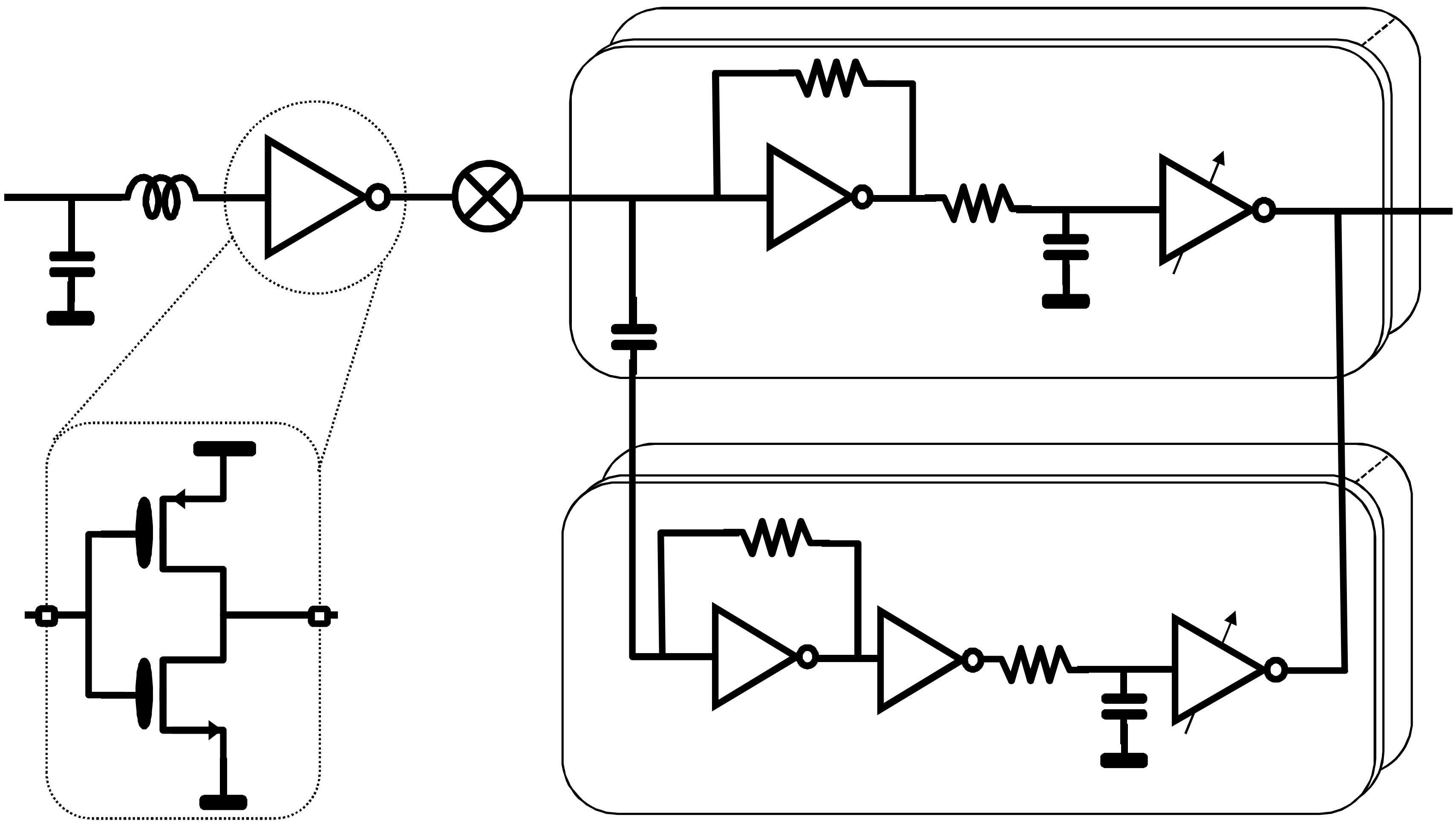
Limiter Based Architecture



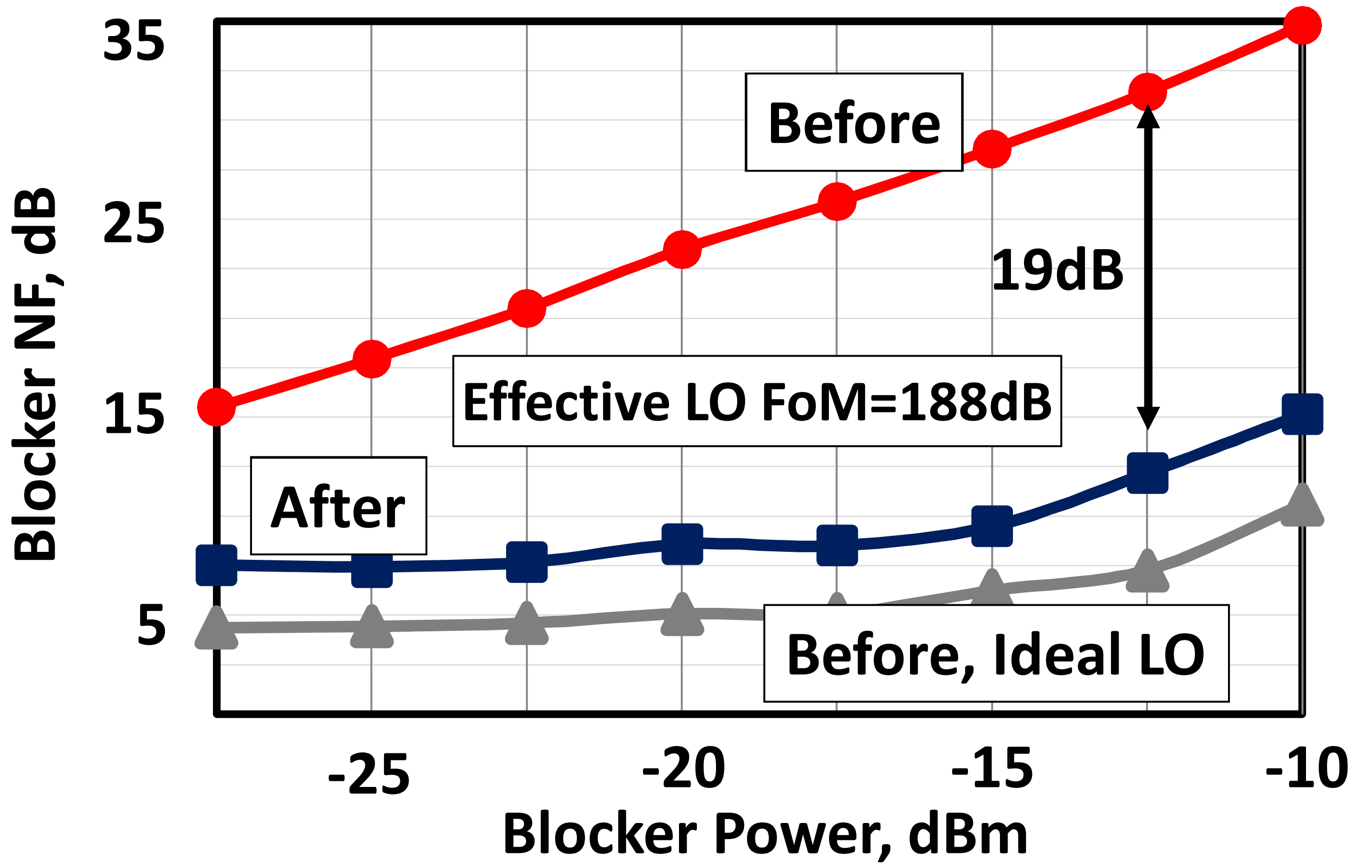
Noise Aliasing in a Limiter



Protoype RM Cancelling Receiver

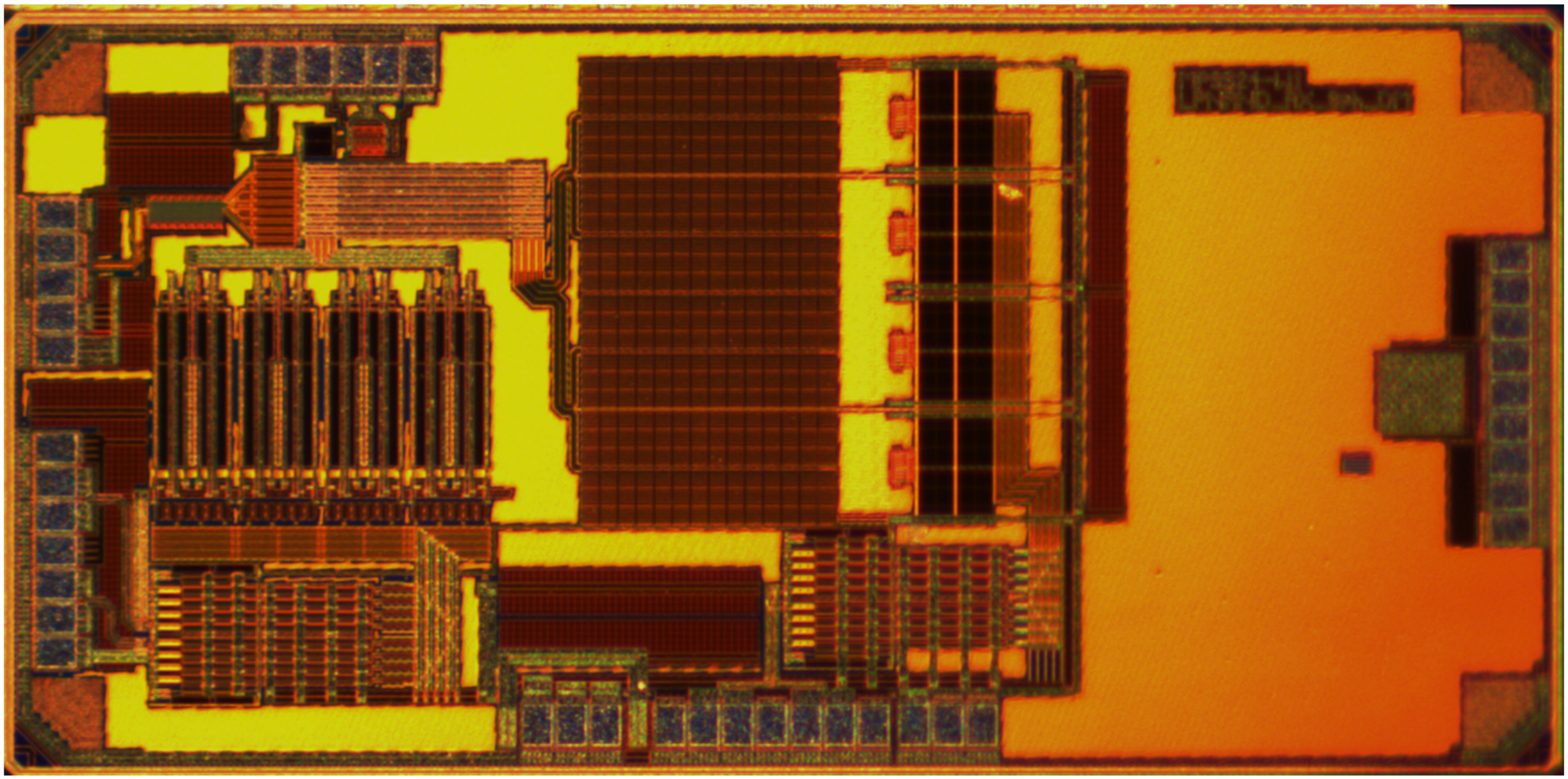


Measured Blocker Noise Figure



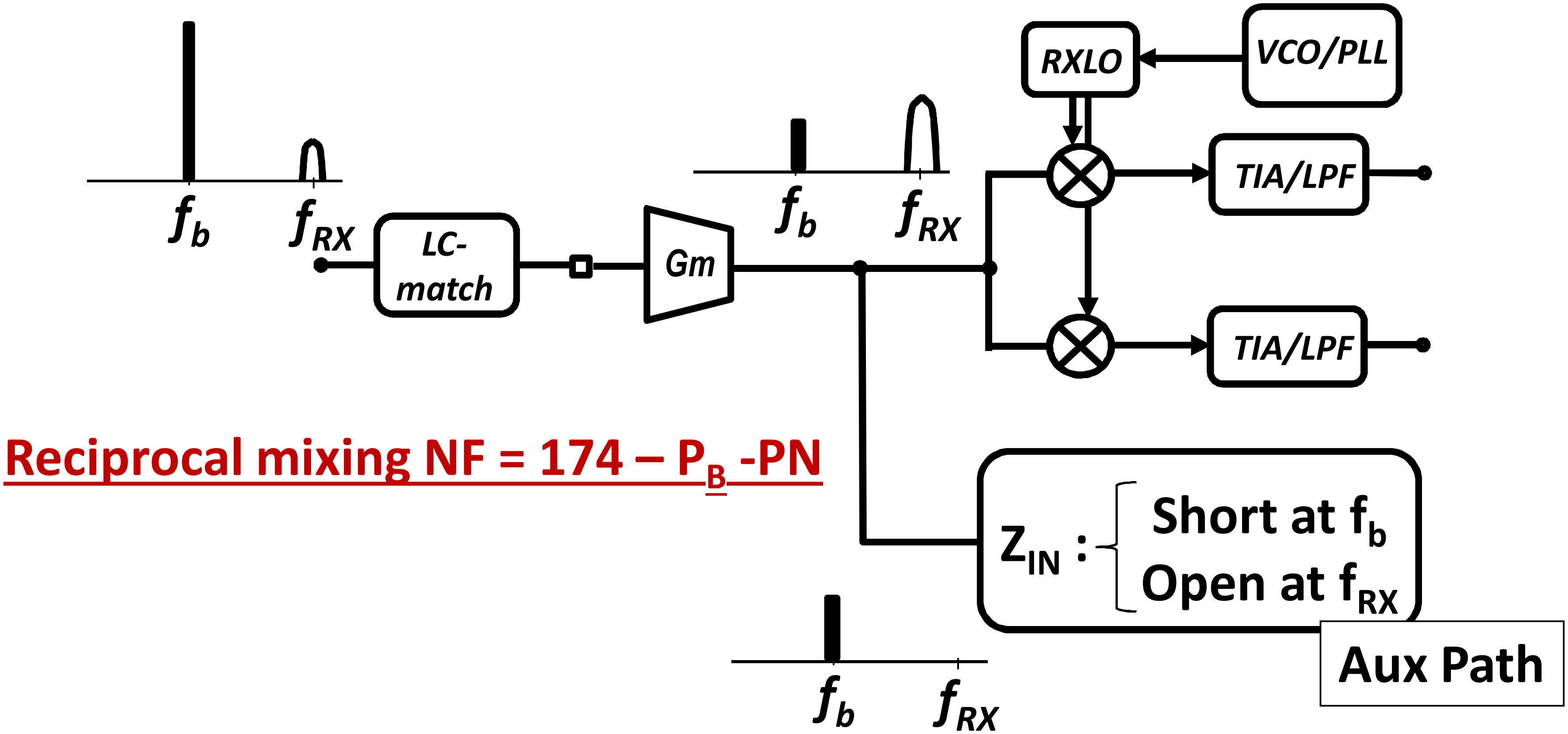
- Blocker offset as low as 10MHz
- SS NF of about 2.4dB

RM Cancelling RX Die Photo



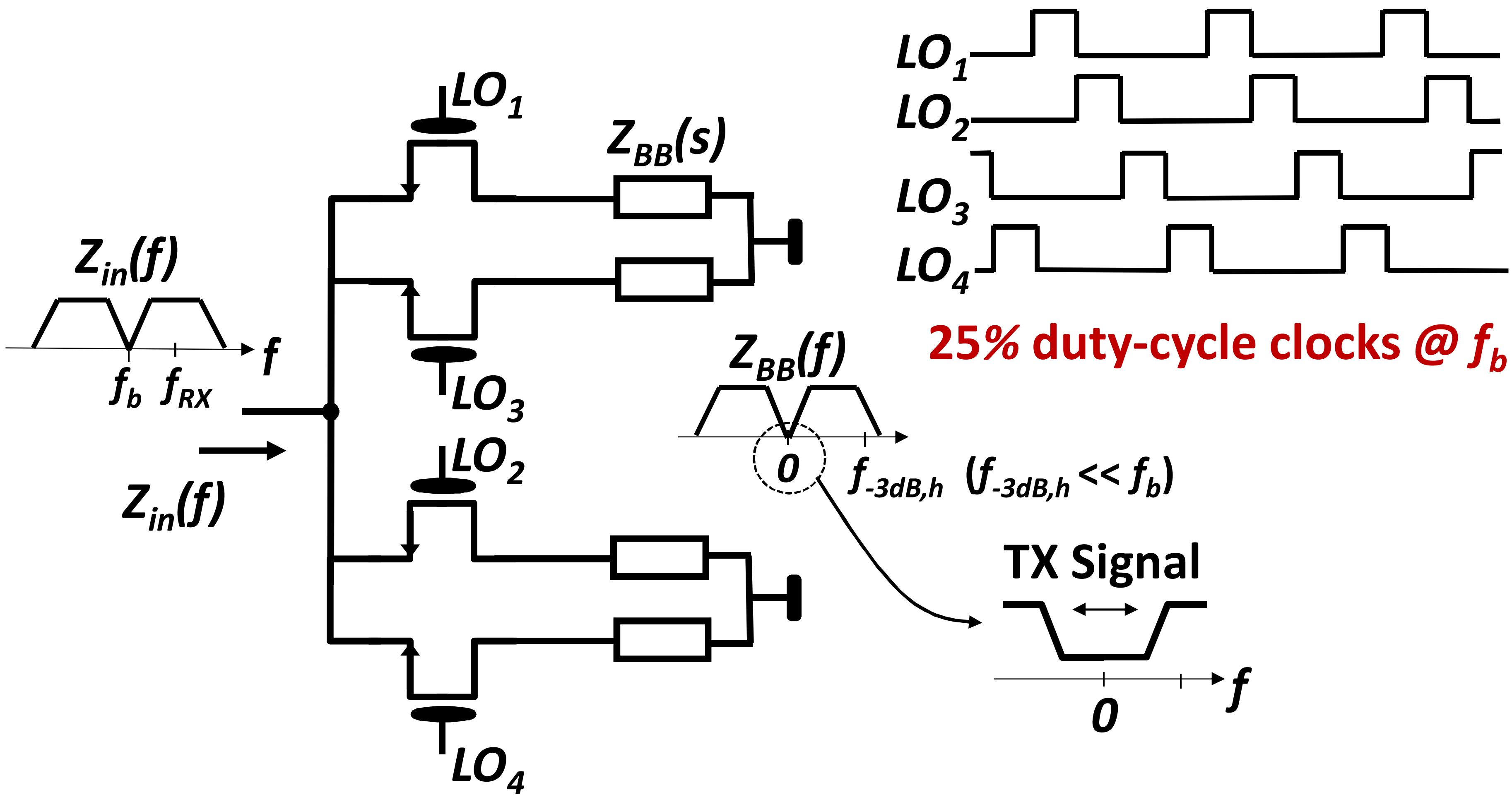
- **40nm CMOS, 1.4mm²**

Receiver Architecture for Coexistence



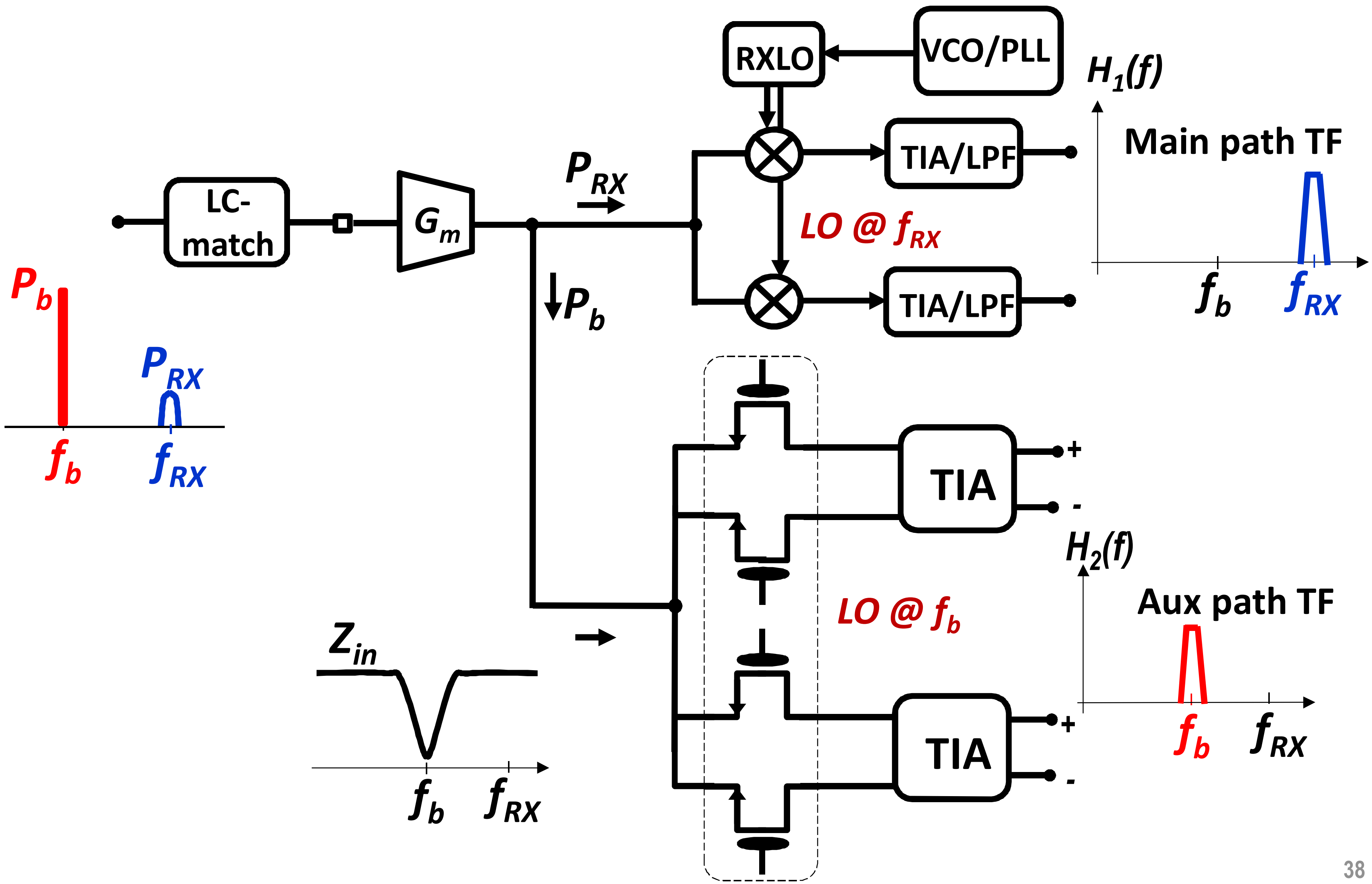
- Second path to divert blocker away
- Relaxes noise and linearity of main receiver

N-Path Impedance Implementation

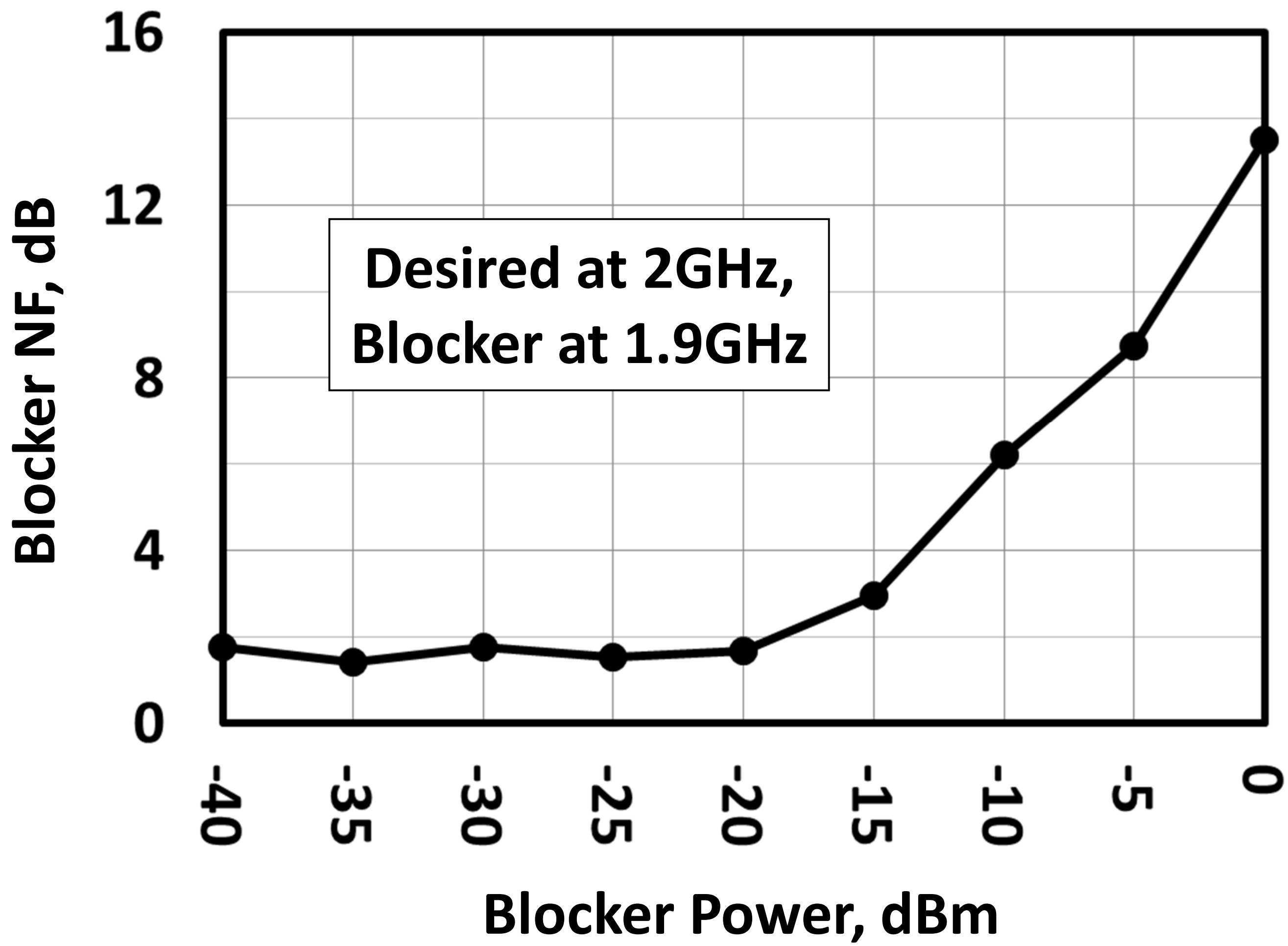


- Clocker by the aggressor TX LO

Coexistence Receiver Architecture



Measured Blocker Noise Figure



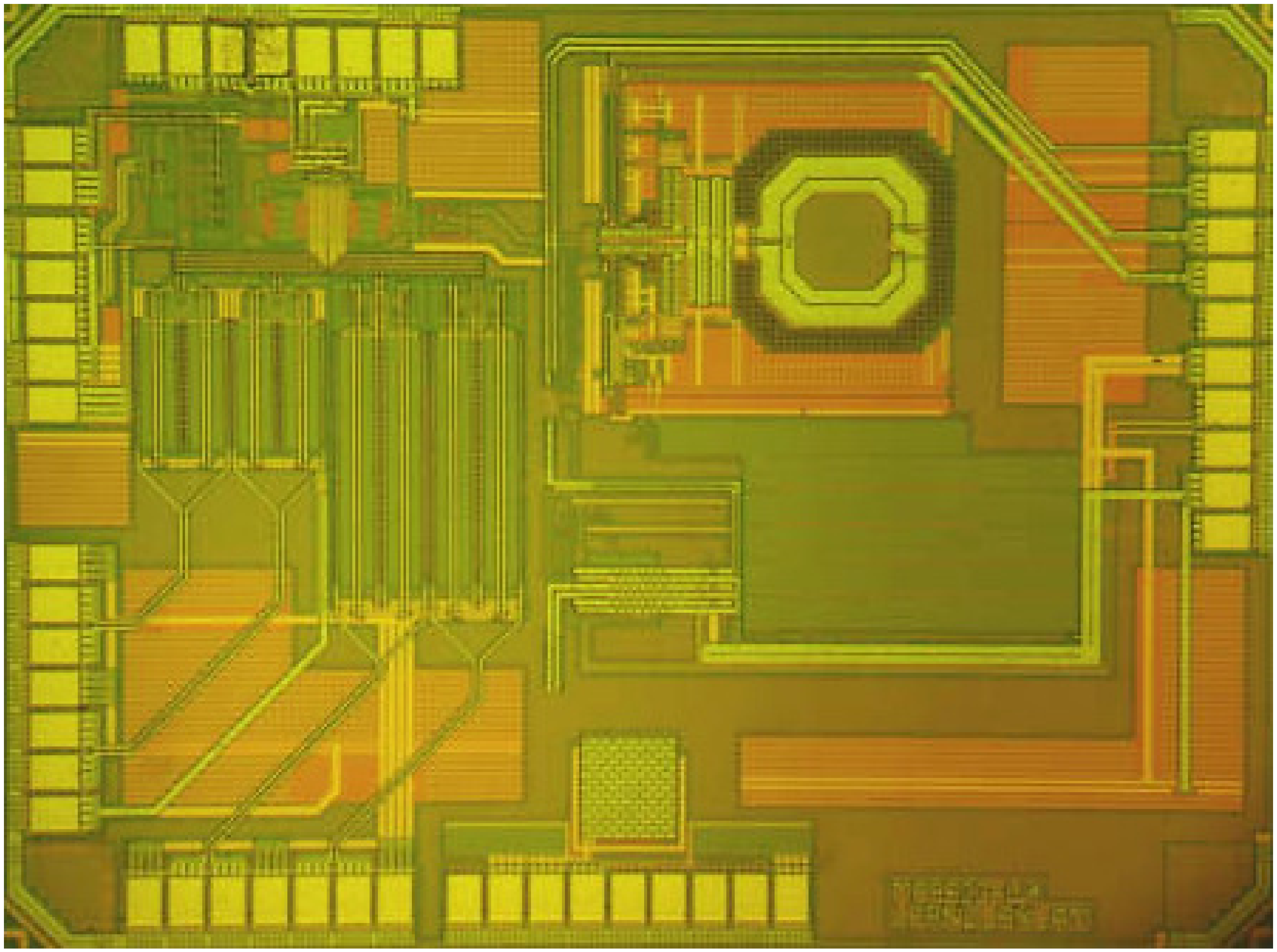
- **NF > 25dB if Aux path de-activated**

RX Performance Summary

Parameter	[1]	[2]	[3]	This work
NF, dB	2.5	2.5	4	1.7
OB IIP3, dBm	-2.5	-4	-14	-2.5
OB IIP2, dBm	> 50	58	N/A	> 50
0dBm Blocker NF, dB	N/A			13.5
Battery Current, mA	65	44	46	10
Total RX Area, mm^2	6.7	3.4	2.2	0.93
Technology	130nm	90nm	65nm	40nm
Application	Cellular	Cellular	WiFi	Generic

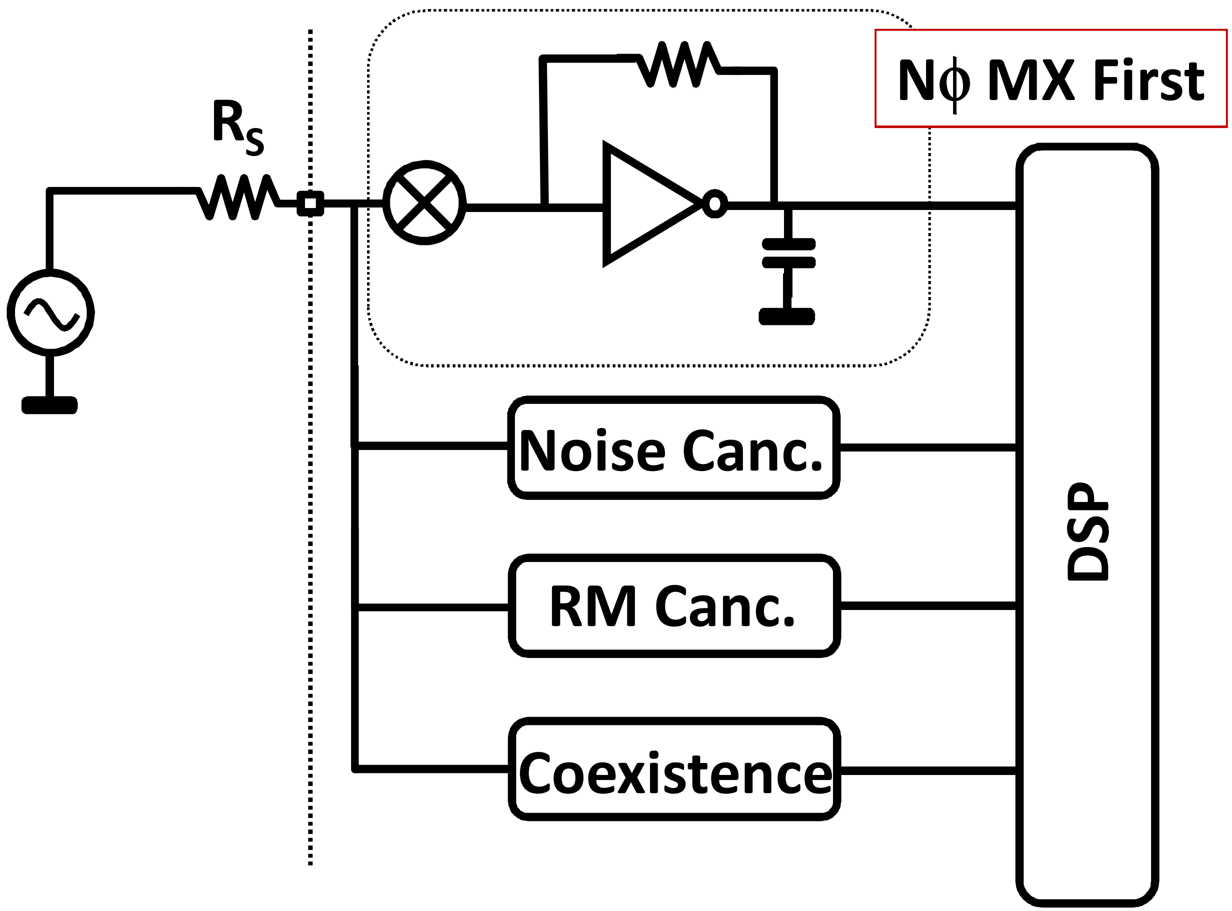
[1] T. Sowlati, et al., "Single-chip multiband WCDMA/HSDPA/HSUPA/EGPRS transceiver with diversity receiver and 3G DigRF interface without SAW filters in transmitter / 3G receiver paths," ISSCC, 2010, pp. 116-117.
[2] M. Nilsson, et al., "A 9-band WCDMA/EDGE transceiver supporting HSPA evolution," ISSCC, 2011, pp. 366-368.
[3] Y. H. Chung, et al., "A 4-in-1 (WiFi/BT/FM/GPS) connectivity SoC with enhanced co-existence performance in 65nm CMOS," ISSCC, 2012.

Coexistence RX Die Photo



40nm CMOS with active area of 0.93mm^2

Summary & Conclusions



- **Scalable**
- **Immune to large blockers and/or low-power**