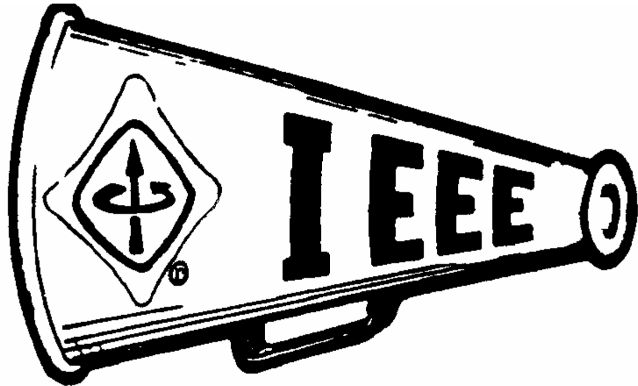
# The Valley Megaphone




Newsletter of the
**Institute of Electrical and Electronics Engineers, Inc.**
**Phoenix Section**
September 2006, Volume XX, Number 9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## *This Issue of The Valley Megaphone Features:*

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IEEE Phoenix Section Executive Committee meeting minutes can be found at: http://www.ieee.org/phoenix

Please send announcements for Valley Megaphone to Eric Palmer: ecpalmer@ieee.org.


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The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly and reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.
Advertising Rates: Full page: $200, 3/4page: $125, ½ page: $75, 1/3 page: $50, 1/4 page: $25.
Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: http://www.ieee.org/phoenix

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**Embry-Riddle, Prescott**
Chair:
Advisor: Chuck Cone
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# Phoenix Section Executive Committee Meeting – First Tuesday of the month.

**Time:** 6:00 pm to 8:30 pm

**Place:** Phoenix Airport Hilton, 2435 South 47th Street
Phoenix, AZ, 85034
Phone: 480-804-6017

**Directions:** From 143, exit University Ave, go west, turn right on 47th street.

**More Info:** Meetings held first Tuesday of month. No meetings in July and August. All interested IEEE members are welcome to attend.

**Contact:** Rao Thallam, Phoenix Section Chairman, ph: (602) 236-5481 or e-mail: thallam@ieee.org

# *2nd ANNUAL ADVANCED MATERIALS FAILURE ANALYSIS (AMFA) WORKSHOP*

**TO BE HELD FRIDAY, APRIL 20, 2007**
**(Following the International Reliability Symposium, SUNDAY-THURSDAY, APRIL 15-19, 2007)**

**HYATT REGENCY HOTEL**
**PHOENIX, ARIZONA**

*AMFA MISSION:*
*To serve the interests of failure analysis & materials characterization professionals by providing a forum for the presentation and* ***active*** *discussion of timely and pertinent technological issues and trends and to promote the development of new capabilities that fill critical gaps in emerging technologies.*

**Unlike traditional conferences that often restrict audience participation, AMFA Workshops provide only top quality invited speakers on leading edge topics, in a format where audience participation is expected and strongly encouraged. Preliminary program details will be available in September, 2006.**

**Mark your calendars now for this exciting event!**

**http://www.amfaworkshop.org**

# 15th Topical Meeting on Electrical Performance of Electronic Packaging

## EPEP 2006

**October 23–25, 2006**
**Scottsdale, Arizona**
**Sponsors:**
**IEEE Components, Packaging and Manufacturing Technology Society**
**IEEE Microwave Theory and Techniques Society**

## Call for Papers

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. Authors are invited to submit papers describing new technical contributions in the areas broadly covered below:

- Current and future issues related to on-chip interconnections
- Router friendly models and modeling tools: accuracy & efficiency
- Modeling and design of high speed digital I/O circuits: signal propagation and reception
- On-chip power delivery and regulation
- Advances in modeling core switching noise, and design of novel solutions
- On-chip measurement techniques
- Package analysis, including numerical methods
- Electromagnetic analysis tools
- Advances in transmission-line techniques
- Power distribution and package resonance
- Long distance propagation in large switching complexes
- Switching noise in multi-layered systems
- Macromodeling techniques
- Signal integrity in mixed signal integrated circuits
- Electrical issues in MEMS packaging
- New and innovative interconnect packaging structures and their electrical performance
- RF/microwave packaging structures and their electrical performance
- MMIC modules and high density packaging
- Experimental characterization techniques
- EMC/EMI sources & effects
- Prediction/measurement of radiation from on-chip sources, interconnect structures and packages
- Electrical design implications for low cost, high volume packaging
- Packaging concerns for wireless communication: design and modeling
- Packaging solutions for on-chip radios: design and modeling
- Performance of packaging for automotive radar systems

**Conference Co-chairs:** Moises Cases, IBM; Paul Franzon, North Carolina State University
**Conference Web Page:** Detailed information can be found at http://www.epep.org
**Paper Submission:** Information for authors can be found on the conference web page. Electronic submissions of no more than four pages must be received no later than **July 10, 2006.**
**Student Paper Award:** Two awards will be presented to the best two papers submitted by students.
**Short Courses/Workshops:** On Sunday, October 22, 2006, a workshop entitled "Future Directions in Packaging" will be presented and short courses/tutorials will be offered.

**Contacts:**
Moises Cases, e-mail: cases@us.ibm.com
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Kelly Sutton, e-mail: epd@engr.arizona.edu

**INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS**
**COMPONENTS, PACKAGING AND**
**MANUFACTURING TECHNOLOGY SOCIETY**
**ECTC Components & RF Program Committee**
**CPMT RF & Wireless Technical Committee**

# 57th ECTC May 29 – June 1, 2007
# Reno, Nevada, USA

The CPMT RF & Wireless Technical Committee and the ECTC Components & RF Program Committee encourage you to submit an abstract to ECTC 2007 in the area of passive components & networks, RF and Microwave components and modules and subsystems. ECTC is the premier Electronic Components and Packaging conference held annually and attended by about 1000 delegates with equal participation from companies and academia. As in the past, Components, RF & Microwave related papers are solicited for focus sessions during this prestigious conference.

**Passive components**

Design, Materials, Processes and manufacturing considerations for discrete passive components- resistors, capacitors, inductors and passive networks

**Integrated / Embedded Passives for digital, mixed signal, RF/Microwave applications:**

Design, technology, characterization - Embedded passives (inductors, capacitors) for RF/microwave applications & evaluation of their performance in terms of Quality Factor (Q), component value, fabrication challenges & cost

**RF and Microwave Components:**

Integrated Antennas, filters, baluns, RFID/sensors, RF MEMS, high power and high efficiency RF/microwave power amplifiers – design, technology, new high frequency characterization methodologies

**RF and Microwave Modules:**

RF/Microwave Packaging techniques & characterization

Module Integration in semiconductor, ceramic, organic or glass substrates for UWB, integrated transceivers for Zigbee, mobile digital TV ---

EMI and innovative shielding techniques for passive components and mixed signal application

**SUBMISSIONS:**

Please submit abstracts using the ECTC web site: www.ectc.net by October 15, 2006. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the "Components & RF" focused sessions **YOU MUST SELECT**

**"Components & RF" committee as your PRIMARY subcommittee preference**

when you submit your abstract at the ECTC web site. Again, to have your paper considered for the RF & microwave components sessions, please do the following:

STEP #1: Submit abstract through the ECTC web site (www.ectc.net) and select **"Components & RF" as PRIMARY subcommittee** preference

STEP #2: Email abstract copy and author's email & contact information to: Craig Gaw at c.a.gaw@ieee.org & Mahadevan Iyer at mahadevan.iyr@ece.gatech.edu

Craig Gaw, Chair - CPMT RF & Wireless TC
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Mahadevan K Iyer, Chair - ECTC RF & Components TC
Georgia Institute of Technology
mahadevan.iyer@ece.gatech.edu

# PES September 2006 Luncheon Meeting

*Date:* Thursday, September 21, 2006

*Time:* 11:30 am - 12:00 noon: Registration
12:00 noon: Lunch
12:30 pm: Program

*Location:* SRP PERA Club
1 E. Continental Dr.
Tempe, AZ

*Speaker:* James Hsu, Senior Principal Engineer, Transmission System Planning Department, Salt River Project

*Topic:* Palo Verde Congestion Management

*Cost:* $8.00 (Students $4.00)

*Reservations:* Contact Michelle at (602) 437-0469 or submit your name through the PES website at http://ewh.ieee.org/soc/pes/phoenix/ .
Reservations deadline is Noon Monday, September 18, 2006.

*Abstract:*

A presentation of the technical analysis of utilizing the Special Protection Systems (SPS) such as (1): a direct load tripping scheme (DLT) during the two major generating units' outages to mitigate the post-transient voltage instability problem and (2): a direct generator tripping scheme (DGT) in the event of double circuits outage to maintain transient stability performance to meet the reliability criteria. Implementation of these SPS can minimize the adverse impact and prevent from further system wide spread cascading outages on the existing system and therefore will maximize system power transfer capability. Discussion of the planning studies and the associated technical advantages that can be achieved by utilizing these two types of special protection systems in the WECC major southwest network hub.

*Biography:*

Mr. Hsu graduated from the National Taipei Institute of Technology in electrical engineering in 1962. He received his MSEE degree from the State University of New York at Binghamton in 1970. During 1968 to 1978, Mr. Hsu was an employee at New York State Electric & Gas Corporation, working primarily with New York Power Pool (NYPP) and Northeast Power Coordinating Council (NPCC) system studies. He has been with Salt River Project since 1978. He is currently a senior principal engineer in the Transmission System Planning Department of Salt River Project. His primary responsibility includes developing plans for the company’s major transmission projects and directing technical studies for power system planning and operations. He is a member of the IEEE Dynamic Stability Performance Subcommittee and has recently made submission to the CIGRE Task Force 38-02-25 on “Modeling of Gas Turbines and Steam Turbines in Combined-Cycle Power Plants”. He has authored and coauthored several papers on power system planning and power system analysis and techniques. Mr. Hsu is a registered Professional Engineer in the State of Arizona

# $49^{TH}$ ANNUAL IEEE – PES GOLF OUTING

| | |
|---|---|
| DATE: | Saturday, SEPTEMBER 23RD, 2006 |
| TIME: | 8:00 a.m. SHOTGUN START- Best Ball Four Man Scramble |
| PLACE: | ANTELOPE HILLS GOLF CLUB<br>One Perkins Dr.<br>Prescott, AZ 86301 |
| FEE PER PLAYER: | $ 85.00 - includes: Green Fees, Golf Cart, Buffet Lunch |
| PRIZES: | Prizes for the top three teams plus individual skills will be awarded. There will also be a raffle. |
| LUNCH: | Included- will be served immediately following golf |
| RESERVATIONS: | Call Steve or Pam by September $6^{th}$ @ (480) 661-8599<br>Reservations deadline is Wednesday, September 6, 2006. |

CHECKS MUST BE MADE PAYABLE TO: IEEE – PES (If not checks will be returned)
Checks must be received by September 8, 2006. (No later!)

PLEASE MAIL CHECKS TO: IEEE – PES
c/o Clark Power Products
10752 N. $89^{th}$ Place # 104
Scottsdale, AZ 85260

# Institute of Electrical and Electronics Engineers, Inc.
## Phoenix Section
### Components, Packaging and Manufacturing Technology Society Chapter
### &
### Waves and Devices Chapter

*PRESENT AN ALL-DAY WORKSHOP ON*

# Convergence in Communication and Computing

**Date:** Friday, November 17th, 2006 **Time:** 7:00 A.M. – 5:00 P.M.
**Location:** Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

## Abstract

**The convergence of mobility, seamless connectivity, and broadband access are the underpinning of next-generation communication systems. Several new applications such as video-conferencing and wireless multimedia are emerging to leverage this capability. Many communication platforms (3G Cellular, WiMax, WLAN, etc.) compete to provide the best solutions for consumer needs in communication, computing and entertainment products. Technology challenges - component through system level - abound for realizing such opportunities at a marketable price point. This one day workshop will bring together experts from industry, academia, government labs, and the financial community to share market visions and to discuss technology issues, options, opportunities and emerging standards. The goal is to provide a comprehensive view of the challenges facing system, device, interconnect and packaging technologies. A panel discussion on the "Future of Convergence in Communications" will bring closure to the day's workshop. Vendors in the entire supply chain will display their products and services throughout the day.**

## Topics

- Vision – A View of the Future of Convergence
- Market – Current Status and Future Trends
- Business Model
- System and Architecture
- Communication Technology Options and Standards
- Device Technology – RF, Microwave, Analog, and Base Band / Graphic Processing
- Packaging – Mobile Products and Infrastructure
- Antenna / Propagation
- System Integration
- Panel discussion on the Future of Convergence in Communications

Chair: Vasu Atluri (480) 554-0360 Co-Chair: Chuck Weitzel (480) 413-5906

**Technical Committee**

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| Shahin Farahani | (480) 413-6010 | Rashaunda Henderson | (480) 413-5374 | Mel Miller | (480) 413-6111 | Dragan Zupac | (480) 413-3964 |

For General Information: http://www.ieee.org/phoenix
For Workshop Registration Forms: Sergio Pacheco (480) 413-3737
For Vendor Registration Forms: Vivek Gupta (480) 554-2195

**IEEE Components, Packaging and Manufacturing Technology Society**
**Phoenix Chapter**

**Tuesday, September 19th, 2006 Tutorial Meeting**

# Failure Analyses for Electronic Packaging

Dr. Jonathan Harris, President, CMC Interconnect Technologies, Tempe, Arizona
Mr. Ken Tylor, Manager, Sonoscan, Inc., Scottsdale, Arizona
Dr. Dev Gupta, CTO, APSTL, Scottsdale, Arizona
Dr. Rajen Dias, Principal Engineer, Intel Corporation, Chandler, Arizona

## Tutorial Scope

Introduce basic methods, tools and techniques of failure analyses practiced in microelectronic packaging. Present applications in Flip Chip Interconnect, Pb-free solders, High Performance Processor Packaging, and Ceramic & Plastic Packaging. Discuss failure modes, mechanisms and resolutions in these application areas. Look beyond the limitations of current day's tools and techniques to address the needs of next generation interconnect and package technologies.

## Tutorial Agenda

| | |
|---|---|
| 12:00 – 12:50 PM | Registration |
| 12:50 PM – 1:00 PM | Welcome Address by Dr. Mali Mahalingam and Dr. Daniel Lu |
| 1:00 PM – 2:00 PM | How Interfacial Structure Can Play a Major Role in Packaging Reliability<br>*Dr. Jon Harris, CMC Interconnect Technologies* |
| 2:00 PM – 3:00 PM | Introduction to Acoustic Micro Imaging and Its Applications<br>*Mr. Ken Tylor,* Sonoscan, Inc. |
| 3:00 PM – 3:30 PM | Refreshment Break |
| 3:30 PM – 4:30 PM | Failure Analyses for Flip Chip Packages<br>*Dr. Dev Gupta, APSTL* |
| 4:30 PM – 5:30 PM | Next Generation Analytical Tools for Package Failure Analysis<br>*Dr. Rajen Dias, Intel Corporation* |
| 5:30 PM – 5:45 PM | Tutorial Wrap-Up |

## Tutorial Abstracts

*How Interfacial Structure Can Play a Major Role in Package Reliability?*
*Dr. Jon Harris, CMC Interconnect Technologies*

This talk will investigate the general role of interfacial microstructure on the reliability of package construction. Specifically, the talk will focus on the role of intermetallic compound morphology in determining failure modes when mechanical stress is applied to the package. Methods for delineating interfacial structures will be discussed, including cross-sectional SEM and optical microscopy. Examples of the controlling effect of interfacial microstructure will be given from ceramic and plastic packaging technologies. The role of Pb-free solders on intermetallic compound formation will also be described.

*Introduction to Acoustic Micro Imaging and Its Applications*
*Mr. Ken Tylor, Sonoscan, Inc.*

Ultrasound is a form of mechanical energy and is, therefore, sensitive to the elastic properties of the materials it travels through. It is particularly sensitive to locating air gaps (cracks, delaminations and voids). Acoustic Micro Imaging (AMI) uses high frequency ultrasound (5 – 300MHz) to image internal features and characterize physical

defects that occur during the manufacturing process or environmental stress. This presentation will provide an overview of the basics of ultrasound, how it is used for Acoustic Imaging, and explores a variety of applications (including: plastic encapsulated ICs, power devices, flipchips, MLCCs, etc.). It will also cover the role of AMI in industry standards, current developments, and future advancements.

*Failure Analyses for Flip Chip Packages*
*Dr. Dev Gupta, APSTL*

Flip chip packaging is now pervasive for high performance processors and is spreading into the less critical but yet larger volume Portable Electronics applications. As this once robust high end technology has to adjust to changes in materials sets ( low – k, Pb – free,.. ) and undergoes cost cutting in order to expand its applications, reliability issues and failure analyses need to be revisited. Failure and Root Cause Analyses during Package Qualification as well as Field Failures play a crucial role in building confidence for outsourced manufacturing. Failure Analyses can be more effective when the Analyst understands typical vulnerabilities of a technology. This presentation covers both fundamentals of Flip Chip packaging as well as successful approaches to Failure Analyses.

*Next Generation Analytical Tools for Package Failure Analysis*
*Dr. Rajen Dias, Intel Corporation*

Advanced packaging solutions for high performance microprocessors involve use of multi-level interconnections, shrinking geometries and improved thermal solutions. These trends together with the introduction of low k dielectrics and Cu metallization in next generation Si technologies and new package substrate materials has resulted in severe die/package thermal - mechanical mismatch concerns. Packaging solutions for non CPU applications such as memory, chip sets, networking and communication chips are driven by miniaturization, stacked die for increase in functionality and Pb free applications.

Understanding the defect and intrinsic failure mechanisms during the development and certification of these new package technologies is becoming extremely difficult and time consuming using traditional approaches to failure analysis. Non destructive methods to detect the onset of these mechanisms are critical to time to information in the current era of rapidly shrinking development cycles. This talk will discuss the unique challenges faced by the failure analyst and will focus on advancements in three nondestructive tools – Scanning SQUID microscopy for detecting shorts, 3D x-ray radiography/tomography for imaging various levels of interconnections and scanning acoustic microscopy for detecting interfacial delamination and defects. In addition, novel analytical tools such as Laser Spallation for understanding interfacial adhesion and Laser milling for package delayering and microsurgery will be introduced.

## Speaker Biographies

**Dr. Jonathan Harris** has played a leadership role in the advanced ceramic materials and electronic packaging industry over the past 20 years. Dr. Harris is currently the President of *CMC* Interconnect *Technologies*, a materials analysis and consulting firm which focuses on the electronic interconnect industry. CMC provides a range of technology services including materials characterization, failure analysis, device/package deprocessing, and technical market analysis. CMC's clients include Fortune 100 device manufacturers and advanced materials companies. Prior to founding *CMC Interconnect Technologies* in 2003, Dr. Harris was President of *CMC Wireless Components*, a high thermal performance ceramic packaging company which served the telecommunications, optics, and medical industries. Dr. Harris received his doctorate in Solid State Physics from Brown University (Providence, RI) in 1983. He is the author of over 50 publications and book chapters and has 20 US Patents.

Dr. Jonathan Harris, President, CMC Interconnect Technologies
7755 S. Research Drive, Suite 115, Tempe, AZ 85284
Tel: (480) 496-5120    Email: jharris@cmcinterconnect.com

**Mr. Ken Tylor** holds a Bachelor of Science degree in Physics from Wheaton College in Wheaton, Illinois. He started with Sonoscan in 1989. During his nine years at the corporate office in the Chicago area, he was involved in various aspects of the laboratory and instrument quality assurance. He was also part of the team opening Sonoscan's first off-site laboratory in San Jose, California. In 1998 Ken moved to Phoenix, Arizona, to start up and manage Sonoscan's second branch laboratory, supporting customers in the southwest region of the country.

Ken Tylor, Analytical Testing Laboratory Manager, Sonoscan, Inc.
7585 E. Redfield Road, Suite 106, Scottsdale, AZ 85260
Tel: (480) 342 – 9400    Email: SSW@Sonoscan.com

**Dr. Dev Gupta** is an industry recognized expert in Advanced Packaging who regularly teaches Professional Development Courses at IEEE organized international conferences and contributes to industry publications. As a Material Scientist Dr. Gupta has been deeply involved in applying modern failure analyses techniques to the package technologies he has worked on. Since the late '80s Dev has been involved in pioneering the development of key Flip Chip packaging technologies at Motorola. Later at Intel he solved key technological bottlenecks to volume production of organic substrates and managed the design & start up of the original factories for same in Japan. At APSTL, a company engaged in developing and licensing flip chip and wafer level packaging technologies for low cost applications like mobile phones, Dr. Gupta has developed technologies for electroless nickel and column bump flip chip processes and managed turnkey engineering of same at customer fabs in both the US and Far East.

Dr. Dev Gupta, Chief Technology Officer, APSTL, Scottsdale, Arizona
Phone: (480) 540-3232 Email: apstl@az.rmci.net

**Dr. Rajen Dias** graduated with a Bachelor of Science degree in Metallurgy and Material Science from Indian Institute of Technology, Madras, India, and an MS and Ph.D. in Material Science at Lehigh University. He worked at Intel Corporation for 21 years in the assembly technology development Quality & Reliability department. His areas of focus have been understanding failure modes and mechanisms in new packages, training failure analysts corporate wide and responsible for developing the next generation analytical tools and techniques for package failure analysis.

Dr. Rajen Dias, Principal Engineer, Intel Corporation, Tempe, Arizona
5000 W. Chandler Blvd., Mail Stop: CH5-263, Chandler, Arizona - 85226
Phone: (480) 554-5202 Email: rajen.c.dias@intel.com

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|---|---|
| **Date:** | Tuesday, September 19th, 2006 |
| **Location:** | Amphitheater (Located in Third Floor)<br>Hilton Phoenix Airport, 2435 South 47th Street, Phoenix, Arizona - 85034<br>Tel: (480) 894-1600; Website: www.phoenixairport.hilton |
| **Time:** | 12:00 PM – 12:50 PM Registration<br>12:50 PM – 5:45 PM Program<br>3:00 PM – 3:30 PM Refreshment Break |
| **Cost:** | $15 for IEEE members / $25 for Non-IEEE Members (Includes Tutorial Material and Refreshments) |
| **Registration:** | www.ieee.org/phoenix |
| **Audience:** | IEEE members and non-members all are welcome to attend. |

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***For more information please call any of the following officers:***

Mali Mahalingam (480) 413-5368
Vivek Gupta (480) 554-2195
Vladimir Noveski (480) 554-2375
Vasu Atluri (480) 554-0360
Debendra Mallik (480) 554-5328
Rao Bonda (480) 413-6121
Daniel Lu (480) 552-2909
Victor Prokofiev (480) 552-0228
Jim Drye (480) 413-3604

# JOIN the IEEE CPMT Society

Relevant Information can be obtained at
**www.cpmt.org**

IEEE — THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC. — CPMT IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

**IEEE Components, Packaging and Manufacturing Technology Society**
**Phoenix Chapter**

**Tuesday, September 19th, 2006 Tutorial Meeting**

# Failure Analyses for Electronic Packaging


Dr. Jonathan Harris, President, CMC Interconnect Technologies, Tempe, Arizona
Mr. Ken Tylor, Manager, Sonoscan, Inc., Scottsdale, Arizona
Dr. Dev Gupta, CTO, APSTL, Scottsdale, Arizona
Dr. Rajen Dias, Principal Engineer, Intel Corporation, Chandler, Arizona

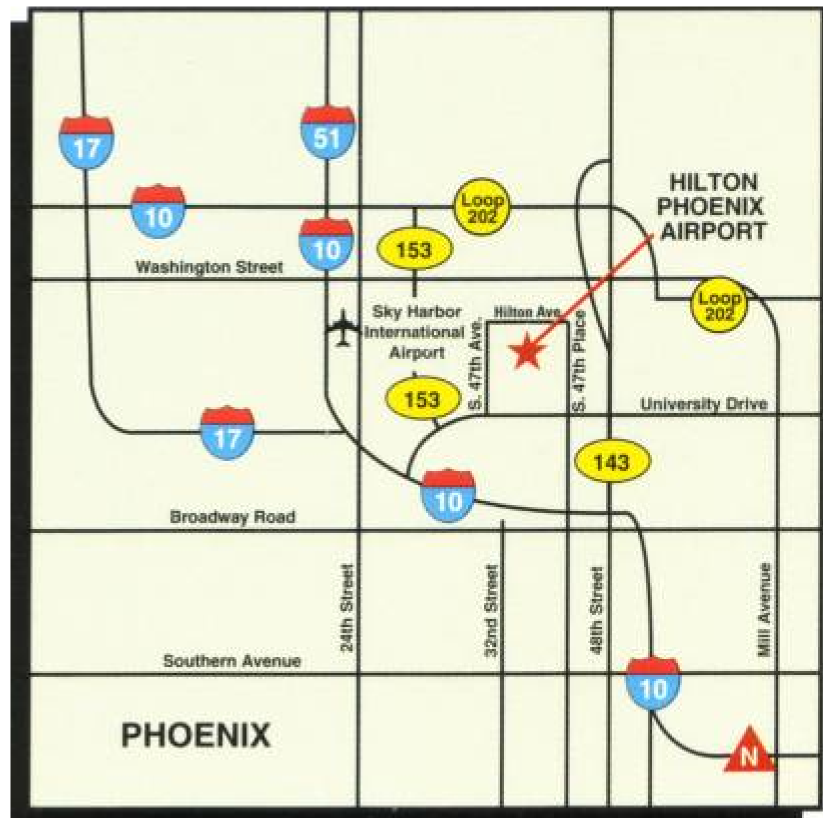

## Tutorial Registration at www.ieee.org/phoenix

# TUTORIAL LOCATION DETAILS

**Hilton Phoenix Airport**
**is located at**
**2435 South 47th Street**
**Phoenix, Arizona 85034**

**West of 143 Freeway and North of University Drive**

**For Further Assistance Call**
**(480) 894-1600**



# IEEE Phoenix Area Consultants Network September Meeting: Tax Strategies for Small Business Owners

**Date:** Thursday, September 14, 2006

**Time:** Networking begins at 6:30 p.m.
Dinner begins at 7:00 p.m.
Program starts at 8:00 p.m.

**Place:** Denny's Restaurant
3315 N. Scottsdale Rd. (at Osborn)
Scottsdale, Arizona 85251

**Abstract:** Michael R. Oxford, President & Jeanne Seese, CPA of Oxford Retirement & Estate Planning will present a talk on tax strategies for small business owners. Their talk will also cover benefits and executive life planning for consultants and other small business owners.

Oxford has 25 years experience in estate planning and small business management. He is a small business owner and brings that perspective to his discussion. Seese received her CPA in 1994. She has prepared personal and business taxes since 1984.

For more information, contact Vaughn Treude, vaughn@nakota-software.com , or see the IEEE PACN website, www.ieeepacn.com.

**INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS**

**WAVES AND DEVICES**
**PHOENIX CHAPTER**

**September 8, 2006 MTTS Meeting**
**www.eas.asu.edu/~wadweb**

# 0-60 GHz in Three Years: mm-Wave CMOS Research at BWRC

**Prof. Ali M. Niknejad**
Berkeley Wireless Research Center (BWRC), University of California, Berkeley

## Abstract

CMOS technology scaling in many ways has been detrimental to analog circuits, producing devices with lower intrinsic gain and wider variability. One important and notable exception, though, is the speed of the scaled device, now exceeding 100 GHz. The 60 GHz spectrum, considered out of the reach of conventional technology only a few years ago, is now within the grasp of inexpensive digital CMOS technology. This talk will chronicle the BWRC effort to design and fabricate 60 GHz circuits and systems in 130 nm CMOS. Operation at this high carrier frequency enables a host of new applications, such as ultra high speed short range wireless communication and low cost portable radar systems. The talk will include design considerations for medium range gigabit-per-second WLAN system. Lastly, the talk will investigate the future trends of CMOS technology scaling for mm-wave applications. Measured results of power gain, power consumption, and noise in a 90 nm CMOS technology will demonstrate a promising future for mm-wave CMOS.

## Biography

**Ali M. Niknejad** received the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 2000. He spent two years in industry working on RF CMOS power amplifiers. He is currently an associate professor in the EECS department at UC Berkeley and co-director of the Berkeley Wireless Research Center and the BSIM Research Group. He served as an associate editor of the IEEE JSSC and is now serving on the TPC for CICC and ISSCC. Prof. Niknejad was co-recipient of the Outstanding Technology Directions Paper at ISSCC 2004 for co-developing a modeling approach for devices up to 65 GHz.

**Date: September 8, 2006**

**Location: Group Conference Rm, Bldg 94, Freescale Semiconductor, 2100 E. Elliot Rd., Tempe, AZ**
Use Freescale Main Entrance (South) facing Elliot Road

**Time: 3:00 - 4:00pm Presentation**
For more information, please call Chuck Weitzel (Chapter Chair) at (480) 413-5906.

# IEEE Region-6 Director-Elect for 2007 – 2008 Election

**Submitted by Vasudeva P. Atluri, IEEE Phoenix Section Officer**

IEEE is currently in the process of nominating and electing of the officers for the upcoming years. One can find all the information related to the IEEE Elections at the following website: http://www.ieee.org/portal/pages/iportals/aboutus/whatis/bylaws/i-308.html#DE. IEEE Region 6 has nominated two candidates, Dr. S.K. Ramesh and Dr. Leonard J. Bond, for Director-Elect for the two years term, 2007 and 2008, for inclusion on the election ballot for voting by eligible IEEE members from Region 6. IEEE Phoenix Section members are strongly encouraged to take part in the elections by casting a vote. The key information related to election ballots is as follows:

Ballot Submission Schedule: On or before September 1st, 2006, the Board of Directors shall submit to eligible voting members on record as of August 1st, 2006, a ballot listing all nominees for the positions to be filled by election by the membership.

Ballot Marking; Voting; Tellers Committee Announcement; Election Results: Ballots will be valid only when completed in accordance with the instructions accompanying the ballot and when received at IEEE Headquarters or by a qualified organization designated by the IEEE Executive Committee before twelve o'clock noon on the first working day following October 31st (the "final election ballot receipt date"). Ballots shall be validated and votes shall be tallied under the actual or delegated supervision of the Tellers Committee not later than the fifth working day following the final election ballot receipt date. As provided in Bylaw I-306.21, the Tellers Committee shall announce the result of the tally of the votes not later than the eighth working day following the final election ballot receipt date in a report to the Board of Directors signed by the Chair of the Tellers Committee. The results of the vote shall become official upon acceptance by the Board of Directors of the Tellers Committee report, and if applicable the Credentials Committee report. Each nominee for office listed on the ballot and each write-in candidate having votes recorded in such report according to Bylaw I-308.14 shall be advised promptly of the Tellers Committee tally of the votes applicable to their respective elections. Eligible voting members shall be permitted to vote in each election for one nominee for each office appearing on the ballot. Subject to Bylaws I-302.9 and I-306.5, the nominee, for each office for which the election is being held, receiving the greatest number of qualified votes shall be declared elected. In the event of a tie vote, the Board of Directors shall choose between the nominees involved.

The following paragraphs give a brief biography, IEEE contributions, and statements for the two candidates nominated for IEEE Region 6 Director-Elect position.

**S. K. Ramesh, Ph.D.**
Department Chair/Professor of Electrical and Electronic Engineering
California State University
Sacramento, California, USA
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Email: rameshs@ecs.csus.edu
Website: www.rameshregion6.com

S. K. Ramesh has served the IEEE at the Chapter, Section, Area and Regional levels. Recent recognitions include the 2004 IEEE Region 6 Outstanding Community Service Award and the 2000 Person of the Year Award from the Sacramento Engineering Regional Consortium. The Sacramento Chapter of IEEE LEOS was named the 2005 Most Improved Chapter under his leadership. He is the Counselor of the IEEE CSUS Student Branch which won the 2003 RAB Student Branch Membership Growth Award in Region 6. Dr. Ramesh is active on several Boards including SARTA (www.sarta.org) and McClellan Technology Incubator (www.mtisac.com ) which emphasize job creation and foster the growth of the high technology sector in the region. Dr. Ramesh is a Professor in the Electrical and Electronic Engineering Department at California State University, Sacramento and has served as the Department Chair since 1994. He received his PhD degree in 1986 from Southern Illinois University, Carbondale.

**IEEE Activities** -- (S'80-M'86-SM'93) ***REGIONS:*** Region 6: Operating Committee, 2001-2004; Central Area Chair, 2001-2004; Awards Committee, 2002-2003, Central Area Student Activities Chair, 1994-1995 & 1998-2000; ***SECTIONS:*** Sacramento: Chair, 1992-1993; Vice-Chair, 1991-1992; Secretary, 1990-1991; Membership Development Committee Chair, 1993-1994; Student Activities Chair, 1993-Present. Section Executive Committee, 1990 – 1994 and 2004 – Present. ***SOCIETIES:*** Lasers and Electro-Optics: LEOS Sacramento Section Chapter Chair, 1989-1992 & 2004-Present. ***STUDENT BRANCHES:*** California State University, Sacramento: Student Branch Counselor, 1990-Present; ***CONFERENCES:*** Invited Presentation at IEEE Deans Summit 2003:Fostering Campus Collaborations (www.ieee.org/eab/fcc ), Reviewer and Technical Program Committee Member, IEEE International Conference on Communications – ICC 2003 and ICC 2001, Reviewer and Member Program Technical Committee, Optical Networking Symposium, IEEE Globecom 2002, Reviewer IEEE Frontiers in Education Conference, IEEE FIE 2001. ***REPRESENTATIVE***: Region 6 representative, IEEE-USA Committee on Communications and Information Policy, 2005.

***AWARDS:*** IEEE Region 6 Outstanding Community Service Award, 2004. LEOS Sacramento, Most Improved Chapter, 2005-06 and 1991-92; LEOS Sacramento, Largest Membership Growth, 1992-93; CSU Sacramento Student Branch, RAB Membership Growth, Region 6, 2002-03, IEEE CSUS Student Branch, Outstanding Branch Counselor Award, .1999, IEEE CSUS Student Branch, Outstanding Service Award, 1998.

***Dr. S.K. Ramesh's Statement:***

I have served the IEEE in several leadership roles at the Chapter, Section, Area and Regional levels. I understand the challenges facing the IEEE, and will use my extensive experience working with several organizations, and non-profit boards to serve you effectively.

If elected as the IEEE Region 6 Director I will:

- Strengthen Sections to proactively serve the professional and career needs of members
- Emphasize Strategic Planning, Teamwork and Leadership Development for Section Officers
- Support interactions between IEEE and industry to enhance the profession and support members activities
- Provide prudent fiscal leadership, monitor, evaluate and deliver programs of value to our members
- Present the Region's needs effectively on the Board of Directors
- Enhance awareness of engineering in pre-college students and especially women and minorities

It is an honor and a privilege to be nominated and I would appreciate your vote. Please visit my candidate web site at www.rameshregion6.com for additional information.

**Leonard J. Bond, PhD.**
Director
Center for Advanced Energy Studies
Idaho National Laboratory
Tel: (208) 526-9150
Email: Leonard.bond@inl.gov
Website: http://CAESenergy.org

Dr. Bond received a Bachelor of Science in Applied Physics (1974) and a PhD in Physics (1978) from The City University, London. He is an expert in ultrasonics. He is a Senior Member, IEEE; Member IEE, Chartered Electrical Engineer (UK); Fellow, Institute of Physics and a Chartered Physicist (UK). He is an Affiliate Faculty at University of Idaho and Idaho State University. He moved to USA in 1990. The posts he held included: Reader in Ultrasonics, University College, University of London; Guest Scientist, NIST, Boulder and Research Professor, University of Colorado, Boulder; Chief Scientist, Denver Research Institute; Laboratory Fellow: Pacific Northwest National Laboratory. He has participated in PNNL Management Skills Development Program (1999-2002). He is received PNNL Exceptional Performance Award 2003 and Battelle Key Contributor Award 2003. He is also a recipient of the IEEE Richland Section, Engineer of the year 2002. He is currently serving as a USA representative in International Electrotechnical Commision (IEC/TC 45) Nuclear Instrumentation working group. He authored or co-authored more than 250 publications and holds 7 patents. Member American Red Cross, Greater Idaho, Leadership Council.

**IEEE Activities** -- (S'76-A'77, M'92-SM'2005) ***SECTIONS:*** Member Eastern Idaho and previously Richland, WA; Colorado and London (UK). ***COUNCILS:*** Nanotechnology: Administrative Committee, 2002-2004; Publications Committee, 2002-2003. ***SOCIETIES:*** Member, Ultrasonics, Ferroelectrics and Frequency Control (UFFC) since 1976. ***CONFERENCES:*** 3rd Annual IEEE Nanotechnology Conference (IEEE-NANO 2003), Organizing Committee/Publications Committee Chair. ***REPRESENTATIVE:*** Ultrasonics, Ferroelectrics and Frequency Control: UFFC Member Representative to IEEE Nanotechnology Council, 2002-2004. ***AWARDS:*** IEEE Richland Section Engineer of the Year, 2002.

***Dr. Leonard J. Bond's Statement:***

**IEEE Meeting the USA Energy and Workforce Challenges - Fuelling the Future:** The US faces unprecedented challenges in delivering secure and affordable energy and it is projected that 40% of US skilled workers could retire within 5 years. The IEEE has a duty and responsibility to better address the energy technology challenges, look towards "post-oil," lead interdisciplinary meetings, present the issues and becoming increasingly engaged in education and workforce supply. My experience in academia, industry and national laboratories, as well as three IEEE regions, gives me a perspective and management experience base that can ensure critical issues are better addressed. A strong and active IEEE Region 6, with growing membership, is needed to move forward into this century in a position of influence. I have been a member of the IEEE for 31 years. Until 12 months ago I was an academic and then a research scientist. I was mostly a user of publications and a conference participant. My current position enables me to now give back to the IEEE, from which I have benefited, and give leadership to address energy, climate change and workforce challenges.

# IEEE Senior Membership

Dr. Vasudeva P. Atluri
IEEE Phoenix Section Officer

IEEE Phoenix Section has taken the responsibility for helping eligible IEEE members within the section for getting elevated to IEEE Senior Member grade. IEEE Admissions and Advancement (A&A) committee meets about eight times a year to review and decide on the applications for Senior Member grade. The next two meetings are being held on September 23rd, 2006, in Atlanta, Georgia; October, 2006 (date and location yet to be decided); and November 18th, 2006, in New Orleans, Louisiana. If you meet the requirements for Senior Member grade as listed below, please send your detailed resume including IEEE Member Number, Home Address / Telephone Number / Fax Number / Personal Email Address; Business Address / Telephone Number / Fax Number / Business Email Address; Academic Credentials including starting and ending month for each program; Professional / Work Experience including starting and ending month for each assignment; Publications / Presentations / Patents / Etc.; Honors / Awards; Professional Affiliations / Memberships; Up to Four References Contact Information who are IEEE members; etc. IEEE Phoenix Section will help you with IEEE Senior Member References in case you are not able to find one. Please send your resume in word format to my attention at both vpatluri@ieee.org and vasudeva.atluri@intel.com. The resumes should be received at least six weeks prior to next scheduled IEEE Admissions and Advancement Committee meetings mentioned above for 2006. The meeting schedule for 2007 is not yet decided by IEEE. Additional information regarding IEEE Senior Member grade and IEEE Admissions and Advancement Committee meetings can be obtained by accessing http://www.ieee.org/organizations/rab/md/smprogram.html. The following paragraphs also give a brief summary of the IEEE Senior Member program.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. The benefits of IEEE Senior Membership benefits include:

- The professional recognition of your peers for technical and professional excellence.
- An attractive fine wood and bronze engraved Senior Member plaque to proudly display.
- Up to $25.00 gift certificate toward one new Society membership.
- A letter of commendation to your employer on the achievement of Senior Member grade (upon the request of the newly elected Senior Member.)
- Announcement of elevation in Section/Society and/or local newsletters, newspapers and notices.
- Eligibility to hold executive IEEE volunteer positions.
- Can serve as Reference for Senior Member applicants.
- Invited to be on the panel to review Senior Member applications.

IEEE takes keen interest in encouraging members to get elevated to higher grades for the following reasons:

- Many Executive Volunteer offices require that a member hold Senior Member grade.
- Senior Members provide leadership on a volunteer basis.

- The percent and number of IEEE Senior Members reflects on the competence and prestige of IEEE, its products and services.
- Senior Membership in IEEE is key to Retention:
  - Senior Members have a retention rate of 98%.
  - A greater percentage of Senior Members belongs to more IEEE Societies than do other IEEE member grades.
  - Senior Members volunteer at a higher percentage rate than do other grades of IEEE members.

To qualify for Senior Member elevation, an applicant should meet certain requirements as listed below. IEEE Bylaw I-105.3 sets forth the criteria for elevation to Senior Member grade, as follows:

For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE-designated fields. The candidate shall have been in professional practice for at least ten years and shall have shown significant performance over a period of at least five of those years."

***IEEE Designated Fields:***

IEEE-designated Fields include Engineering, Computer Science and Information Technology, Physical Sciences, Biological and Medical Sciences, Mathematics, and Technical Communications, Education, Management, Law, and Policy. Additional information regarding IEEE-designated fields can be obtained by accessing http://www.ieee.org/portal/pages/membership/rep/designatedfields.html. The following paragraphs assist individuals in determining whether they possess the requisite academic credentials or work experience for membership in the IEEE at the grade of Member. Membership at all grades is described in IEEE Bylaw I-104 and can be accessed at http://www.ieee.org/portal/pages/about/whatis/bylaws/index.html.

Member grade requirements include:

- An individual who shall have received a three-to-five year university-level or higher degree in an IEEE designated field, as listed above
- An individual who shall have received a three-to-five year university-level or higher degree from an accredited institution or program
- An individual who has at least three years of professional work experience engaged in teaching, creating, developing, practicing or managing in IEEE-designated fields
- An individual who, through at least six years of professional work experience, has demonstrated competence in teaching, creating, developing, practicing or managing within IEEE-designated fields

Sufficient work experience that can be categorized as being in one or more of the six technical areas is also sufficient for admission or advancement to Member grade. In judging whether education or work experience is relevant to the six technical areas, one critical test is: Does it apply, or is it related to the application of, mathematics, science, or technology for the benefit of humankind?

***Ten Years of Professional Experience:***

The A&A Committee evaluating your application will count the years you have been in professional practice. Your educational experience is credited toward that time as follows:

- 3 years for a baccalaureate degree in an IEEE-designated field as listed above
- 4 years if you hold a baccalaureate and masters degree
- 5 years if you hold a doctorate

***Five Years of Significant Performance:***

Many prospective applicants make the mistake of assuming that "significant performance" requires special awards, patents or other extremely sophisticated technical accomplishments; such is not the case. Substantial job responsibilities such as team leader, task supervisor, engineer in charge of a program or project, engineer or scientist performing research with some measure of success (papers), or faculty developing and teaching courses with research and publications, all are indications of significant performance well as the following:

a. Substantial engineering, responsibility or achievement
b. Publication of engineering or scientific papers, books or inventions
c. Technical direction or management of important scientific or engineering work with evidence of accomplishment
d. Recognized contributions to the welfare of the scientific or engineering profession
e. Development or furtherance of important scientific or engineering courses that fall within the IEEE designated fields of interest.
f. Contributions equivalent to those of (a) to (e) above in areas such as technical editing, patent prosecution or patent law, provided these contributions serve to substantially advance progress in IEEE designated fields.

Significant performance that would serve to qualify an individual for elevation to Senior Member need not have occurred in the years immediately prior to the application. Thus, life and retired members are eligible for elevation.

The following are examples of significant performance that would serve to qualify an individual for elevation to Senior Member. In each case, we are assuming that three qualified references were provided:

**Case 1**. An applicant/nominee has a bachelor's degree and seven additional years of professional experience beyond graduation in an area encompassed by one of IEEE's technical Societies, which meets the requirement of ten years of professional experience. Significant performance can be demonstrated by describing substantial job responsibilities (e.g., team leader) for a period of at least five years. **Result**: All criteria are satisfied and the application is **Approved**.

**Case 2**. Same as Case 1, except that the applicant/nominee worked in industry for one year following graduation with the bachelor's degree and then was a full-time graduate student for two years, obtaining a masters degree. The applicant demonstrates significant performance during another five years in industry. **Result: Approved**

**Case 3**. An applicant/nominee has bachelor, masters, and doctoral degrees in an IEEE-designated field. Five years of significant performance in academia, industry, or government beyond the doctoral degree are demonstrated (e.g., a faculty member with five years beyond the doctorate and promotion to associate professor). **Result: Approved**

**Case 4**. An applicant/nominee has no degree and has worked for many years in the electric industry as a technician. Ten years ago, he accepted an engineering level position and continued with it since that time. Included was a period of at least five years with demonstrated significant performance. **Result: Approved**

**Case 5**. An applicant/nominee retired some years ago and has not been active recently in the profession. Prior to retirement, the applicant/nominee had at least ten years of professional experience, including five years of significant performance. **Result: Approved**.

***References:***

The applicant must also provide three references from *current* IEEE members holding Senior Member, Fellow or Honorary Member grade. Your professional colleagues are your best source of these references. If you have difficulty in locating Senior Members or Fellows to serve as references, please contact your local Section or Chapter for assistance.

The applicant is responsible for contacting his/her references. Referees must send a brief note of recommendation directly to IEEE, preferably using the Senior Member Reference Form. If the applicant is being nominated by a Senior Member or Fellow, TWO OTHER references are required.

Submittal of a reference form does not by itself constitute a nomination. In order for a nomination to be processed as such, the nomination section of the application form has to be filled in, with or without a nominating entity. However, if you wish your Section or Society to receive a rebate of $10 for each successful nomination as part of the Nominate a Senior Member Initiative, the