The Valley Megaphone

Newsletter of the
Institute of Electrical and Electronics Engineers, Inc.
Phoenix Section
October 2006, Volume XX, Number 10

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This Issue of The Valley Megaphone Features:

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Contents:

IEEE Phoenix Section Executive Committee meeting minutes can be found at: http://www.ieee.org/phoenix

Please send announcements for Valley Megaphone to Eric Palmer: ecpalmer@ieee.org.

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The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly and reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.
Advertising Rates: Full page: $200, 3/4page: $125, ½ page: $75, 1/3 page: $50, 1/4 page: $25.
Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: http://www.ieee.org/phoenix

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Phoenix Section Executive Committee Meeting – First Tuesday of the month.

Time: 6:00 pm to 8:30 pm

Place: Phoenix Airport Hilton, 2435 South 47th Street
Phoenix, AZ, 85034
Phone: 480-804-6017

Directions: From 143, exit University Ave, go west, turn right on 47th street.

More Info: Meetings held first Tuesday of month. No meetings in July and August. All interested IEEE members are welcome to attend.

Contact: Rao Thallam, Phoenix Section Chairman, ph: (602) 236-5481 or e-mail: thallam@ieee.org

IEEE GOLD (Graduates of the Last Decade) Phoenix would like to congratulate the graduates of 2006:

- Kevin Schmier, June 2006, BS in Computer Engineering Tech, DeVry University
- Kent Farnswarth, Spring 2006, BS in Electronics Engineering Tech, ASU East
- Aisha Bajwa, May 2006, BS in Electrical Engineering, ASU Main
- Hassan Qasem, Spring 2006, MS in Electronics Engineering Tech, ASU East
- Bo Li, Spring 2006, MS in Electronics Engineering Tech, ASU East
- Arunkumar Ramamoorthy, Fall 2006, Ph.D. in Electrical Engineering-Solid State Physics, ASU Main

Congratulations on your accomplishment, and IEEE GOLD welcomes you to the professional world! We look forward to you being a part of GOLD!

To read about IEEE GOLD: www.ieee.org/gold.

2nd ANNUAL ADVANCED MATERIALS FAILURE ANALYSIS (AMFA) WORKSHOP

TO BE HELD FRIDAY, APRIL 20, 2007
(Following the International Reliability Symposium, SUNDAY-THURSDAY, APRIL 15-19, 2007)

HYATT REGENCY HOTEL
PHOENIX, ARIZONA

AMFA MISSION:
*To serve the interests of failure analysis & materials characterization professionals by providing a forum for the presentation and **active** discussion of timely and pertinent technological issues and trends and to promote the development of new capabilities that fill critical gaps in emerging technologies.*

Unlike traditional conferences that often restrict audience participation, AMFA Workshops provide only top quality invited speakers on leading edge topics, in a format where audience participation is expected and strongly encouraged. Preliminary program details will be available in September, 2006.

Mark your calendars now for this exciting event!

http://www.amfaworkshop.org

15th Topical Meeting on Electrical Performance of Electronic Packaging

EPEP 2006

October 23–25, 2006
Scottsdale, Arizona
Sponsors:
IEEE Components, Packaging and Manufacturing Technology Society
IEEE Microwave Theory and Techniques Society

Call for Papers

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. Authors are invited to submit papers describing new technical contributions in the areas broadly covered below:

- Current and future issues related to on-chip interconnections
- Router friendly models and modeling tools: accuracy & efficiency
- Modeling and design of high speed digital I/O circuits: signal propagation and reception
- On-chip power delivery and regulation
- Advances in modeling core switching noise, and design of novel solutions
- On-chip measurement techniques
- Package analysis, including numerical methods
- Electromagnetic analysis tools
- Advances in transmission-line techniques
- Power distribution and package resonance
- Long distance propagation in large switching complexes
- Switching noise in multi-layered systems
- Macromodeling techniques
- Signal integrity in mixed signal integrated circuits
- Electrical issues in MEMS packaging
- New and innovative interconnect packaging structures and their electrical performance
- RF/microwave packaging structures and their electrical performance
- MMIC modules and high density packaging
- Experimental characterization techniques
- EMC/EMI sources & effects
- Prediction/measurement of radiation from on-chip sources, interconnect structures and packages
- Electrical design implications for low cost, high volume packaging
- Packaging concerns for wireless communication: design and modeling
- Packaging solutions for on-chip radios: design and modeling
- Performance of packaging for automotive radar systems

Conference Co-chairs: Moises Cases, IBM; Paul Franzon, North Carolina State University
Conference Web Page: Detailed information can be found at http://www.epep.org
Paper Submission: Information for authors can be found on the conference web page. Electronic submissions of no more than four pages must be received no later than **July 10, 2006.**
Student Paper Award: Two awards will be presented to the best two papers submitted by students.
Short Courses/Workshops: On Sunday, October 22, 2006, a workshop entitled "Future Directions in Packaging" will be presented and short courses/tutorials will be offered.
Contacts:
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INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.
COMPONENTS, PACKAGING AND
MANUFACTURING TECHNOLOGY SOCIETY
ECTC Components & RF Program Committee
CPMT RF & Wireless Technical Committee

57th ECTC May 29 – June 1, 2007
Reno, Nevada, USA

The CPMT RF & Wireless Technical Committee and the ECTC Components & RF Program Committee encourage you to submit an abstract to ECTC 2007 in the area of passive components & networks, RF and Microwave components and modules and subsystems. ECTC is the premier Electronic Components and Packaging conference held annually and attended by about 1000 delegates with equal participation from companies and academia. As in the past, Components, RF & Microwave related papers are solicited for focus sessions during this prestigious conference.

Passive components

Design, Materials, Processes and manufacturing considerations for discrete passive components- resistors, capacitors, inductors and passive networks

Integrated / Embedded Passives for digital, mixed signal, RF/Microwave applications:

Design, technology, characterization - Embedded passives (inductors, capacitors) for RF/microwave applications & evaluation of their performance in terms of Quality Factor (Q), component value, fabrication challenges & cost

RF and Microwave Components:

Integrated Antennas, filters, baluns, RFID/sensors, RF MEMS, high power and high efficiency RF/microwave power amplifiers – design, technology, new high frequency characterization methodologies

RF and Microwave Modules:

RF/Microwave Packaging techniques & characterization

Module Integration in semiconductor, ceramic, organic or glass substrates for UWB, integrated transceivers for Zigbee, mobile digital TV ---

EMI and innovative shielding techniques for passive components and mixed signal application

SUBMISSIONS:
Please submit abstracts using the ECTC web site: www.ectc.net by October 15, 2006. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the "Components & RF" focused sessions **YOU MUST SELECT**

"Components & RF" committee as your PRIMARY subcommittee preference

when you submit your abstract at the ECTC web site. Again, to have your paper considered for the RF & microwave components sessions, please do the following:

STEP #1: Submit abstract through the ECTC web site (www.ectc.net) and select **"Components & RF" as PRIMARY subcommittee** preference

STEP #2: Email abstract copy and author's email & contact information to: Craig Gaw at c.a.gaw@ieee.org & Mahadevan Iyer at mahadevan.iyr@ece.gatech.edu

Craig Gaw, Chair - CPMT RF & Wireless TC
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Institute of Electrical and Electronics Engineers, Inc.

Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter

&

Waves and Devices Chapter

PRESENT AN ALL-DAY WORKSHOP ON

Convergence in Communication and Computing

Date: Friday, November 17th, 2006 **Time:** 7:00 A.M. – 5:00 P.M.
Location: Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

Abstract

The convergence of mobility, seamless connectivity, and broadband access are the underpinning of next-generation communication systems. Several new applications such as video-conferencing and wireless multimedia are emerging to leverage this capability. Many communication platforms (3G Cellular, WiMax, WLAN, etc.) compete to provide the best solutions for consumer needs in communication, computing and entertainment products. Technology challenges - component through system level - abound for realizing such opportunities at a marketable price point. This one day workshop will bring together experts from industry, academia, government labs, and the financial community to share market visions and to discuss technology issues, options, opportunities and emerging standards. The goal is to provide a comprehensive view of the challenges facing system, device, interconnect and packaging technologies. A panel discussion on the "Future of Convergence in Communications" will bring closure to the day's workshop. Vendors in the entire supply chain will display their products and services throughout the day.

Topics

- Vision – A View of the Future of Convergence
- Market – Current Status and Future Trends
- Business Model
- System and Architecture
- Communication Technology Options and Standards
- Device Technology – RF, Microwave, Analog, and Base Band / Graphic Processing
- Packaging – Mobile Products and Infrastructure
- Antenna / Propagation
- System Integration
- Panel discussion on the Future of Convergence in Communications

Chair: Vasu Atluri (480) 554-0360 **Co-Chair:** Chuck Weitzel (480) 413-

Technical

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For General Information: http://www.ieee.org/phoenix
For Workshop Registration Forms: Sergio Pacheco (480) 413-3737
For Vendor Registration Forms: Vivek Gupta (480) 554-2195

IEEE Region-6 Director-Elect for 2007 – 2008 Election

Submitted by Vasudeva P. Atluri, IEEE Phoenix Section Officer

IEEE is currently in the process of nominating and electing of the officers for the upcoming years. One can find all the information related to the IEEE Elections at the following website: http://www.ieee.org/portal/pages/iportals/aboutus/whatis/bylaws/i-308.html#DE. IEEE Region 6 has nominated two candidates, Dr. S.K. Ramesh and Dr. Leonard J. Bond, for Director-Elect for the two years term, 2007 and 2008, for inclusion on the election ballot for voting by eligible IEEE members from Region 6. IEEE Phoenix Section members are strongly encouraged to take part in the elections by casting a vote. The key information related to election ballots is as follows:

Ballot Submission Schedule: On or before September 1st, 2006, the Board of Directors shall submit to eligible voting members on record as of August 1st, 2006, a ballot listing all nominees for the positions to be filled by election by the membership.

Ballot Marking; Voting; Tellers Committee Announcement; Election Results: Ballots will be valid only when completed in accordance with the instructions accompanying the ballot and when received at IEEE Headquarters or by a qualified organization designated by the IEEE Executive Committee before twelve o'clock noon on the first working day following October 31st (the "final election ballot receipt date"). Ballots shall be validated and votes shall be tallied under the actual or delegated supervision of the Tellers Committee not later than the fifth working day following the final election ballot receipt date. As provided in Bylaw I-306.21, the Tellers Committee shall announce the result of the tally of the votes not later than the eighth working day following the final election ballot receipt date in a report to the Board of Directors signed by the Chair of the Tellers Committee. The results of the vote shall become official upon acceptance by the Board of Directors of the Tellers Committee report, and if applicable the Credentials Committee report. Each nominee for office listed on the ballot and each write-in candidate having votes recorded in such report according to Bylaw I-308.14 shall be advised promptly of the Tellers Committee tally of the votes applicable to their respective elections. Eligible voting members shall be permitted to vote in each election for one nominee for each office appearing on the ballot. Subject to Bylaws I-302.9 and I-306.5, the nominee, for each office for which the election is being held, receiving the greatest number of qualified votes shall be declared elected. In the event of a tie vote, the Board of Directors shall choose between the nominees involved.

The following paragraphs give a brief biography, IEEE contributions, and statements for the two candidates nominated for IEEE Region 6 Director-Elect position.

S. K. Ramesh, Ph.D.
Department Chair/Professor of Electrical and Electronic Engineering
California State University
Sacramento, California, USA
Tel: (916) 278-7955
Email: rameshs@ecs.csus.edu
Website: www.rameshregion6.com

S. K. Ramesh has served the IEEE at the Chapter, Section, Area and Regional levels. Recent recognitions include the 2004 IEEE Region 6 Outstanding Community Service Award and the 2000 Person of the Year Award from the Sacramento Engineering Regional Consortium. The Sacramento Chapter of IEEE LEOS was named the 2005 Most Improved Chapter under his leadership. He is the Counselor of the IEEE CSUS Student Branch which won the 2003 RAB Student Branch Membership Growth Award in Region 6. Dr. Ramesh is active on several Boards including SARTA (www.sarta.org) and McClellan Technology Incubator (www.mtisac.com) which emphasize job creation and foster the growth of the high technology sector in the region. Dr. Ramesh is a Professor in the Electrical and Electronic Engineering Department at California State University, Sacramento and has served as the Department Chair since 1994. He received his PhD degree in 1986 from Southern Illinois University, Carbondale.

IEEE Activities -- (S'80-M'86-SM'93) ***REGIONS****:* Region 6: Operating Committee, 2001-2004; Central Area Chair, 2001-2004; Awards Committee, 2002-2003, Central Area Student Activities Chair, 1994-1995 & 1998-2000; ***SECTIONS:*** Sacramento: Chair, 1992-1993; Vice-Chair, 1991-1992; Secretary, 1990-1991; Membership Development Committee Chair, 1993-1994; Student Activities Chair, 1993-Present. Section Executive Committee, 1990 – 1994 and 2004 – Present. ***SOCIETIES****:* Lasers and Electro-Optics: LEOS Sacramento Section Chapter Chair, 1989-1992 & 2004-Present. ***STUDENT BRANCHES****:* California State University, Sacramento: Student Branch Counselor, 1990-Present; ***CONFERENCES****:* Invited Presentation at IEEE Deans Summit 2003:Fostering Campus Collaborations (www.ieee.org/eab/fcc), Reviewer and Technical Program Committee Member, IEEE International Conference on Communications – ICC 2003 and ICC 2001, Reviewer and Member Program Technical Committee, Optical Networking Symposium, IEEE Globecom 2002, Reviewer IEEE Frontiers in Education Conference, IEEE FIE 2001. ***REPRESENTATIVE***: Region 6 representative, IEEE-USA Committee on Communications and Information Policy, 2005.

***AWARDS**:* IEEE Region 6 Outstanding Community Service Award, 2004. LEOS Sacramento, Most Improved Chapter, 2005-06 and 1991-92; LEOS Sacramento, Largest Membership Growth, 1992-93; CSU Sacramento Student Branch, RAB Membership Growth, Region 6, 2002-03, IEEE CSUS Student Branch, Outstanding Branch Counselor Award, .1999, IEEE CSUS Student Branch, Outstanding Service Award, 1998.

Dr. S.K. Ramesh's Statement:

I have served the IEEE in several leadership roles at the Chapter, Section, Area and Regional levels. I understand the challenges facing the IEEE, and will use my extensive experience working with several organizations, and non-profit boards to serve you effectively.

If elected as the IEEE Region 6 Director I will:

- Strengthen Sections to proactively serve the professional and career needs of members
- Emphasize Strategic Planning, Teamwork and Leadership Development for Section Officers
- Support interactions between IEEE and industry to enhance the profession and support members activities
- Provide prudent fiscal leadership, monitor, evaluate and deliver programs of value to our members
- Present the Region's needs effectively on the Board of Directors
- Enhance awareness of engineering in pre-college students and especially women and minorities

It is an honor and a privilege to be nominated and I would appreciate your vote. Please visit my candidate web site at www.rameshregion6.com for additional information.

Leonard J. Bond, PhD.
Director
Center for Advanced Energy Studies
Idaho National Laboratory
Tel: (208) 526-9150
Email: Leonard.bond@inl.gov
Website: http://CAESenergy.org

Dr. Bond received a Bachelor of Science in Applied Physics (1974) and a PhD in Physics (1978) from The City University, London. He is an expert in ultrasonics. He is a Senior Member, IEEE; Member IEE, Chartered Electrical Engineer (UK); Fellow, Institute of Physics and a Chartered Physicist (UK). He is an Affiliate Faculty at University of Idaho and Idaho State University. He moved to USA in 1990. The posts he held included: Reader in Ultrasonics, University College, University of London; Guest Scientist, NIST, Boulder and Research Professor, University of Colorado, Boulder; Chief Scientist, Denver Research Institute; Laboratory Fellow: Pacific Northwest National Laboratory. He has participated in PNNL Management Skills Development Program (1999-2002). He is received PNNL Exceptional Performance Award 2003 and Battelle Key Contributor Award 2003. He is also a recipient of the IEEE Richland Section, Engineer of the year 2002. He is currently serving as a USA representative in International Electrotechnical Commision (IEC/TC 45) Nuclear Instrumentation working group. He authored or co-authored more than 250 publications and holds 7 patents. Member American Red Cross, Greater Idaho, Leadership Council.

IEEE Activities -- (S'76-A'77, M'92-SM'2005) ***SECTIONS:*** Member Eastern Idaho and previously Richland, WA; Colorado and London (UK). ***COUNCILS:*** Nanotechnology: Administrative Committee, 2002-2004; Publications Committee, 2002-2003. ***SOCIETIES**:* Member, Ultrasonics, Ferroelectrics and Frequency Control (UFFC) since 1976. ***CONFERENCES**:* 3rd Annual IEEE Nanotechnology Conference (IEEE-NANO 2003), Organizing Committee/Publications Committee Chair. ***REPRESENTATIVE**:* Ultrasonics, Ferroelectrics and Frequency Control: UFFC Member Representative to IEEE Nanotechnology Council, 2002-2004. ***AWARDS**:* IEEE Richland Section Engineer of the Year, 2002.

Dr. Leonard J. Bond's Statement:

IEEE Meeting the USA Energy and Workforce Challenges - Fuelling the Future: The US faces unprecedented challenges in delivering secure and affordable energy and it is projected that 40% of US skilled workers could retire within 5 years. The IEEE has a duty and responsibility to better address the energy technology challenges, look towards "post-oil," lead interdisciplinary meetings, present the issues and becoming increasingly engaged in education and workforce supply. My experience in academia, industry and national laboratories, as well as three IEEE regions, gives me a perspective and management experience base that can ensure critical issues are better addressed. A strong and active IEEE Region 6, with growing membership, is needed to move forward into this century in a position of influence. I have been a member of the IEEE for 31 years. Until 12 months ago I was an academic and then a research scientist. I was mostly a user of publications and a conference participant. My current position enables me to now give back to the IEEE, from which I have benefited, and give leadership to address energy, climate change and workforce challenges.

IEEE Senior Membership

Dr. Vasudeva P. Atluri
IEEE Phoenix Section Officer

IEEE Phoenix Section has taken the responsibility for helping eligible IEEE members within the section for getting elevated to IEEE Senior Member grade. IEEE Admissions and Advancement (A&A) committee meets about eight times a year to review and decide on the applications for Senior Member grade. The next two meetings are being held on September 23rd, 2006, in Atlanta, Georgia; October, 2006 (date and location yet to be decided); and November 18th, 2006, in New Orleans, Louisiana. If you meet the requirements for Senior Member grade as listed below, please send your detailed resume including IEEE Member Number, Home Address / Telephone Number / Fax Number / Personal Email Address; Business Address / Telephone Number / Fax Number / Business Email Address; Academic Credentials including starting and ending month for each program; Professional / Work Experience including starting and ending month for each assignment; Publications / Presentations / Patents / Etc.; Honors / Awards; Professional Affiliations / Memberships; Up to Four References Contact Information who are IEEE members; etc. IEEE Phoenix Section will help you with IEEE Senior Member References in case you are not able to find one. Please send your resume in word format to my attention at both vpatluri@ieee.org and vasudeva.atluri@intel.com. The resumes should be received at least six weeks prior to next scheduled IEEE Admissions and Advancement Committee meetings mentioned above for 2006. The meeting schedule for 2007 is not yet decided by IEEE. Additional information regarding IEEE Senior Member grade and IEEE Admissions and Advancement Committee meetings can be obtained by accessing http://www.ieee.org/organizations/rab/md/smprogram.html. The following paragraphs also give a brief summary of the IEEE Senior Member program.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. The benefits of IEEE Senior Membership benefits include:

- The professional recognition of your peers for technical and professional excellence.
- An attractive fine wood and bronze engraved Senior Member plaque to proudly display.
- Up to $25.00 gift certificate toward one new Society membership.
- A letter of commendation to your employer on the achievement of Senior Member grade (upon the request of the newly elected Senior Member.)
- Announcement of elevation in Section/Society and/or local newsletters, newspapers and notices.
- Eligibility to hold executive IEEE volunteer positions.
- Can serve as Reference for Senior Member applicants.
- Invited to be on the panel to review Senior Member applications.

IEEE takes keen interest in encouraging members to get elevated to higher grades for the following reasons:

- Many Executive Volunteer offices require that a member hold Senior Member grade.
- Senior Members provide leadership on a volunteer basis.

- The percent and number of IEEE Senior Members reflects on the competence and prestige of IEEE, its products and services.
- Senior Membership in IEEE is key to Retention:
  - Senior Members have a retention rate of 98%.
  - A greater percentage of Senior Members belongs to more IEEE Societies than do other IEEE member grades.
  - Senior Members volunteer at a higher percentage rate than do other grades of IEEE members.

To qualify for Senior Member elevation, an applicant should meet certain requirements as listed below. IEEE Bylaw I-105.3 sets forth the criteria for elevation to Senior Member grade, as follows:

For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE-designated fields. The candidate shall have been in professional practice for at least ten years and shall have shown significant performance over a period of at least five of those years."

IEEE Designated Fields:

IEEE-designated Fields include Engineering, Computer Science and Information Technology, Physical Sciences, Biological and Medical Sciences, Mathematics, and Technical Communications, Education, Management, Law, and Policy. Additional information regarding IEEE-designated fields can be obtained by accessing http://www.ieee.org/portal/pages/membership/rep/designatedfields.html. The following paragraphs assist individuals in determining whether they possess the requisite academic credentials or work experience for membership in the IEEE at the grade of Member. Membership at all grades is described in IEEE Bylaw I-104 and can be accessed at http://www.ieee.org/portal/pages/about/whatis/bylaws/index.html.

Member grade requirements include:

- An individual who shall have received a three-to-five year university-level or higher degree in an IEEE designated field, as listed above
- An individual who shall have received a three-to-five year university-level or higher degree from an accredited institution or program
- An individual who has at least three years of professional work experience engaged in teaching, creating, developing, practicing or managing in IEEE-designated fields
- An individual who, through at least six years of professional work experience, has demonstrated competence in teaching, creating, developing, practicing or managing within IEEE-designated fields

Sufficient work experience that can be categorized as being in one or more of the six technical areas is also sufficient for admission or advancement to Member grade. In judging whether education or work experience is relevant to the six technical areas, one critical test is: Does it apply, or is it related to the application of, mathematics, science, or technology for the benefit of humankind?

Ten Years of Professional Experience:

The A&A Committee evaluating your application will count the years you have been in professional practice. Your educational experience is credited toward that time as follows:

- 3 years for a baccalaureate degree in an IEEE-designated field as listed above
- 4 years if you hold a baccalaureate and masters degree
- 5 years if you hold a doctorate

Five Years of Significant Performance:

Many prospective applicants make the mistake of assuming that "significant performance" requires special awards, patents or other extremely sophisticated technical accomplishments; such is not the case. Substantial job responsibilities such as team leader, task supervisor, engineer in charge of a program or project, engineer or scientist performing research with some measure of success (papers), or faculty developing and teaching courses with research and publications, all are indications of significant performance well as the following:

a. Substantial engineering, responsibility or achievement
b. Publication of engineering or scientific papers, books or inventions
c. Technical direction or management of important scientific or engineering work with evidence of accomplishment
d. Recognized contributions to the welfare of the scientific or engineering profession
e. Development or furtherance of important scientific or engineering courses that fall within the IEEE designated fields of interest.
f. Contributions equivalent to those of (a) to (e) above in areas such as technical editing, patent prosecution or patent law, provided these contributions serve to substantially advance progress in IEEE designated fields.

Significant performance that would serve to qualify an individual for elevation to Senior Member need not have occurred in the years immediately prior to the application. Thus, life and retired members are eligible for elevation.

The following are examples of significant performance that would serve to qualify an individual for elevation to Senior Member. In each case, we are assuming that three qualified references were provided:

Case 1. An applicant/nominee has a bachelor's degree and seven additional years of professional experience beyond graduation in an area encompassed by one of IEEE's technical Societies, which meets the requirement of ten years of professional experience. Significant performance can be demonstrated by describing substantial job responsibilities (e.g., team leader) for a period of at least five years. **Result**: All criteria are satisfied and the application is **Approved**.

Case 2. Same as Case 1, except that the applicant/nominee worked in industry for one year following graduation with the bachelor's degree and then was a full-time graduate student for two years, obtaining a masters degree. The applicant demonstrates significant performance during another five years in industry. **Result: Approved**

Case 3. An applicant/nominee has bachelor, masters, and doctoral degrees in an IEEE-designated field. Five years of significant performance in academia, industry, or government beyond the doctoral degree are demonstrated (e.g., a faculty member with five years beyond the doctorate and promotion to associate professor). **Result: Approved**

Case 4. An applicant/nominee has no degree and has worked for many years in the electric industry as a technician. Ten years ago, he accepted an engineering level position and continued with it since that time. Included was a period of at least five years with demonstrated significant performance. **Result: Approved**

Case 5. An applicant/nominee retired some years ago and has not been active recently in the profession. Prior to retirement, the applicant/nominee had at least ten years of professional experience, including five years of significant performance. **Result: Approved**.

References:

The applicant must also provide three references from *current* IEEE members holding Senior Member, Fellow or Honorary Member grade. Your professional colleagues are your best source of these references. If you have difficulty in locating Senior Members or Fellows to serve as references, please contact your local Section or Chapter for assistance.

The applicant is responsible for contacting his/her references. Referees must send a brief note of recommendation directly to IEEE, preferably using the Senior Member Reference Form. If the applicant is being nominated by a Senior Member or Fellow, TWO OTHER references are required.

Submittal of a reference form does not by itself constitute a nomination. In order for a nomination to be processed as such, the nomination section of the application form has to be filled in, with or without a nominating entity. However, if you wish your Section or Society to receive a rebate of $10 for each successful nomination as part of the Nominate a Senior Member Initiative, the Section or Society's name must be provided.

October Meeting Announcement for the Phoenix Chapter of the IEEE EMC Society

Date: Wednesday, October 25, 2006
Place: Garcia's Mexican Restaurant at Embassy Suites Hotel
Address: 4400 South Rural Road, Tempe, Arizona
Address: Just South of U.S. 60 on West side of Rural Rd.
Time: 5:30PM Social, 6PM Dinner (order off menu), 7PM Meeting and Presentation
Title: Electromagnetic Compatibility of Integrated Circuits
Speaker: Dr. Flavio Canavero, Professor of Circuit Theory and Electromagnetic Compatibility with the Department of Electronics, Politecnico di Torino

Abstract: In today's technological applications, employing ever faster switching signals, the traditional EMC control at system, PCB and cable level is insufficient. An additional step down in size is needed and the electromagnetic emissions and susceptibility of Integrated Circuits (IC) must be considered to assure the EMC compliance of electronic systems. In addition, the high level of integration of modern devices requires that EMC constraints are imposed in the design phase and that the effects of passive elements (package, interconnects, etc) surrounding the IC are considered.

This presentation is intended to provide an overview of the state-of-the-art techniques available for the assessment of Electromagnetic Compatibility and Signal Integrity of high-speed mixed-signal devices with a high degree of integration. A special emphasis will be given to modeling techniques that can help the designer in the simulation and verification phase. Although this presentation is oriented to Designers and System Engineers, it can also be beneficial for a larger audience, including Managers and anyone responsible for technical specifications of devices used in Information and Communication Technology applications.

About the speaker: Flavio G. Canavero (SM '99) received the Laurea degree in electronic engineering from the Politecnico di Torino, Torino, Italy, in 1977, and the PhD degree from the Georgia Institute of Technology, Atlanta, USA, in 1986. Currently he is a Professor of Circuit Theory and Electromagnetic Compatibility with the Department of Electronics, Politecnico di Torino.

His research interests are in the field of Electromagnetic Compatibility, where he works on field coupling to multiwire cables, interconnect and device modeling for signal integrity, and statistical methods in EMC. He is Editor-in-Chief of IEEE Transactions on Electromagnetic Compatibility, and Chair of URSI Commission E. He has co-authored more than 150 papers in international journals and conference proceedings. He is also a member of the Scientific Steering Committees of several International Conferences, and Organizer of the Workshop on Signal Propagation on Interconnects (SPI; 2001 to 2003. and 2007) and of the 2007 IEEE European Systems Packaging Workshop.

RESERVATIONS: Please call Daryl or Mary at Kimmel Gerke Associates in Mesa AZ at 480-755-0080. (If no answer, please leave a voice mail.) You may also register by email at dgerke@emiguru.com . There is no charge for meetings, but you pay for your own meal and drinks. Since we order off the menu, we do not need an exact number, so if you decide at the last minute, please come anyway. You don't need to be an IEEE or EMC Society member to attend -- all are welcome.

IEEE Computer Society Phoenix Chapter

Speaker: Jerry Crow

Topic: Cryptography 101

Date: Wednesday, October 4, 2006, 6:00-8:30 PM

Location: DeVry University, Room 102, West Dunlap Ave, Phoenix, AZ 85021 (1 mile east of I-17 on Dunlap, SE corner of 22nd Ave and Dunlap). Networking will be in the Courtyard (6-7PM with light meal), presentation at 7PM.

Free, everyone is welcome. Please tell others about this meeting. Cryptography 102 will be presented at a later date.

See the Computer Society website for presentation details at http://www.ewh.ieee.org/r6/phoenix/compsociety

News from the IEEE Education Society, Phoenix Chapter

Chair: Martin Reisslein, reisslein@asu.edu
Co-Chair: Darryl Morrell, Darryl.Morrell@asu.edu

We have the following seminars scheduled for the Fall 2006 semester:

Sept. 22nd, 12-1pm in GWC 409 on ASU Tempe campus
Michael McGarry and Dr. Martin Reisslein:
Title: Toward a Fundamental Understanding of Worked Example Engineering Instruction.

Abstract:
Recent research has demonstrated that worked example basedinstructional designs can effectively foster learning of engineering concepts and are supported by contemporary educational theories, including cognitive load theory. However, a number of interrelated fundamental questions, which have neither been addressed in the educational psychology nor in the engineering education literature, remain open including: (A) What is the impact of means-ends practice? (B) What is the effect of backward vs. forward fading of worked example steps? and (C) What is the effect of adaptivity to learner performance? The goal of the present study was to answer these questions by comparing the learning and perceptions about learning of engineering college freshman who learned how to solve electrical circuit problems in five different computer-based learning conditions: (1) problem solving with step-by-step feedback, (2) means-ends problem solving with total feedback, (3) backward fading, (4) forward fading, and (5) adaptive feedback. Forward fading and adaptive feedback practice promoted more students' near problem solving transfer ability than backward fading practice. Furthermore, the adaptive feedback practice group outperformed students in the backward fading practice group on measures of far problem solving transfer.

Oct. 20, 12-1pm in GWC 409
Dr. Jenefer Husman
Tentative Title: Motivation in Engineering Learning and Instruction

Nov. 17th, 12-1pm in GWC 487
Dr. Andreas Spanias
Tentative Title: JAVA Digital Signal Processing (J-DSP) Editor for Engineering Education

As of this summer we have been able to integrate our seminars into the offerings of the ASU Preparing Future Faculty (PFF) program. Students enrolled into the program complete a curriculum of workshops and seminars on topics related to college teaching and faculty careers. With our seminars as electives in this PFF curriculum we will likely be able to achieve good attendance at our seminar and also increase the relevance of the IEEE and IEEE membership for the PFF students.

IEEE Phoenix Area Consultants Network October Meeting: Financial Reporting for Small Businesses

Date: Thursday, October 12, 2006

Time: Networking begins at 6:30 pm
Dinner begins at 7:00 pm
Program starts at 8:00 pm

Place: Denny's Restaurant
3315 N. Scottsdale Rd. (at Osborn)
Scottsdale, Arizona 85251

Abstract: David Everett will discuss the basics of financial reporting and analysis. Topics will include the difference between cash basis accounting and accrual accounting, the anatomy of the income statement and balance sheet and some practical approaches for small businesses to implement a useful financial reporting system.

David P. Everett, CPA, MBA has over ten year's experience in the audit, financial services, retail, manufacturing and media industries and is currently the Corporate Controller at Village Voice Media, the largest publisher of alternative newsweeklies in the nation.

For more information, contact Vaughn Treude, vaughn@nakota-software.com, or see the IEEE PACN website, www.ieeepacn.com.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

WAVES AND DEVICES
PHOENIX CHAPTER

October 25, 2006 Meeting
www.eas.asu.edu/~wadweb

The Redistributed Chip Package: A Breakthrough for Advanced Packaging

Beth Keser, PhD
Packaging Development Manager
Freescale Semiconductor
Tempe, AZ

Abstract

The Redistributed Chip Package (RCP) is a substrate-less embedded chip package that offers a low-cost, high performance, integrated alternative to current wirebond BGA and flip chip BGA packaging. Devices are encapsulated into panels while routing of signals, power, and ground is built directly on the panel. The RCP panel and signal build-up lowers the cost of the package by eliminating wafer bumping and substrates thereby enabling large scale assembly in panel form. The build-up provides better routing capabilities and better integration. Also, by eliminating bumping, the device interconnect is inherently Pb-free, and the stress of the package is reduced enabling ultra-low K device compatibility. The panel is created by attaching device active side down to a substrate, encapsulating and curing the devices, grinding to desired thickness, and then removing the substrate. Signal, power, and ground planes are created using redistribution-like processing. Multi-layer metal RCP packages have passed -40 to 125C air-to-air thermal cycling and HAST after MSL3/260 preconditioning.

Biography

Dr. Beth Keser received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. in Materials Science and Engineering at the University of Illinois at Urbana-Champaign. Beth's interests are in developing new packaging technology for the semiconductor industry. Her past projects include development of a new wafer level packaging technology; establishing a bondpad redistribution process; invention of photoimageable and non-photoimageable low K dielectrics, thermally resistant foams, and liquid crystalline copolyester substrates for PCB's and MCM's; and phase separated block copolymers as negative acting bilayer resists. Her thesis research as well as undergraduate research resulted in 3 U.S. patents and 13 publications. Currently, Beth is a Packaging Development Manager in the Technology Solutions Organization at Freescale in Tempe, AZ. Beth's work at Freescale has resulted in 2 U.S. patent, 3 pending patents, and 10 publications. Beth has been at Freescale/Motorola for nine years. Besides working in R&D, Beth also spent two years managing the packaging

of all new product introductions created by the business groups at Freescale in Tempe. Beth is also a member of the IEEE CPMT ECTC Advanced Packaging committee, co-chair of the IMAPS Flip Chip committee, and Technical Chair of the IMAPS Device Packaging Conference. Beth has been leading the development of the Redistributed Chip Package (RCP) for over three years.

Date: October 25, 2006

Location: Arizona State University, Main Campus, Goldwater Center (GWC) Room 487
See http://www.asu.edu/map/b2.html for more details.

Time: 6:00-7:00pm Presentation, 7:00pm Dinner (Pizza & soda are being provided by the WAD Phoenix Chapter)
For more information, please call Chuck Weitzel (Chapter Chair) at (480) 413-5906.

IEEE Components, Packaging and Manufacturing Technology Society
Phoenix Chapter
Wednesday, October 18th, 2006 Meeting

Scaling Challenges to Packaging

Dr. Debabrata 'Dev' Gupta
Chief Technical Officer
Advanced Packaging & Systems Technology Laboratories LLC
Scottsdale, Arizona

Abstract

The development of electronic interconnection and packaging have been subservient to device and system trends and so far largely carried out in – house by IDMs as an auxiliary to ongoing progress in device technology. Even flip chip technology, which in its several forms, now finds wide application in advanced packaging, has been in continuous use for high - end systems for over 3 decades. The current high volume implementations of electroplated bump flip chip technology too is an off the shelf reuse of technology already in production in smaller volumes. The next generation of device technology (45 nm etc.) will demand shrinkage in interconnect and packages too, and may require in some cases major modification of now conventional solder bumped flip chip technology in order to overcome material and process limitations. To prepare for that challenge, successful past flip chip development activities e,g. electroplated solder bumps, organic substrates and column bump technologies now in widespread use will be reviewed.

More recently the speakers company has developed and licensed low cost flip chip technologies for applications e.g mobile phone handsets where the high reliability needed for microprocessor packages are not needed. Calibrating the technology by application of science rather than elaborate and expensive statistical experimentation are key to rapid development and implementation.

The next generation of devices will require shrinkage of interconnects too. While bumpless interconnects allow integrated processing they introduce tight coupling of stresses. Many forms of compliant bumps are being considered as an intermediate solution. Scaling down of current flip chip technology pose challenges from interfacial stress, electromigration etc. even if some of the processing issues could be solved. Theory driven modifications to the column bump technology originally developed over a decade ago for GaAs has great potential for silicon covered with weak dielectrics even down to 50 um pitch and will be discussed.

Biography

Over the last 17 years, Dr. Debabrata 'Dev' Gupta has been engaged in the development and implementation of advanced packaging technologies eg. flip chip. He has 9 US patents, many papers and several awards in this area. He has chaired and organized several related conferences, including General Chair for one of the annual workshop of the Phoenix chapter of IEEE – CHMT that he helped to start in 1991. Dev holds a PhD in Materials Science and Mathematics from the University of Arizona, Tucson.

Date: Wednesday, October 18th, 2006

Location: Group Conference Room, Freescale Semiconductor, Inc., 2100 E. Elliot Rd. Tempe, Arizona
Enter the facility through the Main (South) lobby, by the flag poles; you will be escorted to the meeting venue.

Time: 5:30-6:00 Social/Refreshments, 6:00-7:00 Presentation, 7:00 Dinner
(Pizza and Soda are being provided by the IEEE CPMT Phoenix Chapter)

IEEE members and non-members all are welcome to attend. Those who plan to attend should be at the facility entrance no later than 6:00 pm, as there will be no escorts available after that.

For more information please call any of the following officers:

Vivek Gupta (480) 554-2195
Vasu Atluri (480) 554-0360
Vladimir Noveski (480) 554-2375
Debendra Mallik (480) 554-5328
Mali Mahalingam (480) 413-5368
Rao Bonda (480) 413-6121
Daniel Lu (480) 552-2909
Victor Prokofiev (480) 552-0228
Jim Drye (480) 413-3604

IEEE Phoenix Section Annual Banquet 2007
Submitted by Dr. Vasudeva P. Atluri

IEEE Phoenix Section Annual Banquet 2007 is scheduled for Saturday, February 10th, 2006, from 6:00 PM to 9:30 PM. The program consists of:

6:00 PM – 7:00 PM:	Registration and Social Hour
7:00 PM – 8:00 PM:	Dinner
8:00 PM – 8:30 PM:	Keynote Presentation
8:30 PM – 9:30 PM:	Program

At the banquet, IEEE Phoenix Members and Non-Members as well as Corporations are recognized for their outstanding technical and professional contributions. Additional information will be available at www.ieee.org/phoenix website by end of October, 2006. Nominations are sought for awards. Nomination form and instructions for nominating will be available at www.ieee.org/phoenix website by mid to end of October, 2006. Please plan and make effort to attend the IEEE Phoenix Section Annual Banquet 2007. Please bring along a friend or colleague to give them a first hand experience of IEEE Phoenix Section in action. This is a good way of promoting membership. For additional information contact Dr. Vasudeva P. Atluri, Awards Committee Chair, IEEE Phoenix Section at vpatluri@ieee.org.