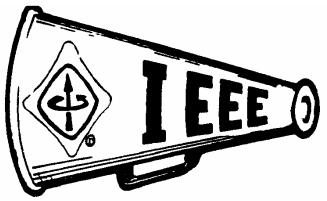
The Valley Megaphone



Newsletter of the Institute of Electrical and Electronics Engineers, Inc. Phoenix Section

May 2006, Volume XX, Number 5

Executive Committee

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Inter-Society Mike Andrews, 480-991-1619 <u>m.andrews@ieee.org</u>

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IEEE Phoenix Section Executive Committee meeting minutes can be found at: <u>http://www.ieee.org/phoenix</u>

Please send announcements for Valley Megaphone to Eric Palmer: <u>ecpalmer@ieee.org</u>.

Executive Committee

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Chapters & Branches

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> Computer Society Cesar A. Vasquez-Carrera cvasquezcarrera@yahoo.com

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GOLD Peter Cioe, 480-441-1702 pcioe@ieee.org

Power Engineering Society Doug Selin, 602-371-6388 douglas.selin@aps.com

> Solid State Circuits Bertan Bakkaloglu bertan@asu.edu

Waves & Devices Society Chuck Weitzel, 480-413-5906 Chuck.weitzel@freescale.com

The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly and reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication. Advertising Rates: Full page: \$200, 3/4page: \$125, ½ page: \$75, 1/3 page: \$50, 1/4 page: \$25.

Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: <u>http://www.ieee.org/phoenix</u>

Student Branches

ASU Main, Engineering Chair: Monir Kahn <u>mmkhan@asu.edu</u> Advisor: Cihan Tepedelenlioglu, (480) 965-6623, Cihan@asu.edu

ASU Main, Computer Society Chair: Prashant Shukla <u>shaukat@asu.edu</u> Advisor: Joseph Urban, 480-965-3374, joseph.urban@asu.edu

ASU Polytechnic Chair: Hassan Qasem hassan.qasem@asu.edu Advisor: Raji Sundararajan, 480-727-1507 Raji@asu.edu

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NAU, Engineering Gabriel Brewer rgb7@dana.ucc.nau.edu Advisor: Phil Mlsna, 928-523-2112 Phillip.Mlsna@nau.edu

> Embry-Riddle, Prescott Chair: Advisor: Chuck Cone <u>conec@erau.edu</u>

Phoenix Section Executive Committee Meeting – First Tuesday of the month.

6:00 pm to 8:30 pm
0.00 pm to 0.50 pm
Phoenix Airport Hilton, 2435 South 47th Street Phoenix, AZ, 85034 Phone: 480-804-6017
From 143, exit University Ave, go west, turn right on 47 th street.
Meetings held first Tuesday of month. No meetings in July and August. All interested IEEE members are welcome to attend.
Rao Thallam, Phoenix Section Chairman, ph: (602) 236-5481 or e-mail: <u>thallam@ieee.org</u>

Message From the Chair

By Rao Thallam



"A Chapter is a technically oriented organizational unit....formed to promote the interests of section members in a specific technical area associated with one or more of the IEEE Societies" Technical Activities Board Operations Manual.

Chapters provide many advantages to members. They offer meetings locally to make technical presentations in a more informal and responsive atmosphere. They can also offer tutorials and workshops. Chapters receive support from the parent societies and the section. Two new chapters are started in the Phoenix Section this year. The

Education Society has a chapter, Prof. Martin Reisslein is the chairman. He can be contacted at: e-mail: <u>resisslein@asu.edu</u>, phone: (480) 965-8593. The Solid State Circuits and Systems Society has a chapter and Prof. Bertan Bakkaloglu is the chairman. His e-mail: bertan@asu.edu, phone: 480-727-0293. More information about these chapters will be published in the Megaphone in the coming months as these chapters elect officers and hold meetings. I wish all the success for these chapters. With addition of these two new chapters, Phoenix Section has eight chapters and two affinity groups.

Congratulations to the officers of the Power Engineering Society Phoenix Chapter for receiving the "High Performing Chapter" Award for 2005 in Region 6. This is great achievement!

I am pleased to announce that Jim Drye is the new Student Activities Chair. Jim was section chairman in 2003 and has significant experience in section operations. He is also very active supporter of the Future Cities Competition and takes leading part in the judging of the competition. Jim can be reached at: jim.drye@fresscale.com and phone: (480) 413-5685

The Region 6 Southwest Area (SWA) Spring 2006 Meeting was held April 8 in University of Nevada, Las Vegas campus. Vasu Atluri, Jim Drye, Ali Movassaghi, Raji Sundararajan, Samir Sharma and Rao Thallam from the Section attended. Vasu is the Area Student Activities Chair for SWA. The student paper contest and micro mouse contest were the main items in the agenda. Ali Movassaghi from the ASU Main Branch presented a paper "Radiation Hardened CMOS Library By Design". He made excellent presentation and won the third place award in the contest. Phoenix Section has not been holding micro mouse contest due to lack of a micro maze. The Student Activities Chair, Jim Drye will be pursuing a proposal to build a micro maze for the section with funding from Region 6. This will help us conduct micro mouse contest for the student branches and also invite participation from high school students.

The Section will be hosting the Southwest Area Fall meeting in ASU on Saturday, October 7, 2006. The main theme will be the training for officers of the chapters and student branches.



May 30 – June 2, 2006 Sheraton San Diego Hotel & Marina San Diego, California

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- Panel Discussion 3D Interconnect
- Plenary Session Packaging Solutions for Future Technologies
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- CPMT Seminar on Advanced Substrate Technologies for SiP / SoP
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Power Engineering SocietyPhoenix Chapter



May 2006 Luncheon Meeting

Date:	Thursday, May 18, 2006
Time:	11:30 am - 12:00 noon: Registration 12:00 noon: Lunch 12:30 pm: Program
Location:	SRP PERA Club <u>(map)</u> 1 E. Continental Dr. Tempe, AZ
Speakers:	Dr. Colin McCullough, 3M Company Juan Gutierrez, Jr., Senior Engineer, T&D Standards, Arizona Public Service Company
Topic:	Uses and Test Results on High Temperature Low Sag ACCR Conductors
Cost:	\$8.00 (Students \$4.00)
Reservation	s:Contact Michelle at (602) 437-0469 or submit your name <u>here</u> . Reservations deadline is Noon Monday, May 15, 2006.

Abstract:

The need to deliver larger amounts of power, with high reliability and performance is a current and pressing requirement of the electric utility industry. Increasing electrical loads, congestion and emergency capacity requirements are creating problems that the transmission grid was never designed to handle. One solution to these challenges is the use of the new generation of high temperature–low sag conductors such as Aluminum Conductor Composite Reinforced (ACCR), which can enable transmission lines to carry up to 2 to 3 times the load of a standard cable, with less sag and few, if any, tower modifications. Aluminum Conductor Composite Reinforced conductor (ACSR) was introduced in the early 20th century. The conductor relies upon a core made from metal matrix composite wires surrounded by high-temperature aluminum wires. This material has been specifically developed for high-temperature overhead conductor applications. The material is as strong as steel with lower electrical resistance and a coefficient of thermal expansion less than steel or aluminum. ACCR can be installed as a replacement conductor on existing right-of-ways, with little or no modifications to existing towers or foundations. This additional capacity and increased efficiency, permits the

upgrade of transmission capacity with minimal environmental impacts, avoiding difficult and lengthy permitting and reduced outage times. The new conductor can help solve transmission bottlenecks, especially restricted power flows associated with operating lines at high temperatures Test facilities have performed a wide range of field and laboratory testing and have collected, analyzed and published extensive data on the conductor and accessories. Several U.S. utilities have installed and are operating ACCR on transmission lines in their networks. These field installations cover a variety of geographic and wind and ice loading areas including areas with heavy ice loading and lines experiencing very high current loads. The presentation will review the testing and qualification of ACCR conductors and report on a recent commercial application and installation in the Phoenix area.

Biographies:

Dr. Colin McCullough is a Materials Scientist at 3M with over 20 years experience in composite materials. Dr McCullough is the lead scientist associated with the testing, qualification and commercial applications of ACCR conductors for overhead transmission. He has written over 30 articles and holds 12 patents. Juan Gutierrez, Jr. is a Graduate of New Mexico State University. He has been working with Arizona Public Service Co since 1985. Juan has worked in T&D Engineering and Standards for 19 years with various material responsibilities, including wire and cable.

Phoenix Area Consultants Network Annual Picnic

In May, the PACN will hold its annual picnic in lieu of our usual Thursday-night meeting. This is a social gettogether and non-members are welcome to come for fun and informal networking.

Date: Saturday, May 13, 2006

Time: Picnic starts around 2 PM

Food served around 4 PM

Place: Lane Garret residence 8502 E Cactus Wren Rd

Scottsdale, Arizona 85250

Food: We will provide burgers and hot dogs, sodas, plates, utensils, etc. Please bring one pot-luck dish such as a casserole, salad, or dessert.

Please RSVP to vaughn@nakota-software.com

Directions: From east loop 101, take the Indian Bend Road exit and head west. Turn left (south) at 86th street, then right (west) on Cactus Wren Road. Lane's home is on the NE corner of 85th and Cactus Wren.
From Scottsdale Road, turn East on Indian Bend Rd. Cross over Hayden Rd., continue east on Indian Bend Rd. and turn south on 84th St. which dead-ends into Cactus Wren. Go left on Cactus Wren one block.



INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS WAVES AND DEVICES PHOENIX CHAPTER

May 17, 2006 EDS Meeting www.eas.asu.edu/~wadweb



Signal Integrity: A Process/Device or a Design Challenge?

Radu Secareanu Freescale Semiconductor

Abstract

Since the invention of the semiconductor device, the imagination of scientists from a broad range of multidisciplinary fields has been the source of a continuous and fast-paced progress. Now, more than ever, developing a solution to a challenge requires multiple points of view. Now, more than ever, complex and diverse functionality is crammed on one common semiconductor substrate, while the quest for high-performance and low-cost is unprecedented. Gigahertz range RF circuits, high-accuracy A-to-D converters, high-speed digital processing units, and high-capacity memories must coexist on-chip with minimal interaction in order to preserve uncompromised functionality of the mixed-signal system.

Some of the aspects with impact on the interaction between various on-chip functional blocks comprising a mixed-signal system are being reviewed in this talk. During operation, an active semiconductor device generates noise. A device typically requires a substrate contact in its vicinity for such reasons as latch-up prevention. A substrate contact is tied to power/ground lines, which, together with the package, feature RLC parasitics. The RLC parasitics, in connection with the circuit operation, generate more noise. To overcome this positive loop for noise generation, one solution is to develop quieter devices together with materials featuring low RLC parasitics. Alternatively, develop process solutions to alleviate the noise, such as triple-wells and low-doped substrates. One step higher, the physical design in direct relationship with process options help in reducing the noise levels by employing such techniques as metal shields and substrate rings. The noise challenges however accentuate with the increase in circuit performances and technology advances. Circuit design solutions for noise reduction must be employed, methodologies for noise reduction such as the use of decoupling capacitors must be developed in order to reduce the noise gap. In this never-ending race, the imagination of scientists in multiple fields such as materials, devices, process, and design is the ultimate limit towards progress.

Dr. Radu Secareanu is with Freescale Semiconductor (formerly Motorola SPS) since 2000 as a member of the Technology R&D Organization, currently a senior member of the Microwave and Mixed-Signal Technologies Laboratory. Since 2002 he is also an adjunct professor in the EE Department at Arizona State University. Radu got his Ph.D. in 2000 from the University of Rochester, previously working for five years as a design R&D engineer. His current research interests are in signal integrity (substrate, interconnect, power-ground network) and the relationship with new technologies and mixed-signal and RF circuit design aspects, and low-voltage and low-power circuit design. He authored and co-authored over thirty referred papers, and five issued and several pending patents. He is an IEEE member, served in several conference committees at various levels, presented several conference tutorials and invited talks, served as IEEE-TVLSI Associate Editor, and is actively involved in SRC activities.

Date: May 17, 2006

Location: Group Conference Rm, Bldg 94, Freescale Semiconductor, 2100 E. Elliot Rd., Tempe, AZ Use Freescale Main Entrance (South) facing Elliot Road

Time: 2:30-3:45pm Seminar

For more information, please call Chuck Weitzel (Chapter Chair) at (480) 413-5906.

IEEE Computer Society Phoenix Chapter

UPCOMING MEETING

Speaker: Dan Houston

Date: Wednesday, May 3, 2006, 6:00-8:30 PM

Location: DeVry University, Room 102, West Dunlap Ave, Phoenix, AZ 85021 (1 mile east of I-17 on Dunlap, SE corner of 22nd Ave and Dunlap). Networking will be in the Courtyard (6-7PM with light meal), presentation at 7PM.

Free, everyone is welcome. Please tell others about this meeting.

Spelunking Tools – Estimation Techniques for Software Projects

All too often, software project estimation feels like peering into a dark cave, guessing at its size, and hoping for the best. We don't know how big the cave is, where it goes, or how far it goes. Nonetheless, we announce its dimensions before crawling in and exploring. In this session, we will discuss tools for sizing up caves before plunging into them.

Dan Houston works on metrics and estimation issues in the Honeywell Aerospace Software Center of Excellence. His research and practical interests are in quantitative software engineering. His publications include papers on cost of software quality, software process modeling and simulation, Six Sigma and software process improvement, and software project risk factors. Dan is an IEEE Senior Member.

NEXT MEETING

Speaker: Jerry Crow, GIAC/GSEC, Network Engineer with EDS Date: Wednesday, October 4, 2006, 6:00-8:30 PM Location: DeVry University Topic: Cryptography/Encryption For more information, contact <u>c.vasquez-carrera@computer.org</u>

VOLUNTEERS NEEDED

IEEE Computer Society Phoenix Chapter needs a:

- 1) <u>Webmaster</u> (to update our website 8 times a year, needs to have MS FrontPage or equivalent, PDF Acrobat Reader/Writer, and a way to FTP and access our website www.ieeecs.com)
- 2) <u>Secretary</u> (to submit meeting attendance online to IEEE Headquarters via L31 reports and maintain the Phoenix Chapter email distribution list.)

We meet October through May at DeVry University in Phoenix (8 mtgs/yr).

Your volunteer work will be rewarding.

Any help will be greatly appreciated.

For more info, contact c.vasquez-carrera@computer.org



IEEE Components, Packaging and Manufacturing Technology Society Phoenix Chapter Wednesday, July 19th, 2006 Meeting

Optoelectronics is Again Vibrant and Penetrating Many New Markets...

Dr. Michael Lebby President and Chief Executive Officer (CEO) Optoelectronics Industry Development Association (OIDA) Washington, DC, USA

Abstract

The OIDA perspective on the global optoelectronics markets and technology vectors will be reviewed in this presentation. In particular, the talk will give the OIDA view on the global HBLED, laser diode, communications, solar cell, image sensor and display industries with major technological trends. The talk will include technology roadmaps, applications and future opportunities. In particular the talk will give an update on the results from OIDAs 2006 roadmap forums on artificial vision, high power lasers and nitride based materials. In addition, the talk will discuss the upcoming roadmap forums on 100Gbps data-rates, silicon photonics and optoelectronic packaging & miniaturization for that will be held later in 2006.

Biography

Dr. Michael Lebby received his D. Eng., Ph.D., MBA and B. Eng. (Hons.) from the University of Bradford, England in 2004, 1987, 1985 and 1984, respectively. More recently, Dr. Lebby received an honorary Doctorate (D. Eng) by the University of Bradford in 2004 for his contributions to the field of optics, optoelectronics, and fiber optic packaging. Since 1977, he has been employed by the British Government, AT&T Bell Laboratories, Motorola, and AMP (now Tyco) in senior technical and business optoelectronic and fiber optic roles. In 1999, Dr. Lebby joined Intel as a venture capitalist and was instrumental in a number of private equity deals in optoelectronic components and networking. In 2001 he founded a new fiber optics company, Ignis Optics, where he served as CEO and Board member. He successfully raised two rounds of financing (with step-ups) that exceeded \$30M during 2001 (also in risk adverse environment) and the company was subsequently acquired by Bookham Technology in October 2003, where he was responsible for corporate and technical strategy. Dr. Lebby is now the president and CEO of OIDA (Optoelectronics Industry Development Association) based in Washington DC. He is growing OIDA into a stronger marketing, technology, and governmental body for its membership. OIDA is known for its technology roadmaps, workshops, industry networking, and government policy. Dr. Lebby frequently provides tutorial lectures, speeches, and courses to senior executives on the dynamics, both economically and technologically, on the optical networking environment. He also advises at the Board level at a number of optical component start-ups in both Europe and the United States. A Fellow of IEEE, Dr. Lebby also holds more than 170 issued US patents and has published and presented regularly in the optoelectronics field. Including international issued (over 57) and pending patents (over 39), the number totals well over 250.

Date:	Wednesday, July 19 th , 2006
Location:	Group Conference Room, Freescale Semiconductor, Inc., 2100 E Elliot Rd. Tempe, Arizona
	Enter the facility through the Main (South) lobby, by the flag poles; you will be escorted to the meeting venue.
Time:	5:30-6:00 Social/Refreshments, 6:00-7:00 Presentation, 7:00 Dinner
	(Pizza and Soda are being provided by the IEEE CPMT Phoenix Chapter)
IFFF members	and non-members all are welcome to attend. Those who plan to attend should be at the facility entrance no later than

IEEE members and non-members all are welcome to attend. Those who plan to attend should be at the facility entrance no later than 6:00 pm, as there will be no escorts available after that.

For more information please call any of the following officers:

Vivek Gupta (480) 554-2195	Debendra Mallik (480) 554-5328	Daniel Lu (480) 552-2909
Vasu Atluri (480) 554-0360	Mali Mahalingam (480) 413-5368	Victor Prokofiev (480) 552-0228



THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, I



IEEE Components, Packaging and Manufacturing Technology Society Phoenix Chapter Wednesday, May 17th, 2006 Meeting

Power Delivery Trends & Challenges for High Performance Microprocessors

Dr. Kaladhar Radhakrishnan Manager – Assembly Technology Development Intel Corporation Phoenix, Arizona

Abstract

Intel and the rest of the semiconductor industry have relied on Moore's law to provide them with an exponentially increasing transistor count that powers today's high performance processors. However, as the transistor count goes up, so do the power delivery challenges. The increasing transistor count coupled with faster switching speed leads to higher current consumption. Conversely, as the device dimensions get smaller, the die voltage has been scaling down to meet the oxide reliability requirements. These two trends combine to yield a power delivery impedance target that is fast approaching sub-milliohm levels. Another by-product of the reduction in the device dimensions is the increase in leakage power. Today's transistors start conducting current even when they are turned off and if left unchecked, the leakage power would soon exceed the active power consumption. One way to combat the leakage power issue is by slowing the frequency growth. With a reduced emphasis on the processor frequency, the process parameters can be tweaked to reduce leakage current at the expense of transistor switching speed. With frequency no longer being the primary knob for improving the processor performance, system architects have turned to other avenues in an effort to improve the overall performance. One example of this is the switch to multiple cores. By adding an extra logic core and reducing the switching frequency, the processor can get a performance boost without a significant power penalty.

Biography

Dr. Kaladhar Radhakrishnan received his BE, MS, and Ph.D. in Electrical Engineering from Coimbatore Institute of Technology, Iowa State University and University of Illinois at Urbana-Champaign respectively. His primary area of specialization for his dissertation work was in Computational Electromagnetics. He joined Intel in 2000 soon after finishing his Ph.D. to work on power and signal distribution problems. His primary area of focus is in enabling power delivery solutions for high power microprocessors. Kaladhar holds multiple patents in the area of design and assembly of microprocessors. Kaladhar is also an active participant in the research community and has over 30 journal and conference publications. He currently manages the Electrical Core Competency team within the Assembly Technology Development organization. Kaladhar can be reached at kaladhar.radhakrishnan@intel.com.

Date:	Wednesday, May 17 th , 2006
Location:	Group Conference Room, Freescale Semiconductor, Inc., 2100 E Elliot Rd. Tempe, Arizona Enter the facility through the Main (South) lobby, by the flag poles; you will be escorted to the meeting venue.
Time:	5:30-6:00 Social/Refreshments, 6:00-7:00 Presentation, 7:00 Dinner (Pizza and Soda are being provided by the IEEE CPMT Phoenix Chapter)
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Vivek Gupta (480) 554-2195 Vasu Atluri (480) 554-0360 Vladimir Noveski (480) 554-2375 Debendra Mallik (480) 554-5328 Mali Mahalingam (480) 413-5368 Rao Bonda (480) 413-6121 Daniel Lu (480) 552-2909 Victor Prokofiev (480) 552-0228 Jim Drye (480) 413-3604

IEEE GOLD Phoenix Chapter www.ieee.org/gold-phoenix

Topic Summary:

Consider a world no longer restricted by lines and cords. The future of telecommunications and networking is total wireless access solutions.

It is one seamless, total communications experience. "Anytime, Anywhere Broadband" Ryan McCaigue, Director of Network Engineering for the Tempe WiFi Network, will discuss Metro Scale WiFi Networks from an engineering and municipal planning perspective.

Speaker: Ryan McCaigue, Director of Network Operations

Prior to joining NeoReach, McCaigue held the position of Dean, Network and Communication Management and Business for DeVry University's Phoenix campus, where he implemented the new degree program in Network and Communications Management and established the "knowledge management task force" creating a searchable resource repository and consolidating course design efforts across 23 campuses nationwide. His collaboration with industry leaders including Microsoft, Intel and Cox Communications determined future technology needs, ensuring parallel between curriculum and corporate objectives.

About NeoReach:

NeoReach is a wholly-owned subsidiary of MobilePro delivering wireless broadband and voice services to our end-user customers. We are focused on growing our current customer bases, developing and deploying wireless technologies, acquiring and growing profitable telecommunications and broadband companies and forging strategic alliances with well positioned companies with complementary product lines and in complementary industries.

We are also an innovator and developer of wireless broadband networks and services. Our wireless broadband networks and services will be provided in our Wireless Access Zones (WAZ) to be primarily located in municipality sponsored areas. These network systems are scalable and flexible and will be readily modified to offer a variety of broadband services.

Date: Thursday June 8th, 6:30pm Location: ASU Memorial Union (Room TBA)

For updated info see website <u>www.ieee.org/gold-phoenix</u> Or e-mail <u>pcioe@ieee.org</u> or Christy.Pack@gdc4s.com



Mobilepre

